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The growth and  
evaluation  
of epilayers grown  
by

**TITLE .....** Silicon Molecular Beam Epitaxy. ....

**AUTHOR** ... Richard F. Houghton

**DEGREE .....**

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The growth and  
evaluation  
of epilayers grown  
by  
Silicon Molecular  
Beam Epitaxy.

by Richard F. Houghton

UNIVERSITY OF WARWICK 1991

Thesis submitted in  
partial fulfilment  
of the requirements of the  
degree of PhD.

Declaration:

The material presented in this thesis is entirely the  
work of the author unless explicitly stated otherwise in the  
text.

*To put aside hints and speak plainly, and dealing with science as a method of demonstration and reasoning capable of human pursuit, I hold that the more this partakes of perfection the smaller the number of propositions it will promise to teach, and fewer yet will it prove. Consequently the more perfect it becomes, the less attractive it will be and the fewer will be its followers. On the other hand magnificent titles and many grandiose promises attract the natural curiosity of men, and hold them forever involved in fallacies and chimeras without ever offering them one single sample of that sharpness of true proof by which the taste may be awakened to know how insipid is its ordinary fare.*

*Galileo, 1623.*

**Dedication.**

**To my mother, and to my father who never did  
see the fruition of my labours.**

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**RFH**

**Oakham, 1991.**

### Abstract.

The aim of this work was to evaluate and improve the quality of epilayers grown by silicon molecular beam epitaxy (Si-MBE).

The first thorough study was carried out on substrate preparation, specifically aimed at the unique conditions that arise during MBE growth. This included both ex-situ wet chemical cleans, and by in-situ thermal desorption with the aid of Si evaporation to remove surface oxide. This enabled the development of a low thermal budget cleaning technique which ideally complemented the low growth temperatures attainable during MBE, one of the technique's major advantages. This cleaning method consisted of ex-situ oxide removal in 2.5% HF solution, followed by in-situ thermal treatment at 700°C for 7 minutes with the aid of a 10Å capping layer.

The dependence of residual doping on growth parameters, and the electrical and optical properties of residually doped epilayers were studied in detail for the first time. Knowledge of these factors is vital for the design of devices in which the carriers are separated from the ionised impurities that give rise to them. The background dopant was identified as phosphorus.

The effect of substrate temperature on chemical purity and crystalline perfection was then studied to determine the optimum temperature for growth. The presence of electrically active traps was analysed by deep level transient spectroscopy, and their concentration was found to fall to a minimum above 600°C. Conversely, crystalline perfection, as determined by a defect revealing etch, was found to increase as temperature decreased, reaching a optimum between 500° and 600°C for the growth rates available during this work.

The use of Ga and B as p-type dopants in Si-MBE was studied. The deficiencies of Ga as a dopant in MBE were explored and explained. To overcome boron's only major weakness, its low vapour pressure, a novel elemental B coevaporation source was designed and constructed, which has now been universally adopted as the method of B coevaporation for MBE. This allows contamination free doping with an industry-standard dopant that exhibits excellent electrical properties. A new model for the incorporation enhancement seen with some dopants during the use of the technique known as potential enhanced doping (PED) is also proposed, involving the incorporation of atoms at damage sites caused by impinging Si<sup>+</sup> ions. Computer modelling illustrated the feasibility of the hypothesis compared to secondary implantation, until now the most widely used model.

The development of the new elemental B source enabled the author to grow the first successful p-type atomic layer ( $\delta$ ) doped epilayers. These had considerable advantages over their n-type, Sb-doped counterparts, due to B's more appropriate incorporation kinetics.

## Chapter 1. Introduction.

### 1.1 An overview of MBE.

Silicon Molecular Beam Epitaxy [Si-MBE] is a vacuum evaporation technique in which Si atoms are made to impinge upon a heated, single crystal Si substrate. Under correct evaporation and vacuum conditions a single crystal epilayer grows. The method was first tried in the early 1960's <Unvala, 1962>, but initially crystal quality was extremely poor, and greatly inferior to the widely used technique of Chemical Vapour Deposition [CVD]. It was demonstrated by Joyce et al. (1969) that the poor crystallinity of such layers was due to inadequate substrate cleanliness and  $\text{SiO}_2$  or  $\text{SiC}$  precipitates which were present on the substrate surface during epitaxy, and caused three dimensional growth to occur. However, with the improvements in ultra-high vacuum [UHV] technology, pressures between  $10^{-10}$  and  $10^{-11}$  Torr became readily achievable, thus giving a low enough residual gas ambient, which along with improved substrate preparation enabled growth of high quality Si epitaxial films.

In 1977 the first Si-MBE epilayers with reasonable material quality and bulk-like properties were reported <Becker & Bean, 1977, Ota, 1977>. The studies involved doping work carried out using Ga, Al and Sb from coevaporation sources, and showed that sharp dopant profiles could be obtained over a reasonably wide dynamic range ( $10^{15}$ - $10^{18}\text{cm}^{-3}$ ). These experiments were carried out using small, resistively heated,

rectangular substrates. However, with the growth of interest and expertise in Si-MBE, and with the need for greater through-put, systems have become larger and more complex, and can now use standard substrates of up to six inches in diameter <Kasper et al, 1988>.

The basis behind the technique is that Si is melted and evaporated under UHV conditions, thus allowing molecular flow, such that the flux arrives at a Si substrate held above the epitaxial temperature. This temperature is dependent on growth rate, but generally between 450-900°C. At temperatures below this, poor crystallinity is observed, since Si atoms arriving at the surface have insufficient energy to incorporate at lattice sites, and a disruption in epitaxial growth results. For epitaxy to occur, growth must be two-dimensional, with incorporation occurring at growth 'steps' which migrate across the surface. The nucleation point for these steps occurs since the substrates are unintentionally cut slightly off the crystal axis, causing lattice planes to terminate at the surface.

Si has a relatively low vapour pressure and high melting point, and so conventional thermal evaporation is unsuitable for the high fluxes required. Instead an electron beam evaporator is used, in which a high energy (8keV) electron beam from a non-line-of-sight tungsten filament is accelerated, focused and scanned across a Si source charge. Only the central portion of this charge becomes molten as it sits in a water cooled copper hearth. This means that the charge provides its own crucible of solid Si to contain the

molten portion of the charge. This is vital since molten Si reacts with all standard crucible materials <Bean, 1981>.

The major advantage of MBE over other device fabrication techniques such as diffusion, ion implantation and conventional CVD is the ability to obtain extremely sharp doping transitions (<100Å/decade)<Kubiak et al, 1984>. Doping can be instantaneously started and stopped, and the growth temperatures normally employed (550-700°C) mean that solid state diffusion is negligible. This allows the synthesis of complex structures such as superlattices or quantum well devices without the smearing of profiles by the diffusion process and also eliminates auto-doping effects from the substrate, a common problem in CVD work.

Doping of the epilayer is carried out during growth either by coevaporation or ion implantation. Initially, dopants commonly used for coevaporation in Si-MBE were limited to Ga and Sb due to their convenient vapour pressures and incorporation kinetics. In and Al have also been tried, but abrupt transitions were found to be impossible due to surface segregation, i.e. the tendency of atoms to preferentially collect at the growing surface rather than remain incorporated in the lattice. More recently, phosphorus doping from a SnP source has been demonstrated <Kubiak et al, 1986>, the compound source being used to reduce the control problems caused by the high vapour pressure of elemental phosphorus.

A major advance in p-type doping was made when elemental B doping was first realised <Kubiak et al, 1985>. B

has a low vapour pressure, which means that a standard, radiatively heated Knudsen-type MBE source cell cannot be used due to its temperature limitations. Evaporation from a resistance-heated Ta foil cell showed that B has excellent incorporation behaviour:- unity sticking coefficient (i.e. all the incident flux is incorporated), 100% activation, high solid solubility limit ( $>10^{20}\text{cm}^{-3}$ ), with negligible vacuum degredation due to the high cell temperature (~1600°C). Compound B sources such as HBO<sub>2</sub> and B<sub>2</sub>O<sub>3</sub> have been used to lower the required cell temperatures, but surface segregation and oxygen incorporation have both been noted <Tuppen et al, 1988>.

Another development in coevaporation was the discovery of the effect known as potential enhanced doping (PED). When a negative bias is placed on the substrate during growth it has been found that incorporation of dopants can be greatly enhanced. This is especially true for Sb, where a bias of -1200V can increase carrier concentration by nearly three orders of magnitude. The mechanism for this is thought to be interaction between atoms in the adlayer of dopant that forms at the growing surface and Si<sup>+</sup> ions produced by electron impact ionisation caused by the electron beam evaporator. Since this method does not rely on the adlayer equilibrium being disturbed during or after doping, as would be the case with shuttering, very abrupt doping transitions can be achieved using PED as a method of profile control. A new interpretation of PED is proposed in Chapter 6.

Low energy implantation during growth has also advanced since its inception. Initial experiments <Ota, 1980><Bean & Shadowki, 1982>, required high substrate temperatures to ensure adequate annealing of ion damage, but recent work has shown ion doping at temperatures as low as 450°C <Houghton et al, 1988>. The major advantage of ion doping is the control and reproducibility of the doping levels that can be readily achieved, since incorporation does not exhibit the exponential substrate and cell temperature dependences nor surface segregation of most coevaporated dopants; instead an ion current can be chosen that will give a known doping level at a given rate. However, the difficulty in producing high enough ion currents at such low energies (<1kV) means that low growth rates must be used to achieve maximum doping levels <Ota, 1980>. Ion doping also involves costly and complex equipment.

Despite the fact that Si-MBE has now been quite extensively researched, little work has been carried out into the material aspects, most interest having been focused on doping structures and their characterisation. However, now that high quality doping can be achieved it has been found that material quality is inadequate for the majority of commercial uses. There is little point in growing and processing a 100A period multilayer structure for mobility studies if defects prevent proper contacting, and unintentional impurities cause soft breakdown of interface junction isolation!

Much of this project has therefore been aimed at studying some of the basic properties of MBE-grown silicon and attempting to improve them primarily by reducing contamination due to the MBE process and by adjustment of the MBE growth parameters. Chapter 2 gives an introduction to the system technology of MBE, and describes the changes made by the author to optimise it for growth of Si. The effects of some basic parameters have been studied in detail for the first time. It has long been known that UHV epitaxy is extremely sensitive to substrate cleanliness, and so this work presents a study of both *in-situ* and *ex-situ* substrate preparation in Chapter 3. In Chapter 4 the effect of another basic parameter, substrate temperature ( $T_S$ ), has also been carefully examined to observe its influence on crystalline, electrical and optical properties of MBE Si. The characteristics of the simplest epilayers, that is undoped material, were also studied in an attempt to better understand the MBE process and the properties of the layers grown and the results are discussed in Chapter 5. Also the problems of p-type doping have been addressed in Chapter 6 to try to enable growth of doped material with optimum electrical properties. The weaknesses of Ga doping are discussed, as is a new elemental boron cell design, which has led to the first ever B delta doping, as is explained in Chapter 7.

## Chapter 2. System technology.

### 2.1 Basic configuration.

The Si-MBE system used for this work was a VG Semicon V80 system, similar to that originally designed for III-V MBE, housed in a class 10,000 cleanroom to ensure adequate system and substrate cleanliness. The system consisted of three separate chambers (see Fig 2.1), substrates entering the machine via a load-lock, which was pumped down to UHV by successive use of rotary, sorption and ion pumps. The second chamber, pumped by a 1000l/s cryopump, was designed for in-vacuo substrate preparation, and contained several cleaning (thermal, Fast Atom Bombardment) and analysis (Auger) stages. In this study, this part of the system was used solely as a transition chamber, as any extra processing prior to epitaxy was found to be detrimental. The main chamber of the system was that used for deposition. Pumped by a 1000l/s cryopump and supplementary 400l/s ion pump, this chamber contained the e-beam evaporator for production of the Si flux, dopant cells (usually one n-type and one p-type), a substrate heater stage, a quadrupole mass spectrometer for residual gas analysis, and a deposition monitor/controller [Inficon Sentinel III] <Googl & Reagan, 1983> to measure the Si flux and control the e-beam evaporator. Cryopanels, which prevented radiative heating of the walls of the chamber and acted as a secondary pump,

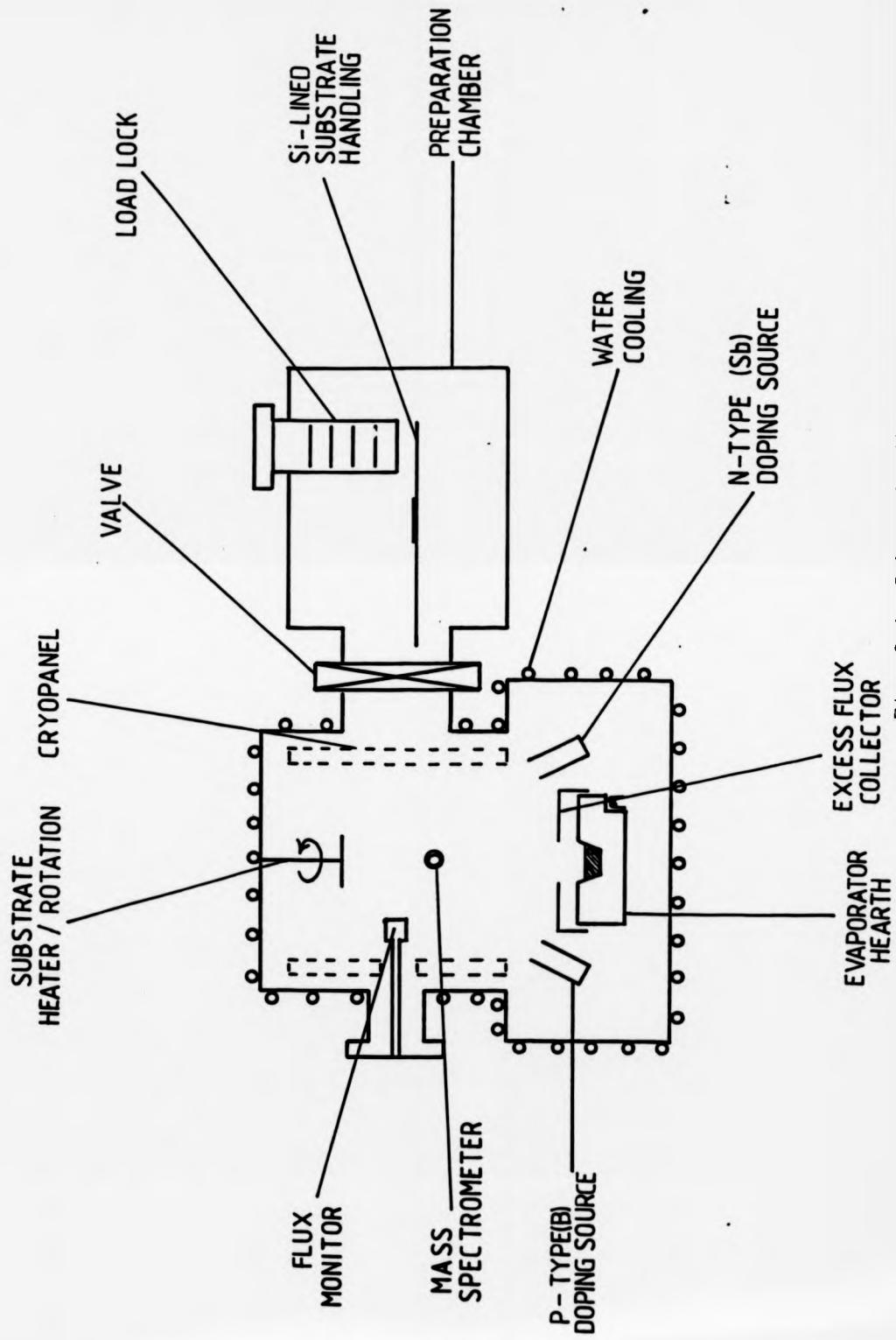


Fig. 2.1 Schematic diagram of the V80 system modified by the author for this study.

were also used for part of this study, until they were replaced by external water cooling.

The system was configured for handling three inch wafers, which could be loaded in batches of four by means of a magazine inserted into the load-lock. Epilayer growth was achieved by evaporating Si from the e-beam evaporator in which the central portion of the Si charge was heated by a stream of 8kV electrons deflected through 270° from a tungsten filament by magnets in the water cooled copper e-gun hearth (see Fig. 2.2). This method meant that the molten Si was held within a solid Si crucible made by the portion of the charge not receiving any electron flux (molten Si reacts with all normal crucible materials <Bean, 1981>). The 270° deflection angle also meant that the filament was not in line of sight to the substrate. The evaporated Si impinged upon a substrate which was radiatively heated during growth by a Ta ribbon heater, so that incident atoms, once on the surface, would have sufficient thermal energy to attain lattice sites.

## 2.2 Modifications.

During these studies several novel modifications were made to the V80 MBE system by the author to try to improve the performance of the machine. As mentioned earlier, the large cryopanel originally in the growth chamber was removed and water-cooling, consisting of 5cm pitch, 1/4in diameter stainless steel tubing, welded around the outside of the

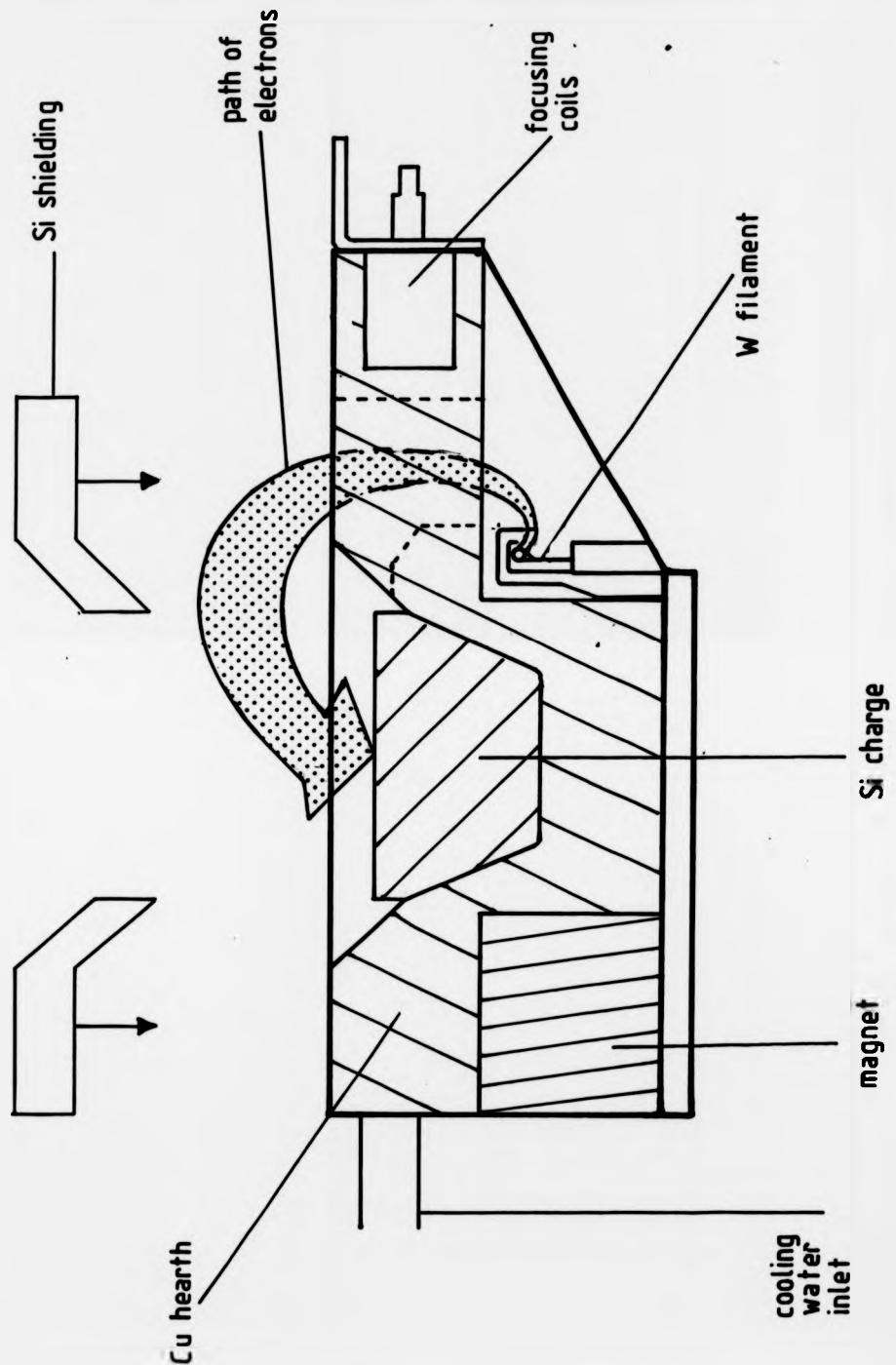


Fig. 2.2 Schematic diagram of electron beam evaporator hearth (Airco Temescal Model SFIH-270-2), illustrating the path of the deflected electrons. Si shielding was installed by the author to minimise Cu contamination from the hearth.

chamber. The reasons for doing this were two-fold: firstly to avoid Si forming flakes on the cryopanel (a stable deposit cannot form due to the thermal cycling that the panel regularly undergoes), and secondly there was concern about electron assisted desorption of hydrocarbons from cryopanels, caused by stray electrons emitted from the e- gun filament or reflected from the source charge. This design modification was not without its disadvantages though, as inevitably some parts of the chamber walls became warmer than with cryopanel cooling present. The water cooling did, however, prove to be very effective, the majority of the chamber being held at approximately 16°C at the exterior surface with the e-gun and substrate heater running (the input water temperature was 11°C). The hottest part of the system reached approximately 30°C, this local heating being due to the absence of cooling around an inaccessible flange. The effect of this change on background doping is discussed in Chapter 4. A small cryopanel in the deposition chamber, with optional Titanium Sublimation Pump (TSP), allowed the minimum base pressure to reach below  $1 \times 10^{-10}$  Torr.

Another system change was to mount the e- gun almost centrally (2cm off axis) within the deposition chamber. This allowed substrate rotation to be avoided if desired. The reason for this was to eliminate moving parts during growth which could be a source of particulate and carbon <Farley et al, 1987> contamination due to friction within the bearings. This modification, along with tight collimation of the Si beam, did lead, however, to severe problems with layer

uniformity, both in thickness and doping. However, this was advantageous for some applications, as each epilayer could provide samples with a known range of thicknesses and carrier concentrations. To achieve this, the layers had to be fully mapped, using an in-house-designed "spider's web"-shaped Ta mask to provide epilayer thickness information, and four point probe measurements for carrier concentration distribution. For most applications rotation was used to improve uniformity.

The other major design change was to manufacture as many internal system components as possible from Si, to limit any potential sources of metallic contamination within the system. These included parts of the substrate heater, Si beam collimator, various pieces of shielding for the e- gun hearth, deposition monitor and dopant cells, and also extensively on the in-vacuo substrate transport mechanism. Various methods of substrate manipulation have been tried in the past, including the use of Mo, Ta and graphite rings to support the substrate during movement through the system, as well as gripping the substrate independently by use of a "wobble stick" with PTFE coated jaws. However, all of these methods offered potential sources of contamination, and the technique employed for the majority of this study involved the use of Si rings to carry the substrate. The substrate holder on the heater stage was also manufactured from Si, as was the top surface of the trolley used to transport the wafers from the preparation chamber to the growth chamber. All

**these modifications were employed to yield the minimum  
contamination of epilayers due to the MBE growth process.**

## Chapter 3. Substrate Preparation.

### 3.1 Introduction.

#### 3.1.1 Background.

The aim of this investigation was to develop a low temperature clean to reduce dislocation levels within the epilayers, since the existence of a defect in the active device region can be catastrophic for the device <Kolbesen & Muhlbauer, 1982>, a persistent weakness of Si-MBE for applications in VLSI. The move towards low preparation temperatures is to minimise thermal processing in the growth chamber which can be a source of contamination (see Chapter 5). To this end, the author tried and developed various *in-* and *ex-situ* cleaning techniques, testing their efficacy by monitoring dislocation levels. Until recently, the substrate cleaning procedures used prior to epitaxy have been taken from other areas of Si technology <Kern & Puotinen, 1970, Henderson, 1972>, but Si-MBE layers have been found to be extremely sensitive to interface quality <Joyce et al, 1969>. Dislocation levels have been monitored for layers of thickness between 0.6 and 36um, and their dislocation densities have been found not to be significantly dependent on thickness (see Fig. 3.1). This indicates that the majority of such defects are nucleated at or near the epilayer/substrate interface, in turn implying that the properties of the substrate surface

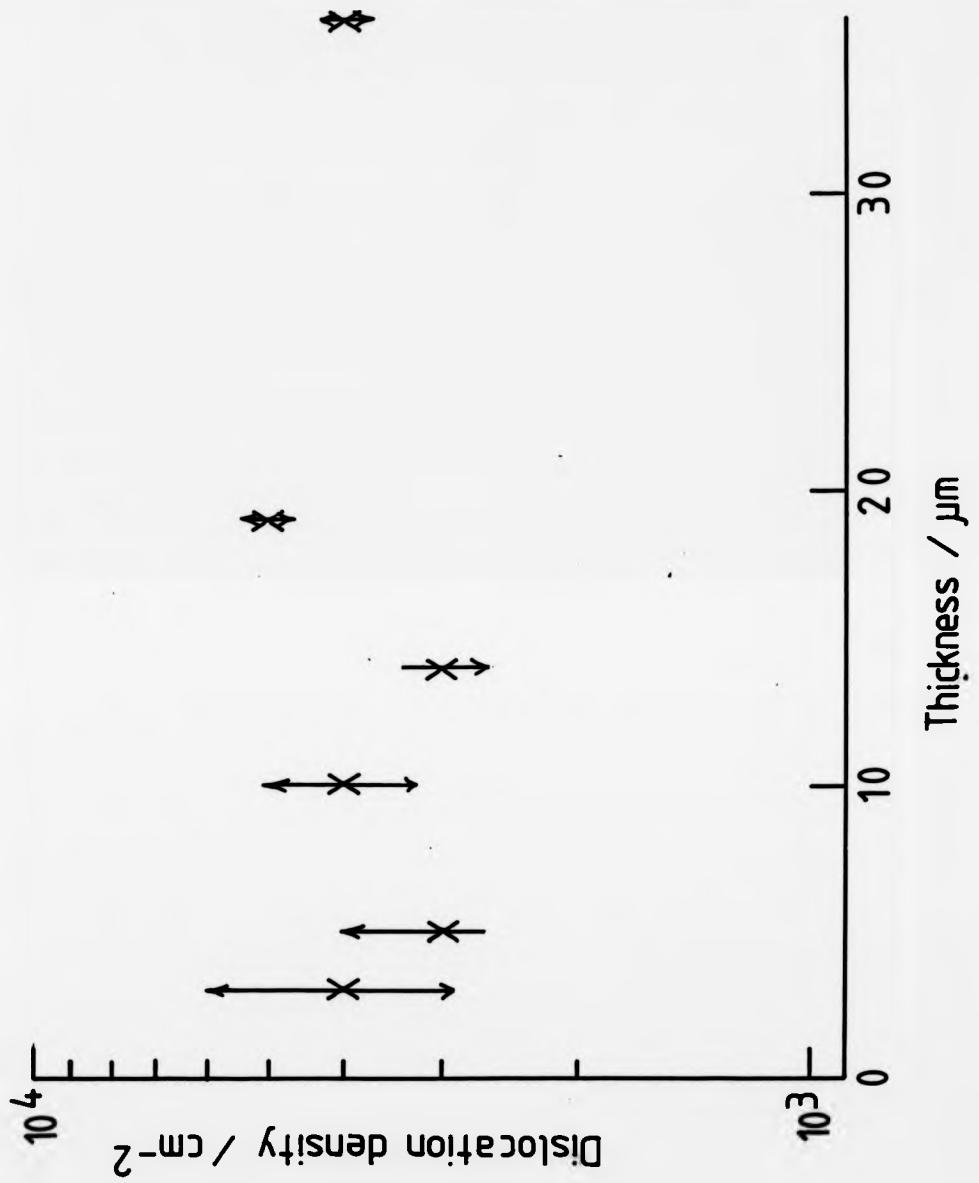


Fig. 3.1 Graph showing that epilayer thickness has a negligible effect on dislocation density.  
(All layers grown at  $550 < T_s < 650^\circ\text{C}$ )

and the nature of the first few monolayers of Si deposited are of immense importance to the crystallographic quality of the films grown.

### 3.1.2 Cleaning techniques in Si-MBE.

Material grown by MBE is very dependent on the cleanliness of the surface on which it is grown. The substrate must be free from oxide and carbon species <Unvala, 1972>, as well as transition metals<Pearce & McMahon, 1977>, if high quality electrical and crystalline properties are to be achieved. To generate a surface of such 'atomic' cleanliness, several methods have been tried.

Firstly there is the wet chemical clean, which takes three basic forms: an acidic clean, an alkaline clean or a combination of the two. The most common clean used in all branches of the silicon industry is the so-called "RCA" clean <Kern & Puotinen, 1970> in which wafers are rinsed in DI water, placed in hot alkaline peroxide, oxide-stripped in dilute HF, heated in acidic peroxide and then rinsed and spun dry. The action of the alkaline peroxide is to remove residual organic compounds, while the acidic clean removes remaining atomic and ionic contaminants.

An important variation of the RCA technique is the so-called 'Shiraki' clean [Ishizaka et al, 1982] which involves repeated boils in  $\text{HNO}_3:\text{H}_2\text{O}$  and  $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  solutions.

Firstly the native oxide is removed in 2.5% HF solution, then

the substrates are cleaned in the acidic and peroxide boils. The oxide formed in this oxidising solution is then removed in dilute HF and the cleaning process repeated, followed by spin drying and insertion into the vacuum system.

Another, more novel, ex-situ treatment that has been found to yield good results is that of exposure to ozone. The action of ozone is to remove surface hydrocarbons by oxidation <Vig, 1985>. Two methods have been tried: the dry UV ozone clean (UVOCS), in which substrates are exposed to UV light from a Hg lamp <Tabe, 1984>, and ozone bubbling during a wet chemical clean <Tatsumi et al, 1985>. Both have been demonstrated to greatly reduce interfacial C levels as measured by X-ray photoelectron spectroscopy (XPS) and SIMS <Pidduck et al, 1988>. This removal of carbon species reduced dislocation levels to  $\sim 3 \times 10^3 \text{ cm}^{-3}$  <Tabe, 1984> for [100] substrates, if immediately inserted into the UHV system. Metallic contamination has not been monitored for the UVOCS method, but little reduction is likely to be caused by the oxidation process <Pidduck et al, 1988>.

Recent work at Jet Propulsion Laboratory <Grunthaner et al, 1988> has illustrated a new chemical clean involving the removal of the native oxide by HF/Ethanol solution in an N<sub>2</sub> ambient, growth and removal of a thick (1000Å) sacrificial thermal oxide, and then growth of a thin (100Å) protective thermal oxide. This is removed by an HF dip, and passivation of the Si surface by H from the HF solution prevents significant oxide formation prior to insertion into the MBE system. The use of a sacrificial oxide is unusual prior to

epitaxy, but should yield low contamination. The high temperature (1000°C) required for its growth could be disadvantageous for some purposes. Recent work <Grunthaner et al, 1989> has shown this sacrificial oxide to be unnecessary, the native oxide removal in HF/Ethanol solution being sufficient to yield a clean, unoxidised surface. Analysis for metallic contamination has not been carried out. If a high temperature *in-situ* stage is not used, 0.05% of a monolayer of oxygen has been shown to be present at the surface <*ibid.*>, 100 times greater than HF/H<sub>2</sub>O or HF/Ethanol preparation with a high (>700°C) temperature stage. The effect on dislocation density in subsequent epilayers cleaned using the JPL technique has not been studied.

The process of *in-situ* oxide removal after these *ex-situ* cleans has also been studied, by conventional means such as transient mass spectrometry (TMS) and XPS <Hardeman et al, 1985>, and by the purpose-built technique of laser light scattering (LLS), in which diffuse scattering gives information on surface topography <Robbins et al, 1987>. These methods have led to a better understanding of oxide removal, involving hole formation in the surface oxide <Frantsuzov & Makrushkin, 1976>.

*In-situ* contamination removal by the physical method of ion sputter cleaning has also been adopted as a standard pre-epitaxy clean <Bean et al, 1977>. For this, Ar<sup>+</sup> ions at ~1keV are used to bombard the substrate surface to sputter any surface contamination. The resulting amorphisation of the Si surface is then removed by annealing at ~800°C. The

sputtering is carried out at room temperature to minimise residual damage and to prevent Ar+ ions from channelling deep (~100Å) into the substrate.

Despite the research into the above and other cleaning techniques, no single method has been agreed upon for general use. For this reason a study was made of the preparation of an optimum Si surface for epitaxial growth, to supersede the previous method used at Warwick of simple insertion of 'as-received' substrates into the system. As received wafers were originally used since it was felt that manufacturers' cleaning techniques should be good enough such that any other chemical procedure carried out prior to epitaxy would have a detrimental effect on cleanliness. However, it has been found that even large manufacturers with carefully researched proprietary cleans have periodic problems with contamination, illustrating the difficulties involved in the area of substrate cleaning. Also, the oxide present on as-received wafers is relatively thick and stable <Grundner & Jacob, 1986>, and thus more difficult to remove *in-situ*, so various preparation techniques have been studied for use with MBE.

Few studies have used dislocation count as an indication of substrate cleanliness. This is somewhat surprising, since it is much more sensitive than surface analysis techniques (in principle a single impurity atom can nucleate a defect and thus be detected), and gives data on the eventual aim of the clean, i.e. defect reduction.

### **3.1.3 Defects in Si-MBE.**

There are four types of defect found in MBE-grown silicon after a defect-revealing etch:

- (i) dislocations
- (ii) stacking faults
- (iii) saucer pits (s-pits)
- (iv) particle induced defects.

The densities of the first two are both dependent on interface quality and can thus be affected, and hopefully reduced, by substrate cleaning. Densities of these defects can also be used to give an indication of the efficiency of a chemical clean. Evidence has been obtained that dislocations are caused by surface C and O, usually as complexes <McFee et al, 1983> probably causing strain that cannot be taken up by the lattice which nucleates a dislocation. Stacking faults are usually caused by inadequate removal of surface oxide<Futagami, 1980> whilst s-pits are thought to be caused by metallic precipitates <Pearce & McMahon, 1977>. Thus, decreases in dislocation count can be correlated with a reduction in carbon and oxygen coverage; similarly decreases in s-pit densities are indicative of less metallic contamination on the substrate. Stacking faults were rarely seen in this work, and their appearance indicated an unusually thick or stable oxide had been grown and was not properly removed by the *in-situ* thermal treatment.

### **3.1.4 Analytical techniques.**

**There are few techniques available for detecting the low levels of contamination found in MBE-grown epitaxial layers. C and O are particularly difficult<Sykes, 1987>, the general technique used being SIMS which has a bulk detection limit of  $\sim 10^{18} \text{cm}^{-3}$ . For Cu the detection limit is  $\sim 10^{16} \text{cm}^{-3}$ , sufficient to see interfacial contamination but not sensitive enough for analysis through the epilayer. For this, the techniques of Neutron Activation Analysis (NAA) and Atomic Absorption (AA) were used.**

**Analytical methods to ascertain the performance of the various chemical cleans included routine defect etching of all layers, and secondary ion mass spectrometry (SIMS) profiles of selected layers. The defect etching was done by the ASTM approved technique of using dilute Schimmel preferential etchant <Schimmel, 1979>. During the SIMS analysis metals were profiled using an  $\text{O}_2^+$  primary ion source, while C and O in the epilayers were analysed using a  $\text{Cs}^+$  primary beam, after allowing the sample and system to pump down overnight prior to analysis, to reduce the C and O backgrounds.**

### **3.2 Methodology.**

The main contaminants on the Si surface are carbon, metallic impurities and, of course, the native oxide. The method of low temperature preparation to give an atomically clean surface must therefore involve three processes:

- [i] Removal of native oxide and contaminants
- [ii] Regrowth of a thin, pure, protective oxide prior to insertion into the UHV system
- [iii] *In-situ* oxide removal.

The following section will discuss the methods used.

#### **3.2.1 Ex-situ wet chemical clean.**

The first step of the process is the removal of the native oxide. The normal method of achieving this is to place the substrate in a dilute HF/DI water solution for a short period of time. This was optimised and standardised to 2 minutes in 2.5% HF solution. Shorter times than this produced patchy oxide removal, longer times offer no advantages, and may cause metals from the solution to be adsorbed onto the substrate surface. Once the oxide had been removed the wafer was rinsed in flowing DI water until the resistivity of the efflux was equal to that of the influx. However, it has been found that the hydrogenated Si surface can pick up metals, especially Cu, from the HF and DI water solution. To avoid this, a second method was tried in which the substrate was suspended over concentrated HF (48%) in an air-tight

container, with no DI water rinse, thus obviating the need for contact between the substrate and water. However, this method was found to yield a patchy surface with areas of incomplete oxide removal, and so was abandoned in preference of the HF solution dip.

After oxide removal the substrates were placed in a chemical bath to clean the surface and regrow an oxide. Chemicals used were semiconductor grade, high purity, filtered, supplied by Countdown <1991>, and the water was 18Mohm deionized. The solutions used were as follows:

- [i] HNO<sub>3</sub>:H<sub>2</sub>O, HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O ('Shiraki' clean)
- [ii] 3HCl:1H<sub>2</sub>O<sub>2</sub>:1H<sub>2</sub>O
- [iii] 1HNO<sub>3</sub>:1H<sub>2</sub>O
- [iv] 1NH<sub>4</sub>OH:1H<sub>2</sub>O<sub>2</sub>:4H<sub>2</sub>O
- [v] 1NH<sub>4</sub>OH:6H<sub>2</sub>O<sub>2</sub>:20H<sub>2</sub>O
- [vi] HF/H<sub>2</sub>O

Method i) involved two successive 10 minute boils in each solution followed by a 30 min rinse in flowing DI H<sub>2</sub>O; in methods ii), iii) and iv) substrates were boiled in solution for 10 mins followed by a 30 min DI rinse; for clean v) a 15 min boil was used to allow for the slower rate of oxide formation in the less concentrated solution, again followed by a 30 min rinse in flowing DI. Substrates were then spun dry in a PTFE spinner in a class 100 work-station, and immediately inserted into the vacuum system.

As well as these full chemical cleans with an oxide regrowth to protect the Si surface, another procedure tried was the HF dip stage alone [vi], a novel approach when first

carried out by the author. This removed the oxide, leaving a hydrogenated surface which allowed minimal oxide regrowth. After a dip in 2.5% HF/DI water solution for 2 minutes, the substrates were rinsed and dried as above. Spin-drying was also carried out in a hood filled with flowing high-purity nitrogen gas from which the substrates could be loaded directly into the nitrogen filled system load-lock, to minimise oxide growth prior to entry into the vacuum chamber. This technique was found to have a negligible effect on dislocation levels.

### 3.2.2 In-situ clean.

After a chemically cleaned substrate had been loaded into the system, the final step before growth was the removal of the chemically grown oxide. Previously the standard technique had been simple thermal desorption, i.e. heating the substrate to 900°C to desorb surface oxide. However, more efficient means of performing this function have recently been proposed, and a study to optimise these was performed. The first method was the flux (or 'rad') clean <Tabe, 1982, Kugiyama et al, 1985> in which a substrate was held at high temperature [850-900°C] and exposed to a low Si flux, insufficient to initiate growth, but instead inducing oxide desorption via the reaction



The second method, known as 'capping' <Tatsumi et al, 1985>, involves depositing a thin layer (~20Å) of Si at room temperature, then heating the substrate to 850-900°C so that the oxide reacts with the capping layer according to the same reaction as above, desorbing the oxide as volatile SiO. This method was improved for this study by heating the substrate to 350-400°C before depositing the capping layer, this temperature having been shown by high resolution electron energy loss spectroscopy (HREELS) <Grundner & Jacob, 1986> to be sufficient to desorb any hydrocarbon remaining on the Si surface. The Si cap grown by this method will be polycrystalline, since it is growing on the thin surfacial oxide.

In practice, the second method proved easier to implement reproducibly due to the difficulty in controlling evaporation from the electron beam evaporator at the low fluxes (<1A/s) required to prevent growth during the 'rad' clean. During the high temperature stage of the clean, with the substrate shutter closed, the e- beam evaporator was ramped up to the rate required for growth, and once this had stabilised (2-3 mins), growth was initiated and then the substrate temperature reduced to that required for growth after a few monolayers had been grown. This procedure was found to be vital to achieve good morphology, especially at low (<650°C) growth temperatures, since lowering the substrate temperature before initiation of growth was found to yield heavily dislocated material, probably due to the low surface mobility and initial roughness of the substrate.

### **3.3 Results.**

#### **3.3.1 The effects of chemical cleaning.**

Fig.3.2 shows the results of the various wet chemical cleans, illustrating their efficacy at reducing the dislocation density. Prior to embarking on the cleaning processes, the typical dislocation levels in layers grown in the V80 system were between  $10^5$ - $10^6$  cm $^{-2}$ . The best of the chemical cleans can therefore be seen to have reduced dislocation levels by approximately two orders of magnitude. Due to the rather statistical nature of work with defects, many layers have to be grown for each condition to establish reliable data. The error bars in Fig. 3.2 therefore indicate the standard deviation of the levels achieved for wafers cleaned by each method, and the central points are the means for all the layers. It is interesting to note that the two stage 'Shiraki' clean <Ishizaka et al, 1982> yielded poorer results than the single stage HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O or HNO<sub>3</sub>:H<sub>2</sub>O cleans. Possible reasons for this are that the Shiraki oxide grown was thicker, and/or increased hydrocarbon contamination during this protracted cleaning schedule.

The alkaline cleans proved to be less effective than the acidic ones in decreasing the defect density. The diluted form [1NH<sub>4</sub>OH:6H<sub>2</sub>O<sub>2</sub>:20H<sub>2</sub>O] produced no reduction in dislocation densities, and also introduced up to 10<sup>4</sup>cm<sup>-2</sup> of stacking faults, presumably associated with inadequate oxide

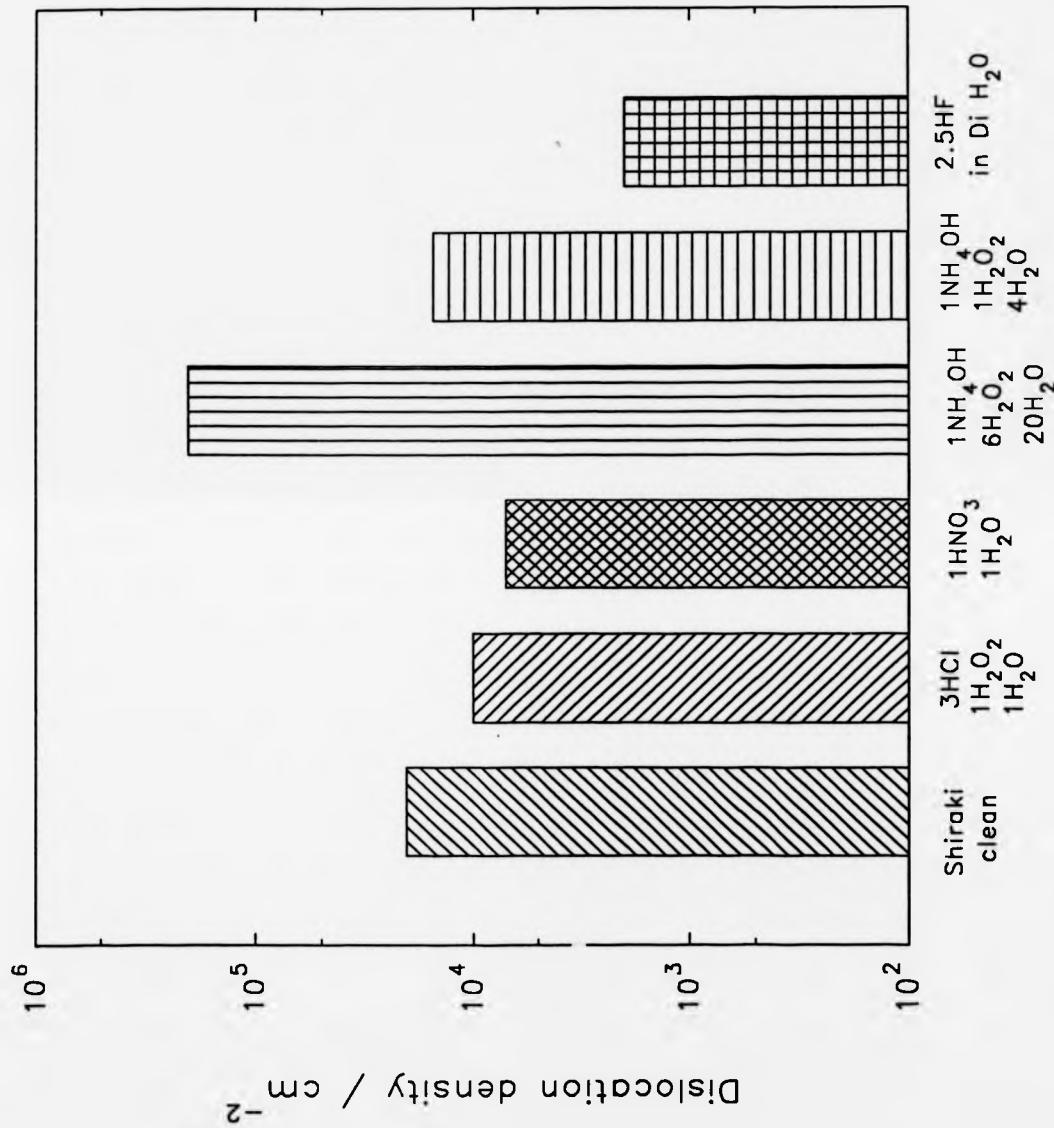


Fig. 3.2 Chart illustrating the efficacy of the various wet chemical cleans, and the spread of results for each. The 2.5% HF dip oxide removal alone provided the lowest, most consistent defect levels. (All layers grown at 550°-T<sub>m</sub><650°C)

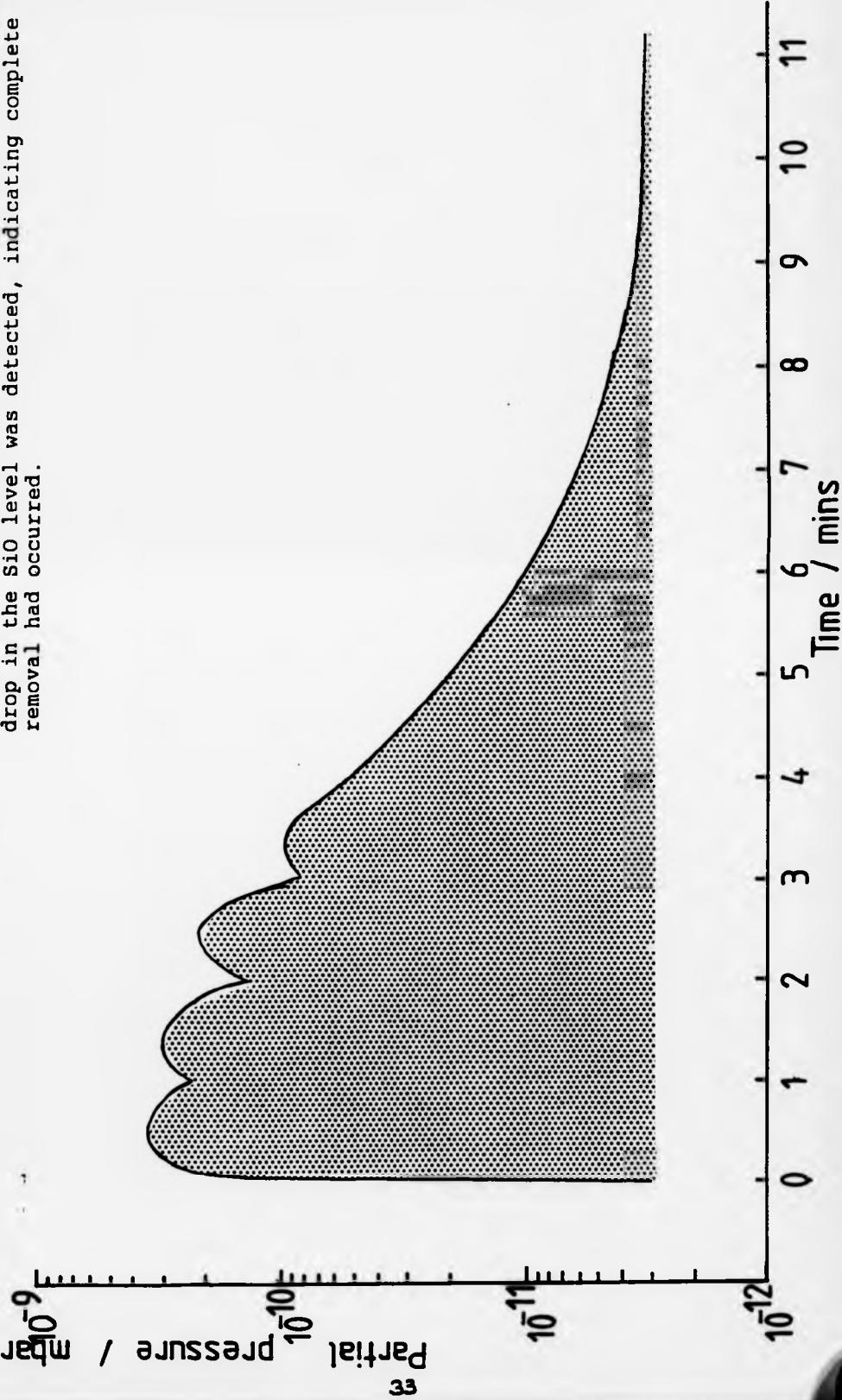
removal. This may be due to slow oxide growth in a weak solution leading to the formation of very stable  $\text{SiO}_2$ , as opposed to  $\text{SiO}_x$ , where  $x < 2$ , which can be formed by more rapid oxide growth. This  $\text{SiO}_x$  has been shown to be less stable <Ravi & Varker, 1974> so that it can be more easily desorbed during *in-situ* thermal treatment.

### 3.3.2 The nature of grown silicon oxide.

One of the *ex-situ* preparations that has proved most effective in decreasing dislocation count is a simple dip in diluted HF followed by a rinse in flowing DI water, with immediate insertion into the UHV chamber. The resulting oxide is very thin (<10Å <Grundner & Jacob, 1986, Pidduck, 1989>), as the surface is passivated by hydrogenation, and is exposed to air for only the short time between spin-drying and insertion into the system (.2 minutes maximum). Growing a thin capping layer of Si on top of this allows the oxide to be removed relatively easily by low temperature *in-situ* thermal treatment. Monitoring the  $\text{SiO}$  (mass 44) peak with a mass spectrometer indicated that the oxide was removed within 7 minutes at 720°C, as shown in the RGA of Fig. 3.3. This ease of desorption after a capping layer has been grown is, however not the same as that which occurs after thermal treatment of a chemically grown oxide.

It has recently been shown by the use of pulsed laser atom probe (PLAP) analysis <Grovenor et al, 1987> that the

Fig. 3.3 Residual gas analysis of decay of SiO (44) peak during standard in-situ substrate preparation at steps of 500, 600, 700 and 720°C. After 7 minutes at 720°C no further drop in the SiO level was detected, indicating complete removal had occurred.



oxide grown at room temperature after a dip in dilute HF solution is not the equilibrium phase of SiO<sub>2</sub>, but rather is the sub-oxide SiO (see Fig. 3.4). However during the heating process of the thermal clean there are two competing processes that will occur. The first is desorption of the volatile SiO and the second the formation of SiO<sub>2</sub> from the SiO layer. Naturally, if the SiO<sub>2</sub> phase is formed, it will become more difficult to desorb. If a low temperature <300°C cap is grown on top of the SiO before heating to desorb it, the oxide does not relax to SiO<sub>2</sub> and thus can be desorbed at a lower temperature <Grovenor et al, 1987>. It is thus proposed that the action of the cap on wafers given an HF dip is partly to trap the oxide as SiO as well as aiding a transition between SiO<sub>2</sub> and SiO.

The variation of dislocation density with clean-up temperature as illustrated in Fig. 3.5 suggests that lower temperatures were advantageous for reducing dislocation density. This may be due to the tendency for SiO to turn to SiO<sub>2</sub> at higher temperatures, thus making oxide removal more difficult, or the interaction with CH<sub>x</sub> groups (see section 5.3.1). If C is present within the oxide layer it can form SiC in a temperature dependent reaction, forming a possible dislocation nucleation site. At higher temperatures (>800°C) thermal roughening of the Si surface may contribute to the increase in defect levels.

The appearance of oxidation induced stacking faults at clean-up temperatures below 700°C indicated that inadequate or impractically slow oxide removal occurred (the

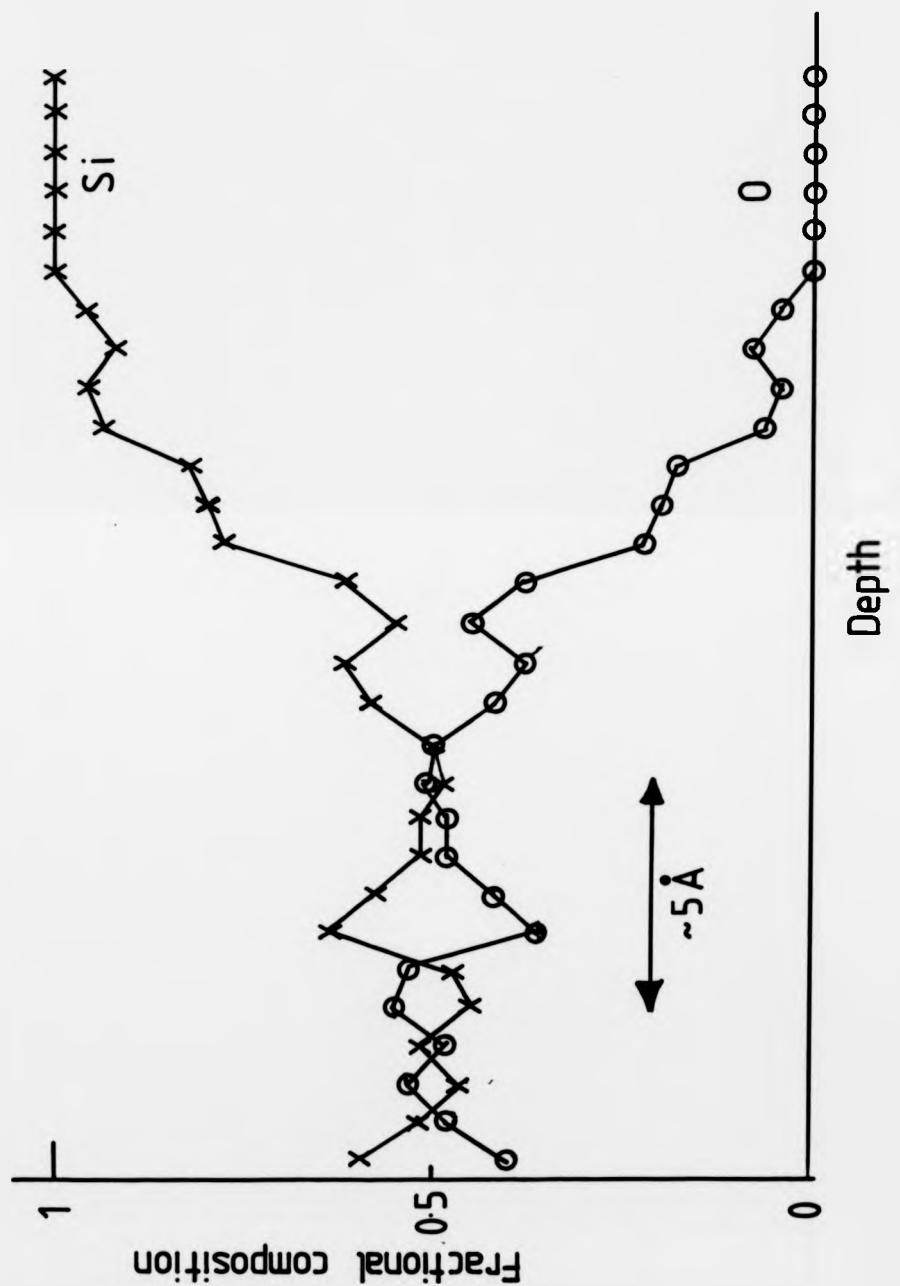


Fig. 3.4 Diagram illustrating the composition of the surfacial oxide after an HF dip and 290 hours air exposure. The oxide formed is clearly  $\text{SiO}$  rather than the equilibrium  $\text{SiO}_2$  phase. (After Grovenor et al., 1987)

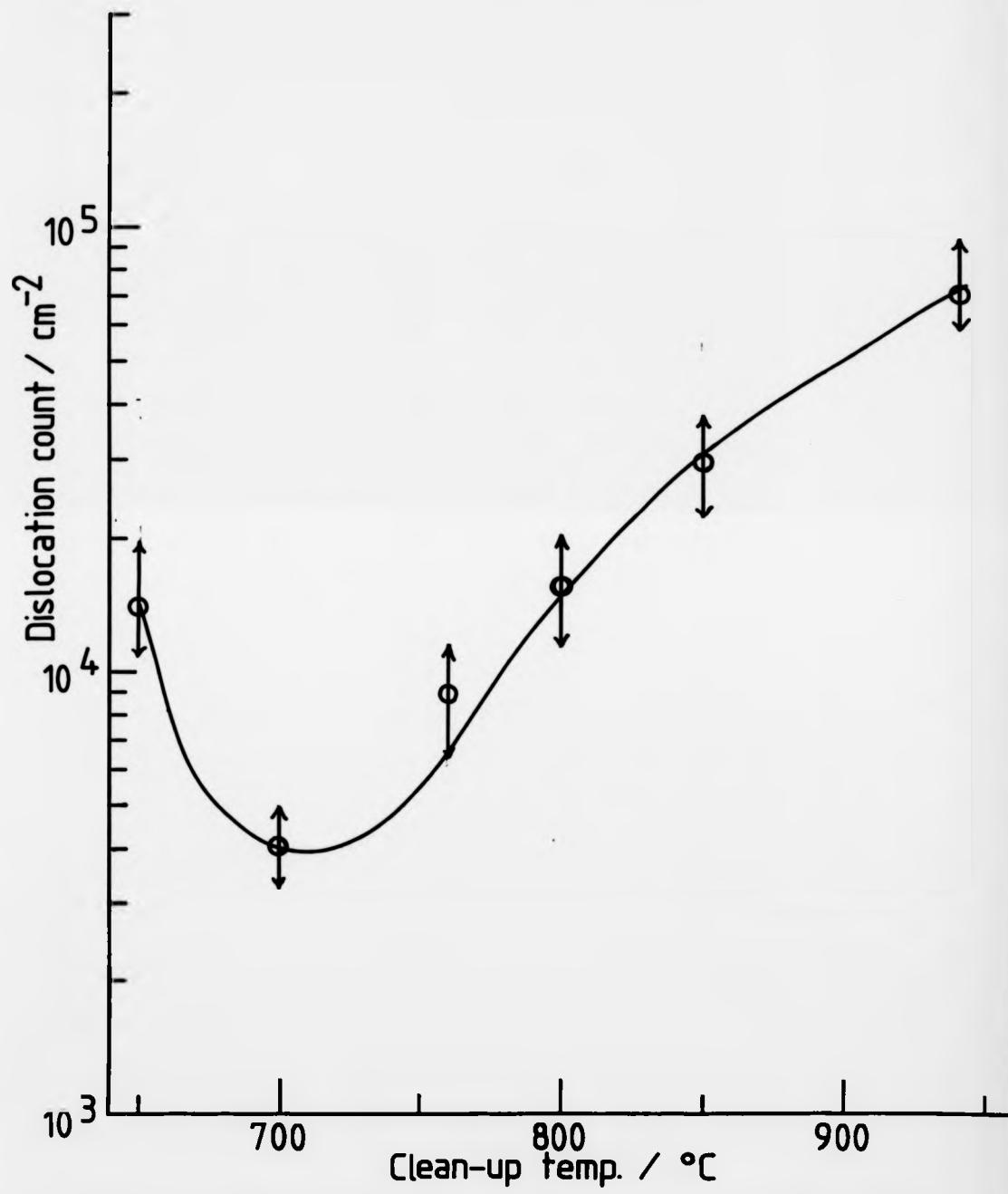


Fig. 3.5 Graph of dislocation density against thermal clean temperature. The variation of dislocation level is probably due to a modification in the surface interactions of  $\text{SiO}_2$ ,  $\text{SiC}$  and  $\text{CH}_4$ . Results shown are for epilayers grown at  $500^\circ\text{C} < T_s < 600^\circ\text{C}$ , after an HF dip.

undesirability of holding the Si surface at high temperature for long periods is discussed in section 5.3.1). The length of time necessary for complete thermal desorption of the oxide was monitored using a mass spectrometer with line of sight to the substrate.

### 3.3.4 Interfacial metallics.

Once the grown oxide has been removed it is desirable to have no residual contaminants, especially metals on the surface. Although these may not cause degradation in the crystalline quality of the epilayer, thus not showing up as macroscopic defects after preferential etching, they can have a strong effect on the layer's electrical properties <Lawrence, 1965>.

The s-pit density in the epilayer after defect etching, which is considered as indicative of metallic contamination (Pearce and McMahon, 1977), was observed to determine the metallic incorporation, but no correlation between chemical clean and s-pit density could be seen. Calculations <Stacy et al, 1981> indicate that a Cu concentration of  $5 \times 10^{13} \text{ cm}^{-3}$  would be required to give an s-pit density of  $10^4 \text{ cm}^{-2}$ , similar in fact to the average s-pit count in this work.

Cu has been found as a major metallic contaminant in undoped layers, as revealed by using SIMS, atomic absorption analysis (AA) and neutron activation analysis (NAA). There are two possible sources of this Cu: the HF/water used for oxide

removal, as metals can be easily adsorbed onto the highly reactive bare Si surface, and from the copper hearth of the electron beam evaporator. To minimise the latter, as much of the hearth as possible was shielded with Si (see Fig. 2.2).

It can be calculated from standard solid state diffusion equations, whether interfacial Cu contamination is a major source of the Cu contamination in the layers. Cu is a very fast diffuser in Si at typical growth temperatures (diffusion coefficient of  $5 \times 10^{-5} \text{ cm}^2/\text{s}$  at  $750^\circ\text{C}$ ) < Sze, 1981 >.

SIMS profiles such as that shown in Fig. 3.6 have revealed Cu at the epi/substrate interface. X-ray fluorescence analysis of as-received and chemically cleaned substrate has also indicated the presence of Cu (see Fig. 3.7). Calculations of impurity concentration through the epilayer can be made from the diffusion equation

$$C(x,t) = C_s \operatorname{erfc}[x/(2\sqrt{Dt})] \quad 3.1$$

where  $C(x,t)$  is the impurity concentration at a distance  $x$  from the surface impurity layer, at a time  $t$ ,  $D$  is the diffusion coefficient at the given temperature, and  $C_s$  is a constant surface concentration. This equation can be modified for a time dependent value of the surface (in this case interface) impurity concentration,  $C_0$ , which applies in this case due to the finite, predeposited impurity source, to give

$$C(x,t) = C_0 / (\pi Dt)^{1/2} \exp[-x^2/(4Dt)] \quad 3.2$$

Using this equation, graphs can be plotted of impurity concentration against depth for various values of time and

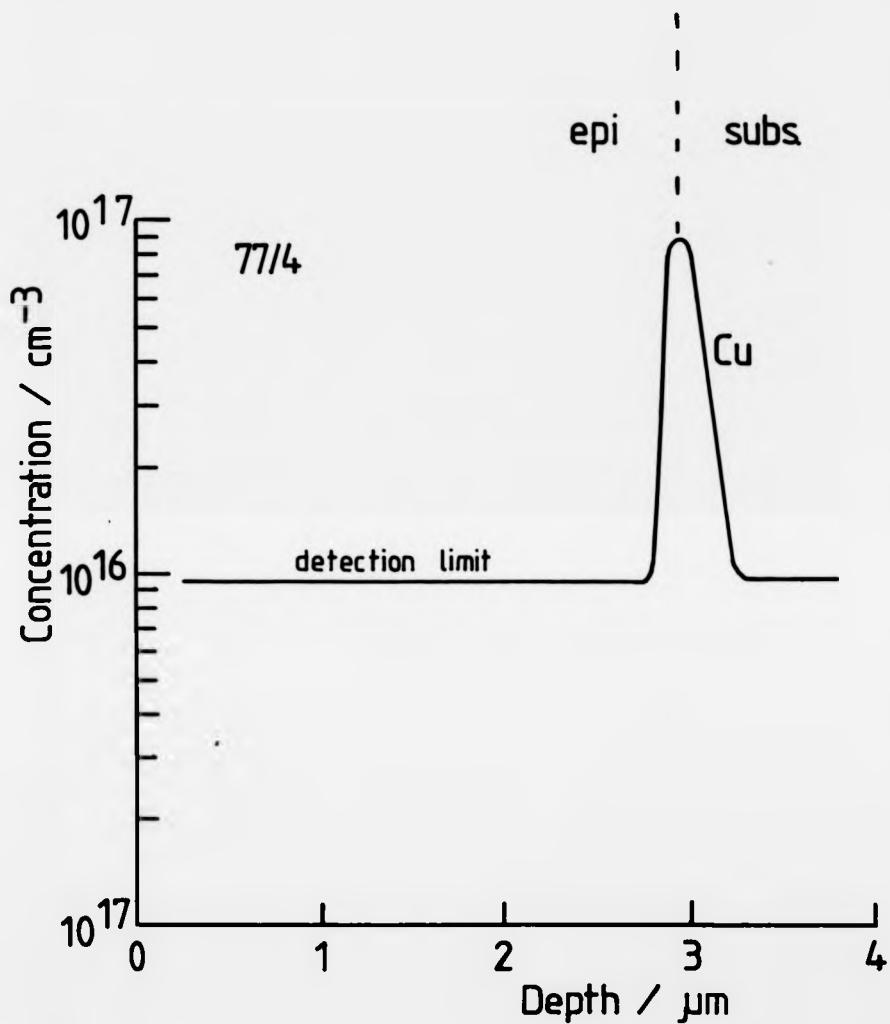


Fig. 3.6 SIMS profile showing the presence of Cu at the substrate/epilayer interface. This layer was chosen for its particularly high Cu spike. Average interfacial levels were usually near or below the SIMS detection limit.

(SIMS performed for the author by Loughborough Consultants)

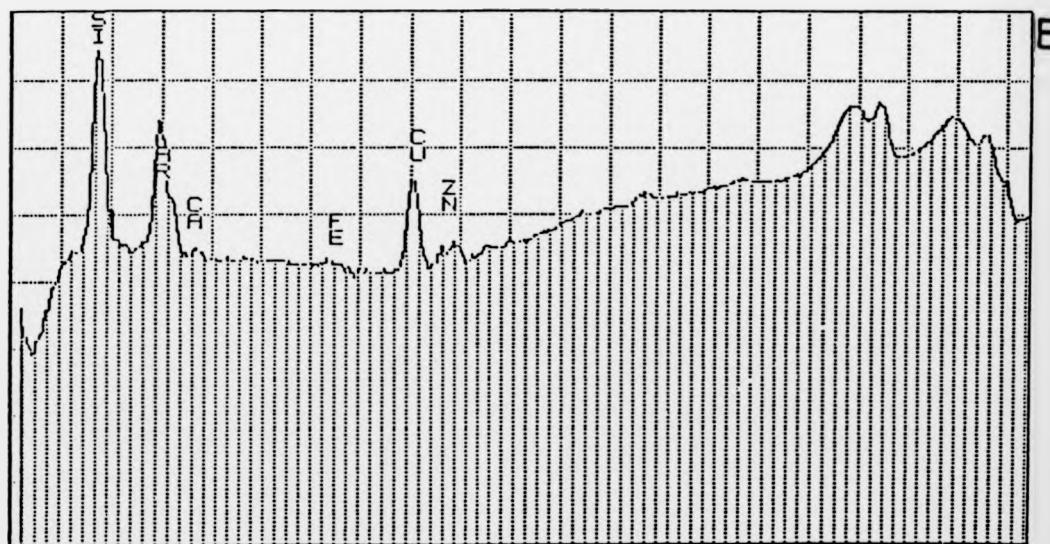
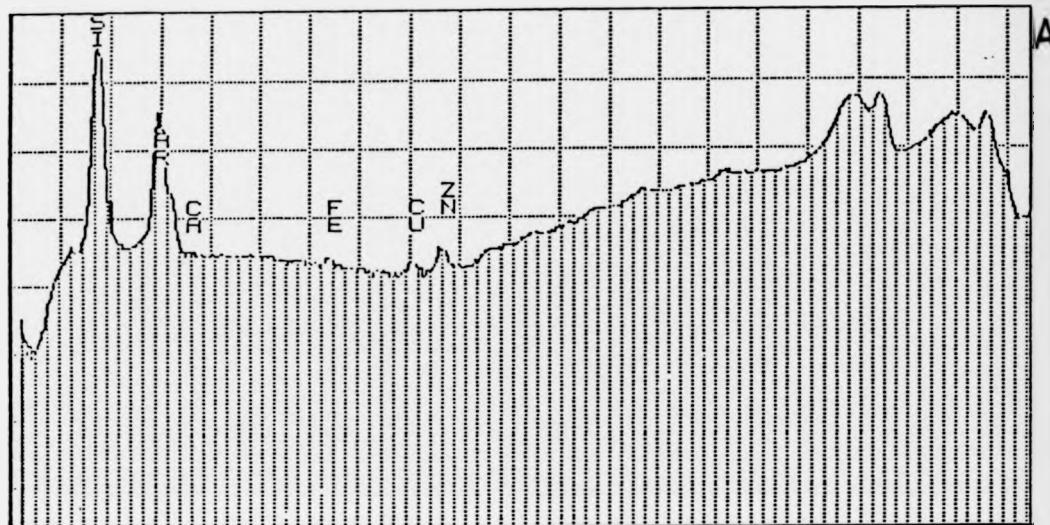


Fig. 3.7 Total reflectance X-ray fluorescence data showing increase in Cu signal after soaking in HF. A) as-received wafer, B) after 30 min dip in Aristar HF (The Cu peak corresponds to a surface concentration of  $\sim 8.8 \times 10^{12} \text{ cm}^{-2}$ . (Analysis carried out by L. Canham, RSRE)

substrate temperature. As expected, these graphs show that at a typical growth temperature and time (say 700°C for 30mins) an almost uniform distribution of Cu should occur throughout the epilayer and well into the substrate, from the initial interface spike. This is in contrast with the SIMS profile of Fig. 3.6 which shows a high, sharp interfacial Cu peak.

It therefore seems that there is a tendency for Cu to segregate at the epi/substrate interface. It has been found <Salih et al, 1985> that if a small percentage of germanium is introduced into a CVD grown buffer layer before homoepitaxial Si deposition, that the resulting misfit dislocations act as sites for metallic gettering.

To test the gettering properties of Si-MBE-grown interfaces samples were annealed in a furnace at various anneal temperatures and times. When layers that had interface Cu levels that were barely detectable by SIMS were annealed, the Cu levels increased by up to two orders of magnitude after only one minute at 1000°C (see Fig. 3.8). A ten minute anneal at 800°C had a similar effect. Defect etching of annealed samples revealed no extra dislocations as a result of the anneal, implying that increased gettering was not due to increased defect levels. This gettering capability of the interface is presumably due to dislocations nucleated there, and to the inherent strain in the lattice. So the high interfacial Cu spike may not necessarily be exclusively related to the cleaning process, but may also derive from metals being incorporated during

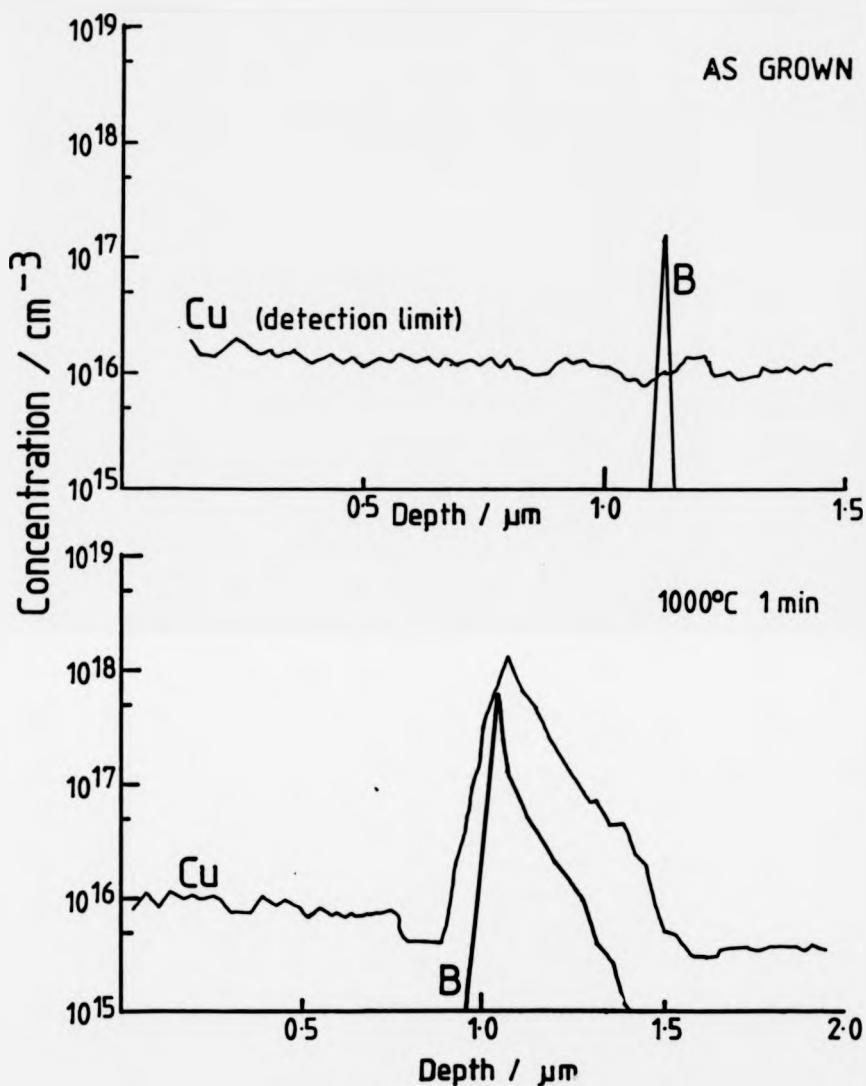


Fig. 3.8 These SIMS profiles show the Cu interfacial peak before and after a 1 minute anneal at 1000°C. Clearly the interface is acting as a gettering site, presumably due to the strain introduced there by dislocation nucleation.  
(SIMS performed for the author by Loughborough Consultants)

growth, as occurs when other forms of intrinsic (IG) <Shimura et al, 1981> or extrinsic (EG) <Lecrosnier et al, 1981> gettering are used.

This result is of great importance, since the properties of the interface may have a significant effect on devices grown by MBE. If junction isolation from the substrate is required, a build-up of metallics will cause soft breakdown, which may have a deleterious effect on device performance. However, if it is known that this contamination layer exists, a buffer layer of Si with the same carrier concentration as the substrate can be grown first. The thickness of this should be greater than that of the depletion width of the junction required for isolation. The electrical properties of the device will therefore not be affected by the epilayer/buffer layer interface.

This imperfect interface could therefore in principle be used as a gettering site to trap transition metals from the epilayer, providing a post epitaxy anneal is an acceptable processing step.

### **3.4 Interfacial Boron.**

#### **3.4.1 Discovery of interfacial contamination.**

During routine eCV analysis of p-type epilayers on p-substrates, it was noticed that a thin p-type spike occurred at the interface, as shown in Fig. 3.9. Its presence was not noticeable with n-type epilayers or substrates since the presence of a p-n junction disrupts the eCV profile at this point. SIMS was used to identify the nature of this peak, which was found to be B, as can be seen in the profile in Fig. 3.10, at an areal concentration of up to  $10^{12}\text{cm}^{-2}$ . The presence of such a peak is naturally highly undesirable in epilayers where the interfacial region is to be used as an active region of the device, or if it is to be used as a p-n junction. Discovery of the source of this B was therefore of importance, so that it could be eradicated.

Similar observations had subsequently been made by other research groups involved in Si-MBE, using various system designs, although there was no evidence for a similar phenomenon in CVD-grown Si layers. This implied the process differences between the two techniques either inhibited or encouraged the presence of the B layer. It was viewed that the higher temperatures used in CVD might be able to remove an innate source of contamination prior to growth, or that the environment during MBE induced the contamination.

Fig. 3.9 A typical eCV profile of a p-type epilayer on a p-type substrate (as-received), clearly illustrating the presence of a p-type spike at the interface.



## DEPTH PROFILE

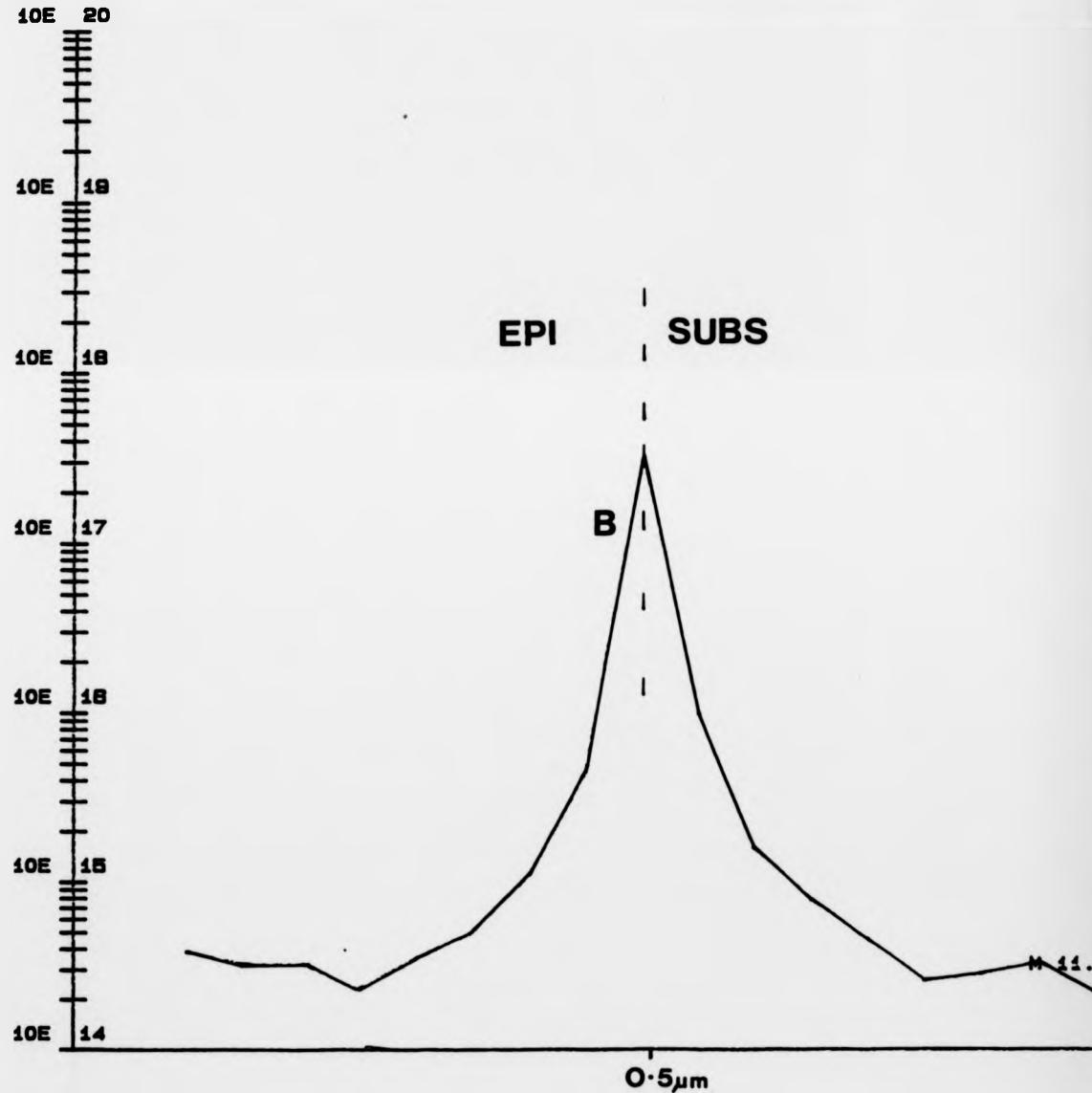


Fig. 3.10 A SIMS profile of the interfacial p-type spike,  
identifying the impurity as being B.  
(SIMS carried out for the author by Loughborough  
Consultants)

### **3.4.2 Identification of contamination sources.**

**Four possible sources of contamination were identified:**

- i) B redistribution into the oxide layer from the substrate**
- ii) wafer contamination during manufacture**
- iii) atmospheric B compounds**
- iv) the MBE growth/ vacuum environment itself.**

Source i) was thought possible since Grove et al. <1964> showed that B preferentially redistributed from substrates into the oxide layer during annealing, and initially the B spike was seen in p-type epilayers on p-type substrates. Subsequent SIMS analysis showed however, that n-type substrates exhibited similar contamination, so this mechanism was discounted.

To determine whether the manufacturer of the wafer affected the surface properties, substrates from various manufacturers [Wacker, Monsanto, Mullard, Sin'etzu and Jasil] were all used for epitaxy. SIMS analysis revealed that the interfacial spike was always present, independent of the make of substrate used, and in approximately the same concentration. Temperature of *in-situ* substrate preparation [up to the maximum achievable  $T_g$  of 900°C] did not affect the concentration, although it was found to affect activation. Comparison of SIMS and eCV profiles at a clean up temperature of 750°C showed that only approximately 5% of the interfacial B was active, whereas about 30% was activated at a preheat temperature of 900°C. Precise values of

activation were unobtainable, since the abruptness of the B spike led to inaccuracy in the eCV due to the technique's lack of resolution, which would lead to an underestimation of activation.

To ascertain whether the B was present on the substrates prior to growth, an experiment was designed to yield a clean Si surface by epitaxial deposition and then to analyse it after exposure to various conditions, in an attempt to recreate those required for contamination. To minimise variables, several conditions could be tested within a single epilayer by performing growth interrupts.

The conditions chosen were:

- a) wafer cooled to room temperature, then reheated for growth to continue at 800°C
- b) wafer cooled, left overnight, then grown on at 800°C
- c) wafer cooled, e- gun degassed, then layer grown on at 800°C
- d) wafer cooled then moved around entire MBE system, followed by growth at 800°C
- e) wafer cooled, exposed to air in load lock, then grown on at 800°C

The first four were found to cause no B accumulation. However, interrupts in which the fresh epitaxial surface was exposed to air did exhibit B contamination. Fig. 3.11 shows a SIMS profile of an epilayer in which this interruption technique was used. The normal interfacial spike is clearly

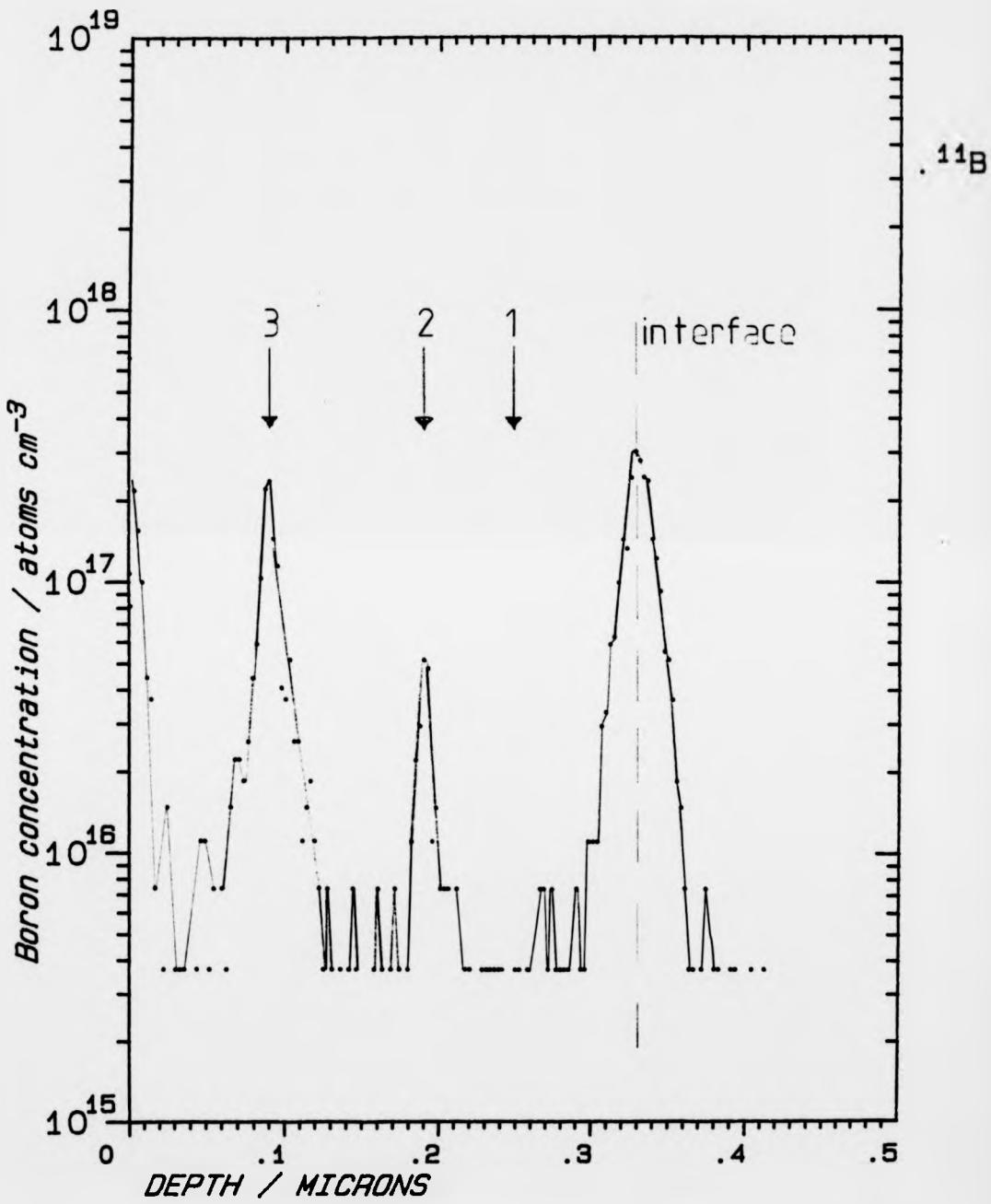


Fig. 3.11 A SIMS profile through an epilayer with three intentional growth interrupts. The interfacial B spike is clearly visible. During the first interrupt the wafer was cooled and moved around the system. During the second it was exposed to air at 100mbar for 5 mins, and the third to air at atmospheric pressure for 5 mins. The second and third show clear B accumulation. (SIMS carried out for the author by Loughborough Consultants)

visible, and the spatial position of interrupts 1, 2 and 3 are marked. At interrupt 1 the wafer was cooled and transported around the MBE system under UHV, causing no detectable contamination. Interrupt 2 involved the wafer being cooled and moved to the system load lock. Here it was exposed to air at a pressure of 100mbar for 5 minutes. Considerable B contamination was evident, at an integrated concentration of  $6 \times 10^{10} \text{ cm}^{-2}$ . Finally, interrupt 3 consisted of wafer cooling, removal to the load lock and exposure to air at atmospheric pressure for 5 minutes. Again, severe B contamination was noted, at an areal concentration of  $8 \times 10^{11} \text{ cm}^{-2}$ , similar to that present at the epilayer/substrate interface.

From these results it was evident that the contamination was not manufacture-induced, but that air exposure of the wafer was a crucial step in contamination. To test whether the UHV environment itself contributed to the interfacial B, rather than air-borne pollution, another interrupt experiment was performed. This time the wafer was exposed to moisture-free research grade O<sub>2</sub>, rather than air. Some B contamination was noted, as shown in Fig. 3.12. This indicated that a B spike could be induced without atmospheric exposure, so the system itself was a source. [It is interesting to note that work on cleaved Si <Froitzheim et al, 1984>, in which cleaved Si<111> was exposed to  $10^{-6} \text{ mbar}$  of CO in a UHV chamber, indicated a small acceptor build-up on the surface. Its origin was not known, but was ascribed to extra states induced by surfacial

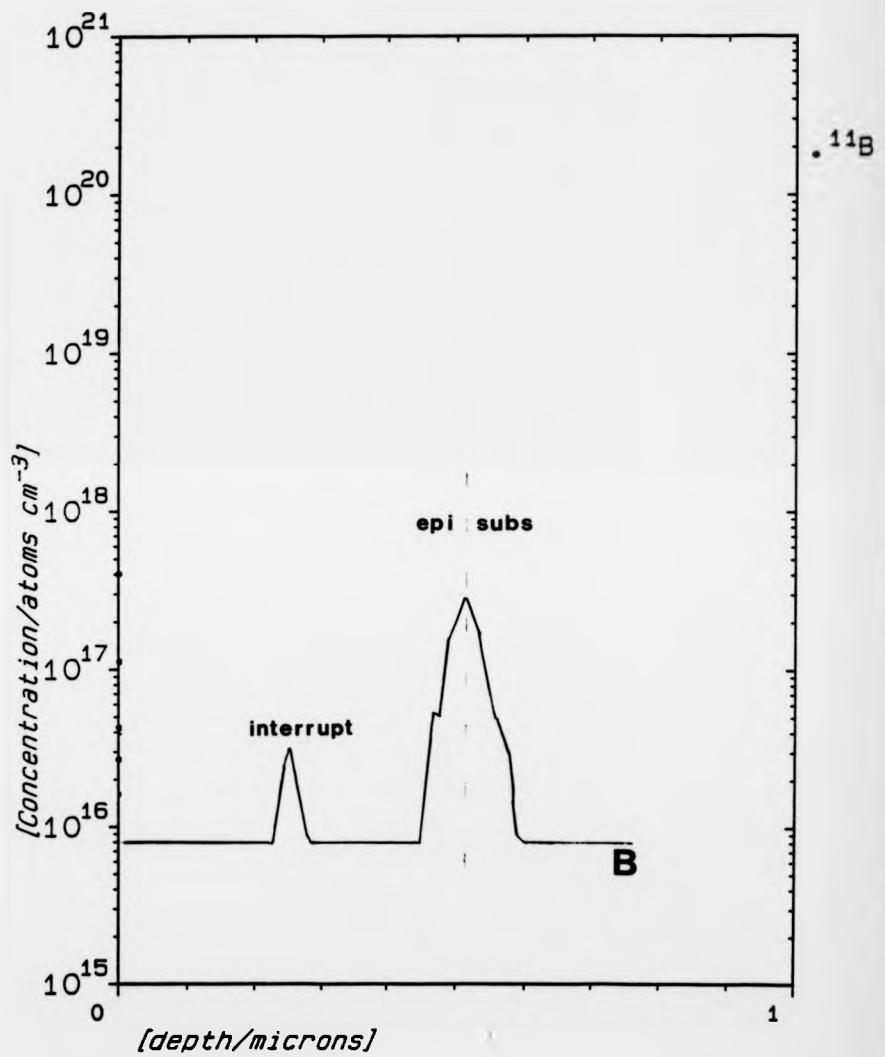
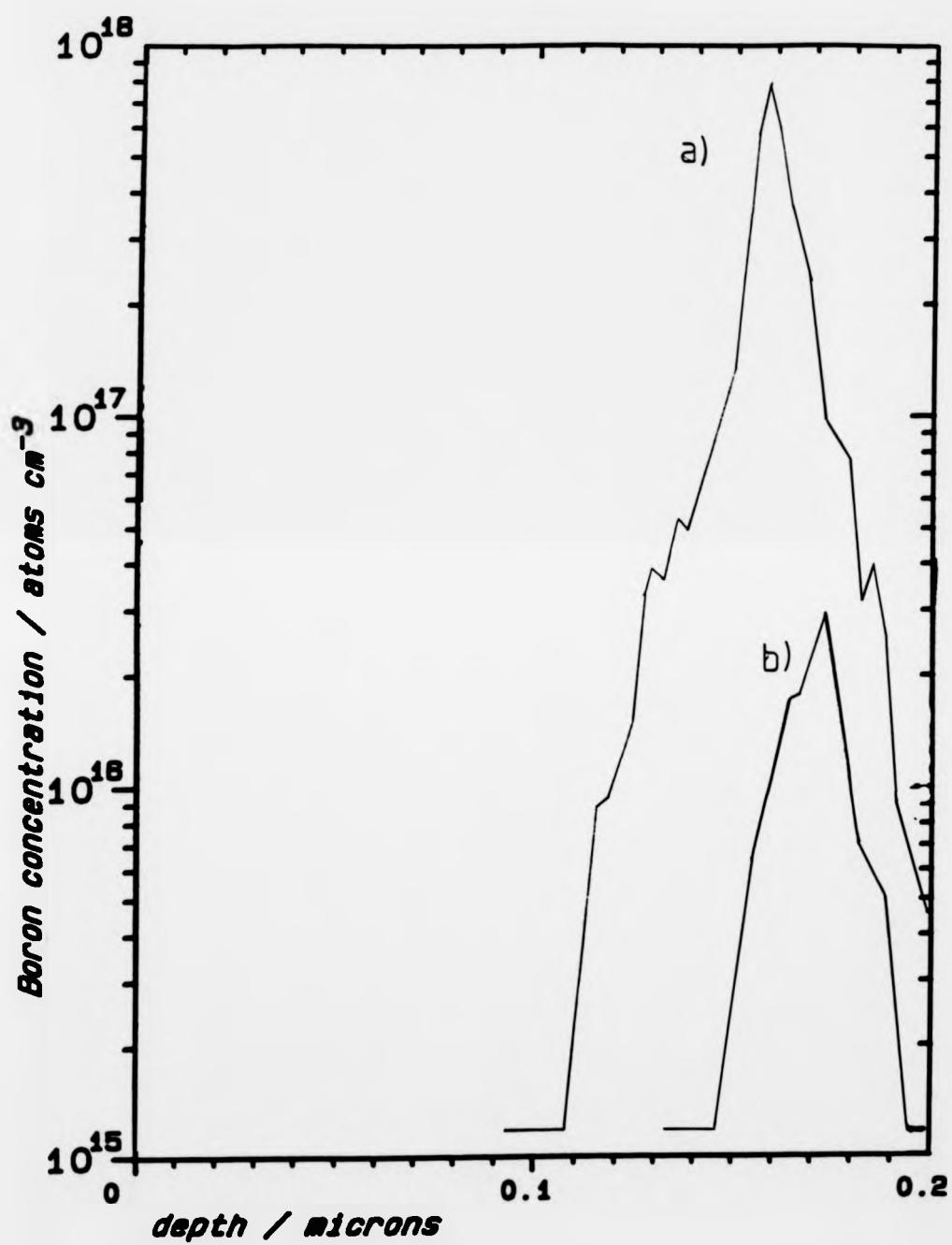


Fig. 3.12 A SIMS profile through an epilayer containing an interrupt and exposure to research grade  $\text{O}_2$  at a pressure of showing that this process also causes the contamination to occur. (SIMS carried out by Mark Dowsett, Warwick University)

SiC, although the C impurity usually acts as a donor in Si <Sze, 1981>. It may be the case that the acceptor was B, caused by the same mechanism as noted here during MBE.)

These results led to the assumption that a reaction occurred between the oxide layer produced during oxygen or air exposure and B rich system components. The main components were pBN source cells and insulators, and borosilicate glass viewports. Removal of all pBN from the system produced no decrease in interfacial contamination. However, replacement of the borosilicate viewports with ones made of quartz had a dramatic effect. Fig. 3.13 shows SIMS profiles comparing the interfacial regions of two epilayers grown under the same conditions ( $T_s=800^\circ\text{C}$ ), but one with borosilicate viewports, the other with quartz. A fifty-fold reduction of interfacial B was evident. The quartz viewports used still contained some borosilicate in the graded seal between the quartz and the stainless steel, since a direct seal between the two is difficult to achieve. Viewports with such a seal are available, but are not suited to use in MBE since the solder used for the join softens at temperatures below those required for bakeout (they are also about ten times more expensive than their borosilicate counterparts).

B contamination of Si surfaces in UHV has been noted previously in glass systems <Allen et al, 1960>, at even higher levels than those seen in MBE layers. The mechanism suggested for transport of the B to the Si surface was that  $\text{B}_2\text{O}_3$  on the surface of the glass reacted with water vapour



### Si epilayer by MBE

Fig. 3.13 SIMS profiles of epilayers grown a) with borosilicate glass viewports and b) with graded-seal quartz viewports. (SIMS carried out by Mark Dowsett, Warwick University)

during bakeout, to form volatile hydroboric acid ( $\text{HBO}_2$ ), for which  $\text{SiO}_2$  has an affinity. This hypothesis is not, however, in agreement with the results of the present study, in which exposure to dry research grade  $\text{O}_2$  also led to B contamination. To elucidate further the role of moisture, substrates were heated to  $300^\circ\text{C}$  for 5 minutes in the system load lock [which had no windows] to ensure complete removal of all water vapour prior to insertion in the deposition chamber, fitted with borosilicate viewports. This process had no effect on the magnitude of the B spike, giving further indication that water vapour was not involved in the contamination process.

Allen et al <1960> suggested that boiling the borosilicate ports in distilled water for 48 hours would remove the  $\text{B}_2\text{O}_3$ -rich surface left after manufacture, to remove the source of B. This was tried in this series of experiments, but its effect on contamination was negligible. This apparent difference in the effect of the boil treatment may have been due to the relatively high initial surface concentrations seen by Allen et al [ $10^{12}\text{-}10^{15}\text{cm}^{-2}$ ], and the insensitivity of the detection technique then used. This was total sample resistance measurement followed by surface etch, which might not have been able to detect the low levels of B induced on the Si surface after the viewports had been boiled.

Similar B surface accumulation has been noted during high temperature annealing of Si <Liehr et al, 1987>. Although no elucidation of the mechanism for the formation of the surface layer was given, the anneal results showed that

total B concentration was independent of anneal time [ $1000 < T_{\text{anneal}} < 1300^{\circ}\text{C}$ ]. This implied that diffusion was occurring from an initial source present prior to annealing, and that no additional contamination was caused due to contamination during the anneal period. This is consistent with the theory that the silicon oxide played a vital role in the *in-situ* formation of the B accumulation.

The wet chemical clean carried out prior to MBE growth was found to have an effect on the concentration of B. Fig. 3.14 shows SIMS profiles of three epilayers grown under similar conditions after various chemical cleans, with all but one of the borosilicate viewports replaced with graded-seal quartz. (The one remaining borosilicate port was retained since a large (FC 120) port was necessary during normal running for adequate observation during substrate manipulation, and a graded quartz replacement of this size was not available. Line of sight to the substrate was kept to a minimum by use of a stainless steel shutter.)

Fig. 3.14a shows the interfacial spike from an epilayer grown under these conditions onto an as-received substrate, with a peak concentration of  $2 \times 10^{17} \text{ cm}^{-3}$  (integrated areal total =  $7 \times 10^{11} \text{ cm}^{-2}$ ). Fig. 3.14b was for an epilayer grown on an RCA-cleaned (Kern and Puotinen, 1970) wafer. The peak height here was  $1.1 \times 10^{18} \text{ cm}^{-3}$  (integrated areal concentration  $2 \times 10^{12} \text{ cm}^{-2}$ ). Finally, Fig. 3.14c shows a SIMS profile through an epilayer grown on a wafer cleaned using a 5min,

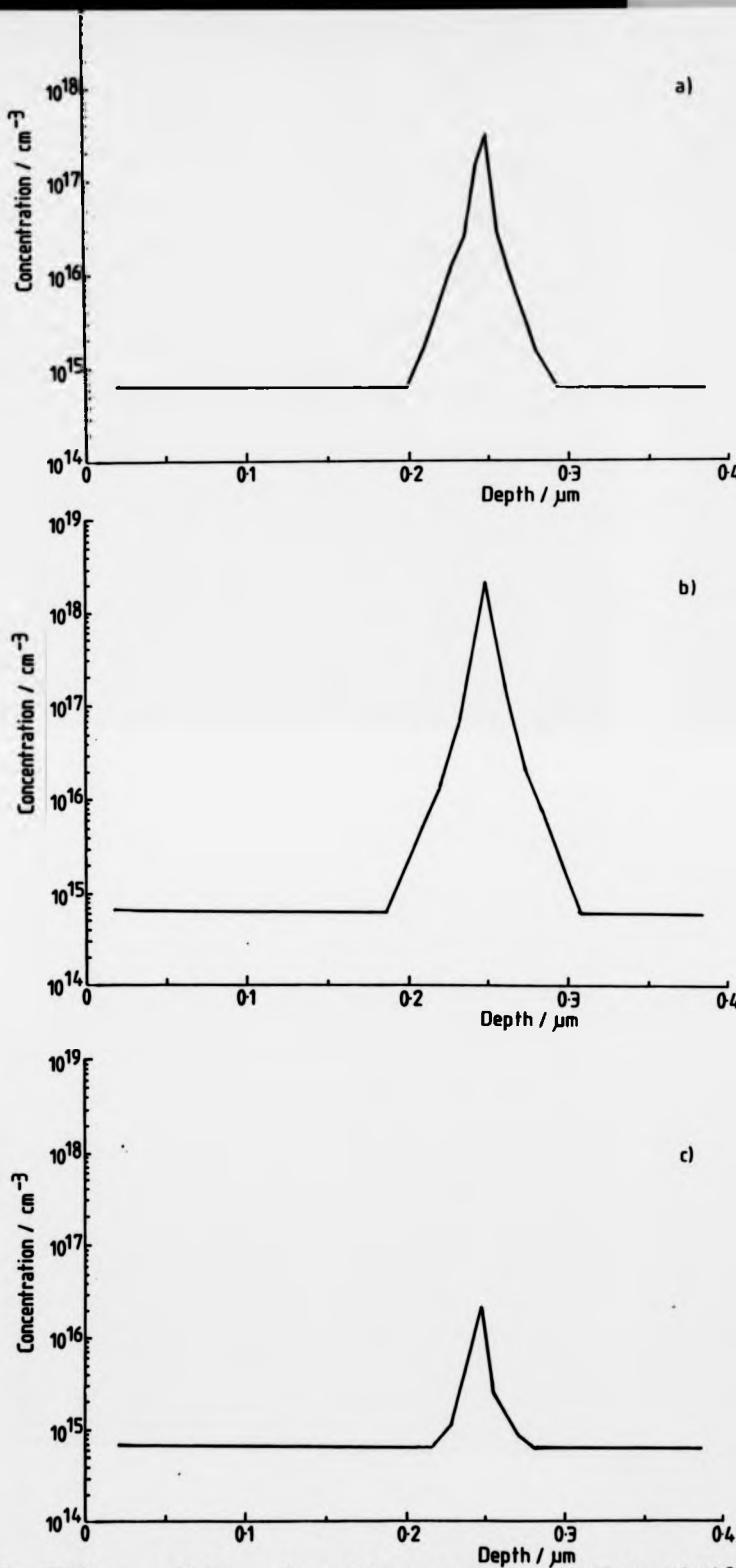
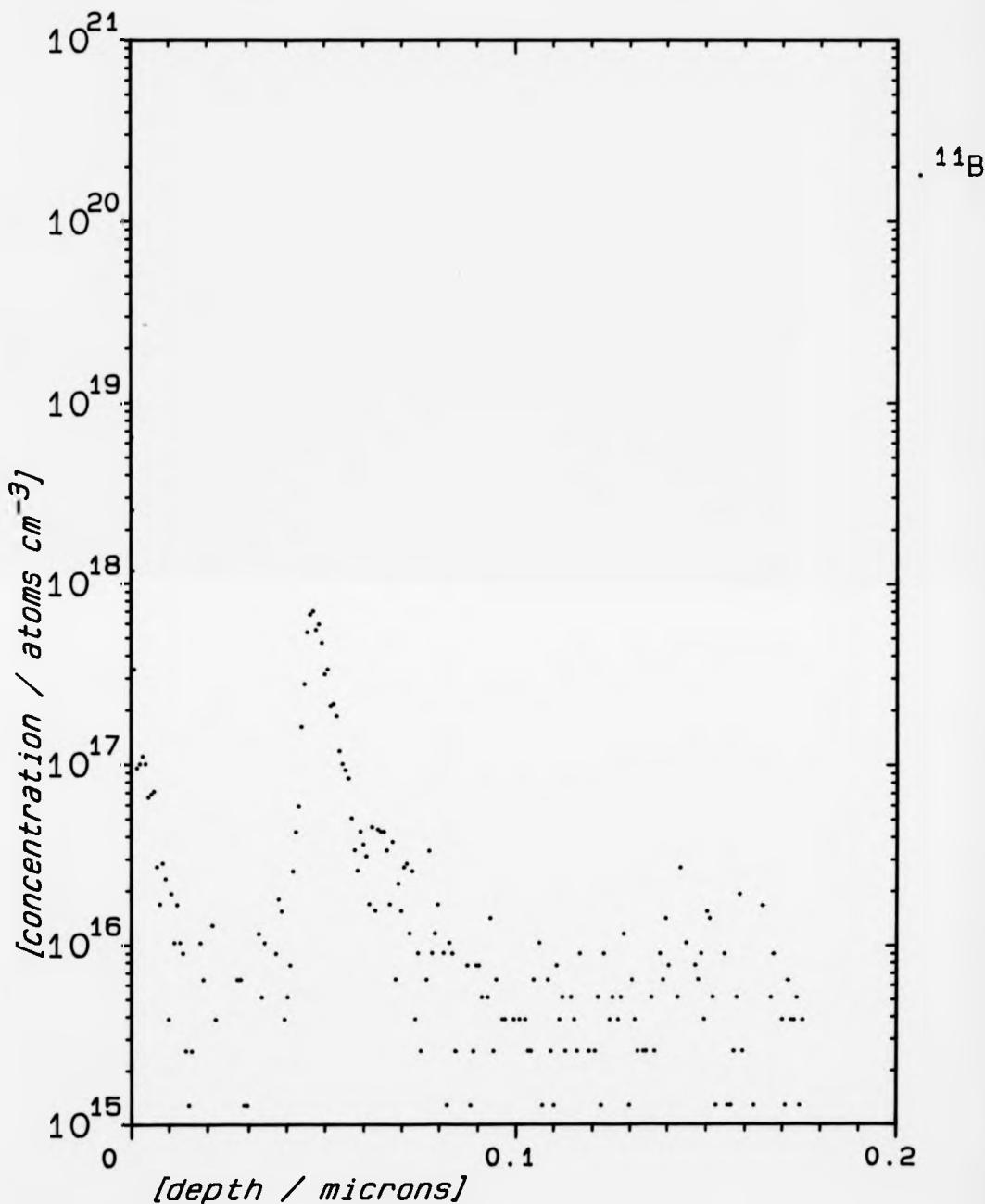


Fig. 3.14 SIMS profiles of epilayers grown under similar growth conditions after various ex-situ cleans: a) as-received, b) RCA cleaned, c) HF dip. (SIMS carried out for the author by Loughborough Consultants)

2.5% HF dip. The peak height was  $2 \times 10^{16} \text{ cm}^{-3}$  (integrated areal concentration  $1 \times 10^{11} \text{ cm}^{-2}$ ).

The reason for this dramatic difference in B contamination must be due to the oxide produced by each cleaning procedure. The as-received wafer would have the native oxide (.20A thick), the Shiraki clean produces a thick (>30A) oxide on the Si surface, whilst the HF dip leaves only a very thin (<10A) oxide layer (see section 3.3.2). The amount of B incorporated thus seemed to be dependent on oxide thickness when the substrate was introduced into the growth chamber.

This implies that the oxide layer must either have contained the contamination prior to insertion into UHV, or caused its adsorption *in vacuo*. To test the hypothesis that the B spike was induced during the substrate heating process, the author grew an amorphous Si layer at room temperature, in order to trap the native oxide of an as-received wafer without any heat treatment. This was analysed by SIMS, which showed that B was present at the amorphous layer/substrate interface (Fig. 3.15), so heating was not involved in the contamination process. This is in agreement with recent work on bevelled SIMS imaging, which found that B was present on the surface of any Si with an oxide present, but in much lower quantities when an HF dip had been performed just prior to imaging <James, 1990>. It seems probable that B is picked up from the atmosphere, probably in the form of gaseous  $\text{B(OH)}_3$ , which is known to be present in air <Fogg et al, 1983>.



#### AMORPHOUS CAP EXPERIMENT

Fig. 3.15 A SIMS profile of an amorphous Si layer grown at room temperature with no heating prior to growth (i.e. no oxide removal). B contamination is still evident.

### 3.4.3 Discussion and conclusion.

The initial magnitude of the p-type spike at the epilayer/substrate interface was sufficient to cause deleterious and unreproducible effects if the interface were to be used for p-n junction isolation of the epilayer. SIMS results have shown that the acceptor was B, and comparison with eCV profiles has shown activation levels of between 5 and 30%. There seem to be two separate sources of this contamination. The first was the borosilicate viewports employed in the system, and their replacement with graded-seal quartz (i.e. still containing a small amount of borosilicate) showed a fifty-fold reduction in the level of interfacial B. The presence of an oxide layer was found to enhance the level of contamination, the concentration of B being dependent on the oxide thickness, as shown by the effects of various chemical cleans. It was also apparent from room temperature studies and SIMS imaging that contamination occurred from the atmosphere via an oxidised form of B such as  $B(OH)_3$ .

It has previously been proposed that the mechanism behind the transport of B from the viewports to the Si wafer was dependent on the presence of water vapour in the oxide layer, which evaporated as the wafer was heated and reacted with  $B_2O_3$  in the glass to produce volatile boric acid, for which silicon dioxide has an affinity. The results of this study, however, disagree with this assumption, since an oxide layer caused by exposure to moisture free  $O_2$  also caused the

contamination. The vapour pressure of  $B_2O_3$  and  $B(OH)_3$  are negligible at room temperature < Tatsumi et al, 1987> so the precise method of transfer is unclear. It may be the case that a layer of oxidised B was deposited around the system during bakeout, and that hot system components acted as secondary sources during growth, although thorough outgassing of all components prior to growth had no effect on B contamination levels.

### 3.5 Summary.

The aim of this study was to determine the optimum substrate cleaning procedure to be carried out prior to epitaxy. The acidic chemical cleans have been found to significantly reduce dislocation levels compared with the use of 'as received' wafers. However, the oxide grown by this method is the stable equilibrium phase of  $SiO_2$  which requires heating to  $>800^{\circ}C$  for removal. Wafers treated by only a dilute HF dip proved to yield epilayers with consistently lower defect levels, but have been shown by X-ray fluorescence to introduce metal contamination. However, annealing experiments have shown that Cu can be gettered at the interface rather than diffusing uniformly through the epilayer. Thus contamination introduced during the ex-situ substrate clean can be confined at the interface.

The B spike found to be present at the interface has been minimised by the removal of borosilicate viewports

where possible, and replacement with quartz, since the borosilicate was found to be a source of contamination. It was noted that the presence of an oxide layer was required for contamination to occur in this manner. Another source was atmospheric B compounds, which seem to accumulate on any air-exposed Si surface. This source can be reduced by performing an HF dip immediately prior to growth, while growth of a buffer layer minimises the effects of the B spike.

The standard substrate clean now adopted for optimum quality epilayers is a 2 minute dip in 2.5% HF solution, followed by a 30 minute rinse in flowing DI. *In-situ*, a 20A Si capping layer is deposited at 350°C followed by thermal desorption for 7 minutes at 720°C. This method has been chosen because of the low defect densities yielded, the low temperature required for oxide desorption and the ease of reproducibility of the chemical cleaning stage. Finally, before growth of the active region of the epilayer, a buffer layer 0.1-0.5um thick is grown to bury any interfacial contamination, and in most cases to form one side of a p-n junction with the device. This gives epilayers with defect counts of  $\sim 10^3 \text{cm}^{-3}$ , which although higher than can be achieved by CVD, is adequate for most research purposes.

## Chapter 4. Residual doping.

### 4.1 Introduction.

The growth of nominally undoped epilayers, i.e. those with no intentional impurities present, can give an excellent insight into the basic properties of MBE-grown material.

Surface interactions during growth are Si-Si rather than with a dopant adlayer, providing the ideal situation for step propagation growth. Knowledge of this undoped growth regime is also vital for the growth of 2-D electron gas devices in which the carriers flow in the undoped region.

Although the clean UHV environment in which the layers are deposited reduces the interaction of contaminants and the clean Si surface, the equivalent of a monolayer of atoms is still impinging on it every few seconds. In practice, the small amounts of impurities which are in the ambient, or generated by materials used in the system and the growth process itself, yield Si containing a finite, and detectable, quantity of contaminants.

These can be divided into three categories, dependent on their electrical properties. Some will be neutral, thus rendering them difficult to detect, especially at low levels. Their neutrality means that they have no effect on the electrical properties of the crystal, but if they are neutral due to the complexing of ionised impurities, such a complex may lead to the formation of a crystallographic defect <McFee et al. 1983>. The second type are those which have energy

levels deep within the Si bandgap. Although they do not cause significant charge carrier formation, they act as effective traps for intentional carriers, and degrade minority carrier lifetimes. They can affect device performance, allowing soft junction breakdown and high leakage currents <Ravi, 1981>. The presence of such traps and their properties will be discussed in Chapter 5. The third type of impurity, and those of major interest to us in this chapter, are those with shallow levels, i.e.  $E_A < 0.1\text{eV}$  below the conduction or above the valence band edges. These form donors and acceptors respectively, which will change the carrier concentration and thus have a strong effect on the material's electrical properties, and are the cause of the residual doping level.

Since the type and concentration of these impurities is dependent on the growth process and materials used, the problems that occur are unique to MBE, and indeed vary from system to system. From analysis of the properties of the unintentional states, the type of impurity present can be determined, and hence, hopefully, its source found, thus allowing minimisation of contamination.

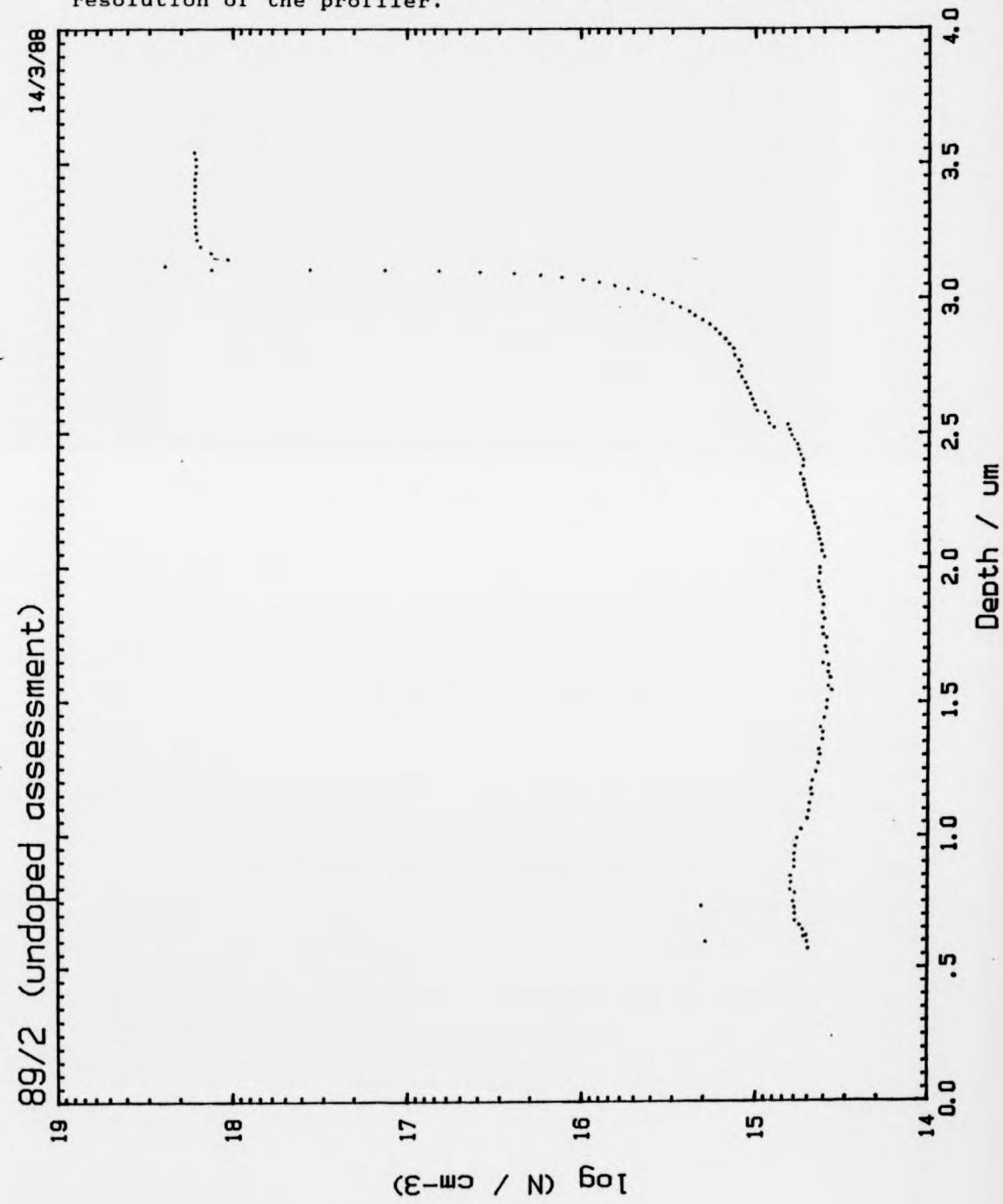
Apart from the interest in nominally undoped material to assess the basic material properties, the control and minimisation of background doping is important for device work. Sharp dopant spikes used to create energy wells may need to be deep to confine carriers properly <Mattey, 1989>, and the barrier height must be known and reproducible. Also the minimum level of intentional doping required to

overcome the background must be known precisely, if a low-doped region needs to be of the opposite type to the residual doping.

#### 4.2 Electrochemical CV [eCV] Profiling.

The standard method of electrical analysis used for examining the residual doping level of epilayers was that of eCV profiling using a Polaron PN4200 plotter. The carrier concentrations of interest here were approaching the lower limit at which the profiler could operate accurately <Pawlik et al, 1986> but results taken were to within +/- 30%. Fig. 4.1 shows a typical profile of an undoped epilayer grown during a series where no dopant sources were fitted to the MBE system. It shows a uniform level of n-type background doping through the layer, at a carrier concentration of  $5 \times 10^{14} \text{ cm}^{-3}$ . This was comparable with a four point probe uniformity scan. Quoted concentrations are as measured by eCV unless otherwise stated.

Fig. 4.1 eCV profile of typical undoped epilayer. The broadening of the interface is due to the increase in Debye length at such low carrier concentrations, which limits the resolution of the profiler.



#### **4.3 Determination of background dopant.**

##### **4.3.1 Dependence of residual doping on growth conditions.**

The effect of changing growth parameters on the residual carrier concentration was examined to try to determine the nature of the dopant. Variation of substrate temperature between 500 and 740°C had no discernable effect on concentration, as can be seen in Fig. 4.2. Growth rate in the range 3 to 12A/s was also found to have no noticeable effect on doping level [Fig.4.3].

This behaviour was unusual for dopants in MBE. Those with non-unity sticking coefficient usually form an adlayer on the growth surface, and display a strong substrate temperature dependence. This is because the bond strength of these dopants on the Si is such that the majority of the adlayer is desorbed before incorporation can occur. The surface residence time is short; the adlayer is in a state of dynamic equilibrium, with almost as many atoms desorbing as adsorbing, only a small percentage being incorporated.

The desorption process, and thus the equilibrium surface coverage, is naturally strongly temperature dependent. As incorporation occurs directly from the adlayer, which acts as a dopant reservoir, the incorporation rate is also dependent on temperature. Such dopants are not growth rate dependent as the rate limiting factor is

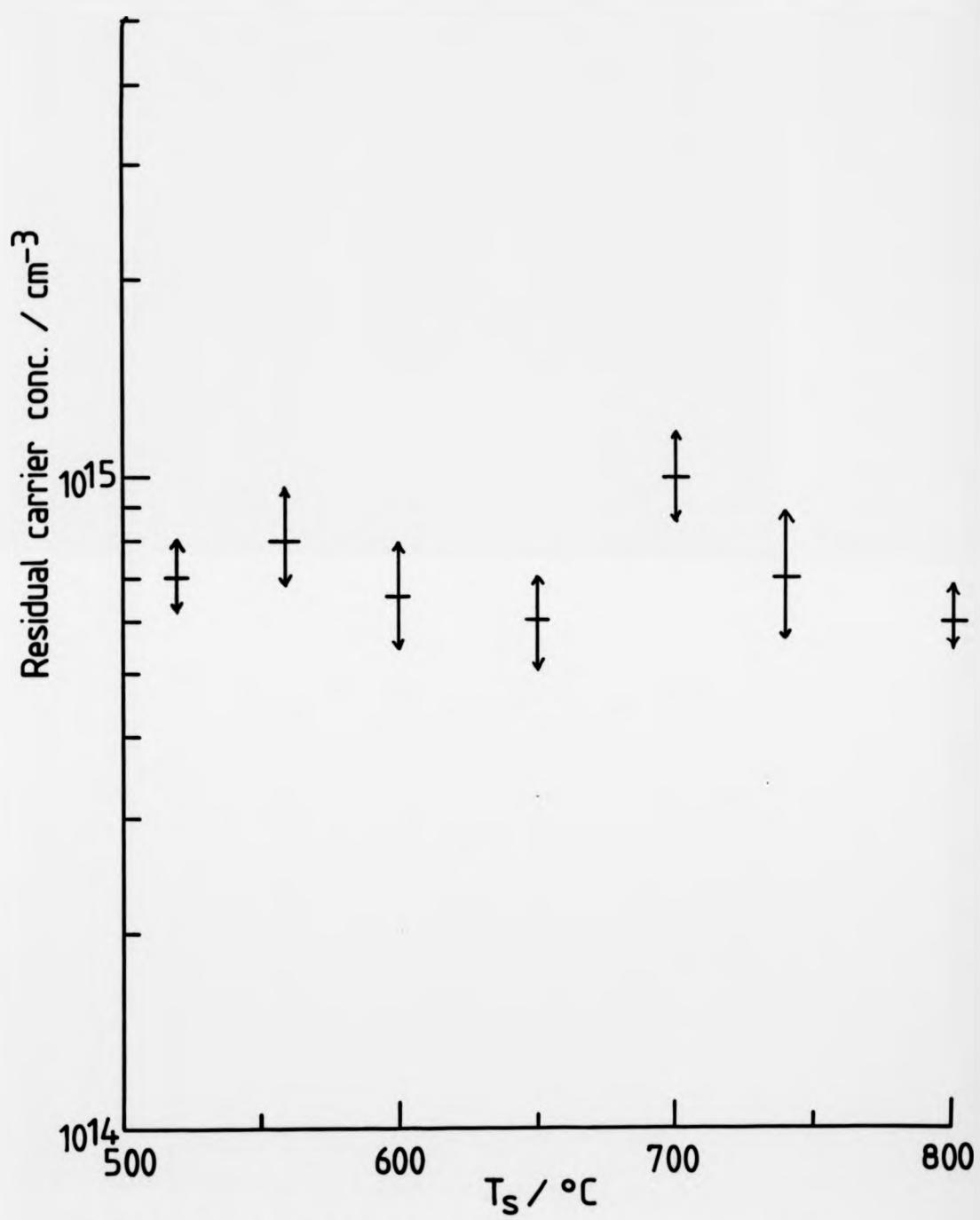


Fig. 4.2 Graph illustrating the negligible effect of substrate temperature on residual carrier concentration.

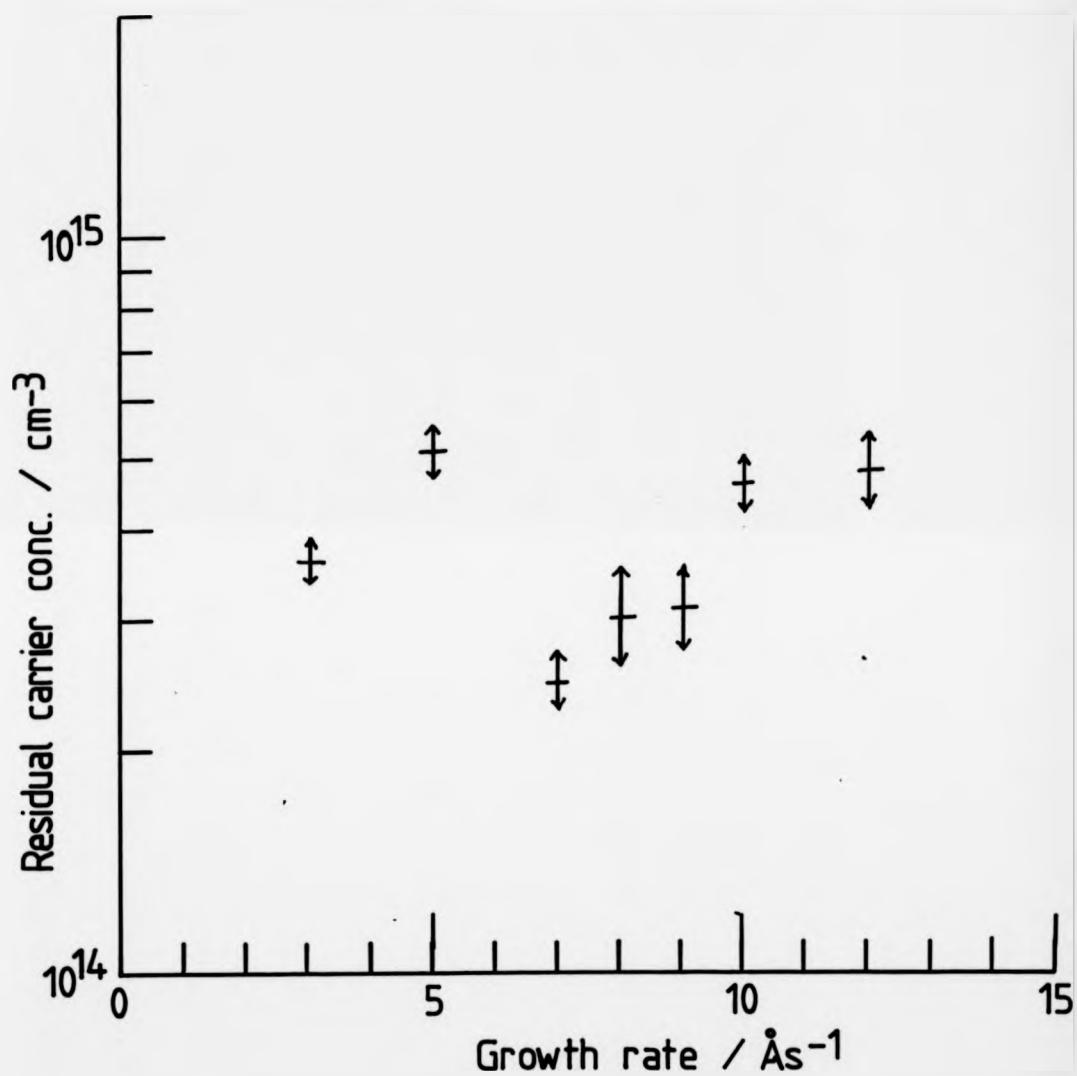


Fig. 4.3 Graph illustrating the negligible effect of growth rate on residual carrier concentration.

incorporation site availability rather than lack of available dopant atoms.

B has a unity sticking coefficient on Si since enough thermal energy to overcome the surface chemisorption is not available at the growth temperatures used, so desorption cannot occur. This means B incorporation is independent of  $T_g$  in the range studied. It is, however, dependent on growth rate, as the rate limiting step for doping is the arrival of B atoms. As growth rate increases the ratio of B atoms to Si atoms arriving at the surface decreases, giving a carrier concentration inversely proportional to deposition rate.

The only known dopant that exhibits similar properties to those observed here is phosphorus, thus giving a positive identification. Phosphorus does not have a unity sticking coefficient, and doping is independent of growth rate. It is also almost independent of substrate temperature, showing only a factor of two change in carrier concentration over a substrate temperature range of between 650 and 820°C <Kubiak et al, 1986>. The abruptness of high-low transitions is sharper than for Ga and Sb, implying little or no surface segregation or adlayer formation. Further conformation of the absence of an adlayer was obtained when a negative bias was applied to the substrate as in the potential enhanced doping technique (see section 1.1). This negative bias had no effect either on intentional P doping, or the residual doping studied here. The fact that an adlayer plays no part in its incorporation kinetics goes some way to explaining the independence from temperature. It would seem that at the

substrate temperatures used the residence time of P atoms on the growing surface is extremely short, too short for adlayer formation to occur. Most immediately desorb, and so incorporation becomes independent of temperature, but is rather a function of lattice site availability. The higher the growth rate the greater the availability of lattice sites, so dopant concentration is independent of rate. These surface kinetics imply spontaneous incorporation into the lattice, indicating the background dopant is phosphorus.

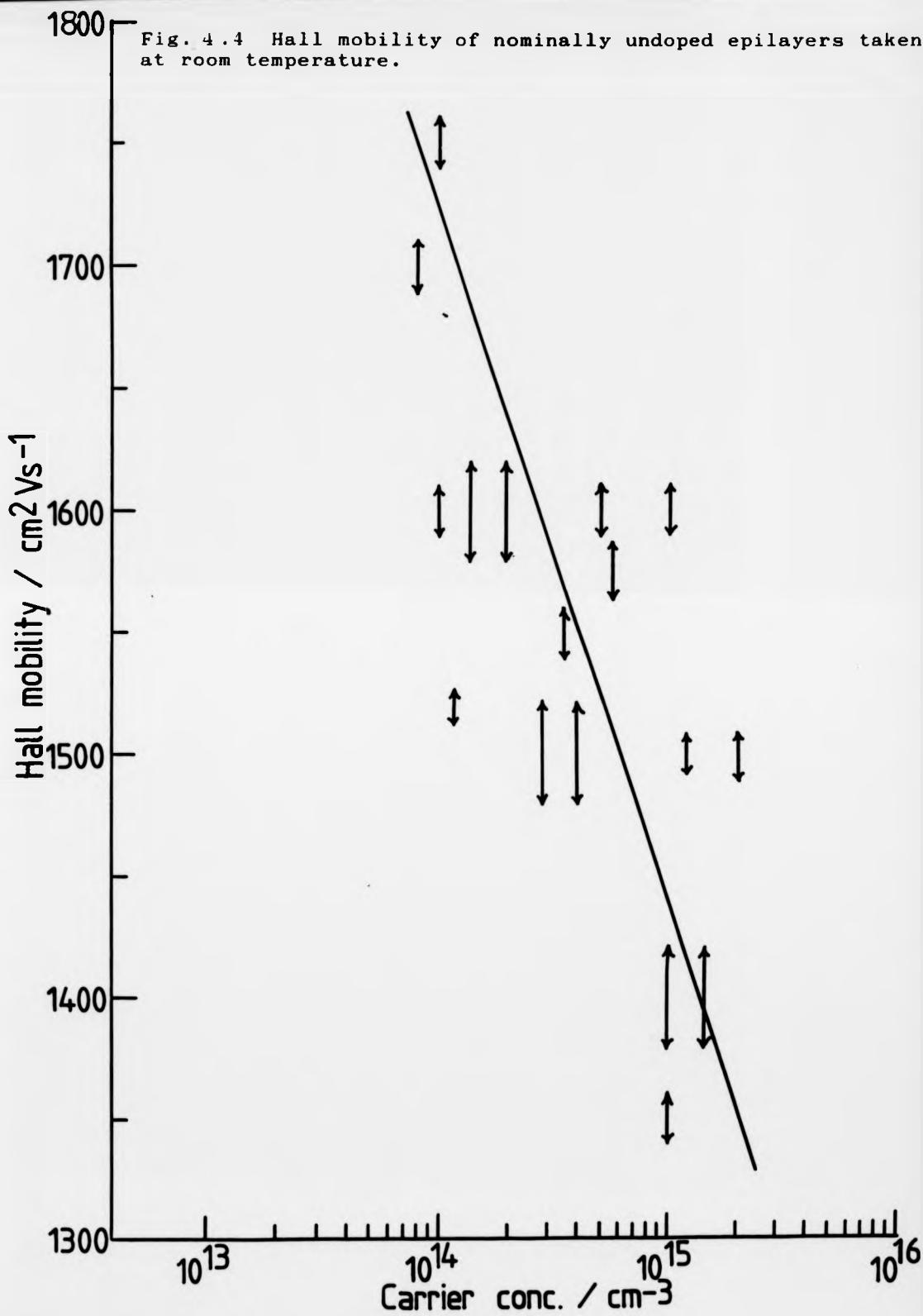
#### 4.3.2 Hall measurements.

Although eCV profiling gives the level of residual doping it cannot give information on the nature of the impurity present. As well as giving information on carrier concentration and mobilities, Hall measurements over a range of temperatures allow the activation energy of the dopant to be determined, thus giving an insight into the cause of the residual doping.

Fig. 4.4 shows the variation of Hall mobility with carrier concentration at room temperature (300K) . The mobility is comparable with that of bulk Si <INSPEC, 1988>. This graph also illustrates the range of carrier concentrations we have seen in "undoped" layers.

Fig. 4.5 shows carrier concentration variation with temperature, showing the expected carrier freeze-out. Fig.

Fig. 4.4 Hall mobility of nominally undoped epilayers taken at room temperature.



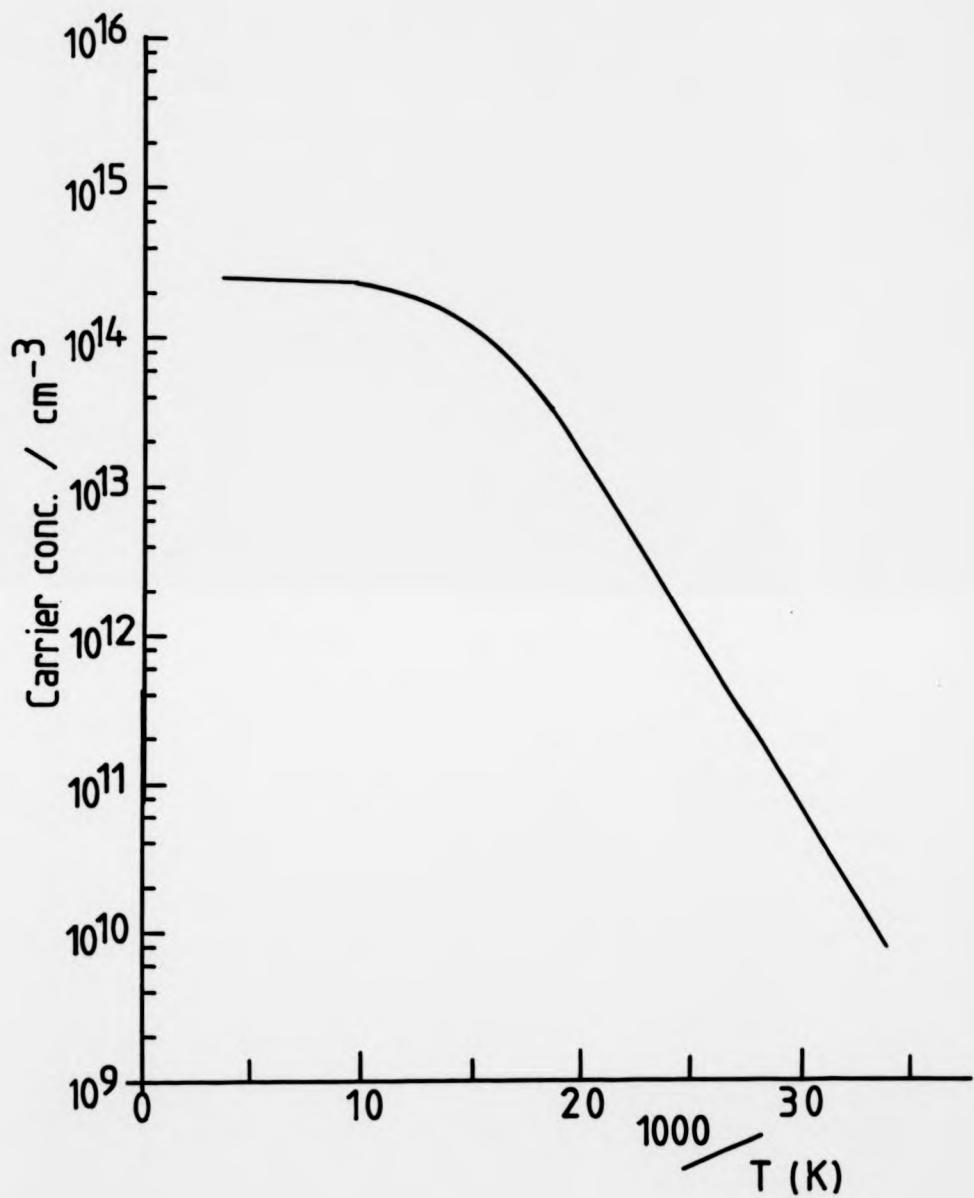


Fig. 4.5 Carrier concentration against reciprocal temperature, showing carrier freeze-out.

4.6 is a replot of these data, using  $\ln(n)$  as the ordinate in order to calculate  $E_A$  from the gradient. For an n-type semiconductor (neglecting holes and neutral acceptors), the general equation relating carrier concentration variation with temperature to the activation energy,  $E_A$ , of the donor can be written as <Seeger, 1985>,

$$\frac{n(n+N_A)}{N_D-N_A-n} = \frac{N_C}{gD} \exp \frac{-E_A}{kT} \quad [4.1]$$

where  $n$ =free carrier concentration

$N_C$ =effective density of states in the conduction band, given by

$$N_C=2(2 m^* kT/h^2)^{3/2}$$

$m^*$ =effective mass of electron

$N_A$ =number of ionised acceptor sites

$N_D$ =number of donor sites

$g_D$ =impurity spin degeneracy

$k$ =Boltzmann constant

$T$ =absolute temperature

Although this method gives only an estimate of  $E_A$  (since, for example, compensation, and the dependence of  $E_A$  on doping level are neglected), it is sufficient to identify the dopant present.

A carrier concentration versus reciprocal temperature curve can be split into three general regions: low temperature (<80K) where  $n < N_A$ , intermediate temperatures (80-200K) where  $n > N_A$ , and high temperatures (>200K) when the

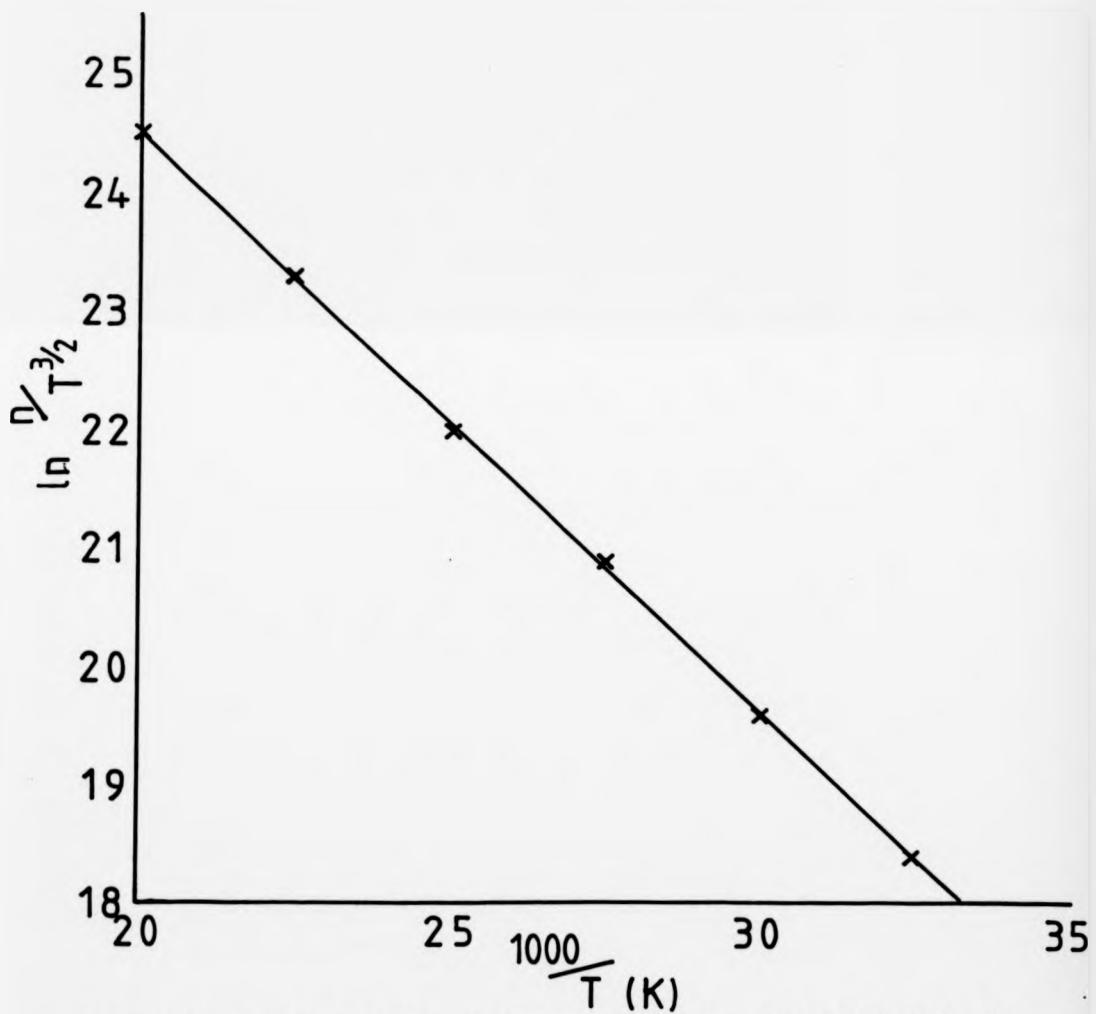


Fig. 4.6 Replot of the data in Fig. 4.5. The gradient of this line can be used to calculate the activation energy of the dopant, and thus aid its identification.

exhaustion region is reached. It is the low temperature that is of interest to us here, where we may assume  $n \ll N_A$  and  $N_D - N_A$ . This allows equation (4.1) to be rearranged as

$$n = \frac{N_C (N_D - N_A)}{g_D N_A} \exp \frac{-E_A}{kT} \quad (4.2)$$

A plot of  $\ln(n)$  against reciprocal temperature [Fig. 4.6] therefore yields a straight line of gradient  $E_A/k$ . From this graph  $E_A$  was found to be  $0.045 \pm 0.001\text{eV}$ . This activation energy indicates that the residual dopant is P, for which the accepted value of  $E_A$  is  $0.044\text{eV}$  *<Sze, 1981>*.

#### 4.3.3 PL analysis.

PL, carried out by King's College, was also useful in determining the residual dopant in Si layers. This method was particularly useful because, despite the qualitative nature of the data yielded, it has comparatively low detection limits when compared with techniques such as SIMS. This allowed detection of impurities in the p.p.b. (generally the detection limit was  $\sim 10^{12}\text{cm}^{-3}$ ) range as was the case for the lowest background doping levels. Thick ( $>5\mu\text{m}$ ) layers were used for these analyses, to allow relatively strong luminescence, and were generally grown on p-type substrates to avoid any ambiguity between epilayer and substrate luminescence.

The PL spectrum in Fig. 4.7 shows a spectrum from an epilayer exhibiting relatively high donor luminescence. The

peak at  $8800\text{cm}^{-1}$  shows that the background dopant was phosphorus, which is in agreement with the findings of the Hall experiments to ascertain activation energy. An As peak in some layers has also been noted. However, not all epilayers examined showed such clear emission from the dopant, even on some layers with relatively high residual levels ( $>10^{15}\text{cm}^{-3}$ ). Recent results have suggested that this was due to metallic impurities which increase the strength of the D1-4 lines at the expense of dopant luminescence.

Experiments carried out by King's college <unpublished>, involved diffusing metals into layers and then reassessing them by PL. These indicated that certain metals, especially Ni and Cu, had a strong effect on the PL spectrum produced. Fig. 4.8 shows three spectra carried out under the same conditions from the same epilayer, unannealed, annealed and after Cu diffusion during anneal. These showed the decrease in both donor and substrate luminescence for the Cu diffused sample. The reasons for this are as yet unclear, but the phenomenon is currently being studied in collaboration with King's College. It would appear that dislocations getter metallics and these form efficient recombination centres, competing with the dopant luminescence process. The dislocation density in the epilayer was found to have an influence on the optical properties of layers after metal diffusion, which substantiates this idea.

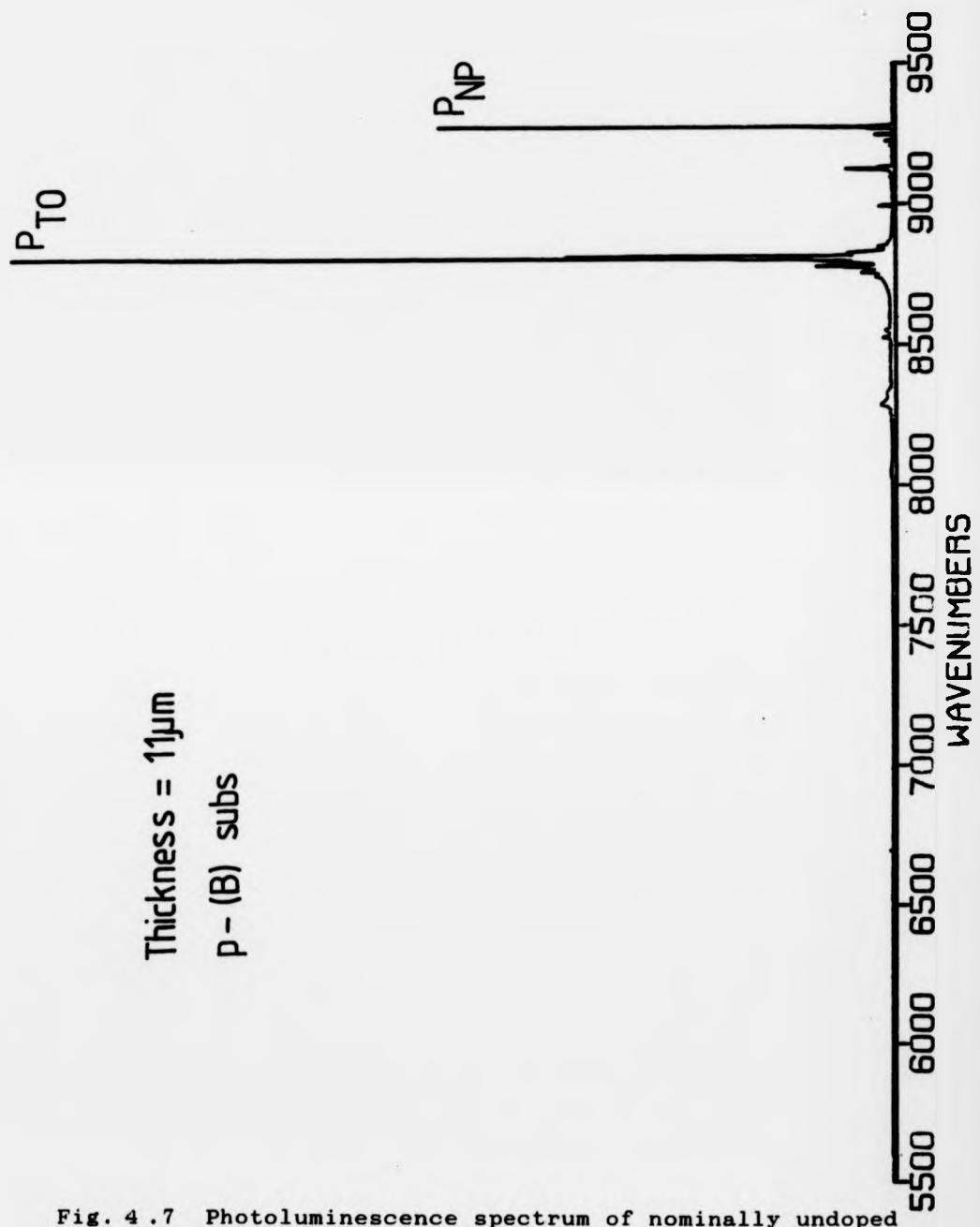
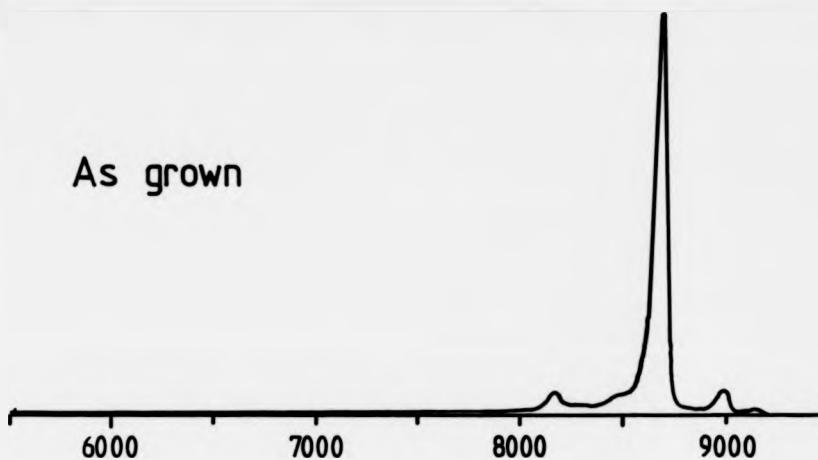
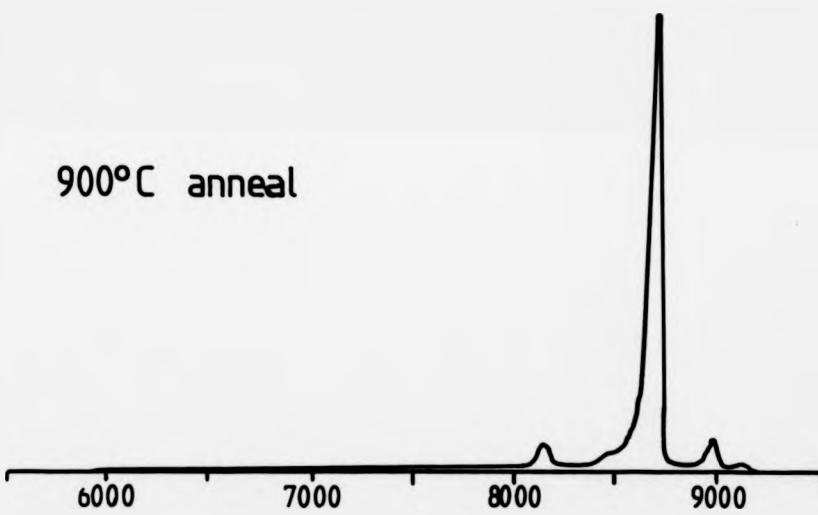


Fig. 4.7 Photoluminescence spectrum of nominally undoped epilayer demonstrating clear phosphorus luminescence.  
(PL carried out by Kings College, London)

As grown



900°C anneal



900°C anneal + Cu in-diffusion

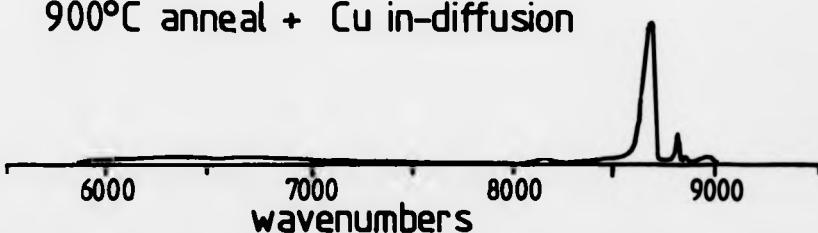


Fig. 4.8 PL spectra demonstrating the effect of annealing and Cu in-diffusion on the optical properties of an MBE layer. A simple anneal at 900°C shows little change. The effect of the introduction of Cu, however, is to weaken dopant luminescence, in preference to the dislocation-associated D lines. (PL carried out by Kings College)

It was also found that luminescence varied considerably across the wafer. Fig. 4.9 shows the spectra obtained from a single epilayer from samples taken from centre to edge. The defect density near each sample was also counted, and a correlation between the two noted. This variation implies that caution must be exhibited when directly comparing emission spectra from two different epilayers, or even from different areas of the same wafer.

#### 4.4 Factors affecting background doping.

##### 4.4.1 System parameters.

The source of phosphorus has been postulated <Iyer, 1988> to be the 304 grade stainless steel from which MBE systems are generally constructed, phosphorus diffusing along grain boundaries during bakeout. This agreed with findings of this study that residual carrier concentration was increased after bakeout but reduced during the growth run. Fig. 4.10 shows carrier concentration against epilayer number within a typical undoped growth series. The first epilayer grown in a series, i.e. directly after bakeout, had a doping level in the mid- $10^{15}\text{cm}^{-3}$ . Over the next few layers the residual level dropped to  $<10^{15}\text{cm}^{-3}$ , suggesting that the source of P was becoming depleted, or buried by evaporated Si. After the growth of about 20um of material a concentration of  $1\text{-}2\times10^{14}\text{cm}^{-3}$  was reached, below which the

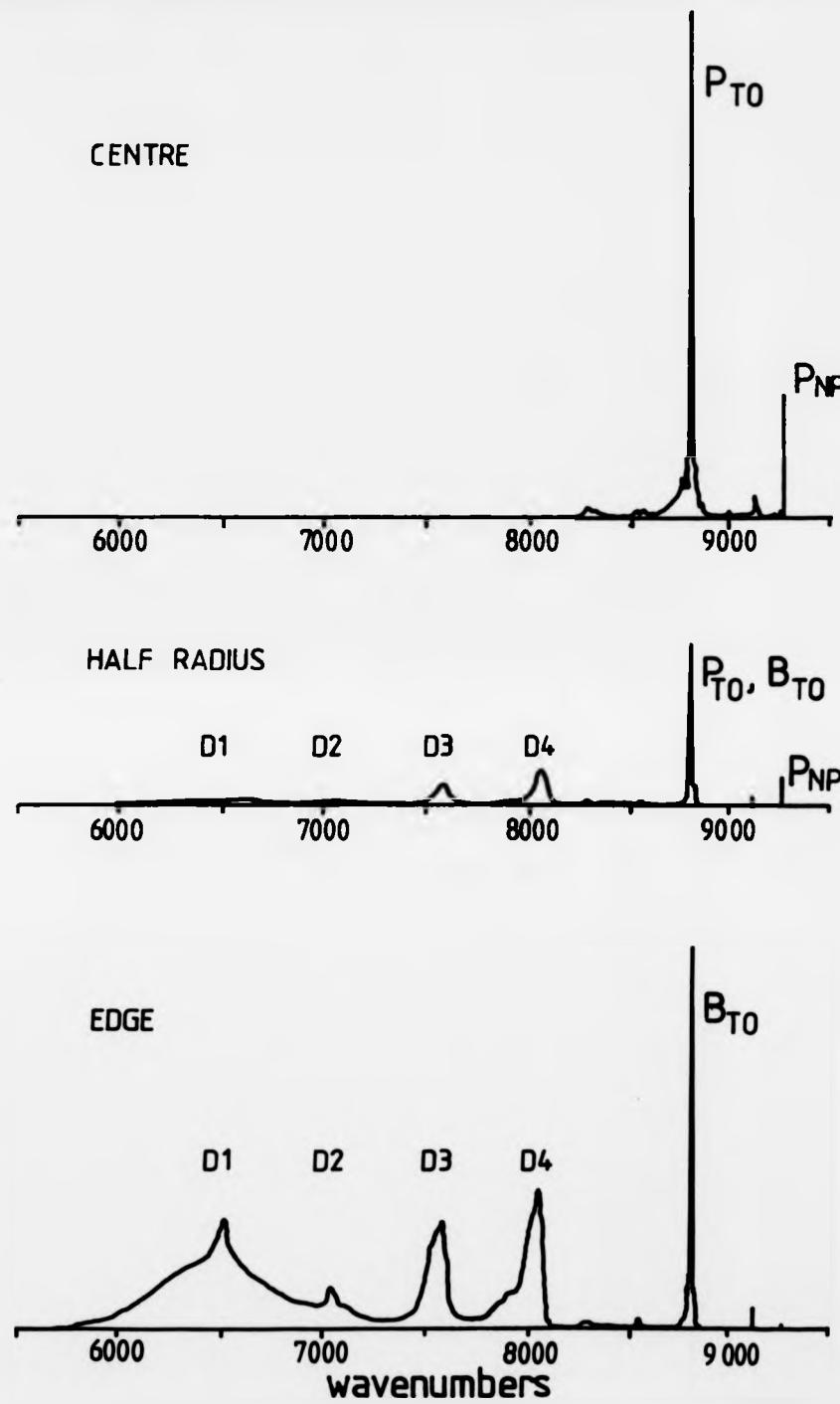


Fig. 4.9 PL spectra showing the variation of properties across the wafer. This change correlates with a change in dislocation level in this sample. It is interesting that the phosphorus peaks from the epilayer become completely masked by the boron peak from the substrate.

(PL carried out by Kings College)

Run 36/X

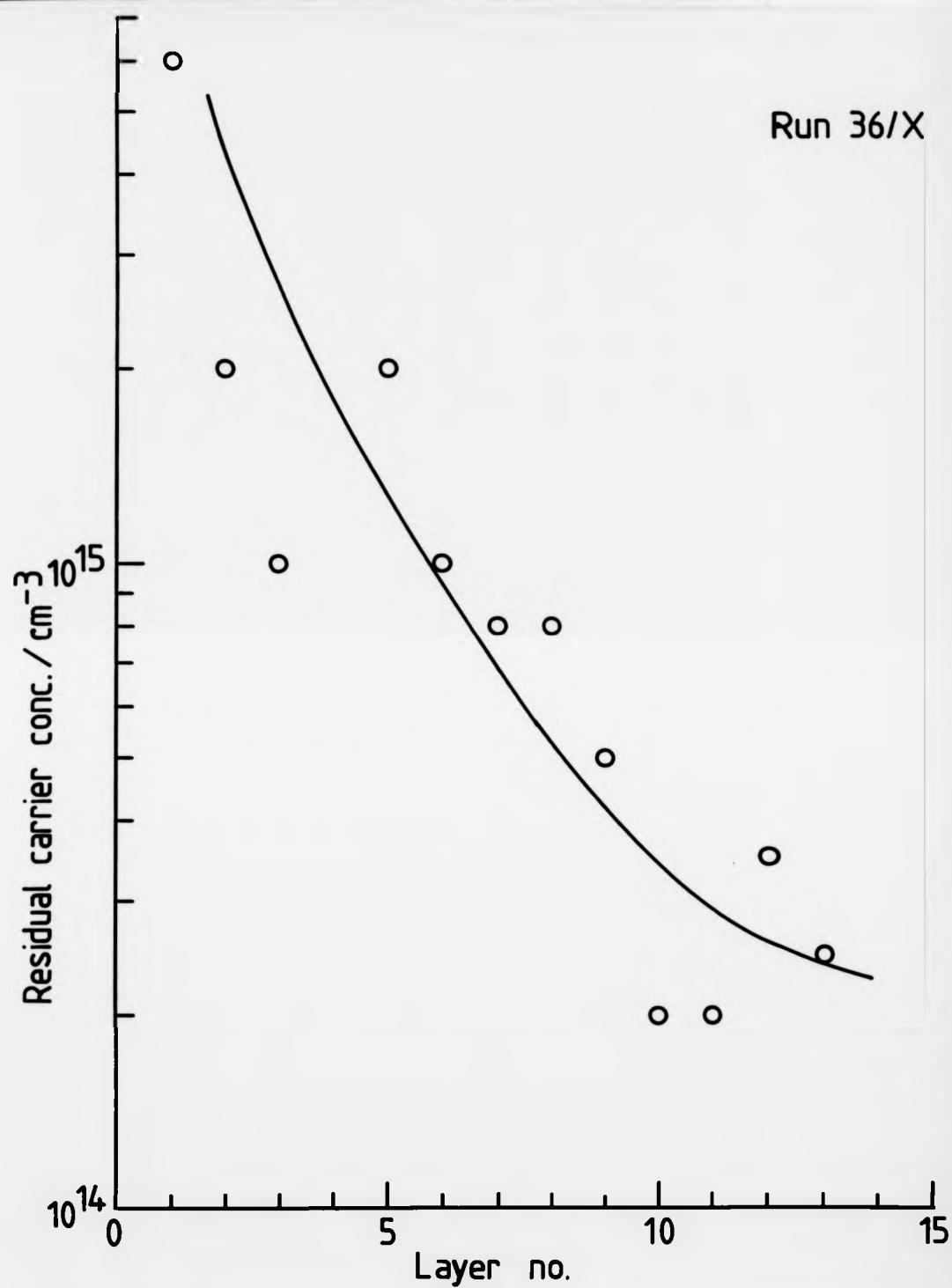


Fig. 4.10 Carrier concentration against epilayer number for an intermediate growth run, illustrating the decrease in carrier concentration with growth of material. Later runs showed a more rapid decrease to the base level of  $10^{14} \text{ cm}^{-3}$ .

level fell only rarely, the lowest we achieved being  $8 \times 10^{13} \text{ cm}^{-3}$ , grown after 30um deposition from bakeout.

It is interesting to note that the minimum background doping level decreased gradually with time (ignoring the initial increase just after each bakeout), as is illustrated in Fig. 4.11. When new the residual carrier concentration was  $.5 \times 10^{15} \text{ cm}^{-3}$  but fell to  $1 \times 10^{14} \text{ cm}^{-3}$  after about 18 months' use. This level remained constant, showing a minimum base level had been reached.

A recent chance discovery supported the theory that stainless steel was the source of phosphorous. During electron bombardment of a Ge source charge it was found that reflected electrons were impinging upon the stainless steel cooling tubes. While in this condition the background doping level dramatically increased to  $10^{18} \text{ cm}^{-3}$  n-type. When the offending pipes were shielded with Si the background went down to its original level of  $10^{14} \text{ cm}^{-3}$ .

#### 4.4.2 Comparison of memory effects of coevaporated dopants.

Memory doping effects are caused by previous intentional use of dopants in the system. The problem is greatest for those dopants which have relatively high vapour pressures, since this means that a warm system component could act as a considerable secondary source. Most of the common dopants have a low sticking coefficient on Si, (i.e. only a small

fraction was incorporated into the layer,) which meant that even if the dopant flux was collimated onto the substrate, most would be desorbed, allowing it to condense on cooler parts of the system to be re-evaporated later.

The highest vapour pressure dopant used in the MBE system was phosphorus <Kubiak et al, 1986>, with a vapour pressure of  $10^{-5}$ mbar at  $1000^{\circ}\text{C}$ . This showed substantial memory effects, increasing the background doping to  $1\times 10^{17}\text{cm}^{-3}$  after a growth run of twenty phosphorus doped epilayers (each about 2um thick). After one system bakeout (28hrs at  $2000^{\circ}\text{C}$ ), this level was reduced to  $6\times 10^{16}\text{cm}^{-3}$ , then to  $1\times 10^{16}\text{cm}^{-3}$  by the end of the run, and to  $2\times 10^{15}\text{cm}^{-3}$  after subsequent bakeout (all levels determined by Hall measurements).

Ga doping also caused a similar effect, turning the background p-type at a concentration of about  $1\times 10^{16}\text{cm}^{-3}$ . Bakeout had little effect on this level, which decreased slowly with time over several growth runs.

Sb, which was used continuously as the main n-type dopant, was found not to noticeably contribute to background doping level under normal circumstances. However, an experiment involving the shutting off of the water-cooling around the MBE system during growth showed a dramatic increase in the residual doping level as the temperature of the chamber walls rose (see eCV plot in Fig. 4.12a). Initially it was believed that this was due to enhanced phosphorus doping from the stainless steel, as is believed to occur during bakeout. However, SIMS analysis,

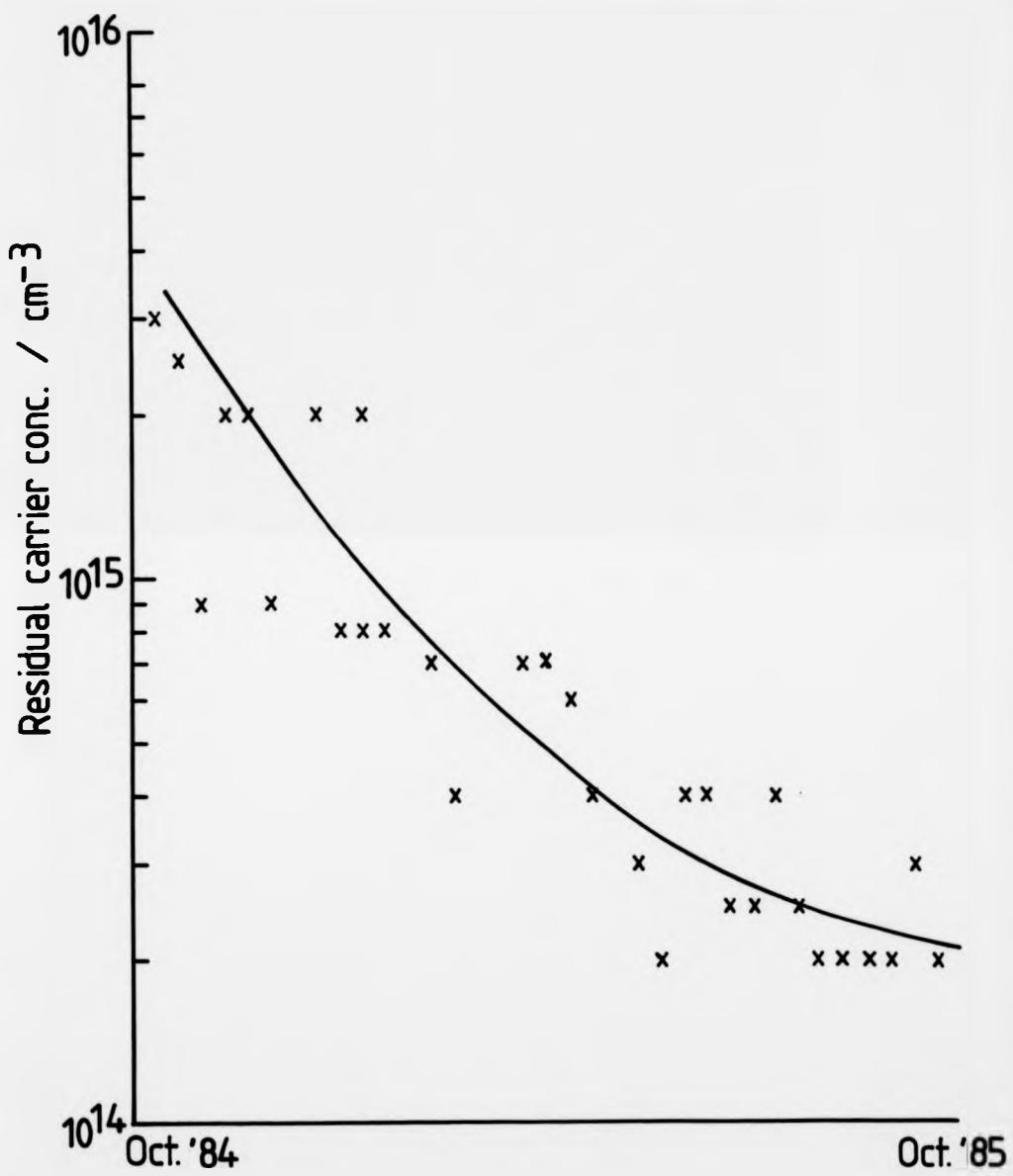


Fig. 4.11 Graph showing the decrease in minimum achievable doping level with time.

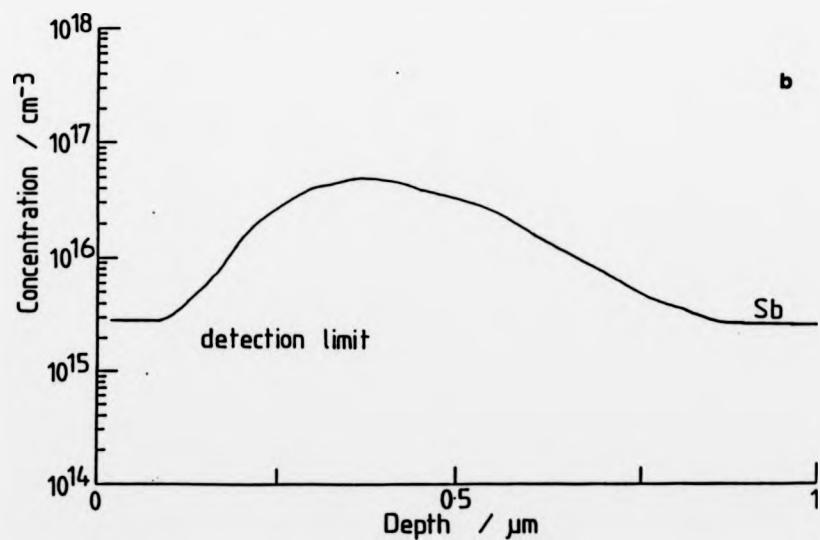
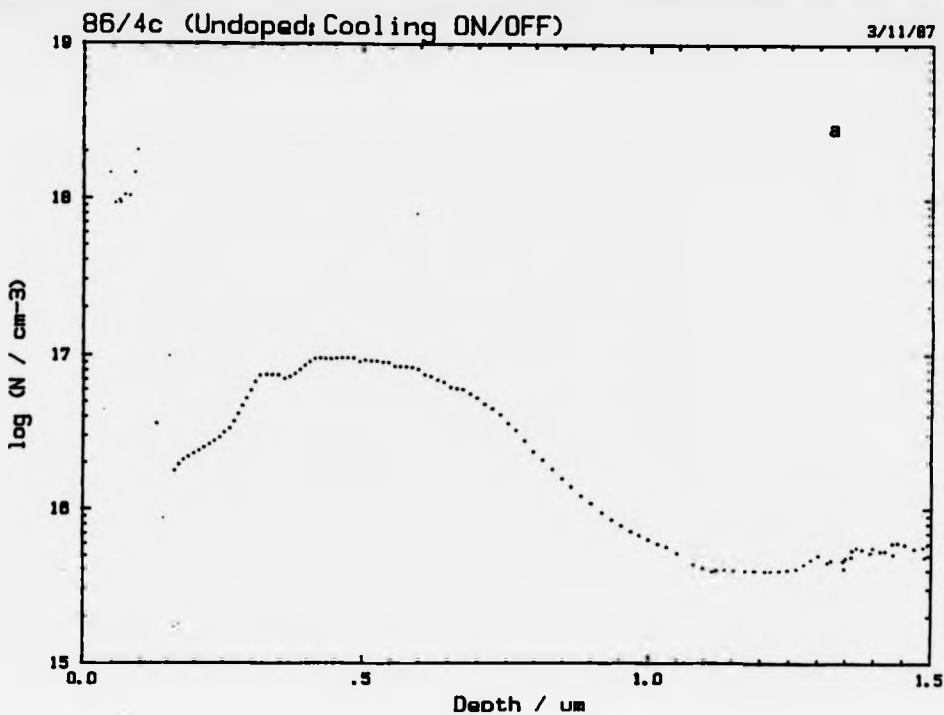


Fig. 4.12 a) eCV profile of epilayer growth during which the system cooling water was intentionally turned off. A marked increase in background doping is evident.

b) SIMS profile of the same epilayer, identifying the residual dopant as Sb.

even using high resolution mode, showed no sign of phosphorus contamination. Instead it was found that the increased carrier concentration was due to secondary Sb doping, as shown in the SIMS profile of Fig. 4.12b. This indicates that a considerable reservoir of Sb is present within the system, and that adequate cooling is essential to avoid such contamination. It is interesting to note that the change-over from cryopanelling to external watercooling had no noticeable effect on background doping. This suggests that the water-cooling is very effective, despite the presence of some "hotspots".

B has been used for several years in the system as an elemental coevaporation source. It did not contribute to background doping due to its low vapour pressure (which is so low that its initial evaporation as an intentional dopant is a problem). Recently, however, the background level became p-type, and was identified by SIMS to be due to B. Few parts of the system become hot enough (at least 1200°C) to cause B to sublime. Initially the Si source charge was thought to be contaminated, but this was not the case. Fig. 4.14 shows a SIMS profile of a camel diode structure which requires a p-type spike to be grown with n regions on either side. An unintentional B background is clearly visible at  $\sim 10^{16} \text{ cm}^{-3}$ . The n- region was achieved by Sb doping to just above the B level. (This illustrates the need for adequate characterisation of background doping, so that it can be overcome by a minimum of doping of the opposite type when

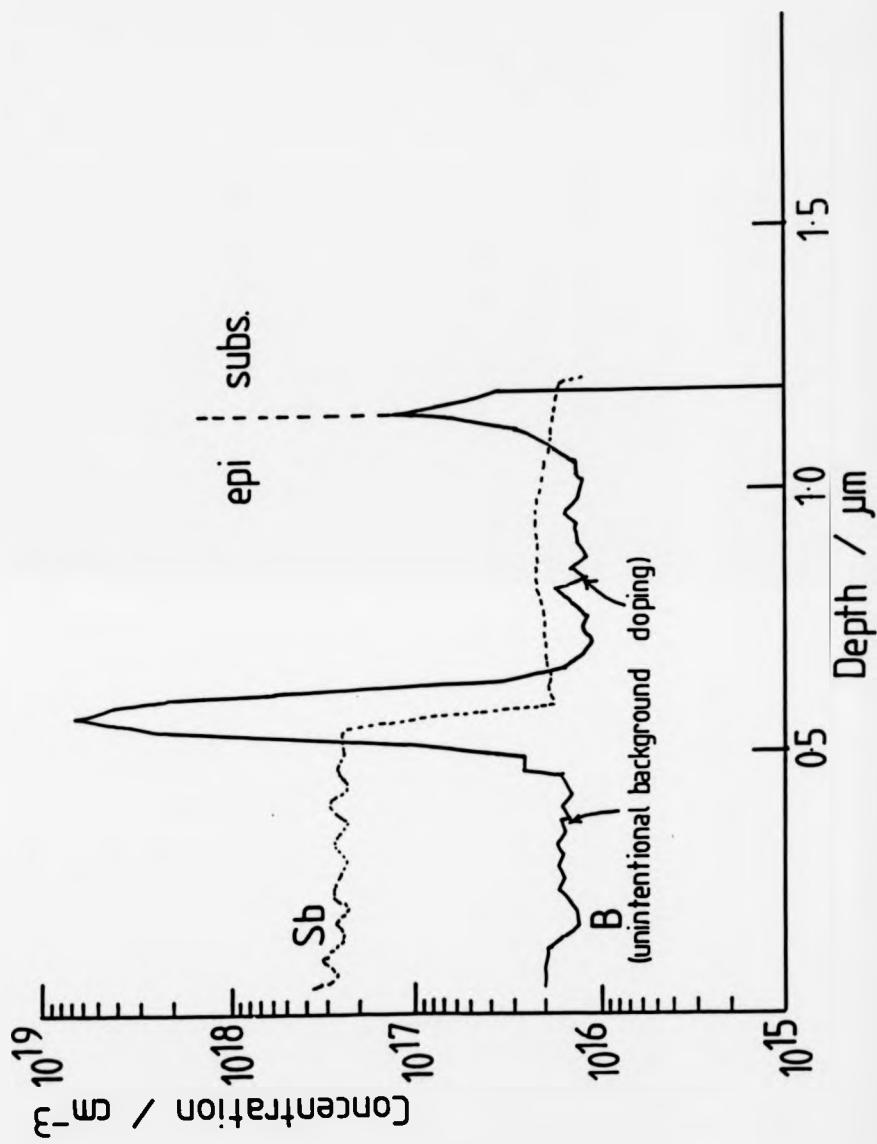


Fig. 4.14 SIMS profile of a camel diode structure, showing residual B doping. The use of Sb to overcome this level for the n- regions of this device is clearly illustrated.

needed for device purposes). We were unable to isolate the source of this background B doping.

#### 4.5 Summary.

The value of  $E_A$  [0.045 $\pm$ .0.001 eV] and results of PL showed quite conclusively that the normal n-type residual dopant in the system was phosphorus. This was endorsed by observation of the incorporation kinetics that correlate with this work on intentional phosphorus doping, which was found to show properties characteristic of P doping.

The level of residual doping has decreased with time from  $10^{16}$  to  $10^{14} \text{ cm}^{-3}$  as the system has matured. Bakeout has the effect of significantly increasing the level for the first few microns of growth, in agreement with the findings of Iyer <Iyer & Delage, 1988>, who suggests phosphorus diffusion along grain boundaries in stainless steel as the source.

A possible means of reducing this level would be to line the inside of the system with a cool shroud (preferably Si) to prevent line of sight to the substrate.

Memory effects of the various dopants used in Si-MBE have been observed, both phosphorus and gallium increasing the background. Sb was found not to contribute to carrier concentration, unless the system cooling was interrupted. B was used for several years with no effect on residual doping, but did for a time become main background dopant at  $\sim 10^{16} \text{ cm}^{-3}$ . The reason for this has yet to be ascertained.

These memory effects could be minimised by careful system changes. Dopant flux collimation onto the substrate and smaller source-substrate distances (currently about 30cm) would minimise the loading of the system, although not erradicating dopant atoms reflected from the hot Si surface. Decreasing the area of the substrate ring holders, which naturally reach high temperatures due to their close proximity to the substrate heater during growth and receive high dopant fluxes, would reduce their effect as a secondary source. All hot areas such as filaments, ion gauges and areas warmed by the substrate heater and Si source should be shielded from line of sight to the substrate. Future system design should take note of these points to achieve the lowest possible residual doping levels.

## Chapter 5. Temperature Dependence of Epilayer Properties.

### 5.1 Introduction.

The aim of this set of experiments was to provide a better insight into the role substrate temperature,  $T_s$ , plays in the crystalline, electrical and optical properties of MBE-grown Si. Epitaxial layers of good crystalline quality can be grown between 500 and 900°C, using suitable *in-situ* and *ex-situ* cleans. Within this range optimum growth temperatures have previously been chosen to alleviate problems due to doping, such as B diffusion at high  $T_s$  <McPhail et al, 1988> and Sb profile smearing that occurs at lower  $T_s$  <Rockett et al, 1985>. With the recent rise in interest in Si-SiGe heteroepitaxy there is a drive towards lowering of  $T_s$  to increase the critical thickness before lattice relaxation occurs causing misfit dislocations, and so the effects of low  $T_s$  on epilayers need to be reviewed.

Previous work on substrate temperature effects <Tabe et al, 1981, Sugiura & Yamaguchi, 1980> have concentrated on the temperature during thermal clean-up. Little work has been carried out on the influence of  $T_s$  on layer properties such as electrically active deep level traps and photoluminescence. These are standard methods of analysing material quality in bulk silicon, which can give an excellent indication of the type of impurities present.

Recent studies <Houghton et al, 1987> have shown deep level states in Si-MBE layers to be  $<10^{14}\text{cm}^{-3}$  total electron traps, but this is still not as low as the concentration achievable by state-of-the-art CVD growth ( $<10^{12}\text{ traps cm}^{-3}$ ) <Hamilton et al, 1988>. Photoluminescence efficiency of layers has also been found to be relatively low, some workers being unable to obtain luminescence in undoped layers, indicating strong non-radiative recombination <Lightowlers et al, 1989>.

### 5.2 Experimental.

For the major DLTS and PL work in this series of experiments, thick (7-10um), nominally undoped ( $<10^{15}\text{cm}^{-3}$  n-type) epilayers were grown at a range of substrate temperatures onto n<sup>++</sup> substrates. These substrates were ideal for DLTS work, and also gave broad PL peaks which made them easily distinguishable from epilayer luminescence. The high doping level in the substrate, however, also caused absorption of excitons from the epilayer, a distinct disadvantage. Prior to epitaxy all wafers were given a standard 2.5% HF dip clean, followed by in-situ outgassing at 450°C, growth of a 10A polysilicon cap and then 5 minutes thermal oxide desorption at 700°C (see chapter 3).

Analysis of the resulting epilayers involved PL, carried out by King's College, to assess optical quality, DLTS, carried out by UMIST, (using a Polaron DL4500) for electrically active defect centres, and SIMS, at both Warwick and Loughborough Consultants, for chemical analysis of C, O and transition metals. Defect etching was routinely carried out on all layers to ascertain crystalline quality.

### 5.3 Results.

#### 5.3.1 Ambient gas interactions in UHV.

One of the main factors affected by substrate temperature is rate of adsorption of residual gases onto the clean, and thus highly reactive, Si surface. Fig. 5.1A shows a typical base residual gas analysis [RGA] from the MBE system after bakeout and source cell and heater outgassing. The major peaks are at masses 1, 2, 4 and 28, indicating the presence of H, He (from the use of a cryopump) and CO (as opposed to N<sub>2</sub> which would also cause a significant 14 [N] peak). The peak at mass 19 is an artefact of the mass spectrometer electron multiplier, caused by electron-induced desorption. Fig. 5.1B shows an RGA spectrum taken during growth, which indicates that the major proportion of the pressure rise is due to hydrogen

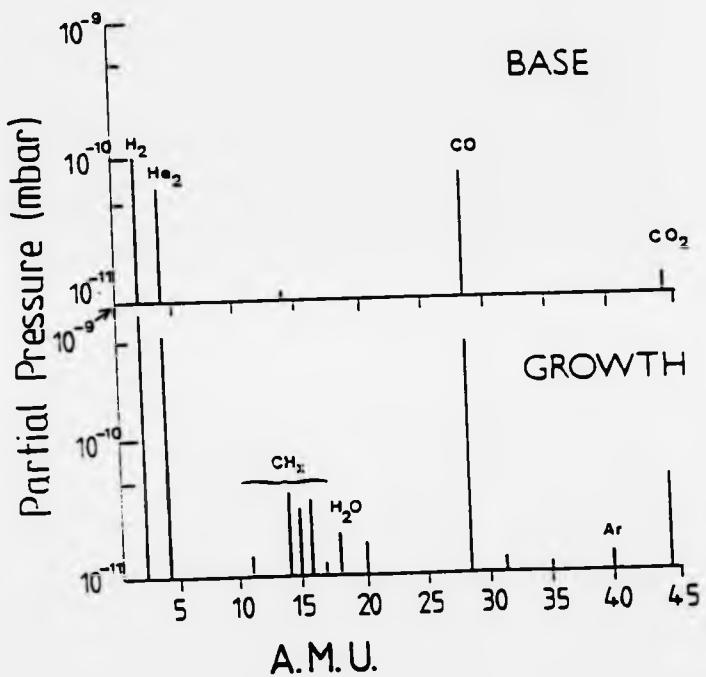


Fig. 5.1a RGA of growth chamber at base pressure after  
bakeout.

Fig. 5.1b RGA of growth chamber during deposition.

which has been found <Kasper & Kibbel, 1983> not to be detrimental to the growth process.

However, carbon species are very undesirable in the ambient due to the connection between carbon and dislocation nucleation <Kolbesen & Muhlbauer, 1982>. Si heated to between 800 and 1000°C in UHV has been shown to form SiC due to surfacial carbon, forming a possible defect site <McFee et al, 1983>. Also, more generally, C can cause a reduction in surface mobility of Si ad-atoms. An experiment was carried out to determine carbon and oxygen adsorption variation with  $T_g$  the results of which are shown in Fig. 5.2. Six minute interrupts in growth were performed at decreasing  $T_g$  within a single epilayer. Carbon and oxygen incorporation were then measured by SIMS and an increase in adsorption with increasing  $T_g$  is clearly indicated. The background levels for both C and O indicate SIMS detection limits. Further experiments were then carried out to determine C levels through the bulk of epilayers grown over a range of temperatures. These also show a decrease of an order of magnitude in C levels with decrease in temperature (see Fig. 5.3). This increase in C incorporation with  $T_g$  does not agree with the work of Kugimiya <Kugimiya et al, 1985> who found increased C uptake at lower temperature. Their data showed no C build-up occurred over a 2 minute interrupt at  $T_g > 750^\circ\text{C}$ , with an extremely small increase above background at 600°C. It is surprising to see no build up of C during a high temperature interrupt since MBE-grown Si is known to contain high C

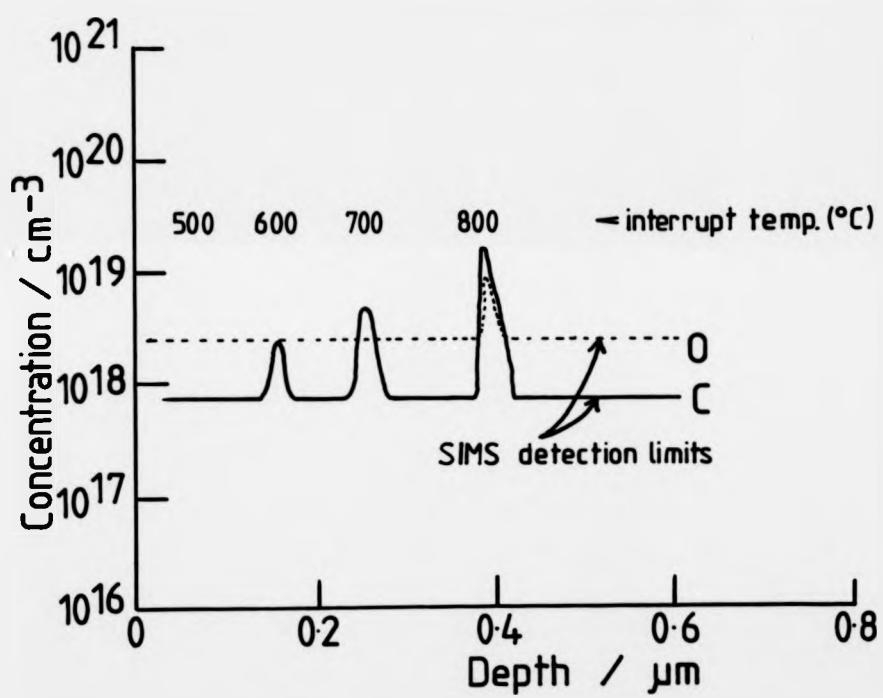


Fig. 5.2 SIMS profile of epilayer containing 4 growth interrupts at various  $T_s$ , illustrating the increased adsorption of C and O with temperature. Note that the base level denotes SIMS instrumental background. (SIMS carried out for the author Loughborough Consultants.)

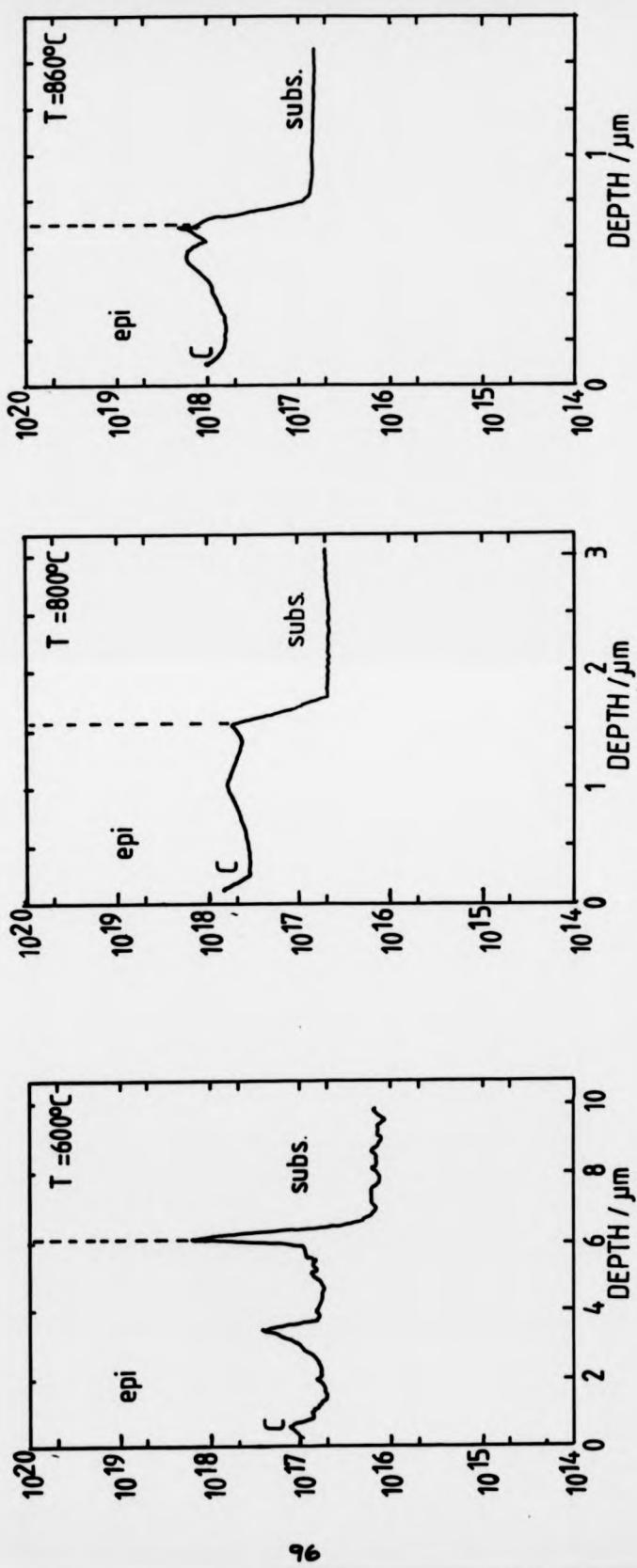


Fig. 5.3 SIMS profile showing increased incorporation of C into the bulk of the epilayer with increasing temperature.  
(SIMS carried out for the author by British Telecom,  
Hartleesham.)

levels due to incorporation during growth. It has been found <Henderson et al, 1971> that a clean Si surface accumulates C when heated in UHV. The quantitative levels found by Kugimiya are not known since only raw SIMS data has been published.

It is possible that the increased C uptake in layers grown by the author was due to increased outgassing. This does not, however, agree with mass spectrometry results taken at various growth temperatures, which showed no increase in carbon compounds in the ambient.

The most prolific carbon compound in the ambient was CO, but the fact that the C and O peaks in the SIMS profile do not scale with each other, and are not interrelated over the interrupt temperature range indicates that carbon was not incorporated as molecular CO. It has been noted previously that CO is volatile at the temperatures used for growth, so the residence time on the surface would be short due to rapid desorption <Yokota et al, 1986>. The bond strength of CO is relatively high [8.2eV], much greater than the thermal energy available at the surface, [ $kT=0.08\text{eV}$  at 1000K]. So, despite the fact that catalytic surface action might aid the reaction, decomposition seems to have a low probability, since the author has noted no correlation between the height of the CO peak in the RGA and dislocation density. It is therefore unlikely that CO caused the high carbon levels within the layers.

It has been found previously that hydrocarbons have a detrimental effect on layer growth <Kasper & Kibbel, 1983>.

These are also volatile species, but with a lower bond strength [the HC bond strength is 4.3eV]. Temperatures above 400°C have been found to greatly reduce hydrocarbon adsorption <Grundner & Jacob, 1986>. At temperatures above 500°C dehydrogenation occurs and SiC is left on the surface. This could not be removed unless the wafers were heated to above 1050°C <Yokota et al, 1986>, which was not possible using the heater in the V80 MBE system [the maximum achievable  $T_g$  was ~900°C], and would be unsuitable for the MBE technique which relies on low processing temperatures for its advantages over other methods of epitaxy.

It seems that the temperature range used for growth was itself a major factor in causing carbon contamination, since it was high enough to bring about dehydrogenation of CH<sub>x</sub> groups, but too low to cause desorption of SiC. The fact that carbon incorporation rose with substrate temperature implies that the rate of dehydrogenation increased faster than the rate of hydrocarbon desorption.

### 5.3.2 Dislocation levels.

The effect of  $T_g$  on extended defects was observed, but negligible influence was noted on particle induced defects or s-pits, as illustrated in Fig. 5.4. Dislocation densities, however, were found to have a strong temperature dependence, showing a minimum concentration between 500 and 600°C (see Fig. 5.5). Below 500°C it was noted that the

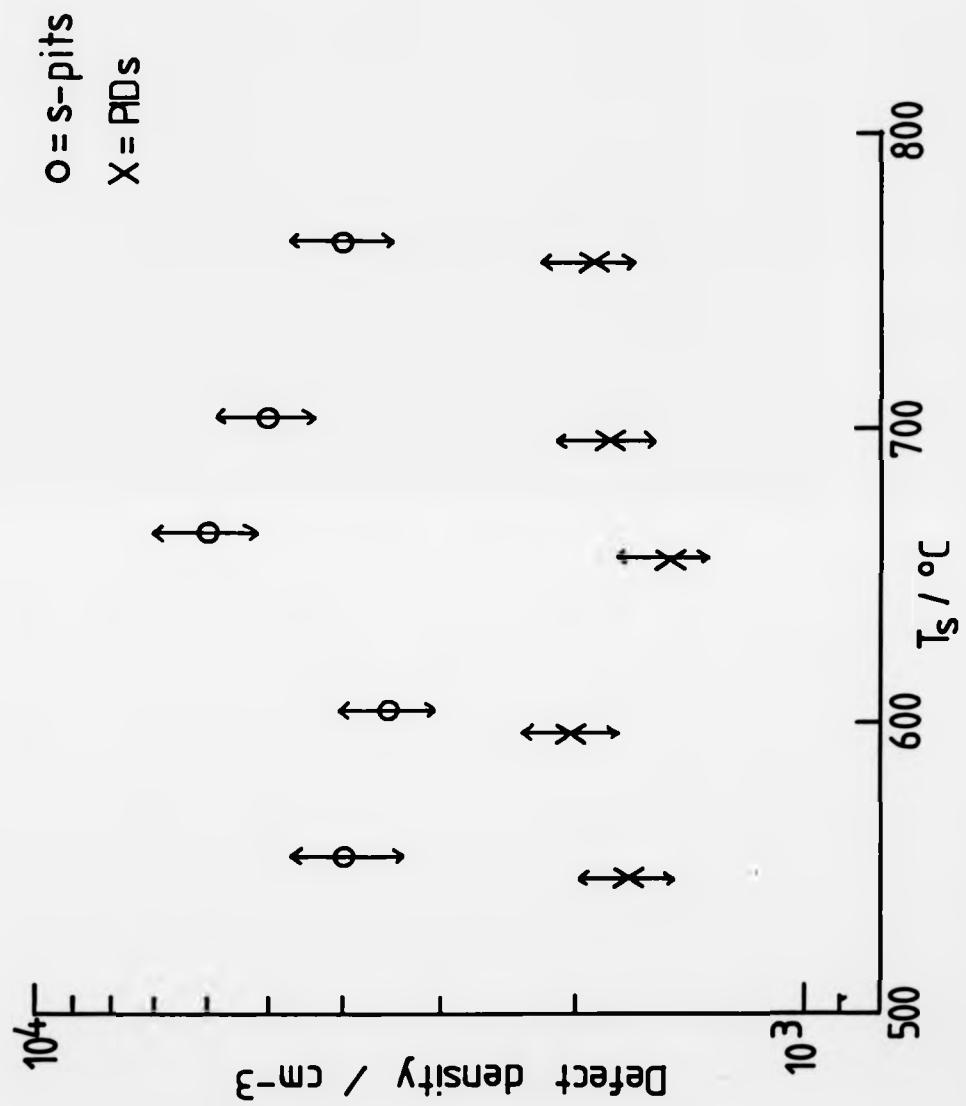


Fig. 5.4 Graph illustrating the independence of s-pit and PID densities from growth temperature.

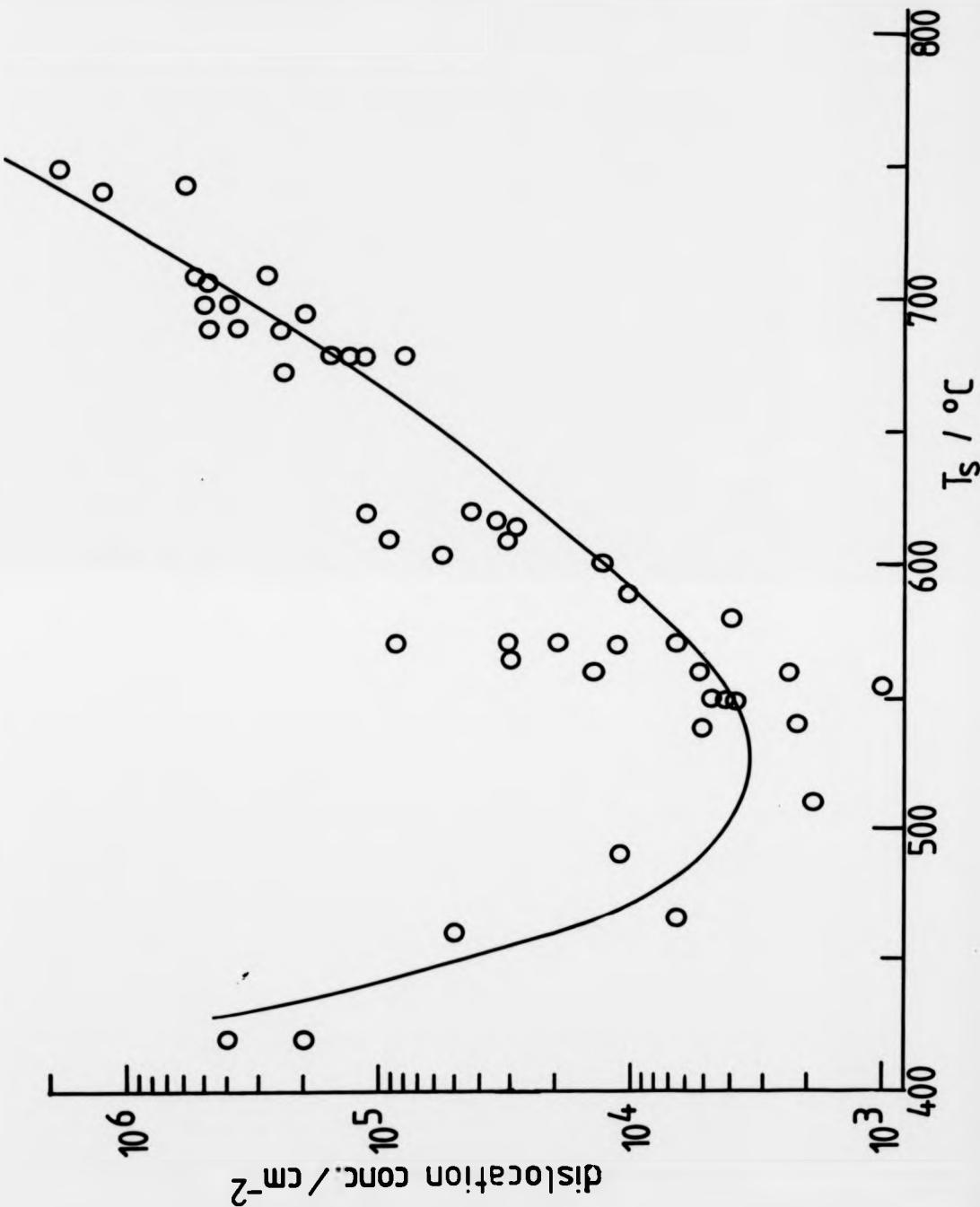


Fig. 5.5 Graph showing the marked dependence of dislocation density on substrate temperature. Note the minimum at around  $550^{\circ}\text{C}$ . All layers were grown under similar conditions, with HF dip and poly-Si cap at  $400^{\circ}\text{C}$  followed by heating to  $700^{\circ}\text{C}$  for 7 minutes. Growth was initiated at  $700^{\circ}\text{C}$ , left at this for ~3 seconds then the heater was adjusted to give the current required for the selected growth temperature. The layers were grown at  $5\text{A/s}$ , to thicknesses between 1.5 and 6.0  $\mu\text{m}$ .

material appeared highly defective ( $>10^7$  dislocations  $\text{cm}^{-3}$ ); at  $T_s < 400^\circ\text{C}$  crystallinity rapidly became extremely poor, the dislocation etch pits becoming indistinguishable from one another. It is, however, noted that other authors claim to have achieved epitaxial growth at temperatures as low as  $250^\circ\text{C}$  *<Jorke, 1988>*, by use of extremely low growth rates ( $<1\text{A/s}$ ). The change in crystalline quality was attributed by Jorke to a change in growth process that has been found to occur at lower growth temperatures. At  $T_g > 550^\circ\text{C}$  two dimensional growth occurs via step propagation across the growing surface, by the Frank-van der Merwe growth mode. This is because the energy of the Si atoms on the surface is sufficiently high for migration to the growth step to occur. Below this temperature, three dimensional island growth (Volmer-Weber mode) begins to occur due to low Si surface mobility, and by  $400^\circ\text{C}$  becomes dominant, yielding material of very poor crystallinity.

Above approximately  $650^\circ\text{C}$  the increase in dislocation density seems attributable to increased carbon at or near the interface. It was noted by TEM that a dark band due to interfacial strain was observable at the interfaces of these more defective layers. This dark band was probably associated with carbon contamination due to residual gas interaction, and the strain induced nucleated dislocations. This strain line was not detectable in epilayers with low dislocation levels ( $<10^4 \text{cm}^{-3}$ ), implying a correlation between carbon and dislocations.

The standard method of deposition was such that approximately 3 seconds after opening the substrate shutter, the heater current was adjusted to that required for growth, cooling governed by the rate of radiant heat loss by the wafer. With the substrate heater set to a high growth temperature, the wafer would be at a high temperature for a longer period during the initial stages of growth, thus allowing more carbon to be incorporated. The actual interfacial carbon levels, as measured by SIMS, did not seem to be dramatically affected by growth temperature, as shown in Fig. 5.3. It seems, however, that only the temperature during the initial stages of growth is important to the dislocation nucleation process, since no correlation between layer thickness and dislocation density was observed [see Fig. 3.1] as would have been the case if nucleation occurred continuously during growth due to C contamination. It may be the case that the reduced surface mobility of Si atoms caused by the presence of C adatoms <Kasper, 1982> is critical to the growth process during the first few hundred angstroms, while the rate of growth step formation reaches equilibrium, and while the Si surface becomes smooth after thermal treatment. This smoothing process has been demonstrated by laser light scattering <Robbins et al, 1987>.

### 5.3.3 Deep Level Analysis.

Samples analysed by DLTS showed a marked growth temperature dependence of all electrically active traps. Four deep levels were found, as shown in Fig. 5.6, and their

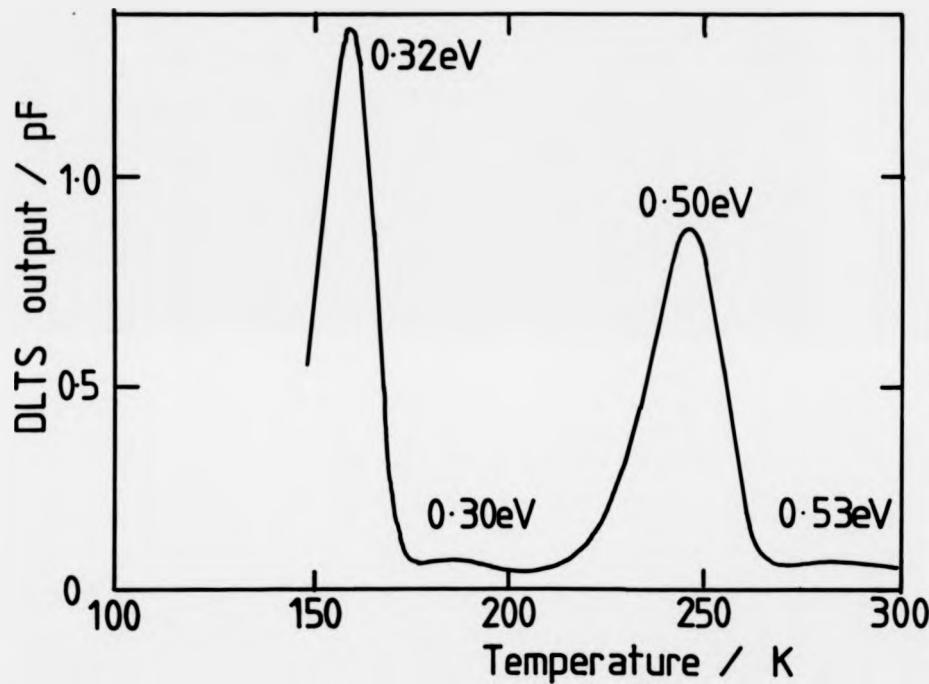


Fig. 5.6 DLTS found four major peaks in our Si-MBE material. The layer with the highest concentrations is shown here (grown at  $T_s=490^\circ\text{C}$ ) in this temperature scan. (DLTS carried out by UMIST.)

respective energies determined by Arrhenius plots [Fig. 5.7]. They were then identified by comparison with previously published data. This suggested that two of the traps, at energies 0.53eV and 0.30eV, were due to two different charge states of the same defect. Work by Sah et al. (1975) has established that this defect is a Si vacancy or vacancy related complex.

The other two traps seen, at 0.32 and 0.50eV, also showed strong temperature dependence as illustrated in Fig. 5.8. The mid-bandgap state at 0.50eV may be due to metallic contamination, as many metals have energy levels around this value <Sze, 1981>. By changing the width of the DLTS filling pulse the capture cross section of this trap was determined as  $4 \times 10^{-14} \text{ cm}^2$ . The emission data were very similar to those of Ta in Si. Ta has previously been detected by SIMS in B doped layers (see chapter 6) and by neutron activation analysis (NAA) in undoped layers, and is therefore a likely candidate for a mid-gap trap. Precise identification was not possible, however, due to the similarity of the emission characteristics of other metallic contaminants. Recent work using a graphite heater instead of a Ta one has shown that this particular trap was no longer present, indicating that the impurity causing the trap was Ta, and the source of this was the substrate heater.

A similar trap to 0.32eV has been seen at 0.29eV by both Omling et al. (1985) and Weber & Alexander (1983), who designated it as being related to dislocations or, more likely, decoration thereof. As has been discussed

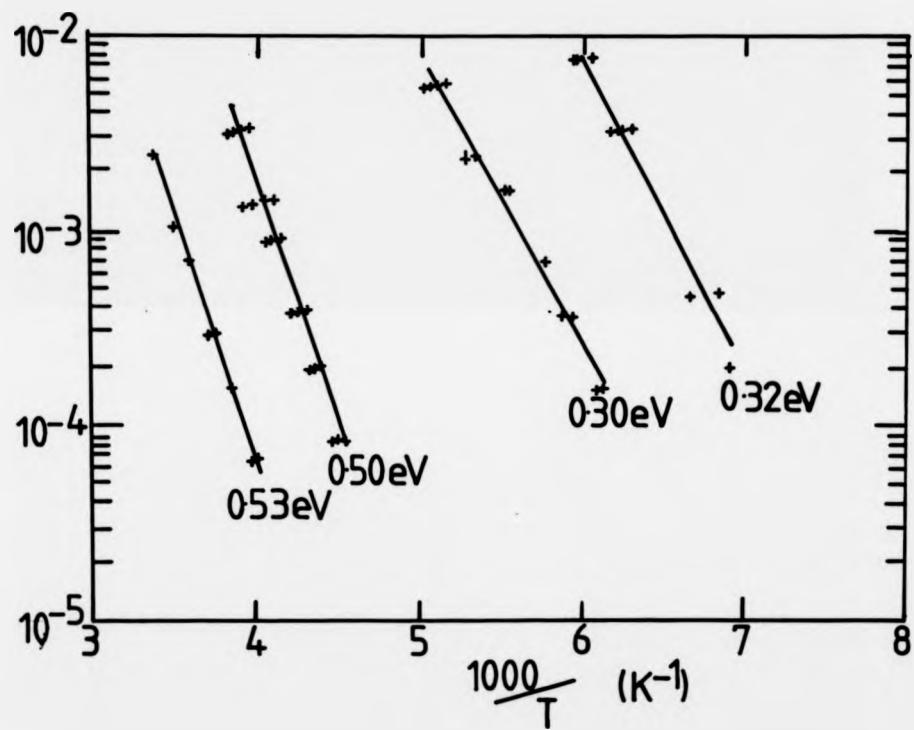


Fig. 5.7 To determine the activation energies of the traps found by DLTS the above Arrhenius plots were made. (DLTS carried out by UMIST.)

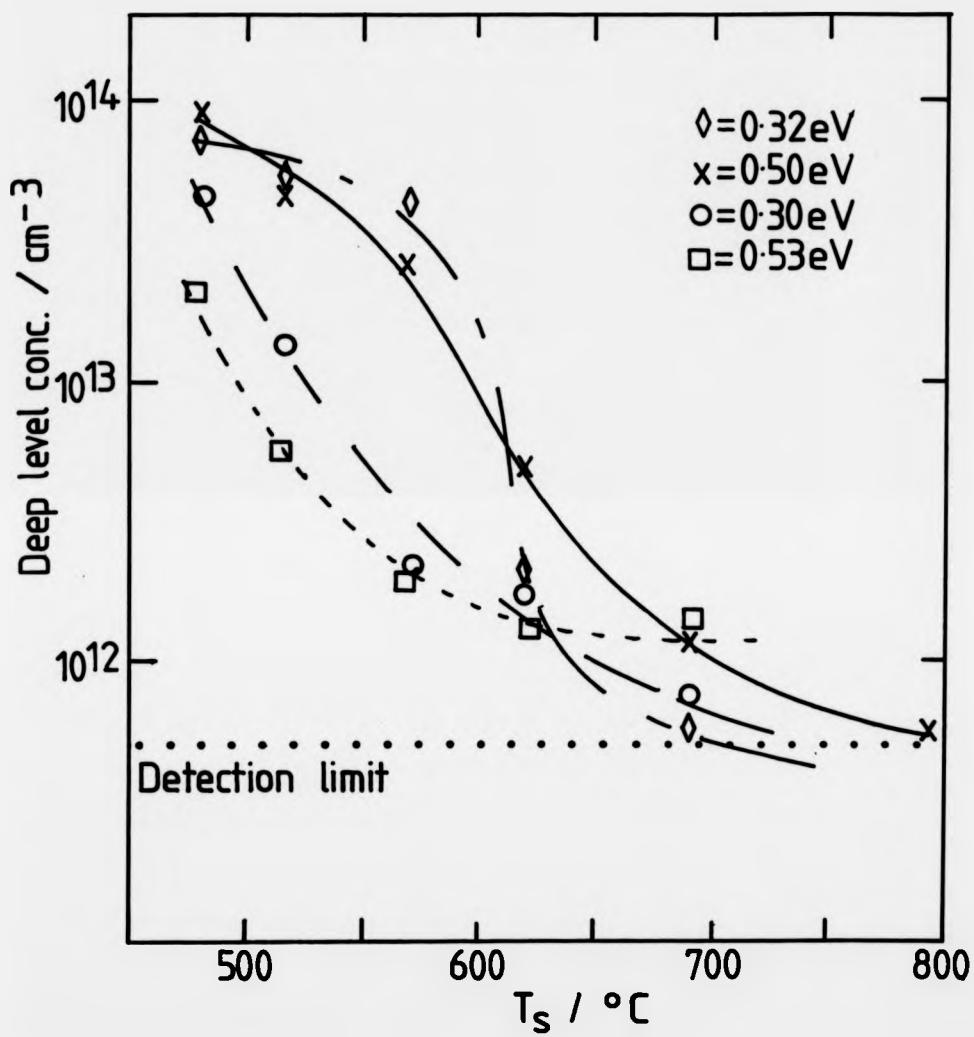


Fig. 5.8 This plot shows the substrate temperature dependence of all four major traps seen by DLTS. Note the dramatic transition of E(0.32) and E(0.50) at ~600°C, yielding high electrical quality material at  $T_s > 700^\circ\text{C}$ .  
 (after Sidebotham et al, 1988)

previously, the actual dislocation density increased with  $T_g$  above 450°C, the inverse of the dependence of trap density on  $T_g$ , indicating that the trap concentration was not directly influenced by dislocation density. If the cause of the trap is dislocation decoration, then either incorporation of the impurities was  $T_g$  dependent, or the higher temperatures allowed the formation of inactive impurity clusters.

The latter is more likely to be the case, and the fall in deep level trap concentration at substrate temperatures above 600°C may be linked to the increase in dislocation levels, as shown in Fig. 5.5. It has already been postulated that dislocations may act as gettering sites (see section 3.3.3). Their increase in density would encourage precipitation of electrically active metal impurities, especially fast diffusers like Cu and Ta, and both the traps at 0.50 and 0.32eV are possibly due to transition metals. The higher temperatures would also increase the diffusion rate, as well as the number of gettering sites. The work of Sah and Wang <1975> suggested that the vacancy related traps [0.53 and 0.30eV] could not be fully removed by gettering using phosphosilicate glass in bulk material. However, dislocations have been shown to getter vacancies <Queisser, 1983>, so the increase in dislocation density could have an effect on them too.

It is also possible that these vacancy-related traps are linked to the growth mechanism in which Si atoms have a lower surface mobility at low temperatures promoting conditions in which vacancy formation in the lattice can occur. Further evidence for this was provided by

photoluminescence spectra of epilayers grown at low  $T_g$ , which showed a continuum of overlapping peaks at long wavelengths, thought to be connected with point defects, as will be discussed in the following section.

#### 5.3.4 Photoluminescence.

PL analysis of bulk Si is now a well researched and useful tool for studying material quality. Analysis of epitaxial material, however, presents several problems <Sandhu et al, 1985>. Luminescence efficiency is governed not only by surface recombination as in bulk material, but also by interfacial and substrate properties. The interface recombination velocity and substrate carrier lifetime both have effects on the intensity of luminescence from the substrate. If the lifetime in the substrate is long compared to that in the epilayer, a build-up will occur on the substrate side of the interface, thus increasing substrate luminescence. This effect is enhanced if the epilayer is thin since it is more likely that optical penetration through to the substrate will occur. However, careful measurement and analysis of data from epitaxial layers allows substrate and epilayer luminescence to be distinguished, and useful materials information to be gained.

The main features appearing in PL spectra of nominally undoped MBE-grown material are the A-line and dislocation related peaks called D lines. The A-line is caused by bound

exciton decay of an iso-electronic centre that has been related to a nitrogen complex <Alt & Tapfer, 1985>. D lines 1 to 4 are all seen at various intensities in MBE Si. They have been attributed to radiative transitions between shallow levels ( $E_i=4$  to  $7\text{meV}$ ) and deep level states within the Si bandgap at levels given by  $E_g-E_i-hf$ , where  $E_g$  is the Si bandgap,  $E_i$  is the ionisation energy of the impurity, and  $hf$  is the photon energy. It has been found that these levels are not related to impurities or point defects, nor to dangling bonds on the dislocations <Suezawa, 1983>, although this contradicts the findings of the work on intentional metal diffusion described previously (see section 3.3.3). D1 and D2 have been assigned to geometric kinks on dislocations. The D lines can be considered as pairs D1/2 and D3/4, since the origin of each line in the pair is similar. D1 and D2 are caused by bound-to-bound transitions, whereas D3 and D4 originate from a free-to-bound transition <Drozdov et al, 1977>. D3 and D4 have been found to give a better indication of dislocation levels than D1 and D2, due to the latter pair's interdependence, the D1 dominating the D2 peak at high dislocation levels ( $>10^7\text{cm}^{-2}$ ), perhaps even suppressing it <Sauer et al, 1985>.

Both the A and D lines are visible at all growth temperatures, but are clearly temperature dependent. Fig. 5.9 <Hamilton et al, 1988> shows the relative intensities of the A-line in

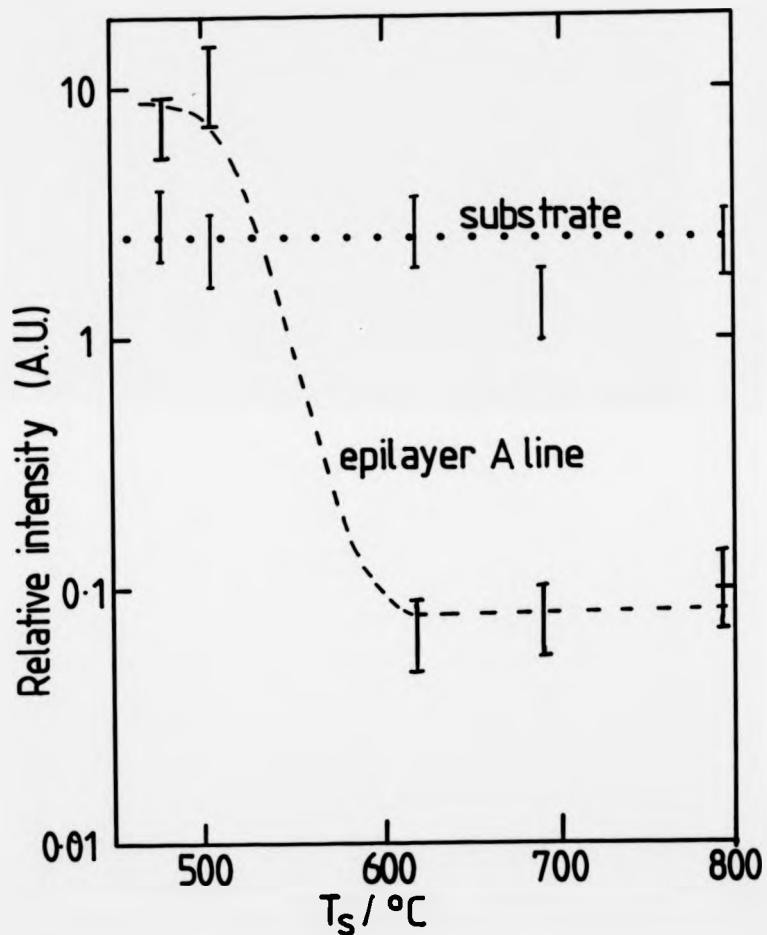


Fig. 5.9 Comparison of the relative intensities of the A-line in layers grown at various  $T_s$  with respect to substrate luminescence. <After Hamilton et al., 1988>

epilayers compared to the total substrate luminescence. The intensities of the D lines, due to lattice defects, is less easy to treat quantitatively due to their dependence on impurity concentrations as well as defect density and substrate temperature (see Chapter 4).

For low  $T_s$  a continuum of peaks was observed at high wavelengths (see Fig. 5.10), probably deriving from the high concentration of point defects , i.e. vacancies and interstitials, produced at this temperature. (Its apparent cut-off below 6000 wavenumbers is due to loss of sensitivity in the germanium detector.) These could be due to the lack of surface mobility of impinging Si atoms, which have insufficient energy to attain lattice sites. This agrees with the DLTS findings of a vacancy related trap, the concentration of which increases dramatically at substrate temperatures below  $-550^{\circ}\text{C}$ . It has been deduced from reflected high energy electron diffraction oscillation studies that two dimensional layer by layer growth ceases below  $600^{\circ}\text{C}$  <Gossman & Feldman, 1985, Aarts et al, 1986>. This supports the theory that a change in growth mechanism occurs at this point. It has been shown by RHEED and reflection electron microscopy [REM] that at  $450^{\circ}\text{C}$  layer by layer growth no longer occurred, with atoms arriving and incorporating independently. By  $750^{\circ}\text{C}$  layers grow solely by atomic step migration. It may be this change in growth mode that prevents the formation of point defects at higher  $T_s$ .

It has been noted that shallow impurity luminescence is greater at higher substrate temperatures. Dislocation

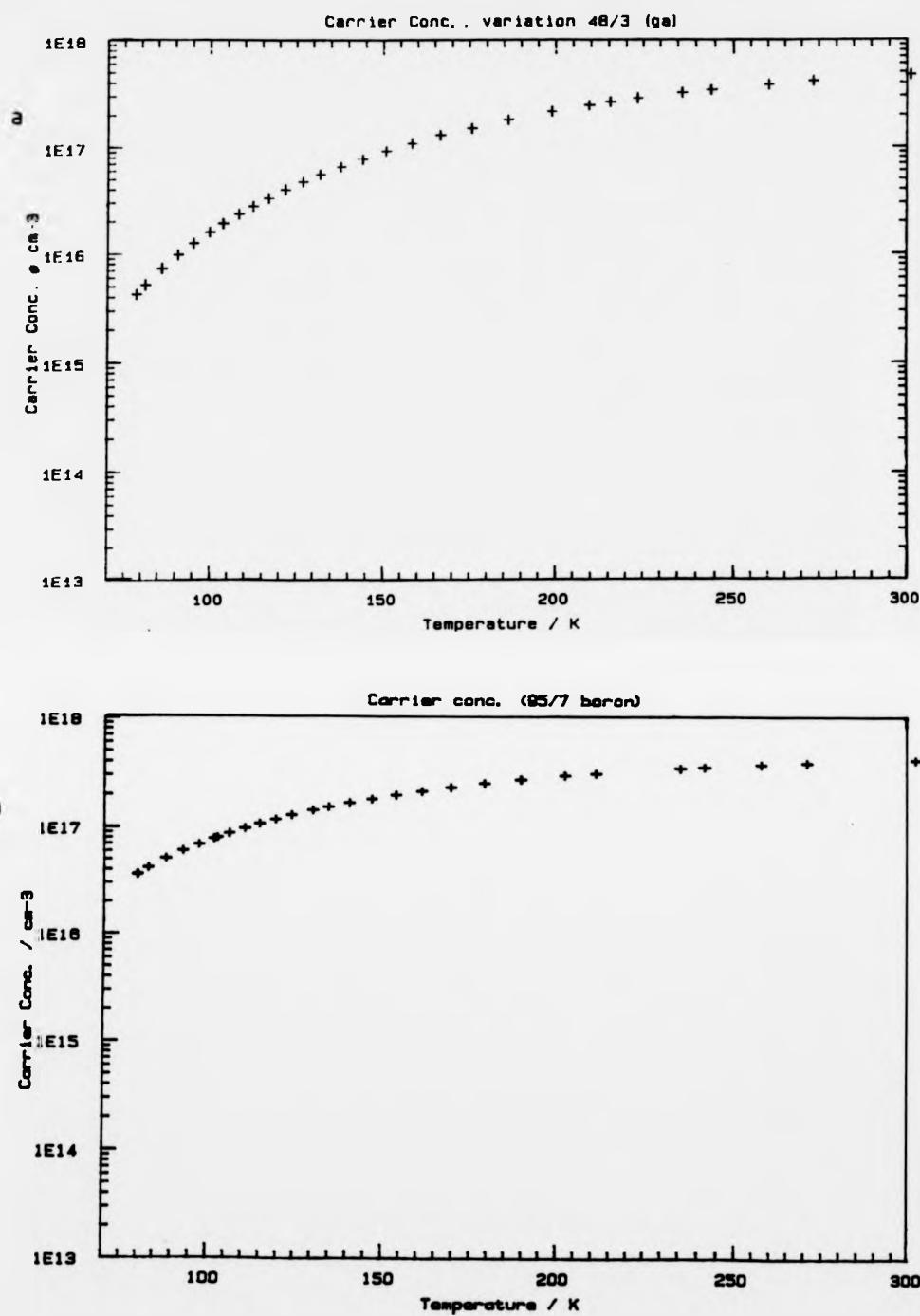


Fig. 6. 9 Carrier concentration vs temperature curve from Hall measurements:- a) for Ga, illustrating the relatively high temperature carrier freeze out that occurs due to its high activation energy in Si, b) a boron doped layer for comparison with a.

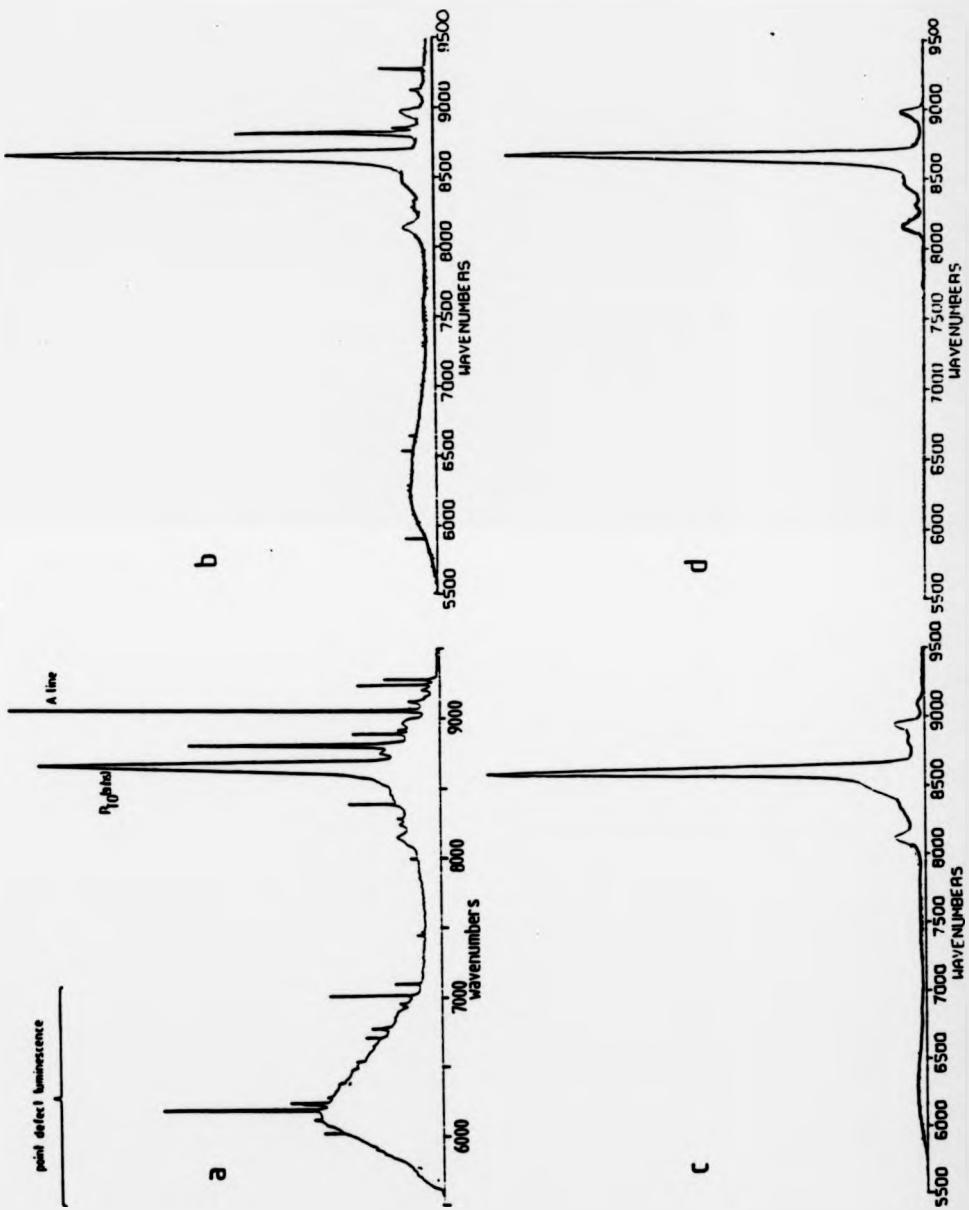


Fig. 5.10 Variation of luminescence with temperature.  
 a)  $T_g = 480^\circ\text{C}$ , b)  $T_g = 520^\circ\text{C}$ , c)  $T_g = 600^\circ\text{C}$ , d)  $T_g = 690^\circ\text{C}$ .  
 Strong point defect luminescence is evident at low substrate temperature.

density has been found to increase with temperature above  $600^{\circ}\text{C}$ , and it is likely that the two effects are related. In the previous section the possibility of dislocations gettering electron traps was discussed. The PL process is governed to a large extent by the presence of non-radiative recombination centres, and if these were being effectively gettered, then a larger proportion of excitons would be available to undergo recombination via a radiative path. This would increase the strength of the signal from shallow impurities. To test this hypothesis, two layers grown at the same temperature ( $690^{\circ}\text{C}$ ), but with different dislocation levels were analysed. The results are shown in figure 5.11. The layer with the greater number of dislocations ( $10^6\text{cm}^{-3}$ ) showed luminescence from the shallow impurities Al, B and P, whilst the layer with the lower dislocation density ( $10^4\text{cm}^{-3}$ ) did not. This gives support to the theory that gettering by dislocations of non-radiative centres occurs allowing more efficient luminescence, and is in agreement with the suggestion in the previous section that increased dislocation levels getter electrically active defect centres.

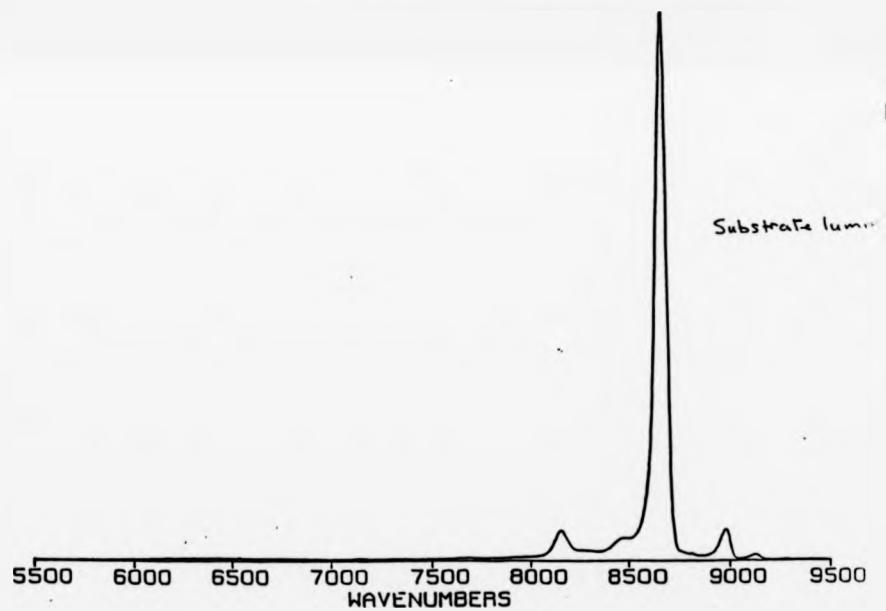
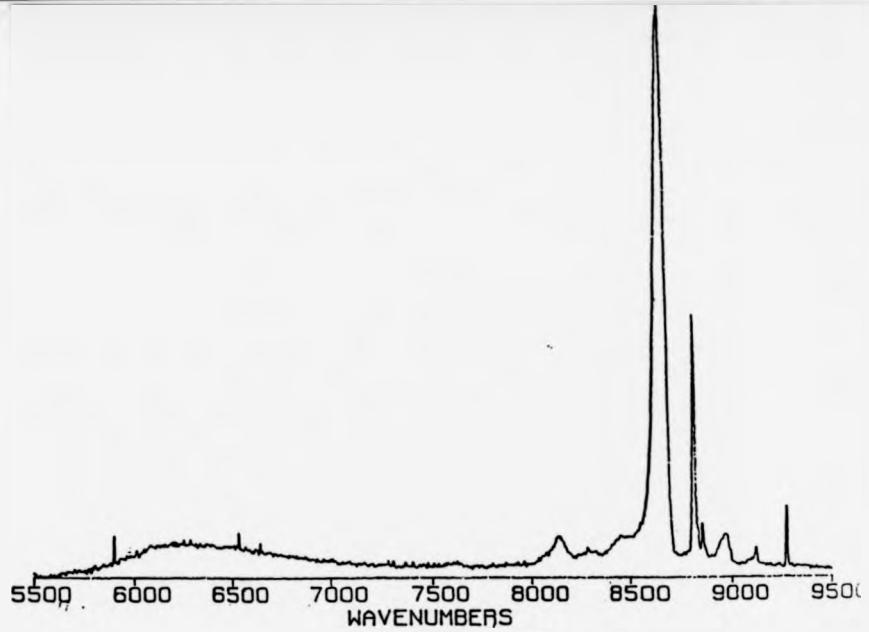


Fig. 5.11 Photoluminescence spectra from two epilayers both grown at 690°C. a) is of a layer with high dislocation density ( $>10^6\text{cm}^{-2}$ ) showing clear epilayer luminescence. b) is of a low dislocation density ( $<10^4\text{cm}^{-2}$ ) with poor epilayer luminescence.

#### 5.4 Summary.

The defects found by DLTS and PL show a marked temperature dependence. The concentrations of all four deep level traps fell from  $10^{14} \text{ cm}^{-3}$  for  $T_g=500^\circ\text{C}$  to  $10^{12} \text{ cm}^{-3}$  at  $T_g>700^\circ\text{C}$ , the latter being comparable to CVD material. The higher level would suggest low minority carrier lifetime and poor device performance <Ravi, 1981>. PL analysis shows the presence of point defects below  $550^\circ\text{C}$ , believed to be attributable to a change in growth mechanism from two dimensional to three dimensional growth. The D1 to D4 lines were found to vary with temperature, but since several factors affected their magnitude (defect density, impurity concentration, position on wafer), a simple temperature dependence was not easy to determine.

The increase in shallow impurity luminescence and the decrease in electrical trap concentration at higher  $T_g$  can both be explained by the associated increase in dislocation densities, with the dislocations acting as gettering sites for non-radiative centres and electrically active defects.

Crystallographic defects did not all show substrate temperature dependence. PID's showed no variation with temperature, as would be expected due to their being caused by flux or flaking problems. S-pit densities also showed no change, which is somewhat surprising. Transition metals have high diffusion coefficients at higher substrate temperatures, and might be expected to change the s-pit concentration due to formation of clusters, or

surfacial/interfacial gettering. Dislocations, however, showed a strong dependence, increasing with growth temperature. Chemical analysis by SIMS showed an increase in C and O uptake with temperature, but this alone was unlikely to be the cause of the change in dislocation densities, as there appeared to be little nucleation occurring in the bulk of the epilayer. Since growth was always initiated at a standard clean-up temperature, and the growth temperature affected the dislocation density, it is concluded that most dislocations nucleate in the first few hundred angstroms of growth. The laser light scattering experiments carried out at RSRE, Malvern, showed that this was when the rough Si surface was smoothing out, and it would appear that this process was vital in determining the eventual dislocation density.

Deep levels have a detrimental effect on device performance <Kolbesen & Muhlbauer, 1982>, so these centres must be eradicated to obtain high quality epitaxial material. Since dislocation density increases with substrate temperature, a compromise has to be chosen to optimise layer properties. For homoepitaxy, the ideal would be  $650 < T_g < 700^\circ\text{C}$ , which would yield films with  $\sim 5 \times 10^{12} \text{ traps cm}^{-3}$  and dislocation levels of  $\sim 10^4 \text{ cm}^{-3}$ . For Si-Ge epitaxy,  $T_g$  has to be considerably lower than this (<500-550°C). The current study has shown that epilayer properties deteriorate in this range. Future work must address the fundamental causes of the problems discovered and identified in this study to allow lower temperature epitaxy to yield the highest quality films. Very recent work on the Si-Ge heterojunction

bipolar transistor and Si/Ge multilayerstructures have highlighted the important role being played by metallic contamination.

Carbon incorporation was also found to have a noticeable dependence on substrate temperature, increasing with  $T_g$ , both during growth, and at interruptions in growth. Carbon has been found to have several detrimental effects on Si. Firstly it can act as a nucleation site for defects <McFee et al, 1983>, especially if there is a high oxygen content. It can also have an effect on device performance, especially those designed for high power use, and processing defects have been noted to occur in greater numbers in carbon-rich wafers <Kolbesen & Muhlbauer, 1982>. It has even been postulated that carbon levels within the Si bandgap form a non-radiative path that prevents Si from lasing <Goodman, 1988>.

## Chapter 6. P-type Doping in Si-MBE.

### 6.1 Introduction.

P-type doping in Si-MBE has been heavily researched since the initial development of MBE as a viable technique for producing high quality epitaxial material <Becker & Bean, 1977, Iyer et al, 1981>. Ga has been most widely used as a coevaporated source due to its convenient vapour pressure <Bean, 1981>. However, Ga has some major shortcomings due to its relatively low solid solubility ( $3 \times 10^{18} \text{ cm}^{-3}$ ) in Si at the growth temperatures used, and its incorporation kinetics. During growth of doped epitaxial layers, most dopants form an adlayer of atoms on the growing surface, and it is from this adlayer that dopant is incorporated into available lattice sites <Rockett et al, 1985>. After adsorption, most of the atoms will desorb from the surface, with only a small fraction undergoing incorporation. The number of atoms in the adlayer builds up from the initiation of growth until an equilibrium is obtained between adsorbing and desorbing atoms, this equilibrium being dependent on dopant flux and growth temperature <Iyer et al, 1982>.

However, the nature of the adlayer formed by dopants in Si varies considerably. Auger analysis at room temperature <Allen et al, 1982> of Ga adsorption on Si shows that Ga does not saturate the Auger signal but instead levels out at an equilibrium signal slightly higher than that of Si. This implies that the surface layer is composed of a large amount of Si as

well as Ga. From this observation it has been postulated that Ga forms 3-D islands on the surface during growth *<ibid.>*. Because of this there is no change in the incorporation kinetics after approximately the first monolayer has been adsorbed onto the surface. It was found that the incorporation rate starts to saturate at about a tenth of a monolayer, which supports the theory that the Ga forms clusters. Also, electron diffraction patterns of the clean Si surface became blurred and eventually indistinguishable once approximately five monolayers equivalents of Ga had been deposited.

The desorption energy remained constant between a surface coverage of about 0.1 and several monolayers, and the desorption energy [2.88eV] is almost equal to the vaporization energy [2.9eV] *<Metzger & Allen, 1984>*. This implies the desorbing Ga is mainly leaving from a Ga surface. These Ga islands act as a reservoir of dopant which can smear out an intended dopant profile.

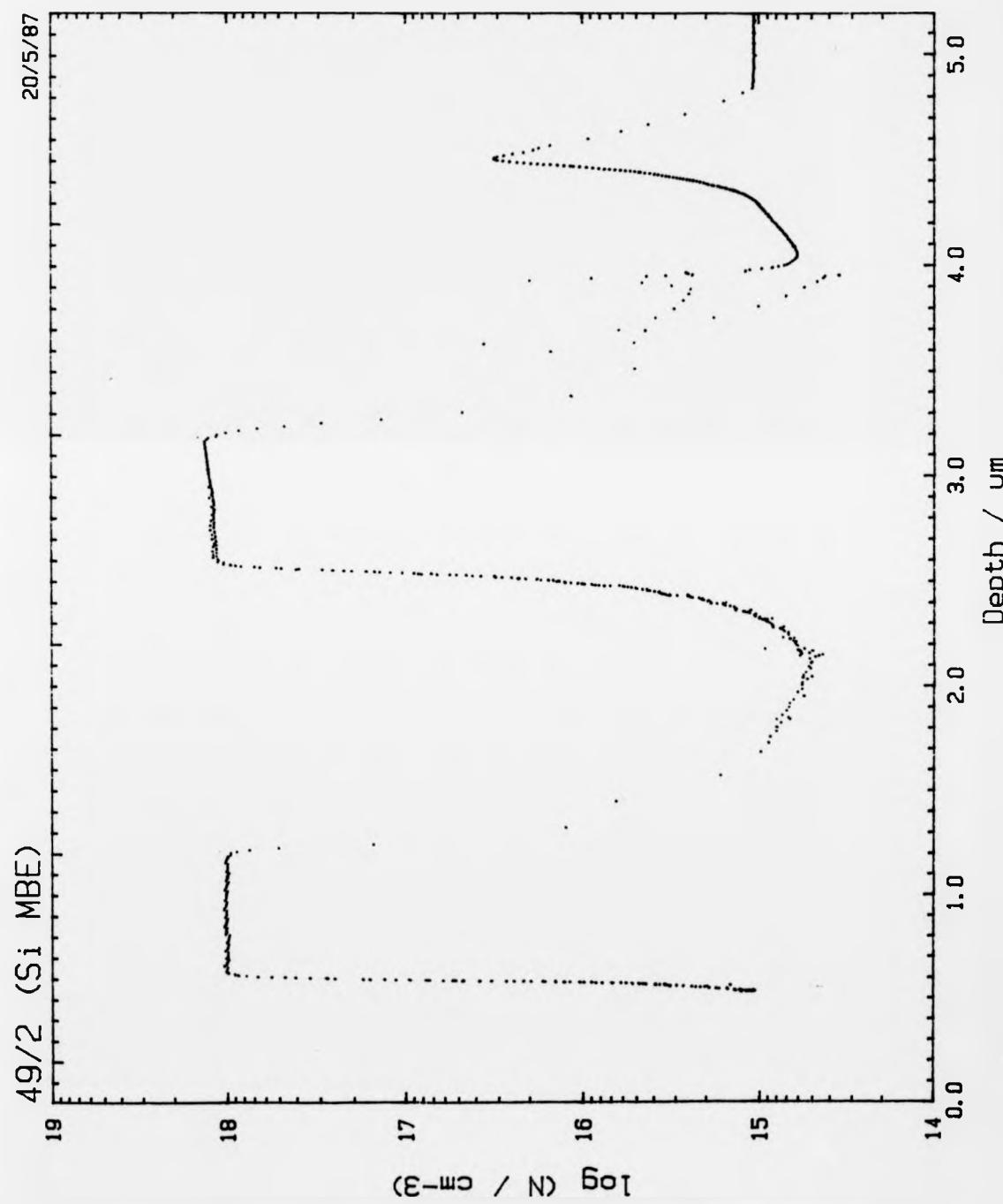
The problems of profile smearing due to an adlayer and low solubility can be overcome by the use of solid phase epitaxy (SPE) in which a thin amorphous layer of highly doped material is grown at room temperature and then recrystallized at high temperature. This method has been used successfully, especially when carried out as an iterative process of successive amorphous growth and recrystallization *<Ahlers & Allen, 1988>*. The material grown by this technique is not, however, of the highest material quality and the process is time-consuming, so has not been generally adopted. There is

also the "build-up/flash-off" method proposed by Iyer <Iyer et al, 1981> in which the dopant adlayer is allowed to reach equilibrium before growth, and when doping is to be terminated the substrate temperature is ramped up to desorb the adlayer. This technique does reduce profile smearing and sharp structures can easily be grown (see Fig. 6.1).

Low energy ion implantation during growth has also been researched <Ota, 1980, Bean & Shadowski, 1982> using ions such as B+, BF<sub>2</sub>+ or Ga+. For this, low energy ions (<1keV) are produced from a plasma, mass filtered, focused and scanned across the wafer during growth. The technique has the advantage that the exponential temperature dependencies of dopant evaporation flux and sticking coefficient, (i.e. the proportion of the incident flux actually incorporated into the epilayer) which make coevaporation dopant concentration hard to control, are not a problem. Precise dopant concentrations can thus be achieved by simply selecting a measured ion current and there is also no smearing of the dopant profile by surface segregation, nor due to the ion implantation since ion energies involved are very low.

However, ion implantation has its own drawbacks, not least of which are the cost and complexity of the source itself. For reasonable epitaxial growth rates, high ion currents are required, which are difficult to obtain with such low energy ions. Initially high growth temperatures were required to achieve good morphology and high

Fig. 6.1 eCV profile showing the abrupt changes in carrier concentration achievable with Ga using the 'build-up/flash-off' technique.



activation, but recent work <Houghton et al, 1988> has shown that high quality material can be grown at temperatures as low as 450°C.

To avoid the problems of Ga doping and the complexity of ion implantation, a great deal of research has recently been carried out into coevaporation B doping. The two most common sources are metaboric acid,  $\text{HBO}_2$  <Tatsumi et al, 1987> and boric oxide,  $\text{B}_2\text{O}_3$  <Ostrom & Allen, 1986>. However, recent work <Tuppen et al, 1988> has shown that oxygen incorporation occurs at substrate temperatures <700°C.

The group at Warwick has been one of the few to use elemental boron as a dopant source. This has the major disadvantage of a very low vapour pressure, which means high cell temperatures are necessary to give viable doping levels. This has been carried out successfully <Kubiak et al, 1985> using a Ta foil boat, giving excellent dynamic range and maximum doping levels ( $2 \times 10^{20} \text{ cm}^{-3}$ ). However, SIMS analyses have shown that unintentional impurities have been incorporated due to a reaction between the Ta cell and the boron <Houghton et al, 1987> [see Fig. 6.2]. A new cell was therefore designed and built to overcome this problem.

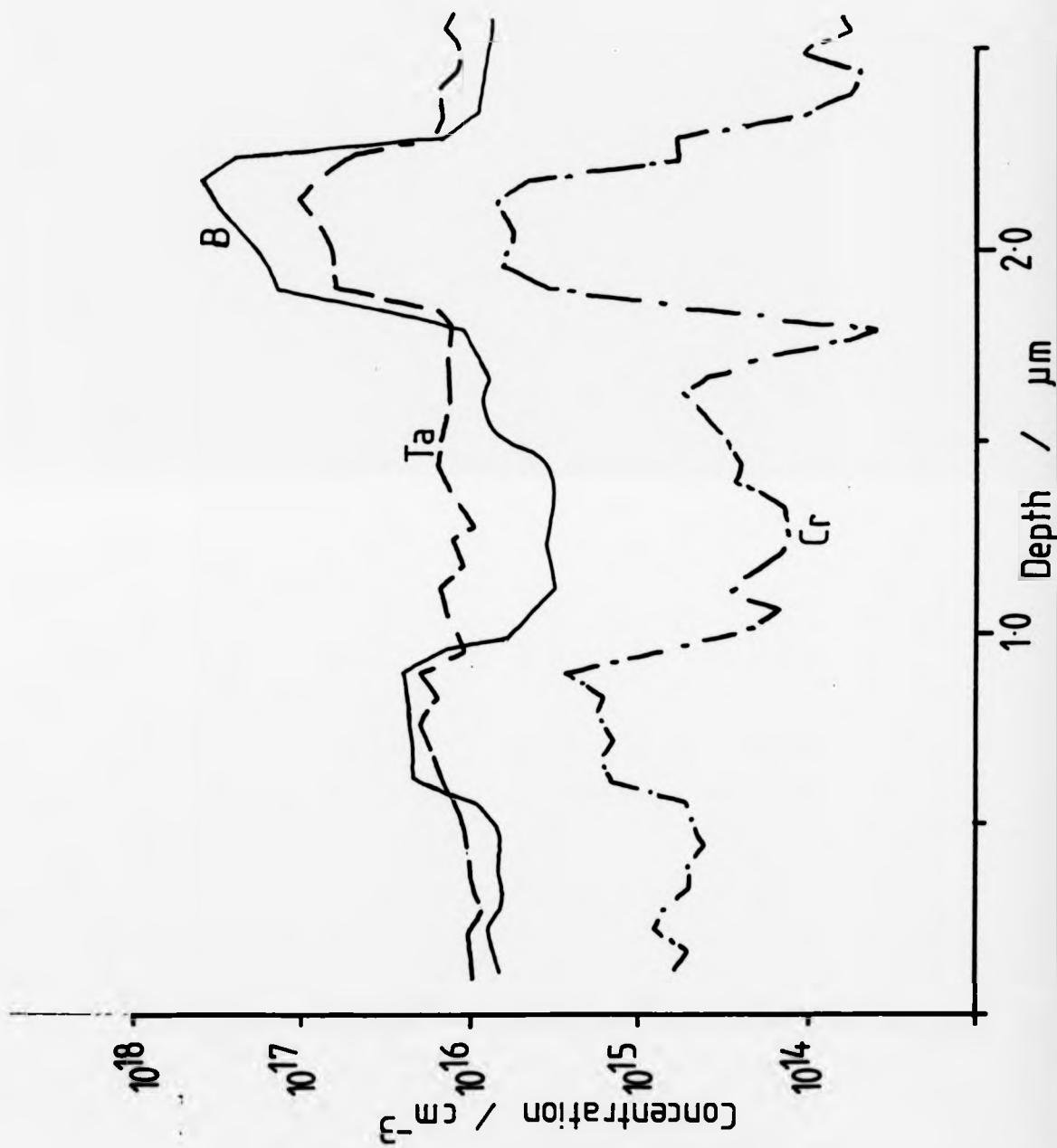


Fig. 6.2 SIMS profile clearly indicating metallic contamination commensurate with B doping when using a Ta boat to evaporate the B. Cr incorporation is due to warming of stainless steel by the unshielded cell. <Houghton et al, 1987>

## 6.2 Source cell designs.

### 6.2.1 Ga cell.

Until now, Ga has been evaporated from a pyrolytic boron nitride [pBN] cell, but it has been shown that this can decompose at the temperatures required for Ga doping <Iyer et al, 1981> (up to  $1150^{\circ}\text{C}$ ), acting as a B dopant source. A novel cell was therefore designed using quartz as the cell material. This has the advantage of being Si based and so should not cause impurities to be released into the system. It was also fairly easy to work, allowing a relatively complicated design to be fabricated, as opposed to the CVD-type process required to make pBN cell. The cell was constructed as in Fig. 6.3. The thermocouple [chromel/alumel] was positioned such that it sat within the Ga charge, but protected by quartz, thus allowing accurate temperature measurements without fear of contact with the source material. The cell was resistively heated by Ta wire wrapped around the outside of the quartz. Ta heat reflectors were placed around the whole assembly to avoid radiative heating of the system.

### 6.2.2 B cell.

Due to the incorporation of Ta caused by reaction between source and cell material, a completely new design

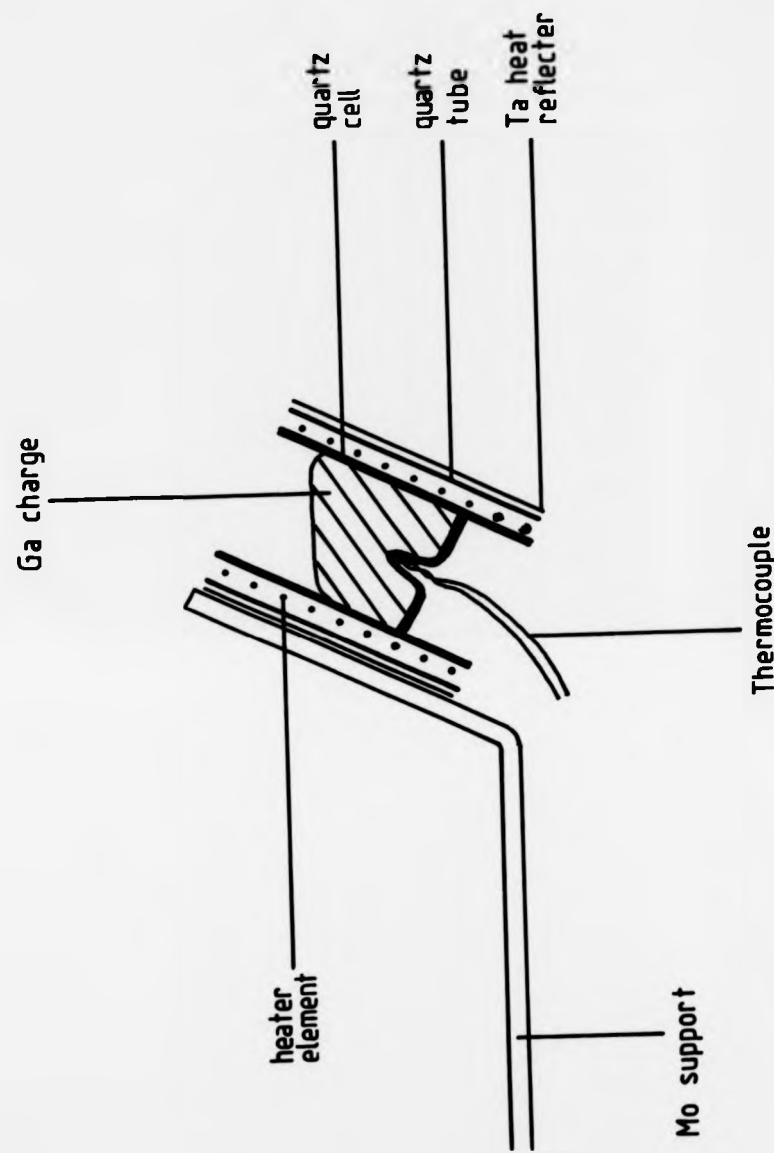


Fig. 6.3 Schematic diagram of Ga cell fabricated from quartz. Note strategic placing of the thermocouple.

was required which avoided contact between B and any refractory metal. After several attempts at using Ta cells lined with graphite foil, and all graphite designs, the cell illustrated in Fig. 6.4 was finally chosen. This consisted of a solid piece of 3mm OD graphite tube turned down and drilled so that the 6N's boron granules could be loaded into it. Electrical contact was made via strips of Mo and Ta foils. Ta was found to diffuse through graphite causing cell failure and possible contamination. Mo foil was therefore used to make direct contact to the graphite. Mo, however, becomes brittle after heating, so a further Ta foil layer was used to provide rigidity.

A disadvantage of this cell was its low electrical resistance, which necessitated the use of a high current (up to 100A at 10V) power supply. Optimum Mo and Ta foil thicknesses and cell design were found, compromising between current required and cell longevity. The cell was then surrounded by a water-cooled jacket to prevent radiative heating of the vacuum chamber, due to the high power being dissipated.

### 6.3 Characterisation.

As in previous chapters, analysis carried out included SIMS, eCV and also Hall measurements of mobility and carrier concentration using the Van der Pauw (1958) technique. Defect etching was routinely carried out on all layers.

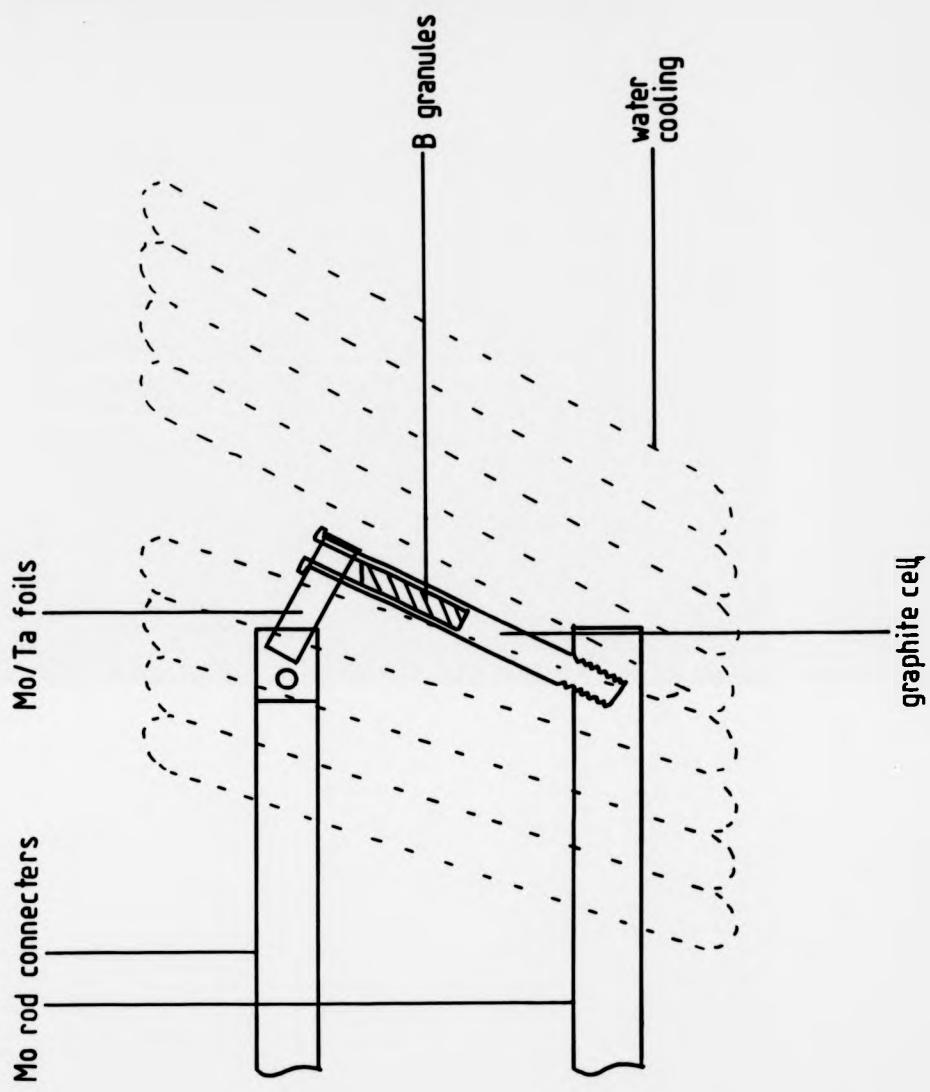


Fig. 6.4 Schematic diagram of B cell designed and manufactured by the author from high purity graphite.

Selected layers were also submitted to transmission electron microscopy (TEM).

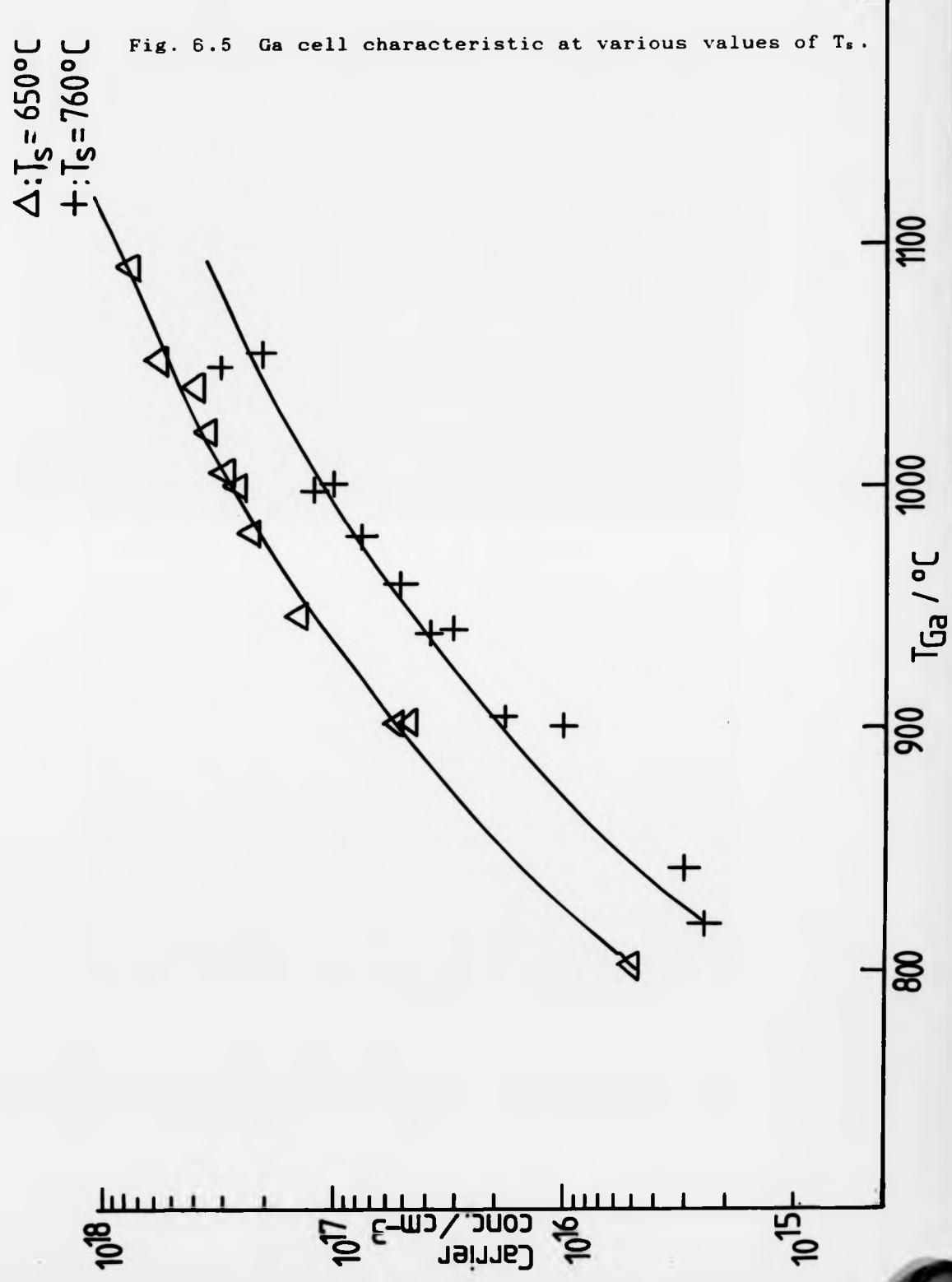
#### **6.4. Results of Ga doping.**

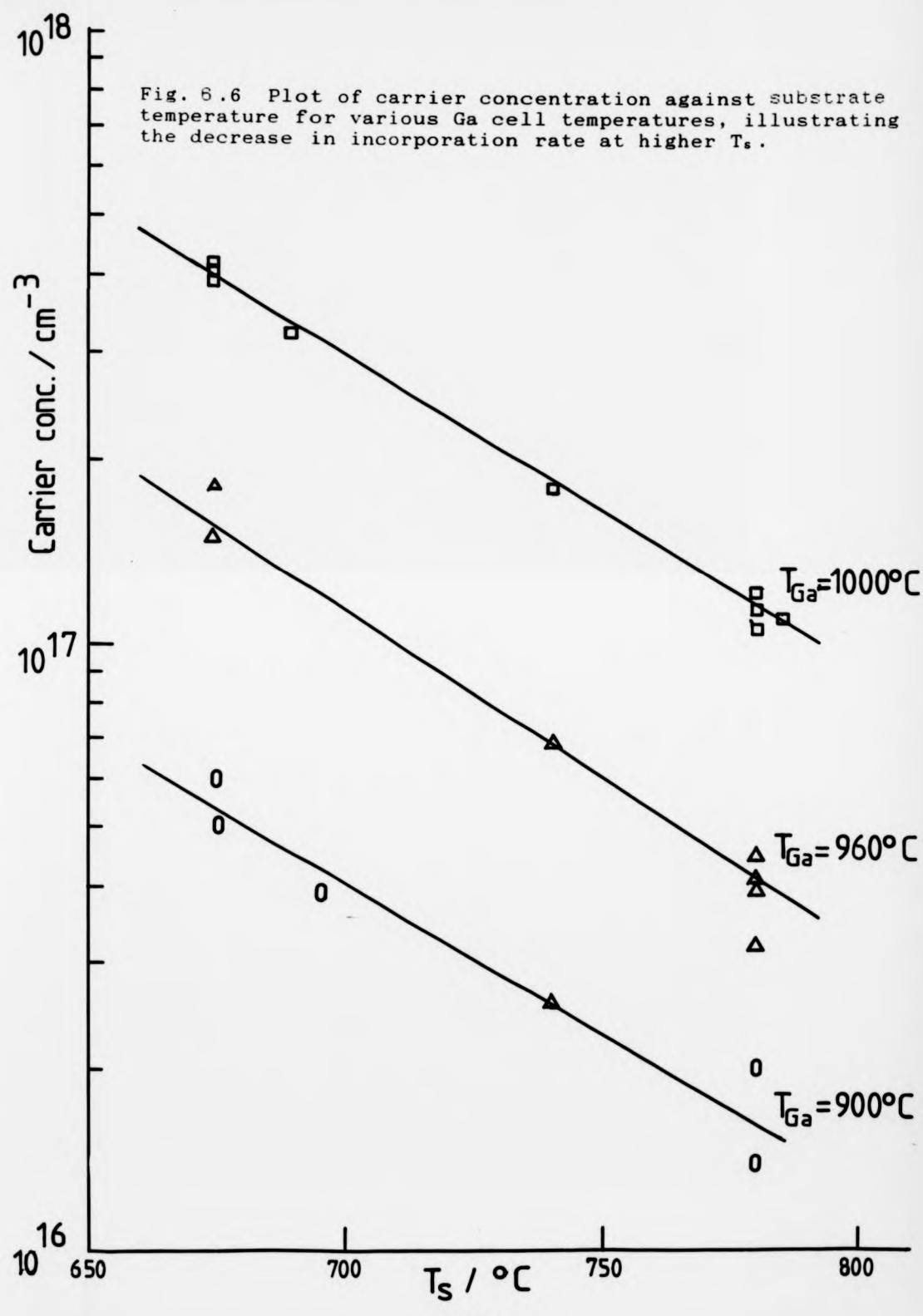
##### **6.4.1 Carrier concentration.**

The effects of source and substrate temperature on doping level are given in Figs. 6.5 and 6.6 respectively. The nature of the source temperature curve suggests that it scales directly with Ga vapour pressure as calculated from the Clausius-Clapeyron equation <see for example, Zemanski & Dittman, 1981 for a derivation of the equation>. The substrate temperature curve shows the normal behaviour of relatively high vapour pressure dopants that form an adlayer on the growing surface <Becker & Bean, 1977>. As the substrate temperature increased, more dopant was thermally desorbed rather than being incorporated into the lattice. Thus the lowest substrate temperatures gave the highest doping levels. The highest doping level achieved in this group of experiments was  $1 \times 10^{18} \text{ cm}^{-3}$  at a substrate temperature of 650°C, and cell temperature of 1100°C. Maximum cell temperature was limited to this due to the range of the chromel/alumel thermocouple used and to avoid the softening of the quartz cell material.

At these relatively high doping levels an increase in the density of dislocations was seen (Fig. 6.7) in uniform epilayers grown without the use of the build-up technique

Fig. 6.5 Ga cell characteristic at various values of  $T_s$ .





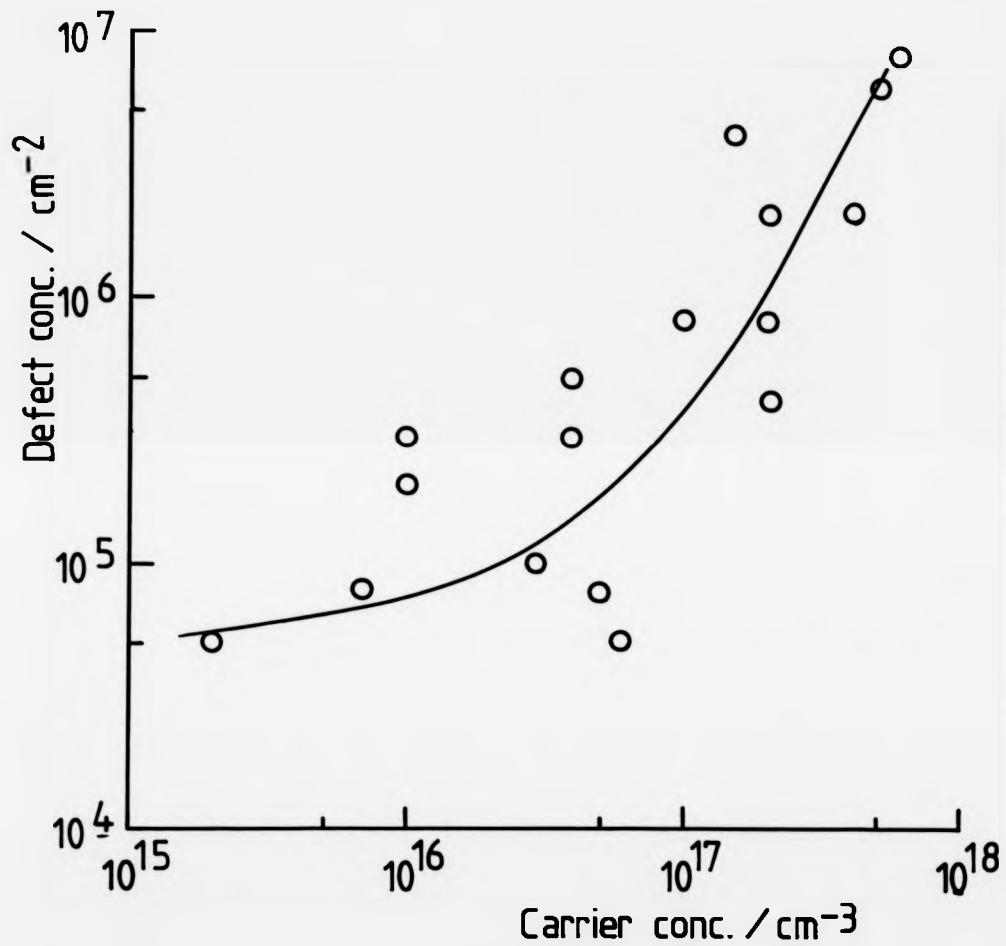


Fig. 6.7 Graph of dislocation etch pit density against carrier concentration for Ga doped material. Note that these layers were grown with no substrate preparation, bar a high temperature oxide desorption at  $850^\circ\text{C}$ , i.e. normal dislocation level  $\sim 10^5 \text{ cm}^{-2}$ . At high Ga doping levels an increase in dislocations is evident.

<Iyer et al, 1981>. This could be due to the strain introduced into the lattice by the relatively large Ga ion <Pinndoria, 1990>, or to a disturbance in growth caused by the adlayer.

A decrease in mobility at 77K compared to bulk B values was noted, as can be seen in Fig. 6.8 which shows mobility as determined by Hall measurements. Mobility values at 300K lie approximately on the bulk value line. These graphs should be compared with the mobility and carrier concentration against temperature curves for Si:Ga and Si:B in Fig. 6.9 for a better understanding of the temperature characteristics of Si:Ga.

At 77K there should be an equal amount of phonon scattering in both Ga and B samples. For a given 77K carrier concentration there should also be an equal number of ionised impurity scattering centres. The only difference is the number of unionised impurities present, implying unionised impurity scattering is playing an important role. Since carrier freeze out occurs more rapidly for Ga due to its higher ionisation energy (the Ga acceptor band lies 72meV above the valence band edge), the density of neutral Ga atoms in a sample of a given 77K carrier concentration is higher than in an equivalent B doped layer. This is somewhat surprising since the influence of unionised scatterers on mobility is usually assumed to be negligible above 20K <Seeger, 1985>.

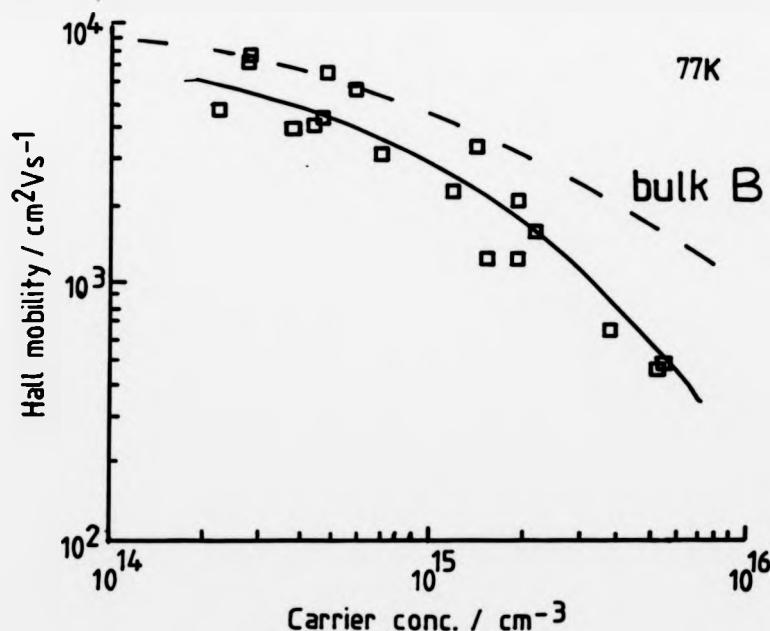
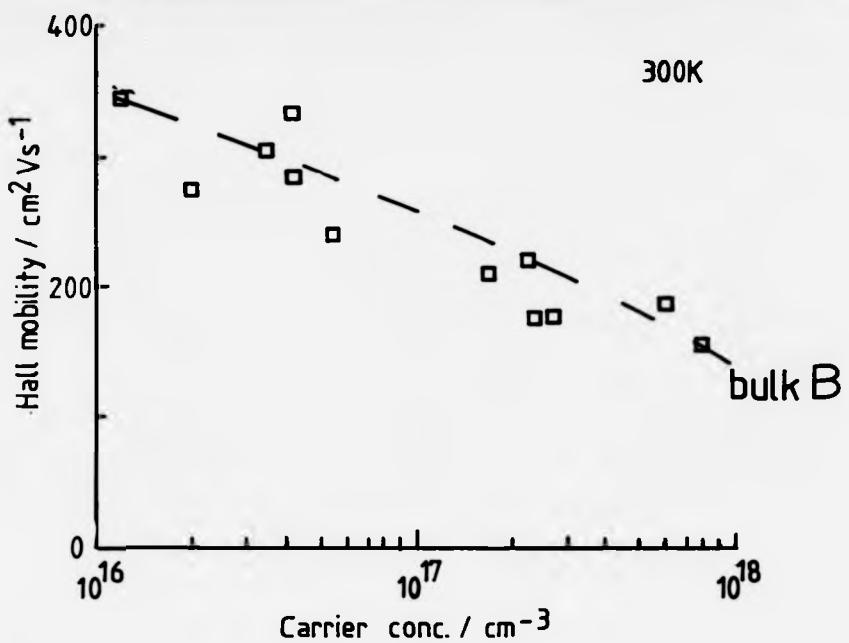


Fig. 6.8 Hall mobilities of Ga doped epilayers at a) 300K and b) 77K. At 77K, mobilities of highly doped layers are considerably lower than those of bulk B doped material.

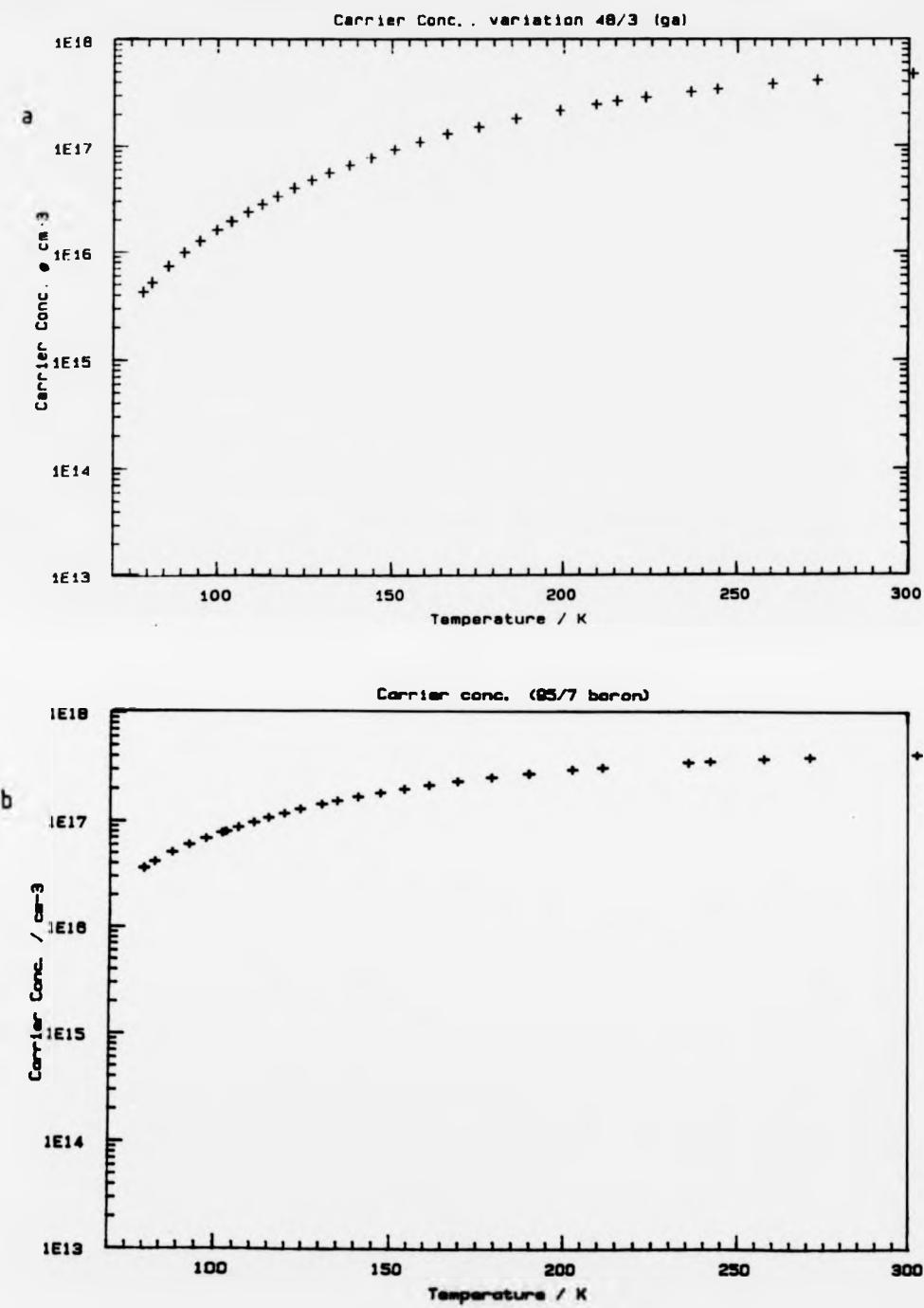


Fig. 6.9 Carrier concentration vs temperature curve from Hall measurements:- a) for Ga, illustrating the relatively high temperature carrier freeze out that occurs due to its high activation energy in Si, b) a boron doped layer for comparison with a.

#### **6.4.2 Profile control.**

##### **6.4.2a Potential enhanced doping (PED).**

The method of potential enhanced doping (PED) in which a negative potential is applied to a substrate during growth to enhance dopant incorporation has been used very successfully with Sb <Kubiak et al, 1985> (see section 2.1). It can give an increase in doping levels of three orders of magnitude, with extremely abrupt transitions. The dopant adlayer acts as a reservoir from which incorporation occurs, and in the time taken for this to reach equilibrium during doping transitions the profile becomes smeared. The use of PED avoids this since a change in surface coverage is not required. During this set of experiments the effect of PED on Ga-doped films was assessed, and the results are shown in Fig. 6.10. It can be seen that for Ga only a very slight enhancement (approximately a factor of two) is seen when a negative voltage is applied to the substrate. Also, there is a decrease in incorporation efficiency for high negative voltages (>500V). In an attempt to understand these phenomena, the mechanism behind the PED effect has been examined, and a new model formulated.

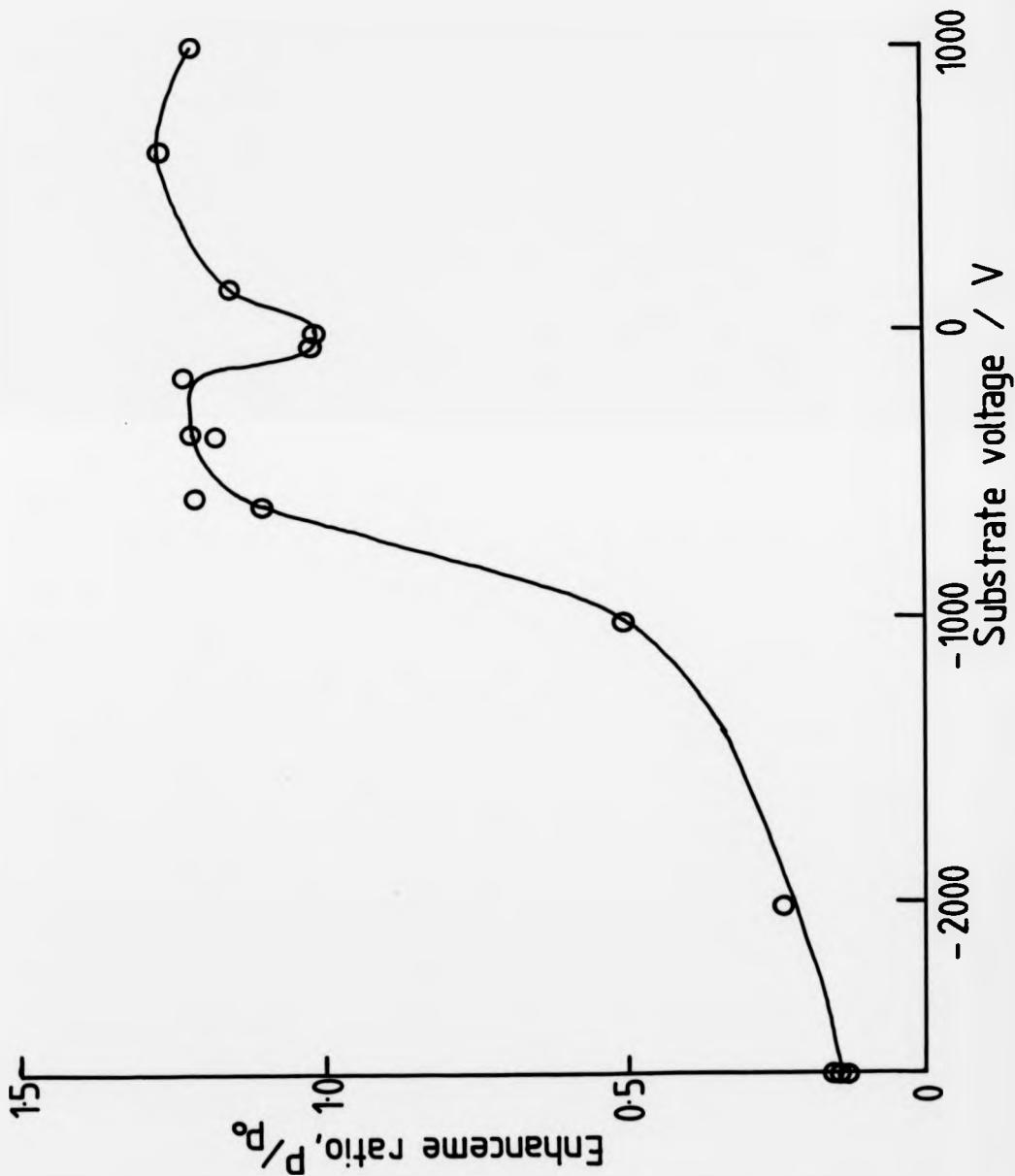


Fig. 6.10 Graph showing the effect of PED on carrier concentration for Ga doped layers. The maximum enhancement ratio is negligible compared for that achieved with Sb. The reduction in incorporation at high negative bias may be due to adlayer polarization.

#### 6.4.2a A new model for potential enhanced doping.

It has been proposed by Jorke <1986> that the PED technique relies on secondary implantation of dopant atoms from the adlayer by Si<sup>+</sup> ions formed during the electron beam irradiation of the Si charge. The fact that it is Si<sup>+</sup> ions that are the cause of the enhancement is implied by the fact that only negative voltages show a reproducible effect <Kubiak et al, 1985> and by work involving additional ionisation of the Si flux by use of an electron impact ioniser <Jorke and Kibbel, 1985> which shows that the enhancement can be increased. Positive substrate voltages, which would attract electrons to the substrate, have been found to cause a highly unreproducible effect. This is in contrast to work carried out using electron irradiation from an electron gun during Sb doping <Delage et al, 1987>. This showed enhanced incorporation of a similar order to that during PED. They attributed this to cracking of Sb<sub>4</sub> into the monoatomic form, thus aiding incorporation. The causal effect would appear to be different from that involved in PED, since the charge is naturally opposite, and the current density required was approximately 100 times that used in PED. [Delage used a maximum total emission current of 2.5mA defocused to impinge on a 2" substrate, equivalent to -100uAcm<sup>-2</sup>]. Ion emission from the electron gun may also have been occurring.

It has previously been calculated <Iyer & Delage, 1988>

that approximately  $3 \times 10^{-6}$  of the total Si flux leaving the evaporator is ionised. This does not agree with work carried out by Airco Temescal on the e- gun used in this study, which suggests that approximately  $5 \times 10^{-4}$  (0.05%) of the flux was ionized <Hill, 1988>. For direct secondary implantation to account for doping levels of  $10^{19} \text{ cm}^{-3}$ , the number of ions impinging at the growth surface would need to be  $1 \times 10^{13} \text{ cm}^{-2 \text{s}^{-1}}$  at a growth rate of 5A/s. At this rate the Si flux,  $F_{\text{Si}}$ , will be  $2 \times 10^{15} \text{ cm}^{-2 \text{s}^{-1}}$ . Assuming ions can be attracted from the flux from an area ten times greater than that of the substrate <Jorke, 1988> then the ion flux,  $J_I$ , will be

$$\begin{aligned} J_I &= 10 \times \text{Si flux} \times \text{ionized fraction of flux} \quad 6.1 \\ &= 10 \times 2 \times 10^{15} \times 5 \times 10^{-4} \\ &= 1 \times 10^{13} \text{ cm}^{-2 \text{s}^{-1}} \end{aligned}$$

High doping levels would thus require the optimum case that every impinging  $\text{Si}^+$  ion hits and implants an Sb atom. This is not likely to be the case, however, since the Sb adlayer is <1 monolayer thick [both Iyer and Jorke assumed ~0.1 monolayer ( $1 \times 10^{14}$  atoms  $\text{cm}^{-2}$ ) in their calculations]. Since the covalent radius of an Sb atom is 1.41Å, the fraction of the surface,  $A_{\text{Sb}}$ , covered by Sb will be given by

$$A_{Sb} = (1.41 \times 10^{-8})^2 \times \pi \times 1 \times 10^{14}$$
$$= 6.2 \times 10^{-2}$$
$$\sim 1/16 \text{ of surface}$$

6.2

This therefore shows that only about 1 ion in 16 is likely to directly hit an Sb atom. Also for a relatively light ion such as Si (mass 28) to exchange enough momentum to allow a heavy atom such as Sb (mass 123) to be secondarily implanted below the first monolayer of Si, the incident angle would need to be very close to the normal, which will not generally be the case. The probability of a single Si<sup>+</sup> ion being able to incorporate more than one Sb atom, as proposed by Iyer, is negligible <Kelly, 1985>. The overall probability of recoil implantation occurring is thus extremely low.

The author therefore proposes a different mechanism for incorporation enhancement caused by the use of PED. This involves the lattice damage caused as the incident Si<sup>+</sup> ions lose their energy in the crystal. It is proposed that the vacancies thus caused act as incorporation sites for dopant atoms from the adlayer, increasing the rate of uptake of dopant, and thus the carrier concentration. These vacancies act as preferential incorporation sites for the same reasons as the terraces which form the normal two-dimensional mode of growth. Dangling bonds provide potential wells into which adatoms will fall and be incorporated into the lattice <kelly, 1985>. The fact that some Si atoms segregate to the surface during damage formation means that there are not enough impact-created interstitial Si atoms to refill all the vacancies created, thus the lifetime of the vacancy is prolonged.

The effect of ion and neutron irradiation on the crystal lattice has long been studied <Kinchin and Pease, 1955><Bauerlin, 1962>, and the formation of vacancies and interstitials studied. This has shown that the maximum number of displaced atoms,  $N(E)$ , caused by an impinging ion is given by the expression

$$N(E) = 0.42 \times E/E_d \quad 6.3$$

where  $E$ =energy of impinging ion

$E_d$ =threshold energy for  
displacement.

For this work, the damage caused by impinging  $\text{Si}^+$  ions has been modelled by the author using an implantation analysis programme known as "SUSPRE" <SUSPRE, 1986>. This relates the damage induced in the lattice to the nuclear energy deposition profile due to bombardment, using a modified <Norgett et al, 1975> Kinchin-Pease formula, i.e.

$$\text{Damage}(x) = 0.42 \times E_n(x)/E_d \quad 6.4$$

where  $E_n(x)$ =nuclear energy loss at depth  $x$ .

The equation used to calculate the fractional damage is

$$D(x) = N \cdot (1 - \exp(-P(x)/s)) \quad 6.5$$

where  $N$ =atomic density of target

$s$ =sputtering yield

$P(x)$ =integral of damage( $x$ ) between

$x$  and  $x+t$  where  $t$  is the

thickness eroded by the beam.

The program gave a damage profile for given incident energy and ion dose for specified impinging and target species. The dose was calculated from the incident ion current during growth. This was measured by placing a Faraday cup in the position of the substrate during evaporation, and biasing the cup in a similar manner to that used for the substrate during PED. The results of this are shown in Fig. 6.11.

The model then predicted the percentage damage (i.e. the ratio of off-site to on-site atoms  $\times 100$ ) at a given depth. It was assumed for these calculations that the damage occurring within the first two monolayers of the epilayer would account for the majority of sites for incorporation, and so their number,  $N_{\text{dam}}$ , was calculated by multiplying the percentage damage in the first two monolayers by the number of atoms in a monolayer, i.e.

$$N_{\text{dam}} = D_1/100 \times n_{\text{mono}} + D_2/100 \times n_{\text{mono}} \quad 6.6$$

where  $D_1$ =% damage in 1st monolayer

$D_2$ =% damage in 2nd monolayer

$n_{\text{mono}}$ =number of atoms in a monolayer

( $\sim 1 \times 10^{15} \text{ cm}^{-2}$ ).

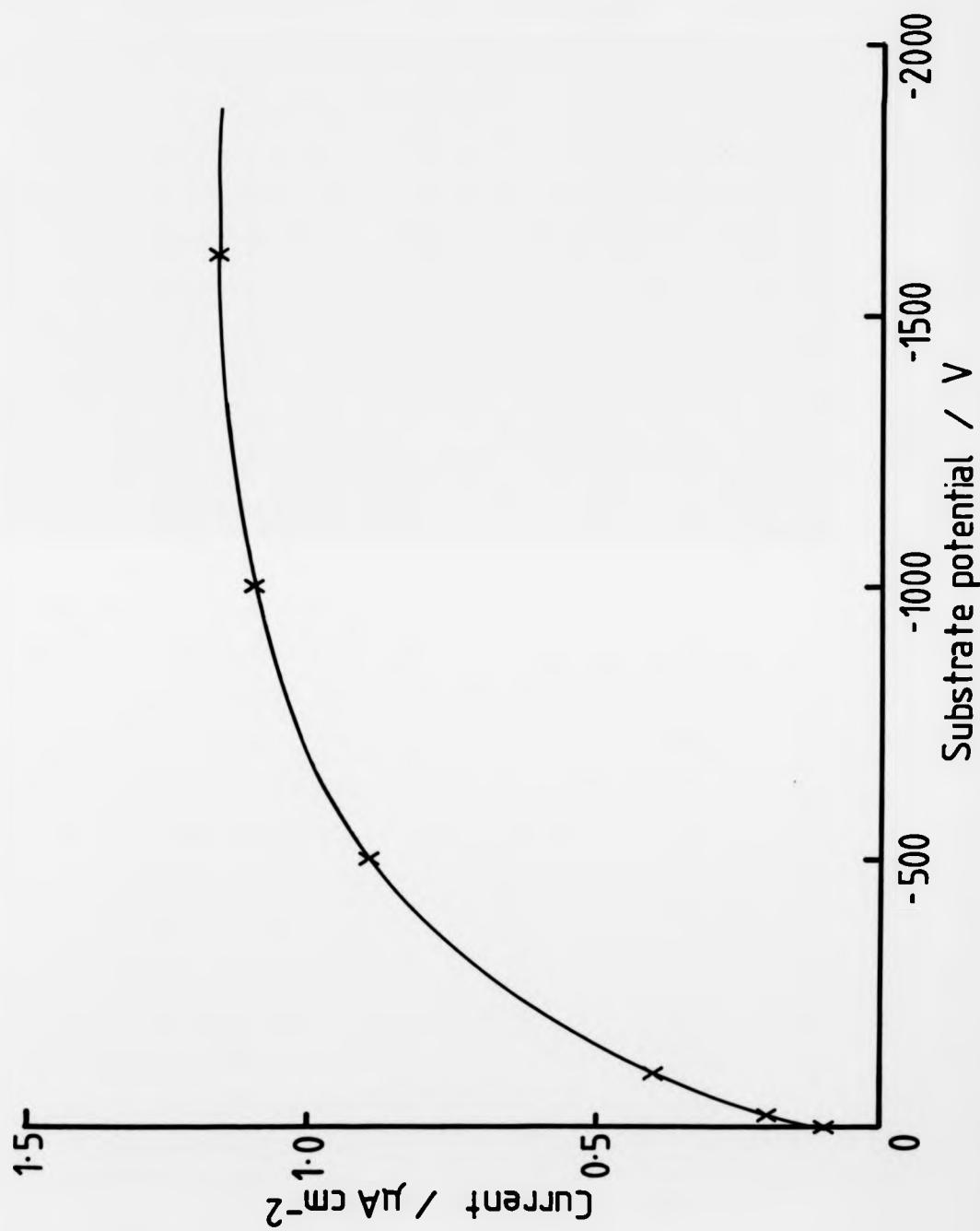


Fig. 6.11 Graph of ion flux against substrate voltage as measured by a Faraday cup in place of the substrate.

**Fig. 6.12 compares  $N_{\text{dam}}$  with the enhancement ratio  $n/n_0$**  (where  $n$  is the carrier concentration with PED and  $n_0$  is the carrier concentration under identical conditions but without PED) over a range of substrate voltages for Sb doping. Both curves exhibit the same dependence on voltage, showing that the enhancement ratio increases in proportion to the number of damage sites. This is strong support for the hypothesis that segregation and damage are responsible for the PED effect.

The number of vacancies created is also of the right order to give the carrier concentration seen during PED.  $2 \times 10^{13} \text{ cm}^{-2}$  vacancies at a substrate potential of 2.6kV is equivalent to  $\sim 6 \times 10^{20} \text{ cm}^{-3}$  in the bulk. Assuming some of these will be taken up by arriving Si atoms, and some may be annealed faster than dopant incorporation can occur, this is consistent with the carrier concentration  $\sim 4 \times 10^{19} \text{ cm}^{-3}$  ( $T_g = 750^\circ\text{C}$ ) seen at this voltage (and similarly for those over the whole range of voltages used for PED).

The enhancement ratio has been seen to be independent of substrate temperature <Kubiak et al, 1985>. (This is not to be confused with the absolute reduction in carrier concentration at high  $T_g$  caused by reduced adlayer coverage, which is accounted for by using the ratio  $n/n_0$ .) Since the damage would be annealed faster at higher temperatures it might be expected that the reduction in the number of vacancies would have the effect of decreasing the incorporation enhancement. However, the increased

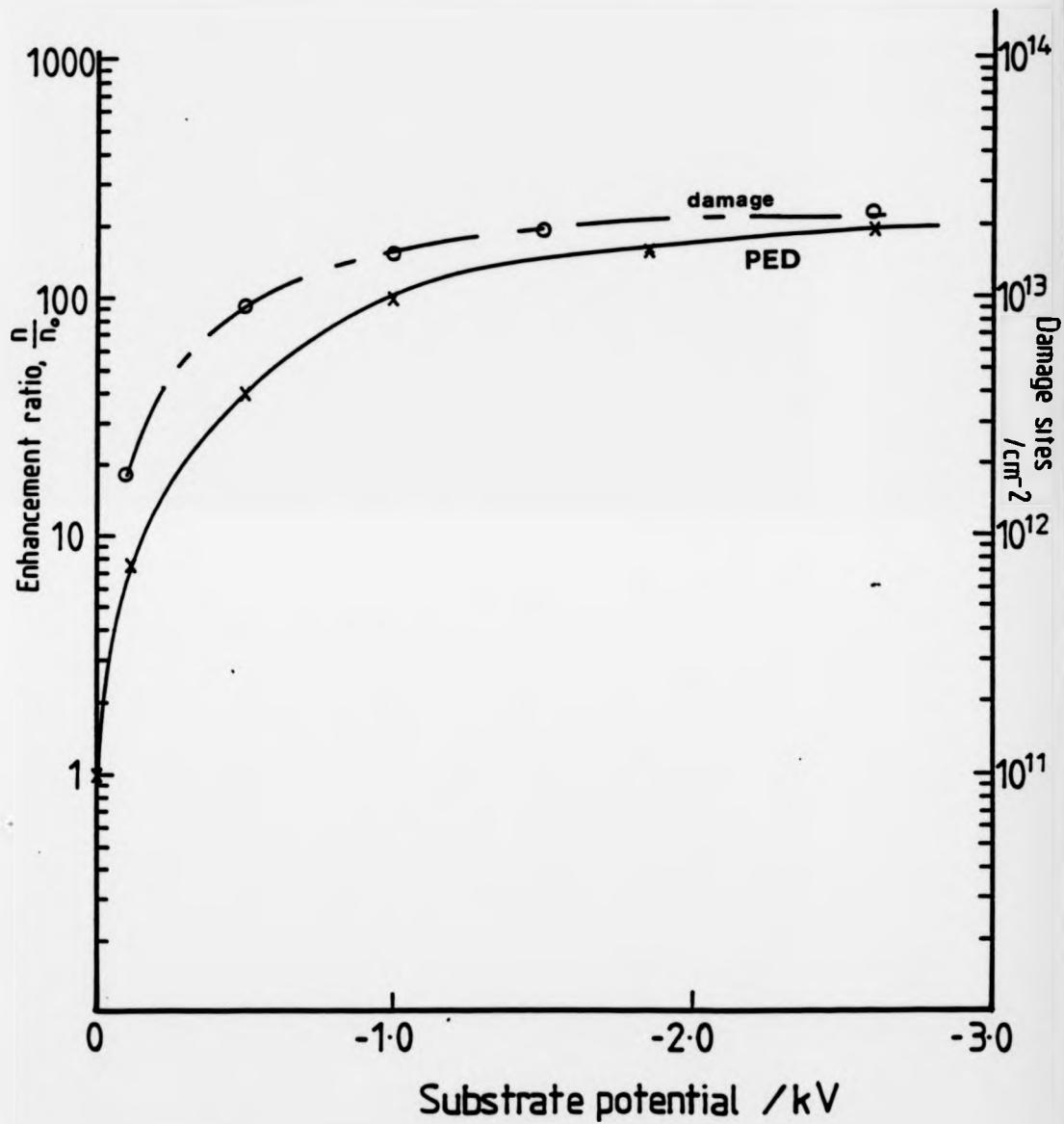


Fig. 6.12 Graph illustrating the correlation between the number of damage sites in the first two monolayers with the PED enhancement ratio,  $n/n_0$  (i.e. ratio of carrier concentrations with and without PED) for various substrate voltages.

temperature would also raise the surface mobility of the dopant atoms in the adlayer, allowing faster migration to a damage site, compensating for the more rapid annealing. The independence from substrate temperature is therefore consistent with the theory.

As stated previously, the relatively low levels of damage induced by these low energy Si<sup>+</sup> ions are continually being annealed out at the temperatures used for growth, in a similar manner to that caused during intentional ion-implantation during growth, so layer quality is not affected.

Using this new PED model, a further explanation for the effects of PED on Ga doping can be put forward. The agglomeration of Ga atoms on Si into three-dimensional islands means that their surface mobility on Si is lower than Sb, with its uniform, submonolayer coverage. Since the enhancement in incorporation requires migration to damage sites, the PED effect on Ga will be smaller. At high substrate potentials incorporation efficiency for Ga actually decreases from its value without PED. A possible cause of this decrease is that the substrate voltage affects the polarizability of the adatom. It has been found <Chopra, 1966> that this can lead to enhanced island formation of metals on glass. If this were the case, tighter binding of Ga islands might mean fewer atoms were available to incorporate at growth steps or damage sites, due to an even lower surface mobility.

An effect similar to the decrease in Ga incorporation efficiency during PED has also been noted in Ga ion doping with 100% Ga ions <Sakamoto & Komura, 1983>. An

accelerating voltage of 1kV was found to yield lower carrier concentrations than an accelerating voltage of 500V, but no physical reason for this was given.

#### 6.4.2c Build-up/Flash-off.

This technique in which the adlayer is carefully controlled, as mentioned in section 6.1, has been used effectively, but some deficiencies have been found during this series of experiments. When using the build-up technique the author has found that an inactive spike of Ga is incorporated into the layer. This can clearly be seen by comparing the eCV in Fig. 6.13 with the SIMS profile in Fig. 6.14. Such a large spike of Ga will inevitably strain the lattice, perhaps nucleating dislocations.

There are two possible reasons for the appearance of such a spike. The first is that the adlayer is at an equilibrium level different to that during growth. The second is that Ga atoms are incorporating at lattice sites during the build-up process, implying that incorporation is time dependent rather than dependent on the equilibrium between the adlayer and the lattice. The fact that Ga doping is independent of growth rate under normal circumstances <Iyer et al, 1981> suggests the first hypothesis is more likely.

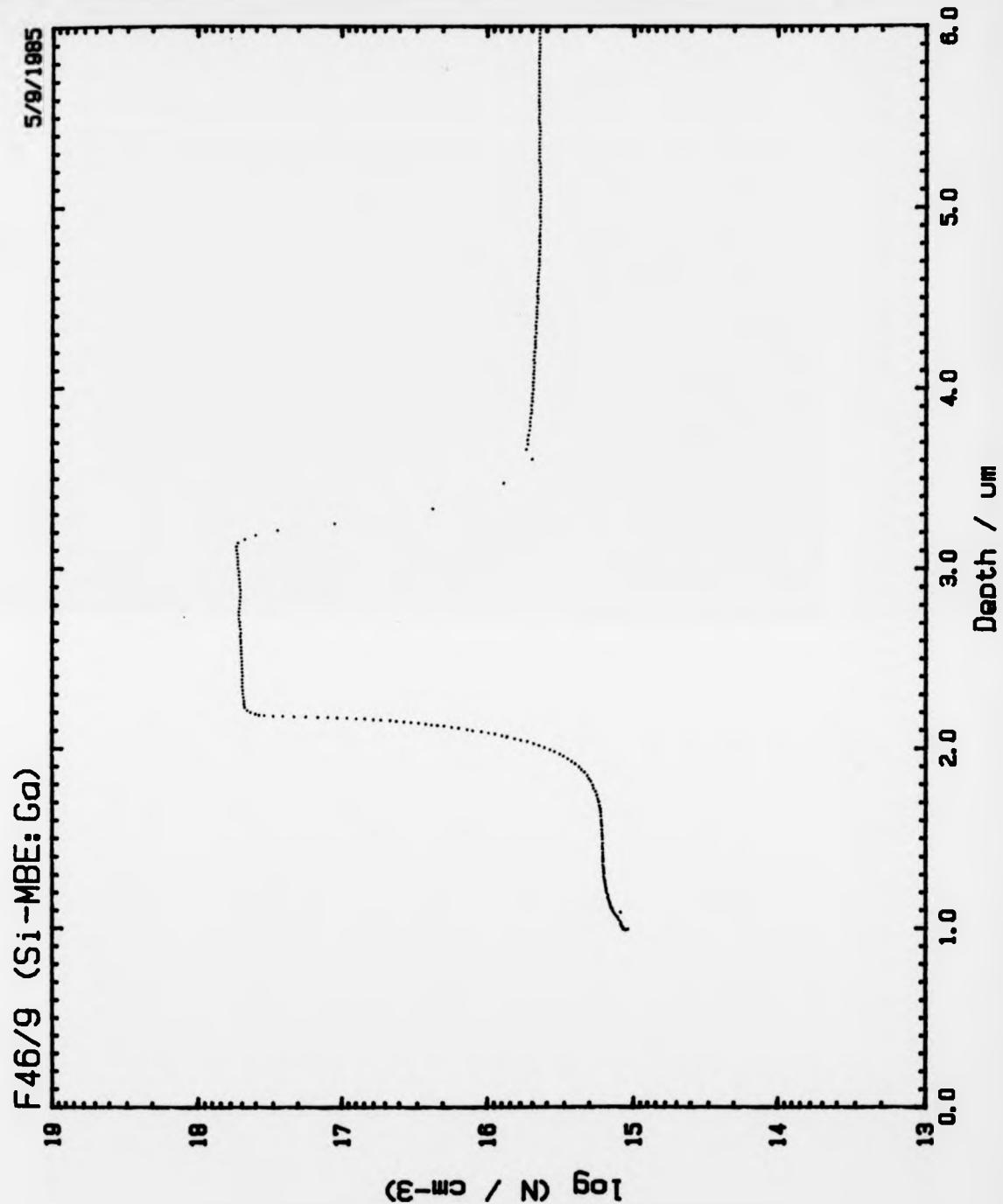


Fig. 6.13 eCV profile of Ga doped layer in which the 'build-up' profile control technique was used. (c.f. Fig 6.14)

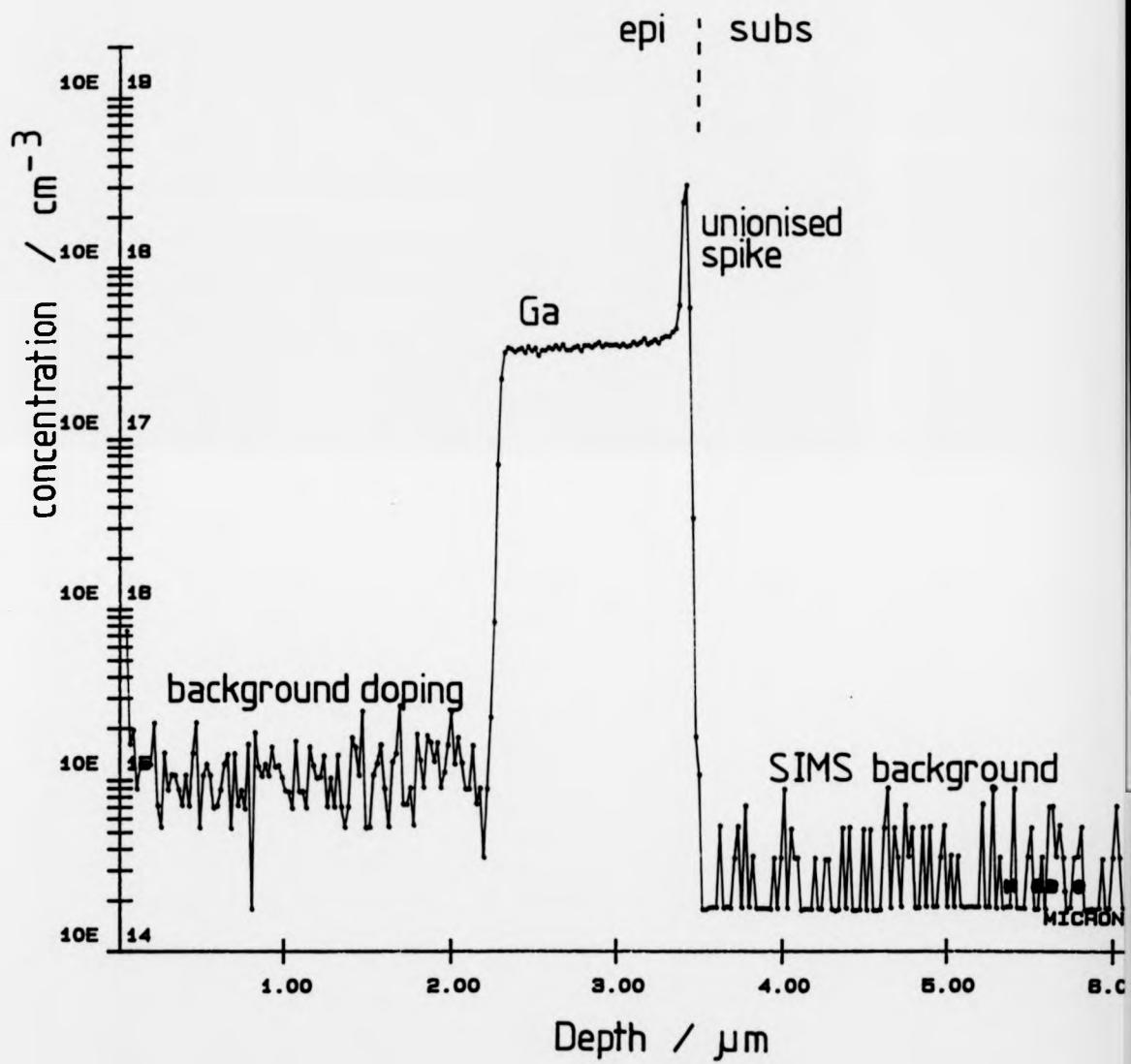


Fig. 6.14 SIMS profile of same layer as in Fig. 6.13, with inactive dopant spike clearly visible where 'build-up' was performed. (SIMS carried out for the author by SAT)

#### 6.4.3 The effect of Ga on background doping.

As has been discussed in previous chapters, the minimum residual doping level is  $<10^{14}\text{cm}^{-3}$  n-type. However, after having used Ga as a dopant for about 50um growth, the background had become  $1\times10^{15}\text{cm}^{-3}$  p-type. The level was found to increase steadily during a growth series. This memory effect, caused by re-evaporation of Ga from hot surfaces, was probably due to the substrate heater and components around this, especially the substrate holder, which naturally receives a high Ga flux. System walls were protected by cryopanels for this series of experiments.

#### 6.5 B doping.

The doping level against cell temperature for the B cell made from graphite is shown in Fig. 6.15. The B doping level is inversely proportional to growth rate but independent of substrate temperature, with unity sticking coefficient <Kubiak et al, 1985>. The calibration curve in Fig. 6.16 has thus been normalized to a growth rate of 5A/s. The maximum doping level achieved was  $2\times10^{19}\text{cm}^{-3}$  at 2A/s (limited by the contacts weakening at high cell temperature), lower than that achievable by the most recent experiments with compound sources <Tatsumi et al, 1987>, but without the inherent oxygen incorporation, that occurs at lower substrate temperatures. Because B diffuses rapidly in Si above 750°C <McPhail et al, 1988>, low

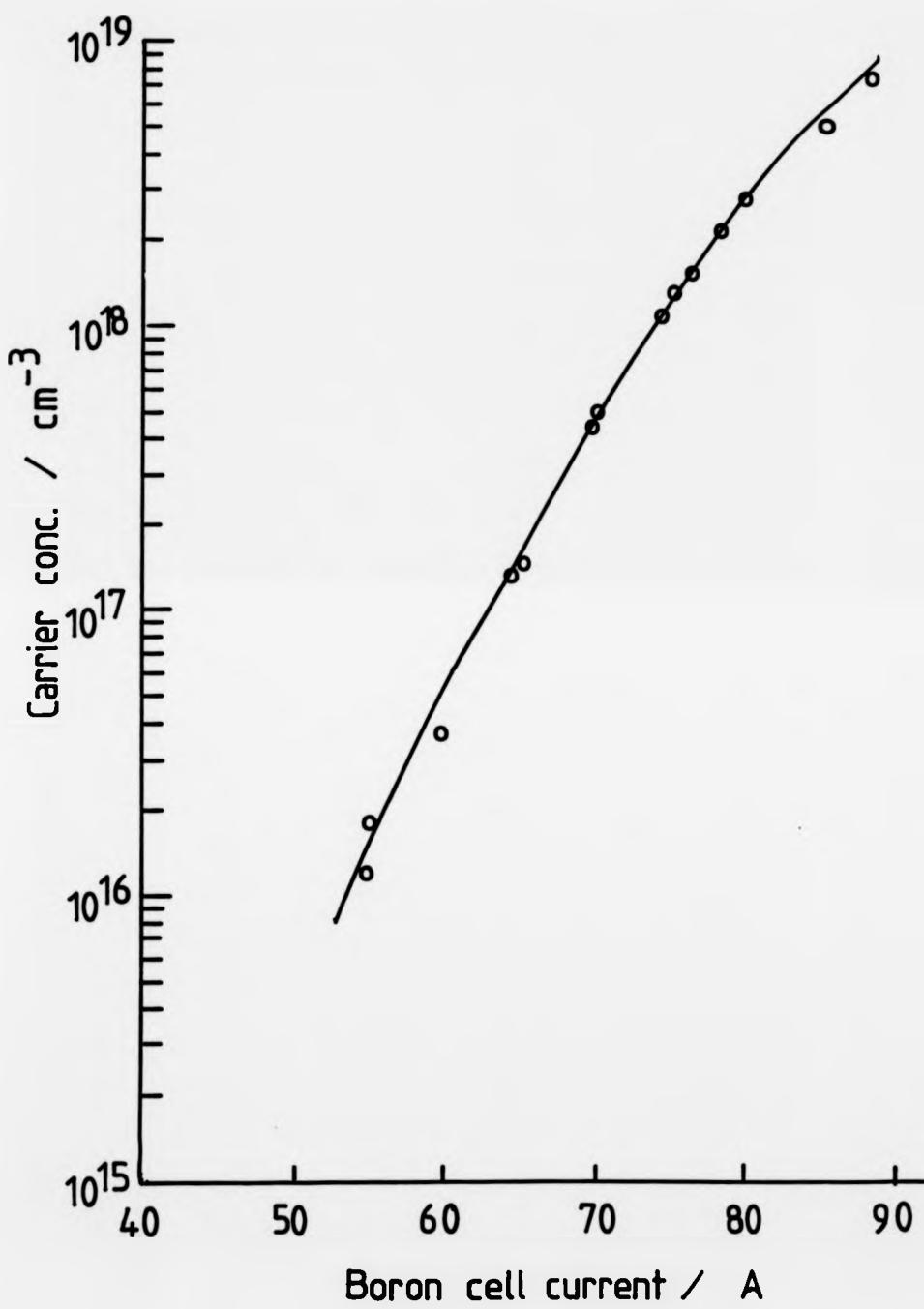


Fig. 6.15 Carrier concentration against B cell input current. All points are normalised to a growth rate of 5A/s.

substrate temperatures are required for sharp profiles, and are vital for structures such as delta-doped FETs (see Chapter 7), camel diodes and doping superlattices.

The main aim of this design of source cells was to give a pure dopant flux, with reliable and stable characteristics. Fig. 6.16 shows a SIMS profile for impurities in a B-doped layer using this graphite cell and shows no unintentional impurity incorporation. No degradation in vacuum quality was evident once the cell had been thoroughly outgassed, despite the high temperature needed for B evaporation, indicating that the water-cooled shroud was preventing radiative heating of the chamber. It was found that a critical temperature had to be reached to achieve full outgassing (-1600°C). After this, the large hydrocarbon and CO<sub>2</sub> peaks became negligible. The only peaks remaining were H<sub>2</sub> and CO (see Fig. 6.17).

Transitions in carrier concentrations using this design of cell are extremely sharp due to its very low thermal mass. Fig. 6.18 shows the wide dynamic range and abrupt transition that can be made with the cell.

Cell lifetime was found to be good once an optimum design had been chosen. Well over 100um of B-doped material of various carrier concentrations (up to  $2 \times 10^{19} \text{ cm}^{-3}$ ) were grown with the same cell without it failing. Over this period calibration remained constant, indicating very good stability (Fig. 6.15). This is partly due to the fact that only a very small amount of B actually sublimes to generate

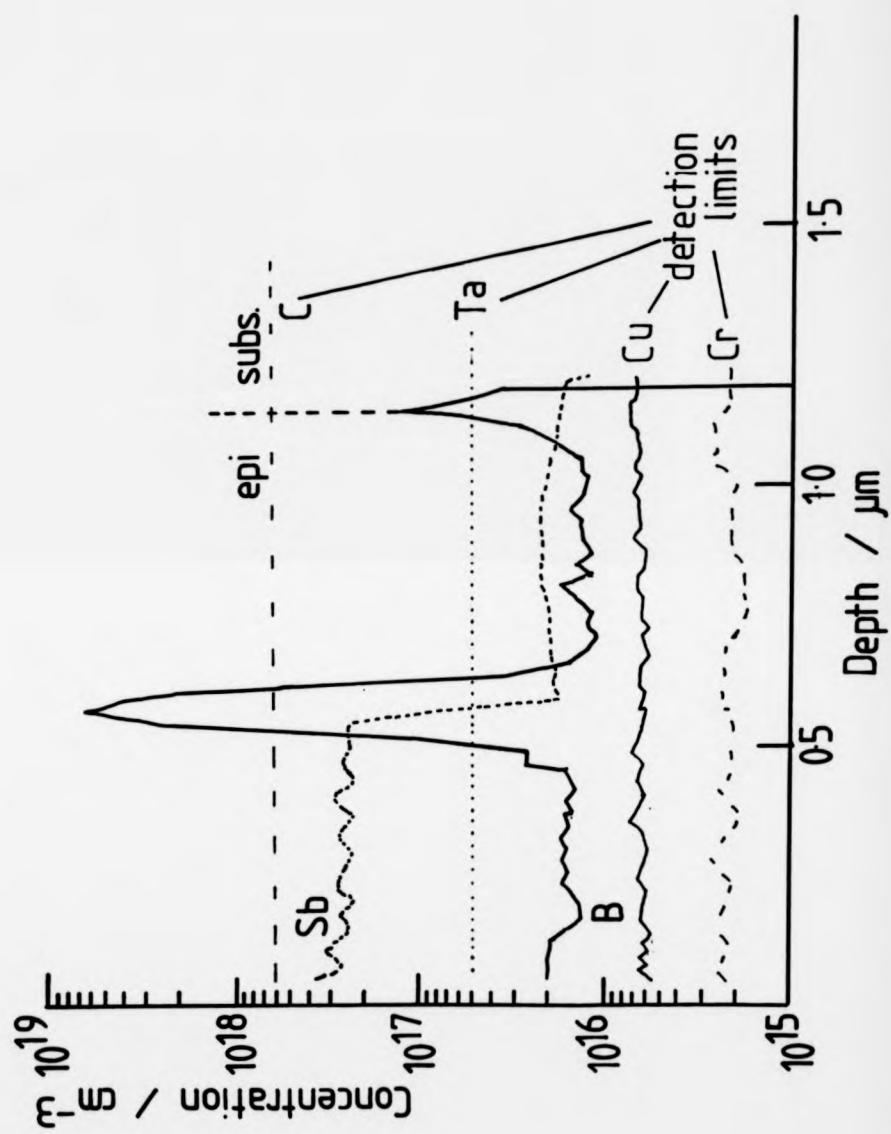


Fig. 6.16 SIMS profile of B spike grown using the graphite cell. No metallic or carbon contamination was detected.

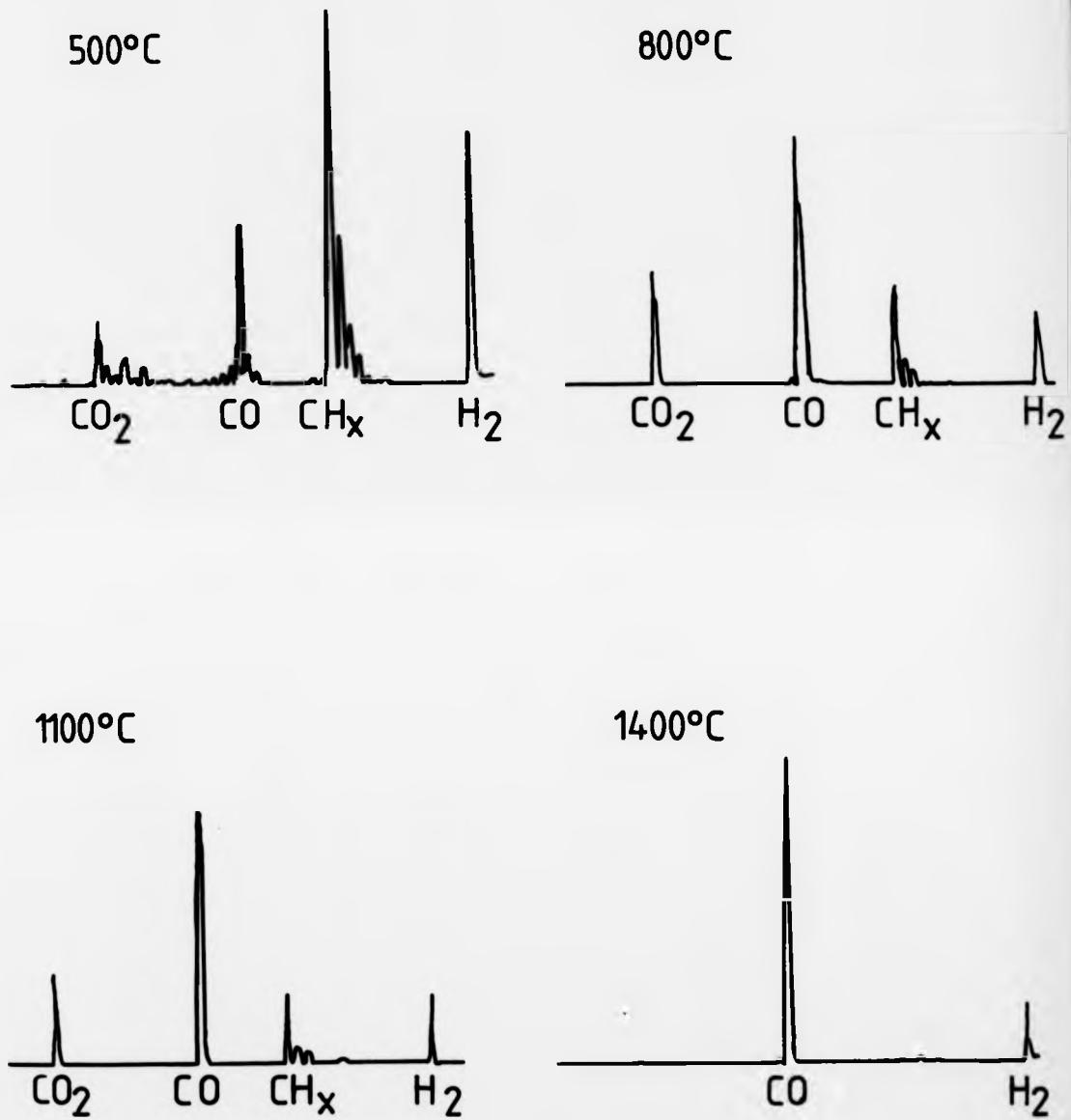
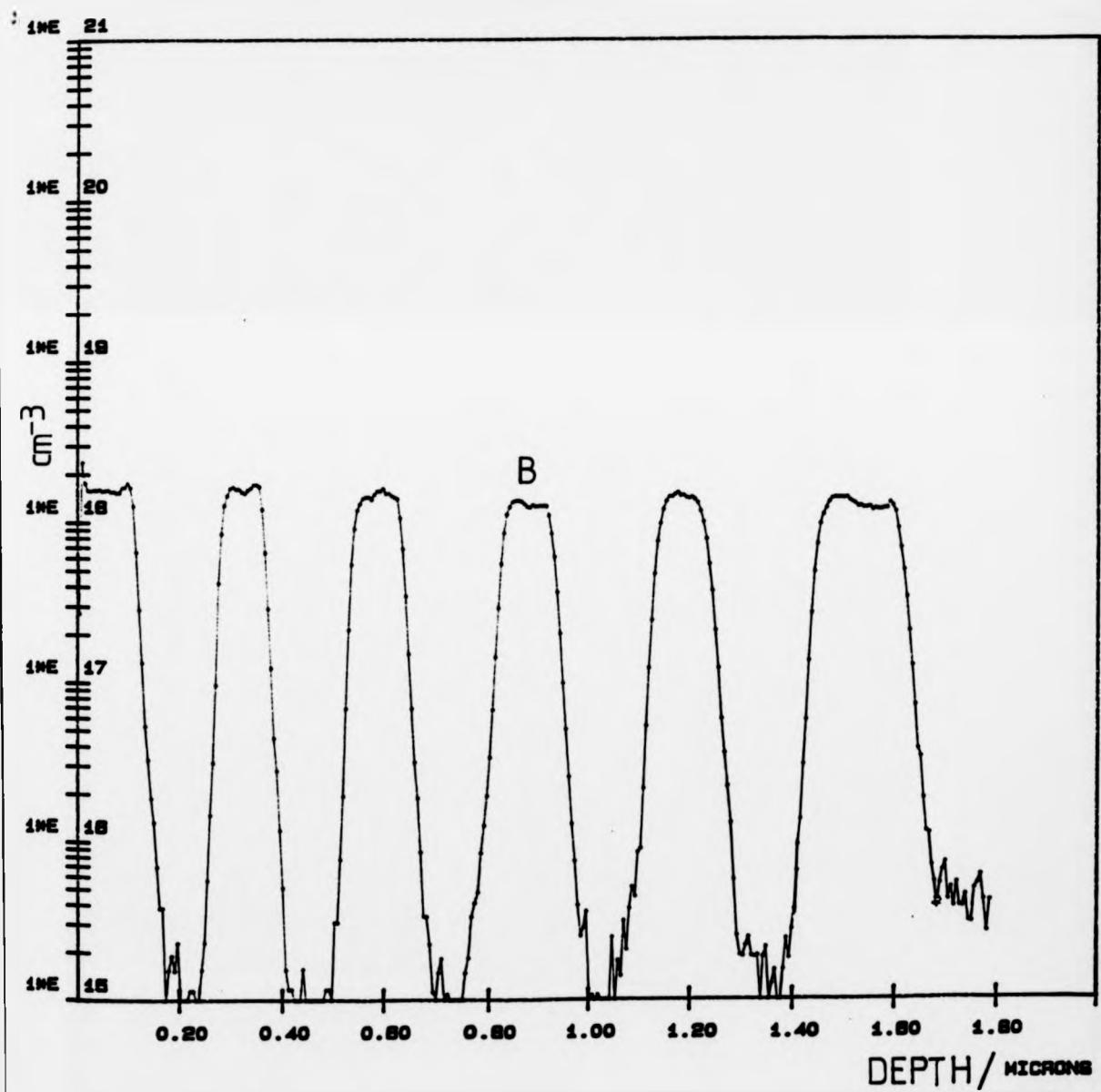


Fig. 6.17 RGAs showing out-gassing of graphite B cell after having been held at stated temperatures for 5 minutes. The hydro carbons rapidly disappeared on reaching 1400°C.

Fig. 6.18 SIMS profile showing an epilayer containing abrupt transitions and wide dynamic range, doped using the graphite cell for boron effusion.



the flux, so frequent exhaustion and consequent recharging of the cell does not occur.

This new design of B cell was found to overcome the inherent problems of elemental B doping, providing a responsive and durable source. It has been used by the author to grow pioneering delta-doped [i.e. a single atomic layer of doped material] epilayers, as will be discussed in the following chapter.

#### 6.5 Summary.

This chapter has dealt with the effective coevaporation of the two main p-type dopants in Si-MBE. A new theory has been proposed, attempting to explain the effects of PED by ion damage and consequent vacancy formation, allowing preferential dopant incorporation from the adlayer. This hypothesis seems more physically realistic than that of secondary implantation.

Ga, the more commonly used p-type dopant has limitations due its low solid solubility limit and its tendency to surface segregate during growth. The advantage of Ga, and the reason why it has become so widely used, is its ease of evaporation due to convenient vapour pressure. The nature of coevaporated boron is, however, in contrast with this. Its electrical and kinetic properties are excellent: complete activation, bulk-like mobility and unity sticking coefficient.

However, its low vapour pressure means that care is required in the design and construction of a source cell able to provide a pure dopant flux, and not to cause any degradation of the UHV environment within the MBE system. Such a cell has been shown here and its stability and reliability have been demonstrated.

## Chapter 7. Boron delta-doping in Si-MBE.

### 7.1 Introduction.

One of the reasons for developing the graphite B cell was for the fabrication of 'delta-doped' layers, ideally containing just a single atomic plane of highly doped material. In practice, the dopant spike extends over several atomic planes. The high levels of controllability and reproducibility of the cell, coupled with the properties of B as a dopant (unity sticking coefficient, high solid solubility limit, no surface segregation) form a near ideal combination for the production of these sharp spikes.

Delta-doped layers are currently of major interest due to the novel electronic properties which have been attributed to them theoretically. It has been proposed <Dohler, 1978> that a 2-D carrier gas occurs within the V-shaped quantum well produced by the extremely narrow dopant spike. If the delta-layer is of the opposite carrier type to the bulk of the material, the layer causes a strong space charge region. This confines carrier movement, and a 2-D gas results due to the quantisation of the motion of the carriers perpendicular to the layer. This situation is similar to that present in the space charge region of an MOS structure, but without an interface region. Such an interface may not be ideally abrupt, can act as a scattering centre <Hartstein et al, 1976>, and possible strain in the layer may cause fluctuations in potential. Apart from these practical considerations, the delta-doped system is much easier to model theoretically due

to its simplicity; there are no interfaces, no matrix mismatch and no change in dielectric properties, all of which occur at the Si/SiO<sub>2</sub> interface in a conventional MOS structure. These factors make delta doping an interesting research tool for investigation of phenomena such as the 2-D metal insulator transition <Dohler, 1978>, as well as device applications such as delta-doped MOSFETs.

MBE provides the only viable technique currently available for the fabrication of delta-doped material, because of the precise temporal and spacial dopant control which can be achieved. However, even the normal growth methods employed in MBE produce some broadening of dopant profiles, and so alterations to the standard technique have had to be developed to overcome its short-comings. The first delta-doped layers in Si were grown using solid phase epitaxy <Zeindl, 1987>, with Sb as the dopant. For this, a p-type (Ga) region was grown in the normal way. Growth was then stopped, the substrate cooled to room temperature, and a known surface coverage of Sb was deposited. (The substrate was kept at room temperature to prevent desorption of Sb from the Si surface during this stage.) This was then covered with 20-30Å of amorphous Si, which was subsequently recrystallised at 700°C, and the final p-type layer deposited in the conventional way.

This method has several drawbacks, however. Firstly the substrate was cooled before the dopant deposition, and not reheated until after the growth of the amorphous Si layer. It is known that at temperatures below 400°C hydrocarbons

are adsorbed onto the Si surface (see section 5.3.1), and these would be trapped by the amorphous layer. The second disadvantage of this method is the use of recrystallisation, which can yield material of relatively poor crystallinity (see section 6.1) <Ahlers et al, 1988>. Also the recrystallisation stage requires the substrate to be held at high temperature without deposition occurring, a situation which has been shown to enhance incorporation of C. The high doping levels required are above the solid solubility of Sb in Si at these temperatures, and therefore complete ionisation of the dopant layer during the recrystallisation stage has been difficult to achieve, especially at high surface concentrations <van Gorkum et al, 1989>

To overcome these problems, the author devised a novel technique of delta-layer growth, using elemental B as the dopant source. B has the advantages of having a unity sticking coefficient <Kubiak et al, 1985>, so that cooling to room temperature could be avoided, and having a solid solubility an order of magnitude higher than Sb at 700°C. However, the drawback with B is that it can diffuse through Si at an appreciable rate (up to several monolayers a minute at  $T_g > 700^\circ\text{C}$ ) <McPhail et al, 1988, Vick & Whittle, 1969>, so the thermal budget must be minimised during and after deposition, but without compromising material quality.

B delta doping has previously been tried unsuccessfully by Tatsumi et al <1988>, using an HBO<sub>2</sub> source. They found that the spike became smeared, and only 70% activation could be achieved. This smearing was attributed to surface

segregation of the B layer during the final stage of growth. This is in agreement with work by Tuppen et al <1988> who also noted the existence of surface segregation during doping with a compound B source. Since all the layers grown by Tatsumi et al were at substrate temperatures between 700 and 850°C, solid state diffusion of the B would also have occurred. Their measurements of broadening were stated values made by Auger electron spectroscopy, and no information on profile symmetry was given- surface segregation naturally gives a strongly asymmetrical profile- so the magnitude of each effect cannot be ascertained.

The fact that only 70% activation of the delta-layer was achieved, is also in agreement with the work of Tuppen et al, who could only achieve a maximum carrier concentration of  $9 \times 10^{19} \text{ cm}^{-3}$  at  $T_s=850^\circ\text{C}$ , even with a B concentration of  $4 \times 10^{20} \text{ cm}^{-3}$ . Elemental B doping has achieved carrier concentrations of  $3 \times 10^{20} \text{ cm}^{-3}$  and 100% activation at these temperatures <Kubiak et al, 1985>. The difference seems to be due to surface clustering of B atoms at high  $T_s$  when using compound sources. This is not caused by inadequate surface decomposition of the molecules at such temperatures, since it has been seen by SIMS that under such conditions O incorporation is negligible, although it increases rapidly below 700°C <Tuppen et al, 1988>.

The lack of activation is surprising, since intuitively it would be this regime which was closest to the situation during elemental B doping, in which 100% activation can be achieved. Fewer O atoms are present on the surface or

incorporating into the lattice than at low  $T_g$ , so their effect on B incorporation should be smaller. The author suggests that a possible reason for this is that the  $B_2$  species results after dissociation, and that this is directly incorporated or that the two B atoms are incorporated on adjacent lattice sites, either of which could result in an inactive complex.

### **7.2 Factors affecting the growth parameters for delta layers.**

As has been stated previously, the main objectives in growing a delta-doped layer from an elemental B source are:

- i) incorporation of correct areal density of B
- ii) high spatial resolution of B
- iii) minimisation of thermal budget during and after deposition of the delta
- iv) maximisation of activation
- v) maximisation of crystalline perfection

Unfortunately some of these are competing processes (e.g. i and iii are best performed by growth interruption which may compromise v (see section 5.3.1), and achieving iv and v must be to the detriment of iii), so an optimum situation must be established. Since the sticking coefficient of B in Si is unity, B does not desorb from the surface, so a low temperature amorphous cap and subsequent recrystallisation are not required, thus aiding the accomplishment of v above. This is a distinct advantage over the methods used for Sb delta doping.

Growth of such a thin, highly doped spike during normal epitaxial deposition is not feasible, even at the lowest achievable and controllable growth rates (.2A/s in the Warwick MBE system), due to cell reaction times and flux equilibration. It is therefore necessary to interrupt growth in order to deposit a selected surface coverage of B. In this way the dopant cell could be used at a relatively low temperature to increase the time required for this deposition, thus increasing the accuracy of the final surface coverage. This long evaporation time reduces errors in the calculated coverage due to equilibration times. This time was also chosen with consideration to the fact that minimisation of interrupt time was desirable.

Surface coverage and necessary evaporation times were calculated from the extensive calibration runs of epilayer doping, using the equation

$$\text{Surface coverage, } N_g = N_A r t \quad 7.1$$

where  $N_A$ =dopant conc. in calibration layer/cm<sup>-3</sup>  
 $r$ =growth rate of calibration layer/cm s<sup>-1</sup>  
 $t$ =dopant deposition time/s

Using a calibration curve such as that in Fig. 6.16, normalised to a growth rate of 5A/s, equation 7.1 becomes

$$N_g = 5.0 \times 10^{-8} \times N_A \times t \quad 7.2$$

Since, for B,  $N_A$  is independent of substrate temperature, the two parameters which govern the surface coverage during a growth interrupt are the source cell temperature and the exposure time.

To minimise solid state diffusion this interrupt needed to be carried out at a relatively low substrate temperature. A

low temperature was also desirable to minimise C uptake (see section 5.3.1), although it was necessary to keep it above 350°C to avoid hydrocarbon adsorption.

The minimum temperature required for full activation is difficult to ascertain due to the unique situation presented by this method of growth. Bulk activation after dopant implantation has been widely studied <see for example Hofker et al, 1975, Csepregi et al, 1978>, and is generally understood. This process, however, also involves recrystallisation of Si amorphised by the implantation, and involves a large spread of dopant relatively deep within the material. In the present case, the B starts as a surface layer, with a consequently higher diffusivity, which is being buried by an impinging flux. Under low surface concentration conditions ( $\sim 2 \times 10^{10} \text{ cm}^{-2}$  or less) it would be expected that incorporation at lattice sites, and hence activation, would be readily achievable at normal epitaxial growth temperatures ( $>500^\circ\text{C}$ ). However, in the highly saturated regime used for delta doping, with up to  $1 \times 10^{13} \text{ atoms cm}^{-2}$ , this would not be the case, as diffusion and solid solubility are too low.

It has been shown <Kubiak et al, 1985> that active B doping during MBE can exceed the solid solubility limit. However, the author experienced difficulty in high B doping at low substrate temperatures. Fig. 7.1a shows a B spike measured by SIMS of a layer grown at  $600^\circ\text{C}$ . A shoulder is clearly visible on the spike, and any B incorporated above the level of the shoulder was found to be inactive [c.f. eCV profile of the same layer in Fig. 7.1b]. The shoulder is broadened by

solid state diffusion during growth and device processing. The fact that the top, inactive portion of the spike does not diffuse suggests that the B has precipitated, and so has much less mobility within the lattice. This phenomenon was found to decrease at higher  $T_g$ , with full activation achievable above 650°C, at the maximum possible doping level of  $2 \times 10^{19} \text{ cm}^{-3}$  (during normal epitaxial growth). This temperature was therefore used as an empirical minimum for activation of the delta layer in this study.

After the deposition of the dopant layer, the final layer of Si could be laid down. During this process an increase in substrate temperature was required for high quality epitaxy, and activation of the dopant layer. Again, the thermal budget needed to be minimised during this stage to minimise diffusion. Fortunately this top layer needed to be only a few hundred angstroms thick, sufficient to remove the epilayer surface from the active region of the delta layer.

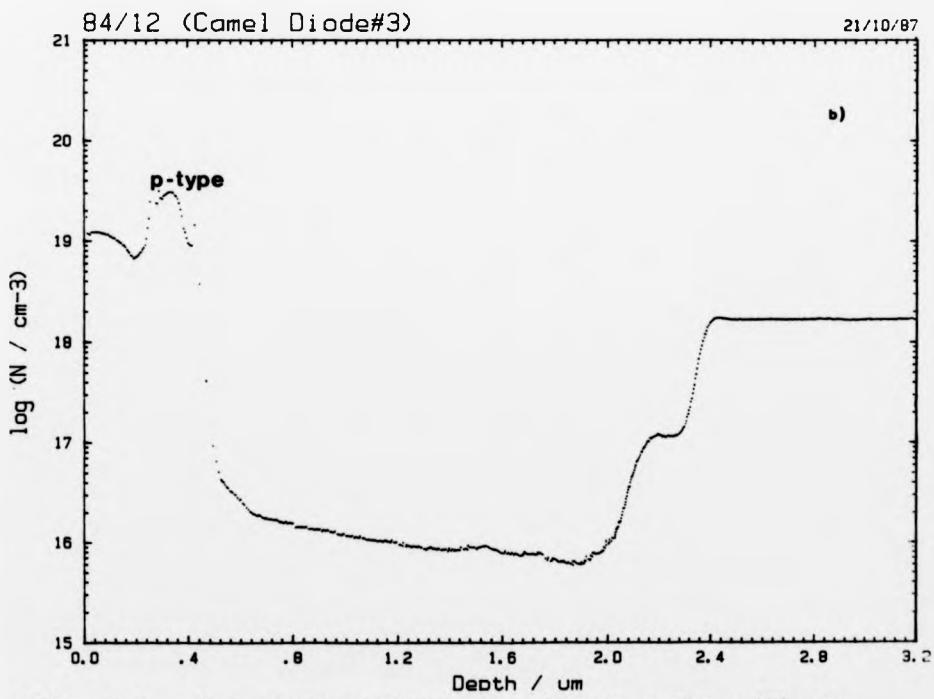
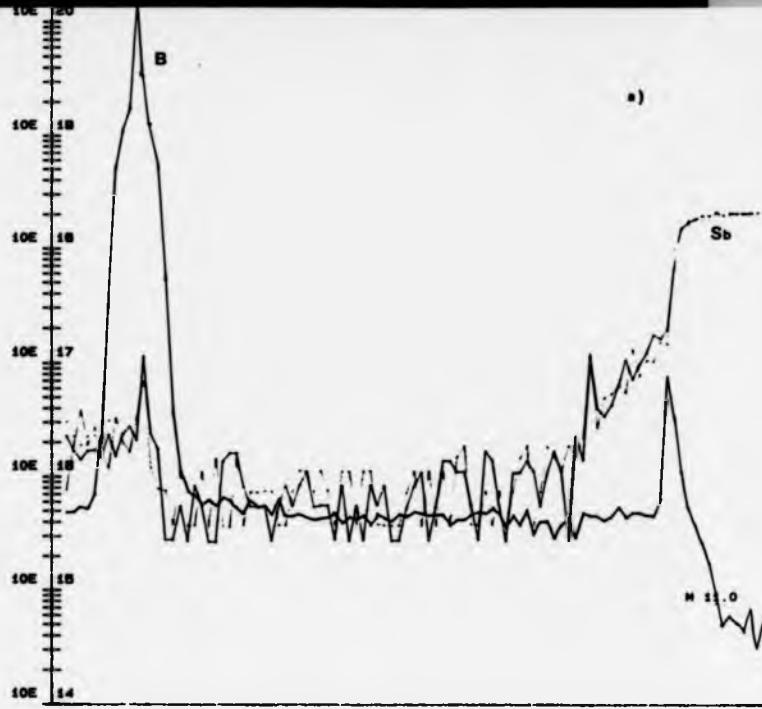


Fig. 7.1 a) A SIMS profile of a boron spike with an unintentional shoulder occurring at the solid solubility limit. b) is an ECV profile of the same layer, indicating that any boron above the solid solubility limit is electrically inactive. (SIMS carried out for the author by Loughborough Consultants)

### 7.3 Details of the chosen growth parameters.

Fig. 7.2 shows a schematic of the various stages involved in the growth of a delta-doped epilayer for fabrication, including the parameters selected by the author. P- (1-3 ohm-cm) backdamage substrates were used, and onto these a 0.3um buffer layer was grown with the same doping level as the substrate, to bury the interface from the active device region. Next the first low doped n-type (Sb) region was grown at 700°C, 5A/s. At this stage, prior to deposition of the delta layer, minimisation of the thermal budget was not necessary, and 700°C is an ideal temperature for Sb doping to minimise surface segregation. For this low level of doping PED was not necessary. After this, growth was interrupted by shuttering the e- gun, and the substrate was cooled to 400°C. The calculated surface coverage was then deposited at a given flux ( $N_s/t$ ). The flux chosen was, in most cases,  $4 \times 10^{10}$  atoms  $\text{cm}^{-2}\text{s}^{-1}$ . The surface coverages ranged between  $2 \times 10^{12}\text{cm}^{-2}$  and  $1 \times 10^{13}\text{cm}^{-2}$ , giving values of  $t$  between 40 and 240s. Finally  $T_g$  was increased to 700°C and the top layer of n- (Sb) Si was grown at 6.5A/s to a thickness of ~1000A. This was sufficient for full activation with minimal dopant diffusion. The thermal budget during device processing would be higher than that during growth <Mattey et al, 1989>, but it was the author's desire that the growth alone should provide a fully activated delta with minimal diffusion, so that factors

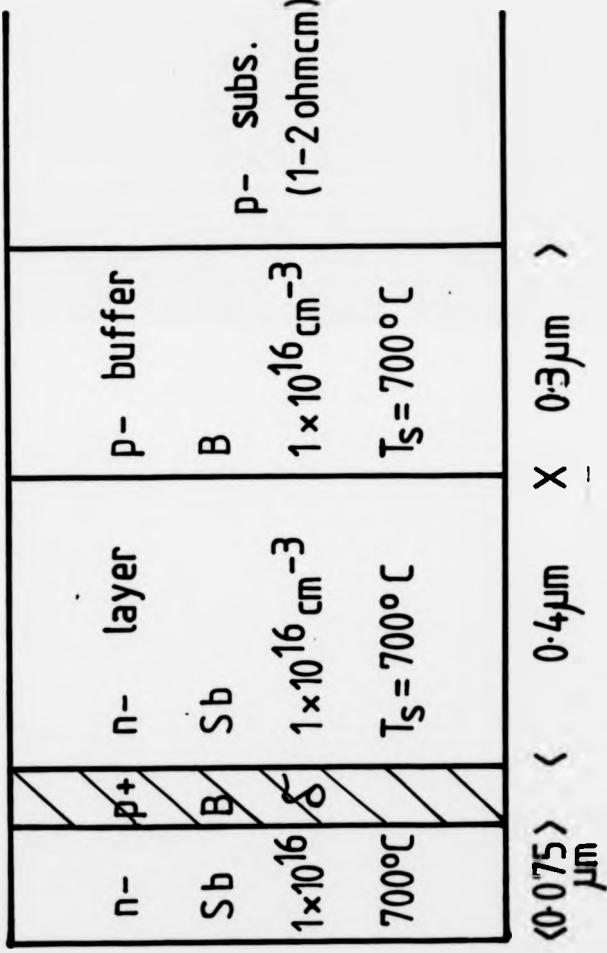


Fig. 7.2 A schematic diagram of the actual structure of a delta-doped structure grown during this study, including chosen growth parameters.

outside the grower's control did not need to be solely relied upon for correct functioning of the device.

#### 7.4 Diffusion of the delta during growth.

The expected diffusion profile due to the growth temperature for the constant total dopant level in the delta can be calculated using Fick's law, as in equation 7.3:

$$C(x,t) = \frac{C_0}{(Dt)} \cdot \exp \left( -\frac{x^2}{4Dt} \right) \quad 7.3$$

where D=diffusion coefficient of B in Si

There are few data available for the diffusion coefficient of B in Si at temperatures below 1000°C, and only one qualitative study has been made using MBE-grown Si <McPhail et al, 1988>, in which the author was involved.

Considerable effort has been expended to characterise and describe B diffusion behaviour at higher temperatures <see for example Kurtz and Yee, 1960 and Schwettman, 1974>. Often this was carried out in an oxidising atmosphere in which the oxygen gradient affects diffusion, which is not the case during MBE. Of more interest is work carried out in an inert atmosphere. Work by Vick and Whittle <1969> and Hofker et al. <1973> gave experimental data down to temperatures of 700°C and 800°C respectively, but all these authors were dealing with higher total concentrations than is the case for delta doping (usually with ion implantation doses of  $>10^{15} \text{cm}^{-2}$ ). Under such conditions diffusion becomes non-Fickian, i.e.

Fick's law is not obeyed, and the diffusion coefficient seemingly becomes dependent on dopant concentration. More recent work <Dominguez and Jaraiz, 1987> has described this non-Fickian regime and the transition to Fickian behaviour. They derived the same expression for the B diffusion coefficient under both conditions. The coefficient is therefore independent of concentration, although other factors become important at very high B levels, such as the formation of Si-B complexes. Agreement of this theoretical model with experimental data was excellent.

The expression for the diffusion coefficient of B in Si,  $D_B$ , derived by Dominguez and Jaraiz was

$$D_B = 2 \times 10^{-4} \exp[-2.30(eV)/kT].$$

For a temperature of 700°C this gives a value of  $D_B = 2.8 \times 10^{-16} \text{ cm}^2 \text{ s}^{-1}$ . It is this value of  $D_B$  that the author has chosen to use to model the expected diffusion profile of the delta layer. (It is interesting to note that this figure agrees well with simple extrapolation of the data of Kurtz and Yee <1960> rather than the complex mathematical methods of many authors in the interim.)

### 7.5 Results.

A SIMS profile of one of the delta layers grown by the author is shown in Fig. 7.3. This was the first working B delta-doped epilayer ever grown, and its electrical

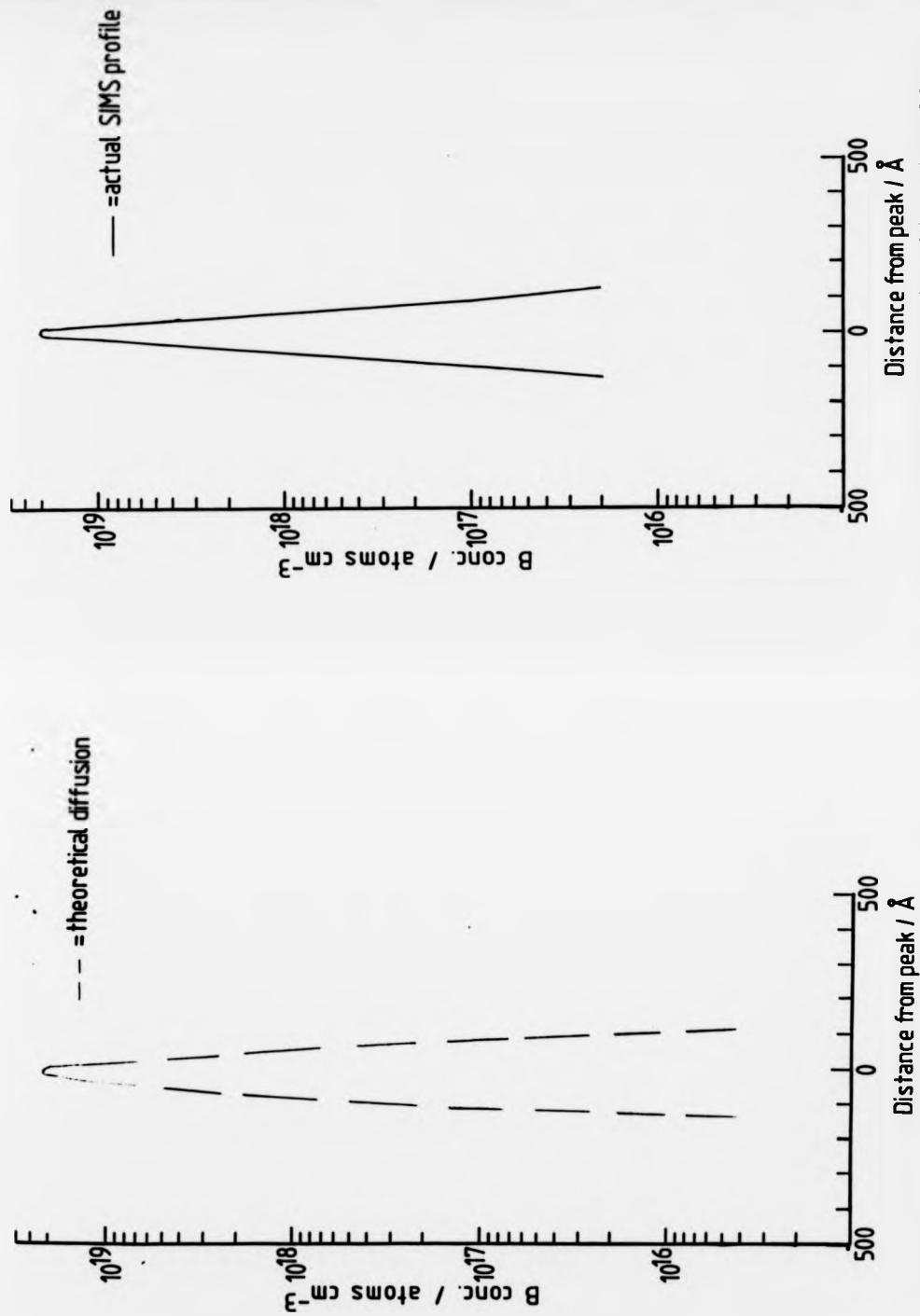


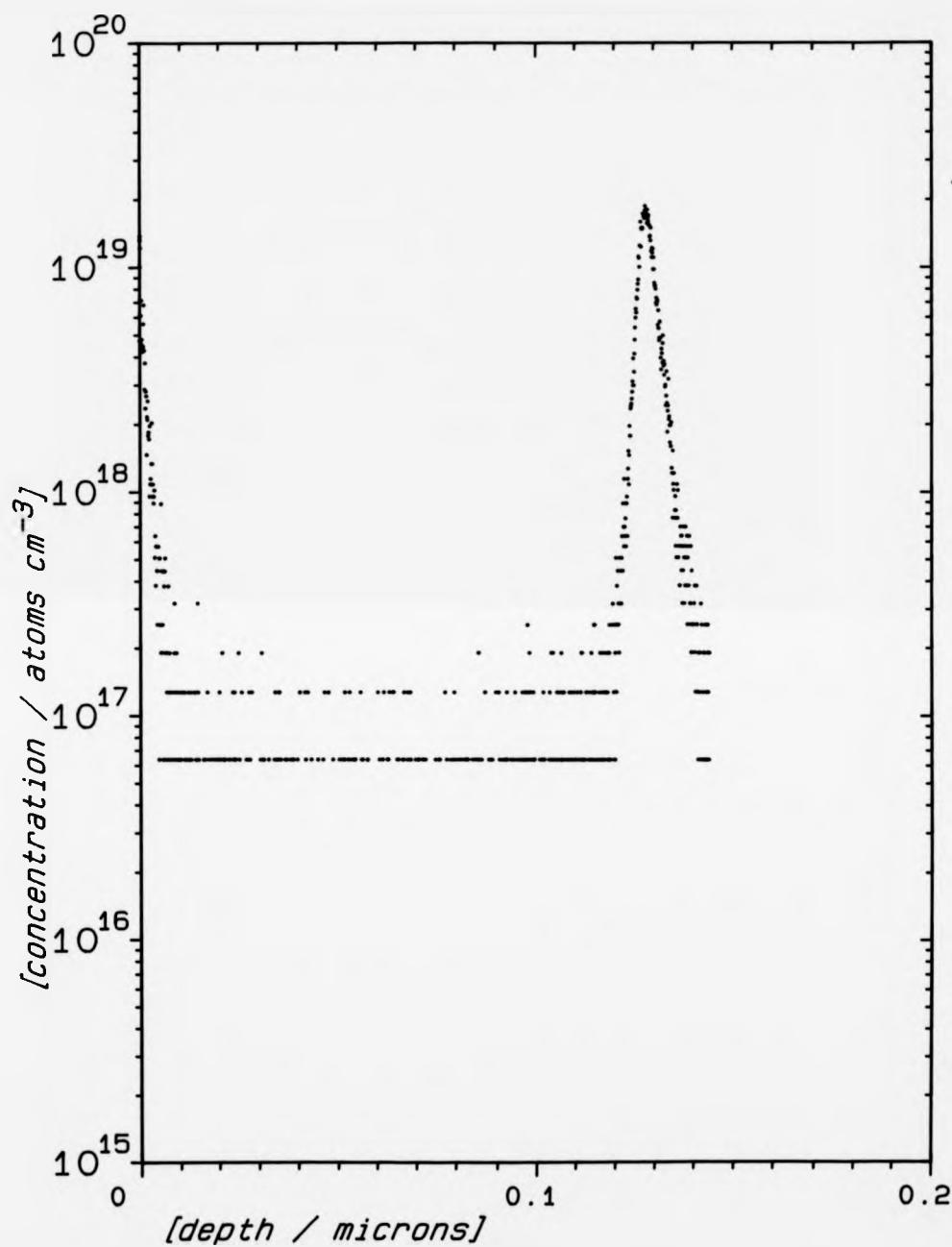
Fig. 7.3b Initial SIMS profile of a B delta. The profile is broadened by SIMS effects. (SIMS carried out for the author by Loughborough Consultants)

Fig. 7.3a Calculated diffusion profile of B delta.

properties have been rigorously studied, and are discussed elsewhere <Mattey et al, 1990>. The SIMS was carried out at a relatively high primary ion energy, and so resolution is compromised. However, this procedure showed the basic position of the delta, and software was able to integrate under the spike during analysis to give the total dopant level. This was found to be equivalent to  $9.7 \times 10^{12} \text{ cm}^{-2}$ , in excellent agreement with the expected surface coverage of  $1 \times 10^{13} \text{ cm}^{-2}$  as calculated by the author prior to growth.

Fig. 7.4 shows an extremely high resolution profile of the delta layer, showing a full-width-at-half-maximum [FWHM] of 35Å. The primary ion energy at the sample was only 0.45keV per O<sup>-</sup> ion, and the SIMS analysis itself was the product of much effort to advance the resolution of the technique <Mattey et al, 1990>. However, the delta was so abrupt that it was thought that the analysis was still causing discernable broadening of the actual dopant profile. Using data taken at a range of primary ion energies the FWHM was extrapolated to zero energy. This gave a FWHM of 27Å.

Due to the extreme abruptness of the doped layer, and the difficulty of contacting to it accurately, there are no electrical techniques that can be used to accurately analyse the material without it undergoing device processing. Electrical analysis by Hall measurements on the device-processed layer showed the total carrier concentration in the delta to be  $(9+/-2) \times 10^{12} \text{ cm}^{-2}$  (assuming a Hall scattering factor of unity, and that only one sub-band is occupied).



Boron delta 100/23 900eV impact

Fig. 7.4 High resolution SIMS profile of B delta, carried out using a primary ion energy of 0.45kV per oxygen ion. (SIMS carried out by Mark Dowsett, Warwick University)

This is in good agreement with the areal density determined by SIMS, indicating that complete activation was achieved.

The other technique used to give information on the as-grown layer was transmission electron microscopy [TEM].

Fig. 7.5 shows a TEM photomicrograph of a cross-section through a  $1 \times 10^{13} \text{ cm}^{-2}$  layer. The contrast is due to the effect of strain caused by the high B concentration. Measurement of this dark band gave an estimate of delta thickness of 20A. This photograph also shows the epilayer to be of high material quality both above and below the delta, since no defects were observable.

#### 7.6 Discussion.

Here we have been interested in the material properties of the layers grown. The methodology adopted achieved the incorporation of a very accurate amount of dopant with high spatial resolution, with a measured FWHM of between 20-30A. The crystalline quality of the material was also good; the density of dislocations seen was comparable to that seen in undoped material grown at a similar substrate temperature. The fact that the doping spike was so close to the surface meant that any defects nucleated there would only be seen as a surface texture after even a minimal defect etch <Archer, 1982>, rather than a quantifiable defect count, but such a texture was not observed. The TEM substantiates this, showing no visible dislocation network in the field of view,

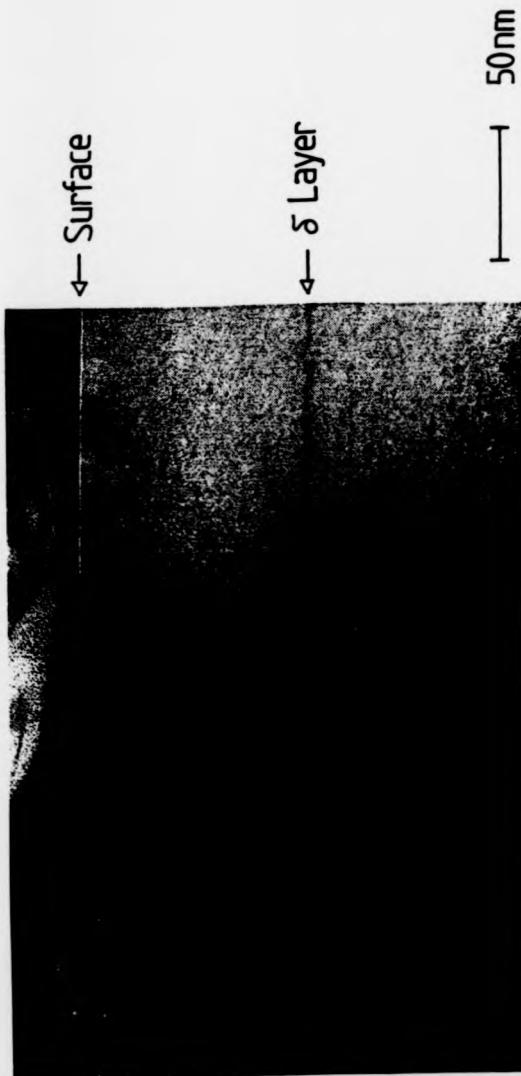


Fig. 7.5 Transmission electron photomicrograph of a boron delta layer, showing the width of the delta to be approximately 20A. (TEM carried out by J. Whitehurst, Oxford)

indicating an upper limit to the defect density of  $10^5 \text{ cm}^{-2}$  <Augustus, 1989>.

The other factor of interest is the broadening of the delta. Comparison of the expected profile due to diffusion during growth and the actual profile as determined by SIMS showed that the actual spike is slightly narrower than predicted. The basic shape of the measured profile is not in accordance with that expected from mere diffusion. A diffused profile is proportional to  $\exp(-x^2)$ , giving a rounded peak, whereas the SIMS profile was triangular, giving a sharply defined peak. Thus simply modifying the diffusion coefficient or diffusion time to give coincident peak height or FWHM would not yield a coincident curve. This implies that the SIMS analysis itself is affecting the shape of the measured spike.

As has been mentioned previously, some SIMS induced broadening was still thought to be occurring <Mattey et al, 1990>, even at the extremely low primary energies used [0.45kV per O<sup>-</sup> ion]. Further evidence for this was taken to be the asymmetric shape of the spike, with a less abrupt trailing edge than leading edge, characteristic of a SIMS artefact. It was thought to be due to the growth process, since the only other mechanism, apart from diffusion, that could affect the profile was dopant surface segregation. This would, however, degrade the abruptness of the SIMS leading edge rather than the trailing one. The author suggests that diffusion into the Si beneath the B adlayer would be expected to occur during the heating of the substrate prior to the growth of the final

1000A layer. This implies that SIMS distortion of the profile was less than was previously thought <Mattey et al, 1990>.

It was also implied that the SIMS profile contained no information on the actual peak shape, due to SIMS artefacts. The author believes, however, that the zero energy extrapolation does give qualitative information, since the asymmetry was to be expected due to the growth methodology.

### 7.7 Conclusion.

This work has resulted in the growth of the first successful B delta-doped Si. It was achieved by a novel growth methodology chosen by the author, involving no room temperature deposition stage, using a graphite B cell also designed by the author. The crystalline properties were good (dislocation count  $7 \times 10^4 \text{cm}^{-2}$  in the bulk of the epilayer), as was dopant activation, with a sheet density of  $(9+/-2) \times 10^{12} \text{cm}^{-2}$  (as determined by Hall measurements), compared with an areal dopant density of  $9.7 \times 10^{12} \text{cm}^{-2}$ . This areal density was within 3% of that intended. The extreme abruptness of the dopant spike made it difficult to analyse, but SIMS extrapolation gave a FWHM of 27A, and TEM a thickness of .20A. At the time of writing, these B doped deltas grown by the author are the only ones in existence.

## Chapter 8. Overview and further work.

The aim of the materials work in this study was to elucidate some of the problems inherent in state-of-the-art Si-MBE growth. Minimisation of crystalline defects has been achieved to an extent - the base level has been reduced from  $\sim 10^6 \text{ cm}^{-2}$  to  $\sim 10^3 \text{ cm}^{-2}$ . It has not been found possible to reduce the count below this figure by *ex-situ* or *in-situ* substrate preparation. This would seem to imply that the growth regime used in this study does itself induce dislocations. Vacuum quality is certainly the next area to examine, since it is well known that high partial pressures of certain gases are detrimental to material quality <Kasper & Kibbel, 1983>. Residual gas interactions need to be carefully studied. Reduction of residuals is not easy, as the base RGA is defined by the pumping system; the best alternative is controlled leak-in of certain gases known to be present, such as H, He, N<sub>2</sub>, CO, CO<sub>2</sub>, and O<sub>2</sub>, and examination of their effects. The presence of dislocations can be used to advantage, however, since their gettering properties may be utilised to remove electrically active impurities from the epilayer.

The importance of substrate temperature has been investigated to try to find an optimum region for growth. Unfortunately there are several different aspects of material quality that are influenced in different ways. Firstly, doping requires low T<sub>s</sub> to minimise B diffusion, but higher temperatures to prevent profile smearing and to allow high B

doping, since solid solubility is strongly temperature dependent. This study has also revealed some less obvious effects. Crystalline quality improves at low temperature, dislocation levels falling by more than an order of magnitude between 700 and 525°C. Conversely, deep level traps increase as  $T_g$  decreases, 600°C being a critical temperature above which trap levels fall to a minimum. (The presence of these traps is *per se* a problem which must be tackled. If they are due to impurities, Ta being the most likely culprit for at least one of the traps present, the source must be eliminated. The other deep levels seem more related to the growth process itself, and their exact cause needs further careful analysis; their dependence on other growth parameters such as growth rate and vacuum quality is important, to complement the temperature data collected here.) It is probable that these two factors are related. Dislocations which have been found to nucleate in greater concentrations at high growth temperatures, presumably due to increased C incorporation during the first few hundred angstroms of growth, may act as gettering sites for impurities. These can serve to affect the number of electrically active traps in the material.

It may be the case that the highest quality epilayers require several temperature changes during growth to ensure optimum parameters for different regions within the layers. This will be especially true for SiGe work which has the additional factor of critical thickness dependence on temperature.

An interesting conclusion can be drawn from the fact that the dislocation density is a function of growth temperature,  $T_g$ , but not a function of epilayer thickness. Since the method used for all layers was to initiate growth at a standard temperature then lower it to that desired for growth, for  $T_g$  to play a role in defect formation they must be nucleated during the early stages of growth rather than at the interface. Since thickness had a negligible effect on dislocation density, nucleation was obviously not occurring at a uniform rate throughout the epilayer. It seems likely that the vast majority of dislocations form in the first few hundred angstroms of the layer. This would explain why even the most effective substrate preparation prior to growth did not reduce dislocations below a base level of  $\sim 10^3 \text{ cm}^{-2}$ . This is a period that has been shown by laser light scattering to be when the rough Si surface is undergoing a smoothing process. Further investigation of this region of growth is essential if material quality is to be further improved.

The causes of residual doping in the system have been positively identified, the normal base level being due to phosphorus from stainless steel. The minimum level of  $10^{14} \text{ cm}^{-3}$  may be difficult to better, as the stainless steel source is an integral part of the system, with no obvious replacement, although improved shielding of the inside of the chamber may have an effect. Adequate cooling has been shown to be essential.

The other problem addressed in this work was the search for a more ideal p-type dopant source. The use of Sb

and PED provides precise profile control over a wide dynamic range, with convenient coevaporation properties, and has proved a near ideal n-type dopant. The mechanism of PED is still not fully understood; the proposed mechanism of direct secondary implantation seems physically improbable. A better explanation may be provided by the damage caused by the impinging ions providing preferential incorporation sites, as proposed here. The properties of traditional p-type dopant in Si-MBE, Ga, have been studied in this work, and the deficiencies noted. Low solid solubility limit, low sticking coefficient and surface segregation all limit its usefulness. A new B source has been demonstrated, B having far more desirable properties apart from its vapour pressure. Doping levels of up to  $10^{19}\text{cm}^{-3}$  have been achieved with sharp transitions.

It is hoped that the knowledge gained through this study will have aided the future growth of production quality epitaxial Si, allowing the fabrication of novel devices that will be of interest to both the physicist and the electronic engineer.

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## Appendix: Analysis techniques.

### 1 Deep Level Transient Spectroscopy (DLTS).

DLTS is a technique used to detect deep level electrical traps <Sandhu et al, 1985>. It involves pulse-biasing a Schottky barrier (usually to zero from a negative potential), to fill the mid-gap states, and then examining the capacitance transient.

The capacitance of a Schottky barrier is given by

$$C = \frac{AE}{w_D} = \left[ \frac{A^2 q E}{2(V_{bi} - V)} (N_D - N_A) \right]^{\frac{1}{2}} \quad (1.1)$$

where  $A$  = area

$E$  = permittivity

$w_D$  = depletion width

$q$  = electronic charge

$V_{bi}$  = built in voltage

$V$  = applied voltage

$(N_D - N_A)$  = net ionised impurity concentration

The traps will contribute their own component,  $\hat{C}$ , to the capacitance. So for  $N_T$  traps, where  $N_T \ll N_D - N_A$ ,

$$\frac{\hat{C}}{C} = \frac{N_T}{2(N_D - N_A)} \quad (1.2)$$

The capacitance transient due to pulse filling of the traps is sampled at two points in time,  $t_1$  and  $t_2$ , after the pulse, and the change in capacitance,  $\hat{C}_{t1} - \hat{C}_{t2}$ , is plotted against temperature. This gives useful information since the electron emission rate,  $e_n$ , is given by

$$e_n = \frac{1}{T} = A_n \exp -\frac{E_T}{kT} \quad (1.3)$$

where  $A_n$  = constant

$T_c$  = time constant

$E_T$  = trap energy

$k$  = Boltzmann's constant

$T$  = absolute temperature

and is strongly temperature dependent. If this emission rate is very fast all emission will occur before  $t_1$ , and thus  $^C_{t1} - ^C_{t2} = 0$ . Also if the rate is very slow there will be negligible difference between  $^C_{t1}$  and  $^C_{t2}$ . Between these two extremes there will be a temperature at which  $^C_{t1} - ^C_{t2}$  will be a maximum, and this will occur when the emission rate equals the time constant of the system, i.e.

$$e_n = \frac{\ln(t_1 - t_2)}{(t_1 - t_2)} \quad (1.4)$$

The temperature at which this occurs will be characteristic of the trap causing the transient.

Activation energies,  $E_A$ , for the traps can be calculated by temperature scanning for various 'rate windows', i.e. different values of  $t_1$  and  $t_2$ . This gives a series of values of  $e_n$  and  $T$ . From an Arrhenius plot of these,  $E_A$  can be calculated (see eqn. 1.3). The value of  $E_A$  is then compared with previously identified trap data to try to establish the nature of the traps present.

## 2 Electrochemical Capacitance-Voltage Measurements eCV.

Conventional CV profiling relies on the fact that a reverse biased Schottky barrier exhibits a capacitance change dependent on the carrier concentration at the depletion edge, caused by the bias potential, according to the equation

$$\frac{d(1/C^2)}{dV} = \frac{2}{qEnA^2} \quad (1.5)$$

where  $n = [N_D - N_A]$

and the depletion width,  $w_D$ , is given by

$$w_D = \frac{AE}{C} \quad (1.6)$$

So sweeping the bias potential, thus changing  $w_D$ , gives a depth profile of carrier concentration.

This technique has a limited depth range since avalanche breakdown of the Schottky barrier will occur when the field reaches a certain value, dependent on doping level. To overcome this problem, electrochemical CV profiling involves the use of an electrolyte to replace the metal side of the Schottky barrier. This electrolyte is also used to etch through the sample, taking off a precisely known thickness of material under certain bias conditions, so that another CV measurement can be made. By successive measurement and dissolution, a depth profile can be obtained.

This is carried out in practice by forming a Schottky barrier between the Si sample and an electrolyte of 1M NaF/0.05M H<sub>2</sub>SO<sub>4</sub>, the area of which is precisely defined by a PVC sealing ring. The capacitance measurement is made via a

Pt cathode passing an AC signal, whilst dissolution current is supplied from a carbon cathode with a DC voltage. The sample is biased using a saturated calomel electrode (SCE).

The profiler actually measures the doping level by examining the effect of modulating the depletion width <Ambridge and Faktor, 1975>. Equations 1.5 and 1.6 can be combined to give the relation

$$n = \frac{2E}{q} \frac{dV}{d(w^2)} \quad (1.7)$$

The depletion width is modulated by a 30kHz signal on a 3kHz carrier giving measurements of C and dC. The total depth at which the carrier concentration is measured is found by adding the depletion width,  $w_D$ , to the depth of material removed,  $w_R$ , the latter being determined from the dissolution current via the relation

$$w_R = \frac{M}{NFDA} \int I dt \quad (1.8)$$

where M = molecular weight of sample

N = valence number

F = Faraday number

D = density

A = sample area

This allows a plot of n vs. thickness to be plotted. An explanation of the system used to carry out the measurements has been given by Ambridge and Faktor <1975>.

Although the technique of eCV profiling is useful and accurate for most doping profiles, it does have its limitations.

Firstly, the upper doping level at which the profiler can operate is determined by the level at which avalanche breakdown of the Schottky barrier occurs due to the applied measuring voltage <Ambridge and Faktor, 1975>. In practice, this occurs at about  $2\text{-}3 \times 10^{19}\text{cm}^{-3}$ . The lower measureable limit is due to the fact that the CV characteristic is taken when the conductance is at its lowest point, and relatively independent of voltage. For low-doped samples this occurs at high measuring biases, and this can lead to high leakage currents and causes poor depth resolution.

### 3 Photoluminescence.

The principle involved in PL analysis is that if energy is given to a sample by irradiation with light, the absorption of photons causes the generation of electron-hole pairs. Some of these excitons will subsequently undergo radiative recombination (most, ~99%, will recombine via a competing, non-radiative path, such as the Auger process), emitting light of a characteristic wavelength. There are several recombination transitions observed by PL, which are illustrated in Fig. A1.1. These show that luminescence can be caused by dopants and by deep level states. Any energy level within the bandgap can act as a trap, and thus as a recombination/generation centre. Si is an indirect bandgap

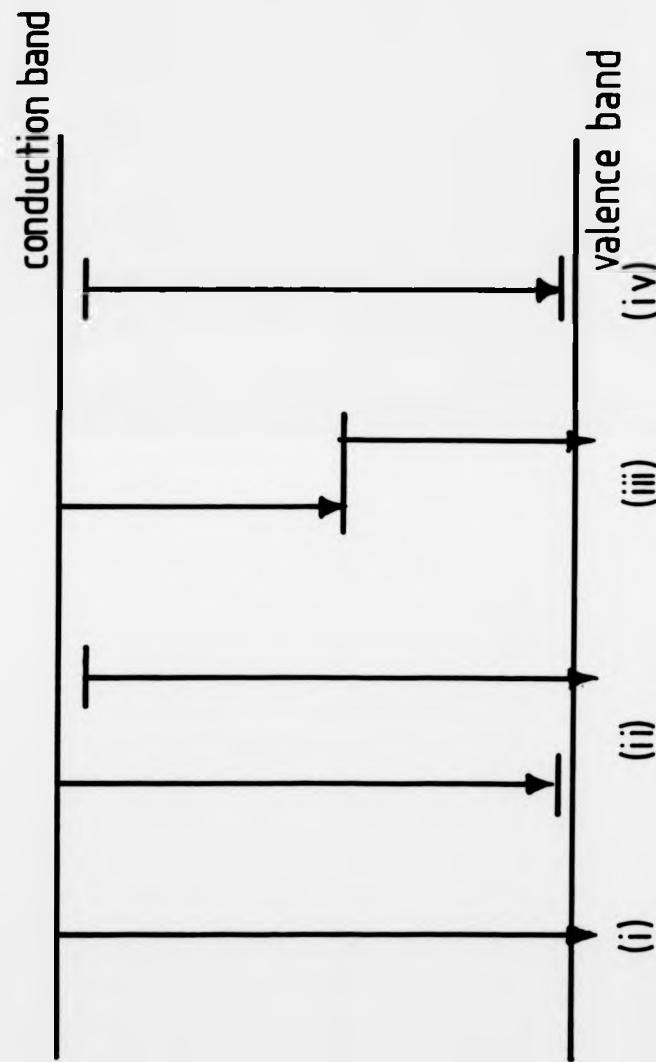


Fig. A.1 Schematic diagram showing the possible transitions that can occur to cause luminescence. (i) interband, (ii) shallow levels (dopants), (iii) deep levels (other impurities), (iv) impurity to impurity (bound to bound).

material, so although a deep impurity can cause a direct radiative transition due to the large number of possible values of its wavefunction, levels nearer the band edges require a momentum change to allow radiative emission. This momentum change is usually supplied by interaction with a phonon; at the low temperatures required for PL few phonons are available for absorption, so the change is usually by phonon emission. This must allow the correct momentum change, the highest probability being for transverse-optical and -acoustic phonons. The energy of the emitted photon will therefore be <Sze, 1981>,

$$hv = E_1 - E_2 - E_p \quad (1.9)$$

where  $h$  = Planck's constant

$v$  = photon frequency

$E_1$  = initial energy level

$E_2$  = final energy level

$E_p$  = phonon energy

By measuring the emission intensity over a range of wavelengths, a spectrum can be obtained with varying intensity peaks at various wavelengths. These can then be compared to known transitions, and the centres present determined. Because the luminescence efficiency of some transitions is greater than others, and surface effects have a strong influence on luminescence, the data is mainly qualitative in nature.

The technique is performed in practice by irradiating the sample with a laser <Robbins et al, 1985>. The sample is held at liquid helium temperature [4.2K] so that nearly all

carriers are in the ground state, and to prevent any thermal non-radiative processes. This also prevents thermal broadening of the emission peaks. Luminescence is then detected by a monochromator/Ge detector or photomultiplier.

Whilst PL is a well established technique for the study of bulk Si, for analysis of epilayers there are several problems that have to be overcome. As has already been stated, surfaces cause differential non-radiative effects <Hamilton et al, 1988>. This is also true of interfaces and defects, which means that MBE material has highly variable luminescent properties. Penetration of photons through the epilayer to the substrate means less excitation of the epilayer, increased contribution from the substrate, and more interface effects. Similar effects occur if exciton diffusion occurs to such an extent that recombination occurs in the substrate. It is also important to be able to distinguish between substrate and epilayer luminescence. In the present studies these problems were minimised by growing relatively thick epilayers (>5um) onto substrates of the opposite carrier type to the epilayer.

#### 4 Secondary Ion Mass Spectrometry (SIMS).

SIMS is a destructive analysis technique in which monoenergetic, mass-filtered primary ions are scanned across the sample surface to sputter away the surface material <Sykes, 1987>. A small percentage of the resultant sputter yield will be ionised, and this is collected, mass-filtered and

analysed by a magnetic sector or quadrupole mass spectrometer. The number of counts for selected masses, relative to a matrix signal, is measured, and as the sample is continuously being eroded a depth profile is constructed.

Once the raw data has been collected as ion counts against time, a calibrated impurity concentration profile is obtained by analysing an ion implanted standard containing a known dose of the impurity required in the same matrix as the sample. Depth calibration is performed by measuring the crater depth with a surface profilometer.

There are several factors that affect the accuracy of the results obtained. Firstly there are crater edge effects; since the edge of the scanned area may influence the overall secondary ion count from the crater as a whole, the gated area, i.e. the area from which the secondary ions are collected, is much smaller than the actual crater. Secondly there is atomic mixing in which a profile may be broadened due to interaction between the energetic primary beam and an impurity layer in the sample. Further distortions may occur due to segregation of atoms at the interface between the ion damaged and bulk regions, the presence of an uneven crater bottom, and instrumental drift.

The analyses for this study were carried out in two machines, EVA 2000, a quadrupole instrument at Warwick, and a Cameca 3F, a magnetic sector system at Loughborough Consultants. Each machine had its advantages, EVA 2000 being useful for high resolution work for thin structures ( $O_2^+$  primary source) and the Cameca having the advantage of the

option of a Cs<sup>+</sup> source for profiling for oxygen, carbon and phosphorus.

### 5 Defect etching.

Another routine characterisation technique used on nearly all layers was preferential defect etching. This involved the immersion of a clean sample in an etchant that preferentially attacks the strain areas caused by crystalline defects. Once revealed in this manner the defects could be counted using an optical interference microscope. The optimum etch for <100> epitaxial Si has been found to be a diluted form of Schimmel etch <Schimmel, 1979>. This has been chosen since it has a relatively slow etch rate (-0.5um/min, dependent on carrier concentration), which allows a precise amount of material to be removed, preventing total removal of thin epilayers. It also produces a smooth etch surface, permitting even shallow defects to be clearly revealed.

It was found that ideally half to two thirds (up to 2um) of the epilayer should be removed for optimum defect clarity. Removal of more material did not improve etch features, but rather made them over-etch and become indistinct.

The etching was carried out by placing a solvent cleaned sample (hot methanol, 2 minutes) in a PTFE beaker and covering it with ~20ml (~1cm deep) of etchant. It was then agitated to prevent formation of bubbles on the sample surface, and once the required amount of material had been

removed, the beaker was flushed with copious quantities of DI water to terminate the reaction. The samples were then viewed on either a 100-1000 $\times$  Olympus microscope, or a Reichart-Jung Polymet 100-3000 $\times$  microscope, both of which were equipped with Nomarski interference optics. By counting defects within a known area of view, their density was calculated. Fifteen points on each sample, which included a complete centre to edge portion of the wafer, were counted to give a density distribution.

#### 6 Hall measurements.

This technique makes use of the fact that if a magnetic field,  $B$ , is applied to a conducting sample, the carriers are deflected in a direction perpendicular to that field. This sets up an electric field,  $E_H$ , perpendicular to  $B$  (see Fig. A1.2). At equilibrium, the force on the carrier due to the magnetic and electric fields will balance out, i.e.

$$E_H e = Bev \quad (1.10)$$

where  $e$  = electronic charge

$v$  = carrier velocity

The current density,  $J_x$ , can be written as

$$J_x = nev$$

$$v = \frac{J_x}{ne} \quad (1.11)$$

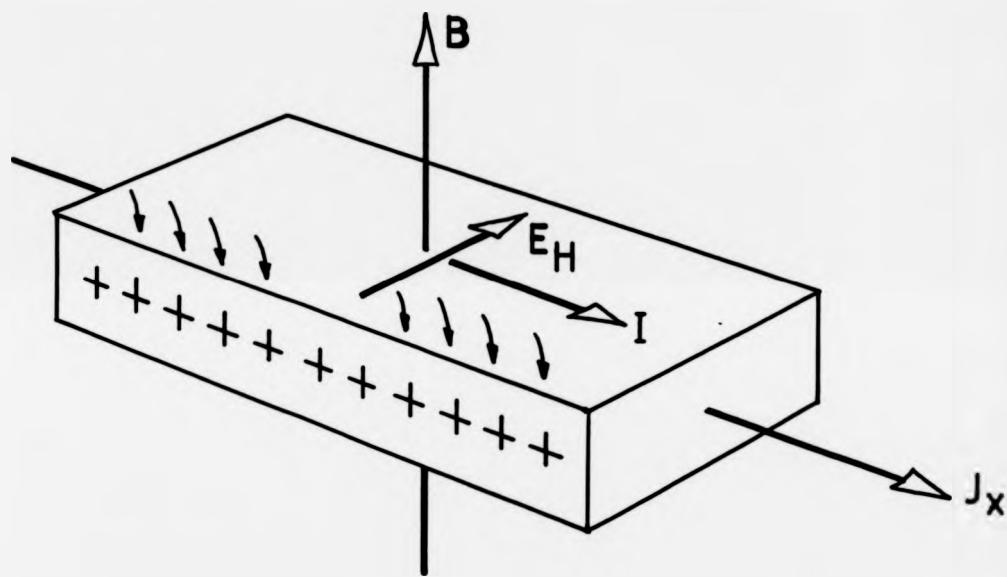


Fig. A.2 Schematic arrangement of the Hall effect, illustrating the deflection of holes, and the consequent electric field,  $\mathbf{E}_H$ , set up when a sample is placed in a magnetic field,  $\mathbf{B}$ .

Combining equations (10) and (11) gives

$$\frac{E_H}{BJ_x} = \frac{1}{ne} \quad (1.12)$$

$E_H/[BJ_x]$  will be a constant for a given temperature, and is defined as the Hall coefficient,  $R_H$ .

The carrier velocity,  $v$ , varies with carrier concentration and type, so equation (1.12) is more correctly written as

$$R_H = \frac{r}{ne}$$

where  $r$  is the Hall scattering factor

For most purposes,  $r$  is taken as unity, although theoretical calculations show that it can vary between 0.8 and 2, dependent on doping <del Alamo & Swanson, 1984>.

During actual Hall measurements, the voltage,  $V_H$ , set up across the sample, and the current,  $I$ , passed through it are measured since

$$\frac{E_H}{J_x} = \frac{V_H}{I} \quad t$$

where  $t$  = sample thickness

The sign of  $V_H$ , and hence  $R_H$ , is dependent on the type of carrier present, so by finding  $R_H$  both the carrier type and concentration can easily be calculated. For measurements on epilayers, the Hall cross configuration, as proposed by van der Pauw (1958), was used. This involved masking a cross on the epilayer with wax, and etching the exposed area with CP4A etchant (5HNO<sub>3</sub>:3Acetic acid:3HF)

well into the substrate. The four contacts were made using Ga/In eutectic and a gold pad, clamped in phosphor-bronze terminals. This was then placed in the field produced by a 0.52 Tesla magnet. Samples for static 77K measurements were simply immersed in liquid nitrogen. Temperature dependence runs were made in a purpose built cryostat < Biswas, 1990 >.

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The growth and  
evaluation  
of epilayers grown

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Beam Epitaxy.

AUTHOR ... Richard F. Houghton

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