Materials Science in Semiconductor Processing 122 (2021) 105527

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Full length article

The improvement of atomic layer deposited SiO_2/4H-SiC interfaces via a high temperature forming gas anneal

A.B. Renz *, O.J. Vavasour, P.M. Gammon, F. Li, T. Dai, M. Antoniou, G.W.C. Baker, E. Bashar, N.E. Grant, J.D. Murphy, P.A. Mawby, V.A. Shah

School of Engineering, University of Warwick, Coventry, CV4 7 AL, UK

ARTICLE INFO

Keywords:
4H-siC
SiO_2/4H-siC interface
Atomic layer deposition
Forming gas anneal

ABSTRACT

This letter reports on the improvement of a SiO_2 layer formed by atomic layer deposition on 4H-SiC, using a post-deposition anneal in forming gas ambient. Capacitance–voltage measurements revealed good electrical properties, compared to a thermal oxide which was grown in N_2O, with flatband voltage values averaging at -0.29 V and a low positive mobile ion charge density in the order of 10^{10} cm^{-2}. XPS analysis revealed the FG annealed sample to have the most Si rich interface comparatively to other PDAs, with a C:Si ratio of 0.72, allowing more Si bonds to be terminated. SIMS analysis identified an increase in hydrogen near the interface of the FG-annealed sample with a peak concentration of 2.12×10^{21} cm^{-3}. It is concluded that the improvement in electrical performance is due to the hydrogen passivating trap states at the SiO_2/4H-SiC interface.

1. Introduction

Silicon carbide (SiC) devices are now prevalent in the 600 – 1700 V blocking voltage range. A key advantage of SiC is the possibility to form the same native oxide as silicon (Si), silicon dioxide (SiO_2), meaning it is highly compatible with mature Si processing. SiO_2 still represents the most widely used dielectric in power electronics, due to its favourable band offset and wide bandgap compared to other dielectrics such as aluminium oxide (Al_2O_3) [1]. Despite the favourable properties of SiC – its wide bandgap, high thermal conductivity and stable native oxide – surface passivation and gate oxides have been hampered by residual carbon at the interface following oxidation [2,3]. The density of interface trapped charge, D_{IT}, at SiO_2/SiC interfaces is several orders of magnitude higher than in SiO_2/Si interfaces, and threshold voltage instability is limiting uptake of commercial metal–oxide–semiconductor field-effect transistors (MOSFETs) [4].

An alternative to the thermal oxidation of SiC is the deposition of SiO_2 via atomic layer deposition (ALD), which offers high conformity and fine control of the deposition process. By depositing the layer, the substrate consumption and the amount of carbon released from the substrate is minimised, and defect densities associated with trapped carbon during thermal oxidation can be greatly reduced [5]. Critically however, a post-deposition anneal (PDA) is necessary after the deposition of dielectrics to improve the electrical performance of the layers. The choice of the PDA will determine leakage performance of the oxide and the D_{IT} at the interface. Investigations into PDAs have shown that high temperature anneals (>1000 °C) in nitrous or nitric oxide [6,7] , argon [8] or forming gas [9] ambient have all resulted in a reduction in the D_{IT} and an increase in channel mobility compared to the as-deposited layer [6–8]. In the past, forming gas anneals (FGA) have been studied extensively, especially on SiO_2/Silicon (Si) interfaces, with fewer reports having focused on thermally grown SiO_2/SiC structures [10–12]. More recent investigations have been published using a dry oxidation process followed by both nitric oxide (NO) anneals and FG-anneals [13,14], with improvements clearly correlated to the FGA. Further reports suggest that a two-step post-oxidation FG anneal, carried out at 800 °C and 1100 °C, for 30 min each, improves the interface quality, but also increase C–V hysteresis significantly, indicating that a large amount of mobile ions were introduced by this anneal [15–17]. Therefore, whether an anneal in forming gas is beneficial or detrimental to the interface quality remains an outstanding question.

Authors have previously reported a PDA study of ALD-deposited SiO_2 layers [9] across a temperature range of 900–1300 °C in reducing, inert and oxidising ambients, trying to apply the mechanism of FGA at elevated temperatures. The most significant outcome [9] was the improvement brought about by a 1100 °C PDA in forming gas ambient, which increased the breakdown field to greater than 10 MV/cm, outperforming a high quality thermal oxidation process in N_2O ambient [18].

In this letter, we present, for the first time, a study of ALD-deposited SiO_2 on 4H-SiC, in which the electrical properties of metal–oxide–semiconductor capacitors (MOSCAPs) are extracted, including D_{IT},

* Corresponding author.
E-mail address: A.Renz@warwick.ac.uk (A.B. Renz).

https://doi.org/10.1016/j.mssp.2020.105527
Received 2 June 2020; Received in revised form 24 September 2020; Accepted 19 October 2020
Available online 26 October 2020

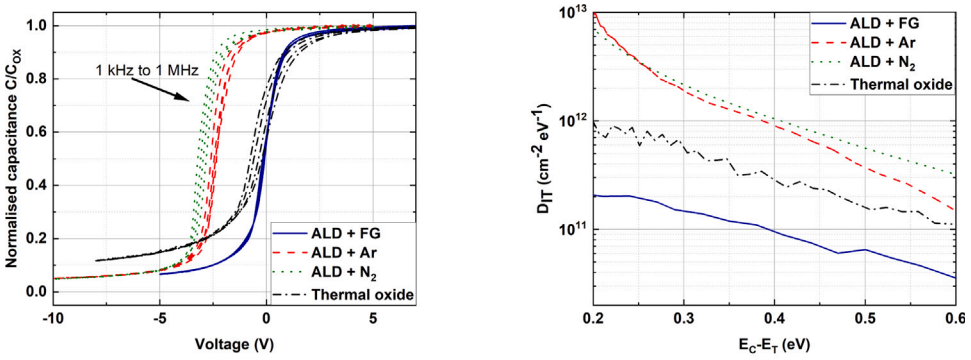


Fig. 1. (a) Capacitance–voltage curves (1 kHz, 10 kHz, 100 kHz, 1 MHz), normalised to the oxide capacitance, of annealed ALD-deposited and thermally oxidised samples and (b) D_{IT} with respect to the energy trap level E_T below the conduction band level E_C.

flatband voltage (V_{FB}), hysteresis voltage (V_H) and positive mobile ion charge. Furthermore, X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) are used to analyse the oxide–semiconductor interface to understand the physical mechanism behind the improvement brought about by the forming gas anneal. The investigation focuses on the aforementioned forming gas PDA, but also includes the impact of PDAs in nitrogen (N_2) and argon (Ar) ambients to clearly distinguish the effect of the forming gas ambient. For benchmarking reasons, a thermal oxidation process in N_2O ambient was also included.

2. Experimental

MOSCAPs were fabricated to analyse the effect of different annealing ambients on the interface quality. 4H-SiC epilayers were grown at Warwick using an LPE ACiS M8 reactor. Growth temperature was 1650 °C and used a trichlorosilane (TCS) and ethylene (C_2H_4) mix in an H_2 ambient at a nominal growth rate of 30 μm/h. 10 μm thick epilayers were intentionally doped during growth at 4×10^{15} cm^{-3} with nitrogen on a 1×10^{19} cm^{-3} highly N-doped substrate. The wafers were diced into 10 × 10 mm chips and cleaned with a solvent clean, followed by a HF(10%)/RCA1/HF(10%)/ RCA2/HF(10%) process. Samples were rinsed after the final HF step. The thermal oxide samples underwent oxidation in a furnace at 1300 °C for 4 h in a Ar:N_2O (4 slm:1 slm) ambient [18] resulting in a 55 nm layer thickness, measured via interferometry. The ALD samples underwent SiO_2 deposition in an Ultratech Fiji G2 Plasma-Enhanced ALD system, with a substrate temperature of 200 °C, bis(diethylamino)silane (BDEAS) as the Si precursor and O_2 plasma as a co-reagent. The layer thickness after 550 cycles was extracted by atomic force microscopy (AFM) to be 28 nm, with thickness variations below 1.5 nm between each anneal, considered negligible. Following deposition, the ALD samples were loaded into a high-temperature anneal furnace, where they were annealed either in argon, nitrogen or forming gas (FG, 5% H_2; 95% N_2), each process being 1 h in duration with a gas flow of 5 slm and a temperature of 1100 °C. For the MOSCAP samples, Al gate contacts (1 μm) were then deposited and patterned using a wet etch and a 1 μm Al ohmic contact was deposited on the backside using electron beam evaporation.

3. Results and discussion

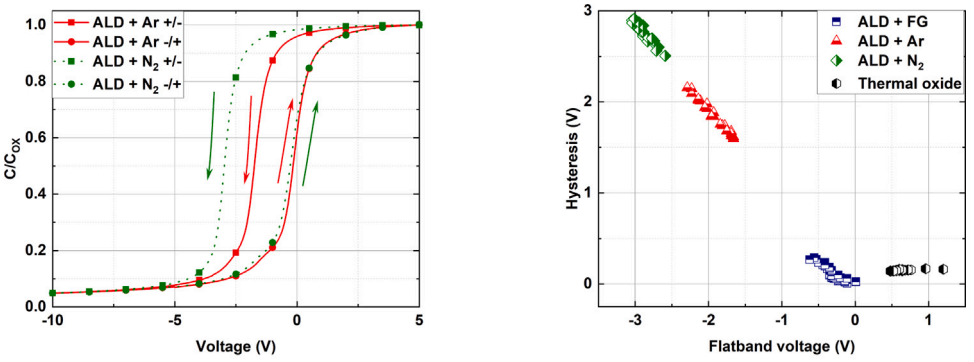
Room temperature vertical capacitance–voltage (C–V) measurements were recorded using an Agilent E4980A LCR meter, with the D_{IT} being calculated using the high-low method (1 MHz and 100 Hz). 100 Hz was chosen as the low frequency for the extraction of trap levels to keep a logarithmic frequency range from 10^2 to 10^6 Hz [19]. The surface potential was calculated using the Berglund integral [20], integrating around the flatband voltage [21]. The inaccuracies of this approach due to higher time constant dispersion in SiC as opposed to Si, shifting the surface potential towards the majority band edge, have been described in recent investigations [22,23]. However, since this investigation is a comparative study of different anneals, an estimate of D_{IT} can be provided and general trends can be derived and, as problems such as an underestimation of interface traps are considered to equally affect the whole sample set. An overview of results of at least 50 room temperature measurements per dataset are shown in Table 1. Representative C–V responses as well as their associated D_{IT} profiles relative to the conduction band edge are shown in Fig. 1. The D_{IT} extracted from the sample which was grown in N_2O ambient is in agreement with other reports [18]. They are also very repeatable with the flatband voltage and hysteresis both having tight distributions, averaging 0.61 V and 0.15 V, respectively.

Table 1
Summary of measured flatband voltage, hysteresis and frequency dispersion in accumulation values of 50 samples per category, with device areas of 1.26×10^{-3} cm^2 and 3.14×10^{-4} cm^2. A mixture of device areas was used for each treatment with no significant area effects being observed. Mean values are provided with standard deviations. Results for the ALD as-deposited samples have been reported previously [9].

Sample	Flatband voltage (V)	Hysteresis (V)	Frequency dispersion (%×dec^{-1})
ALD as-deposited [9]	8.39 ± 1.02	0.19 ± 0.13	2.58 ± 1.54
ALD+FG	−0.29 ± 0.13	0.10 ± 0.08	0.33 ± 0.29
ALD+Ar	−2.72 ± 0.79	1.86 ± 0.18	0.31 ± 0.15
ALD+N_2	−2.93 ± 0.12	2.83 ± 0.15	0.25 ± 0.11
Thermal oxide	0.61 ± 0.12	0.15 ± 0.01	0.40 ± 0.19

Although the Ar and N_2 annealed ALD-deposited oxides both improved upon the as-deposited ALD sample's average flatband voltage of 8.4 V [9], their C–V responses are poor compared to the N_2O oxidation process, with average flatband voltages decreasing to −2.72 V and −2.93 V, indicating the presence of positive charge at, or near, the interface. Furthermore, their high average hysteresis voltage values of 1.85 V and 2.83 V respectively indicate a significant quantity of positive mobile ions in the dielectric layer, which will be subject to further investigation later in this report.

The most significant outcome of this study is that the forming gas annealed samples show the most promising performance of the dataset, with flatband voltages averaging −0.29 V and the hysteresis values averaging 0.10 V, as shown in Fig. 1(b). The density of interface traps of the forming gas annealed samples is lower than the other datasets, with a D_{IT} of 2.12×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV, an order of magnitude lower than the N_2O oxide growth process. Of further significance is the deviation between forming gas and nitrogen annealed samples, with the D_{IT} of the N_2 samples being 6.6×10^{12} cm^{-2} eV^{-1} at



(a) (b)

Fig. 2. (a) Hysteresis C–V response of Ar and N_2 annealed samples at 1 MHz. Samples were swept from accumulation to deep depletion and backwards. (b) Hysteresis voltage plotted over flatband voltage for 50 MOSCAPs per different sample.

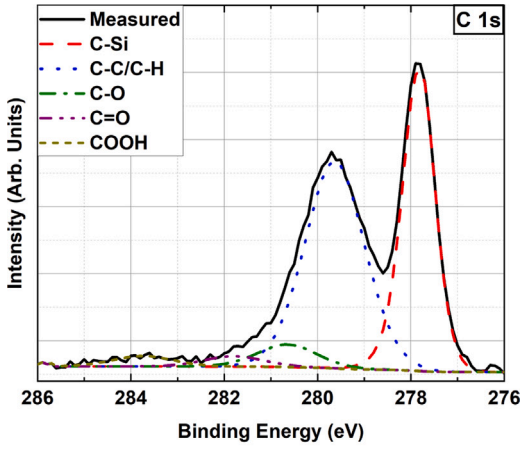
$E_C - E_T = 0.2$ eV. This is a first indication of the possible impact of hydrogen on the electrical performance of the investigated MOSCAPs.

The existence of another charge phenomenon within the different MOSCAP oxide layers was quantified by analysing the hysteresis in their C–V responses. Representative responses of the Ar and N_2 annealed samples at 1 MHz are shown in Fig. 2(a). They were first swept from accumulation into deep depletion, keeping the oxide electric field below 3 MV/cm. Afterwards, the same samples were swept "backwards". The observed dependence on the sweep direction is an indication of positive mobile charge states near the interface which are spontaneously generated during the operation of the device, causing a counter-clockwise capacitance shift. The counter-clockwise hysteresis was observed in the FG-annealed and thermally oxidised samples as well. Investigations on thermally oxidised SiO_2/4H-SiC structures initially suggested extrinsic effects such as ions introduced by metallisation or through hydrogen related anneals as the cause for the counter-clockwise hysteresis behaviour [24–26]. This was later found out to be an intrinsic behaviour, in which mobile positive ions in the oxide are accelerated towards the bottom of the SiO_2/SiC interface with deteriorating consequences on its interface trap density, reliability and bias temperature instability in measured MOSFETs [15,16]. The mobile charge areal density (D_{MC}) can then be calculated using the following relationship [21]:

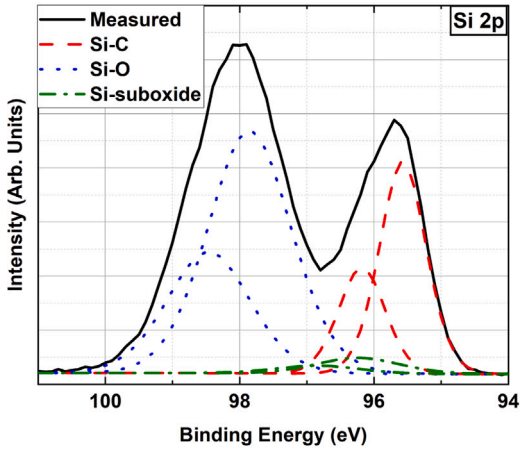
$$D_{MC} = (\Delta V_{FB} \times C_{OX}) / q, \quad (1)$$

where q is the electron charge (C), C_{OX} is the oxide capacitance per unit area (F cm^{-2}) and ΔV_{FB} is the hysteresis voltage (V). An overview of the density of mobile ion charge can be found in Table 2. The Ar and N_2 annealed MOSCAPs had the highest density of mobile ion charge, averaging 3.71×10^{11} cm^{-2} and 5.63×10^{11} cm^{-2}, respectively. In contrast, the forming gas annealed MOSCAPs had a much reduced density of these, averaging 1.13×10^{10} cm^{-2}, a value very slightly lower than the average value for the N_2O- oxidised MOSCAPs. The reduction in hysteresis voltage can also be seen in Fig. 2, with the hysteresis voltage being the flatband voltage difference between the measurements. The outcome of the FG-annealed improvement also represents a reduction by more than an order of magnitude compared to previous reports of ALD-deposited SiO_2 [6], and a reduction by a factor of 4 when compared to reports on high-quality ALD-deposited Al_2O_3 [27,28], which showed clockwise hysteresis, which were the result of slow states in the oxide.

For a further investigation into the origin of the improvement brought about by the FG-anneal, XPS was performed using a Kratos Axis Ultra DLD system on ALD as-deposited, N_2-annealed and FG-annealed SiO_2-SiC samples to investigate interface stoichiometry. Direct quantification of carbon clusters is not possible due to adventitious carbon that appears at the same binding energy as carbon clusters. However,



(a)



(b)

Fig. 3. XPS data and fits for the (a) C 1s region and (b) Si 2p region of the ALD as-deposited sample.

the stoichiometric ratio of Si–C in the Si 2p spectrum and C–Si in the C 1s spectrum is used to investigate interface chemistry. The samples were illuminated with Al Kα X-rays (1486.6 eV) and the spectra were

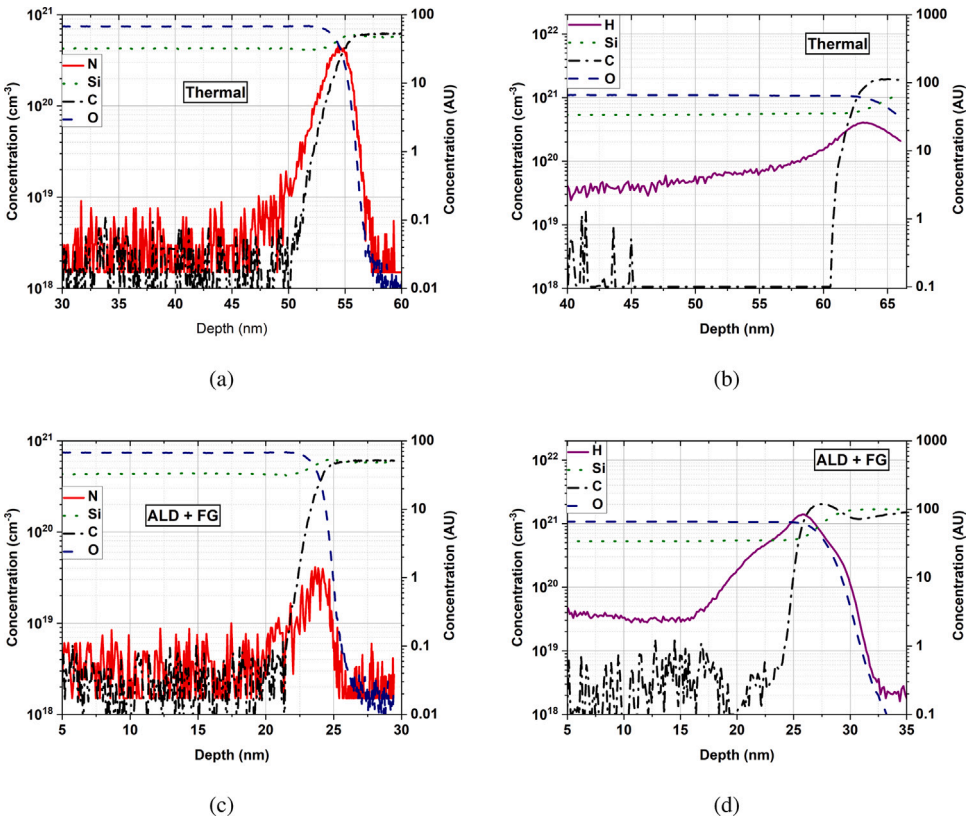


Fig. 4. SIMS profiles of nitrogen (a) and hydrogen (b) in the thermally oxidised sample and nitrogen (c) and hydrogen (d) in the FG-annealed ALD-deposited sample. Samples had a deposited/grown SiO_2 layer on top of the semiconductor, profiles are shown for the whole of the oxide and the first 5–10 nm of the semiconductor. H and N are quantified with absolute values, Si, C and O with arbitrary units.

Table 2
Density of mobile charge states from 25 samples each with a device area of 1.257×10^{-3} cm^2. Values are average values provided with standard deviations.

Sample	Density of mobile charge states (cm^{-2})
ALD+FG	$1.13\times10^{10} \pm 5.84\times10^{9}$
ALD+Ar	$3.71\times10^{11} \pm 3.47\times10^{10}$
ALD+N_2	$5.63\times10^{11} \pm 2.28\times10^{10}$
Thermal oxide	$1.28\times10^{10} \pm 9.00\times10^{8}$

analysed at a take off angle (ToA) of 90°, giving a 3 λ depth of 10 nm. All investigated oxides were approximately 5 nm thick. High-resolution core spectra were taken for Si *2p*, C *1s*, O *1s* and N *1s*, and the data were analysed using the CasaXPS software package, employing Shirley backgrounds and Voigt (Gaussian–Lorentzian) lineshapes. XPS data and fits of the ALD as-deposited sample can be found in Fig. 3. Only marginally different spectra and fits were obtained for the other investigated samples. All three ALD samples showed a higher signal from Si–C in the Si *2p* spectrum than the C–Si in the C *1s*, implying Si enrichment at the surface. The as-deposited sample showed the least Si enrichment, with a C:Si ratio of 0.8, the N_2-annealed sample's ratio was 0.74 and the FG-annealed sample showed a marginal decrease to 0.72.

These C:Si ratios contrast sharply with those from thermal oxidation processes [29], where the C:Si ratio is higher than 1. However, N_2O processes have been shown to improve stoichiometry, bringing the C:Si ratio closer to 1, than for dry oxidation processes [29]. In thermal oxidation processes in N_2O ambient, N is assumed to passivate excess carbon, resulting in an overall less defective interface. In deposition processes, however, the C:Si ratio lower than 1 suggests that native Si and the Si precursor BDEAS bind to C, resulting in little-to-no residual carbon at the interface and excess Si dominating interface defect levels. In contrast to C defects, which are typically reduced only by nitridation, a wider range of Si passivation treatments exist, most prominently FG annealing [21]. The decrease in C:Si ratio with any anneal step, as well as a decrease in the Si-suboxide component, suggests that Si complexes, such as Si dimers or Si_xO_y groups, are broken down into simple Si dangling bonds, which can be readily passivated with a FG anneal. When compared to work by Umeda et al. [30,31] using electron spin resonance (ESR) and electrically detected magnetic resonance (EDMR) on thermally grown SiO_2/SiC, no signal for Si dangling bonds (P_b) was found, but that the carbon dangling bond (P_bc) signal is characterised in abundance. Here, although not a direct comparison, we note that thermally grown oxides have a c-rich interface which would support an analogous larger P_bc signal. This underlines the fundamental difference between the thermally grown and the deposited SiO_2/SiC interface.

Secondary ion mass spectrometry (SIMS) was performed to investigate the distribution of nitrogen and hydrogen located at the interfaces of the thermally-grown oxide and FG-annealed ALD-deposited oxide. Due to the complexity and background noise level of SIMS measurements in MOS structures, individual samples were prepared in parallel for each profile. H and N SIMS profiles from the thermal and the FG sample are shown in Fig. 4. In these, H and N are quantified with absolute values, with Si, C and O only quantified in arbitrary units. It should be noted that the detection limit for N in SiO_2 is 2×10^{18} cm^{-3}, and H in SiO_2 is 3×10^{19} cm^{-3}, shown on the graphs. As Table 3 and Fig. 4(b) show, N appears at the interface for both samples, with similar observations for H. These increases in atomic concentration can also partly originate from measurement artefacts such as a residual atmospheric contamination on the surface before oxide growth/deposition , a change in ionisation efficiency as SIMS sputters through the interface, and charging/charge compensation changing near the interface. As such, comparisons are made based on the maximum concentration of N and H at the interface, with results shown in Table 3. As one might

Table 3
SIMS results: peak interfacial concentration of H and N.

Process	Peak H concentration (cm^{-3})	Peak N concentration (cm^{-3})
Thermal	3.50×10^{20}	4.48×10^{20}
ALD+FG	1.50×10^{21}	4.40×10^{19}

expect, the thermally-grown oxide shows the highest peak nitrogen concentration, approximately an order of magnitude higher than the deposited oxide, and hydrogen concentration four times lower than ALD-FG oxide. The N profile for the thermal sample is similar to Fig. 4(a), where the N levels fall below detection limits, hence both are localised to the interface rather than distributed through the oxide. Diametrically, the H peak concentration is four times lower within the thermally-grown oxide, than the ALD-FG sample. However, whilst H levels are detected throughout the thermal oxide, they fall below detection limits in the ALD-FG sample, having implications on how this potential mobile charge can move. The results support the notion that the improvement in electrical performance of the ALD FG-annealed oxide layers can be down to the hydrogen passivation of Si dangling bonds at the oxide–semiconductor interface. The aforementioned theory of the hydrogen passivation effect is also backed up by theoretical descriptions [3,32], in which hydrogen was found to have the potential to passivate traps near SiO_2/4H-SiC interfaces.

4. Conclusion

In summary, a high quality SiO_2/SiC interface has been developed by annealing the ALD deposited SiO_2 layer in forming gas for one hour at 1100 °C. This has brought about improvements to the ALD layer in terms of flatband voltage (-0.29 ± 0.13 V) , hysteresis (0.10 ± 0.08 V), D_{IT} (2.12×10^{11} cm^{-2} eV^{-1} at $E_C - E_T = 0.2$ eV) and positive mobile charge density near the interface of 1.13×10^{10} cm^{-2}. XPS analysis revealed a Si-rich interface for all ALD-deposited samples, with the FG having the most Si-rich interface with a C:Si ratio of 0.72. As Si-suboxide components were reduced as well, this suggests that the anneal breaks down Si complexes into Si dangling bonds, which can then be passivated. SIMS analysis demonstrated an increase in hydrogen concentration near the interface of the annealed sample when compared to a thermal sample, with a peak concentration of 1.50×10^{21} cm^{-3} being four times higher than for the thermal oxide, suggesting that the improvement in electrical performance is due to hydrogen passivation of trap states at the oxide–semiconductor interface. It is concluded that a more stoichiometric interface allows compositionally greater hydrogen passivation. Hence, passivation in ALD-deposited SiO_2/4H-SiC becomes similar to the well known thermal SiO_2/Si system, and is outlined here for the first time.

CRediT authorship contribution statement

A.B. Renz: Investigation, Methodology, Conceptualisation, Software, Writing - original draft. **O.J. Vavasour:** Conceptualisation, Formal analysis, Writing - review. **P.M. Gammon:** Conceptualisation, Writing - review & editing, Resources, Supervision, Project administration. **F. Li:** Validation, Conceptualisation, Writing - review & editing. **T. Dai:** Validation, Writing - review & editing. **M. Antoniou:** Writing - review & editing. **G.W.C. Baker:** Software, Validation. **E. Bashar:** Formal analysis, Software, Writing - review & editing. **N.E. Grant:** Methodology, Conceptualisation, Writing - review. **J.D. Murphy:** Writing - review & editing, Resources. **P.A. Mawby:** Resources, Writing - review & editing, Project administration. **V.A. Shah:** Conceptualisation, Validation, Resources, Writing - review & editing, Funding acquisition, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

The work presented in this paper has been carried out as part of EPSRC projects EP/P017363/1 and EP/R00448X/1. The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

[1] V. Afanas' ev, M. Bassler, G. Pensl, M. Schulz, E. Stein von Kamienski, Band offsets and electronic structure of SiC/SiO_2 interfaces, J. Appl. Phys. 79 (6) (1996) 3108–3114.
[2] A. O'Neill, O. Vavasour, S. Russell, F. Arith, J. Urresti, P. Gammon, Dielectrics in silicon carbide devices: Technology and application, Adv. Silicon Carbide Electron. Technol. II: Core Technol. Silicon Carbide Device Process. 69 (2020) 63.
[3] S. Wang, S. Dhar, S.-r. Wang, A. Ahyi, A. Franceschetti, J. Williams, L.C. Feldman, S.T. Pantelides, Bonding at the SiC-SiO_2 interface and the effects of nitrogen and hydrogen, Phys. Rev. Lett. 98 (2) (2007) 026101.
[4] F. Roccaforte, P. Fiorenza, G. Greco, R.L. Nigro, F. Giannazzo, F. Iucolano, M. Saggio, Emerging trends in wide band gap semiconductors (SiC and GaN) technology for power devices, Microelectron. Eng. 187 (2018) 66–77.
[5] C. Kim, J. Hyun Moon, J. Hyuk Yim, D. Hyun Lee, J. Ho Lee, H. Hee Lee, H. Joon Kim, Comparison of thermal and atomic-layer-deposited oxides on 4H-SiC after post-oxidation-annealing in nitric oxide, Appl. Phys. Lett. 100 (8) (2012) 082112.
[6] X. Yang, B. Lee, V. Misra, Electrical characteristics of SiO_2 deposited by atomic layer deposition on 4H–SiC after nitrous oxide anneal, IEEE Trans. Electron Devices 63 (7) (2016) 2826–2830.
[7] M.S. Kang, B.M. Lee, V. Misra, Improved threshold voltage instability in 4H-SiC MOSFETs with atomic layer deposited SiO_2, in: Materials Science Forum, Vol. 924, Trans Tech Publ, 2018, pp. 498–501.
[8] S. Lee, J.M. Kim, C. Kim, H. Kim, H.J. Kang, M.-W. Ha, H.J. Kim, Densification of silicon dioxide formed by plasma-enhanced atomic layer deposition on 4h-silicon carbide using argon post-deposition annealing, Ceram. Int. 44 (12) (2018) 13565–13571.
[9] A. Renz, O. Vavasour, P. Gammon, F. Li, T. Dai, S. Esfahani, G. Baker, N. Grant, J. Murphy, P. Mawby, V. Shah, Development of high-quality gate oxide on 4H-SiC using atomic layer deposition, in: Materials Science Forum, Vol. 1004, Trans Tech Publ, 2020, pp. 547–553.
[10] F. Allerstam, E.Ö. Sveinbjörnsson, A study of deep energy-level traps at the 4H-SiC/SiO_2 interface and their passivation by hydrogen, in: Materials Science Forum, Vol. 600, Trans Tech Publ, 2009, pp. 755–758.
[11] J.-L. Cantin, H.J. von Bardeleben, Forming gas annealing of the carbon PbC center in oxidized porous 3C-and 4H-SiC: an EPR study, in: Materials Science Forum, Vol. 527, Trans Tech Publ, 2006, pp. 1015–1018.
[12] H.J. von Bardeleben, J. Cantin, Y. Shishkin, R.P. Devaty, W.J. Choyke, Microscopic structure and electrical activity of 4H-SiC/SiO_2 interface defects: An EPR study of oxidized porous SiC, in: Materials Science Forum, Vol. 457, Trans Tech Publ, 2004, pp. 1457–1462.
[13] Z. Peng, Y. Wang, H. Shen, C. Li, J. Wu, Y. Bai, K. Liu, X. Liu, Effects of combined NO and forming gas annealing on interfacial properties and oxide reliability of 4H-SiC MOS structures, Microelectron. Reliab. 58 (2016) 192–196.
[14] W. Yiyu, P. Zhaoyang, S. Huajun, L. Chengzhan, W. Jia, T. Yachao, Z. Yanli, C. Ximing, L. Kean, L. Xinyu, Characterization of the effects of nitrogen and hydrogen passivation on SiO_2/4H-SiC interface by low temperature conductance measurements, J. Semicond. 37 (2) (2016) 026001.
[15] A. Chanthaphan, T. Hosoi, S. Mitani, Y. Nakano, T. Nakamura, T. Shimura, H. Watanabe, Investigation of unusual mobile ion effects in thermally grown SiO_2 on 4H-SiC (0001) at high temperatures, Appl. Phys. Lett. 100 (25) (2012) 252103.
[16] A. Chanthaphan, T. Hosoi, Y. Nakano, T. Nakamura, T. Shimura, H. Watanabe, Understanding and controlling bias-temperature instability in SiC metal-oxide-semiconductor devices induced by unusual generation of mobile ions, Appl. Phys. Lett. 102 (9) (2013) 093510.
[17] A. Chanthaphan, T. Hosoi, Y. Nakano, T. Nakamura, T. Shimura, H. Watanabe, Improved bias-temperature instability characteristics in SiC metal-oxide-semiconductor devices with aluminum oxynitride dielectrics, Appl. Phys. Lett. 104 (12) (2014) 122105.
[18] H. Rong, Y.K. Sharma, T. Dai, F. Li, M.R. Jennings, S.A. Russell, D.M. Martin, P.A. Mawby, High temperature nitridation of 4H-SiC MOSFETs, in: Materials Science Forum, Vol. 858, Trans Tech Publ, 2016, pp. 623–626.

[19] T. Kimoto, J.A. Cooper, Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications, John Wiley & Sons, 2014.
[20] C. Berglund, Surface states at steam-grown silicon-silicon dioxide interfaces, IEEE Trans. Electron Devices (10) (1966) 701–705.
[21] D.K. Schroder, Semiconductor Material and Device Characterization, John Wiley & Sons, 2015.
[22] H. Yoshioka, T. Nakamura, T. Kimoto, Generation of very fast states by nitridation of the SiO_2/SiC interface, J. Appl. Phys. 112 (2) (2012) 024520.
[23] A.V. Penumatcha, S. Swandono, J.A. Cooper, Limitations of the high-low c-v technique for MOS interfaces with large time constant dispersion, IEEE Trans. Electron Devices 60 (3) (2013) 923–926.
[24] T. Okayama, S. Arthur, J. Garrett, M. Rao, Bias-stress induced threshold voltage and drain current instability in 4H–SiC DMOSFETs, Solid-State Electron. 52 (1) (2008) 164–170.
[25] A.J. Lelis, D.B. Habersat, R. Green, N. Goldsman, Temperature-dependence of SiC MOSFET threshold-voltage instability, in: Materials Science Forum, Vol. 600, Trans Tech Publ, 2009, pp. 807–810.
[26] Z. Chen, A. Ahyi, X. Zhu, M. Li, T. Isaacs-Smith, J. Williams, L.C. Feldman, MOS characteristics of C-face 4H-SiC, J. Electron. Mater. 39 (5) (2010) 526–529.
[27] E. Schilirò, R. Lo Nigro, P. Fiorenza, F. Roccaforte, Negative charge trapping effects in Al_2o_3 films grown by atomic layer deposition onto thermally oxidized 4H-SiC, AIP Adv. 6 (7) (2016) 075021.
[28] S.S. Suvanam, M. Usman, D. Martin, M.G. Yazdi, M. Linnarsson, A. Tempez, M. Götelid, A. Hallén, Improved interface and electrical properties of atomic layer deposited Al_2o_3/4H-SiC, Appl. Surf. Sci. 433 (2018) 108–115.
[29] A. Renz, V. Shah, O. Vavasour, Y. Bonyadi, F. Li, T. Dai, G. Baker, S. Hindmarsh, Y. Han, M. Walker, et al., The improvement of Mo/4H-SiC schottky diodes via a P_2o_5 surface passivation treatment, J. Appl. Phys. 127 (2) (2020) 025704.
[30] T. Umeda, M. Okamoto, R. Kosugi, S. Harada, R. Arai, Y. Sato, T. Makino, T. Ohshima, SiC MOS interface states: Difference between Si face and C face, ECS Trans. 58 (7) (2013) 55.
[31] T. Umeda, Y. Nakano, E. Higa, T. Okuda, T. Kimoto, T. Hosoi, H. Watanabe, M. Sometani, S. Harada, Electron-spin-resonance and electrically detected-magnetic-resonance characterization on PbC center in various 4H-SiC (0001)/SiO_2 interfaces, J. Appl. Phys. 127 (14) (2020) 145301.
[32] A.-M. El-Sayed, Y. Wimmer, W. Goes, T. Grasser, V.V. Afanas'ev, A.L. Shluger, Theoretical models of hydrogen-induced defects in amorphous silicon dioxide, Phys. Rev. B 92 (1) (2015) 014107.