Simulations and Measurements of Failure Modes in SiC Cascode JFETs under Short Circuit Conditions

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***Abstract*—Using experimental measurements and finite element simulations, this paper investigates the failure mode of SiC Cascode JFETs under short circuit (SC) conditions. Unlike SiC MOSFETs, where failure results in a shorted gate-source terminal (resulting from gate oxide failure), in SiC Cascode JFETs, failure usually occurs in drain-source short with the gate of the Low Voltage (LV) silicon MOSFET still operational. Measurements show that after the LV Si MOSFET gate is turned OFF, a high tail current results in the Cascode drain terminal with the drain-source voltage falling to approximately half of the blocking voltage, suggesting that the JFET is in linear mode. Finite element simulations show that thermally generated carriers in the JFET depletion region cause high leakage currents through the internal JFET gate terminal capable of turning-ON the JFET (after turn-OFF of the LV Si MOSFET) into linear mode. The measured short circuit withstand time (SCWT) is shown to be independent of temperature unlike silicon MOSFETs where the SC withstand time increases with the initial temperature.**

Keywords—Short Circuit, SiC, Cascode JFET, TCAD simulations, Robustness, Reliability

I. INTRODUCTION

SiC Cascode JFETs are a promising device technology that combines the gate oxide reliability of silicon MOSFETs with the fast switching of SiC MOSFETs [1, 2]. SiC MOSFETs have been reported to have reduced gate oxide reliability compared to silicon MOSFETs and IGBTs [3-7], hence, the Cascode is attractive because it avoids the problem of increased interface trap density and fixed oxide traps in SiC/SiO_2 MOS interfaces. The cascode is formed by connecting a low voltage (LV) silicon MOSFET between the gate-source terminals of a High Voltage (HV) SiC JFET so that the normally ON operation of the JFET is converted into normally OFF operation (as long as the MOSFET breakdown voltage is larger than the magnitude of the JFET pinch-off voltage). Fig. 1 shows the internal configuration of the cascode structure.

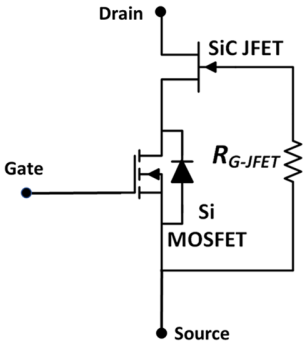

Fig. 1. SiC Cascode JFET structure

As SiC cascode JFETs are gaining popularity in different applications [8-10], reliability and robustness studies are fundamental for increasing their adoption. Hence, it has become necessary to understand the failure mode of SiC devices under short circuit (SC) conditions. In SiC MOSFETs, various studies have shown that the gate terminal is the failure point under SC conditions. This results from thermally generated carriers tunnelling through the gate oxide thereby causing permanent damage [11-15].

The performance of SiC Cascode JFETs under SC conditions has also been evaluated previously [16, 17], where the trade-off between the short circuit withstand time SCWT and specific on-resistance is demonstrated. In SiC Cascode JFETs, since a LV silicon MOSFET is used, the failure mode is different. For example, considering unclamped inductive switching (UIS), previous studies indicated the key role of the gate leakage current of the JFET during UIS conditions [18-20]. This paper aims to investigate the failure modes of SiC Cascode JFETs during SC conditions. This is achieved by performing

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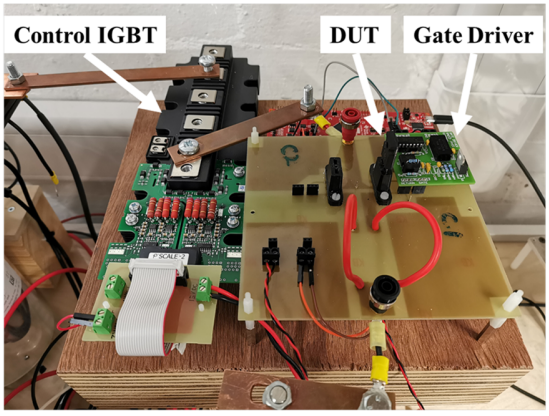
single pulse SC tests on SiC Cascode JFETs while increasing the pulse duration to the point of failure. These measurements are performed at different initial junction temperatures to investigate the temperature sensitivity of the SCWT. TCAD simulations are used to understand the internal physics of the device under short circuit so as to understand the failure mode.

This paper is structured as follows, in section II, the SC experimental methodology and experimental results are presented, Section III presents SC finite element (FE) simulations of the Cascode JFET performed in SILVACO TCAD and Section IV concludes the paper.

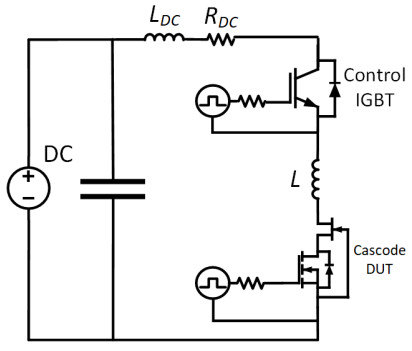
II. SHORT CIRCUIT EXPERIMENT

A. *Short Circuit Methodology*

The short circuit test system is shown in Fig. 2(a), with the electrical schematic show in Fig. 2(b). It comprises of a DC voltage source (400 V), DC link capacitors, a control IGBT, and the Device Under Test (DUT). The DUT is a 650 V/31 A SiC Cascode JFET from UnitedSiC with datasheet reference UJ3C065080K3S and the control IGBT is a 1200 V/1000 A IGBT from Infineon with datasheet reference FF1000R17IE4. A DSP is used to control the gate drivers of the IGBT and the SiC Cascode JFET in a non-destructive short circuit [21, 22]. The IGBT is turned ON before the DUT and turned-OFF after the DUT thereby ensuring the DUT is disconnected from the power supply, after the defined short circuit test duration, as shown in Fig. 3. The IGBT is a 1000 A power module hence, is



(a)



(b)

Fig. 2. (a) Experimental setup (b) Electrical Schematic

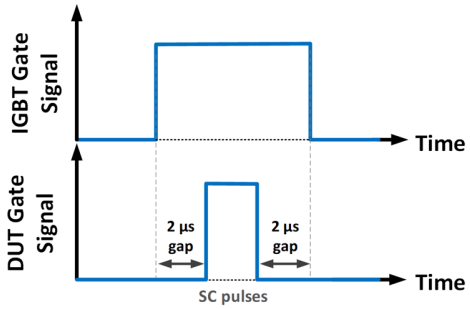


Fig. 3 Gate signals during the short circuit test

not susceptible to failure at the short circuit current levels of the evaluated SiC Cascode JFET.

B. *Short Circuit Results*

Fig. 4 shows measurements of SC currents in the SiC Cascode JFET for various durations. The duration of the SC is extended until the device fails. As seen in Fig. 4, the device fails with drain-source current runaway. Subsequent failure analysis revealed that the drain-source terminals of the Cascode device where short-circuited with the gate-source terminals still functional. Fig. 5 shows the corresponding drain-source voltage measurements showing a precipitous reduction in V_{DS} although not to zero as would be expected in a proper drain-source short-

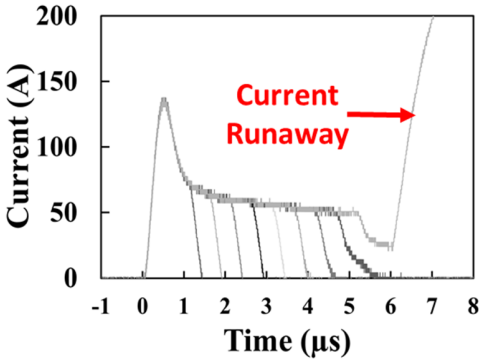


Fig. 4. Short circuit current measurements for different durations until failure

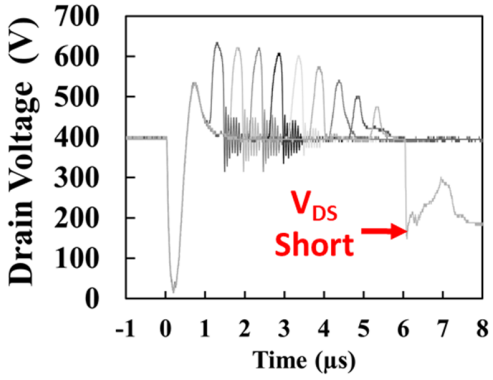


Fig. 5. Corresponding Short circuit Voltage measurements.

circuit. Finite element simulations will show that this is due to the JFET turning ON.

In the case of the SiC cascode, the last pass short-circuit current transient for different initial case temperatures is shown in Fig. 6. Although there is a slight reduction of the peak current with increasing case temperature, the SCWT is temperature invariant. Different device technologies will have different short-circuit performance, hence, similar measurements of SCWT were performed at different initial case temperatures for a 650 V SiC Trench MOSFET with datasheet reference SCT3080AL, a 650 V Silicon super-junction MOSFETs with datasheet reference IPW65R080CFDA and a 650 V silicon MOSFET with datasheet reference SiHG33N60EF. All devices have similar current ratings between 30 A and 40 A at 25 °C. The SCWTs for these devices are shown in Fig. 7 where the SiC Cascode device has a SCWT independent of initial temperature whereas the silicon devices have SCWTs that increase with initial temperature. In this case of the SiC Trench MOSFET, the SCWT reduces with temperature.

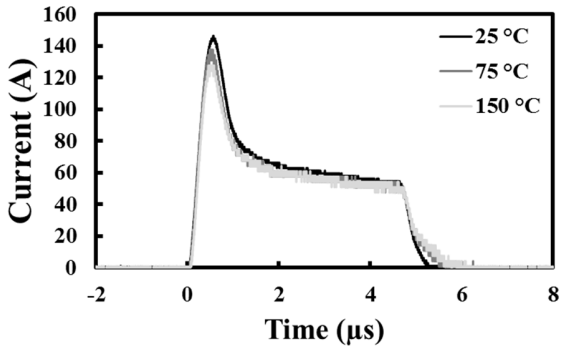


Fig. 6. Short circuit current transients for the SiC Cascode for different initial case temperatures

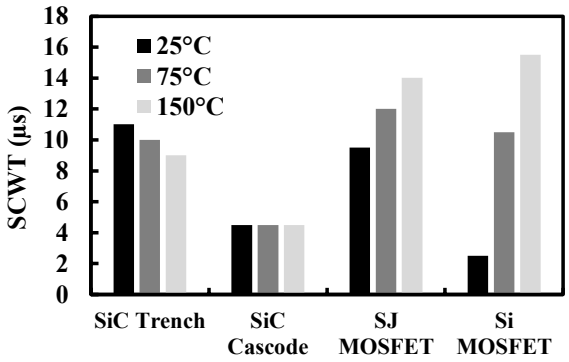


Fig. 7. SCWT measured for different technologies at different temperatures

III. Finite Element Simulations

The SiC Cascode JFET has been simulated in SILVACO using mixed-mode TCAD simulations with the structure parameters shown in Table I. Fig. 8 shows the structure of the device used in the simulations.

TABLE I. Simulation parameters for SiC Cascode JFET

Parameter	Values
Source doping (cm^{-3})	$1x10^{19}$
Channel Length (µm)	1.2
Drift layer thickness (µm)	6.0
Drift layer doping (cm^{-3})	$2.33x10^{16}$
Drain doping (cm^{-3})	$1x10^{19}$
Channel doping (cm^{-3})	$2.33x10^{16}$
JFET gate doping (cm^{-3})	$1x10^{19}$
Cell pitch (µm)	3.2
Area factor (µm)	$6x10^{5}$
Breakdown (V)	800

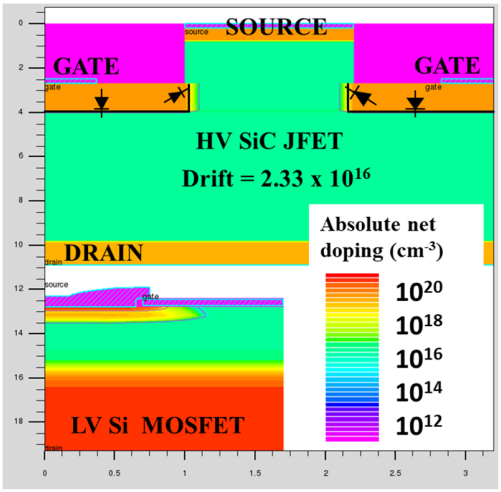


Fig. 8. Simulated SiC Cascode JFET structure

The drift region of the simulated device is designed for a theoretical breakdown of 800 V, usual breakdown voltage for a 650 V rated device. For the simulations in SILVACO, the physical models CVT (accounts for the inversion layer mobility), BGN (accounts for bandgap narrowing at high temperatures), SRH (accounts for carrier lifetime), ANALYTIC (accounts for the low field mobility), FLDMOB (accounts for field dependent effective mobility), and AUGER (accounts for Auger recombination at high carrier densities) were enabled. The heat flow within the device is calculated by enabling the LAT.TEMP model statement. To further increase the accuracy of the chip temperature, the temperature dependent heat capacity of 4H-SiC is specified using values from the literature [23].

Fig. 9 and Fig. 10 show the simulated short circuit currents and voltages extracted from SILVACO. The results show the short circuit current and voltage waveforms for different short circuit durations. Also shown in Fig. 9 is the extracted hotspot temperature. Hot-spot temperatures of more than 1000 °C are observed in these simulations. The simulation predicts thermal runaway of the drain source current during failure and the simulated V_{DS} characteristics are similar to the experimental results in Fig. 5. To understand the internal physics of failure,

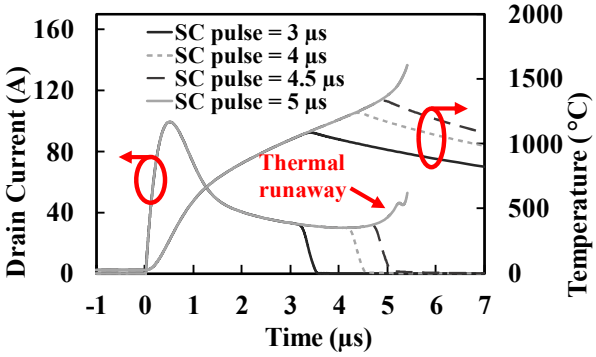


Fig. 9. Simulated short circuit current characteristics of SiC Cascode JFET

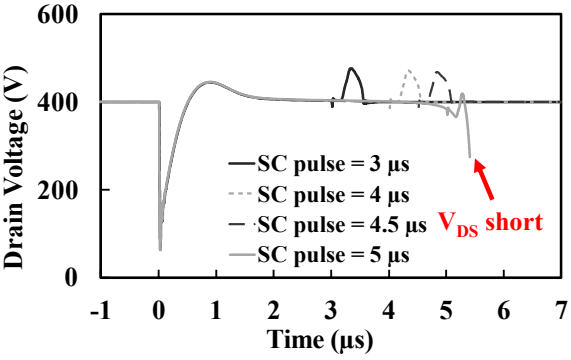


Fig. 10 Simulated short circuit drain-source voltage characteristics of SiC Cascode JFET

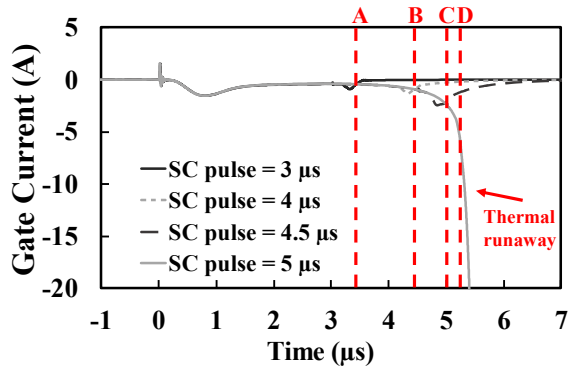


Fig. 11. Simulated internal JFET gate current

the gate current of the JFET is extracted from the simulation, as shown in Fig. 11 for the different short circuit durations.

This gate current should always be on the order of magnitude of micro-amperes since it is a leakage current of a reverse biased PN junction when the device is turned OFF. However, the point of failure (approximately point D in Fig. 11) shows a significant increase in the JFET gate leakage current, which occurs at the end of the LV silicon MOSFET turn-ON duration. The leakage current observed here is the result of thermally generated carriers in the device resulting in thermal runaway. This JFET gate leakage current causes a voltage drop at the gate-source terminal of the JFET due to $R_{G\text{-}JFET}$. If the voltage drop across R_{GJFET} is large enough to turn the JFET ON, the device will operate in linear mode and since the silicon MOSFET is OFF and the channel is closed, the current will flow through the JFET gate thereby causing damage. Since the LV silicon MOSFET is OFF, it is not damaged by the excessive SC currents hence, remains operational after the short circuit failure. Fig. 12 shows the schematic of the Cascode JFET indicating the SC current flow path before and during failure. Before failure, all the current flows through the LV Si MOSFET, but as the device is closer to failure, the JFET gate current increases.

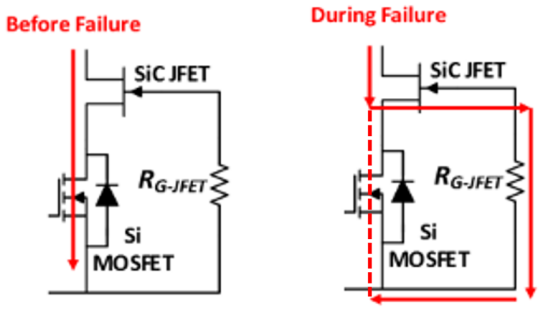


Fig. 12. Cascode schematic showing current flow path under SC Failure

The 2D current density plots from the simulated Cascode JFET can be key for explaining this failure mechanism. The device 2D current density plots and 2D temperature plots have been extracted from the simulation for two different pulse durations case 1: pulse before failure (4.5 µs), and case 2: Failure pulse (5 µs). The 2D current density plots were extracted at the time instants A(3.5 µs), B(4.5 µs) C(5 µs) and D(5.3 µs) indicated in Fig. 11.

Fig. 13(a) to Fig. 13(d) show the 2D current density contour plots corresponding to the short circuit pulse before failure case. Analysing the current contours in Fig. 13(a) to Fig. 13(d), the current density in the regions adjacent to the JFET gate does not increase substantially during the short-circuit pulse. As the LV MOSFET is switched OFF carrier generation in the JFET depletion region reduces indicating a successful suppression the SC current. The leakage current through the JFET gate can be seen in all four current density plots and its peak value occurs at time instant C (Fig. 11) and a reduction is observed at time instant D the current through the gate reduces as confirming Fig. 11.

Fig. 14 shows the extracted carrier density along the cross-sectional cutline shown in Fig. 13. The extracted cross-sectional cutline is done along the JFET gate, providing a clearer assessment the JFET gate leakage current.

Fig. 15 shows the simulated temperature in the JFET and the LV Si MOSFET at time instant D (5.3 µs) from Fig. 11. The MOSFET is approximately at 29 °C indicating a slight increase from the starting temperature of 27 °C while the JFET hotspot has not reached the critical failure temperature. This shows that all the SC energy dissipated by the SiC Cascode JFET is dissipated by the HV JFET without any stress on the LV MOSFET, confirming results previously reported [17, 20].

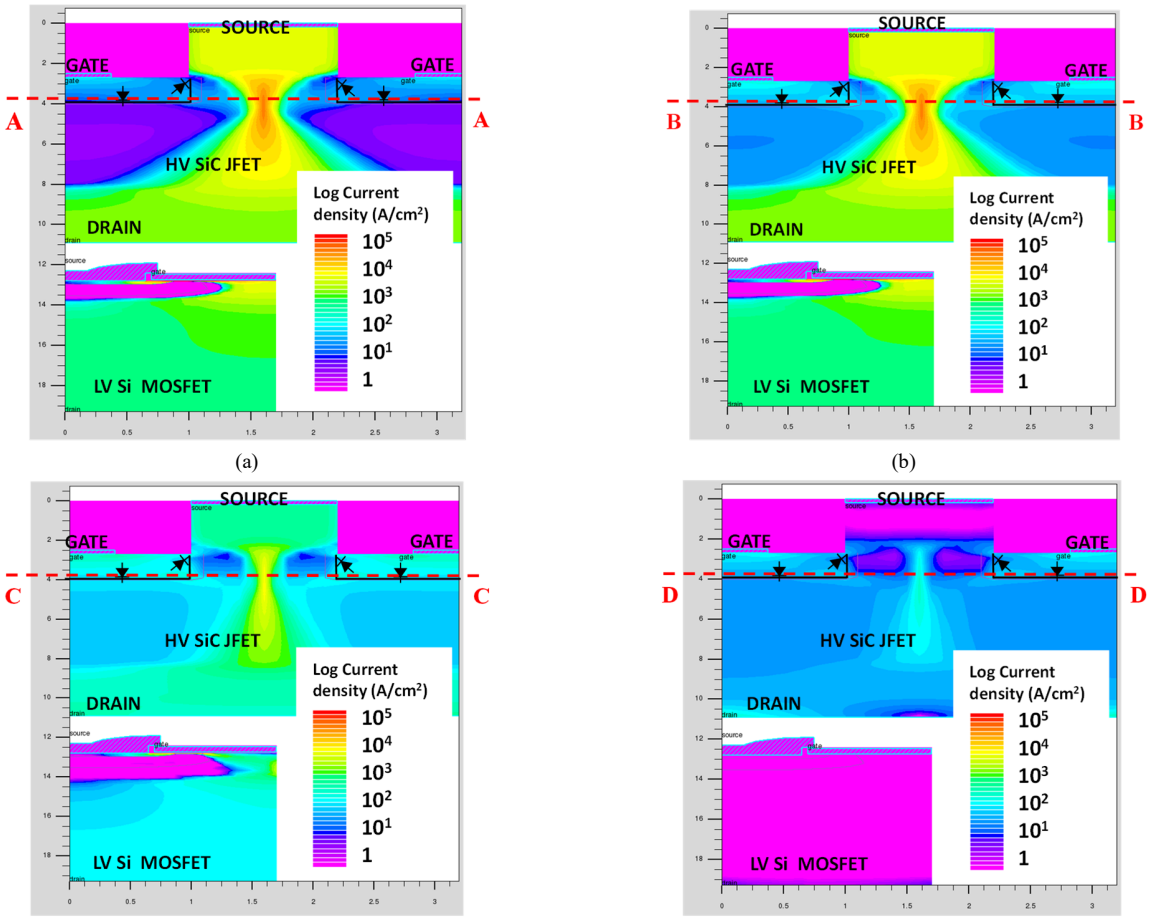


Fig. 13. 2D Current density contour plots during SC, SC pulse duration = 4.5 µs
(a) Time instant A (3.5 µs) (b) Time instant B (4.5 µs) (c) Time instant C (5 µs) (d) Time instant D (5.3 µs)

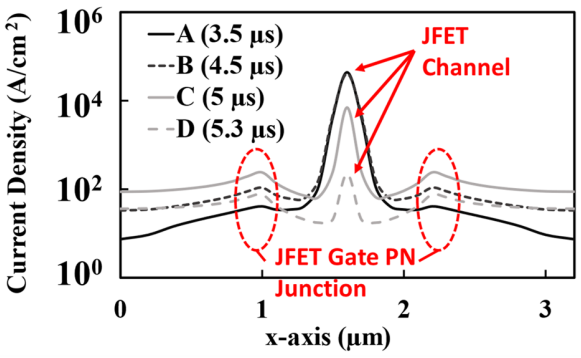


Fig. 14. Extracted total current density along cross-section cutline at different time instants (SC pulse duration = 4.5 µs)

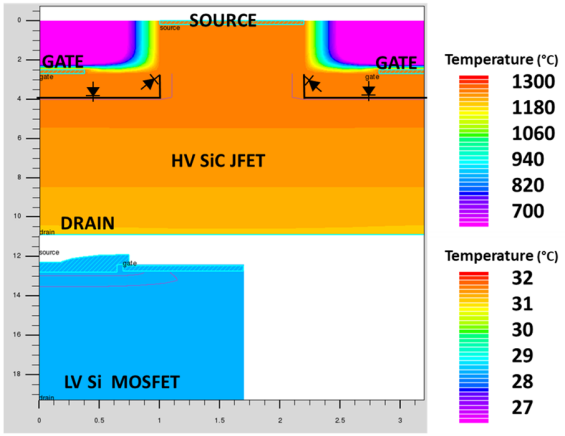


Fig. 15. 2D Temperature distribution plot showing JFET temperature in comparison to LV MOSFET temperature (SC pulse duration = 4.5 µs)

The 2D current density contour plots of the device subjected to the short circuit failure pulse case are shown in Fig. 16(a) to Fig. 16(d). Compared with the no failure case, Fig. 16 (c) and Fig. 16(d) show an increase in thermally generated carriers in the JFET depletion region. This causes a failure in the JFET gate PN junction leading to currents of magnitude greater than 20 A to flow out of the JFET gate, as can be seen in Fig.11. Current of this magnitude is enough to induce a voltage on R_{GJFET} greater than the magnitude of the JFET pinch-off, thereby turning ON the JFET channel and causing the JFET to operate in linear mode. In this mode, the short circuit current flows from the JFET

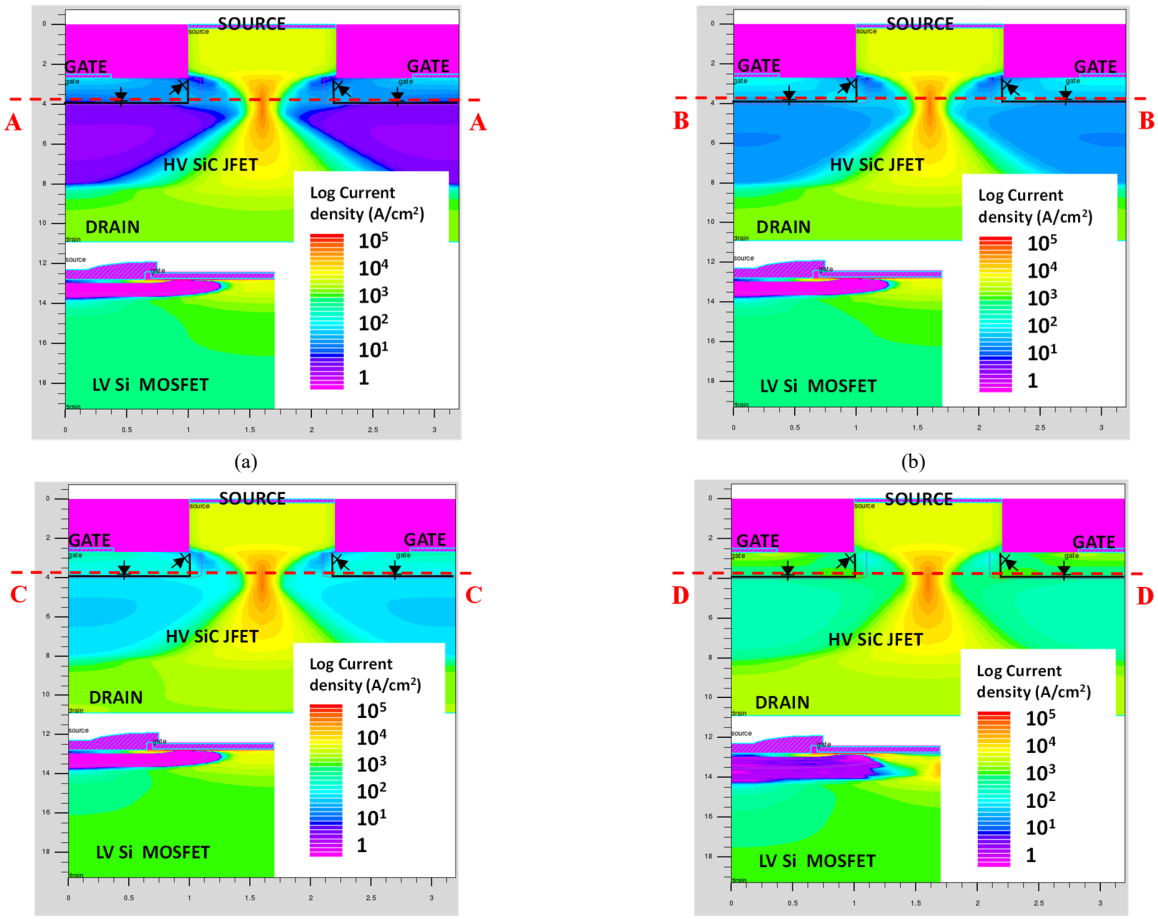


Fig. 16. 2D Current density contour plots during SC, SC pulse duration = 5 µs
(a) Time instant A (3.5 µs) (b) Time instant B (4.5 µs) (c) Time instant C (5 µs) (d) Time instant D (5.3 µs)

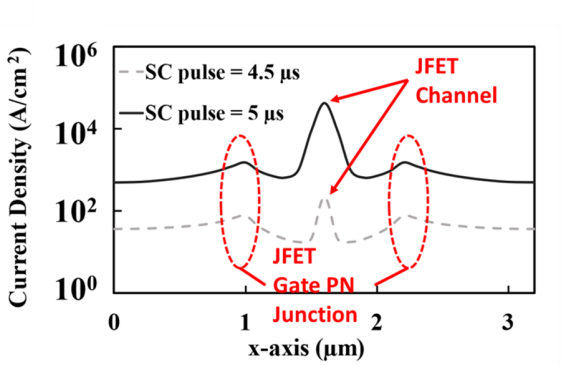


Fig. 17. Extracted total current density along cross-section cutline at time instant D (5.3 µs). SC pulses of 4.5 µs (NO FAIL) and 5 µs (FAIL)

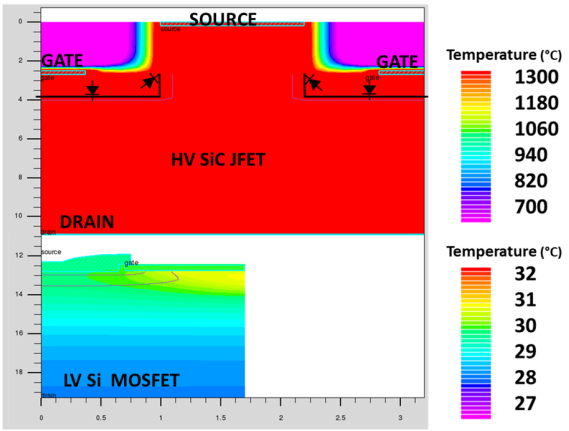


Fig.18 2D Temperature distribution plot showing JFET temperature in comparison to LV MOSFET temperature (SC pulse duration = 5 µs)

drain into the gate terminal since the LV MOSFET is off as shown in Fig.12.

Fig. 17 compares the extracted current density along the cross-sectional cutline of the JFET at the time instant D (5.3 µs), for the two evaluated cases. These cases are: (i) device failing at 5 µs and (ii) device successfully turning OFF at 4.5 µs. The highest current density, as expected is in the JFET channel and a considerable increase of the JFET gate leakage current is observed in the case of the failed device.

Fig. 18 shows the simulated temperature in the JFET and the LV Si MOSFET at time instant D (5.3 µs) for the failed case. In this case, the MOSFET hotspot temperature only experiences a

negligible increase (27 °C to 31 °C), whereas the JFET has exceeded the failure temperature for SiC and undergoes thermal failure.

IV. Conclusion

Finite element simulations and measurements show that SiC Cascode JFETs fail under with source-drain short circuit failure due to excessive leakage currents flowing through the JFET gate resulting from thermally generated carriers in the depletion region. The LV MOSFET is usually operational since it turns OFF safely while the JFET undergoes thermal runaway. The short circuit withstand time of the JFET is shown to be independent of the initial device temperature. Similar measurements performed on similarly rated silicon MOSFETs showed that the SCWT increases with temperature while in SiC Trench MOSFETs that SCWT reduces with initial device temperature. This indicates that the failure mode in SiC Cascode JFETs is independent of initial device temperature.

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