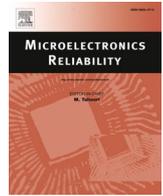




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# Benchmarking the robustness of Si and SiC MOSFETs: Unclamped inductive switching and short-circuit performance

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## ABSTRACT

The reliability and robustness of power devices are key areas of research for increasing the adoption of wide bandgap power semiconductors. This paper benchmarks the robustness under short-circuit (SC) and unclamped inductive switching (UIS) of 650 V SiC trench MOSFETs, SiC planar MOSFETs and silicon super-junction MOSFETs. The performance is characterised at 75 °C and 150 °C and the results show that the SiC MOSFETs have reduced temperature sensitivity under both SC and UIS conditions, which will be beneficial from the application point of view. In the case of the silicon MOSFET, increasing the temperature enhances the short-circuit withstand time as the peak short-circuit current is reduced. The opposite trend is observed for UIS, with a reduction of robustness as the temperature is increased. The absolute SC and avalanche energies are lower for the SiC MOSFETs, but if the chip areas are considered, the energy densities are higher in the SiC MOSFETs, with the SiC Trench having a superior critical SC energy and the SiC planar having a higher avalanche energy density. The higher critical SC and UIS energy densities in SiC MOSFETs, together with their higher thermal resistances result in higher peak junction temperatures and clear hotspots are identified using Finite Element simulations.

## 1. Introduction

The superior performance of wide bandgap (WBG) power devices like silicon carbide (SiC) and gallium nitride (GaN) has been paradigm shifting in power electronics. The adoption of SiC devices in the automotive sector has driven a golden era for WBG power electronics, with developments in traction inverters, on-board and off-board battery chargers. The benefits arising from the WBG material properties result in more compact and efficient converters, capable of switching at higher frequencies (reducing the size of the passive components) and operating at higher junction temperatures.

Other areas like rail traction, more-electric-aircraft or marine propulsion are poised to adopt SiC power devices and fully benefit from their superior properties. Nevertheless, it is not only performance that is relevant for power electronic devices. Reliability and robustness are paramount and there have been numerous challenges for SiC power devices. The different thermomechanical properties of SiC chips require the development of suitable packaging methods [1], the increased defect density in the gate oxide and interface contributes the higher threshold voltage instability in SiC MOSFETs [2] and suitable qualification and

characterisation methods are required for SiC and GaN devices, as defined by the JEDEC JC-70 committee.

Single event robustness is a key test for power devices. This is assessed using both short-circuit (SC) and unclamped inductive switching (UIS) tests. In these tests, the power devices are subjected to both high current and high temperature and the ability of the device to withstand such events is benchmarked.

This paper investigates and compares the SC and UIS performance of a 650 V SiC trench MOSFET, a 650 V SiC planar MOSFET and a 650 V Si super-junction (SJ) MOSFET at different junction temperatures. The characteristics of the devices are summarised in Table 1, where the chip area was extracted after opening the TO-247 package.

The higher critical electrical field in SiC means that SiC devices have a lower resistance than their silicon counterparts, as a thinner drift layer is required for enabling the blocking voltage capability. The lower specific ON-state resistance in SiC MOSFETs [3] means that for the same ON-state resistance, SiC chips will be smaller. This reduced chip size will mean higher thermal resistances as well as higher current densities in abnormal conditions like UIS or SC. The objective of this study is comparing and benchmarking the impact of the material properties on

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**Table 1**  
Device characteristics.

	SiC trench	SiC planar	Si MOSFET
Current rating (A) @ 100 °C	21	16	21
ON-state resistance (mΩ) @ 100 °C	91	135	136
Thermal resistance (K/W)	0.86	1.53	0.45
Input capacitance (nF)	0.571	0.64	3.454
Chip size (mm <sup>2</sup> )	6.25	2.89	31.6

the single event robustness of a series of Si and SiC MOSFETs, hence figures of merit will be used in addition to the conventional metrics.

## 2. Short-circuit performance of Si and SiC MOSFETs

The ability of a power device to withstand SC events is an important robustness metric, with the maximum short-circuit withstand time (SCWT) usually provided in the datasheets of the devices. Nevertheless, for comparing the performance of different device technologies under SC other metrics like the SC energy density, the impact of temperature or the failure mechanism are required.

### 2.1. Experimental setup

The SC test performed in this paper is Hard-Switching-Fault (HSF) [4] and the electrical schematic is shown in Fig. 1. In this setup a control IGBT (with a current rating greater than the SC current of the device under test (DUT)) is used for achieving a non-destructive short-circuit [5].

For these investigations, the DC link ( $V_{DC}$ ) was set at 400 V and the DUT was driven using the recommended gate voltage. The parasitic elements in the circuit are responsible for the overshoots and dips of the drain-source voltage during the SC test, as shown in Fig. 2. The drain current  $I_D$  is measured using a Rogowski coil and the drain-source voltage  $V_{DS}$  using a high voltage differential voltage probe. The characteristic tail current (SC degradation indicator in SiC MOSFETs [4,5]) is observed.

The robustness of the devices under SC was evaluated at two different case temperatures (75 °C and 150 °C). These temperatures were defined using a small electric heater attached to the device, allowing enough time to reach thermal equilibrium. The maximum SCWT was determined increasing the duration of the short-circuit until failure. To minimise the impact of self-heating, enough recovery time (5 min) is left between consecutive SC events.

### 2.2. Results and analysis

To perform this analysis 3 devices of each technology were characterised until failure at each temperature to account for statistical

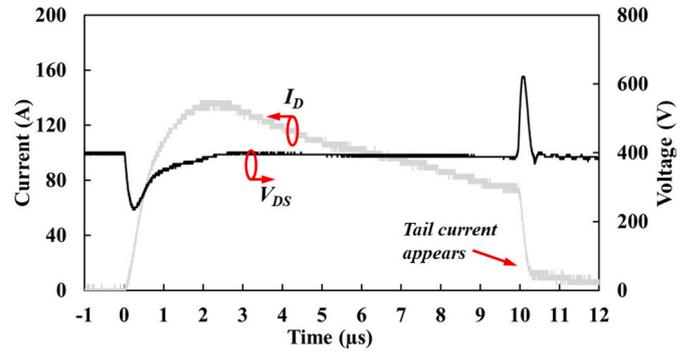


Fig. 2. SC transient waveforms.

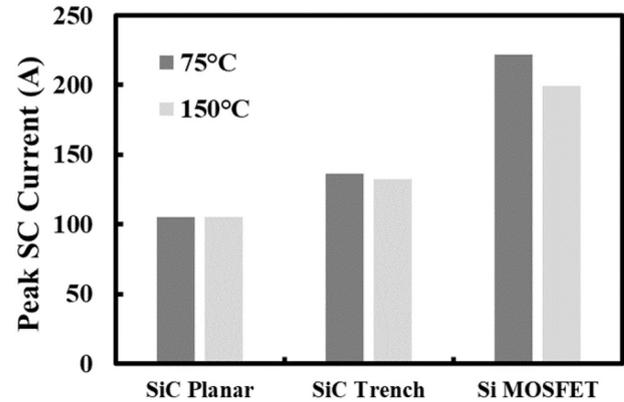


Fig. 3. Peak SC current.

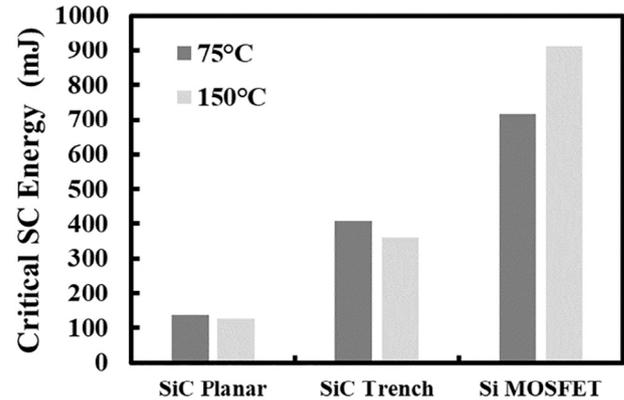


Fig. 4. Critical SC energy.

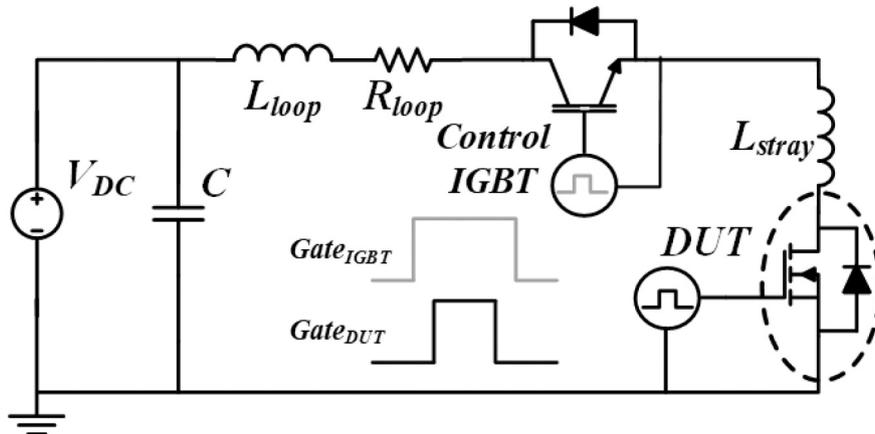


Fig. 1. SC test schematic.

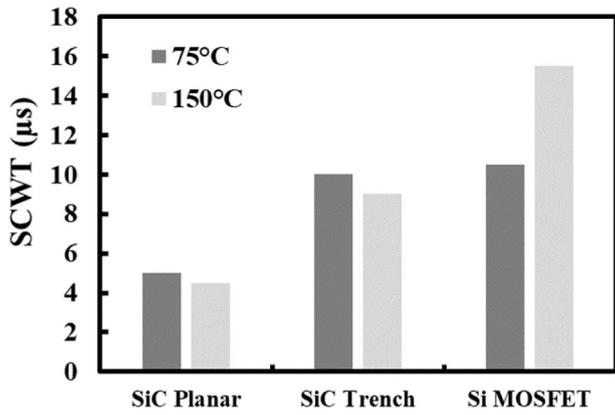


Fig. 5. Short-circuit withstand time.

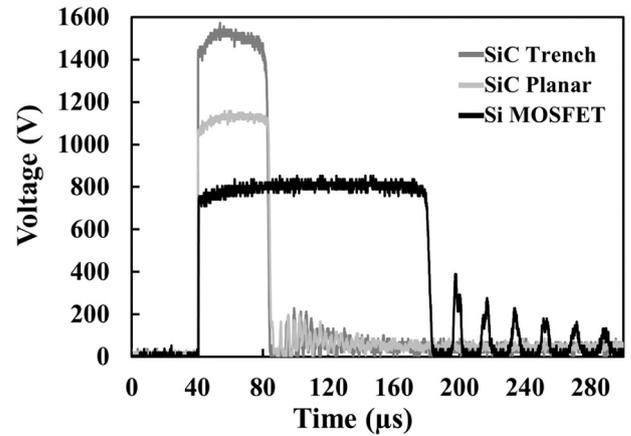


Fig. 8. Drain-source voltage transients during UIS.

Table 2  
Failure mechanisms under SC.

	Failure mechanisms
Si MOSFET	Gate-source (shorted), drain-source (shorted)
SiC planar MOSFET	Gate-source (shorted), drain-source (OK)
SiC trench MOSFET	Gate-source (shorted), drain-source (OK)

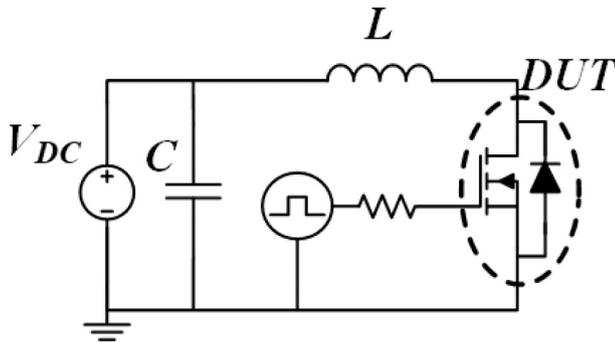


Fig. 6. UIS test schematic.

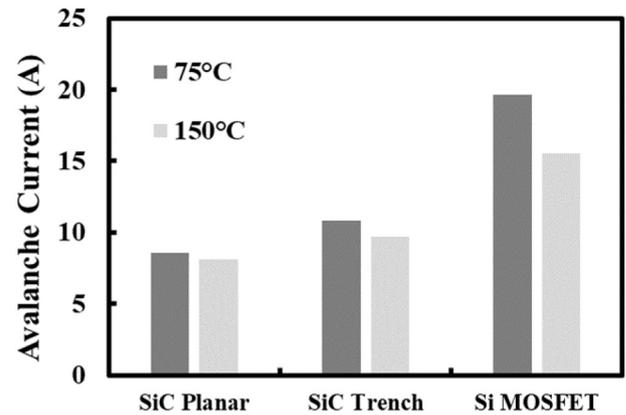


Fig. 9. Peak avalanche current (last pass).

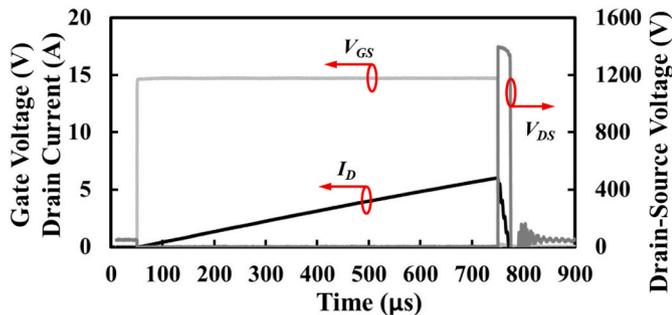


Fig. 7. Example of UIS waveforms.

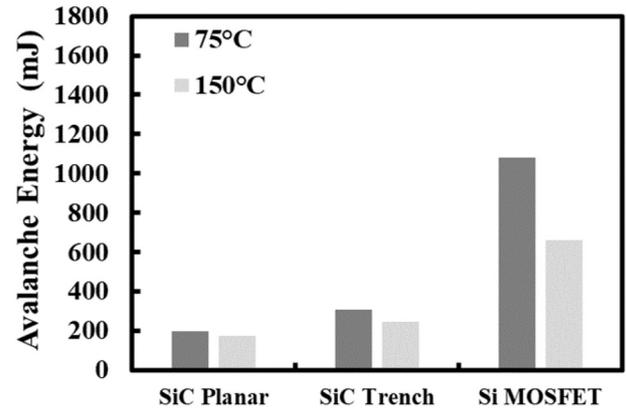


Fig. 10. Avalanche energy (last pass).

dispersion. The mean values of the last pass measurement are used for the analysis. The results, shown in Figs. 3 to 5 include the peak short-circuit current, SCWT and SC energy.

The failure mechanisms for the SC tests are summarised in Table 2.

### 3. Unclamped inductive switching performance of Si and SiC MOSFETs

Another important test to benchmark the robustness of power

devices is unclamped inductive switching (UIS). In this test the power device is also simultaneously subjected to high current and high voltage and both the design of the device (susceptibility of the parasitic BJT to latching) and power dissipation can be evaluated [6] (Fig. 6).

#### 3.1. Experimental setup

UIS tests were performed using the test circuit shown in Fig. 7. In this test, the DUT is triggered with a gate pulse of a defined duration and the inductor  $L$  is charged at a current rate defined by  $V_{DC}/L$ , where  $V_{DC}$  is the DC link voltage. When the DUT is turned OFF, the energy stored in the

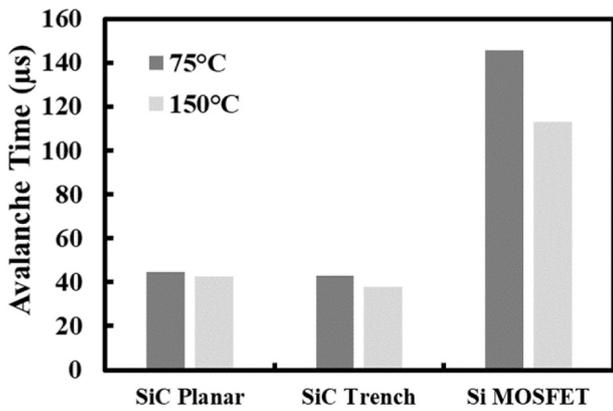


Fig. 11. Avalanche time (last pass).

Table 3  
Failure mechanisms under UIS.

	Failure mechanisms
Si MOSFET	Gate-source (shorted) drain-source (shorted)
SiC planar MOSFET	Gate-source (shorted) drain-source (shorted)
SiC trench MOSFET	Gate-source (shorted) drain-source (shorted)

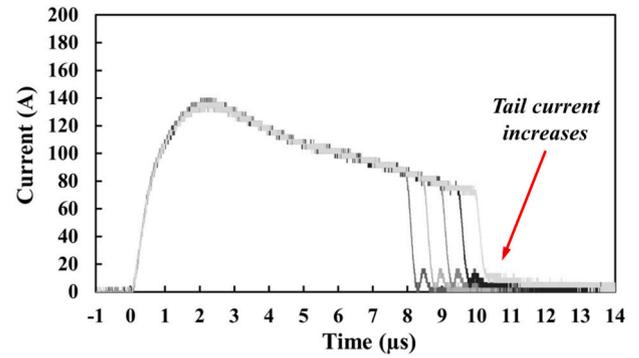


Fig. 13. Impact of increasing the SC time – SiC trench – Drain current.

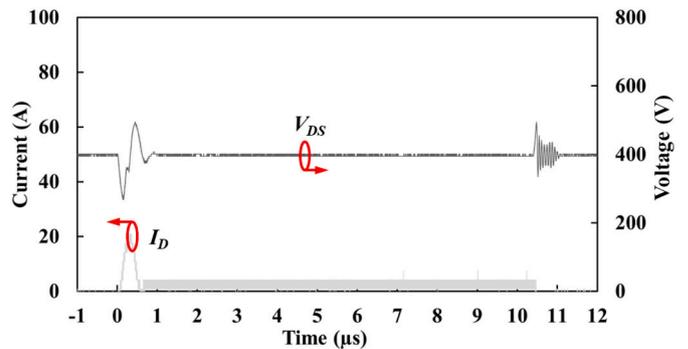


Fig. 14. SiC trench MOSFET after SC failure. Drain current and drain-source voltage transient.

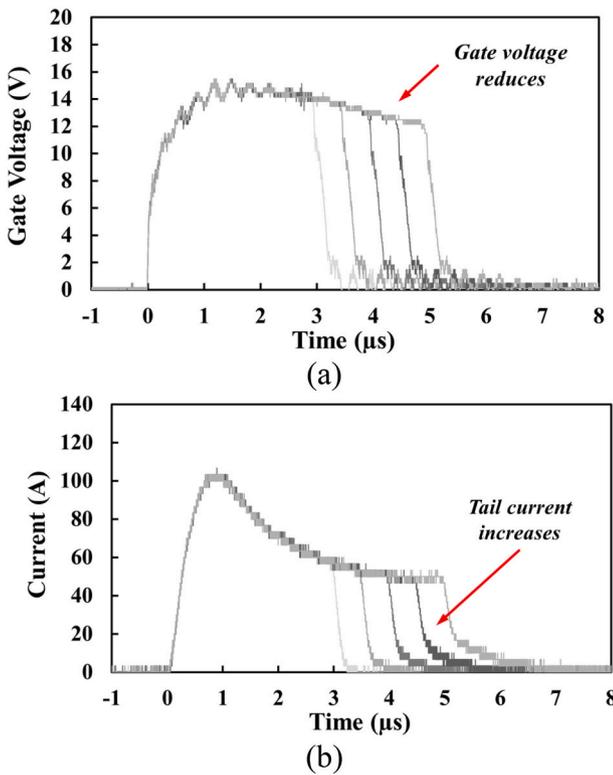


Fig. 12. Impact of increasing the SC time – SiC planar. (a) Gate voltage (b) drain current.

inductor flows through the DUT as an avalanche current via impact ionisation. The drain-source voltage rises to the breakdown voltage  $V_{BR}$  of the device and a high energy is dissipated (Fig. 8). For the circuit in Fig. 7, this energy ( $E_{AV}$ ) can be calculated using Eq. (1). The avalanche time  $t_{AV}$  [7] depends on the inductor size and peak avalanche current  $I_{AV}$  (Eq. (2))

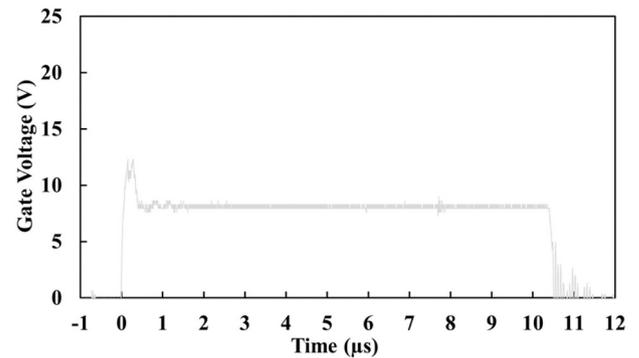


Fig. 15. SiC trench MOSFET after SC failure. Gate voltage transient.

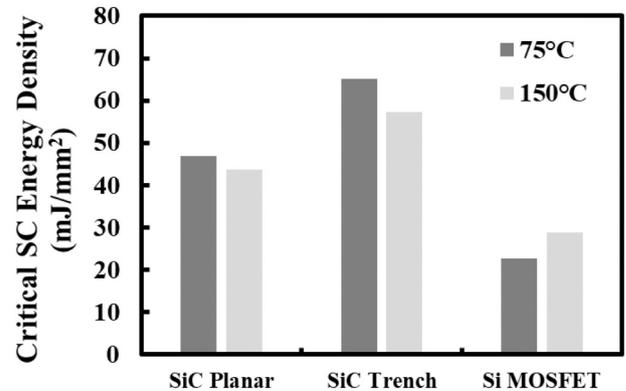


Fig. 16. Critical SC energy density.

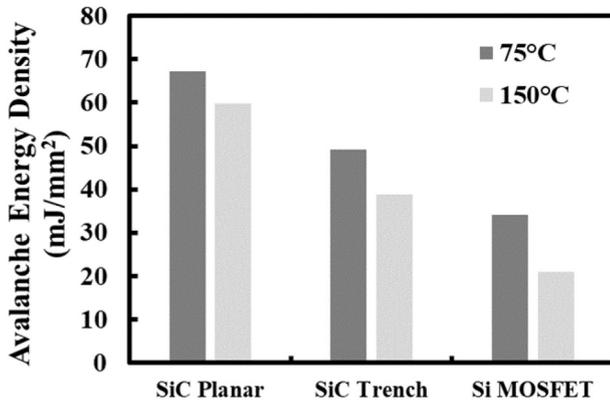


Fig. 17. Avalanche energy density (last pass).

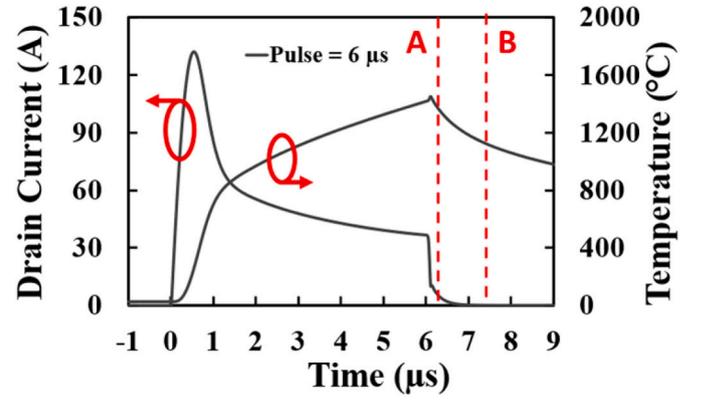


Fig. 20. FE modelling of SC – SiC planar – Drain current transient and junction temperature.

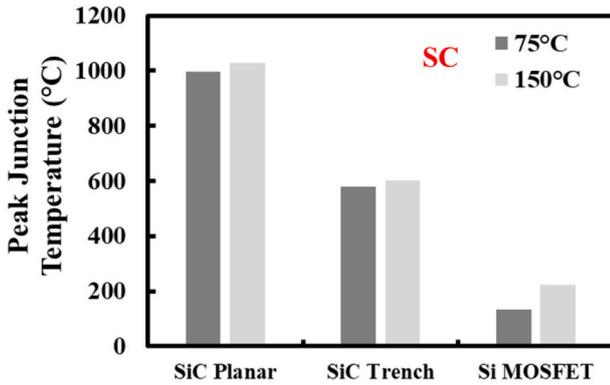


Fig. 18. Estimated peak junction temperatures during SC.

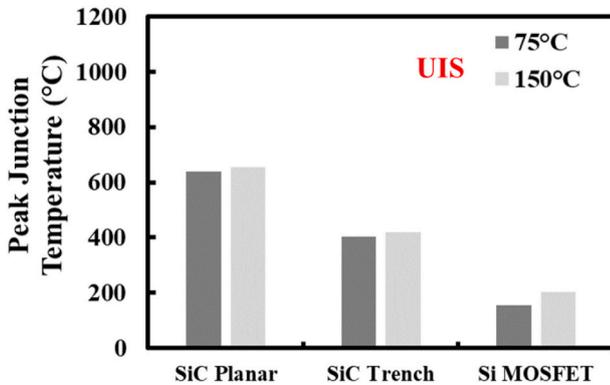


Fig. 19. Estimated peak junction temperatures during UIS.

$$E_{AV} = \frac{1}{2} \frac{L \cdot I_{AV}^2}{1 - \frac{V_{DC}}{V_{BR}}} \quad (1)$$

$$t_{AV} = \frac{I_{AV} \cdot L}{V_{BR} - V_{DC}} \quad (2)$$

The ruggedness of the devices was benchmarked at 75 °C and 150 °C. The value of the DC link voltage was 50 V, the inductor selected was 6 mH (to evaluate power dissipation during UIS) and the duration of the pulse was increased until the device failed, leaving enough time between UIS events to minimise the impact of self-heating.

### 3.2. Results and analysis

As in the case of SC benchmarking, 3 devices of each technology were characterised until failure at each temperature. The devices evaluated in this study are 650 V rated devices, however the measured  $V_{BR}$  values were around 1500 V for the SiC trench MOSFET, around 1050 V for the SiC planar MOSFET and 815 V for the silicon device, as shown in Fig. 8. This is a well-known characteristic of SiC MOSFETs, where the real breakdown voltage is higher than the rated drain-source voltage, with 1200 V devices having a  $V_{BR}$  of around 1700 V [6,8].

The last pass results, shown in Figs. 9 to 11, include the last pass avalanche peak current  $I_{AV}$ , the critical avalanche energy and avalanche time. The failure mechanisms for the UIS tests are summarised in Table 3.

## 4. Discussion and thermal analysis

Comparing both technologies, the first remarkable difference is the reduced temperature sensitivity of SiC MOSFETs under SC and UIS. The wide bandgap properties of SiC are the reason behind this reduced temperature sensitivity, with only a slight reduction of the SC and UIS robustness as the temperature increases from 75 °C to 150 °C, for both the planar and the trench SiC MOSFETs.

At 75 °C the selected SiC trench MOSFET has a SCWT time comparable to the evaluated silicon MOSFET, however when the temperature is increased to 150 °C, the reduction of the short-circuit current causes an increase of the SCWT for the Si MOSFET (Fig. 5). The selected SiC planar MOSFET has a reduced SCWT compared to both the Si MOSFET and the SiC Trench MOSFET.

Two degradation mechanisms were observed in SiC MOSFETs as the SC pulse was increased: (a) the progressive reduction of the effective gate voltage and (b) the appearance and gradual increase of a tail current [9]. This is shown in Fig. 12 for the SiC planar MOSFET, where a reduction of the effective gate voltage of around 2.5 V is observed. This effective gate voltage reduction is caused by the increase in the gate leakage current as the temperature of the device increases [10]. The tail

Table 4  
FE simulation parameters.

Parameter	Planar MOSFET
Source doping (cm <sup>-3</sup> )	1 × 10 <sup>19</sup>
Channel length (µm)	0.3
Drift layer thickness (µm)	8.5
Drift layer doping (cm <sup>-3</sup> )	1.5 × 10 <sup>15</sup>
Drain doping (cm <sup>-3</sup> )	1 × 10 <sup>19</sup>
P-body doping (cm <sup>-3</sup> )	1.5 × 10 <sup>17</sup>
Oxide thickness (nm)	50

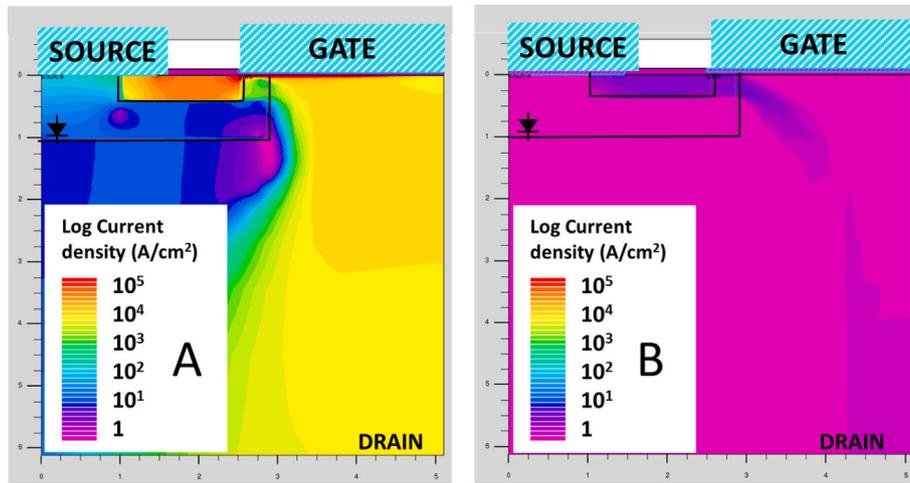


Fig. 21. SiC planar MOSFET. Log current density (FE).

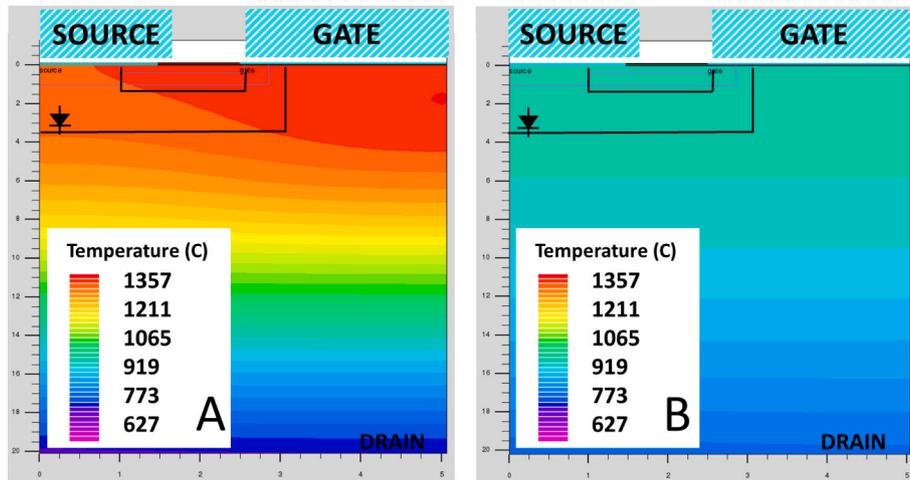


Fig. 22. SiC planar MOSFET. Temperature (FE).

current was not as apparent in the SiC trench as in the SiC planar MOSFET, as shown in Fig. 13, with just a small increase. These two features were not observed in the Si MOSFET.

Considering the failure mechanisms, the most remarkable difference, is the “soft-failure” [11] observed in the SiC MOSFETs (gate-source shorted and the capability of blocking voltage intact). This is shown in Fig. 14, which shows the applied gate pulse after the last pass. This figure shows how the device is still blocking the DC link voltage but is not conducting a SC current, with only a few amps flowing through the device. Fig. 15 shows that the applied gate voltage is considerably reduced because of the increased gate leakage current (gate oxide damaged during the SC tests [10]). The lower effective gate voltage causes the partial turn-ON of the SiC MOSFET (high drain-source resistance) and the drain current is limited.

Focusing on the UIS results the opposite trend is observed, with a reduced UIS capability of the Si MOSFET as the temperature is increased. Fig. 10 shows that the avalanche critical energy reducing around a 40 % in the Si MOSFET, whereas in the case of the SiC MOSFETs, the impact of temperature is marginal with only a slight reduction.

The reduced size of the SiC chips (approximately 1/5 of the Si chip in the case of the SiC trench MOSFET and 1/11 in the case of the SiC planar) plays a key role on the avalanche and SC ruggedness of the devices and the apparently reduced avalanche ruggedness of the SiC MOSFETs is balanced when the area is taken into consideration. This is

shown in Figs. 16 and 17, where the SC and avalanche energy densities have been calculated dividing the SC energy and avalanche energy by the chip area.

Figs. 16 and 17 show that the energy densities are higher in SiC MOSFETs, with the SiC trench MOSFET outperforming the other devices under SC conditions and the SiC planar MOSFET having the best avalanche energy density capability.

The devices have different thermal resistances, and this will be reflected in the peak junction temperature  $T_{J-PEAK}$ . Using the thermal network provided in the datasheets and the measured SC and avalanche power, the  $T_{J-PEAK}$  values have been calculated and they are shown in Fig. 18 for the SC test and Fig. 19 for the UIS test.

The results show that the reduced chip size and the higher energy density cause higher  $T_{J-PEAK}$  values in the SiC planar MOSFET, especially during SC events. These higher temperatures can explain the failure precursors observed in Fig. 12.

For pulses shorter than 100  $\mu$ s the estimated junction temperatures may not be accurate due to the lack of information in the datasheets. Additionally, these values may not be representative of the hotspots within the cell structure, especially considering the SCWT of 5 to 10  $\mu$ s. To evaluate these hotspots, Finite Element (FE) modelling is paramount [12]. A FE simulation of a SiC planar MOSFET was performed using SILVACO, with the model parameters given in Table 4. The SC transient results are shown in Fig. 20, for a SC time of 6  $\mu$ s and a DC link of 400 V.

Two points of interest are considered: A - Peak junction temperature and B - during the tail current phase. The 2D log current density and temperature distribution are shown in Figs. 21 and 22 respectively. The FE results show how the temperature rises to 1300 °C, and the SC is successfully interrupted. The temperature hotspot is identified below the gate terminal (which was identified as the failure mechanism in the experiments). A current flowing through the channel is observed in Fig. 21(B), explaining the origin of the tail current, in agreement with [9].

## 5. Conclusion

This paper has evaluated the SC and UIS performance of a SiC planar MOSFET, a SiC Trench MOSFET and a silicon SJ MOSFETs. The results show that the SiC MOSFETs have a reduced temperature sensitivity under both SC and UIS conditions. The absolute SC and avalanche energies are lower for the SiC MOSFETs, but if the chip areas are considered, the energy densities are higher in the SiC MOSFETs, with the SiC Trench having a superior critical SC energy density and the SiC Planar having a higher avalanche energy density. FE modelling is used to identify hotspots near the gate of the SiC planar MOSFET.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Acknowledgement

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