Characterization of Integrated Bipolar Transistors using Computer Aided Measurements and Optimisation.

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To Kamila,

Rowayda

and Ahab.

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DECLARATION

This work was solely mine except where acknowledged. This thesis has not been submitted to any other University for a degree.

Some of the material presented in this thesis has been published, in Electronics Letters in 1976., or will be published in the near future.

ABSTRACT

The objective of this thesis was to develop a method for measuring integrated bipolar transistors forming part of an integrated circuit chip. These integrated circuits were produced at Plessey, Caswell. The measurement technique was then used to investigate the validity of the equivalent circuit at present used by Plessey's, over the frequency range up to and beyond f_T. The measuring system was based on the Hewlett Packard microwave network analyser.

A computer aided correction program has been implemented for calibrating the measuring system. This establishes the measurement plane at the terminals of the device, eliminating all the parasitic components.

For calibrating the measuring system, purpose made standards of chip size were made. Ideally one of these would be a perfect matched load. This is difficult to achieve at microwave frequencies. Instead, a thin-film resistor was used. This was characterized and its frequency dependence taken into account in the calibration program.

Using the above computer aided system, the complex S-parameters of the integrated bipolar transistors were measured at several bias conditions. Optimization was used to obtain values for the equivalent circuit from the measured S-parameters.

An appropriate objective function with suitable boundary conditions has been formulated in terms of the measured S-parameters and those calculated from the equivalent circuit.

The component values of the equivalent circuit which give agreement between the measured and calculated S-parameters have been obtained by applying the Hooke and Jeeves optimization routine to minimize the objective function.

CHAPTER 1

INTRODUCTION

This thesis presents a detailed study of a shallow diffused n-p-n integrated circuit bipolar transistor produced at Caswell on Plessey's Bipolar Process III in terms of its small-signal equivalent circuit. The small-signal characteristics are studied in terms of a modified hybrid-Π equivalent circuit produced by the circuit analysis group at Caswell, Plessey, and computer calculations to determine the transistor performance. These integrated bipolar transistors have been chosen for analysis as they have f_T of approximately 2.5 GHz, high gain and low noise figure.

Although microwave transistors have been commercially available for several years, there have been few publications on the accurate characterization of these type of transistor in terms of their small signal properties. Better transistor models are needed to evaluate more precisely the predicted performance at microwave frequencies or at frequencies near f_T. The advantage of computer-aided-circuit design has made it feasible to increase the complexity of both transistors and their small-signal equivalent circuit and still carry out successfully the evaluation of transistor performance.

Formerly, the y, z or h-parameters have been employed to describe transistors at frequencies up to their f_T. Such parameters are not valid at these frequencies as they are measured at frequencies well below f_T. A method of circumventing this has been the use of scattering parameters (S-parameters).

To measure accurately the S-parameters of a device, a reference plane has to be established at its terminals. In order to maintain the above, a computer aided correction program is needed.

Several computer-aided correction programs have been implemented and successfully applied to calibrate the measuring system up to the transistor-package terminals and then measure the S-parameters of a device. It has been difficult to extend the reference plane of measurements up to the device terminals in applying the above computer aided correction programs. This is due to the limited space available in the measuring jig in order to accommodate the standard terminations. If the reference plane is established away from the device terminals, the measured S-parameters will include certain errors. These errors arise from the external connections between the device terminals emitter, base and collector and the corresponding device-package leads. These errors are also due to the pad-capacitance between the device terminals.

1.1. Small Signal Equivalent Circuit.

The conventional hybrid-Π is a poor representation for an integrated circuit transistor at microwave frequencies. A more accurate transistor model is needed to represent the physical behaviour of these transistors at microwave frequencies or frequencies close to f_T of the specified transistor. In addition, for many purposes, a simpler equivalent circuit allowing the designer greater use of intuition is needed at the expense of some accuracy.

Of course, the cruder the approximation, the simpler the equivalent circuit becomes. It is therefore a matter of engineering judgement to decide when we have a reasonable compromise between accuracy and simplicity.

In Chapter 2, the author presents a complete study for an integrated bipolar transistor and shows, in brief, the derivation of its equivalent circuit using the physical properties of the various materials used in the transistor.

Also in Chapter 2, the author presents a simple procedure for determining a simpler equivalent circuit model and shows it to be sufficiently accurate for most applications at frequencies up to f_T. Its various components are fully studied and conditions for its use are also given. A new Π-equivalent circuit model, which is simple and reasonably accurate for the integrated bipolar transistor studied, is implemented.

1.2. S-Parameters

The S-parameters describe the transmission and reflection of power into and out of a microwave network such as a transistor. The S-parameter measurements are carried out with the transistor embedded in a coaxial transmission line system of a characteristic impedance of 50Ω. An automatic network analyser system is normally used in such measurements.

Before commencing S-parameter measurements on the transistor, the reference plane of measurements has to be established at the transistor terminals and the network analyser has to be calibrated up to this plane. For the measurements on transistors, the author will establish the reference plane of measurements at the transistor terminals to eliminate the pad-capacitance and the parasitic effects of the external leads, from the measured S-parameters. The computer aided correction program needed to calibrate the measuring system up to the transistor terminals is implemented and fully discussed in Chapter 3. One of the calibrating standards required by this computer aided correction program is a matched load. Perfect matched loads are difficult to obtain at microwave frequencies. Hence, a thin-film load resistor, which instead can be used as a calibrating standard, is characterized from d.c. up to 8.0 GHz and its frequency dependence is obtained in Chapter 4.

1.3. Transistor-Package

Microwave semiconductor chip-devices such as transistors are usually mounted in standard packages such as H.P. K-disc strip line headers. The integrated bipolar transistors to be characterized in this thesis are in chip form. In Chapter 5, a special transistor-package is designed. This is to protect the transistor chip and to facilitate measurements. As the transistor chips vary in size, the transistor-package is designed with a number of different layouts.

1.4. S-parameter Measurements

In Chapter 6, the small signal y-parameters are calculated from the equivalent circuit derived in Chapter 2, and then the S-parameters are obtained from y-s transformation equations. Hence, the S-parameters are formulated in terms of the physical properties of the transistor. Also in Chapter 6, the S-parameters of the transistor are measured applying the computer aided correction program of Chapter 3. A similar thin-film resistor to that characterized in Chapter 4, is used as a terminating load in calibrating the measuring system. The measured S-parameters are compared with the calculated ones. This is to show the accuracy with which the integrated transistor is represented by the small signal equivalent circuit model of Chapter 2.

1.5. Equivalent Circuit Parameters Optimization

The agreement between the measured and calculated S-parameters of Chapter 6 was found not satisfactory at frequencies up to f_T. This is because some parameter values were approximately estimated at frequencies well below f_T. Others were estimated from the measured results. These factors are fully discussed in Chapter 2.

More accurate equivalent circuit parameter values are needed to reasonably match the measured and calculated results at specific bias conditions.

In Chapter 7, an optimization routine is applied using the theoretically calculated S-parameters of Chapter 6 to obtain component values for the equivalent circuit, which originally gave the calculated S-parameters, and hence ensuring the capabilities of the optimization routine.

The above optimization routine is also applied in Chapter 8 to obtain from the measured transistor S-parameters the complete equivalent circuit component values. These also give a good agreement between the measured and optimized S-parameters of the specified transistor under some boundary conditions.

A Thesis conclusion is given in Chapter 9.

CHAPTER 2

INTEGRATED BIPOLAR TRANSISTOR CIRCUIT MODELS

2.1. Introduction

In various equivalent circuit representations which have been proposed before, T-equivalent or Π-equivalent circuit representations have been used to represent the physical behaviour of the transistor[2(6,14)]. The component values of these models were obtained at frequencies well below f_T and they have been kept constant in calculating the transistor performance at microwave frequencies or frequencies close to f_T. Thus, the validity range of the above models is for frequencies smaller than f_T.[2(15)]

The conventional hybrid-Π or T-models are very poor representations for integrated transistors at microwave frequencies. The incremental hybrid-Π model for an npn transistor is sufficiently complicated at microwave frequencies, that a calculation of the circuit performance in full generality would be tedious and relatively unrewarding. Hence, it is necessary to make approximations. Of course, the cruder the approximation, the simpler the equivalent circuit becomes. It is, therefore, a matter of engineering judgement to decide when we have a reasonable compromise between accuracy and simplicity. Consequently, a modified hybrid-Π model is needed here to represent the physical behaviour of the transistor at microwave frequencies, at which the transistor will be measured.

Attention has to be given to the evaluation of the parasitic elements which degrade the high frequency response of the transistor.

The objective of this study is to investigate the frequency range validity of the modified hybrid-Π model, and to produce a simple and sufficiently accurate equivalent circuit model for the integrated transistors at frequencies near to and above f_T.

In this thesis, the Plessey Process III integrated bipolar transistor type SB630, has been chosen for characterization. This type of transistor has $f_T \simeq 2.5$ GHz, high gain and low noise figure. A modified hybrid-Π model will be used to represent the physical behaviour of this transistor. The various component values of this model, except the emitter junction capacitance $C_{b'e}$, were obtained from low frequency measurements performed on the transistor at Caswell, Plessey. A new method of evaluating $C_{b'e}$ from the measured f_T will be described.

Also, a simplified equivalent circuit model which is sufficiently accurate to represent the specified transistor will be deduced. The conditions under which this model is valid will be given. The effect of the collector spreading resistance R_c, normally neglected, will be studied as this resistance makes a major contribution to the measured value of f_T.

2.2. Integrated Bipolar Transistor Equivalent Circuit.

Integrated bipolar transistors differ mainly in the means by which isolation is achieved between devices, and also in size and geometry. The most frequently used structure is the P-N. junction isolation diffused epitaxy and is shown in Fig. 2.5.b. Base and emitter regions are formed by a double diffusion process. The base is normally formed by a shallow, heavy diffusion followed by a drive-in step which reduces the surface concentration and increases the junction depth.

The emitter diffusion is then done at high surface concentration. This diffusion process tends to give a Guassian distribution of impurities for the base diffusion and complementary error function distribution for the emitter diffusion.[2(1)].

A typical impurity profile for an n-p-n transistor is shown in Fig. 2.1[2(2)]. Because electron mobility is larger than hole mobility, differences in the diffusion of P-type and n-type impurities, and due to the positive oxide charge Q_{ss}, npn transistors have better high frequency

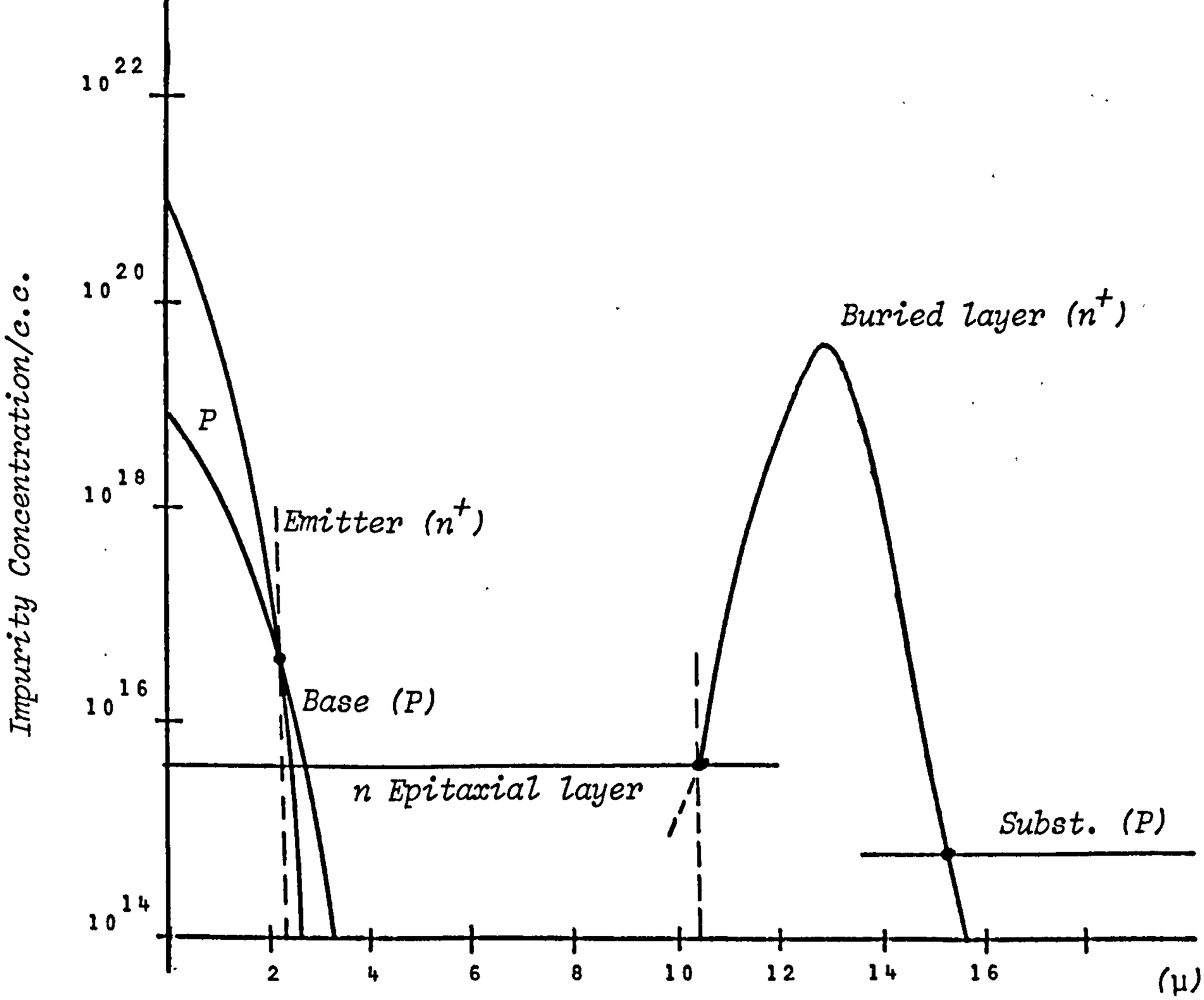


Fig. 2.1. Doping Profile for a npn diffused epitaxy integrated transistor

response than pnp transistors and are almost idealy suited for integrated circuits.

2.2.1. Derivation of an Equivalent Circuit Model Using The Transistor Geometry.

A number of methods could be used to derive an equivalent circuit for the transistors; it is believed that the best method is to derive the circuit elements in terms of the physical processes occuring in the transistors. To simplify the derivations, the electron density distribution in the base region is assumed to be linear, which is valid for microwave transistors.

The change in the distribution of the electron density in the base region of the intrinsic transistor, shown dotted in Fig. 2.5.b, caused by the change of the emitter-active base voltage $\Delta V_{EB'}$, with the collector-base voltage constant ($\Delta V_{C'B'} = 0$) is shown in Fig. 2.2.a. The change due to $\Delta V_{C'B'}$, which effectively reduces the base width W_B, with $\Delta V_{EB'} = 0$, is shown in Fig. 2.2.b.

At low level injection, the collector current I_c flows by diffusion and is given by

$$I_c \simeq qA_E D_n \frac{n(0)}{W_B} \qquad 2.1.$$

where, q is the electronic charge, A_E is the emitter area, D_n is diffusivity of electrons and,

$$n(0) = \frac{n_i^2}{N_{AB}} . \quad EXP \left(\frac{qV_{EB'}}{KT}\right) \qquad 2.2.$$

where, N_{AB} denotes the average acceptor concentration in the base region, n_i is the intrinsic concentration, K in Boltzmann's constant and T is the absolute temperature.

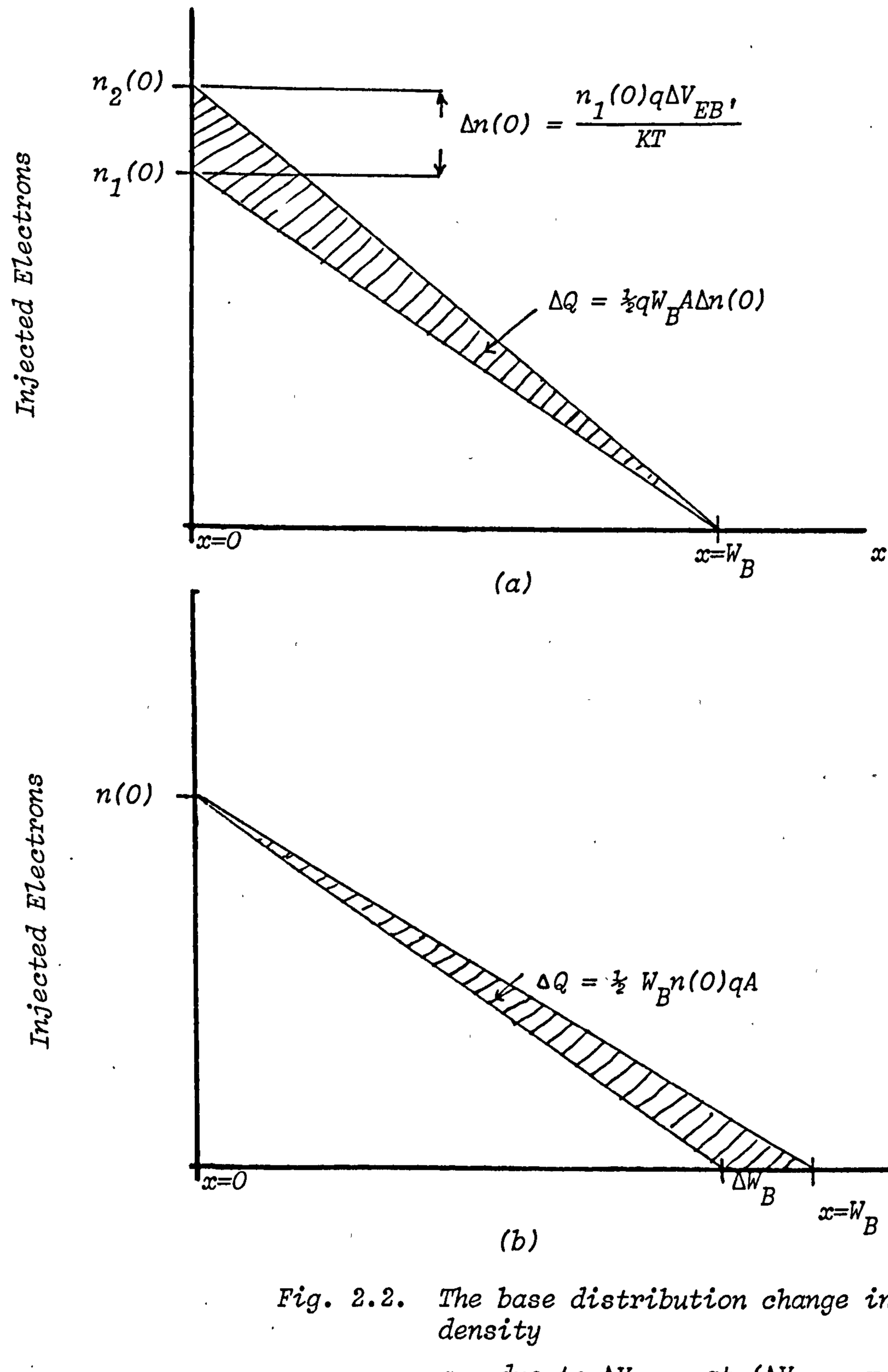


Fig. 2.2. The base distribution change in electron density

a. due to $\Delta V_{EB'}$, at $(\Delta V_{B'C'} = 0)$

b. due to $\Delta V_{B'C'}$, at $(\Delta V_{EB'} = 0)$

Referring to Fig. 2.2.a, the change in the electron density at the emitter junction is,

$$\Delta n(0) = \frac{n_1(0)q}{KT} \cdot \Delta V_{EB'} \qquad 2.3.$$

and, the change in the stored charge in the base region is,

$$\Delta Q = \tfrac{1}{2}.q.W_B A_E.\Delta n(0) \qquad 2.4.$$

The change in the collector current ΔI_c can be obtained using Equations 2.1 - 2.3. Giving,

$$\Delta I_c = \frac{qI_c}{KT} \cdot \Delta V_{EB'} \qquad 2.5.$$

We note from the above equation that qI_c/KT represents the transconductance $\Delta I_c/\Delta V_{EB'}$, g_{m1} of the transistor.

In n-p-n transistors electrons flow out of the base terminal giving the base current I_B; and due to $\Delta V_{EB'}$ this current has to change by ΔI_B to account for the following four basic physical effects:[2(3)]

1) Increase of recombination between electrons and holes in the base region due to the excess electrons injected from the emitter. This requires a base current $\Delta I_{BR} = \frac{\Delta Q}{\tau_o}$, where τ_o is the life time of the electron in the base region.

2) Increase of hole current across the emitter requires extra base current I_{BE} given by: $\Delta I_{BE} = q.A_E.D_P.N_{AB}.\Delta n(0)/W_E N_{DE}$, in which D_P is the diffusivity of holes, W_E is the emitter width and N_{DE} is the average impurity density in the emitter region.

3) Increase of the stored hole density in the base region, to maintain charge neutrality, requires transient base current $\Delta I_{BS} = \Delta Q/\Delta t$. This can be considered as charging a base diffusion capacitance.

4) In addition, the base has to supply a transient current needed to charge the transition emitter capacitance C_{TE}, where per unit area of emitter C_{TE} is the semi-conductor permitivity divided by depletion region width. Giving:

$$\Delta I_{BE} = C_{TE} \cdot \frac{d}{dt} (\Delta V_{EB'})$$

Collecting the above four components of the base current gives:

$$\Delta I_B = \Delta V_{B'E}/R_e + C_{B'E} \frac{d}{dt} (\Delta V_{B'E}) \qquad 2.6.$$

where,

$$C_{B'E} = C_{TE} + C_D$$

$$1/R_e = \frac{D_P W_B N_{AB} \cdot g_m}{D_n W_E N_{DE}} + \frac{C_D}{\tau_o}$$

and C_D is the diffusion capacitance and is given by $g_m \cdot W_B^2/2D_n$.

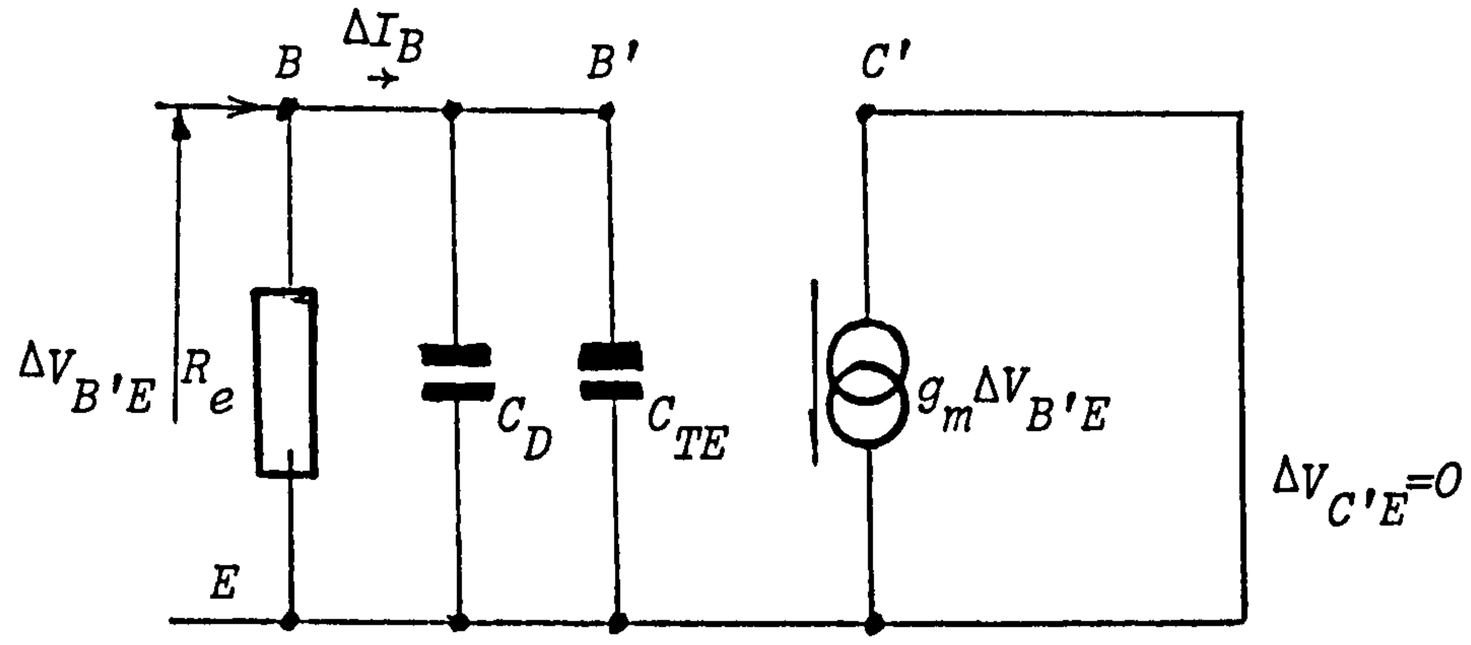
Equations 2.5 and 2.6 can be represented by the equivalent circuit shown in Fig. 2.3.a.

The primary result of a change in the emitter-base voltage is to change the current levels of a transistor. The secondary mechanism of base width modulation due to a change in the collector-base voltage $V_{C'B'}$ is to cause further variations in current levels. These variations have to be represented by additional elements in the equivalent circuit of Fig. 2.3.a.

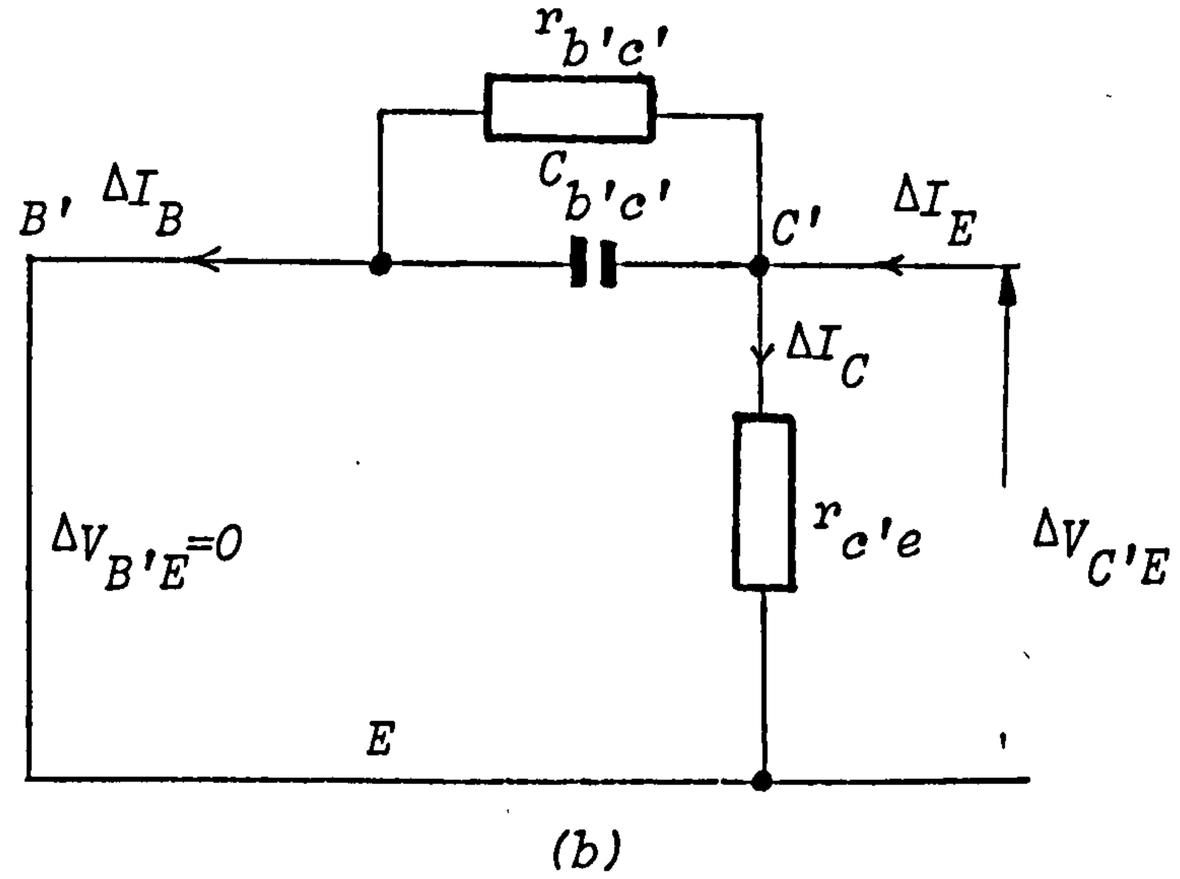
Fig.2.2.b. illustrates the effect of base width modulation on the distribution of the electron density in the base region.

Following a similar procedure to the above, we get

$$\Delta I_C = \Delta V_{C'B'}/r_{c'e} \qquad 2.7.$$



(a)



(b)

Fig. 2.3. The Equivalent Circuit Yielding ΔI_B, and ΔI_C

a. Due to $\Delta V_{B'E}$ only.

b. Due to $\Delta V_{C'B'}$ only.

in which, $r_{c'e}$ is the output resistance and is given by,

$$r_{c'e} = - \frac{I_c}{W} \frac{dW_B}{dV_{C'B'}}$$

and,

$$\Delta I_B = \Delta V_{C'B'}/r_{b'c'} + C_{b'c'} \cdot \frac{d}{dt} (\Delta V_{C'B'}) \qquad 2.8.$$

in which, $r_{b'c'}$ is the feedback resistance and is given by,

$$r_{b'c'} = - \frac{I_c . W_B}{2 D_n \tau_o} \cdot \frac{d\ W_B}{d\ V_{C'B'}}, \text{ and } C_{b'c'}$$

is composed of the collector transition capacitance $C_{TC'}$ and an additional capacitance due to base width modulation. Hence,

$$C_{b'c'} = C_{TC'} - \frac{I_c W_B}{2\ D_n} \cdot \frac{dW_B}{dV_{C'B'}}$$

Since $\Delta V_{B'E} = 0$, then $\Delta V_{C'B'} = \Delta V_{C'E}$

and Equations 2.7 and 2.8 can be represented by the equivalent circuit shown in Fig. 2.3.b.

As $\Delta V_{B'E}$ and $\Delta V_{C'B'}$ act simultaneously, the equivalent circuits in Figs. 2.3.a and 2.3.b are combined to yield the intrinsic Π-equivalent circuit shown in Fig. 2.4.

However, to obtain the complete equivalent circuit we have to add additional elements to account for the parasitic effects.

2.2.2. Circuit Elements Due to the Parasitic Effects

In the npn integrated bipolar transistor structure shown in Fig. 2.5, the base region, collector region and the substrate form a pnp transistor. The p-type substrate, which is usually connected to the most negative voltage in order to achieve component isolation, then acts as a collector for any minority carriers injected from the base into the n-type

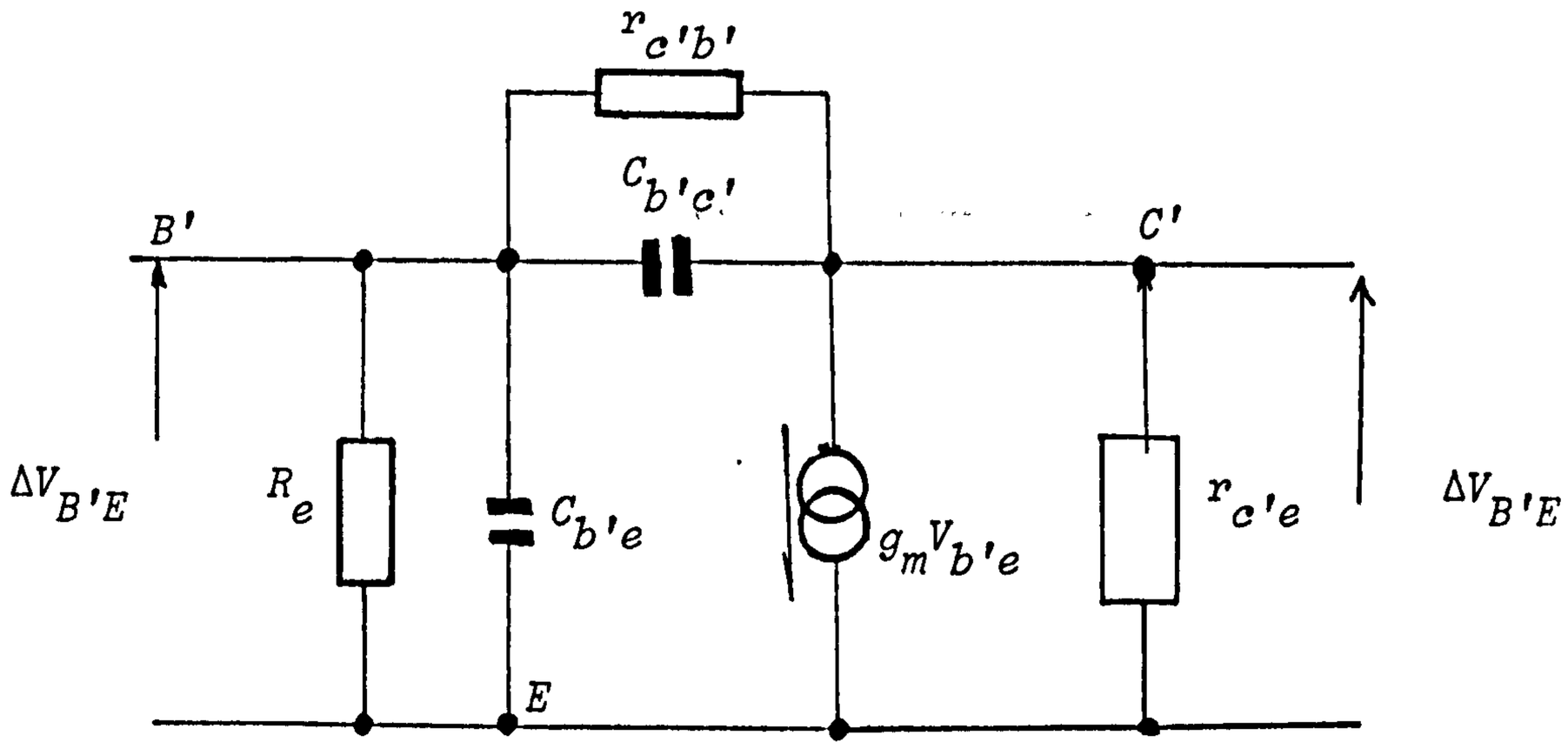
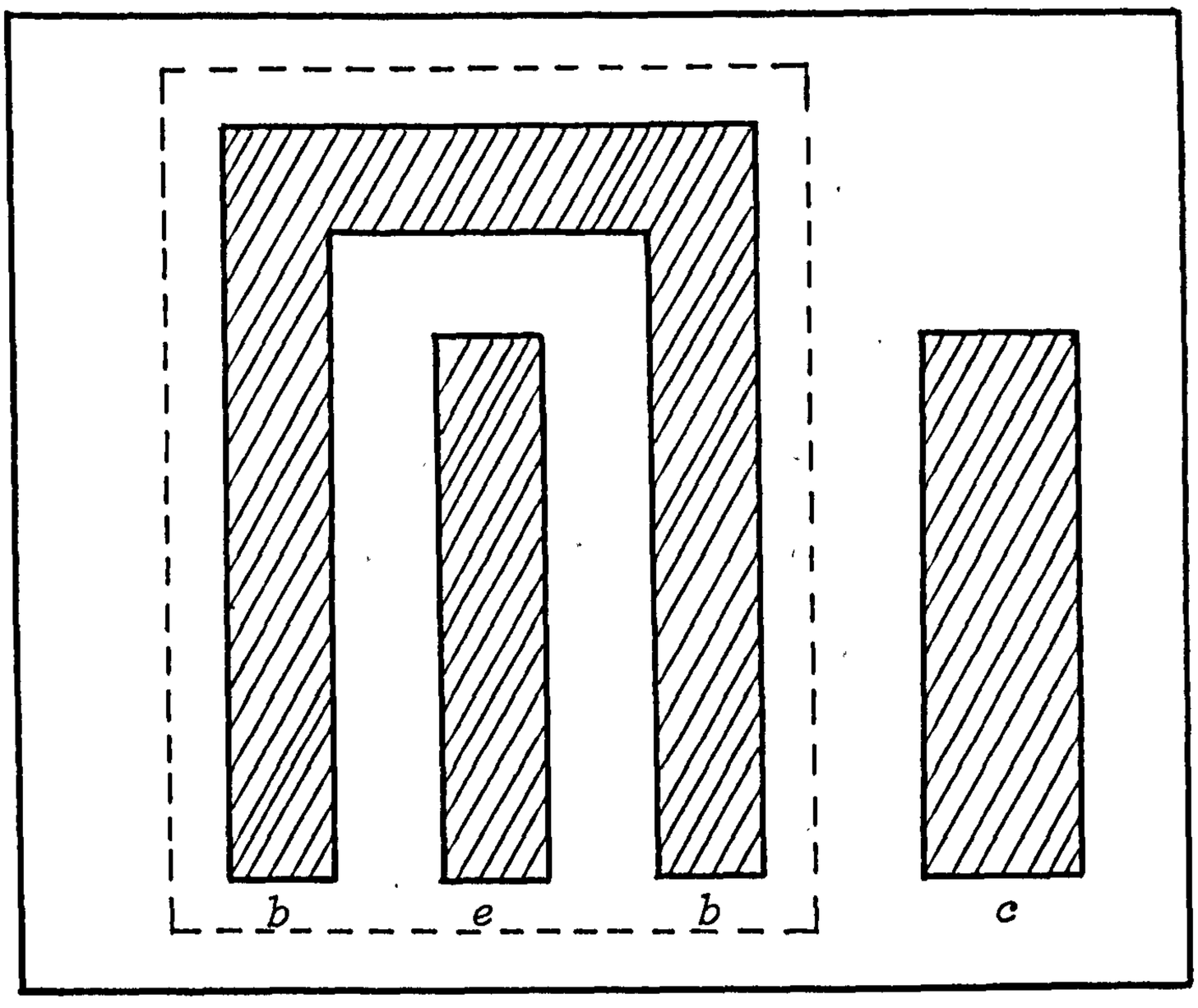
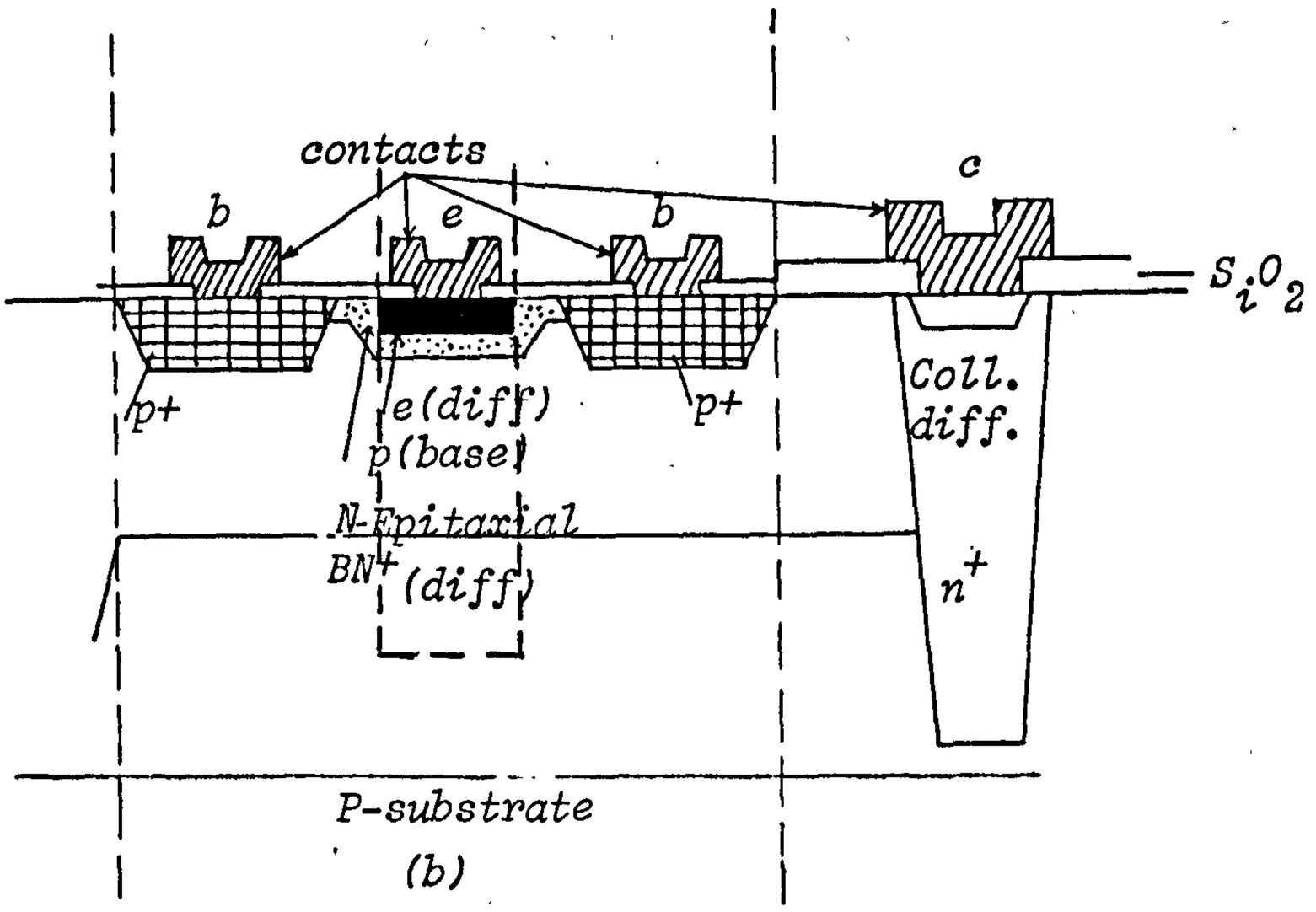


Fig. 2.4. The Combined Intrinsic - Π Equivalent Circuit



(a)



(b)

Fig. 2.5: (a) *A plan view of SB630 transistor (1 cm:6μM)*
(b) *A cross-section of SB630 transistor*
Scale horizontal 1 cm:6μm
vertical 1 cm:1μm

collector region. However, because of the relatively wide collector region in the n-p-n transistor, the pnp parasitic transistor exhibits low gain of the order of unity. Its injection efficiency and transport factor are both considerably less than that of the npn transistor. Moreover, as long as the npn transistor operates in the active region, the pnp transistor is ineffective, with a reverse emitter bias, i.e. it is cut off.

The most important parasitic components are those associated with: the collector spreading resistance, the base spreading resistance, the output capacitance, the substrate isolation capacitance, and the substrate spreading resistance. These will be dealt with in turn.

A. Collector spreading resistance The collector spreading resistance is the ohmic resistance between the collector junction and the collector contact. Due to the top contact requirement to the integrated transistors, the collector spreading resistance is typically larger than that of discrete transistors. It is kept to a minimum by the buried layer technique and by the heavily doped n^+ type side wall diffusion, as shown in Fig. 2.5. This provides a continuous low resistance path from the surface to the collector n^+ region. R_C is approximately given by:

$$R_C \simeq \rho_C \cdot \frac{W_C}{A_E}$$

where W_C is the collector region width and ρ_C is the resistivity.

B. Base spreading resistance and output capacitance The base spreading resistance is the resistance between the base and the base contact. It is formed from several components.

Because the base current flows in a direction transverse to the direction of the normal transistor current flow from emitter to collector, a voltage will build up in the base region along the path of the base current flow. This voltage build up results in a variation of the emitter-base forward bias as a function of distance along the base. This leads to a higher forward bias near the emitter edges than the central part of the

emitter region, which in turn results in a higher current density at the edges. This current crowding effect, makes the total current depend on the periphery of the emitter rather than the area.

For a double strip geometry, the effective base spreading resistance is approximately $R_B/12$,[2(4)] where R_B is the sheet resistance between the base contacts. In the case of a graded base a correction factor that is a function of the impurity ratio N_B/N_{BC} is applied[2(4)]. N_B is the maximum concentration in the base and N_{BC} is the impurity concentration just at the collector junction.

In this study, the integrated bipolar transistor type SB630 made using the Plessey Process III, has been chosen for characterization. The plan view and the cross-section of this transistor are shown to scale in Fig. 2.5.

The components of the base resistance $R_{bb'}$, which determine the average base voltage in the active region of the transistor due to flow of base current to the base contacts, are shown in Fig. 2.6.a. A model based upon the transmission-line approach would be quite accurate, but the resulting equivalent circuit is too complicated to be of practical use. Hence, a simplified model that represents the distributed base resistance and the output capacitance components is given[2(16)] in Fig. 2.6.b. We can define

$$R_{bb'} = r_{bi} + r_{bo} + r_{con} \qquad 2.9.$$

$$C_{ob} = C_{b'c'} + C_1 + C_2 \qquad 2.10$$

where r_{bi} is the resistance in the active region of the transistor under the emitter, r_{bo} is the resistance between the edge of the emitter and the edge of the base contacts, and r_{con} is the base contact resistance. In the transistor geometry shown in Fig. 2.5, it can be seen that the resistance r_{bi} is the main component of the base resistance $R_{bb'}$. Hence,

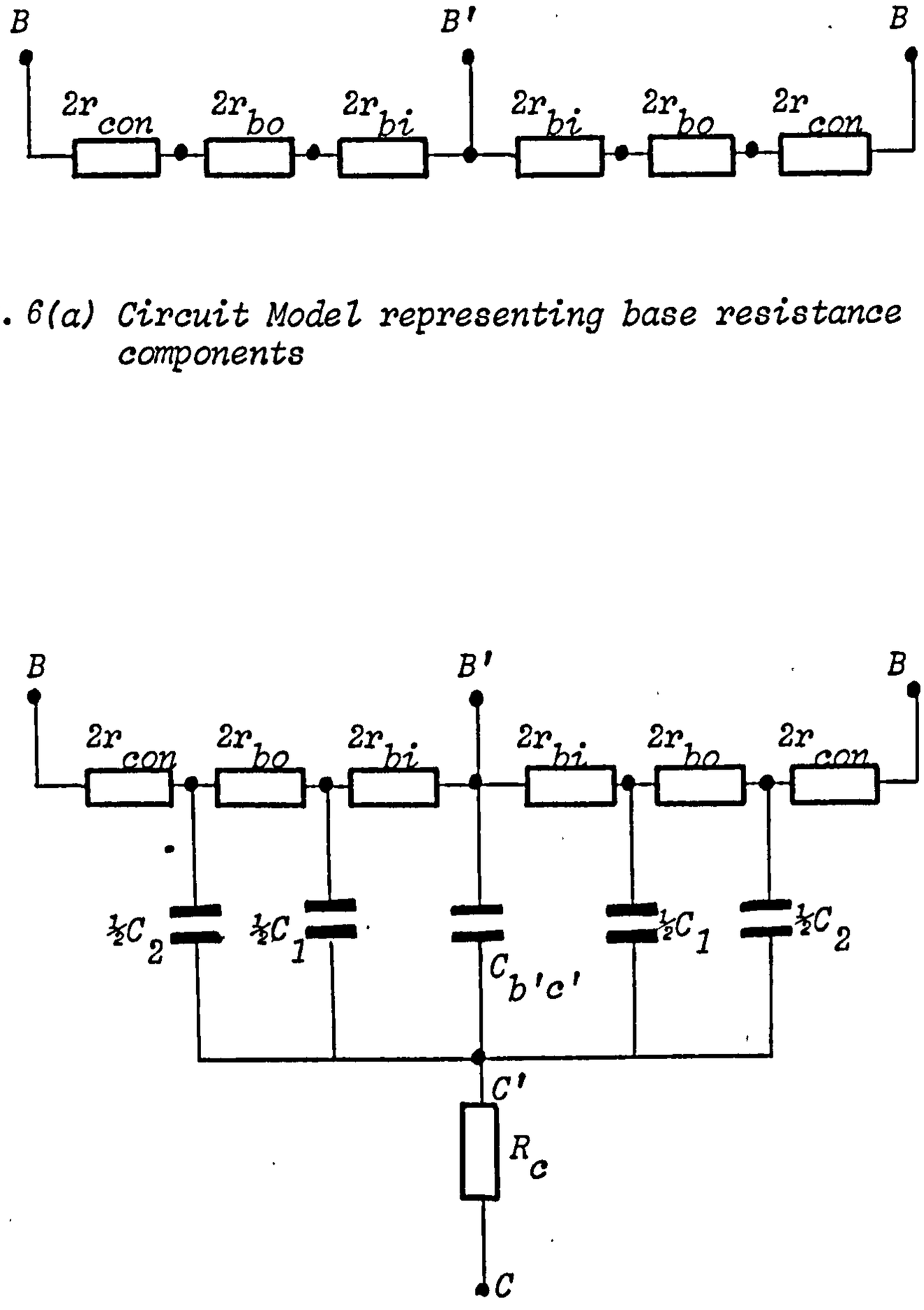


Fig. 2.6(a) Circuit Model representing base resistance components

Fig. 2.6 (b) Circuit Model representing base resistance and distributed collector capacitance (C_{ob})

the contribution of r_{bo} and r_{con} resistances can be neglected and therefore the capacitances C_1 and C_2 can be combined in one capacitance $C_{bc'}$. The relative values for $C_{b'c'}$, C_1 and C_2 depend on the effective areas involved. The transistor geometry shown in Fig. 2.5.b shows, that $C_2 > C_1 > C_{b'c'}$. Numerical values for these capacitors are obtained in Section 2.4.

C. Substrate isolation capacitance The collector substrate isolation capacitance C_o which appears between the collector contact and the substrate has two components. These are the sidewall components and the bottom component as illustrated in Fig. 2.5. For the capacitance calculation the bottom component can be approximated by a step junction. For this component, the collector is more heavily doped than the substrate and therefore the value of the capacitance is determined by the substrate doping. However, the sidewall component may be closely approximated by a linear graded junction and 1/C varies as the cubic root of the junction potential.

D. Substrate spreading resistance The substrate spreading resistance R_s represents the resistance appearing in series with C_o due to the bulk resistance of the material used as a substrate. It can be calculated using the transistor geometry.

2.2.3. Equivalent Circuit including parasitics

In Fig. 2.4 the resistance $r_{c'e}$ is much larger than the practical values of the load resistance, and the feed-back resistance $r_{c'b'}$ is usually larger than the resistance of the output capacitance at operating frequencies. Therefore these two components can be eliminated from the intrinsic transistor equivalent circuit of Fig. 2.4. Including the circuit elements due to the passive parasitic effects, discussed earlier, gives the complete integrated transistor equivalent circuit shown in Fig. 2.7.a, which is approximated for reasons previously mentioned in Section 2.2.2 to that shown in Fig.2.7.b.

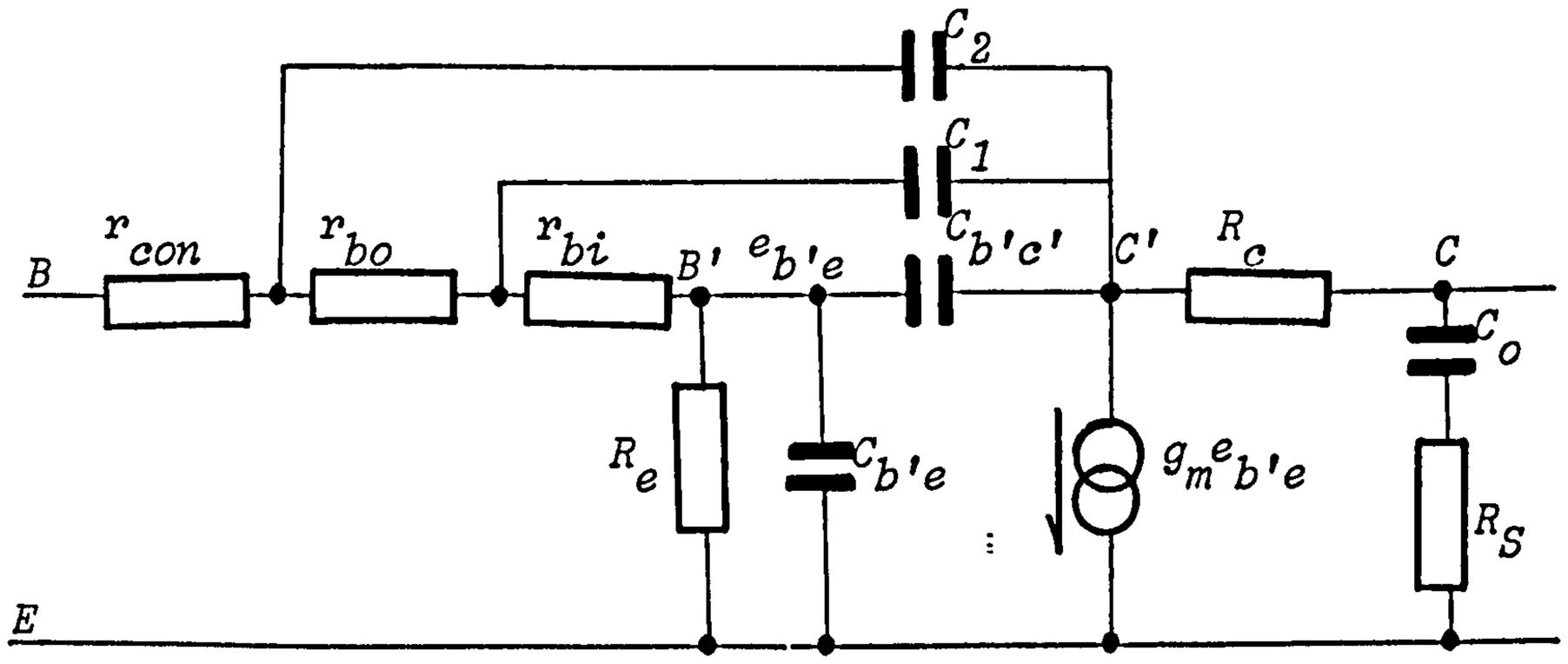


Fig. 2.7.a Full Small-Signal Equivalent Circuit of the SB630 transistor

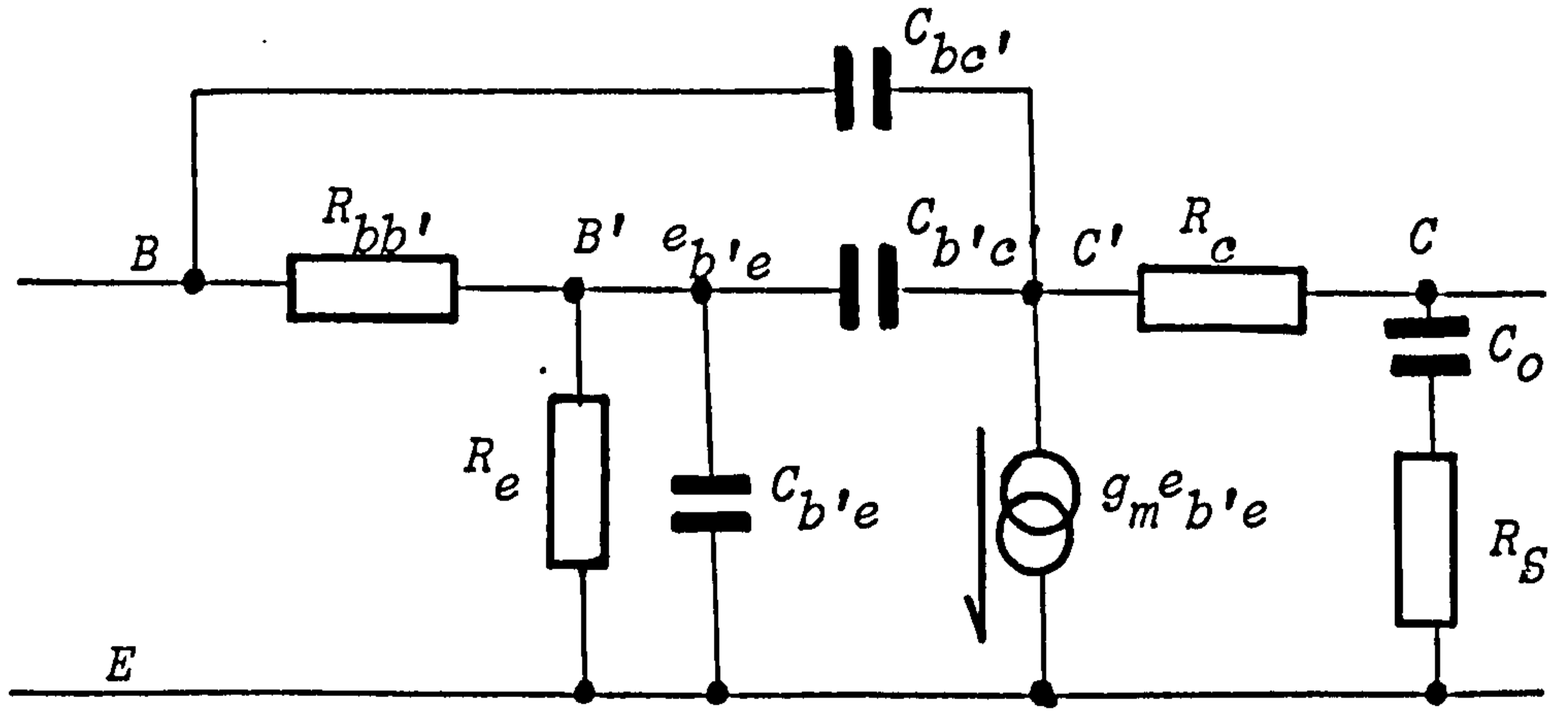


Fig. 2.7.b Approximated Equivalent Circuit of Fig. 2.7.a.

The equivalent circuit of Fig. 2.7.b, is the one used extensively for small-signal analysis at Plessey Caswell.

2.3. The Transistor Frequency Response

At low frequencies, the transistor collector current responds almost instantly to changes in the emitter current. The low frequency common base short-circuit current gain alpha is a constant designated by α_o. At high frequencies, however, alpha becomes a complex function of frequency. This is due to the finite time delay involved in the carrier transport from emitter to collector. α is accurately approximated by[2(4)]:

$$\alpha = \alpha_o \, \mathrm{Exp}(-j\frac{m\omega}{\omega_\alpha})/(1 + j\frac{\omega}{\omega_\alpha}) \qquad 2.11$$

where, m is the excess phase constant, ω_α is related to the physical structure of the transistor through the emitter-to-collector delay time τ_{EC} by: $\frac{1}{\omega_\alpha} = \tau_{EC}$ and ω is the operating frequency.

τ_{EC} represents the sum of five delays encountered by the electrons as they travel from the emitter to the collector as follows:

2.3.1. Emitter-Collector Delay Time

1). The charging time constant of the emitter transi tion capacitance C_{TE}

$$\tau_E = \frac{KT}{qI_E} \cdot C_{TE} \qquad 2.11a$$

in which I_E is the emitter current.

For any arbitrary impurity distribution the transistor capacitance per unit area C_t is given by: $C_t = \epsilon/W_D$, in which ϵ is the permi tivity of the semi-conductor and W_D is the junction depletion region width.

Analytic evaluation of W_D in an integrated transistor is not possible due to the complexity of the impurity profile of a double diffused transistor. It has been indicated, however,[2(5)] that both the complementary error-function and the Gaussian diffusions into a constant background doping, as shown in Fig. 2.1, have a depletion layer width W_D similar to a linear graded junction at low voltages, and similar to a step junction at large reverse bias voltages. It follows that, the linear graded approximation at the emitter junction is good in most cases.

Thus,

$$C_{TE} = A_E \cdot \left[\frac{\epsilon^2 qa}{12\phi_{TE}}\right]^{1/3} \qquad 2.12$$

where,

a is the impurity concentration gradient at the junction, ϕ_{TE} in the total potential across the junction and A_E is the emitter area.

2). In Fig. 2.1, the impurity distribution in the base region is not uniform but is strongly graded. Thus the holes within the base tend to diffuse towards the collector. For equilibrium, this will bring about an electric field pushing the holes toward the emitter-base junction. This same electric field will then be of such direction as to aid the motion of injected electrons. Hence, the injected electrons will now move not only by diffusion but also by drift. As a result, the transit time across the base τ_B will decrease by a factor of $1/\ell n\ (N_B/N_{BC})$.[2(4)] Hence, τ_B is given by:

$$\tau_B = \frac{W_B^2}{2.43 \cdot D_n\ \ell n(N_B/N_{BC})} \qquad 2.12a$$

An important anomaly that leads to a severe limitation in the fabrication of microwave transistors, is the commonly known 'emitter push effect'. The heavy concentration phosphorous emitter diffusion causes the base diffusion to dip under the emitter junction and brings about an irregular junction boundary. This dip effect, however, is not found with an arsenic emitter diffusion assuming that the base diffusion process is the same in both cases. It has been shown,[2(6)] that the base transit time τ_B of an arsenic emitter device is 2 to 3-times smaller than that of a comparable phosphorous emitter device.

3). When the injected electrons reach the edge of the depletion layer of the reverse biased collector-junction they will be swept across this region with their limiting velocities v_s. This is because the electrons experience a strong electric field in the depletion layer area at low collector voltages. This delay time was shown [2(1)] to be

$$\tau_D = \frac{W_D}{2v_s} \qquad 2.13$$

where, W_D is the width of the depletion layer.

4). The collector-base delay time constant τ_C, is due to the charging of the collector transition capacitance C_{TC} through the collector spreading resistance R_C. Therefore:

$$\tau_C = R_C C_{TC} \qquad 2.14$$

As the potential ϕ_{TC} across the collector-base junction is usually large, the step junction is a good approximation, giving

$$C_{TC} = A_C \left(\frac{q \epsilon N_{DA}}{2 \phi_{TC}}\right)^{\frac{1}{2}} \qquad 2.14a$$

where, A_C is the collector area and N_{DA} is an effective impurity concentration that takes into account the relative base and collector dopings.

5). The last delay time to be considered is caused by the substrate isolation capacitance C_o and it is simply given by:

$$\tau_s = R_C\ C_o \qquad 2.15$$

Using Equations 2.11 and 2.14a, with the appropriate symbols, we can write,

$$C_o = A_{sb} \cdot \left(\frac{q \cdot \epsilon \cdot N_{AS}}{2\ \phi_{TS}}\right)^{\frac{1}{2}} + A_{SW}\ \left(\frac{q \cdot \epsilon^2 \cdot a}{12\ \phi_{TS}}\right)^{1/3} \qquad 2.16$$

in which, ϕ_{TS} is the potential across the collector-substrate junction

N_{AS} is the substrate impurity concentration

A_{sb} is the bottom and A_{sw} is the sidewall area respectively of the collector-substrate junction.

Collecting the above five-components of the time delay constants gives the total time delay from emitter-to-collector τ_{EC} from which the grounded base cut-off frequency f_α can be found.

The transistor current gain bandwidth product f_T is the frequency at which the common-emitter short circuit current gain h_{fe} is reduced to unity; using Equation 2.10 f_T is related to f_α by,

$$f_T \simeq \frac{2\pi}{1+m}\ (\tau_E + \tau_B + \tau_C + \tau_D + \tau_3) \qquad 2.17$$

It can be seen that f_T is close to f_α as the excess phase constant, m, is normally smaller than unity.

2.3.2. Dependence of f_T on current and voltage.

Experimentally, it is well known that f_T is a function of the transistor operating point. For a given collector voltage f_T increases with collector current from its value at low collector currents towards a maximum value.

At a certain critical collector current, which depends to some extent on the collector voltage, f_T is observed to decrease with increasing collector current.

At low emitter currents, the predominant time delay constant in Equation 2.17 is τ_E, which is inversely proportional to emitter current. Therefore f_T is directly proportional to the emitter current I_E for a fixed voltage V_{CB}. At relatively higher emitter currents, f_T attains a constant value at which the base transit time τ_B is the most important term.

At a constant V_{CB}, an increase in collector current I_c results in a large voltage drop across R_c and a corresponding decrease in the voltage across the depletion layer. This in turn gives an increase in the collector capacitance C_{TC} and hence τ_C. At large enough collector current, so that all the collector voltage is dropped across R_C, τ_c becomes very large. The rapid fall in f_T occurs at $I_C = (\phi_B + V_{BC})/R_C$, in which ϕ_B is the built in potential at the collector junction.

This fall off of f_T at high currents was discussed in detail by Kirk,[2(8)] where it was shown that the transition region boundary adjacent to the neutral base layer is displaced towards the collector metal contact with increasing collector current. The attendant widening of the neutral base region causes an increase in the transit delay time τ_B. This results in the observed fall of f_T at high currents.

An alternative theory by Van Der Ziel and Agouridis,[2(9)] proposed that this fall results from a saturation effect in the collector transition region. After saturation, the effective transit delay time τ_B is increased by $\{1 + (\frac{L}{2W_B})^2 \cdot (\frac{I_c}{I_o} - 1)^2\}$ when L is the width of the emitter strip and I_o is the collector current at the on-set of saturation. Since

$(L/2W_B)^2 \gg 1$ and $I_c > I_o$, the resulting fall in f_T can be quite significant. In contrast with Kirk's theory, f_T does not approach a limiting value but continues to decrease with increasing I_c.

2.4. Measurements of Equivalent Circuit Parameters

If the approximated equivalent circuit of Fig. 2.7b is to be used to represent the integrated transistor, then it is necessary to be able to find values for its components from parameters that can be measured, such as f_T and h_{fe}.

Most of the experimental measurements involved in evaluating the approximated equivalent circuit components of Fig. 2.7b. were performed on commercially available equipment. Special test systems were built at Caswell by L. Kennedy of Plessey to perform measurements on certain parameters, such as f_T, h_{fe} and components such as $R_{bb'}$ and C_{ob}. The various components of Fig. 2.7b were measured and estimated at Caswell Plessey, except $C_{b'e}$. The measured component values of the approximated equivalent circuit at (I_E = 5mA and V_{CB} = 2V.) are tabulated in Table 2.1.

The parameters f_T and h_{fe} were measured at Caswell and they are shown in Figs. 2.8 and 2.9 respectively[2(11)]. These measurements were performed at a frequency of 200 MHz. The output capacitance C_{ob} was measured at 10 MHz at which frequency the effect of $R_{bb'}$ can be neglected. For the specified transistor (SB630), the reactance of $C_{b'c'}$, is 0.395 MΩ at 10 MHz which is much larger than $R_{bb'}$, thus, justifying neglecting $R_{bb'}$ at the frequency of the C_{ob} measurements.

In the approximated equivalent circuit Fig. 2.7.b, the measured output capacitance C_{ob} has been divided into two parts: the collector-junction capacitance $C_{b'c'}$ and the overlap diode capacitance $C_{bc'}$. The ratio between these two capacitances was calculated from the transistor geometry[2(6)] shown in Fig. 2.5.a in which,

Table 2.1

The Approximated Equivalent Circuit Parameter Values of SB630 Integrated Bipolar Transistor (V_{CB} = 2V, I_E = 5mA)

Transistor parameter or Equivalent circuit component	Measured or calculated value
f_T, measured at 200 MHz	2.5 GHz
h_{FE}, normally measured at low frequency	50
g_m, calculated from (qI_E/KT)	0.2 mhos
R_E, calculated from (h_{FE}/g_m)	250 ohms
$R_{bb'}$, calculated from noise figure	113 ohms
R_C, calculated from the output characteristic	150 ohms
R_S, calculated from transistor geometry	400 ohms
C_o, measured at 1MHz	0.6 pF
C_{ob}, measured at 10 MHz	0.36 pF
$C_{bc'}$, $C_{b'c'}$ calculated from C_{ob}	0.32 pF

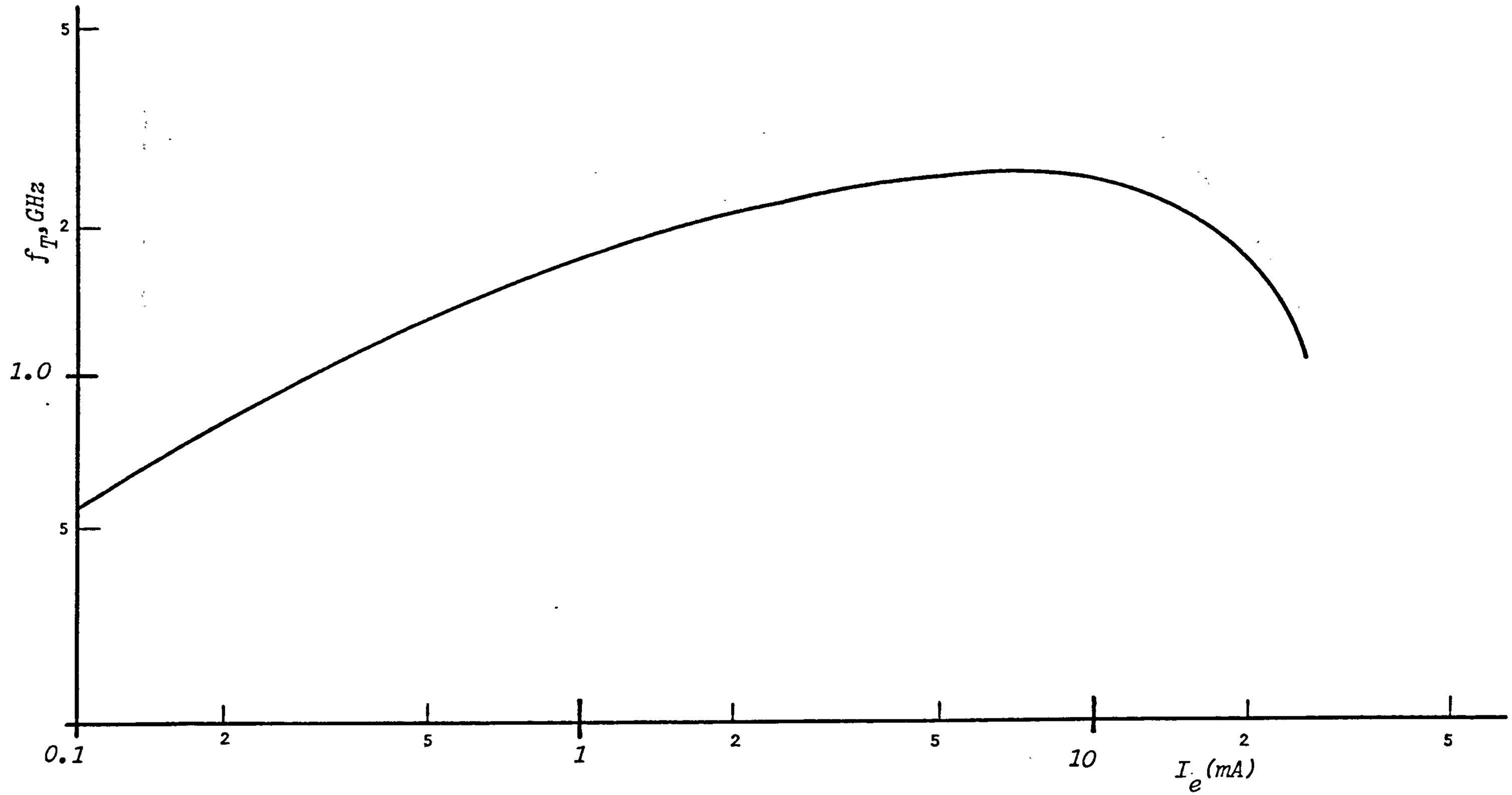


Fig. 2.8

f_T *v* I_e *at (200 MHz ,* V_{cb} *= 2V)*

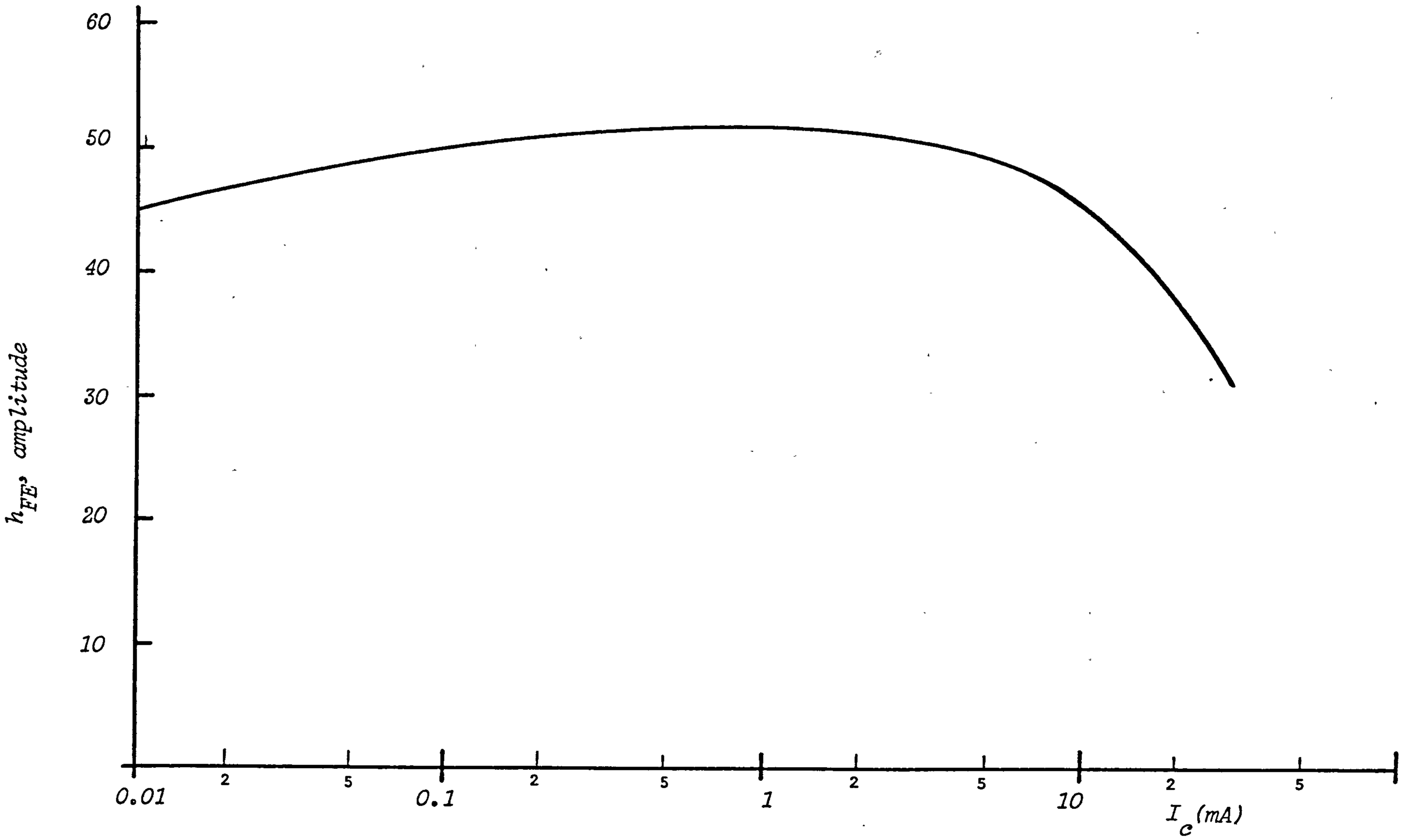


Fig. 2.9

h_{FE} *v* I_c *at (200 MHz,* V_{cb} = *2V)*

$$C_{bc'}/C_{b'c'} = \frac{\text{total area (emitter + base)}}{\text{emitter contact area}} \qquad 2.18$$

total area (emitter + base) = $48 \times 30 = 1440 \ \mu^2$

emitter contact area = $6 \times 30 = 180 \ \mu^2$

Hence, $C_{bc'} = 8.0 \ C_{b'c'}$

The collector spreading resistance R_c has been estimated from the output characteristic of the transistor displayed on the curve tracer. The base resistance $R_{bb'}$ value was obtained from noise figure measurements[2(11)]. The d.c. transconductance g_m is calculated from the expression, $g_m = qI_E/kT$.

where,

k = Boltzmann's constant, 8.62×10^{-5} ev/^oK

T = absolute temperature, 300^oK

I_E = emitter current, mA

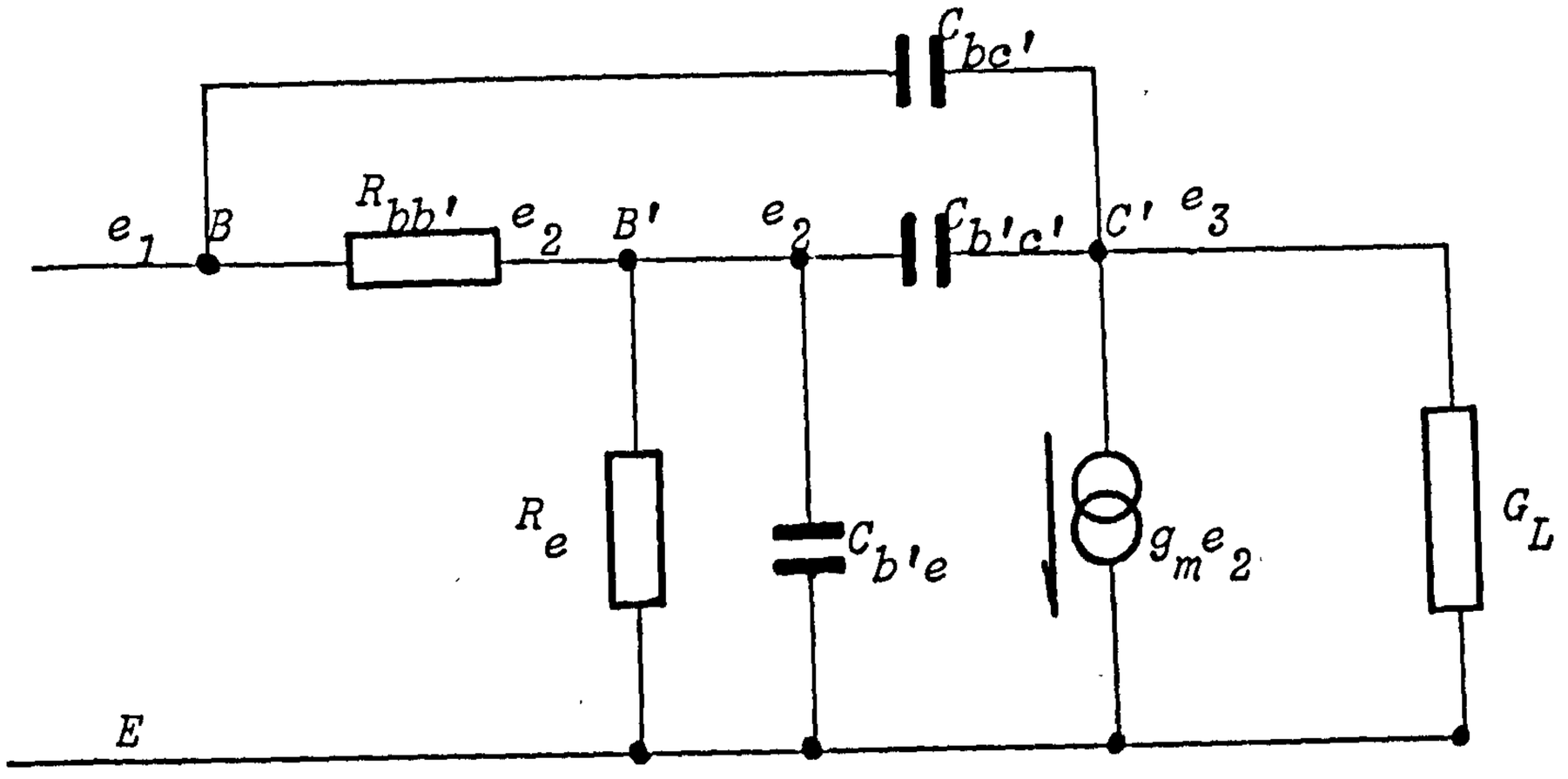
The collector-substrate junction capacitance C_o was measured at 10 MHz and the substrate spreading resistance R_s was calculated from the transistor geometry of Fig. 2.5.a.

The dynamic resistance of the emitter-base junction $R_e = h_{FE}/g_m$, also appears in the circuit model of Fig. 2.7.a.

2.5. Transistor Equivalent Circuit Analysis

In this analysis, it is aimed to produce an exact Miller equivalent circuit from the approximated equivalent circuit model of Fig.2.7.b.

An external load is included in this analysis to give equations suitable for general use. The output circuit of Fig. 2.7.b is combined in one element G_L to make the analysis much simpler as shown in Fig. 2.10 giving:



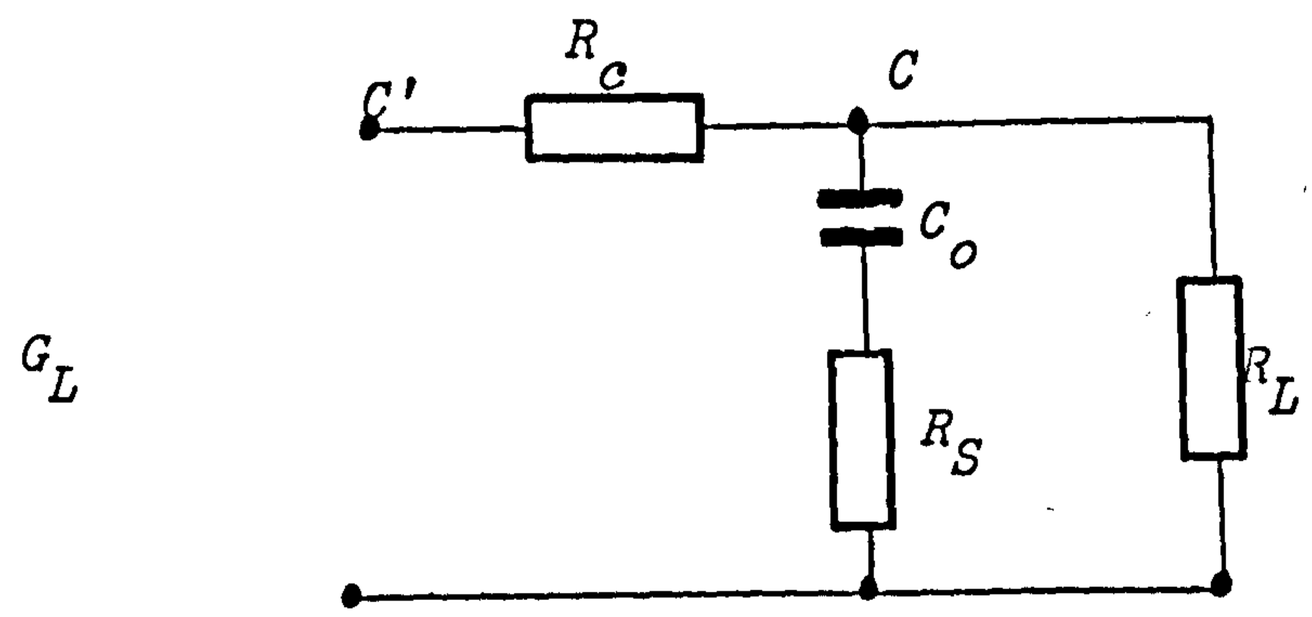


Fig. 2. 10

Full small-signal equivalent circuit (G_L represents the out-put circuit including R_c)

$$G_L = \frac{1+j\omega C_o(R_s+R_L)}{(R_c+R_L)+j\omega C_o(R_sR_L+R_c(R_s+R_L))} \qquad 2.19$$

Nodal analysis techniques were applied to the circuit of Fig. 2.10[2(9)]. Hence, the node current equations at the transistor junctions B,B' and C' respectively are:

$$(G_b+j\omega C_{bc'})e_1 - G_b e_2 - j\omega C_{bc'} e_3 = I_1 \qquad 2.20$$

$$-G_b e_1 + (G_b + G_e + j\omega(C_{b'e} + C_{b'c'}))e_2 - j\omega C_{b'c'} e_3 = 0 \qquad 2.21$$

$$-j\omega C_{bc'} e_1 + (g_m - j\omega C_{b'c'})e_2 + (G_L + j\omega(C_{bc'}+C_{b'c'}))e_3 = 0 \qquad 2.22$$

where $G_b = 1/R_{bb'}$ and $G_e = 1/R_e$.

Equations for the Miller admitances Y_{m1} and Y_{m2} of the Miller equivalent circuit Fig. 2.11 can be easily formulated, giving,

$$Y_{m1} = j\omega C_{b'c'}(1 - e_3/e_2) \qquad 2.23$$

and

$$Y_{m2} = j\omega C_{bc'} (1 - e_3/e_1) \qquad 2.24$$

To evalute Y_{m1} and Y_{m2}, e_3/e_1 and e_3/e_2 ratios have to be found. These ratios can be obtained from the solution of Equations 2.21 and 2.22. See Appendix A. Giving:

$$e_3/e_1 = - \frac{G_b(g_m-j\omega C_{b'c'})-j\omega C_{bc'}(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))}{(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))(G_L+j\omega(C_{bc'}+C_{b'c'}))-j\omega C_{b'c'}(9_m-j\omega C_{b'c'})} \qquad 2.25$$

and

$$e_3/e_2 = - \frac{G_b(g_m-j\omega C_{b'c'})-j\omega C_{bc'}(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))}{G_b(G_L+j\omega(C_{bc'}+C_{b'c'}))-\omega^2 C_{bc'}C_{b'c'}} \qquad 2.26$$

By substitution of Equation 2.26 into Equation 2.23 and Equation 2.25 into Equation 2.24, exact expressions for Y_{m1} and Y_{m2} can be found. The equivalent transconductance G_{m1} in the Miller equivalent circuit is given by the following expression,

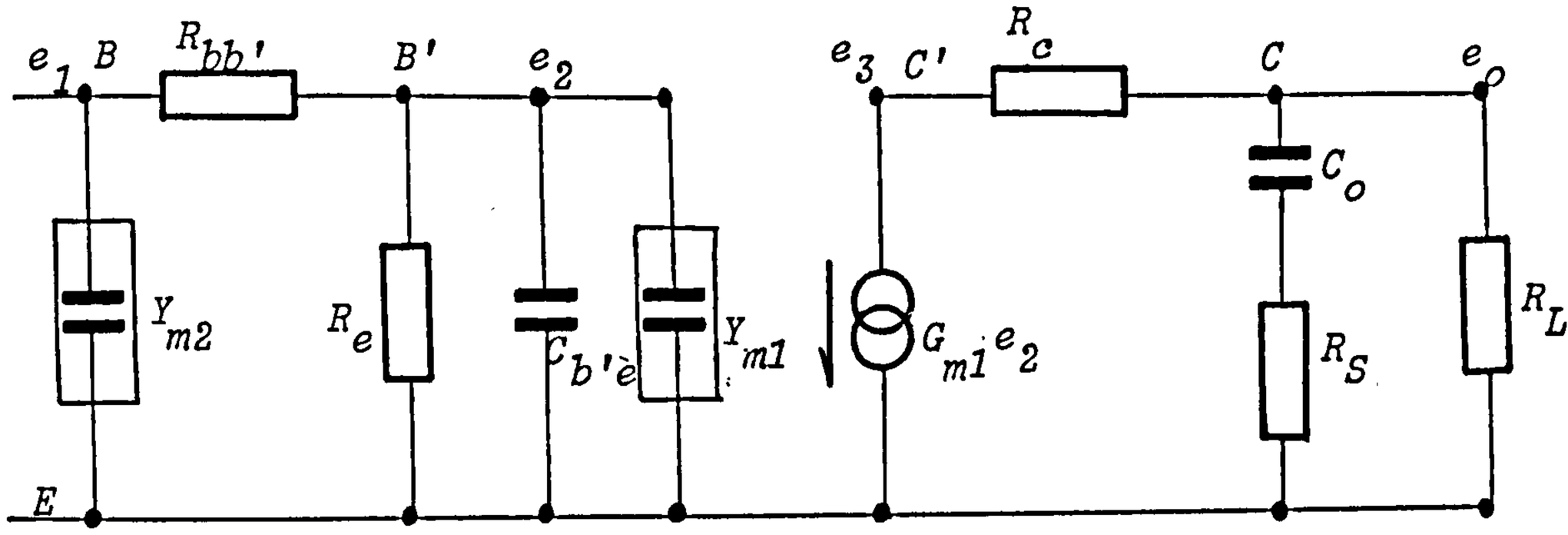


Fig. 2.11

Miller equivalent of Fig.2.10

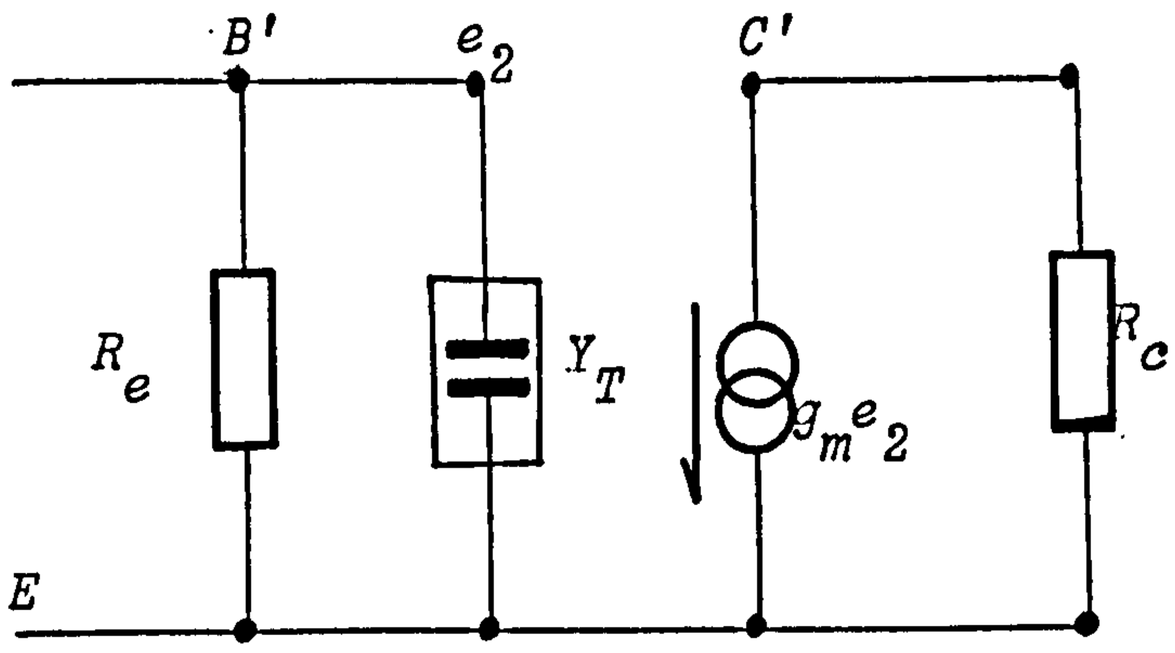


Fig. 2.12

The approximated Miller Equivalent Circuit of Fig.2.11 at f_T measurement.

$$G_{m1} = - e_3 G_L/e_2 \qquad 2.27$$

where G_L is the total load conductance seen at the junction C'E in Fig.2.10, and it is given by Equation 2.19. Equations 2.19, 2.25 and 2.26 are frequency dependent and complex functions of the equivalent circuit components of Fig. 2.10. Consequently, Y_{m1}, Y_{m2} and G_{m1} are also frequency dependent.

Due to the collector-base feed-back capacitances $C_{bc'}$ and $C_{b'c''}$, there is also an additional series combination of R and C shunting the output circuit of the Miller equivalent circuit of Fig. 2.11. This series branch of R and C is normally neglected as they are relatively larger than the practical values for the external load R_L.

The voltage and current gains A_v and A_i of the Miller equivalent circuit Fig. 2.11 can be straightforwardly obtained. Appendix A gives:

$$e_o = - G_{m1} e_2 Z_L \qquad 2.28$$

where Z_L is the impedance of the external load R_L in shunt with a series combination of C_o and R_s, see Fig. 2.7.b, and it is given by:

$$Z_L = \frac{R_L(1+j\omega C_o R_s)}{1+j\omega C_o(R_s+R_L)} \qquad 2.29$$

e_2 in terms of e_1 is,

$$e_2 = \frac{G_b e_1}{G_b+G_e+j\omega C_{b'e}+Y_{m1}} \qquad 2.30$$

and G_{m1} is given by Equation 2.27.

The substitution of Equations 2.29 and 2.30 into Equation 2.28 gives the voltage gain,

$$A_v = e_o/e_1 = - \frac{G_{m1} G_b R_L (1+j\omega C_o R_s)}{(G_b+G_e+j\omega C_{b'e}+Y_{m1})(1+j\omega C_o (R_s+R_L))} \qquad 2.31$$

By definition, the current gain A_i can be given by:

$$A_i = A_v \cdot \frac{Z_{in}}{R_L} \qquad 2.32$$

where Z_{in}, is the input impedance of the Miller equivalent circuit of Fig. 2.11. and it is given by:

$$Z_{in} = \frac{G_b+G_e+j\omega C_{b'e}+Y_{m1}}{(G_b+G_e+j\omega C_{b'e}+Y_{m1}))(G_b+Y_{m2})-G_b^2} \qquad 2.33$$

2.6. The Emitter-Junction Capacitance Calculation

To predict or accurately calculate the transistor performance from the equivalent circuit described in Section 2.4 and shown in Fig. 2.7.b, the emitter junction capacitance $C_{b'e}$ has to be found. The parameters f_T and h_{FE} and the various components of Fig. 2.7.b have been described in Section 2.4, except $C_{b'e}$.

In order to accurately evaluate the capacitance $C_{b'e}$ from the measured f_T, at specific emitter current I_E, an exact Miller equivalent circuit is required. This equivalent circuit has been obtained in Section 2.5 and it is shown in Fig. 2.11. However, a value for $C_{b'e}$ cannot be obtained until values for the Miller admittances Y_{m1} and Y_{m2} are known. These admittances, given by Equations 2.23 and 2.24, are functions of $C_{b'e}$. Explicit solutions of Equations 2.23 and 2.24 was not found possible, but the following approximated method will be shown to be satisfactory[2(12)].

At the frequency of measuring f_T, which is 200 MHz, the Miller admittance Y_{m2} is much larger than G_b. Therefore, G_b can be neglected compared with Y_{m2}. Hence, the Miller admittances Y_{m1} and Y_{m2} and the admittance of the emitter-junction capacitance $C_{b'e}$ can be combined in one element Y_T as shown in Fig. 2.12. Fig. 2.12 also represents the

Miller equivalent circuit of Fig. 2.11 during f_T measurements (R_L = 0.0Ω) from which a value for $C_{b'e}$ can be estimated. The collector spreading resistance R_c is included in this calculation. This latter important factor is usually neglected when calculating $C_{b'e}$ from the measured f_T. The decrease in the $C_{b'e}$ value is mainly due to the R_c Miller effect during the f_T measurements.

At the frequency of measuring f_T, the admittance Y_T reduces to a simple susceptance $j\omega C_T$. Hence, Fig. 2.12 gives

$$C_T = \frac{g_m}{2\Pi f_T} \qquad 2.34$$

and

$$C_T = C_{m1}^T + C_{m2}^T + C_{b'e} \qquad 2.35$$

where C_{m1}^T and C_{m2}^T are the reduced Miller capacitances at the frequency of measuring f_T. At the frequency of f_T measurement C_{m1} and C_{m2} values become ,

$$C_{m1}^T \simeq C_{b'c'} (1 + g_m R_c) \qquad 2.36$$

$$C_{m2}^T \simeq C_{bc'} (1 + g_m R_c G_b/(G_b+G_e)) \qquad 2.37$$

The solution of Equation 2.36 gives $C_{m1}^T \simeq 1.24$ pF and Equation 2.37 gives $C_{m2}^T \simeq 6.94$ pF. Equation 2.34 gives C_T = 12.7 pF. The substitutions of C_{m1}^T, C_{m2}^T and C_T into Equation 2.35 give $C_{b'e}$ = 4.56 pF for the approximation stated above. The data of Table 2.1 has been used in the above calculations.

If R_c were to be neglected in the above calculation, (this is what is commonly done in practice), C_{m1}^T and C_{m2}^T values would reduce to $C_{b'c'}$ and $C_{bc'}$ respectively and the resultant $C_{b'e}$ increases to C_T. This value is large and it is not valid for this type of transistor.[2(11)] The importance of knowing the exact value for R_c is critical in evaluating the Miller capacitances and hence in obtaining an exact value for the emitter-junction capacitance $C_{b'e}$ from the measured f_T.

Fig. 2.13 represents the approximated Miller capacitances C_{m1}^{T} and C_{m2}^{T} at the frequency of measuring f_T as the value of R_c varies from 0 - 200Ω for f_T constant. Fig. 2.13 also represents the resultant $C_{b'e}$ at each value of R_c. Equations 2.34 - 2.37 and the corresponding component values of Table 2.1 were used in the above calculations.

2.7. Equivalent Circuit Frequency Response

In Section 2.6 the Miller capacitance C_{m1} and C_{m2} have been evaluated at the frequency of measuring f_T only to obtain the $C_{b'e}$ value. Hence, the voltage and current gains can be calculated for any external load R_L from the Miller equivalent circuit shown in Fig. 2.11.

For the frequency response calculated here, the exact expressions for the Miller admittances Y_{m1} and Y_{m2}, obtained in Section 2.5 were used. The frequency dependance of Y_{m1}, Y_{m2} and the equivalent transconductance G_{m1} components is also included in these calculations.

The voltage and current gains of the Miller equivalent circuit of Fig. 2.11 were calculated at an external load R_L = 0.1Ω using the equations obtained in Section 2.5. The calculated h_{fe} amplitude is shown in Fig.2.14. Fig. 2.14 also represents the calculated current-gain for R_L = 1KΩ.

The calculated short-circuit current gain h_{fe} gives the same f_T value as that measured. Thus this justifies the approximations applied in Section 2.6 to obtain the correct value for the emitter-junction capacitance $C_{b'e}$ from the measured value of f_T.

The short-circuit current gain h_{fe} for the equivalent circuit of Fig. 2.10 was calculated applying the general computer analysis program G-CAP-2S, and it was identical to that calculated from the Miller equivalent

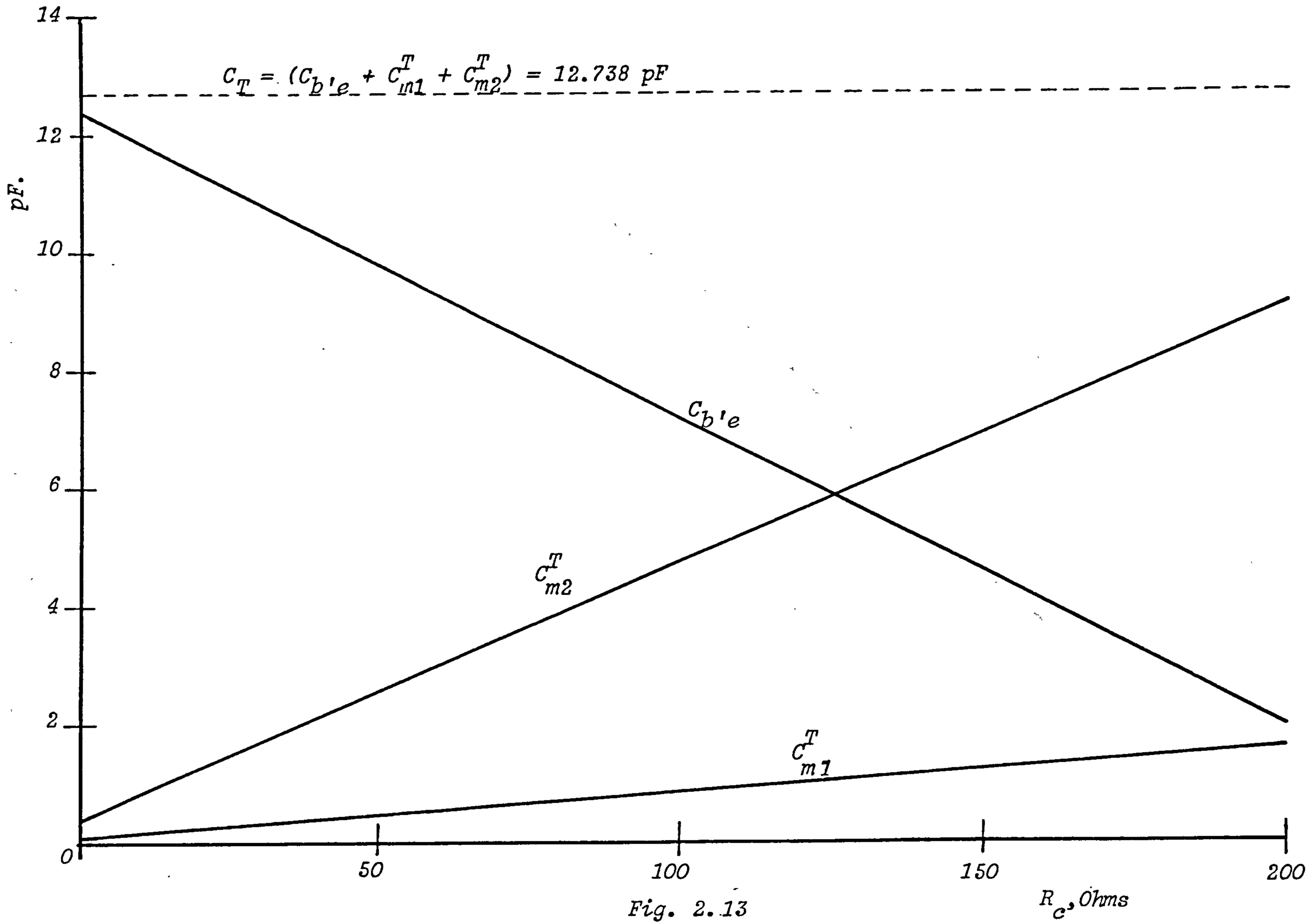


Fig. 2.13

Miller Capactiances C_{m1} and C_{m2} and $C_{b'e}$ at f_T for selected values of R_c

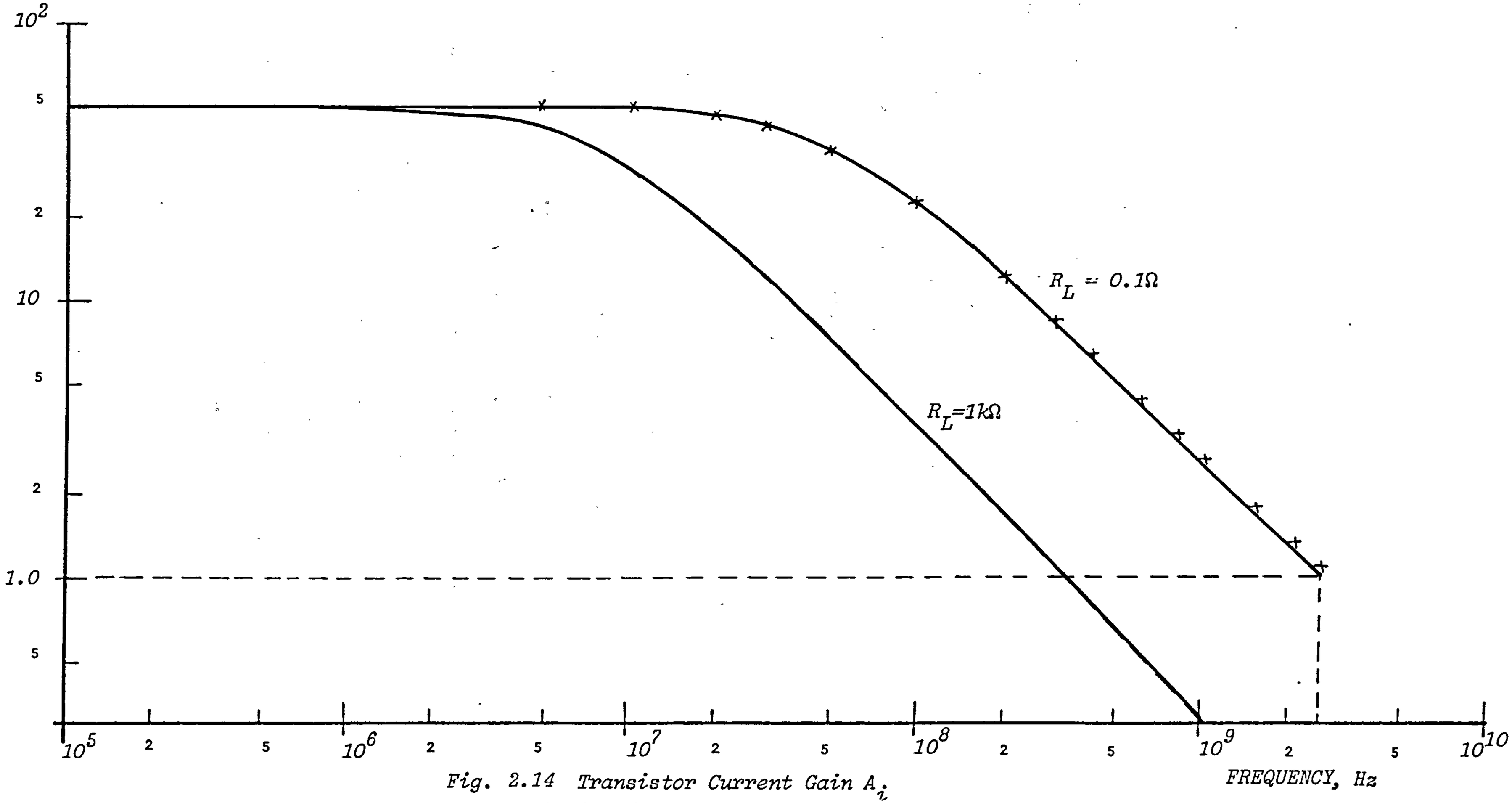


Fig. 2.14 Transistor Current Gain A_i
——, Calculated from Fig. 2.11
xxxx, Calculated from Figs. 2.17 or 2.18

circuit of Fig. 2.11, thus verifying the validity and the accuracy of the Miller equivalent circuit, that it represents the transistor as the equivalent circuit of Fig. 2.10 does. The $C_{b'e}$ value obtained in Section 2.6 was used in both calculations. The voltage gain has also been calculated for several values of R_L. The results of these calculations are shown in Fig. 2.15. As expected, the voltage gain A_v decreases and the roll-off frequency, 3dB point, increases as R_L decreases. At R_L = 1KΩ, A_v is approximately constant over the frequency range up to 20 MHz. At 20 MHz, A_v starts to roll-off. At higher frequencies up to f_T, A_v decreases with more than 6 dB/octave. This steep decrease is due to the series combination of C_o and R_s shunted with R_L at the output of the Miller equivalent circuit of Fig. 2.11. This steep decrease is eliminated for the h_{fe} amplitude graph as the series branch of C_o and R_s is shorted. See Figs. 2.14 and 2.15.

2.8. Simplified Equivalent Circuit Model Analysis

Whilst it has been shown that use of the equations of Sections 2.5 and 2.6 will give accurate results, some of these equations are inconveniently complex. For many purposes, a simpler equivalent circuit allowing the design engineer greater use of intuition is needed at the expense of some accuracy. The major contribution to this would be the simplification of the complex frequency dependence of the equations specified previously. This problem was treated as follows.

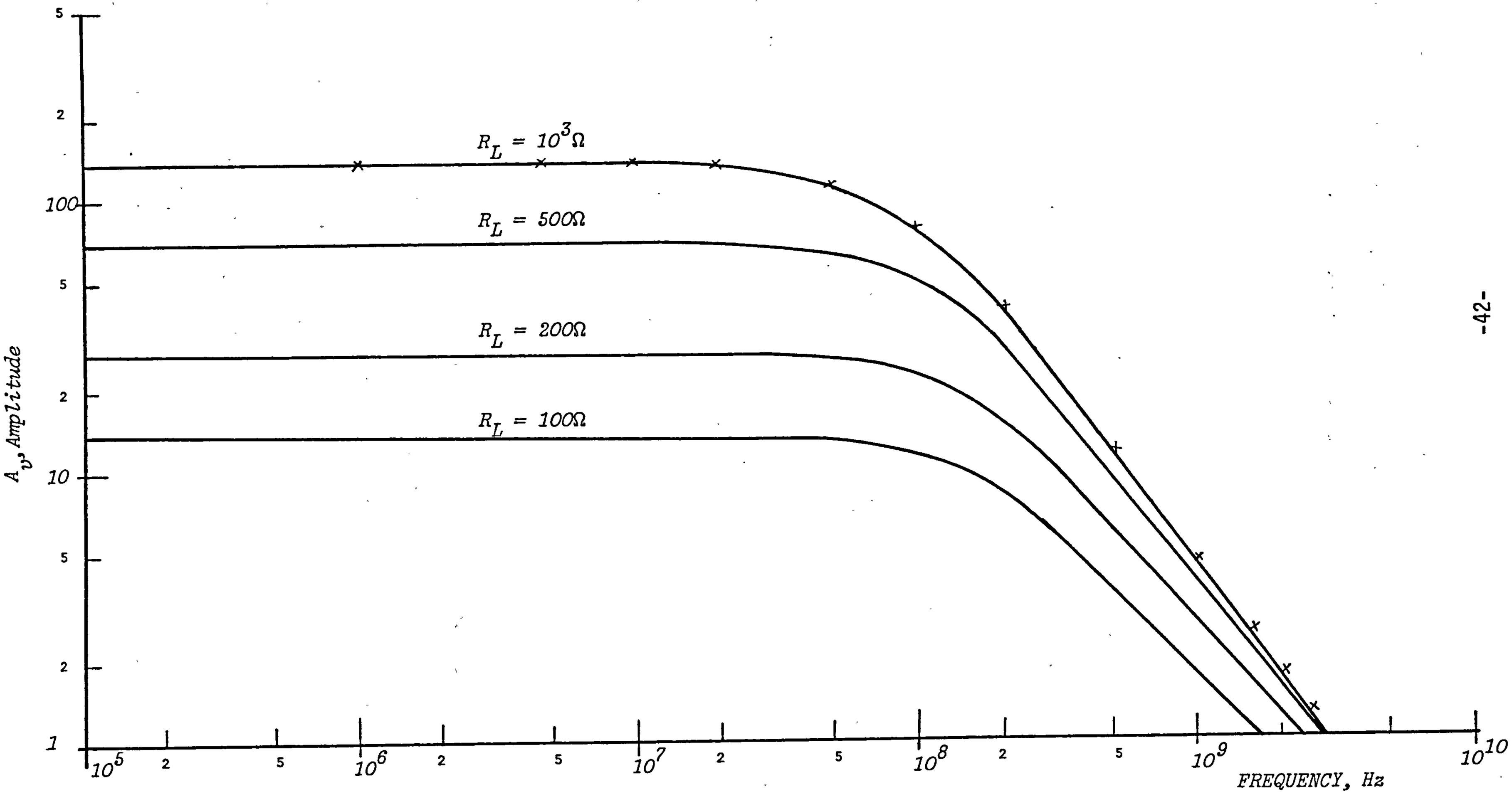


Fig. 2.15 Transistor Voltage Gains A_v
——, Calculated from Figs. 2.11 or 2.12
xxx , Calculated from Figs. 2.17 or 2.18

The Miller admittances Y_{m1} and Y_{m2} and the equivalent transconductance G_{m1} in the Miller equivalent circuit of Fig. 2.11 are dependent on e_3/e_1 and e_3/e_2 ratios. See Section 2.5. The e_3/e_1 and e_3/e_2 ratios, calculated from the equivalent circuit of Fig. 2.10 and given by Equations 2.26 and 2.27, were approximated by neglecting higher order terms of the time constants in the numerator and the denominator of these ratios. These approximations are fully stated in Appendix B, and they are summarized in Table 2.2. An external load R_L is included in this analysis to give equations suitable for general use.

Hence

$$e_3/e_1 = - \frac{g_m G_b (R_c+R_L)(1+j\omega T_1)}{(G_b+G_e)(1+j\omega T_2)(1+j\omega T_3)(1+j\omega T_4)} \qquad 2.39$$

$$\text{and} \quad e_3/e_2 = - \frac{g_m (R_c+R_L)(1+j\omega T_1)}{(1+j\omega T_2)(1+j\omega T_3)} \qquad 2.40$$

$$\text{In which,} \quad T_1 = C_o(R_3R_L + R_c(R_s + R_2))/R_c + R_s) \qquad 2.41$$

$$T_2 = C_o(R_s + R_L) \qquad 2.42$$

$$T_3 = (C_{bc'} + C_{b'c'})(R_c + R_L) \qquad 2.43$$

$$\text{and} \quad T_4 = (C_{b'e} + C_{b'c'})/(G_b + G_e) \qquad 2.44$$

We see that $C_{bc'}$ and $C_{b'c'}$ appear separately only in Equations 2.44 above.

$$\text{Providing,} \quad C_{b'e} \gg C_{b'c'} \qquad 2.45$$

Equation 2.44 reduces to,

$$T_4 = C_{b'e}/(G_b + G_e) \qquad 2.46$$

The Bode-plots of these approximated ratios are shown in Fig. 2.16 at $R_L = 0.0\Omega$, i.e. at f_T measurement. Fig. 2.16 also represents the exact e_3/e_1 and e_3/e_2 ratios calculated from Equations 2.26 and 2.27 respectively.

Table 2.2

Summarized Approximation of e_3/e_2 and e_2/e_1 Ratio*

* See Appendix B

The Approximated Term	Given by Equation	External Load R_L (ohms)	Frequency at which it becomes significant f(GHz)	Remarks
$\omega^2 C_{bc'}(C_{b'e}+C_{b'c'})/g_m G_b$	B.6	-	1.5	Independent of R_L
$\omega\{G_b C_{b'c'}+C_{bc'}(G_b+G_e)\}/g_m G_b$	B.9	-	8.0	Independent of R_L
$\omega C_o\{R_s R_L+R_c(R_s+R_L)\}/(R_c+R_L)$	B.20	$R_L = 0$ $R_L = 1K$	1.0 0.8	
$^2C_o C_{b'c'}\{R_s R_L+R_c(R_s+R_L)\}/$ $g_m(R_c+R_L)$	B.33	$R_L = 0$ $R_L = 1K$	2.5 2.0	
$C_{b'c'}(R_c+R_L)/g_m C_o\{R_s R_L+R_c(R_L+R_s)\}$	B.34	$R_L = 0$ $R_L = 1K$		Frequency Independent (ratio) 8.3×10^{-4} 6.29×14^{-4}
$\omega g_m C_{b'c'}(R_c+R_L)/(G_b+G_e)$	B.36	$R_L = 0$ $R_L = 1K\Omega$	1.0 0.75	
$C_{b'e} > C_{b'c'}$	B.41	-	-	Valid for most transistor

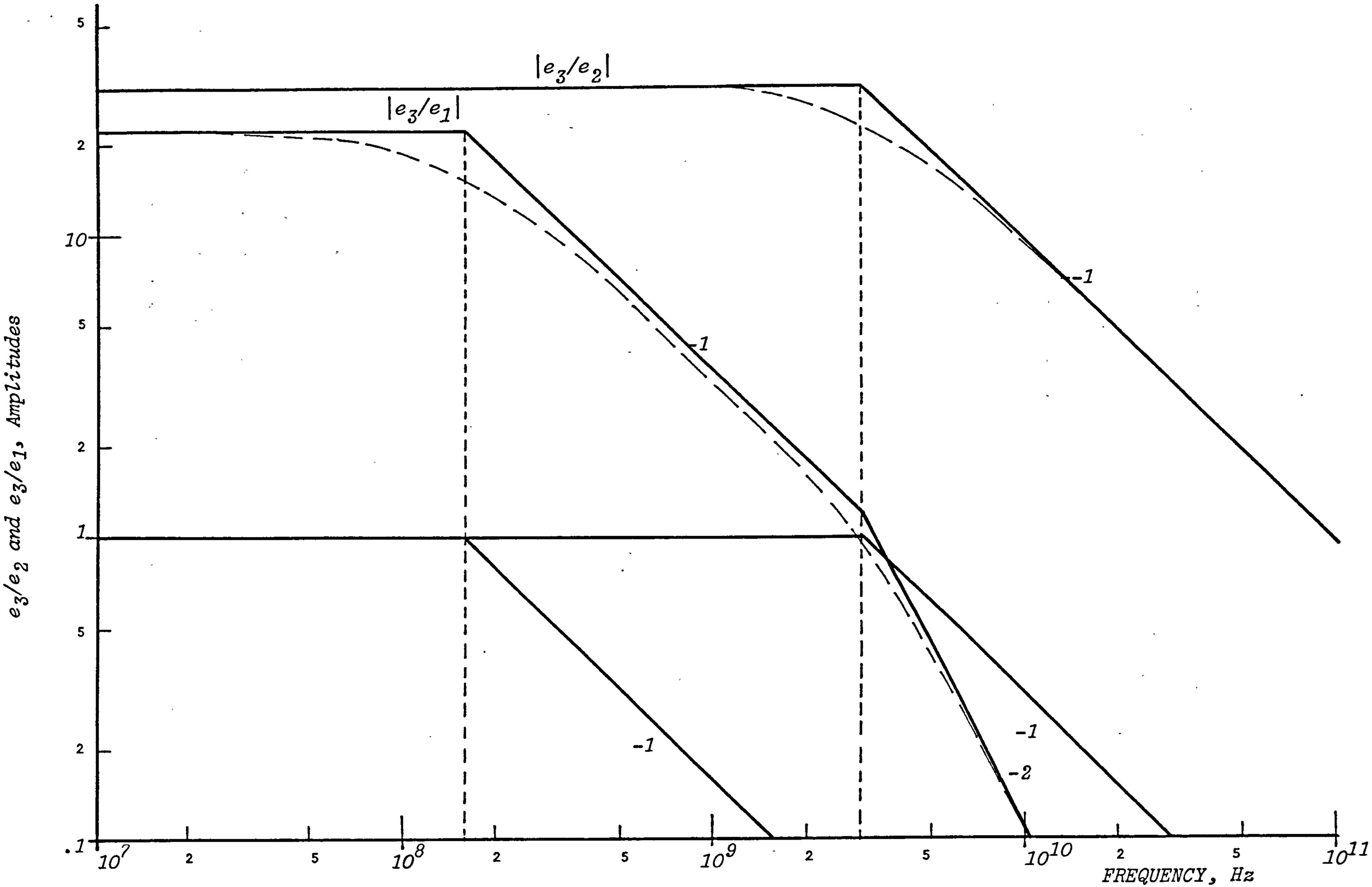


Fig. 2.16
The e_3/e_1 and e_3/e_2 ratio Frequency Response
——— Plots (Equations 2.39 and 2.40)
---- Calculated from Equations 2.28 and 2.29

The capacitances $C_{bc'}$ and $C_{b'c'}$ appear now as one term ($C_{bc'} + C_{b'c'}$) in Equation 2.43. This term is the measured output capacitance C_{ob}, see Section 2.4. It was concluded that the whole of C_{ob} can be connected between the base terminal B and the collector-junction C' in the equivalent circuit of Fig. 2.10. This gives the simplified equivalent circuit of Fig. 2.17, which is in contrast to the conventional hybrid-Π representation.[2(13)]

The simplified Miller equivalent circuit for Fig. 2.17 can be obtained in a similar way as in Section 2.5. See Appendix C. There is now only one Miller admittance Y_m at the input of the simplified Miller equivalent circuit of Fig. 2.18 and it is given by,

$$Y_m = j\omega C_{ob} (1 - e_3'/e_1') \qquad 2.47$$

The equivalent transconductance G_m can be written as,

$$G_m = -(e_3'/e_2') G_L \qquad 2.48$$

$$\text{where, } e_3'/e_1' = - \frac{g_m G_b - j\omega C_{ob}(G_b+G_e+j\omega C_{b'e})}{(G_b+G_e+j\omega C_{b'e})(G_L+j\omega C_{ob})} \qquad 2.49$$

$$e_3'/e_2' = - \frac{g_m G_b + j\omega C_{ob}(G_b+G_e+j\omega C_{b'e})}{G_b(G_L+j\omega C_{ob})} \qquad 2.50$$

and G_L is given by Equation 2. 19

Equations for the voltage and current gains A_v and A_i of the simplfied Miller equivalent circuit of Fig. 2.18 can be obtained as follows. The output voltage e_o' is:

$$e_o' = - G_m e_2' Z_L \qquad 2.51$$

where Z_L and G_m are given by Equations 2. 29 and 2.48 respectively. e_2' in terms of e_1' is (see Appendix C),

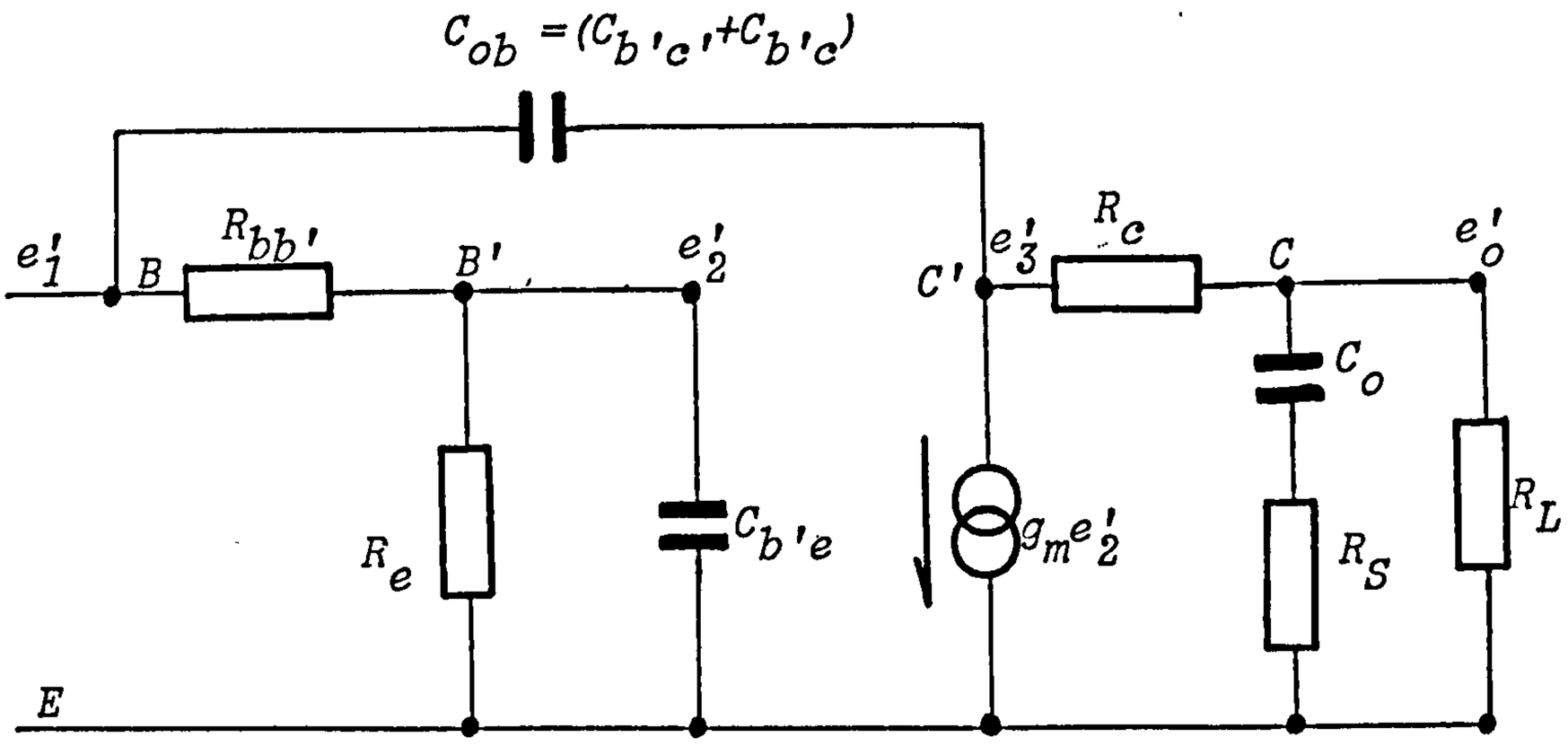


Fig. 2. 17

A Simplified Equivalent Circuit Model of Fig.2.10

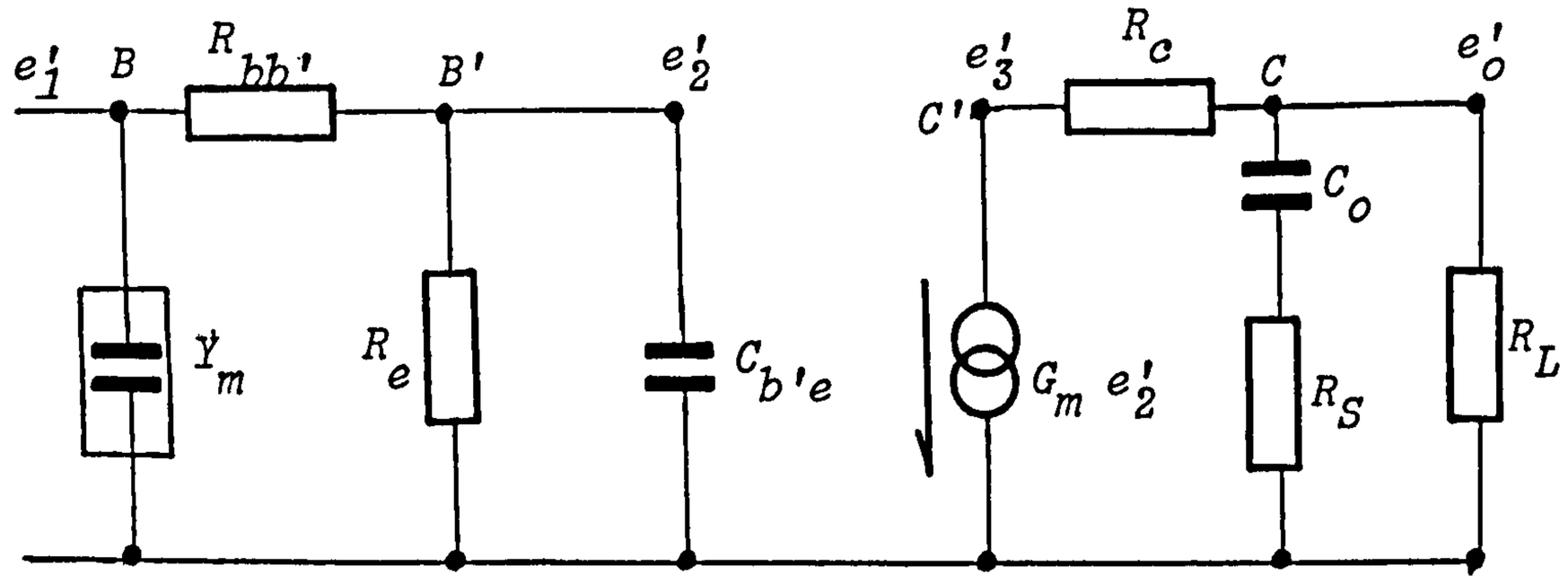


Fig. 2.18

A Miller Equivalent of Fig. 2.17

$$e_2' = \frac{G_b\, e_1'}{G_b+G_e+j\omega C_{b'e}} \qquad 2.52$$

The substitution of Equations 2.29 and 2.52 into Equation 2.51 gives,

$$e_o' = - \frac{G_m G_b R_L (1+j\omega C_o R_s) e_1'}{(G_b+G_e+j\omega C_{b'e})(1+j\omega C_o(R_s+R_L))} \qquad 2.53$$

The voltage gain e_o'/e_1' is then.

$$A_V' = - \frac{G_m G_b R_L (1+j\omega C_o R_s)}{(G_b+G_e+j\omega C_{b'e})(1+j\omega C_o(R_3+R_L))} \qquad 2.54$$

Equation 2.54 can be written as,

$$A_V' = - \frac{G_{m2} G_b R_L (1+j\omega T_5)}{(G_b+G_e)(1+j\omega T_2)(1+j\omega T_4)} \qquad 2.55$$

where $T_5 = C_o R_s$ 2.56

By definition, the current gain A_i' in terms of A_V' is,

$$A_i' = A_V' \cdot Z_{in}'/R_L \qquad 2.57$$

where Z_{in}' in the input impedance of the simplified Miller equivalent circuit of Fig. 2.18 and it is given by,

$$Z_{in}' = \frac{G_b+G_e+j\omega C_{b'e}}{(G_b+G_e+j\omega C_{b'e})(G_b+ Y_m)-G_b^2} \qquad 2.58$$

and R_L is the external load at the output of the simplified Miller equivalent circuit shown in Fig. 2.18.

2.9. The Simplified Equivalent Circuit Frequency Response

To calculate the voltage and circuit gains of the simplified Miller equivalent circuit of Fig. 2.18, the Miller admittance Y_m and the emitter junction capacitance $C_{b'e}$ admittance values have to be found.

The successful approximated method applied in Section 2.6 has been employed here also to evaluate the Miller capacitance C_m^T and then $C_{b'e}$. Thus,

$$C_m^T = C_{ob}(1 + g_m G_b R_c/(G_b+G_e)) \qquad 2.59$$

and $$C_m^T + C_{b'e} = g_m/2\Pi f_T \qquad 2.60$$

Using Table 2.1 data, the solution of Equations 2.59 and 2.60 gives, C_m^T = 7.8 pF and $C_{b'e}$ = 4.9 pF. The $C_{b'e}$ value obtained here is slightly higher than that obtained in Section 2.6. This is due to the approximation nvolved in the equivalent circuit simplification discussed in Section 2.8.

The short-circuit current gain h_{fe} of the simplified Miller equivalent circuit of Fig. 2.18 has been calculated and it is also shown in Fig. 2.14. The voltage gain A_v has been calculated for R_L = 1KΩ and it is also shown in Fig. 2. 15 The approximated equation of Section 2.8 has been used in calculating A_i and the voltage gain A_v.

The agreement between the calculated h_{fe} and the voltage gain A_v for R_L = 1KΩ obtained here and those calculated from the Miller equivalent circuit of Fig. 2.10 is satisfactory up to f_T. Thus, this justifies the approximation nvolved to calculate the emitter-junction capacitance $C_{b'e}$.

Hence, the author concludes that the simplified equivalent circuit of Fig. 2.17, which is in contrast to the hybrid-Π representation, represents the Integrated Bipolar transistor, described in Section 2.2 at frequencies up to f_T as the equivalent circuit model of Fig. 2.10 does.

2.10 The Miller Admittances Frequency Dependence

In Sections 2.6 and 2.9, the Miller admittances Y_{m1} and Y_{m2} in the Miller equivalent of Fig. 2.11 have been evaluated at the frequency of measuring f_T in order to estimate the emitter junction capacitance $C_{b'e}$ and hence to calculate the voltage and current gains.

Here, the author investigates over which frequency range the above approximation, i.e. evaluation of Y_{m1} and Y_{m2} at frequency of measuring f_T, is valid.

The Y_{m1} and Y_{m2} expressions, given by Equations 2.23 and 2.24 in Section 2.5, have been evaluated at $R_L = 0.0\Omega$ using the corresponding component values of Table 2.1. The results of these calculations are shown in Fig. 2.19.

Fig. 2.19 shows that, the $(Y_{m1}/j\omega)$ amplitude remains approximately constant over the frequencies up to f_T. Fig. 2.19 also shows $(Y_{m1}/j\omega)$ phase is zero up to 100 MHz and then it starts to fall down to -40 degrees at f_T. Also, Fig. 2.19 shows that, the $(Y_{m2}/j\omega)$ amplitude is approximately constant up to 100 MHz and at higher frequencies up to f_T starts to fall-off. $(Y_{m2}/j\omega)$ phase is zero up to 10 MHz and at this frequency starts to fall down to approximately -90^o at f_T.

The author concludes, the evaluation of the Miller admittance Y_{m1} and Y_{m2} of the Miller equivalent circuit of Fig. 2.11 at the frequency of measuring f_T in order to evaluate the emitter junction capacitance $C_{b'e}$ from the measured f_T, is satisfactory.[2(12,13)]

2.11. Discussion and Conclusion

The Miller equivalent circuit has been deduced from the approximated equivalent circuit model, of the specified transistor, of Fig. 2.10 The

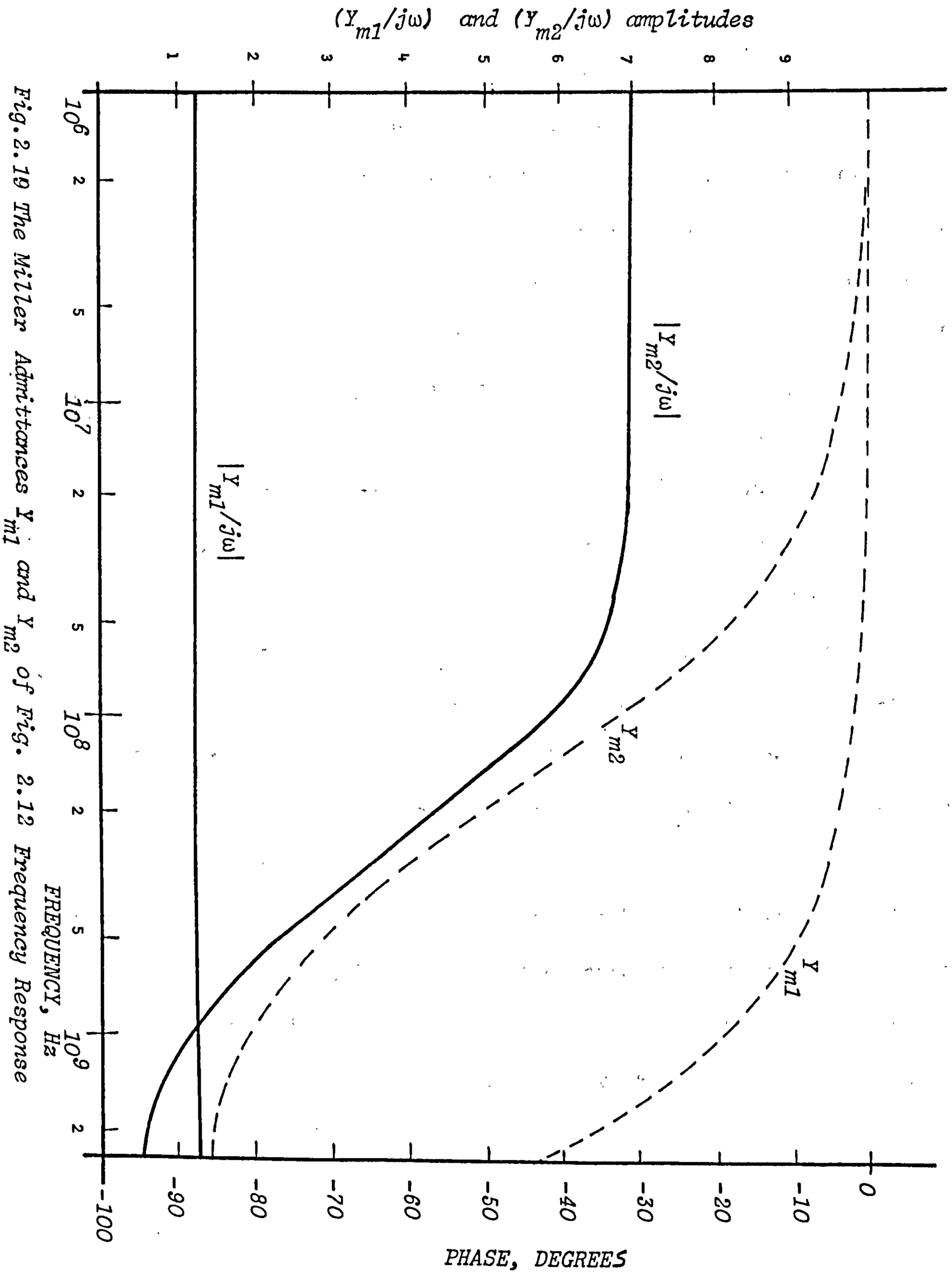


Fig. 2.19 The Miller Admittances Y_{m1} and Y_{m2} of Fig. 2.12 Frequency Response
——, Amplitude. ---, phase.

Miller equivalent circuit of Fig. 2.11 has been used to calculate the voltage and current gains. It has been found that it gives the same frequency response as that calculated from the approximated equivalent circuit of Fig. 2.10 using G-CAP-2S Analysis program as shown in Figs. 2.14 and 2.15. The frequency dependence of the various components of the Miller equivalent circuit of Fig. 2.11 have been studied. The evaluation of the Miller admittances Y_{m1} and Y_{m2} of Fig. 2.11 at the frequency of measuring f_T has been justified. Evaluation of the emitter junction capacitance $C_{b'e}$ applying the approximated method outlined in Section 2.6 was successful as it gives the same f_T value as that measured. A simplified equivalent circuit model of Fig. 2.17 in which the whole of the output capacitance C_{ob} can be considered to be between the base terminal and the collector junction has been deduced. The conditions under which this simplified equivalent circuit model is valid is given in Table 2.2. This simplification has been successfully shown to apply to integrated transistors having $f_T \simeq 2.5$ GHz. The voltage and current gains calculated from the Miller equivalent circuit for Fig. 2.18 were compared in Figs. 2.14 and 2.15 to those calculated from the approximated equivalent circuit model of Fig. 2.10. The agreement between these results was very satisfactory. Thus this justifies the approximation involved both to calculate the emitter junction capacitance $C_{b'e}$ from the measured f_T and to simplify the approximated transistor equivalent circuit of Fig. 2.10. See publications, Chapter 11.

2.12. REFERENCES

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CHAPTER 3

CORRECTION OF MICROWAVE-NETWORK-ANALYSER MEASUREMENT OF 2-PORT DEVICES

3.1. Introduction

Most microwave network analysers measure the amplitudes and phases of the forward and reflected wave to obtain the required parameters. These waves are normally extracted by directional couplers and down converted to an intermediate frequency where easier amplitude and phase comparisons can be made.

Computer aided correction programs may be applied to calibrate out the errors normally associated with the measuring system components. In the available computer correction programs,[3(1-7)] a short circuit, an off-set short and a well calibrated or sliding termination are required. For measurements under many conditions, the sliding termination is not generally available. Also, there may be insufficient room to accommodate a sliding termination in the transistor measuring jig. In the author's present work, the H.P. test-fixture jig has been chosen to accommodate the integrated bipolar transistor, for measuring the transistor S-parameters. Here, a different computer aided correction program is needed to maintain a reference plane of measurements at the device terminals and to calibrate the measuring system up to this reference plane. By this means we obtain accurate S-parameters for the measured transistor, eliminating the effects of parasitics such as bond wire inductance and pad capacitance. Such parasitics can be considered to be part of the system errors.

In the measurement of the scattering parameters (S-parameters) of 2-port microwave devices, the system errors can be represented by a perfect Network Analyser and two equivalent error networks, one each side of the device under test. These errors can be represented in terms of scattering parameters.

3.2. Derivation of the Computer-Corrected Network Analyser Calibration Equations.

Since Hackborn's original paper[3(1)], describing a calibration procedure for a computer-corrected network analyser, various other schemes have been described.[3(2-7)] In all previous treatments, approximations in one way or another have been made in evaluating the error parameters involved and hence the device parameters. In these correction systems[3(2-7)] the leakage power transmitted through the system has been neglected. In the analysis by Hand[3(2)], one error parameter has been assumed to be unity in order to reduce the unknowns and to make the evaluation of the error parameters possible. In others[3(2,5)] the reference plane has not been established at the device terminals. Consequently, the measured parameters of the device under test include some errors mainly due to the variation of the reference plane during system calibration.

It was decided to establish a reference plane at the device terminals so that the measured S-parameters will accurately represent the device under test. Some of the above programs were investigated and have been found not suitable for establishing the reference plane at the transistor terminals.[3(3,5)] This was due to the limited space available in the H.P. test-fixture jig, to accommodate the calibration pieces required.

Fig. 3.1.a represents a system block diagram when a device under test is measured. The signal flow graph of such a system is shown in Fig. 3.1.b. The system errors are represented here by two-equivalent error networks M and N placed between the device and each of the measuring ports. The leakage power transmitted through the measuring system in both directions is considered here and represented by M_L and N_L.

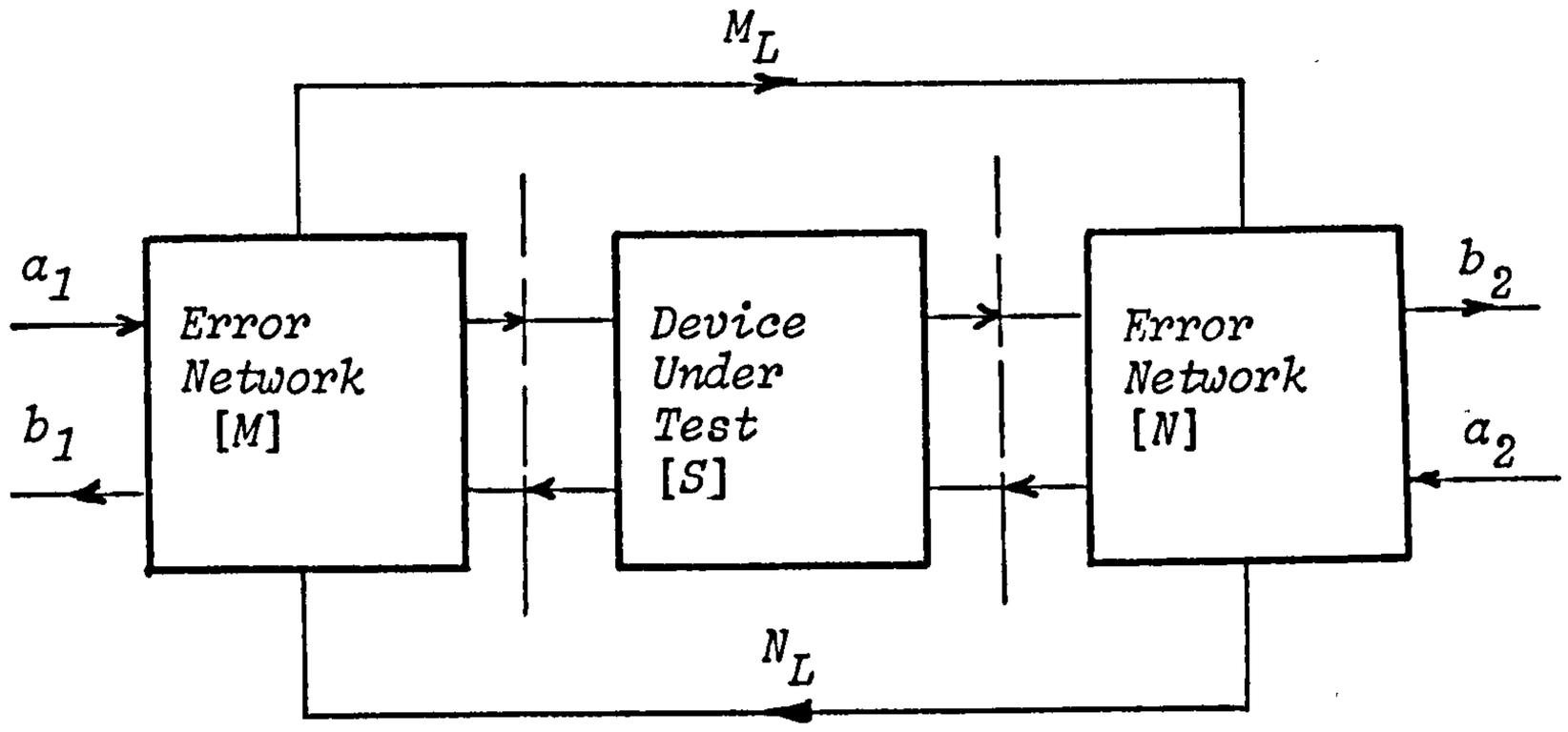

Fig.3.1.a. System Block Diagram

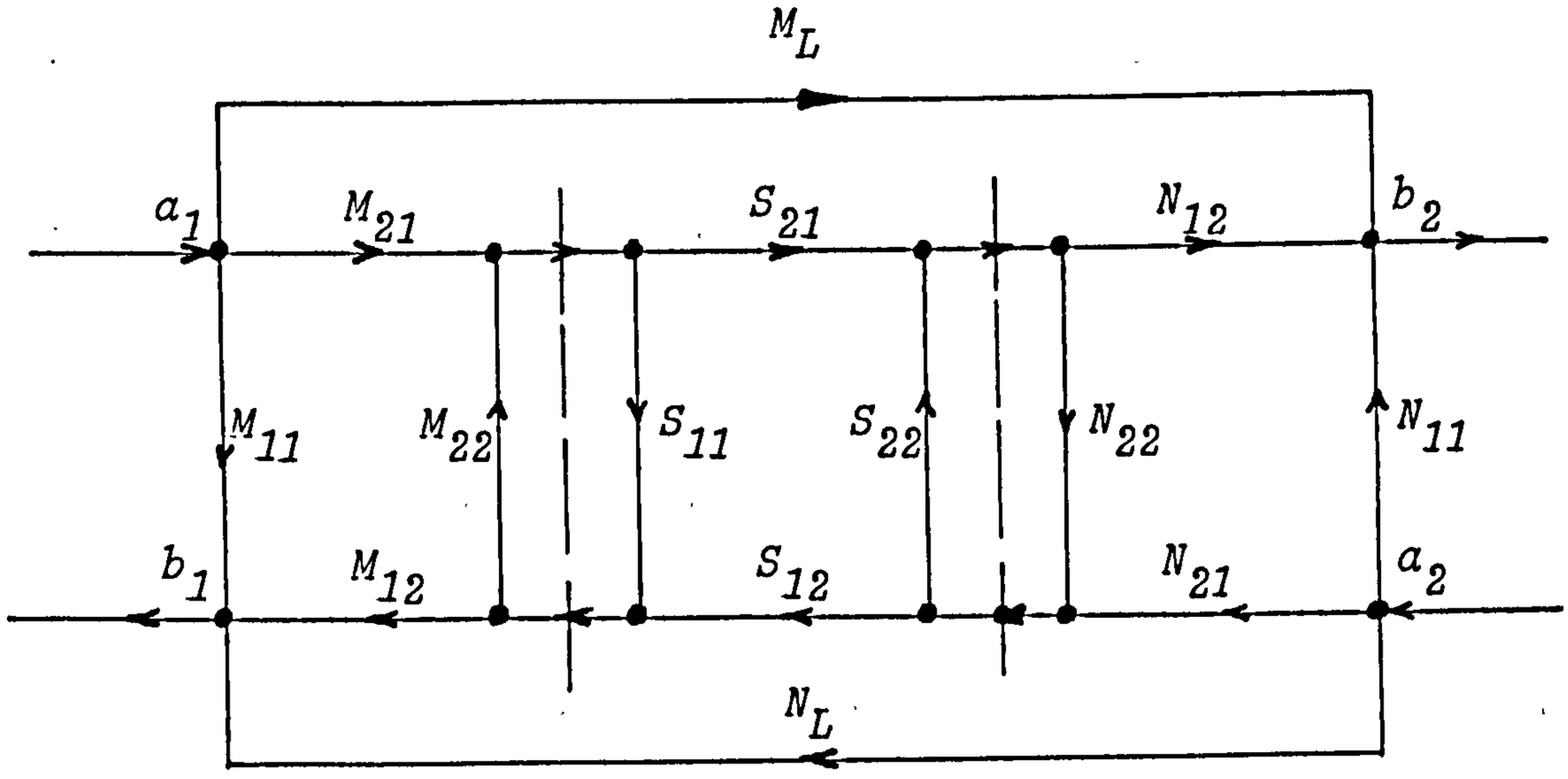

Fig.3.1.b. Flow Graph of System Model of Fig.3.1.a.

Figs. 3.2.a. and 3.2.b. represent the system signal flow-graphs when a_1 and a_2 are fed in turn at ports (1) and (2) respectively. a_1 and a_2 are the incident voltage waves, b_1 and b_2 are the reflected voltage waves at ports (1) and (2) respectively.

Applying signal flow graph analysis and non-touching-loop rule[3(8)] when a_1 is applied at port (1), the measured reflection and transmission coefficients are:

$$M_{R1} = \frac{b_1}{a_1}\Big|_{a_2=0} = M_{11} + \frac{M_{21}M_{12}}{D}\{S_{11}(1 - S_{22}N_{22}) + N_{22}S_{21}S_{12}\} \qquad 3.1$$

and,

$$M_{T1} = \frac{b_2}{a_1}\Big|_{a_2=0} = M_L + \frac{S_{21}}{D} M_{21}N_{12} \qquad 3.2$$

Similarly, when a_2 is applied at port (2) gives:

$$M_{R2} = \frac{b_2}{a_2}\Big|_{a_1=0} = N_{11} + \frac{N_{21}N_{12}}{D}\{S_{22}(1 - S_{11}M_{22}) + M_{22}S_{12}S_{21}\} \qquad 3.3$$

and

$$M_{T2} = \frac{b_1}{a_2}\Big|_{a_1=0} = N_L + \frac{S_{12}}{D} M_{12}N_{21} \qquad 3.4$$

where,

$$D = 1 - S_{11}M_{22} - S_{22}N_{22} - S_{21}S_{12}M_{22}N_{22} + S_{11}S_{22}M_{22}N_{22} \qquad 3.5$$

In Equations 3.1 - 3.5, some parameters appear only as a product, therefore it is not necessary to determine explicity the scattering parameters of the error equivalent networks[3(2)]. These parameters are $M_{21}M_{12}$, $M_{21}N_{12}$, $M_{12}N_{21}$ and $N_{21}N_{12}$. Consequently, the necessary parameters which have to be evaluated can be redefined as:

$$x_1 = M_{11} \qquad x_5 = N_{11}$$

$$x_2 = M_{21}M_{12} \qquad x_6 = N_{21}N_{12}$$

$$x_3 = M_{22} \qquad x_7 = N_{22}$$

$$x_4 = M_{21}N_{12} \qquad x_8 = M_{12}N_{21}$$

$$M = M_L \qquad N = N_L$$

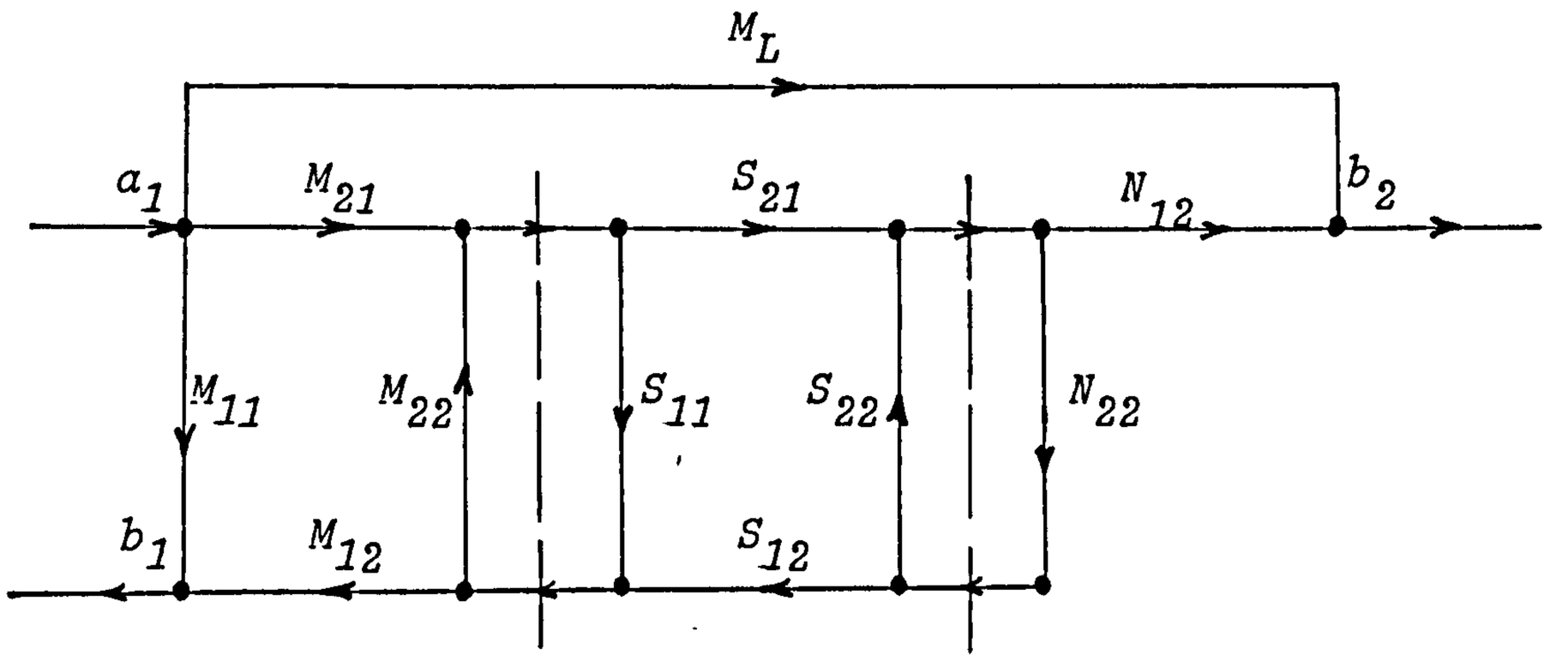

Fig. 3.2.a. Signal Flow Graph of Fig. 3.1.b. at $a_2 = 0$

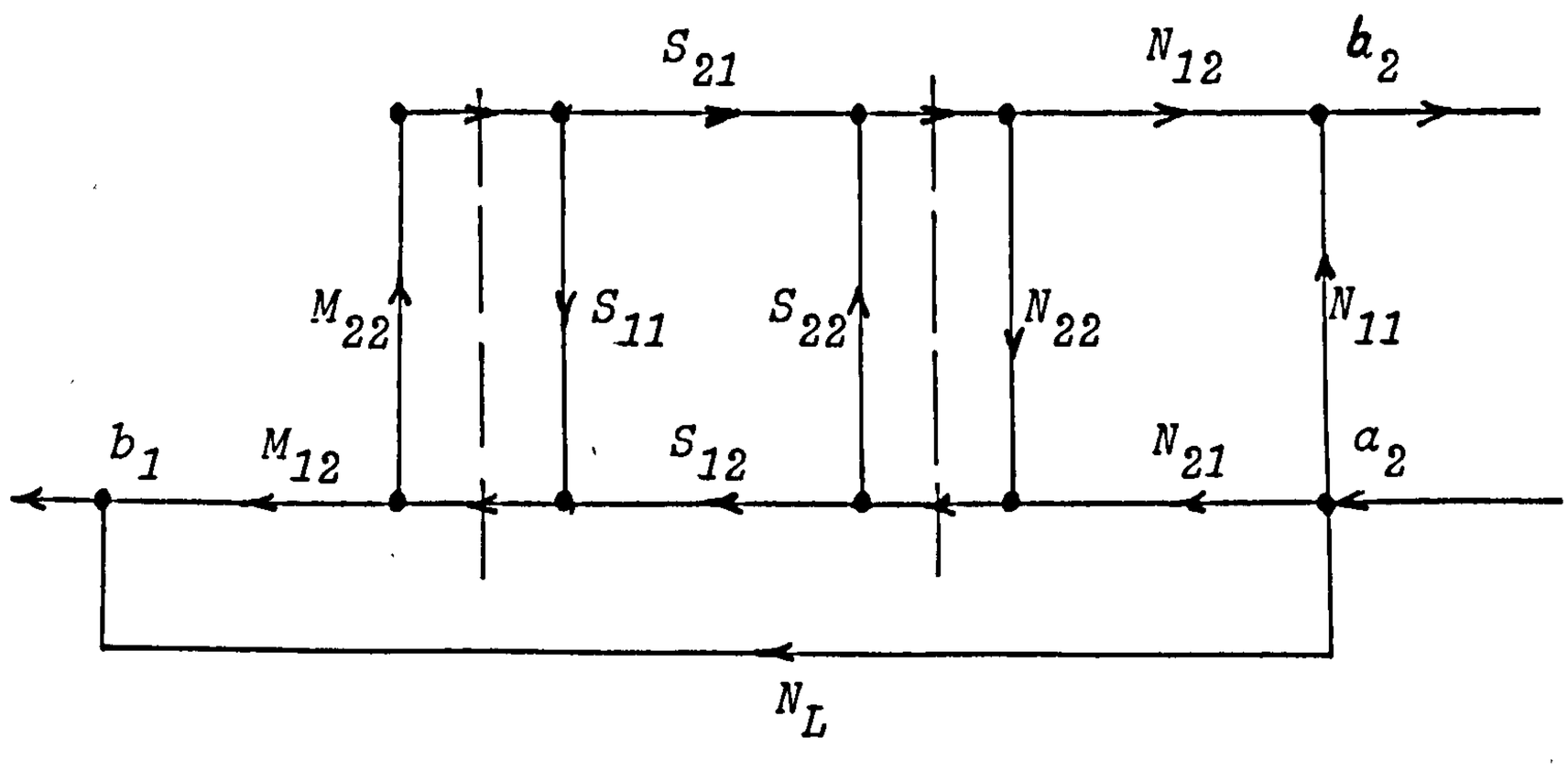

Fig. 3.2.b. Signal Flow Graph of Fig. 3.1.b. at $a_1 = 0$

Equations 3.1 - 3.5 then become:

$$M_{R1} = x_1 + \frac{x_2}{D}\{S_{11}(1 - S_{22}x_7) + x_7S_{21}S_{12}\} \qquad 3.1$$

$$M_{T1} = M + \frac{x_4}{D} \quad S_{21} \qquad 3.2$$

$$M_{R2} = x_5 + \frac{x_6}{D}\{S_{22}(1 - S_{11}x_3) + x_3S_{12}S_{21}\} \qquad 3.3$$

and

$$M_{T2} = N + \frac{x_8}{D} \quad S_{12} \qquad 3.4$$

where,

$$D = (1 - S_{11}x_3)(1 - S_{22}x_7) - x_3x_7S_{21}S_{12} \qquad 3.5$$

3.3. Calibration Procedure:

The equations needed to evaluate the necessary error-parameters, discussed in Section 3.2, and hence the scattering parameters of the device under test, can be obtained from the following calibration procedure[3(3,4)].

In this calibration, the test device is removed and the error networks are terminated in turn by the four-known-standards, namely matched-load, short-circuit, open-circuit and through line. The calibration sequence is as follows:

1. Matched-Load Termination:

$$(S_{11} = S_{22} = S_{21} = S_{12} = 0)$$

a. at port (1).

Equations 3.1 and 3.2 reduce to:

$$M_1 = x_1 \qquad 3.6$$

and $M_2 = M$ 3.7

b. at port (2).

Equations 3.3 and 3.4 reduce to

$$M_3 = x_5 \qquad 3.8$$

and $M_4 = N$ 3.9

2. Short-Circuit Termination:

$$(S_{11} = S_{22} = -1,\ S_{21} = S_{12} = 0)$$

a. at port (1)

Equation 3.1 reduces to:

$$M_5 = x_1 - \frac{x_2}{1 + x_3} \qquad 3.10$$

b. at port (2)

Equation 3.3 reduces to:

$$M_6 = x_5 - \frac{x_6}{1 + x_7} \qquad 3.11$$

3. Open-Circuit Termination:

$$(S_{11} = S_{22} = 1,\ S_{21} = S_{12} = 0)$$

a. at port (1)

Equation 3.1 reduces to:

$$M_7 = x_1 + \frac{x_2}{1 - x_3} \qquad 3.12$$

b. at port (2)

Equation 3.3 reduces to:

$$M_8 = x_5 + \frac{x_6}{1 - x_7} \qquad 3.13$$

4. Through-Line Termination:

$$(S_{11} = S_{22} = 0,\ S_{21} = S_{12} = 1)$$

a. at port (1)

Equation 3.2 reduces to:

$$M_9 = M + \frac{x_4}{1 - x_3 x_7} \qquad 3.14$$

b. at port (2)

Equation 3.4 reduces to:

$$M_{10} = N + \frac{x_8}{1 - x_3x_7} \qquad 3.15$$

Equations 3.6 - 3.15 are simultaneously solved in Appendix D, and the error-parameter values are:

$$M = M_2 \qquad 3.16$$

$$N = M_4 \qquad 3.17$$

$$x_1 = M_1 \qquad 3.18$$

$$x_2 = \frac{2(M_1-M_5)(M_7-M_1)}{(M_7-M_5)} \qquad 3.19$$

$$x_3 = \frac{M_5+M_7-2M_1}{M_7-M_5} \qquad 3.20$$

$$x_4 = (M_9-M_2)(1-x_3x_7) \qquad 3.21$$

$$x_5 = M_3 \qquad 3.22$$

$$x_6 = \frac{2(M_3-M_6)(M_8-M_3)}{(M_8-M_6)} \qquad 3.23$$

$$x_7 = \frac{M_6+M_8-2M_3}{(M_8-M_6)} \qquad 3.24$$

$$x_8 = (M_{10}-M_4)(1-x_3x_7) \qquad 3.25$$

where,

$$x_3x_7 = \frac{(M_5+M_7-2M_1)(M_6+M_8-2M_3)}{(M_7-M_5)(M_8-M_6)} \qquad 3.26$$

then, with the substitution of M, N, x_1,.. x_8, from Equations 3.16 - 3.26, into Equations 3.1 - 3.5, the s-parameters of the device under test can be obtained, therefore,

$$S_{11} = \frac{1}{x_3} \{1 - K(1 + dx_7)\} \qquad 3.27$$

$$S_{22} = \frac{1}{x_7} \{1 - K(1 + cx_3)\} \qquad 3.28$$

$$S_{12} = eK \qquad 3.29$$

and

$$S_{21} = fK \qquad 3.30$$

In which,

$$K = \{1 + cx_3)(1 + dx_7) - ef\, x_3x_7\}^{-1} \qquad 3.31$$

$$c = \frac{M_{R1} - M_1}{x_2} \qquad 3.32$$

$$d = \frac{M_{R2} - M_3}{x_6} \qquad 3.33$$

$$e = \frac{M_{T2} - N}{x_8} \qquad 3.34$$

and

$$f = \frac{M_{T1} - M}{x_4} \qquad 3.35$$

3.4 Computer Aided Measurements:

Equations of the error parameters and device S-parameters of Section 3.3 have been computer programmed and used as an analysis subroutine in a full Computer Aided Correction program available in the Department[3(10)]. To try the program, this computer aided correction program was applied to measure the S-parameters of H.P. 35821E NPN microwave transistor[3(9)] at various bias conditions in the 2.0 - 4.0 GHz frequency band.

Fig. 3.3 represents the measured S-parameters of this transistor at bias condtion, V_{CB} = 15V, I_C = 15mA. The measured parameters S_{21} and S_{12} and those given in the transistor's data sheet are also compared in Fig. 3.3.[3(9)] The measured S_{21} and S_{12} are smaller in amplitude and vary less with frequency. This is due to the different device measured here and that measured by the manufacturer, and the consideration of the leakage power transmitted through the measuring system; this leakage was neglected by the manufacturer during the transistor S-parameter measurements.

3.5. Discussion

Like the computer aided correction programs available, the disadvantage of the program implemented in this chapter is the requirement of the matched load termination, which is difficult to obtain at microwave frequencies. To overcome this disadvantage, a known terminating load will be used instead. This results in the device being characterized with respect to impedances $Z^{(1)}$ and $Z^{(2)}$, as shown in Fig. 3.4, where $Z^{(1)}$ and $Z^{(2)}$ are the frequency dependant impedances of the known terminating loads used, and Z_o is the measuring system characteristic impedance (50Ω).

The device scattering parameters with respect to the impedance Z_o can be obtained by representing the junction at A and B by their scattering parameters as shown in Fig. 3.5.

$$\text{Let } Z_1 = \frac{Z^{(1)}}{Z_o} \qquad 3.36$$

and

$$Z_2 = \frac{Z^{(2)}}{Z_o} \qquad 3.37$$

Hence,

$$S_{11}^{(1)} = \frac{Z_1 - 1}{1 + Z_1} \qquad 3.38$$

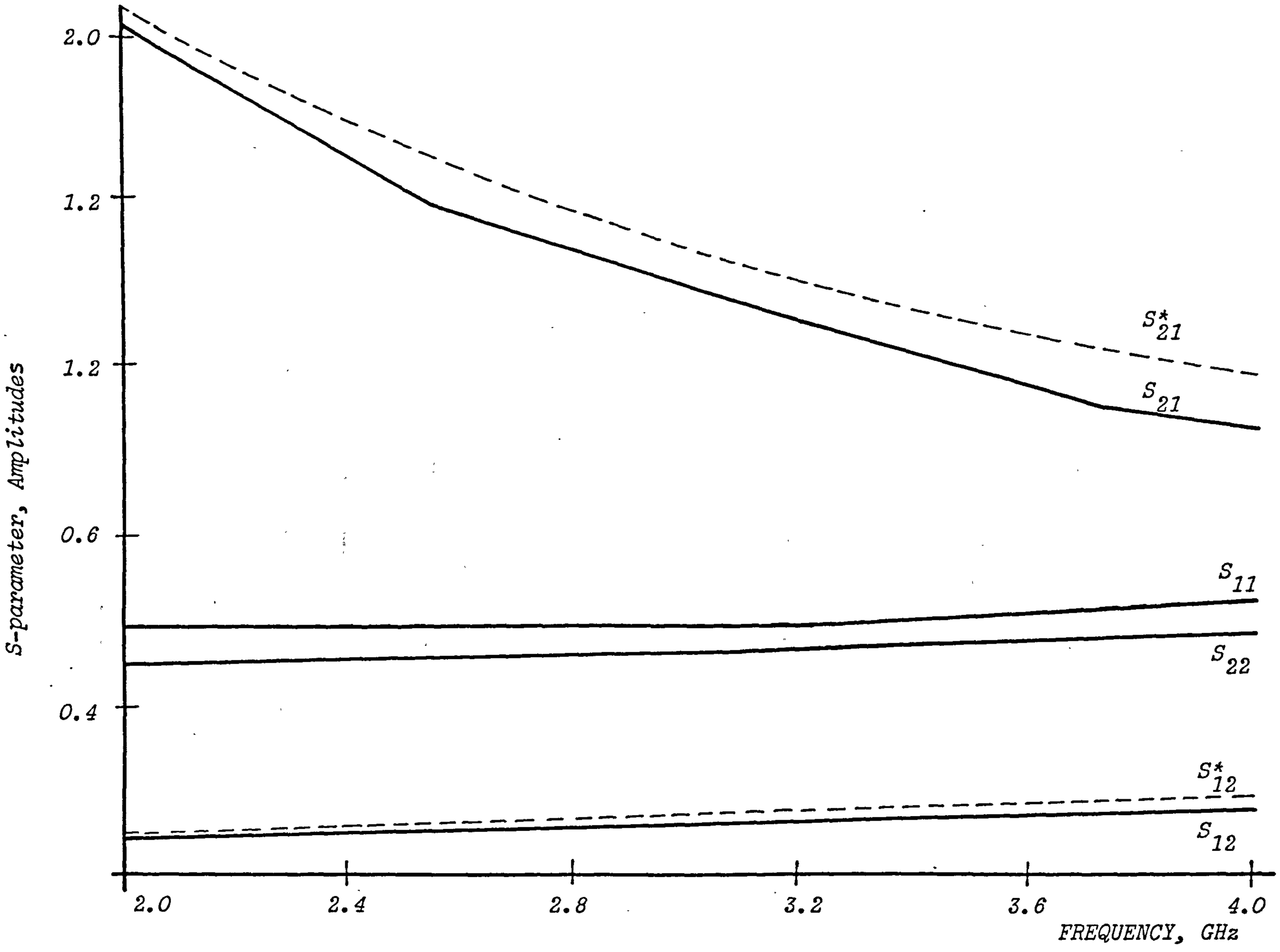

Fig. 3.3. The measured S-parameter of H.P. 34821E Transistor (I_C = 15mA, V_{CB} = 15V.)

* *Extracted from Transistor Data-Sheet.*[4(9)]

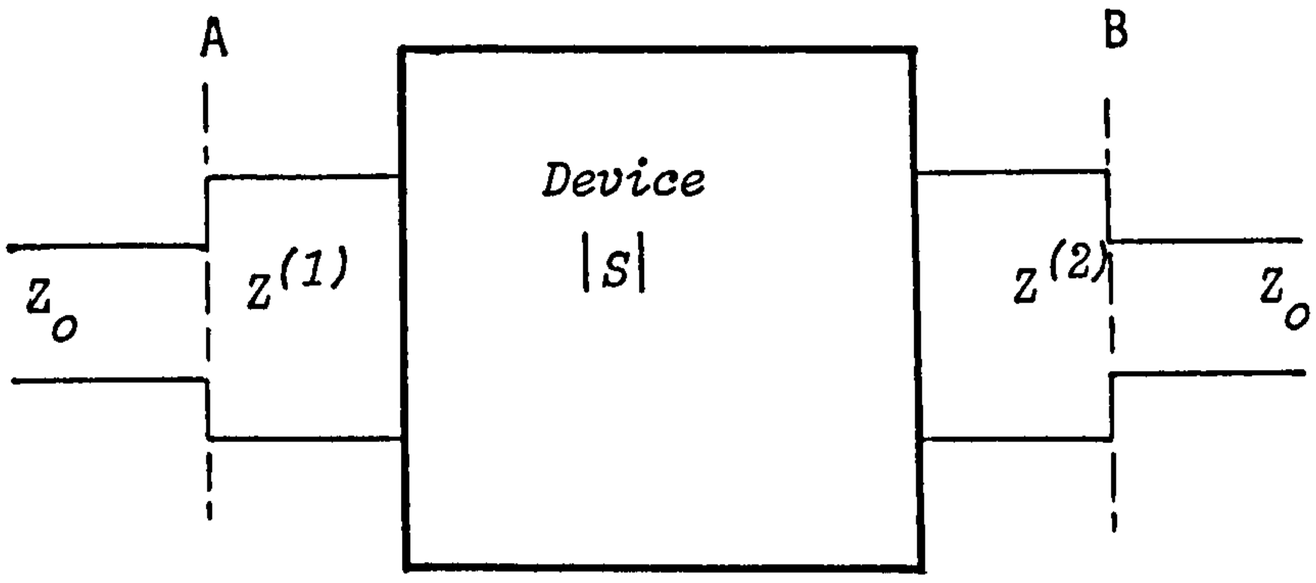

Fig. 3.4. Block Diagram of a Device at Mismatch Termination ($Z^{(1)} \neq Z_o$, $Z^{(2)} \neq Z_o$)

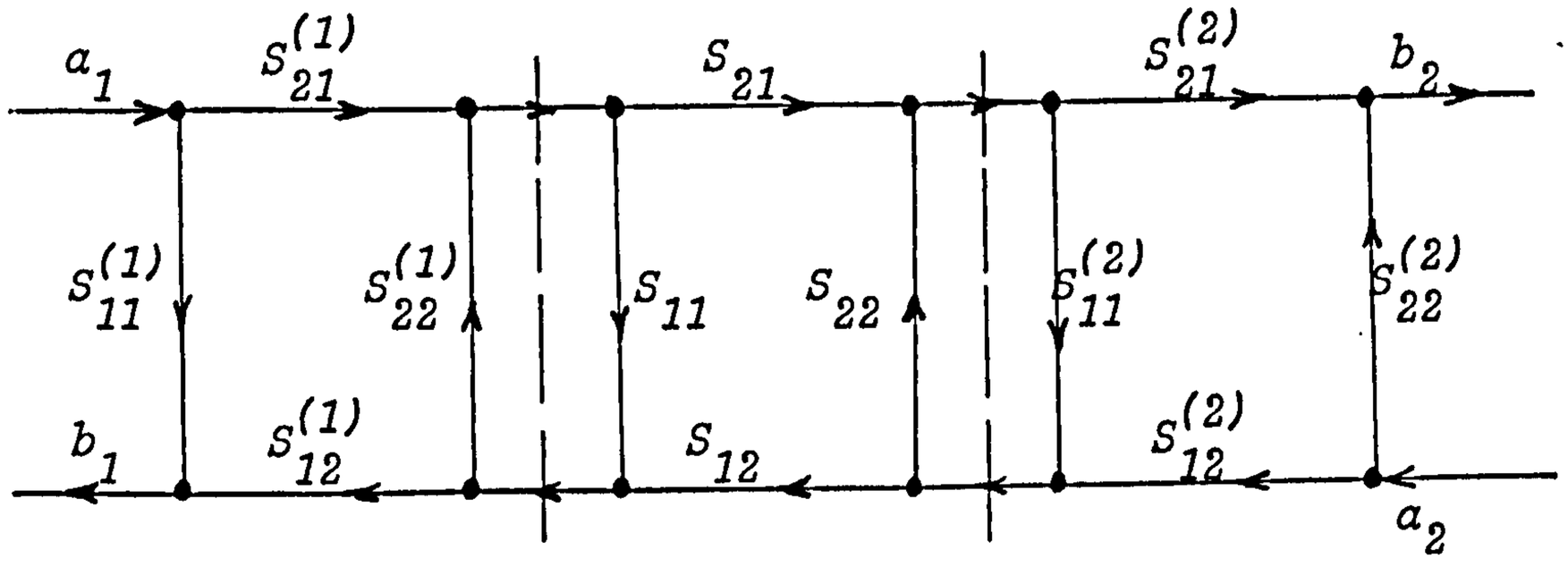

Fig. 3.5. Signal Flow Graph of Fig. 3.4.

$$s_{22}^{(1)} = \frac{1 - Z_1}{1 + Z_1} \qquad 3.39$$

$$s_{21}^{(1)} = (1 - s_{11}^{(1)}).\ \sqrt{Z} \qquad 3.40$$

$$s_{12}^{(1)} = (1 - s_{22}^{(1)}).\ \frac{1}{\sqrt{Z}} \qquad 3.41$$

and

$$s_{11}^{(2)} = \frac{1 - Z_2}{1 + Z_2} \qquad 3.42$$

$$s_{22}^{(2)} = \frac{Z_2 - 1}{1 + Z_2} \qquad 3.43$$

$$s_{21}^{(2)} = (1 - s_{11}^{(2)}).\ \frac{1}{\sqrt{Z_2}} \qquad 3.44$$

$$s_{12}^{(2)} = (1 - s_{22}^{(2)}).\ \sqrt{Z_2} \qquad 3.45$$

Applying signal flow-graph analysis and the non-touching loop rule to Fig. 3.5 gives the S-parameters at a 50-Ω plane.[3(8)]

Hence the S-parameters are:

$$S_{M11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = s_{11}^{(1)} + \frac{s_{21}^{(1)} s_{12}^{(1)}}{D} \{S_{11}(1 - S_{22}s_{11}^{(2)}) + s_{11}^{(2)} S_{21}S_{12}\} \qquad 3.46$$

$$S_{M21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{S_{21}}{D}\ s_{21}^{(1)} s_{21}^{(2)} \qquad 3.47$$

$$S_{M22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = s_{22}^{(2)} + \frac{s_{21}^{(2)} s_{12}^{(2)}}{D} \{S_{22}(1 - S_{11}s_{22}^{(1)}) + s_{22}^{(1)} S_{21}S_{12}\} \qquad 3.48$$

and

$$S_{M12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = \frac{S_{12}}{D}\ s_{12}^{(1)}\ s_{12}^{(2)} \qquad 3.49$$

where,

$$D = 1 - S_{11}S_{22}^{(1)} - S_{22}S_{11}^{(2)} - S_{21}S_{12}S_{22}^{(1)}S_{11}^{(2)} + S_{11}S_{22}S_{22}^{(1)}S_{11}^{(2)} \qquad 3.50$$

The implemented computer aided correction program of Section 3.3 is consequently modified to give direct S-parameters at the mismatch terminations. i.e. the measured S-parameters of the device under mismatch termination is converted into a 50-Ω plane in intermediate steps within the computer correction analysis.

3.6. Conclusion

In the computer aided correction program implemented in this Chapter, the leakage power transmitted through the measuring system, usually neglected, has been considered. The reference plane has been established at the device terminals in order to accurately measure the device scattering parameters. Four known calibration pieces namely matched-load, short-circuit, open-circuit and through line are needed to successfully evaluate the error parameters involved and hence to obtain the accurate S-parameter of a device.

The computer aided correction program has been extended and modified to overcome the matched-load difficulty at microwave frequencies. This program will be applied in Chapter 6 in measuring the S-parameters of the transistors described in Chapter 2.

A thin-film resistor will be characterized in the following Chapter and hence it will be used as a standard termination when measuring the S-parameters of the transistors. See Chapter 6.

3.7 REFERENCES

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CHAPTER 4

MODELLING OF A MICROWAVE STANDARD TERMINATION AT FREQUENCIES UP TO 8.0 GHz

4.1. Introduction

The objective of this study was to analyse a thin-film resistor produced by Tek-Wave from D.C. to frequencies up to 8.0 GHz. It was aimed to produce a lumped equivalent circuit model for the resistor and to study its frequency dependence as it was intended to be used as a calibrating standard when measuring the S-parameters of the transistors. This will be discussed in Chapter 6. In this analysis, for the measurements a reference plane is established at the resistor terminals. This was to eliminate all the parasitic components from the measurements.

A different computer aided correction program is needed here to maintain the required reference plane and to obtain measurements on the resistor free from the errors associated with the measuring system and those due to discontinuities.

An optimization routine is required to produce a lumped equivalent circuit which represents the thin-film resistor over frequencies up to 8.0 GHz.

4.2. Device and Package Description

The measuring system has to be calibrated before commencing parameter measurements on any device.[4(6,7)] In the case of a matched load calibration no reflected power should exist. Perfect matched loads are difficult to obtain at microwave frequencies[4(1,2)]. At these frequencies, a load resistor with known frequency dependence can be used instead, see Chapter 3.

A Tek-Wave chip resistor, type 20-0132-50, 50Ω with ± 2.0% accuracy has been chosen for this application[4(4)]. These resistors are deposited on 99.5% alumina substrates. The chip resistor and its proposed equivalent circuit model based on its structure are shown in Figs. 4.1 and 4.2 respectively.

The resistor-chip was mounted on a stud to facilitate measurements in the following manner.

1. The ground plane of the chip resistor was coated by a silver conductive epoxy, EPO-TEK-31 type.
2. The chip was placed on the stud header.
3. The chip and the stud were placed in an oven at 80°C for approximately 30 minutes.
4. The mounted resistor chip together with the stud were removed from the oven and left to cool for at least one hour.

The chip was then firmly mounted and ready to be measured.

4.3. Device Measurements and Calibrations.

The errors in a network-analyser system may be represented by assuming a perfect network analyser and a 2-port error network interposed between it and the device under test.[4(6,7)] The error network may be conveniently characterized in terms of its scattering parameters and will assume the form shown in Fig. 4.3. For calibration purposes, the test device is removed and the error network is terminated in turn by the three short circuits shown.[4(6)]

4.3.1. Measuring Jig.

The measuring jig was designed to provide only a small discontinuity between the mounted resistor chip discussed in Section 4.2, and the inner conductor of the OSM connector.[4(1,2)] A cross-section of this jig, is shown

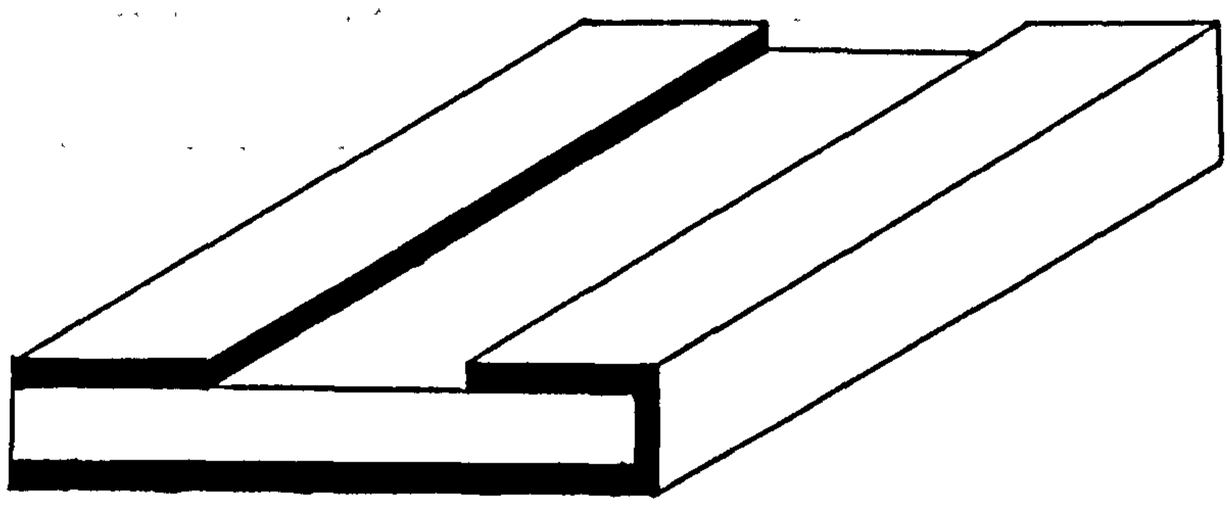


Fig. 4.1. A Tek-Wave Chip Resistor
(20 times full size)

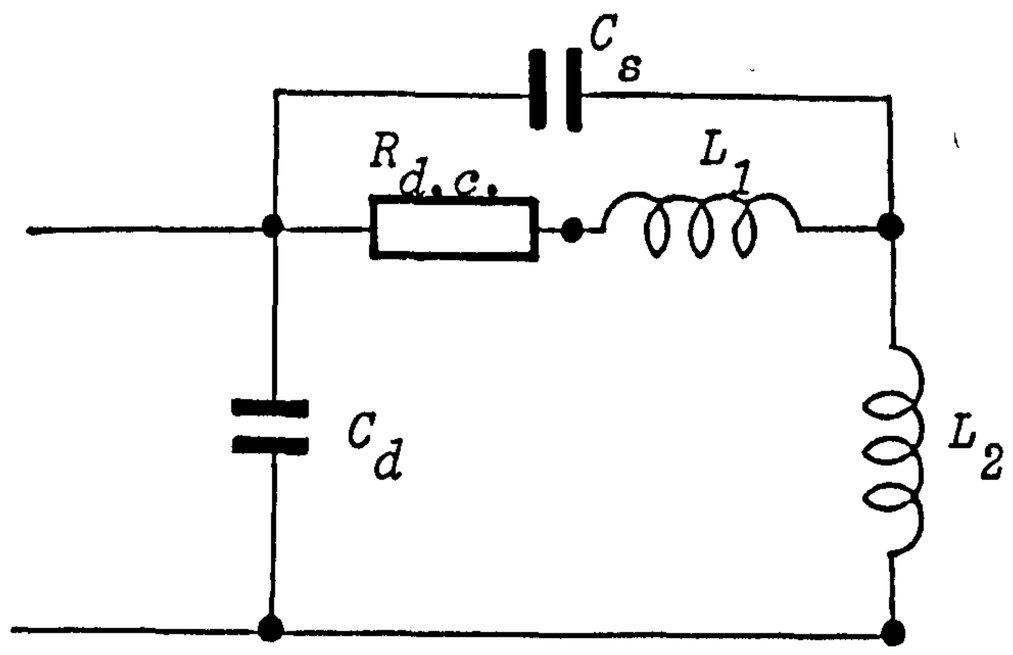


Fig. 4.2 The Proposed High-Frequency Equivalent Circuit Model

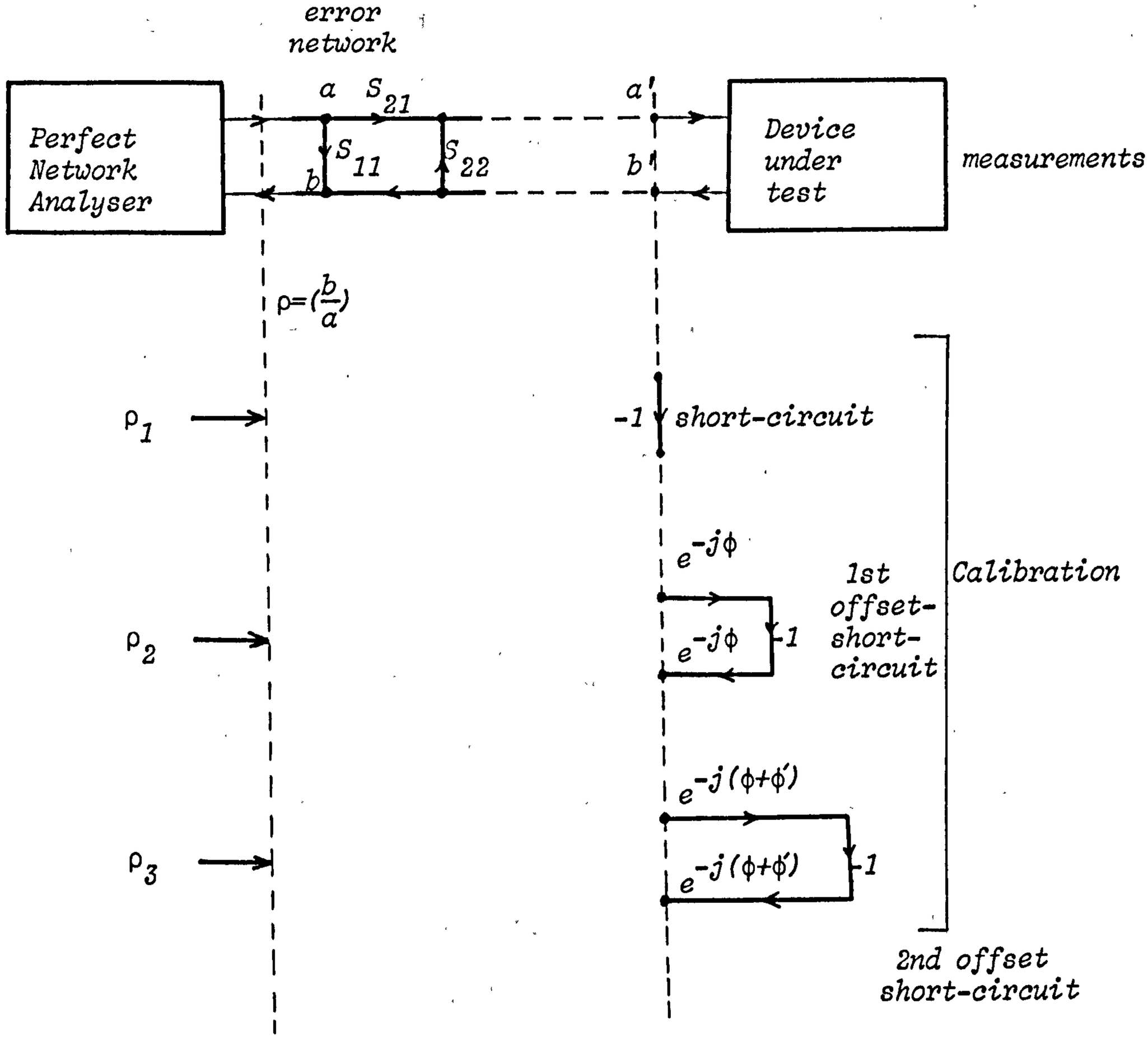


Fig. 4.3 Signal-Flow Graph of System under Calibration

in Figs. 4.4 and 4.5. Care has to be taken when bringing the resistor chip into contact with the OSM inner conductor. The successful method was to connect the measuring jig to the S-parameter test unit via the OSM connector and observe the trace movement on the polar display of the network analyser whilst turning the screw, at the opposite end of the jig, inwards gently. The trace should move towards the centre of the polar display. When perfect contact is made, the trace reaches a stable position near the polar display centre.

Fig. 4.5 represents the assembly diagram of the jig, the mounted chip-resistor and the OSM connector during measurements and the complete proposed equivalent circuit model of the resistor under test.

4.3.2. Computer Aided Correction Program

Several computer-aided correction programs are available to be used in these kind of measurements[4(6,7)]. One, is the two-short and one open circuit correction program.[4(7)] It was recommended by previous investigators[4(6)] to use the three-short-circuit, one direct and two off-sets, computer aided correction program to avoid open-circuit difficulties at microwave frequencies. The three shorts, one direct and two off-sets, required for the H.P. Network analyser calibration prior to the load resistor measurement were designed and investigated. A 50-Ω air line was maintained in these off-set shorts. The centre conductor of the off-set shorts has the same diameter as that of the OSM connector to reduce the discontinuity effect during calibration. The off-set shorts consist of two parts, the inner and outer conductors. It was found that to obtain perfect connection between these parts, the inner part of the two offsets was machined with an annular recess which was filled with solder and then placed inside the outer parts. The off-set shorts were then gently heated at the opposite ends in order to prevent the melted solder

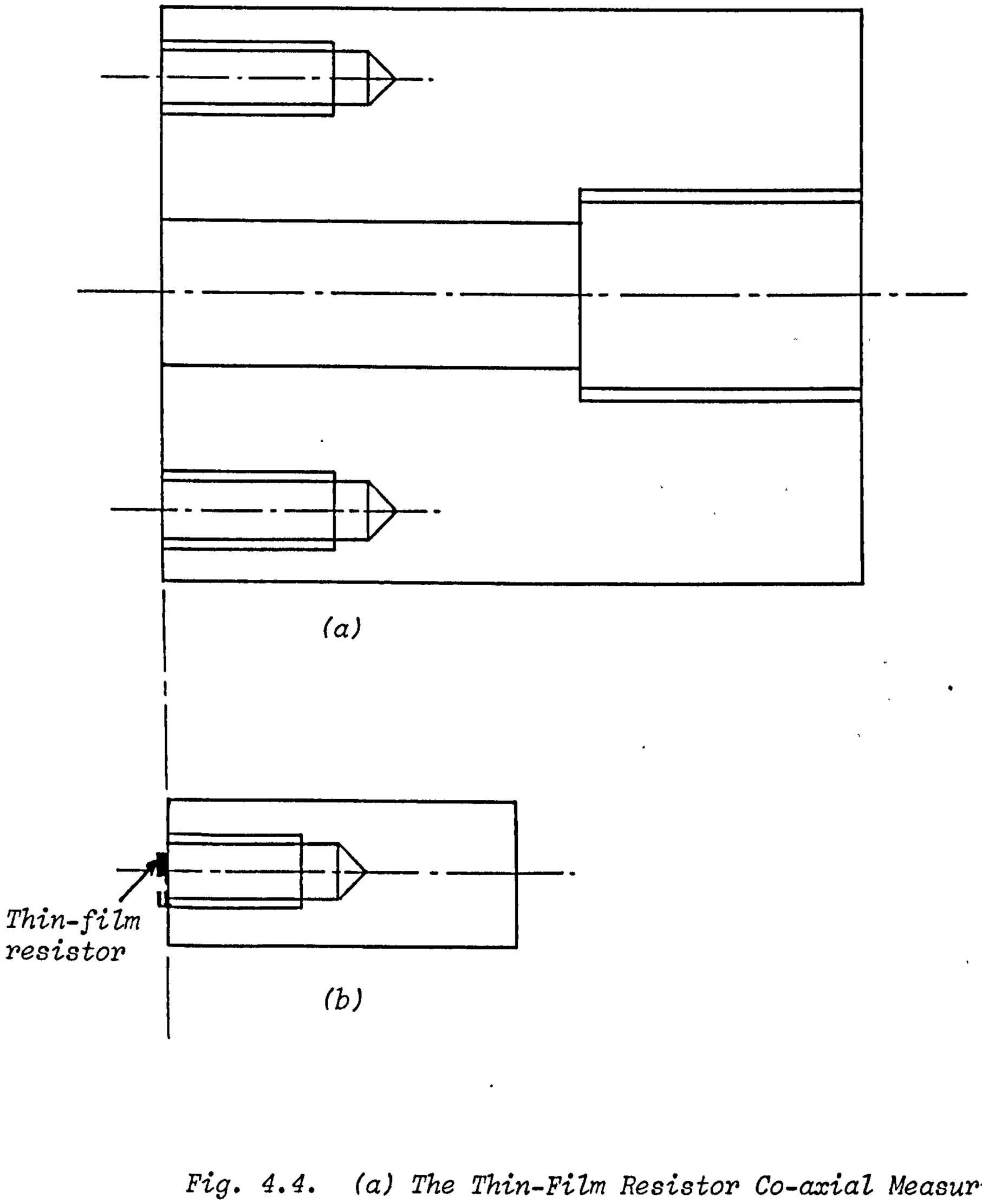
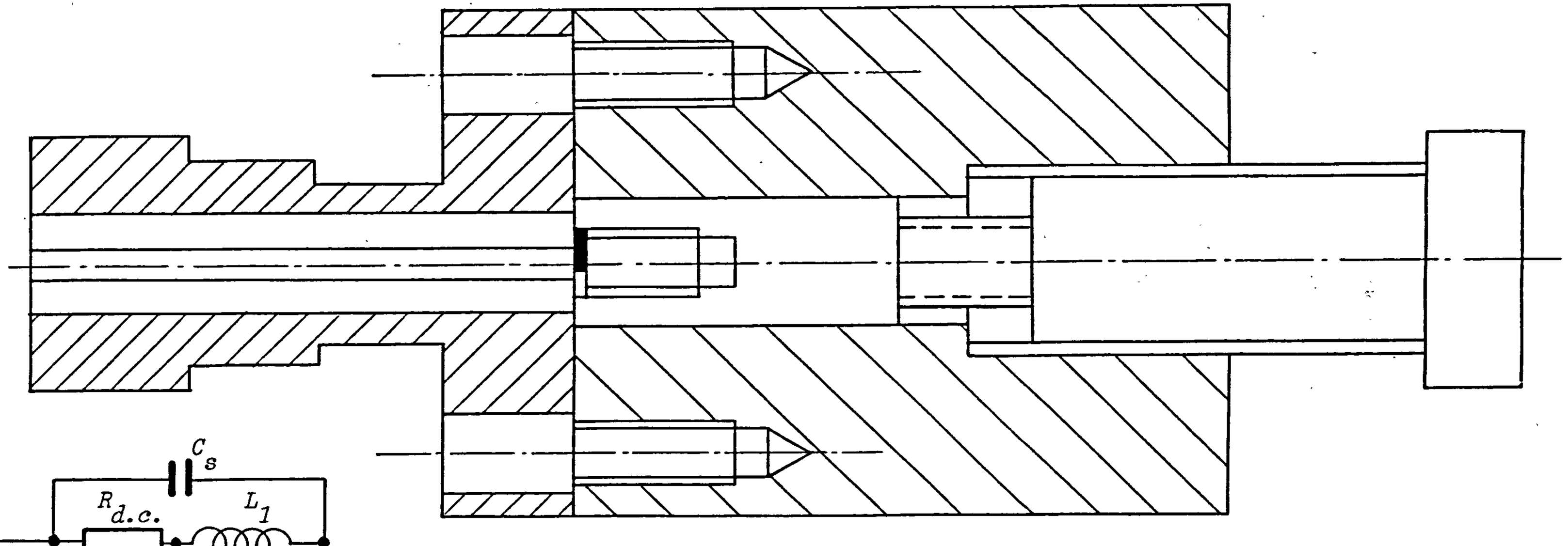
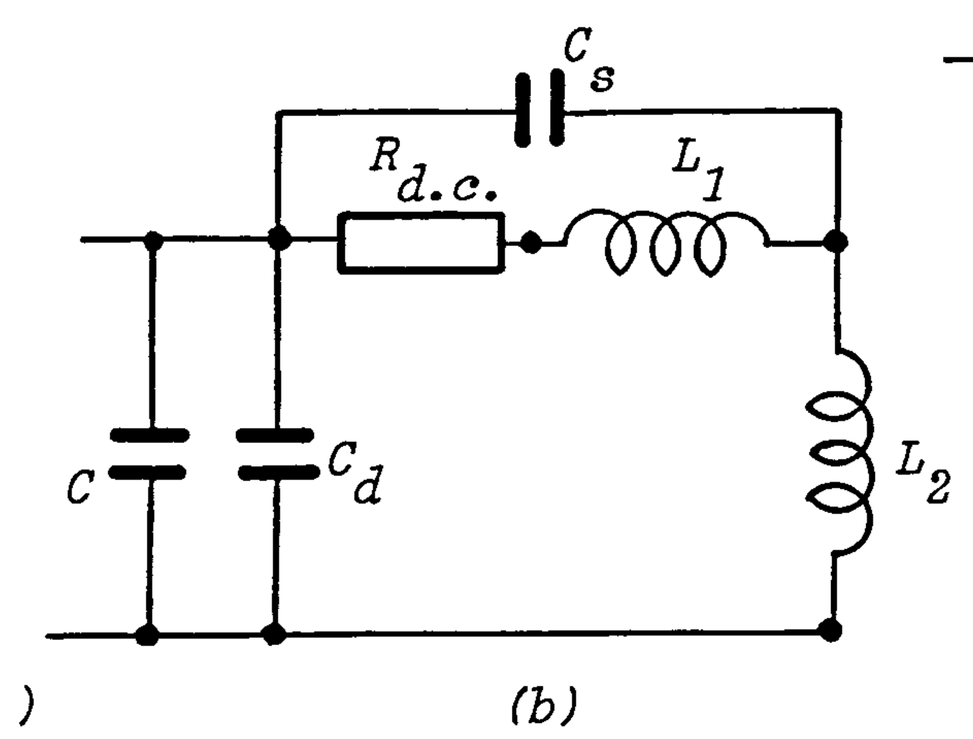


Fig. 4.4. (a) The Thin-Film Resistor Co-axial Measuring-Jig.
(b) The Thin-Film Resistor Mounted on the Stud.
(5 times full size)



(a)



)

(b)

Fig. 4.5. *a. The Arrangement of the Thin-Film Resistor under Measurement (4 times full size)*
b. The Complete Equivalent Circuit

from overflowing onto the centre conductors of the inner parts. The process was checked from time to time under the microscope to ensure the result. The direct short and the two off-set shorts were gold plated for better electrical contact.[4(4)]

Fig. 4.6 represents the cross-section of the two off-set short circuits used in system calibration.

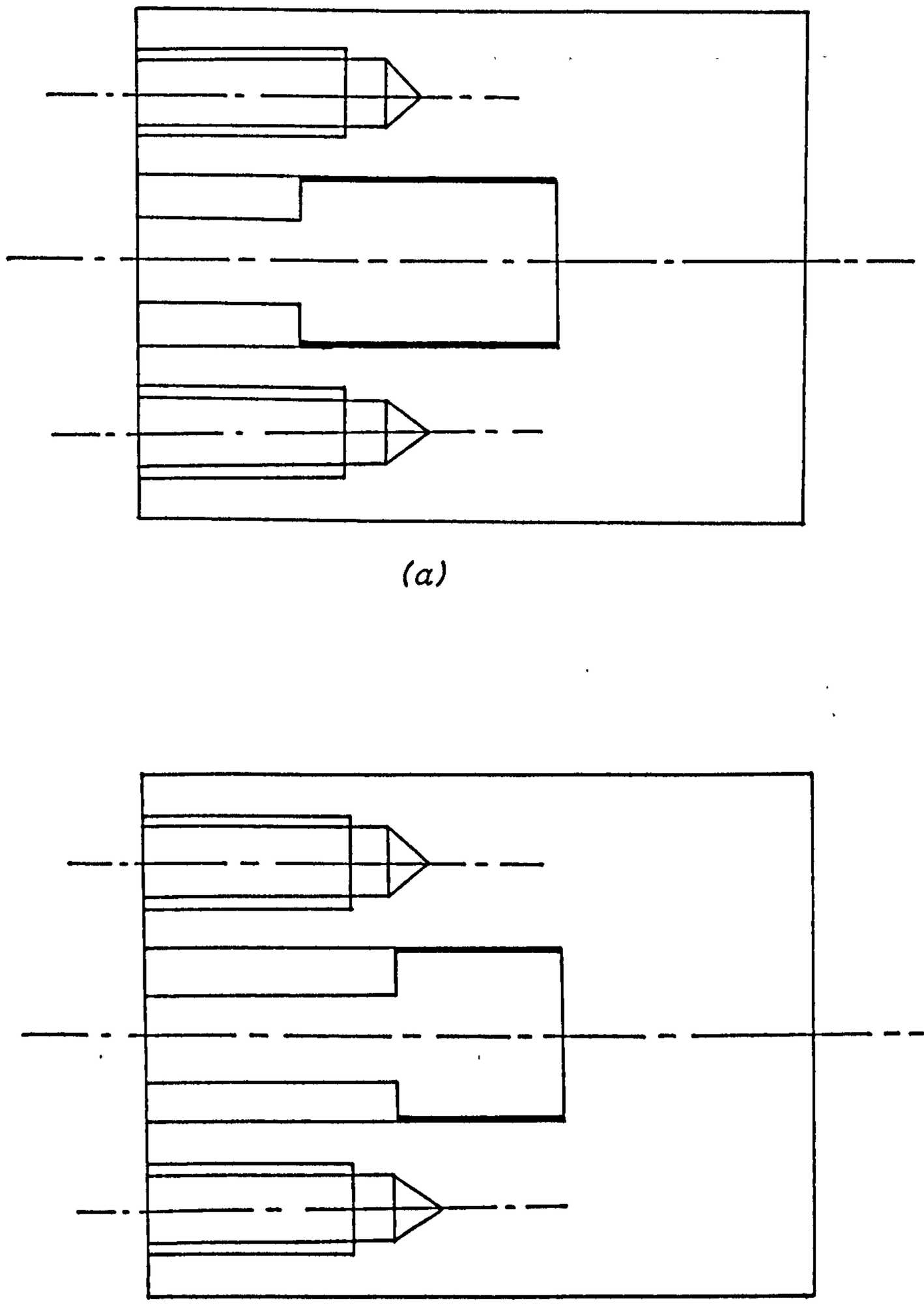
4.3.3. Measurements and Results

Before commencing reflection coefficient measurements on the thin-film resistor, the H.P. Network Analyser measuring system has to be calibrated[4(6)]. In the calibration procedure, Port (1) of the S-parameter test unit is terminated in turn by a direct short, an off-set with small off-set length and finally by the remaining off-set short, discussed in Section 4.3.2.

The stud, where the thin-film-chip resistor is mounted, was placed in the measuring jig. This jig was then connected at port (1) of the S-parameter test unit via the OSM connector, see Fig. 4.5.

The measuring system was calibrated and the reflection coefficient, amplitude and phase, of the thin-film resistor was measured at twenty-one frequency points over the frequency band (2.0 - 4.0 GHz). The three-short-circuit analysis routine utilizing the on-line facilities of the Sigma V was used.[4(6)] The amplitude and phase of the measured reflection coefficients, uncorrected and corrected, are shown in Fig. 4.7. The curves have been drawn through all the measuring points,which have been omitted for clarity. The scatter on the measured points is less than the line thickness.

The calibration procedure for the measuring system was repeated several times and the thin-film resistor was measured after each calibration



(a)

(b)

Fig. 4.6. Cross-Section of the Off-Set short circuits

(a) 1st Off-Set short (l = 1.0 cm)

(b) 2nd Off-Set short (l = 1.5 cm)

(twice full size)

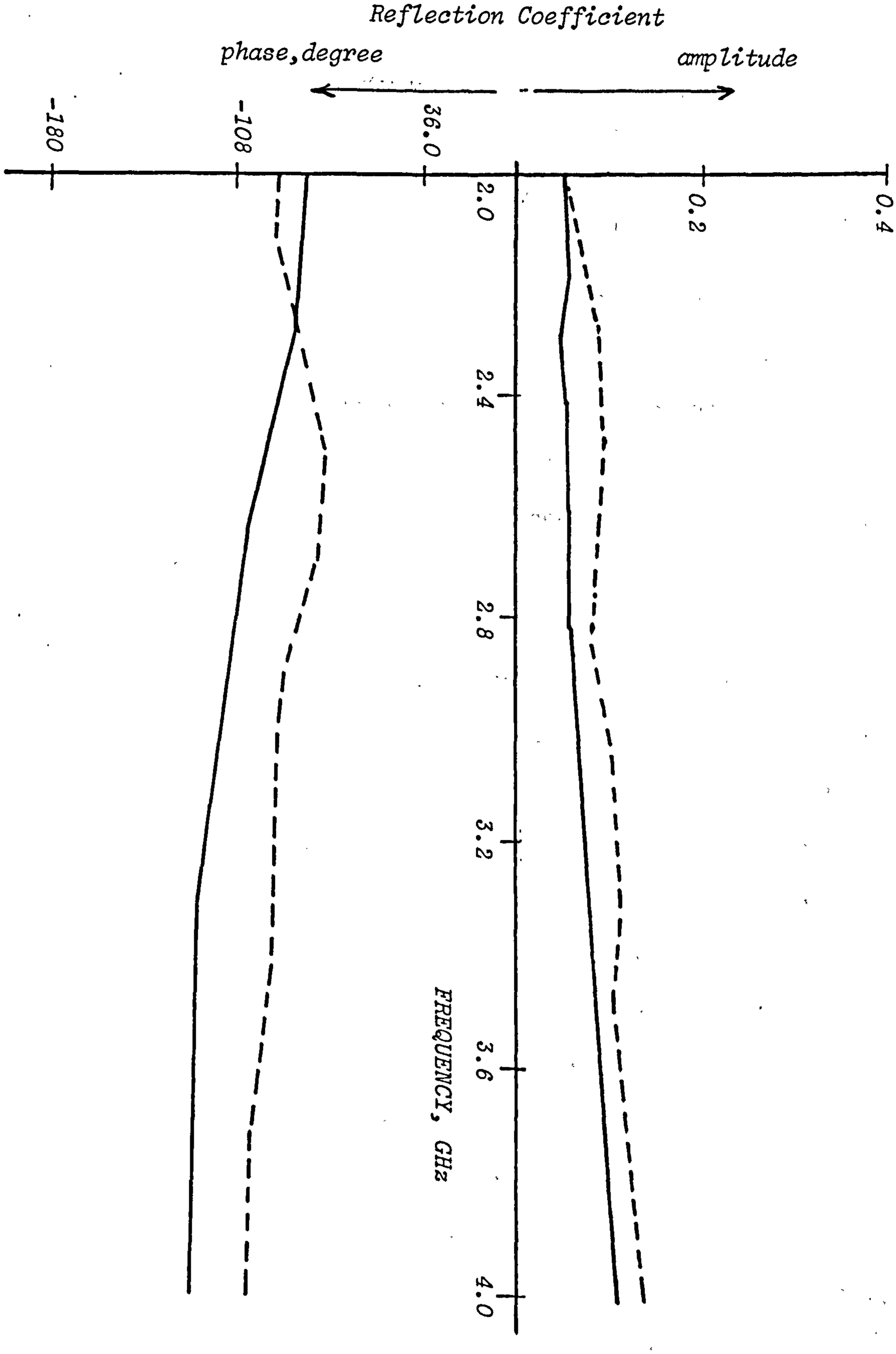


Fig. 4.7 Thin-Film REsistor Reflection Coefficient
---- (Uncorrected)
—— (Corrected)

over the frequency band (2.0 - 4.0 GHz). This was to ensure the repeatability and the constancy of the measurements. Such measurements are shown in Fig. 4.8. The measured reflection coefficients of Fig. 4.8, agree with those shown in Fig. 4.7, showing the repeatability of the measurements obtained after each calibration.

Generally, the corrected result is mainly dependent on the accuracy and the frequency dependence of the short circuit pieces used in calibration.[4(6)] No significant scattering in the corrected results over the frequency band concerned could be observed. The corrected reflection coefficient increases steadily with the operating frequency as expected from the proposed equivalent circuit of Fig. 4.2. The polar display of the reflection coefficient of each calibration piece of frequencies up to 8.0 GHz showed that its phase was proportional to frequency, and no losses could be observed. This indicates the three shorts, one direct and two off-set lengths, used in calibration are perfect and they are frequency independent. Therefore, these shorts are successfully designed.

Again, the measuring system was calibrated using the three-shorts calibration pieces and then the reflection coefficient of the thin-film resistor was measured at 41 frequency points over the frequency band 4.0 → 8.0 GHz. The amplitude and phase of the uncorrected and corrected reflection coefficients are shown in Fig. 4.9.

Due to the limited sweep ranges of the H.P. oscillator the reflection coefficient of the thin-film-resistor was measured in two frequency bands, namely 2 - 4 GHz and 4.0 - 8.0 GHz. Consequently, each frequency band of the sweep oscillator has to be calibrated separately.

At frequencies below 2.0 GHz, the thin-film resistor reflection coefficient values were obtained by extrapolating the corrected results of Fig. 4.7. In the 2.0 - 4.0 GHz band, the amplitude and phase of the

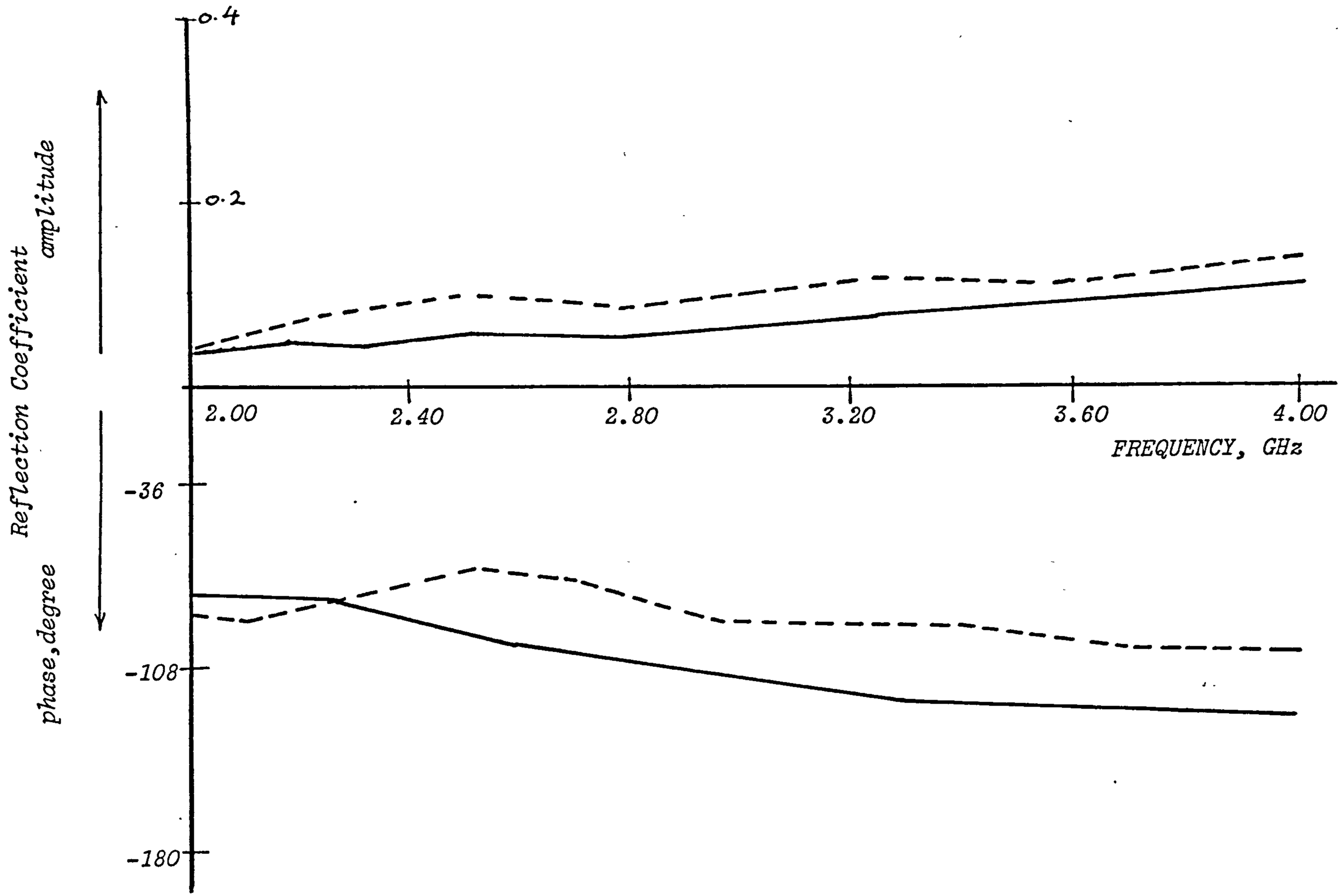


Fig. 4.8 The Repeatability of the Reflection Coefficient
---- (Uncorrected)
—— (Corrected)

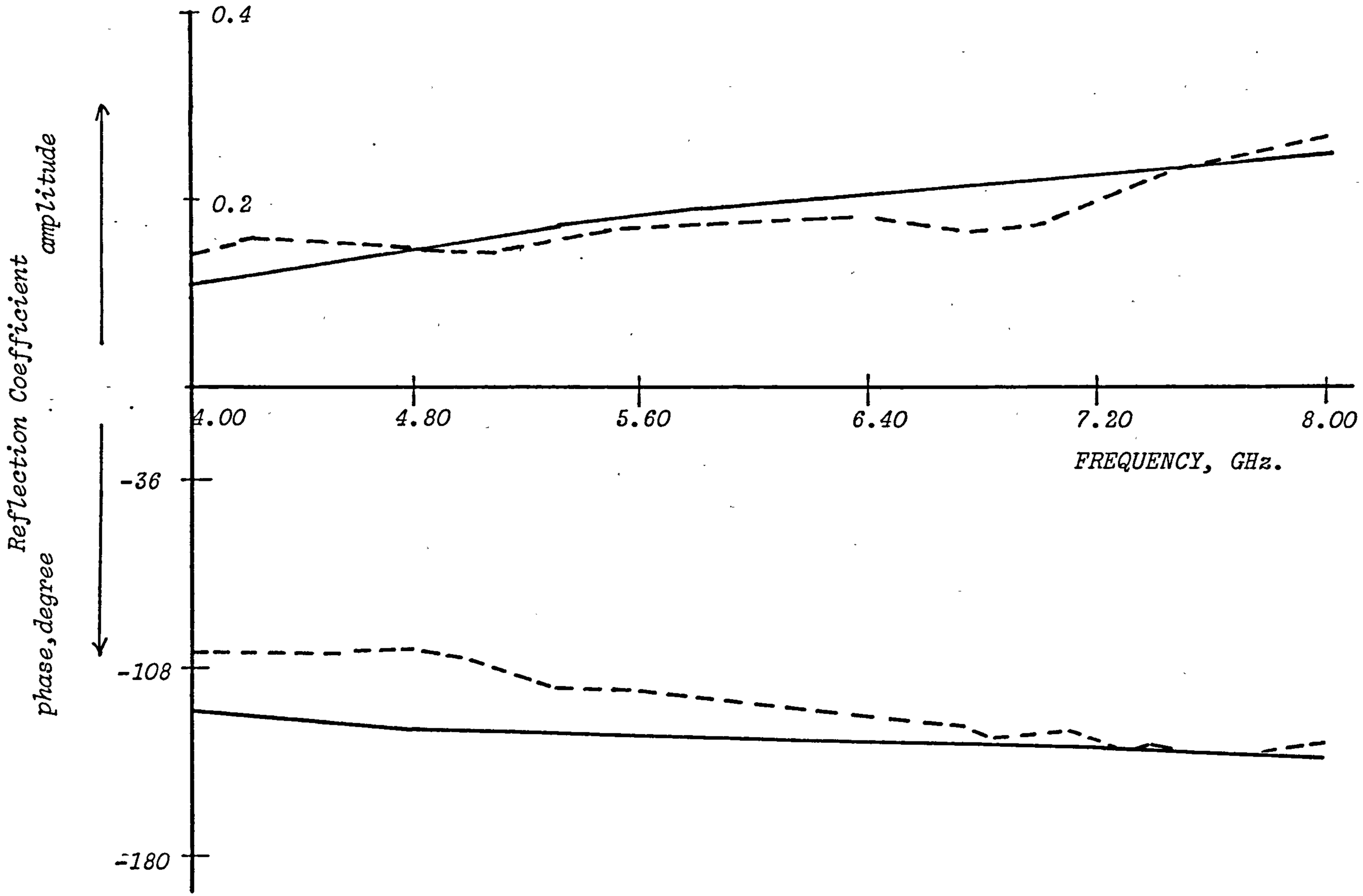


Fig. 4.9 Thin-Film Resistor Reflection Coefficient
---- (Uncorrected)
—— (Corrected)

reflection coefficient approximately increases linearly as the operating frequency increases. The amplitude is approximately doubled as the frequency increases by a factor of 2. The phase decreases by an average of +5.0 degree/200 MHz at the selected frequency points up to 3.0 GHz. This increase is fluctuating in the frequency range 3.0 - 4.0 GHz. The extrapolated amplitude and phase of the reflection coefficient at frequencies from D.C. up to 2.0 GHz are shown in Fig. 4.10. Manual measurements on the thin-film resistor were carried out to ensure the validity of the extrapolated results at selected frequency points up to 2.0 GHz. These measurements are also shown in Fig. 4.10.

4.4. Lumped Equivalent Circuit Model

The short-circuit pieces discussed in Section 4.3.2, required for system calibration, were satisfactorily constructed. The reflection coefficients, amplitude and phase, of the thin-film resistor have been measured and successfully corrected for the errors associated with the measuring system. See Section 4.3.3.

Next was to produce a lumped equivalent circuit model which represents the thin-film resistor over the frequency range up to 8.0 GHz. The proposed equivalent circuit model shown in Fig. 4.2. was considered. In this model, R was taken as the d.c. resistance of the thin-film resistor and has been measured to be 51Ω. C_d is the dielectric capacitance. C_s is the capacitance across the metalization. L_1 and L_2 are the thin-film and the metalization inductances respectively. The above components, namely, R, C_s, D_d, L_1 and L_2 represent the resistor alone. During measurement an additional capacitor C, is involved, see Fig. 4.5. This capacitance represents the parallel plates C_p and the fringing C_f capacitances at the point of discontinuity, plane of measurements.

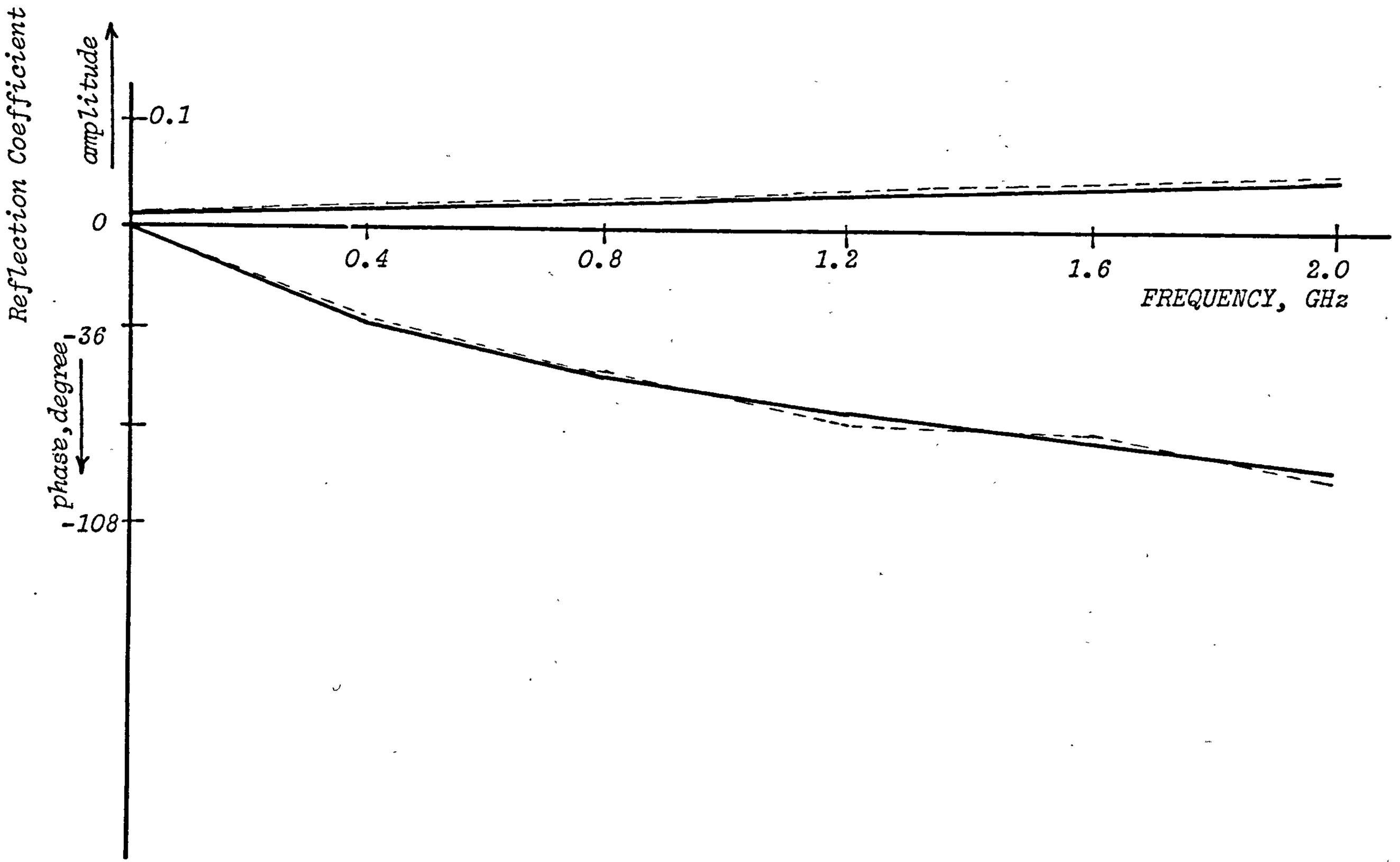


Fig. 4.10 Thin-Film Resistor, Reflection Coefficient
---- (Manual Measurements)
—— (Extrapolated).

Since the chip resistor cross-section is slightly smaller than that of the OSM centre conductor, the parallel plates capacitance C_p approximately reduces to half of its value, due to the arrangement of measuring the chip-resistor, see Fig. 4.5. The C_f and C_p capacitances can be calculated from the following equations[4(5)].

$$C_p = \frac{\Pi}{8} \cdot (D_1)^2 \cdot \left(\frac{\epsilon_o}{2d}\right) \qquad 4.1.$$

and

$$C_f = \epsilon_o \cdot D_1 \cdot \ell n \left(\frac{D_2 - D_1}{2d}\right) \qquad 4.2.$$

where,

ϵ_o = permitivity of free space, 8.85×10^{-12}F/m.

D_1 = OSM inner conductor diameter, 1.3 mm.

D_2 = OSM outer conductor diameter, 4.1 mm.

d = chip thickness, 0.351 mm.

The solution of Equations 4.1 and 4.2 give, $C_p = 1.67 \times 10^{-16}$F and $C_f = 1.592 \times 10^{-14}$F. As these capacitances are in parallel in the equivalent circuit of Fig. 4.5, they can be combined in one capacitance. The resultant capacitance is 1.6087×10^{-14}F which is approximately C_f.

4.5. Equivalent Circuit Optimization

The circuit model of Fig. 4.5 is considered to represent the thin-film resistor at frequencies up to 8.0 GHz. The component values of this circuit model, from which R and C are known, have to be optimized to give an agreement between the measured and calculated reflection coefficients.

The d.c. resistance R of the thin-film resistor was measured to be 51Ω. C is approximately the fringing capacitance C_f at the point of discontinuity during measurements and it was calculated in Section 4.4 to be 0.016 pF. The remaining components C_d, C_s, L_1 and L_2 cannot be

theoretically calculated. An optimization programme called "OPTIMAL" was applied to optimize these components to approximate ly give the measured reflection coefficient at frequencies up to 8.0 GHz.

The OPTIMAL method is a direct search in conjunction with a conjugate gradient method developed in the department.[4(3)]

To carry out the optimization initial values for the components, namely, C_d, C_s, L_1 and L_2 have to be set up. Table 4.1 shows the initial and optimized circuit component values.

The measured and optimized reflection coefficients, amplitudes and phase, are compared in Figs. 4.11 - 4.14, at frequencies up to 8.0 GHz.

The agreement between these results is very satisfactory.

The author concludes, the proposed equivalent circuit model discussed in Section 4.4 and its component values obtained in this section accurately represents the thin-film resistor at frequencies up to 8.0 GHz.

4.6. Discussion and Conclusion

The reflection coefficient of the thin-film resistor has been successfully measured in a coaxial mount. An equivalent circuit model which represents the thin-film resistor has been obtained at frequencies up to 8.0 GHz.

The discontinuity effects at the plane of the measurement have been included in the equivalent circuit model, discussed in Section 4.3.3 and optimized in Section 4.5.

The thin-film resistor characterized in this chapter is a very poor matched load for precision measurements.

Similar thin-film resistors will be mounted on a strip-line package and will be designed and discussed in Chapter 5. In Chapter 6, the packaged thin-film resistor will be used as a known calibrating standard in the

Table 4.1

Thin-film Resistor Equivalent Circuit Element Values

Circuit Element	Initial Value	Optimized Value	Remarks
$R_{d.c}$	51Ω	-	measured
C	0.016 pF	-	calculated
C_d	0.01 pF	0.17 pF	optimized
C_s	0.05 pF	0.2522 pF	optimized
L_1	0.1 nH	0.029 nH	optimized
L_2	0.01 nH	0.0062 nH	optimized

transistor measurements. The thin-film resistors are assumed to be identical in shape and size. The optimized component values of the equivalent circuit of Fig. 4.11, and shown in Table 4.1, will be valid except R. It varies from one resistor to another and it can be easily measured at d.c.

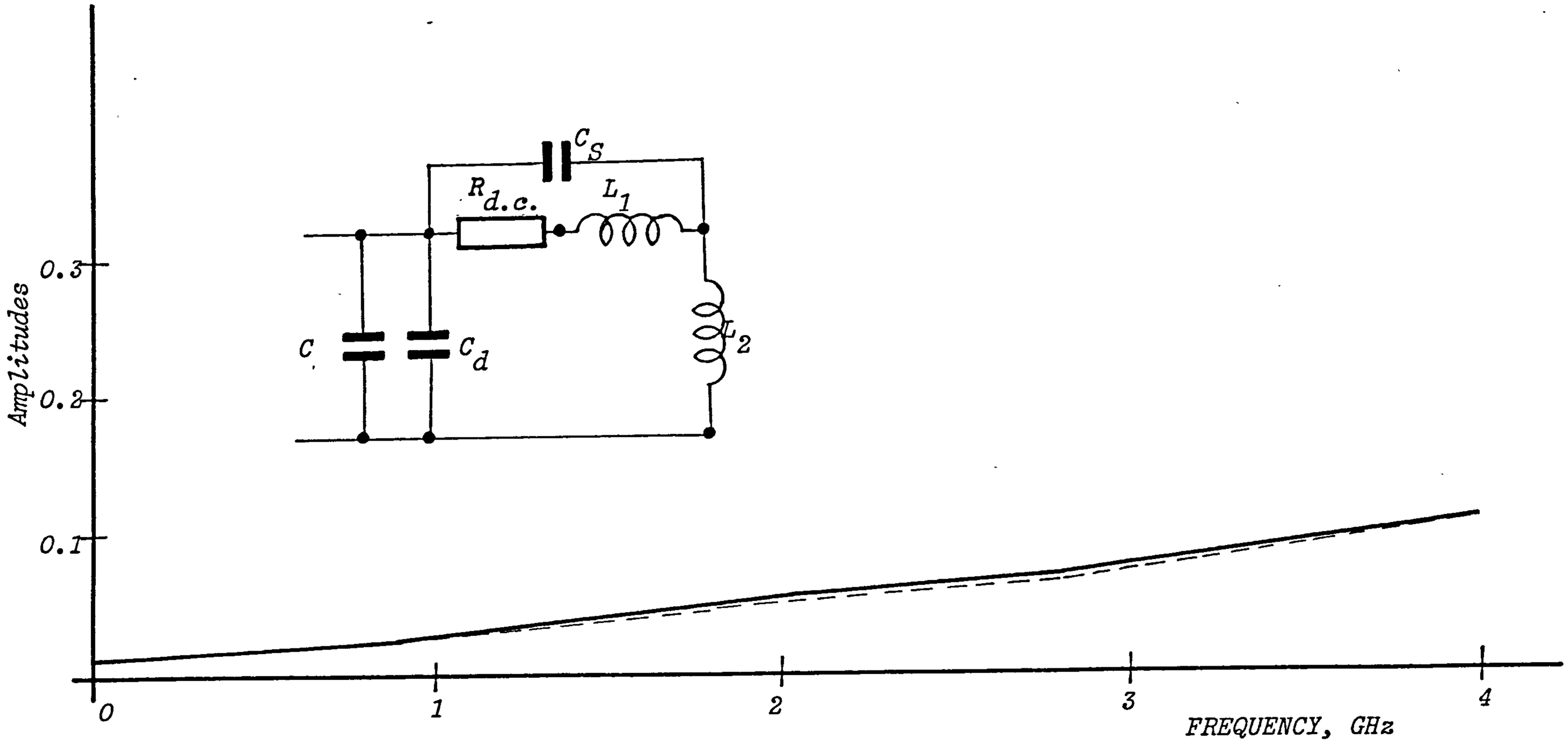


Fig. 4. 11 The Reflection Coefficient Amplitudes of the Thin-Film Resistor (D.C. - 4.0 GHz)

---- (measured) —— (Optimized)

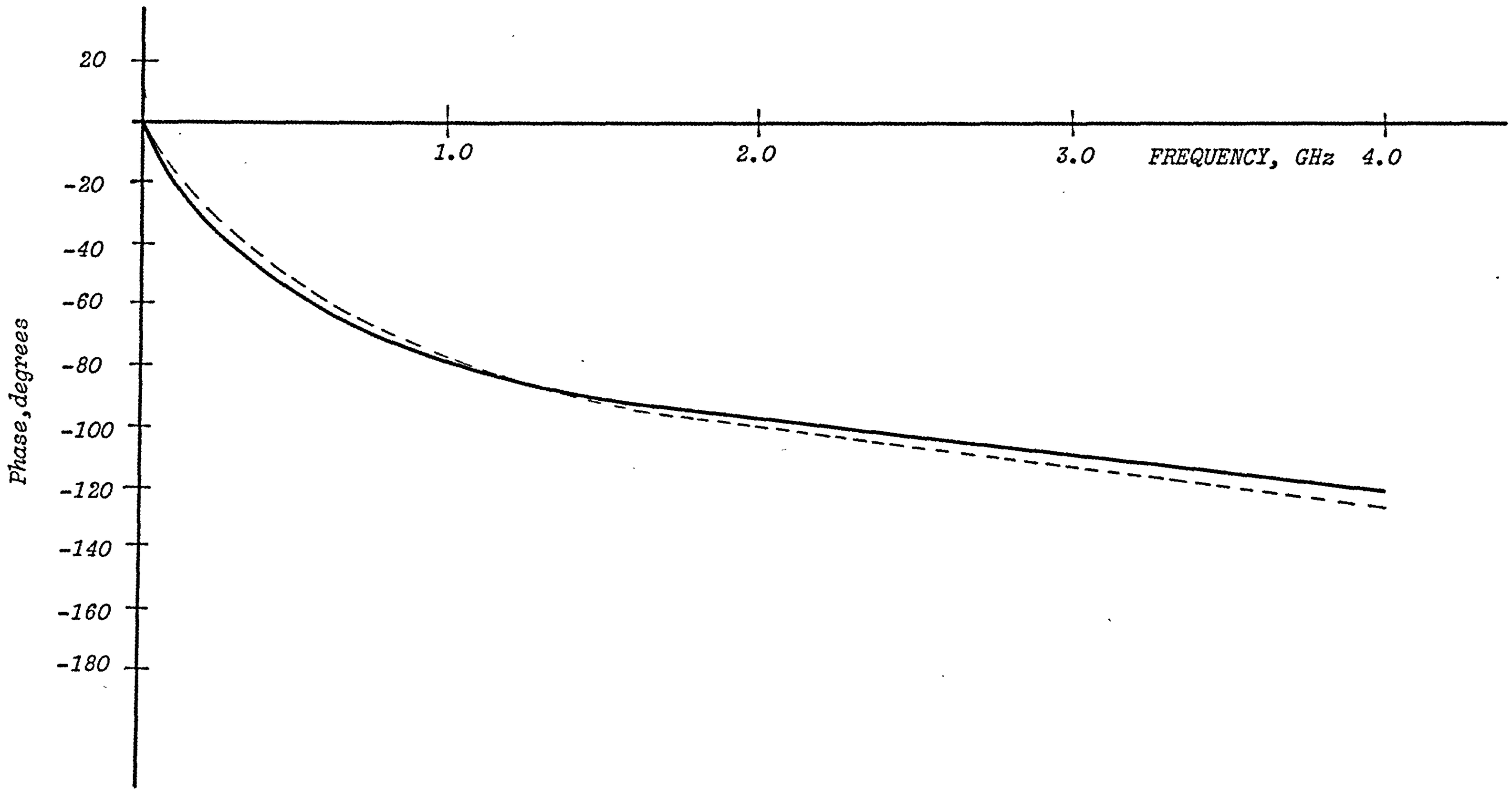


Fig. 4. 12 Thin-film Resistor Reflection Coefficient Phases
---- (Measured)
—— (Optimized)

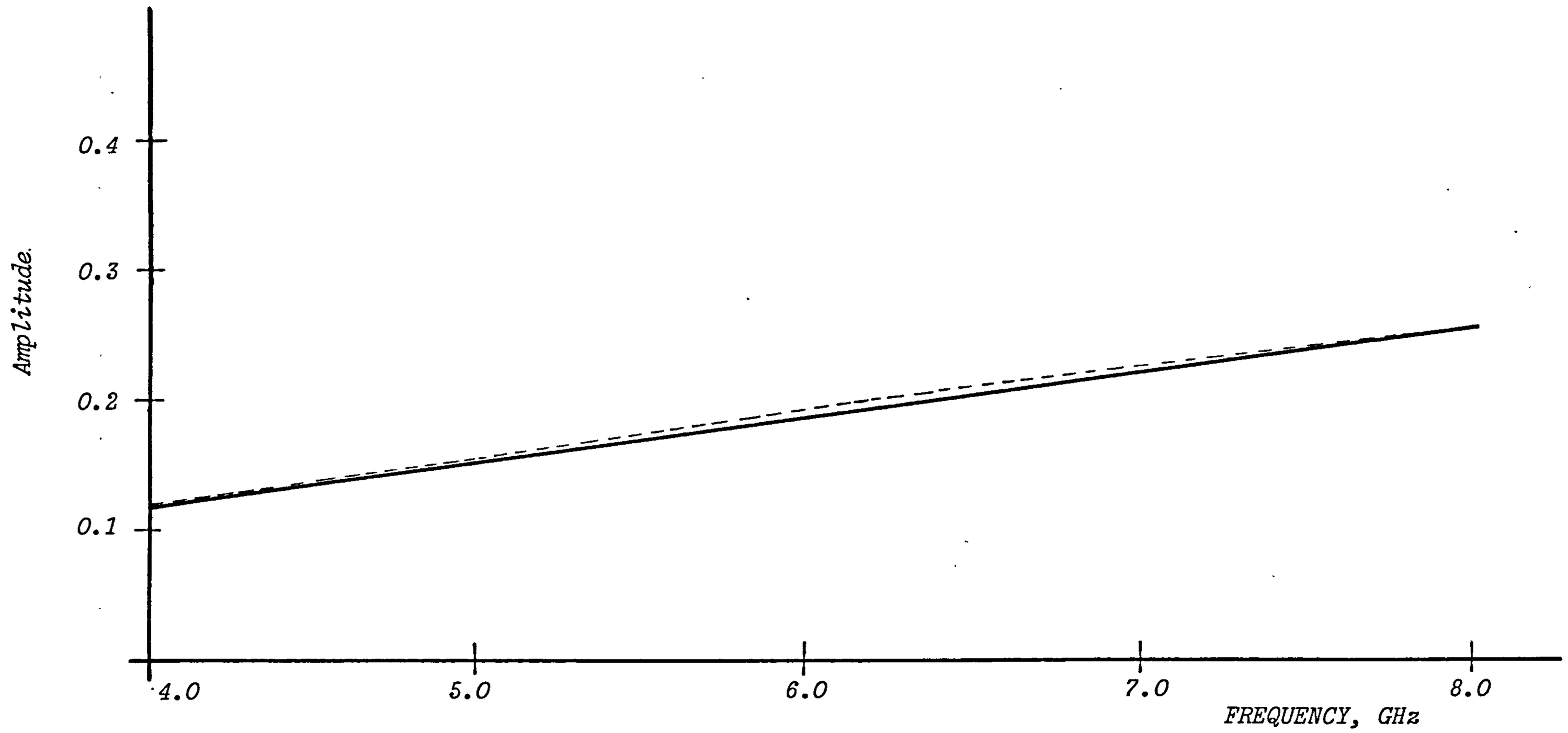


Fig. 4.13 Thin-Film Resistor Reflection Coefficient Amplitudes (4.0 - 8.0 GHz)
----, (measured) ——, (optimized)

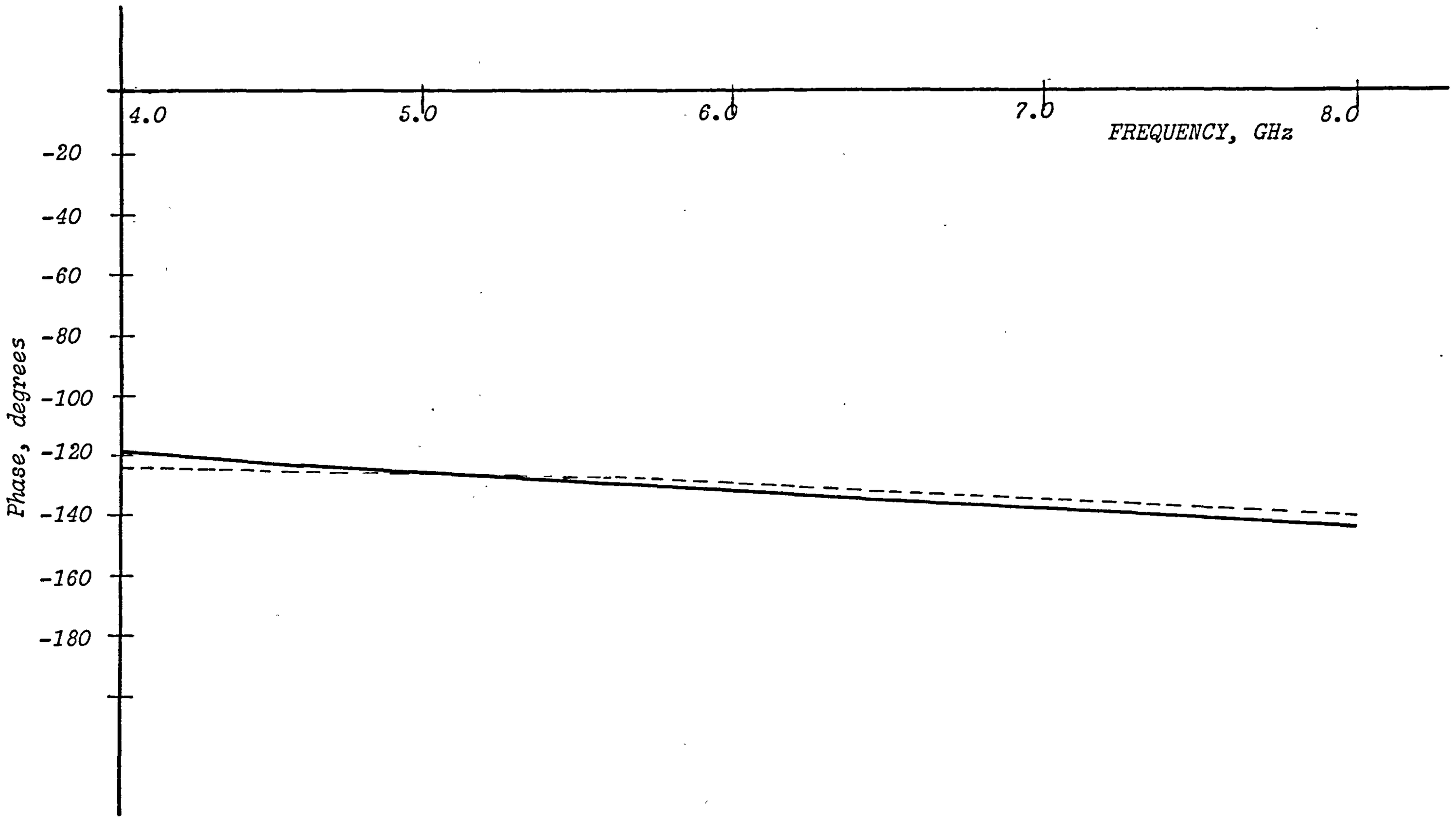


Fig. 4.14 Thin-film Resistor Reflection Coefficient Phases
---- (Measured)
—— (Optimized)

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CHAPTER 5

TRANSISTOR PACKAGE AND MOUNTING

5.1. Introduction

Microwave semi-conductor chip devices such as detectors, amplifiers, transistors and others are usually mounted in standard packages such as H.P. K-disc strip line headers. In some cases special headers have been designed to meet certain requirements.[5(1,2)]

The integrated-bipolar-transistors to be characterized here are in chip-form and they were provided by Allen Clark Research Centre, Plessey.[5(3)] These transistor-chips were produced using WR6A and WT16A masks. These masks have transistors with various emitter, base and collector geometries. The SB630, SB420 and SB820 transistors are the principal devices on these masks.

In this chapter, the preparation of these transistors for measurement will be described. A special transistor-package will be designed. This is to protect the transistor-chip and to facilitate measurements. As these transistor-chips vary in size, a microstrip package with a number of different layouts will be designed. Suitable terminal leads will also be designed. The transistor chips and the terminal leads will be mounted on an appropriate package. External connection between the emitter, base and collector terminals of the mounted transistor-chips and the corresponding package leads will be provided by wire-bonding techniques.

5.2. Transistor Package

The H.P. transistor fixture jig has been chosen as a measuring jig in the transistor measurements. These transistors were specified in Section 5.1. Consequently a microstrip-line transistor-package which fits the space available in the chosen jig has been designed by the author. In the design, the external

connection wires are kept to the minimum possible length to reduce the parasitic effects at microwave frequency[5(1,2)]. The effects can be eliminated by the possibility of extending the 50-Ω line measuring system up to the transistor terminals.[5(1,2)] This will be discussed in detail in the transistor measurement presented in Chapter 6.

Figs. 5.1 and 5.2 show the WR6A and WT16A masks produced at Caswell by Plessey Company. These masks include the required transistors to be measured. See Section 5.1.

Due to the mask size variation and to make the external connections possible, numbers of different strip-line transistor-package layouts have been designed. These packages, designed by the author, have been fabricated by ERA and they are deposited on a 1" × 1" × 0.025" superstrate using thick-film techniques. The superstrate is an ultra-fine-grained 99.5% aluminia substrate having an on fired surface finish of 3-4μ inches. These superstrates were obtained from Material Research Company.[5(4)]

5.3 Transistor-Package Leads:

Suitable terminal leads have been designed by the author to facilitate measurement on the packaged transistor-chips and to fit the space provided in the strip-line package designed in Section 5.2. These leads were made from 0.003" thick copper-strips and they have been sliced into suitable lengths and widths. The base and collector package-leads have been designed to be 1 mm in width and 6 mm in length. The emitter package-lead has been designed to be 2 mm in width and 5 mm in length. These dimensions were designed to fit the corresponding space provided by the H.P. measuring jig.

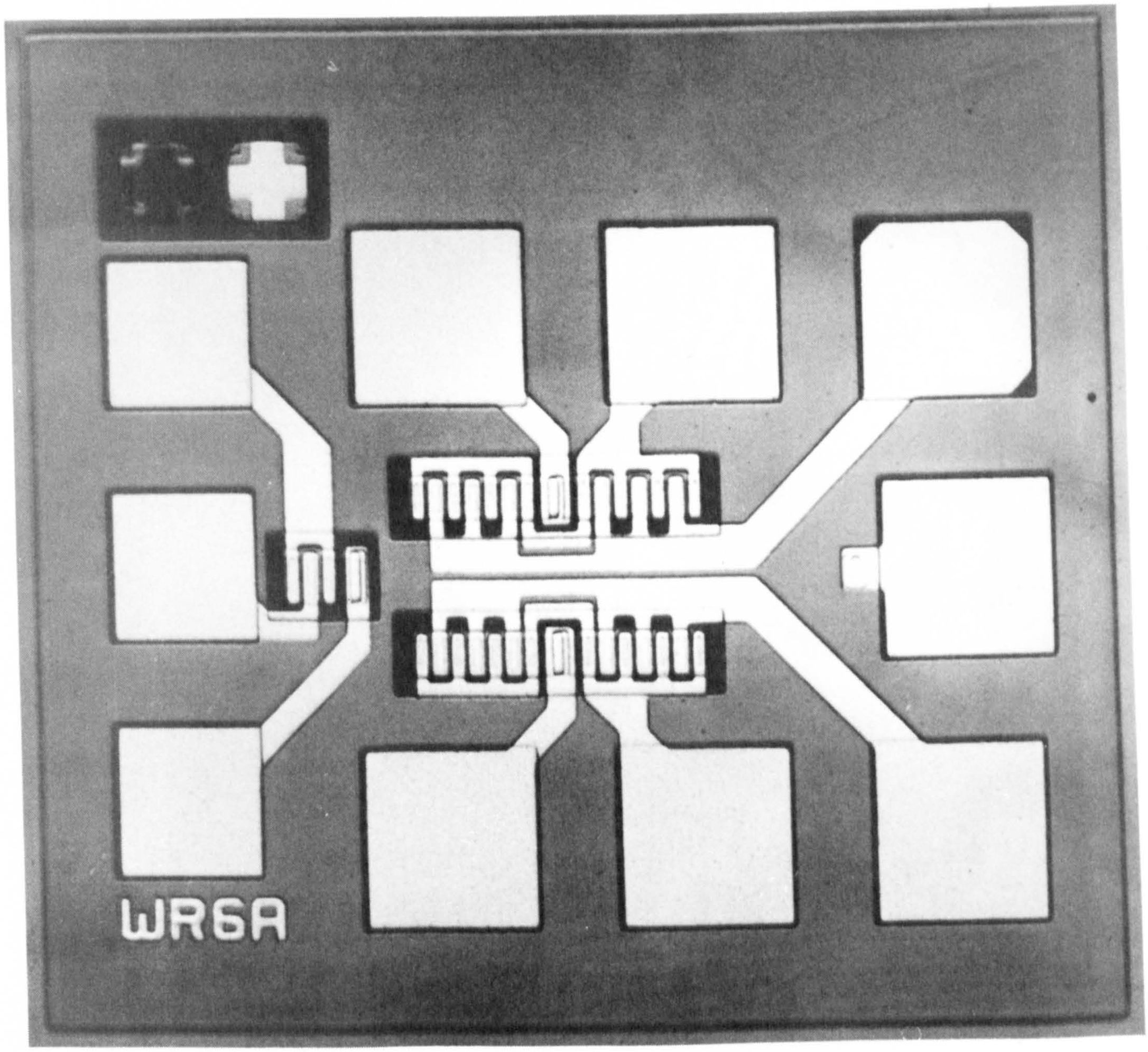

Fig. 5.1. A WR6A-Chip includes SB630 transistor
(Scale of 2000)

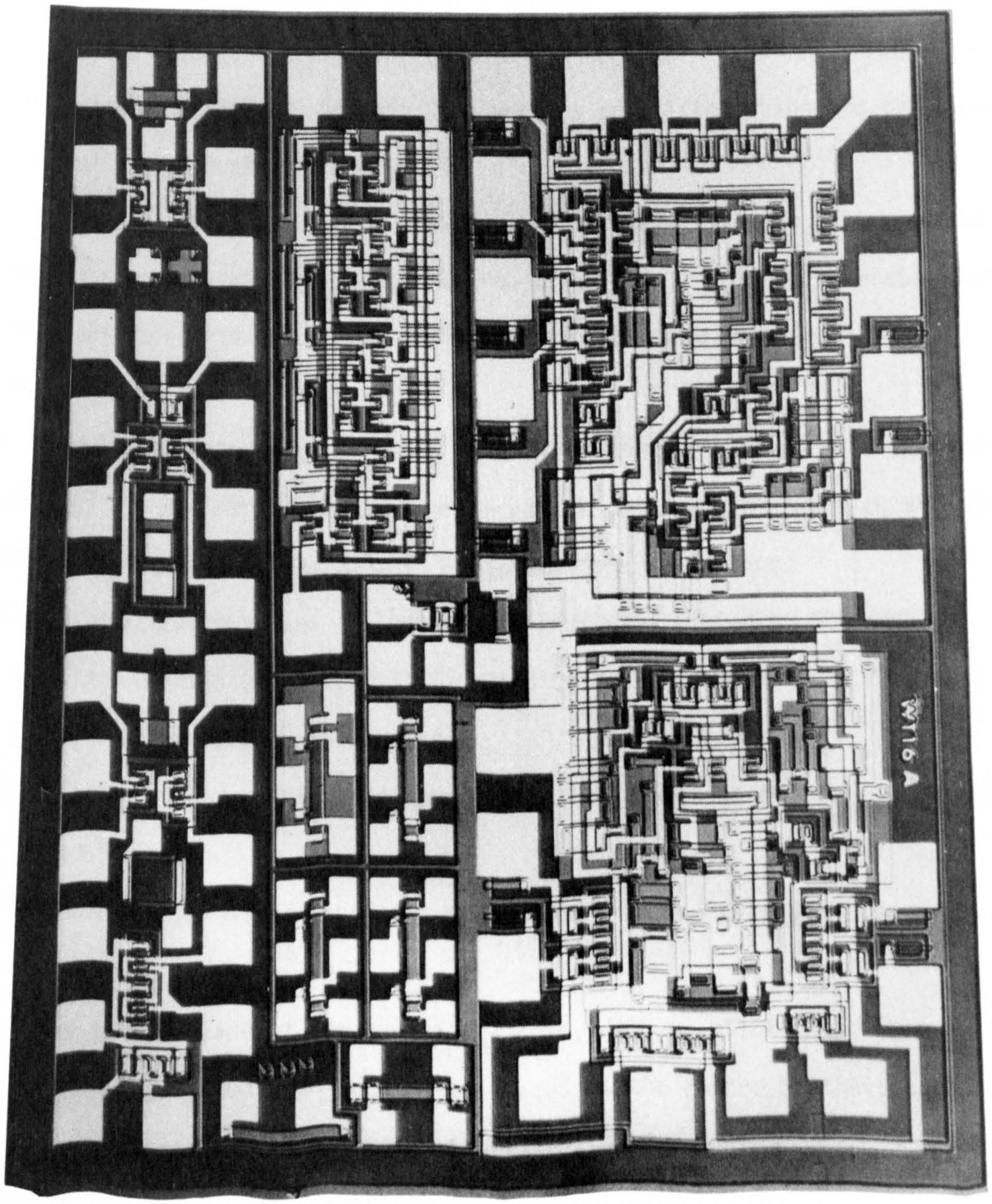

Fig. 5.2. A WT16A-Chip includes SB420 transistor (Scale of 800)

The strip line package terminal leads described above were gold plated for better electrical contacts.[5(5)]

5.4 Transistor-Chip Mounting and Wire Bonding:

The need for a transistor-package and terminal leads has been described in Section 5.1. In this Section, the various transistor-chips and the package-terminal leads mounting procedure is outlined.

It has been found, the package-terminal leads have to be mounted on the transistor-package prior to the transistor-chip. This is to enable mounting the transistor-chip exactly in the centre of the space provided in the transistor-package.

The package-terminal leads were first mounted on several transistor packages and the various transistor-chips have been mounted each on an appropriate transistor-package by the author. This was done as follows.

1. The emitter, base and collector lead ends were coated by EPO-TEK silver conductive epoxy H.31 type and then placed in the corresponding areas of the transistor-package.
2. The transistor-package was then placed in an oven at $80^{o}C$ for approximately 30 minutes.
3. Then, the transistor-package was removed from the oven and exposed to room temperature.
4. The ground plane of the transistor-chip, WR6A or WT16A chip, was coated by the epoxy and then accurately placed at the centre of the space provided in the mounted leads transistor-package.
5. Steps 2 and 3 were repeated.

The packaged transistor-chips are now ready for the next step, which is the external connection between the transistor-chip terminals and the corresponding package terminal leads. These connections have been provided by the use of wire bonding at Caswell, Plessey. Aluminium wire of 0.005" diameter has been used in these connections. A photo for a complete device is shown in Fig. 5.3.

5.5 Conclusion:

T he strip line transistor-package has been accurately designed to fit the H.P. test fixture jig and to hold the various transistor-chip sizes. The package terminal leads and the transistor-chips have been firmly mounted on the strip-line transistor-packages.

The wire bonding technique provided by Plessey wire-bonding group at Caswell was successful. The transistor-chips are now ready for measurements. These transistors will be measured in the following chapter.

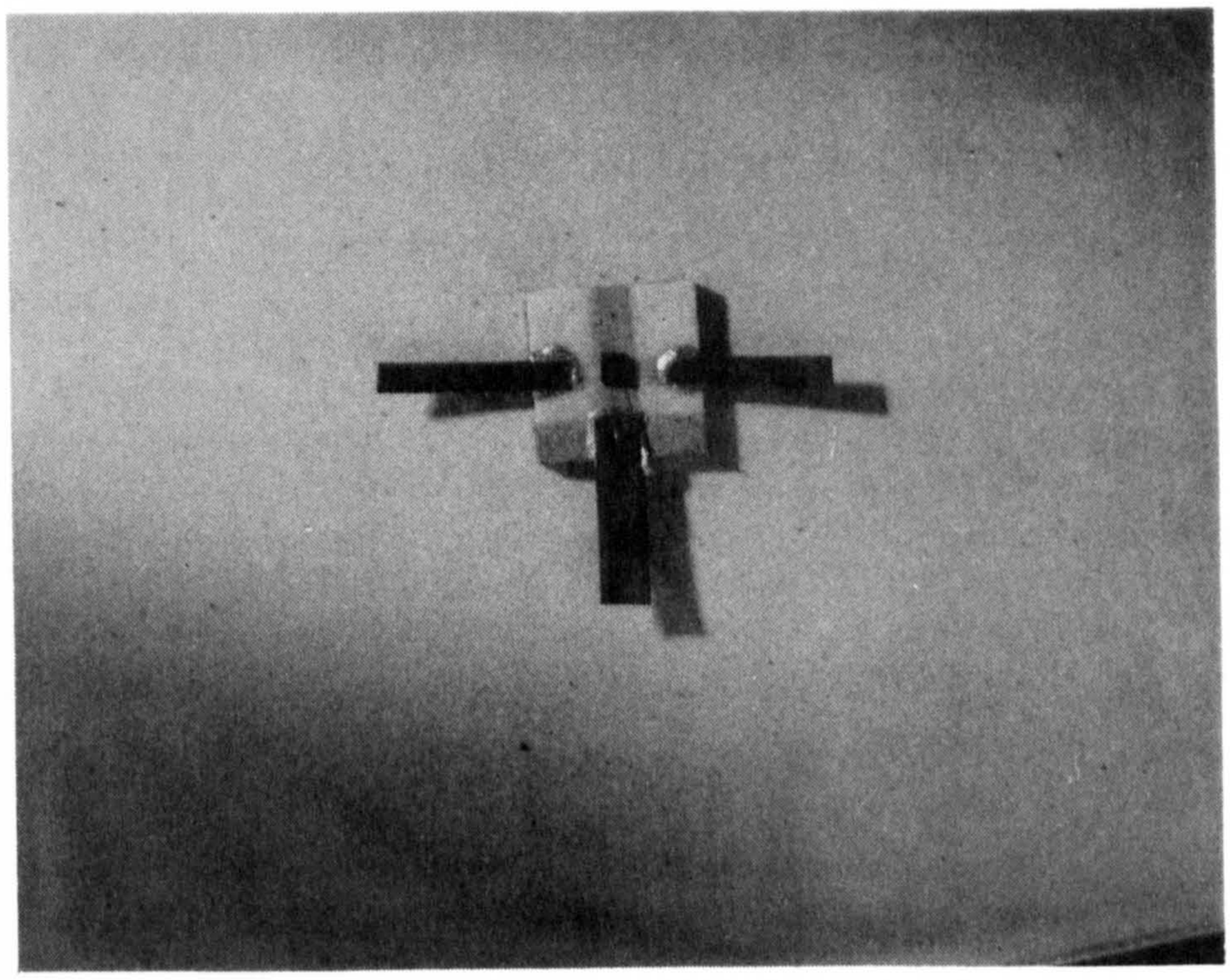

Fig. 5.3. A Complete Package Transistor-Chip
(Scale of 3)

5.6 REFERENCES

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CHAPTER 6

TRANSISTOR S-PARAMETER CALCULATION AND MEASUREMENT

6.1. Introduction

In the preceeding Chapter, the strip-line transistor-package has been described and the transistors to be measured, which are in chip-form, have been mounted on the corresponding strip-line package and wire-bonded. In this Chapter, the measurement of the S-parameters of the specified transistors at several bias conditions applying the implemented computer aided correction program of Chapter 3, will be carried out.

Also, in this Chapter, the analysis of the transistor equivalent circuit in terms of S-parameters will be carried out. These equations will be needed in the formulation of the objective function, described in Chapters 7 and 8.

The Plessey integrated bipolar transistor SB420, which is similar to the SB630 type of transistor but with different emitter width and length, was also measured at the same bias conditions as the SB630. This is to study the S-parameters of both transistors and to show the equivalent circuit element variation from one transistor to another.

Due to the limited ranges of the sweep oscillator of the H.P. network analyser measuring system, the S-parameters of the two transistors were measured first over the frequency range 0.4 - 2.0 GHz and then in the 2.0 - 4.0 GHz frequency-band applying computer aided measurements.

6.2. S-Parameter's Analysis Equations

In this Section, the S-parameters of the SB630 transistor are calculated from its equivalent circuit shown in Fig.2.7.b. This equivalent circuit model and its various parameters and components have been fully discussed in Chapter 2.

It has been found, due to the transistor equivalent circuit complexity, it is easier to calculate first the circuit Y-parameters and then use Y-S transformation equations to obtain the transistor S-parameters.[6(1)]

The transistor circuit model of Fig.2.7b is arranged in Fig. 6.1, for Y-parameter calculations. Using circuit theory and Nodal analysis[6(2,6)], the circuit Y-parameters are then: (See Appendix E)

$$y_{11} = \left.\frac{I_1}{e_1}\right|_{e_o=0} = \frac{1}{A_1}\{x_1A_1 - G_bA_2 - j\omega C_{bc'}A_3\} \qquad 6.1.$$

$$y_{21} = \left.\frac{I_o}{e_1}\right|_{e_o=0} = -\frac{G_c}{A_1}A_3 \qquad 6.2.$$

$$y_{22} = \left.\frac{I_o}{e_o}\right|_{e_1=0} = \frac{1}{A_1}\{x_5A_1 - G_c^2 x_2\} \qquad 6.3.$$

and

$$y_{12} = \left.\frac{I_1}{e_o}\right|_{e_1=0} = -\frac{G_c}{A_1}A_5 \qquad 6.4.$$

in which,

$$A_1 = x_2x_4 + j\omega C_{b'c'}x_3 \qquad 6.5.$$

$$A_2 = G_bx_4 - \omega^2 C_{bc'}C_{b'c'} \qquad 6.6.$$

$$A_3 = G_bx_3 - j\omega C_{bc'}x_2 \qquad 6.7.$$

$$A_5 = j\omega(C_{bc'}x_2 + C_{b'c'}G_b) \qquad 6.8.$$

and,

$$x_1 = G_b + j\omega C_{bc'} \qquad 6.9.$$

$$x_2 = G_b + G_e + j\omega(C_{b'e} + C_{b'c'}) \qquad 6.10.$$

$$x_3 = g_m - j\omega C_{b'c'} \qquad 6.11.$$

$$x_4 = G_c + j\omega(C_{bc'} + C_{b'c'}) \qquad 6.12.$$

$$x_5 = G_c + G_s \qquad 6.13.$$

where,

$$G_s = \frac{j\omega C_o}{1+j\omega C_o R_s} \qquad 6.14.$$

$G_b = 1/R_{bb'}$, $G_e = 1/R_e$ and $G_c = 1/R_c$

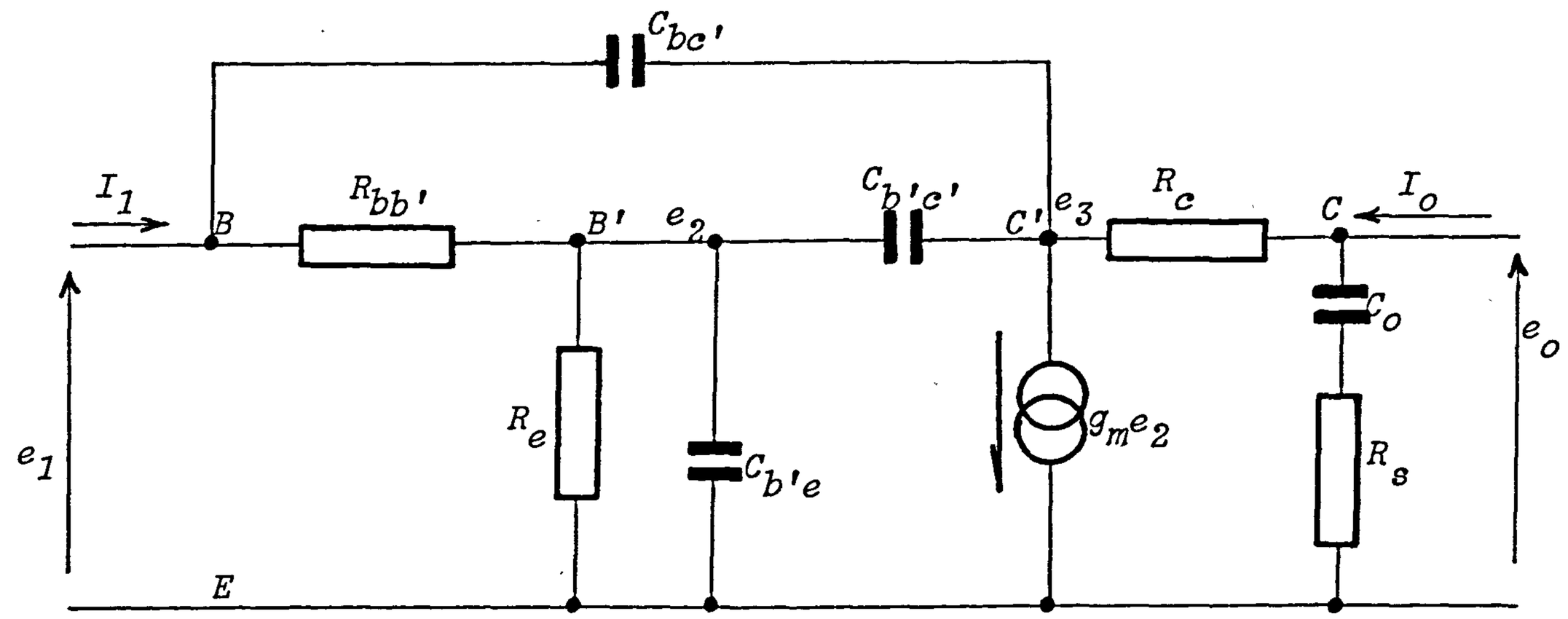


Fig. 6.1. Transistor Small Signal Equivalent Circuit for y-parameter Calculations

Now, the S-parameters could be formulated in terms of the Y-parameters, which are given by Equations 6.1 - 6.4, giving:[6(1)]

$$S_{11} = \frac{1}{A_4} \{(1-50y_{11})(1+50y_{22})+2500y_{21}y_{12}\} \quad 6.15.$$

$$S_{21} = -100y_{21}/A_4 \quad 6.16$$

$$S_{12} = -100y_{12}/A_4 \quad 6.17$$

and

$$S_{22} = \frac{1}{A_4} \{(1+50y_{11})(1-50y_{22})+2500y_{21}y_{12}\} \quad 6.18$$

in which,

$$A_4 = (1+50y_{11})(1+50y_{22})-2500y_{21}y_{12} \quad 6.19$$

The flow diagram for the equivalent circuit analysis which will produce a table of results for the S-parameters of the equivalent circuit at selected frequency points is shown in Fig. 6.2. With the numerical values of Table 2.1 (Section 2.4) for the grounded emitter configuration of the integrated bipolar transistor of Chapter 2, the S-parameters of Fig. 6.3 are obtained.

6.3. Calibration Pieces Descriptions

It has been stated in Chapter 3, that two things are necessary to successfully measure the S-parameters of a device. Firstly, a reference plane of measurement has to be established at its terminals, i.e. the 50-Ω line measuring system has to be extended up to the device terminals. Secondly, the measuring system has to be calibrated at the established reference plane, the device terminals.

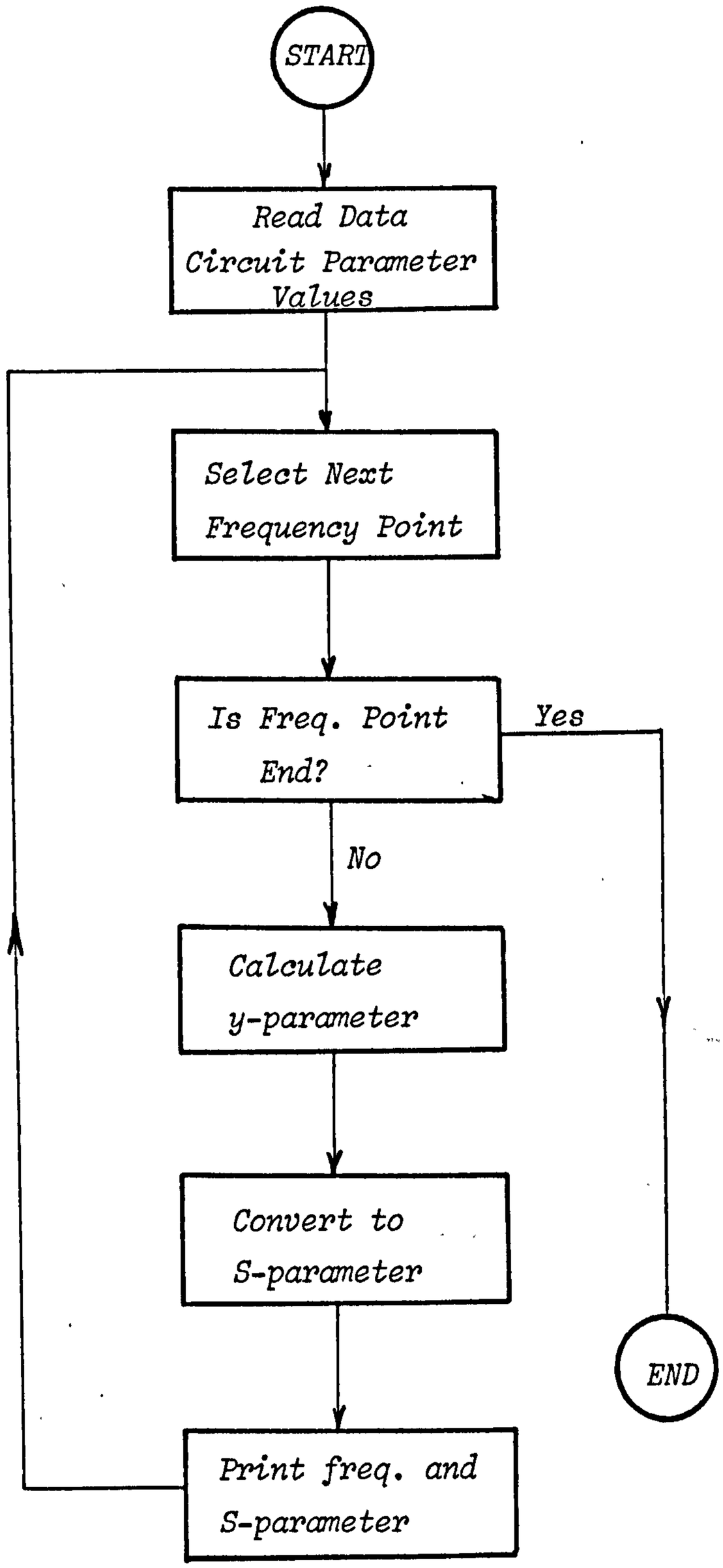


Fig. 6.2. Flow Diagram for S-parameter Calculation of Fig. 6.1.

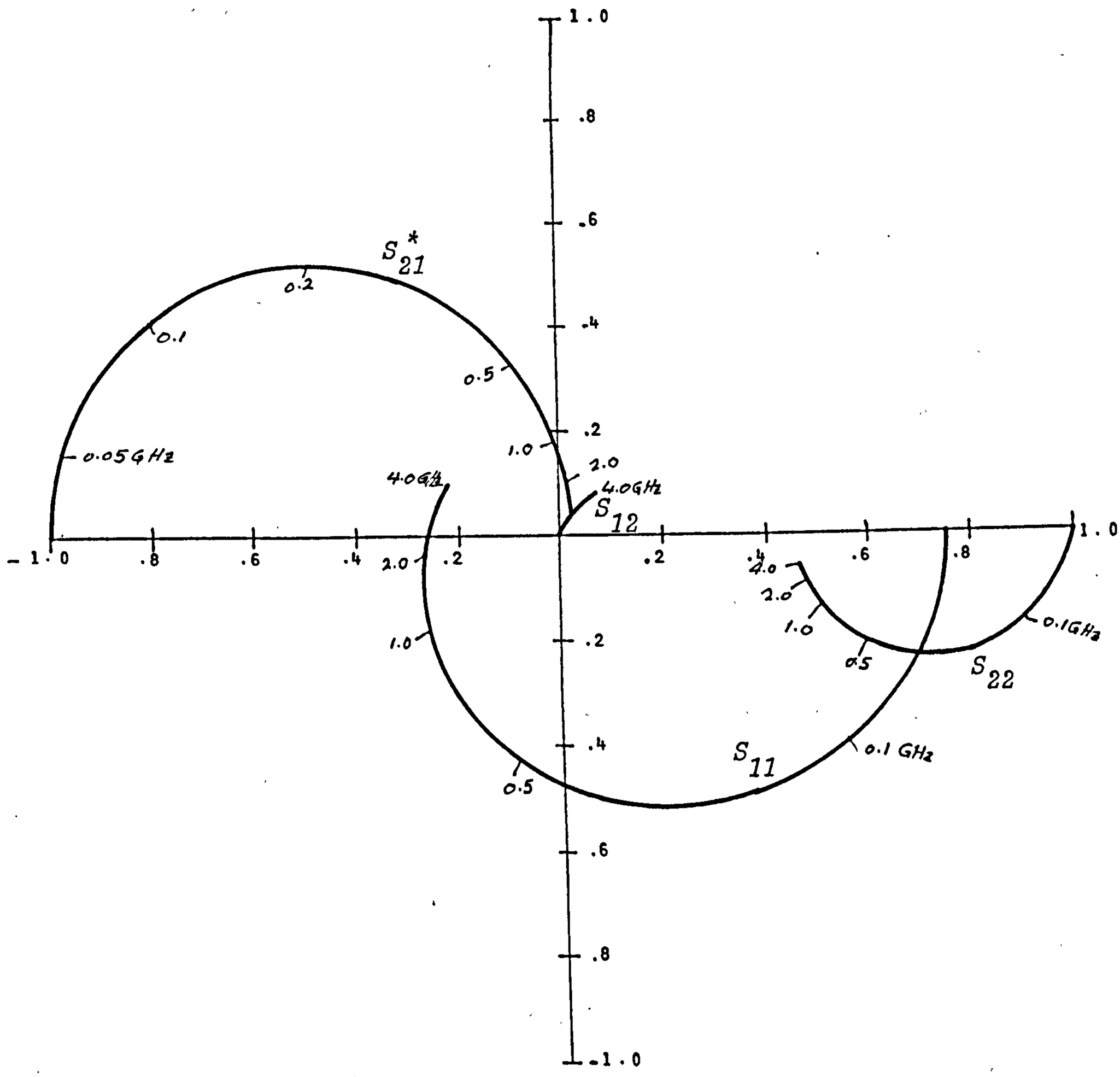


Fig. 6.3. The S-parameter Polar Plots (calculated from SB630 Transistor equivalent circuit of Fig.6.2)

* *Scale of 1:12.1*

In order to calibrate a measuring system and hence measure the S-parameters of a device using the computer aided correction program of Chapter 3, calibrating standards are required. These calibrating standards are matched loads, short-circuits, open-circuits and a through line.

Previous investigators in computer-aided-correction measurement[6(3,5)] have succeeded in extending the reference plane up to the device package, but they have failed to extend the reference plane of the measuring system to the device terminals. This is because the selected calibration pieces, required for system calibration and establishing a reference plane of measurement, do not fit the space available in the device measuring jig.

In the transistor measurements, Section 6.6, the author extends the 50-Ω reference of the measuring system up to the device terminals. This is to obtain accurate values for S-parameters of the transistor. The errors arising from the transistor-package and bonding wires were considered to be included in the error networks placed at each side of the transistor as shown in Fig. 3.1.

The calibration pieces required to extend the 50-Ω line measuring system up to the transistor terminals will be discussed in Sections 6.3.1 and 6.3.2. These calibration standards were mounted on a package designed to fit the space available in the transistor-jig.

6.3.1. Matched Load Termination

It has been stated in Chapter 3, that due to the matched-load difficulties at microwave frequencies, a known load impedance frequency dependence can be used instead to terminate the measuring system during calibration. Hence, A Tek-Wave chip-resistor similar to that characterized in Chapter 3 was mounted on an identical transistor-package, described in Chapter 5. The equivalent circuit model obtained in Chapter 4 and shown in Fig. 4.2. was used to represent this thin-film resistor over the frequency range of interest. Its parameter values will remain constant, except for the value for R_o. R_o is the d.c. resistance of the thin-film resistor and it varies from one chip-resistor to another. Hence, it can be easily measured at D.C.

Two chip-resistors were mounted on strip-line packages, identical to those used for the transistors. This is to terminate in turn ports (1) and (2) of the H.P. network analyser as required by the system calibration procedure of Chapter 3. Fig. 6.4. is a photograph of the packaged-matched loads which are used to terminate in turn ports (1) and (2) of the measuring system, H.P. Network Analyser.

6.3.2. Short-Circuit, Open-Circuit and Through Line Terminations

The open-circuit and through line terminations, required for system calibration as stated in Chapter 3, were produced on Aluminium Metalized-Chips (2WT4A). This type of chip includes transistors identical to those specified in Chapter 5 in size and shape. In this chip, the aluminium conductor pattern is etched in the usual way. The only difference to an ordinary transistor is that the contact windows, i.e. emitter, base and collector, are not etched out, thus leaving no connections to the transistor.

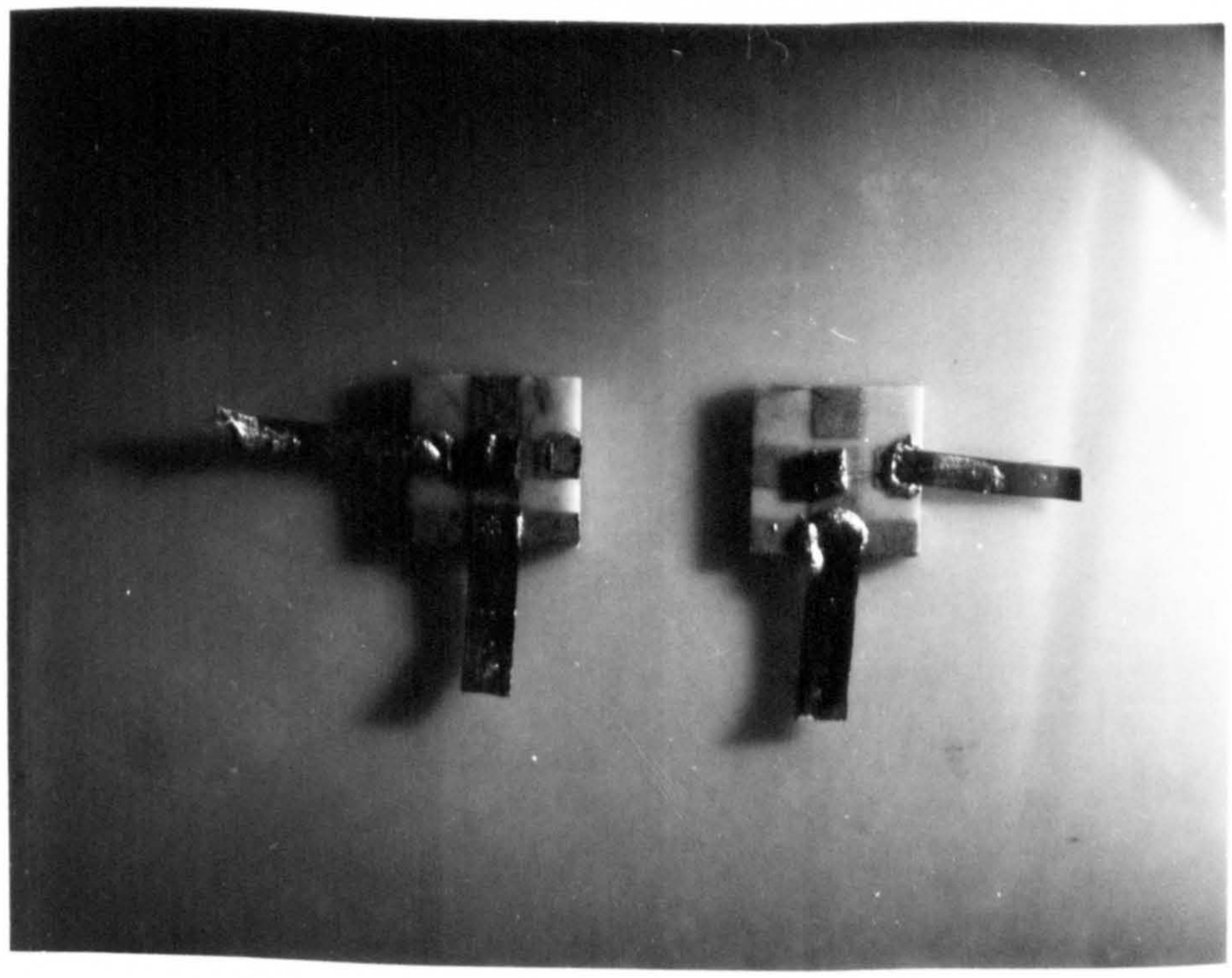


Fig. 6.4. The Packaged Matched Loads (A TEK-WAVE Chip)
Left, for port (1)
Right, for port (2)
(Scale of 3)

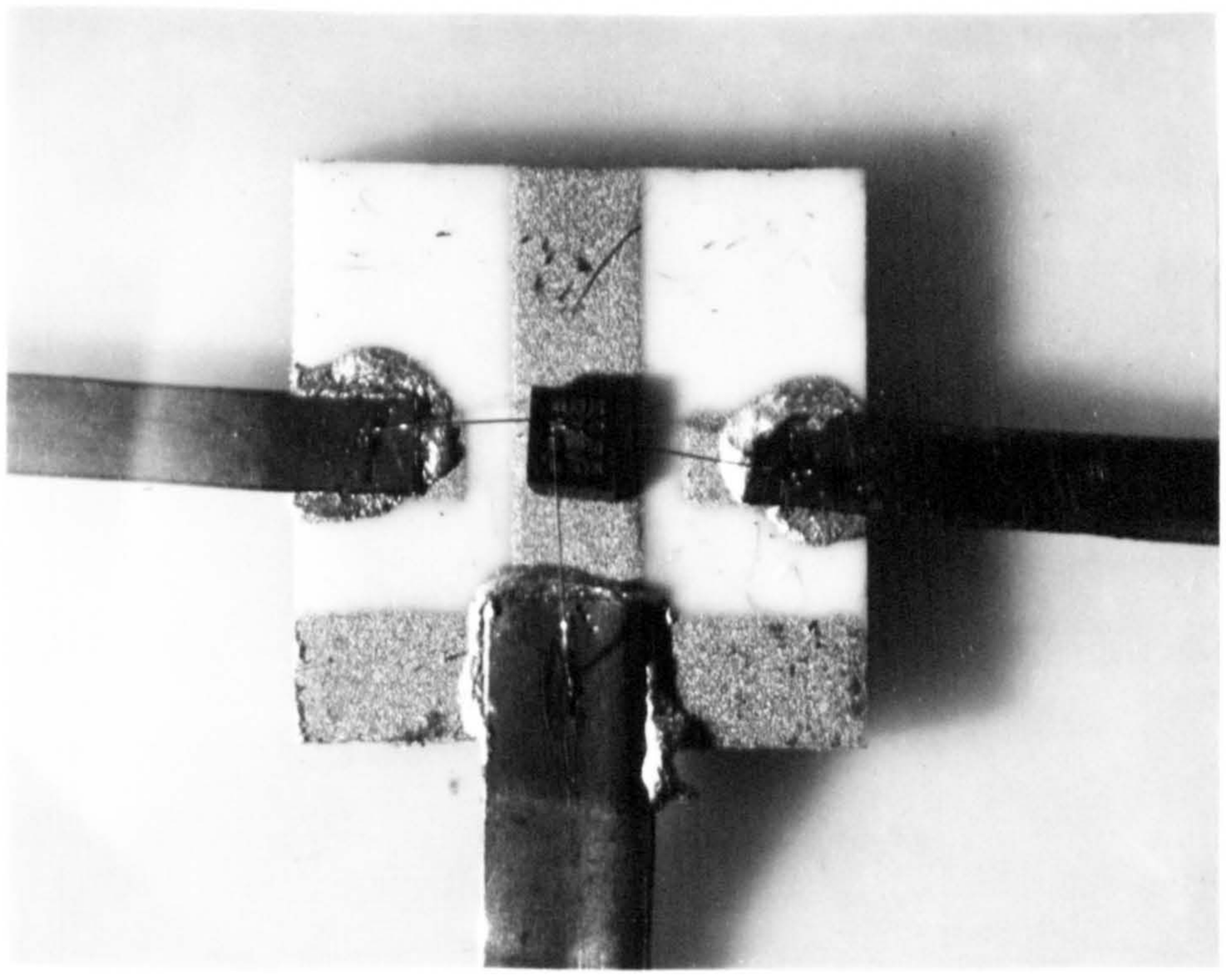


Fig. 6.5. The Packaged Short-Circuit
(WR6A-Chip)
(Scale of 10)

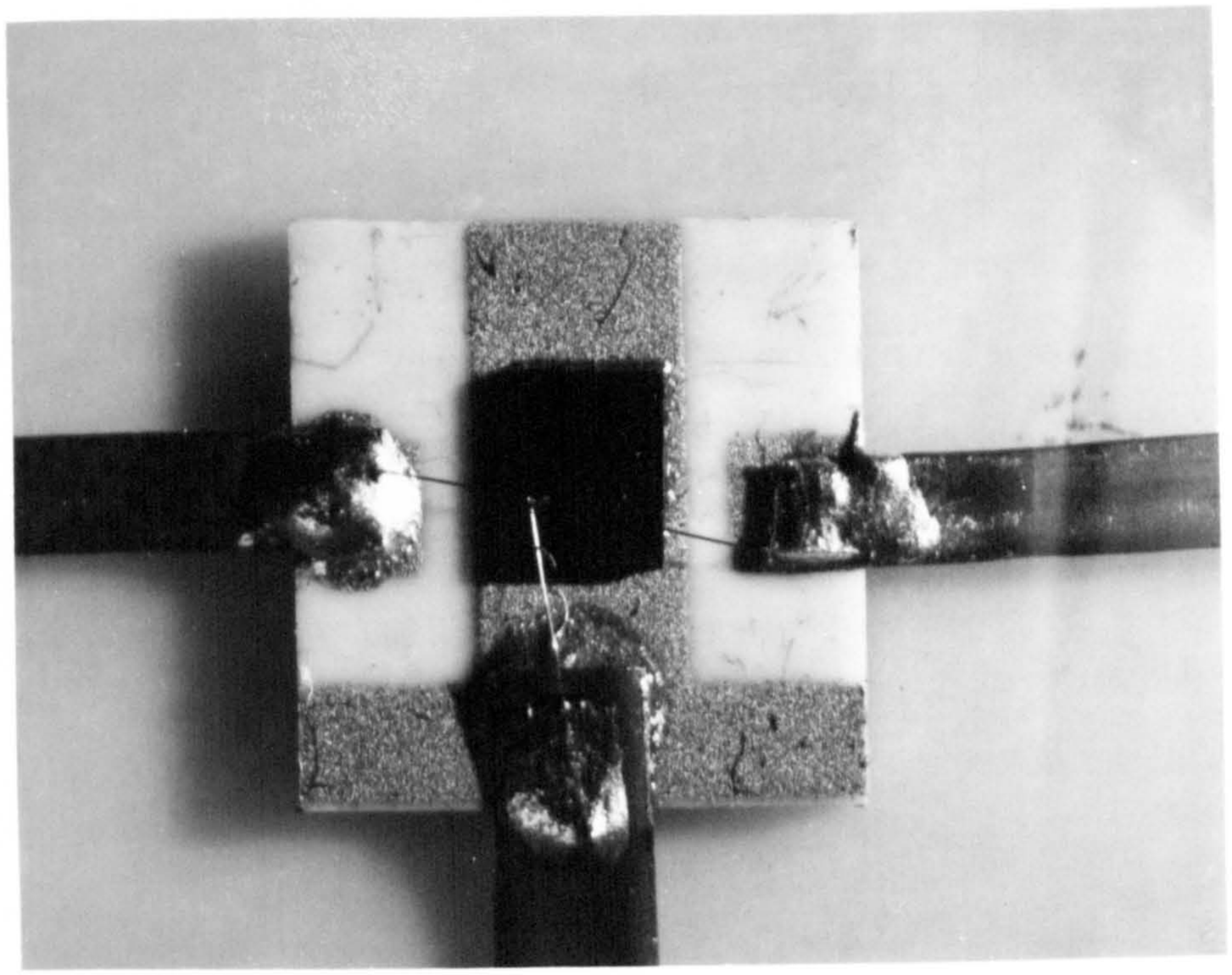
Fig. 6.6 are photographs of the packaged open-circuit and through-line. In these photographs the connection necessary to produce an open-circuit and a through-line are also shown.

It has been found impossible to maintain the connection necessary to produce a short circuit on the 2WT4A chip. This is because, a pad contact area on this chip is not sufficient to accommodate the three wire ends required to produce the short-circuit. Due to this difficulty, the short circuit termination was produced on a WR6A chip. The WR6A-chip includes besides the SB630 transistor, and other integrated circuits which have larger pad contact areas than that of 2WT4A chip. One of these pad contacts, which is sufficient to accommodate the connection required for short-circuit, has been chosen in order to produce the short-circuit.

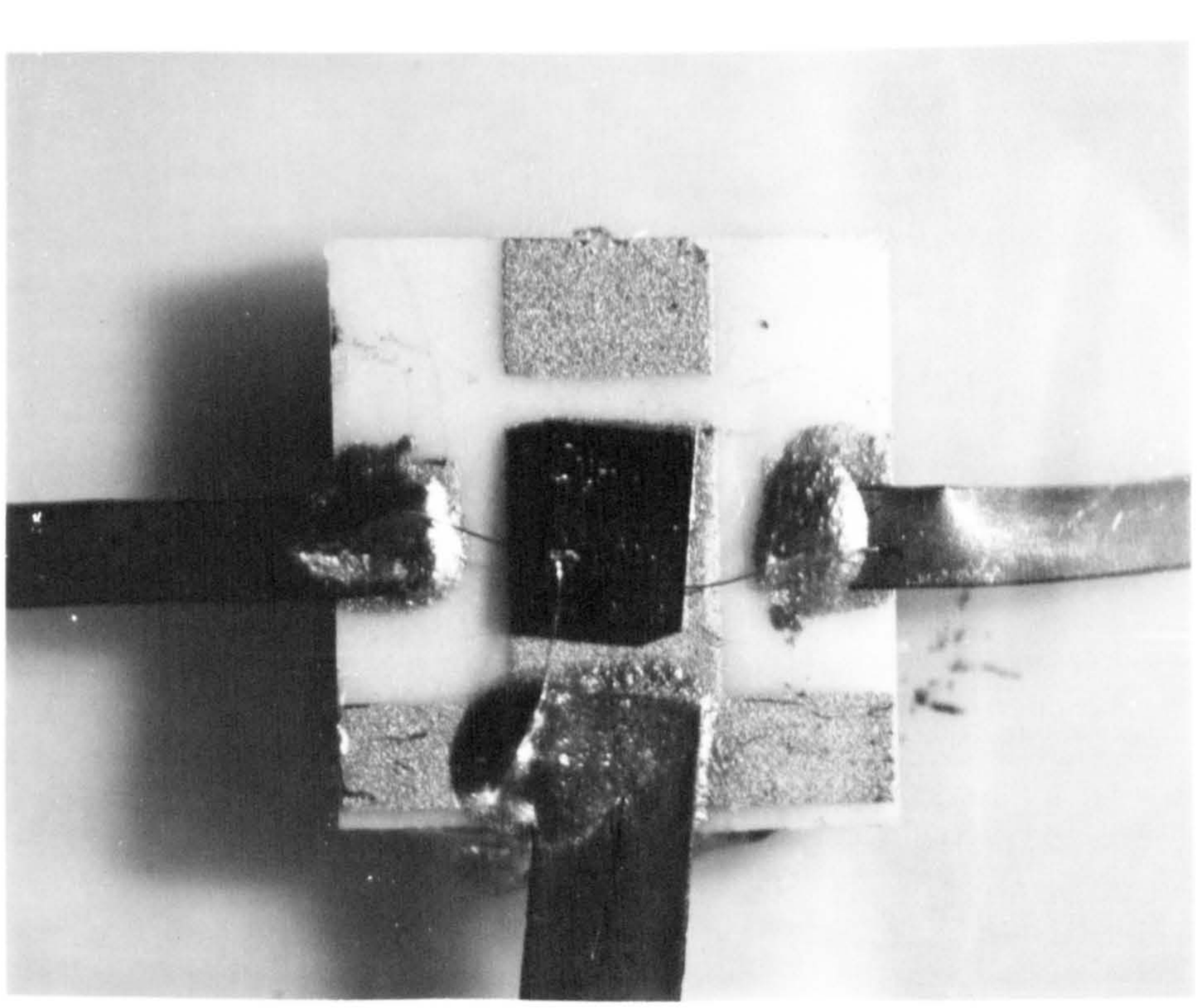
The packaged WR6A-chip, together with the short-circuit connection is shown in Fig. 6.5.

The various chips were obtained from Plessey, Caswell. The wire-bonding involved in producing the various calibration pieces has been done by the Wire-Bonding Group at Caswell.

To study the frequency dependence of the calibration pieces and hence to evaluate the lead-inductance L and the pad-capacitance C_p, short-circuit and open-circuit terminations were measured and their frequency responses were displayed on the polar display of a Network analyser. As expected, it was found that the calibration pieces are lossy at frequencies higher than 1.0 GHz. This is due to shunt loss of the semi-conductor substrate and the 50-Ω line impedance of the measuring system, during the measurements of the calibration pieces.



(a)



(b)

Fig. 6.6. The Packaged 2WT4A-chips (metalized-chip)

(a) Open-Circuited
(b) Through-Line
(Scale of 10)

Both amplitude and phase of the short-circuit and open-circuit could be then measured at any frequency point. Equating the measured amplitude and phase to that calculated from the corresponding equivalent circuits of Fig. 6.7, values for L and C_p could be found. Such procedure gives 1.64 nH and 1.0 pF for L and C_p at 1.0 GHz and 3.0 GHz respectively. Note that the equivalent circuits of Fig. 6.7, were terminated by the 50-Ω impedance of the measuring system, (Network Analyser).

6.4. h_{fe} and output Capacitance Measurements

h_{fe} is possibly the most important small signal equivalent circuit parameter of the transistor. h_{fe} determines the maximum obtainable current gain from such a transistor. This common emitter current transfer ratio, h_{fe}, is normally called the small signal beta of the transistor.

By definition h_{fe} is,[6(2)]

$$h_{fe} = \left.\frac{\Delta i_b}{\Delta i_c}\right|_{V_{CE} = \text{constant}} \qquad 6.20$$

h_{fe} was estimated from the output characteristics of a transistor displayed on a curve tracer at a specific bias condition of V_{CE} and I_c.

The h_{fe} measurements on the selected transistors were performed at Caswell by the author. This was to obtain values for the low frequency forward current gain h_{fe} of the individual transistor.

Fig. 6.8 represents the measured h_{fe} of SB630 and SB420 transistors respectively. The forward current gain h_{fe} was measured at selected bias conditions as these values will be used in the transistors' S-parameter measurements in the following Section.

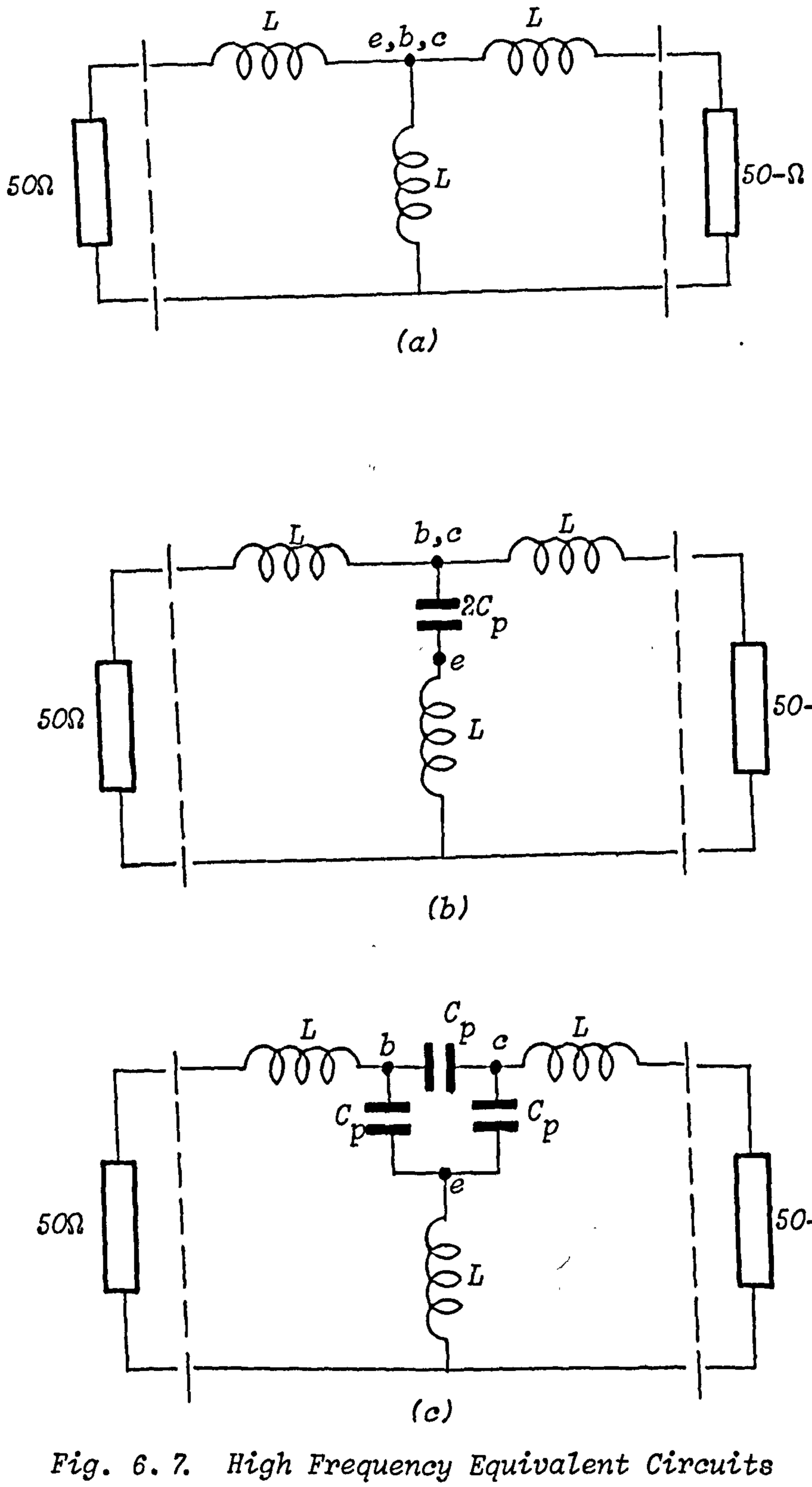


Fig. 6. 7. High Frequency Equivalent Circuits

(a) for short-circuit
(b) for through-line
(c) for open-circuit

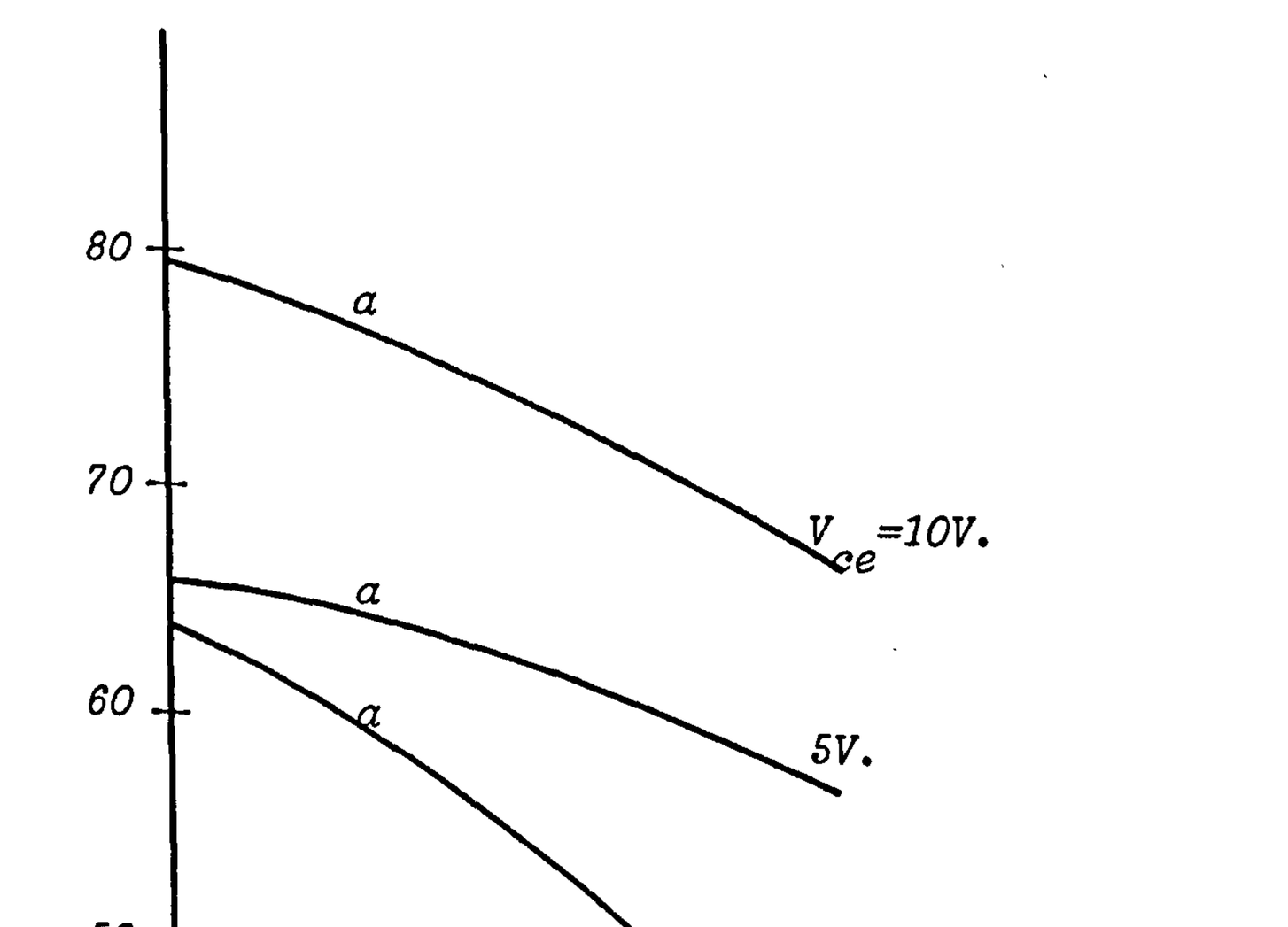


Fig. 6.8. h_{fe} *v* I_c (V_{ce}=2,5 *and 10V)*
a, for SB420 Transistor,
b, for SB630 Transistor.

The output capacitance C_{ob} of the above transistors was measured at Caswell and is shown in Fig. 6.9[6(4)]. Here, the output capacitance is assumed to be equal for all transistors and it is dependent on the collector-base voltage V_{CB}. C_{ob} is also dependent on the area of the transistor. C_{ob} measurements on various transistors made using the Plessey Process III, showed that the C_{ob} value varied by less than 10% from one type of transistor to another[6(4)]. The only question is how C_{ob} could be divided between the junctions BC' and B'C' in the individual transistor equivalent circuit.

6.5. S-parameter Measurement

In Section 6.3 the calibration pieces required for system calibration and to establish the reference plane of measurement, have been described. The SB630 and SB420 transistors have been successfully mounted on the strip-line package, described in Chapter 5, and ready for measurements.

Here, the author will describe the S-parameter measurements on these transistors, carried out at several bias conditions.

In the transistor measurements, the H.P. Automatic Network Analyser measuring system was terminated in turn by the calibration pieces of Section 6.3. The calibration procedure sequence of Section 3.3 was followed. The computer aided correction technique implemented in Chapter 3, was applied to the S-parameter measurements in order to obtain correct values for S-parameter of the transistors. The errors associated with the measuring system and the leakage powers transmitted through the system in both directions have been accounted for.

The specified transistors were measured first over the 0.4 - 2.0 GHz frequency range at 17 frequency points, and secondly over the frequency-band of 2.0 - 4.0 GHz and 21 frequency points at the following bias conditions.

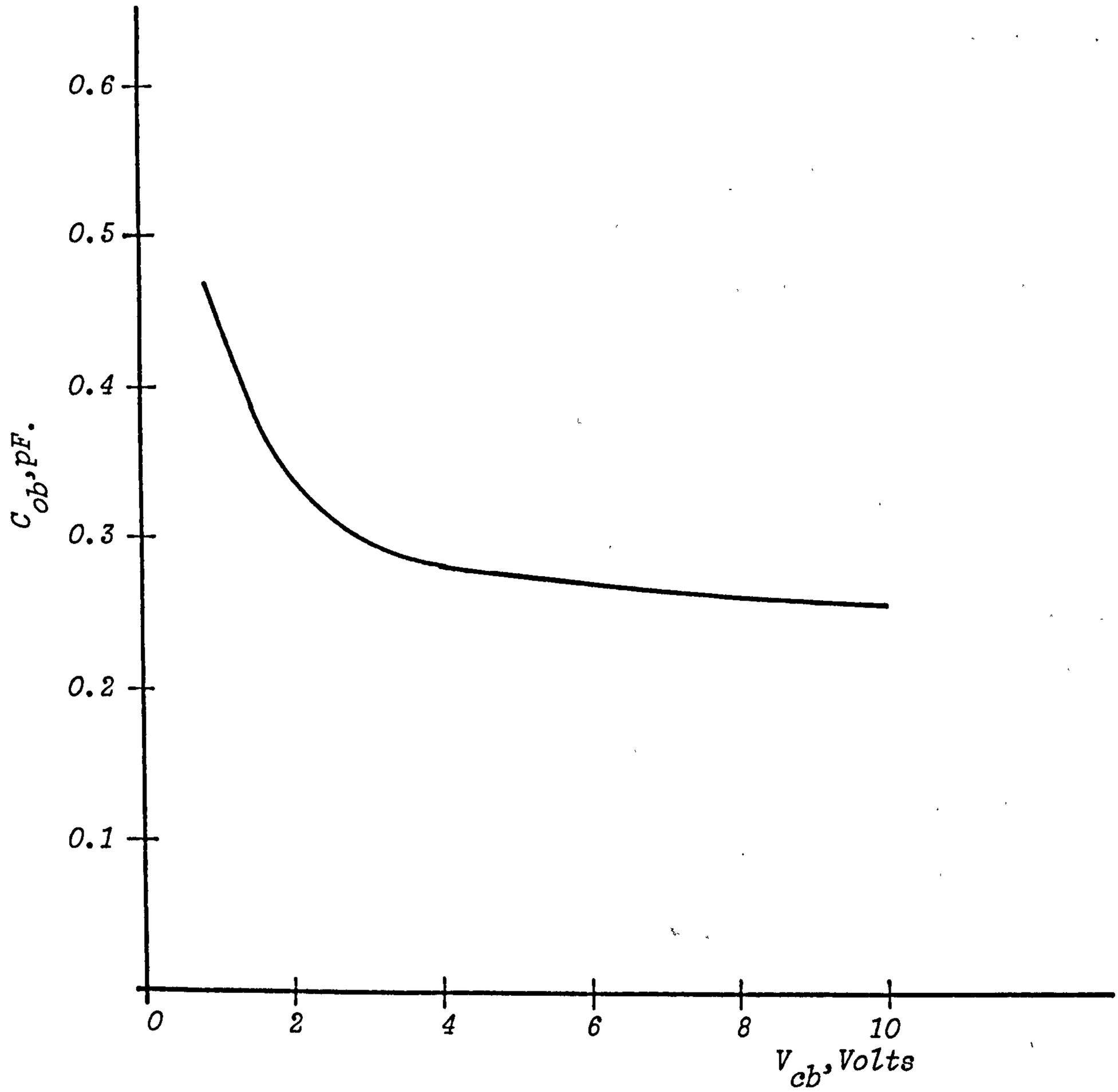


Fig. 6..9. The output capacitance, C_{ob} of Plessey Process III Transistors at I =5mA

e

a) V_{CE} = 2V., I_C = 5, 10 and 15 mA,

b) V_{CE} = 5V., I_C = 5, 10 and 15 mA,

c) V_{CE} =10V., I_C = 5, 10 and 15 mA.

Fig. 6.10 represents the measured S-parameter amplitudes, corrected and uncorrected, for the SB630 transistor at V_{CE} = 2V., and I_C = 10 mA over the frequency-band 2.0 - 4.0 GHz. The curves have been drawn through all the measured frequency points, which have been omitted for clarity. The scatter on the results is less than the line thickness. This is to show the measured results were effectively corrected to give very smooth curves.

The measured S-parameters of the transistors are plotted on polar plots at frequencies from 0.4 GHz - 4.0 GHz in Figs. 6.11 to 6.14, in order to show both amplitude and phase of the measured parameters' variations with operating frequency. Again, the scatter in the measured points lies within the width of the lines shown. It is not practical in this thesis to show the whole of the measured S-parameters of the transistors at all the bias conditions specified above. The author instead, presents representative samples of some of these measurements at two different bias conditions. This is to give an idea of how the transistor S-parameters vary from one bias condition to another, and to show the very smooth appearance of the curves.

In order to ensure repeatability, the S-parameter measurements on the SB630 and SB420 transistors were carried out three times at the V_{CE} = 5V., and I_C = 10 mA bias condition. It was found that, the measured S-parameters of each transistor varied by less than $\pm$ 0.85% in both amplitude and phase. A complete recalibration of the measuring system was made for each of these measurements, in order to ensure the repeatability of making the contacts to the calibration pieces and the transistors.

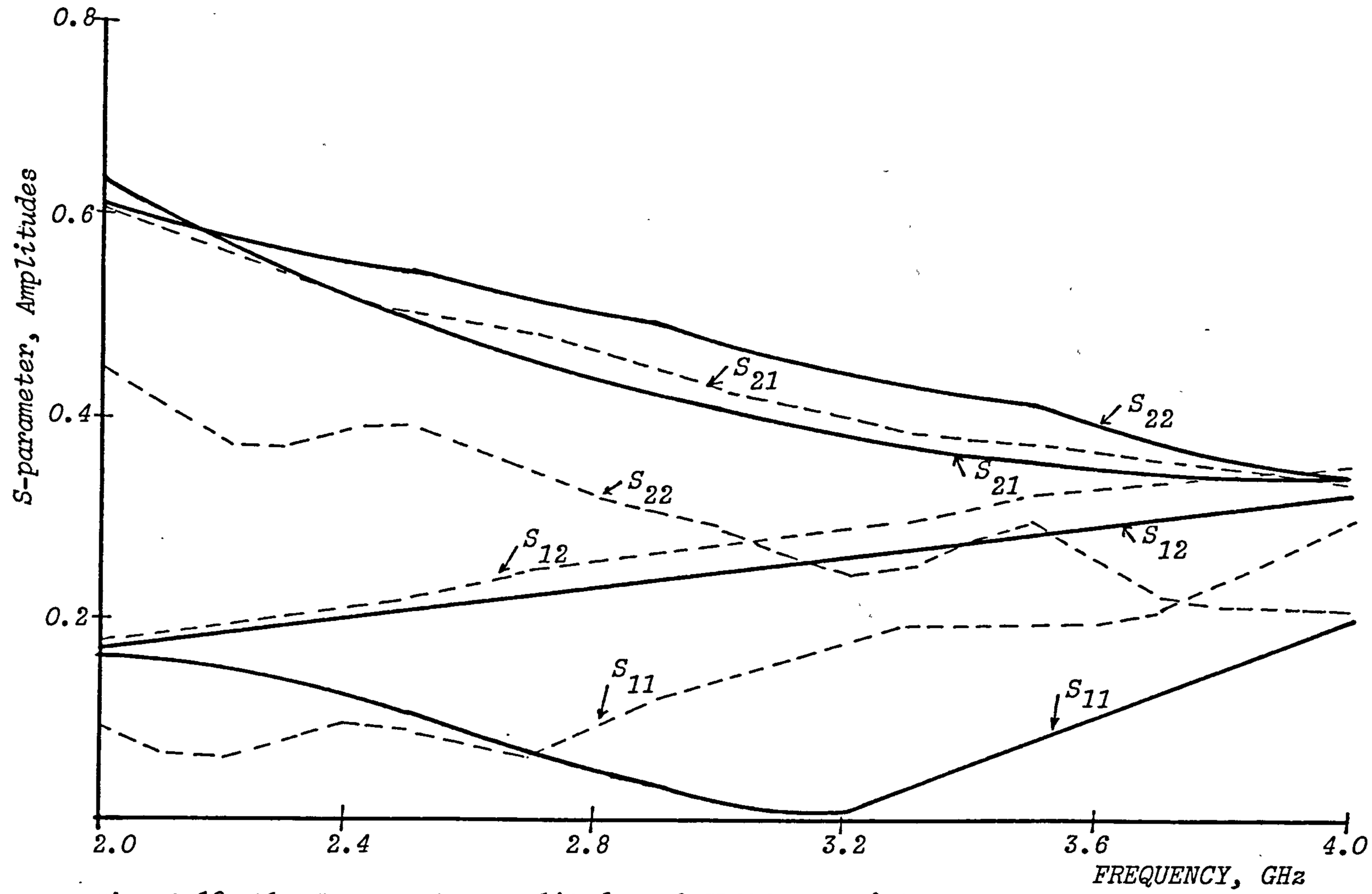


Fig. 6.10. The S-parameter Amplitudes of SB630 Transistor (V_{ce}=2V., I_c=10mA)
----, Uncorrected
——, Corrected

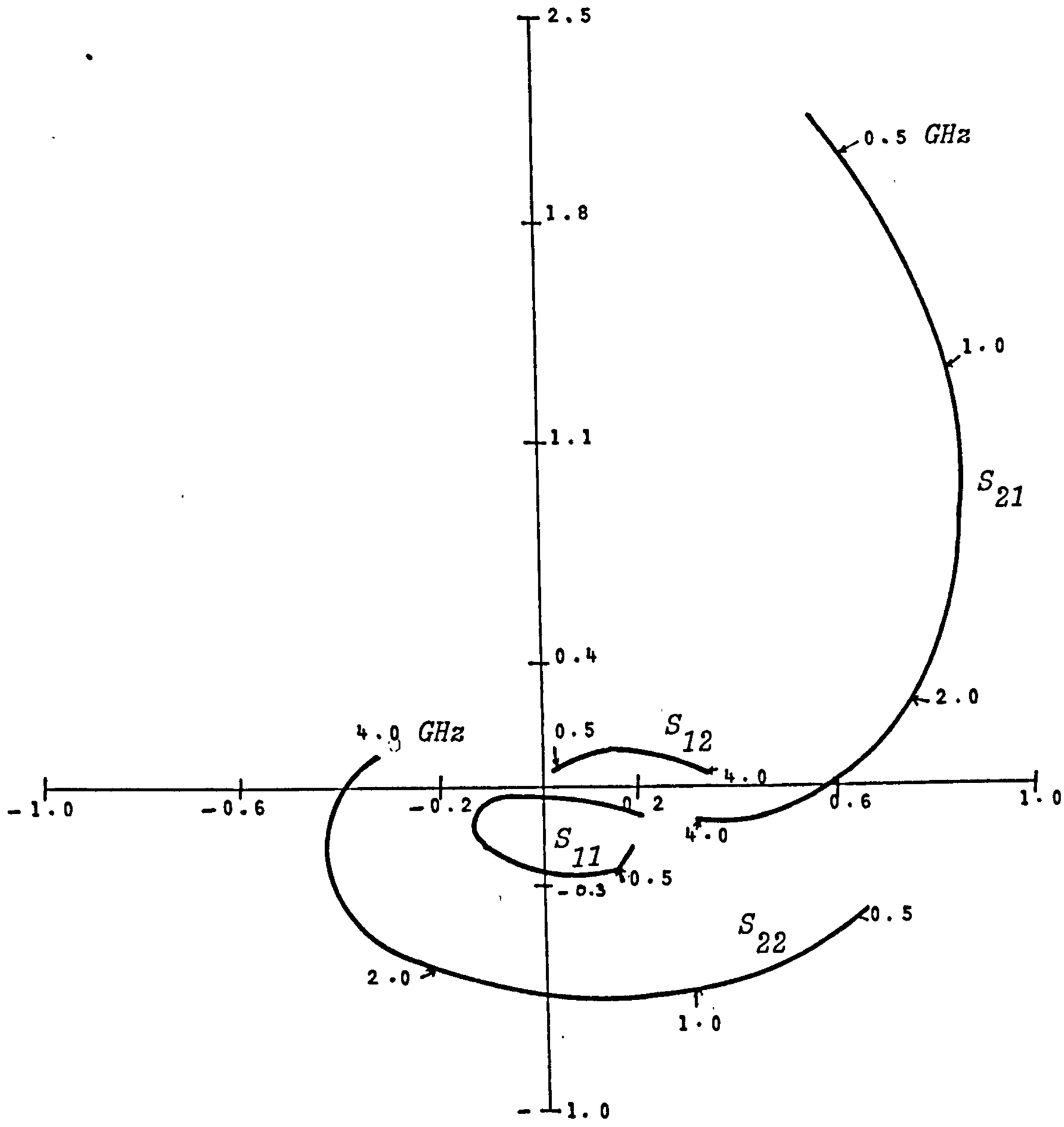


Fig. 6.11. The S-parameter polar plots of the SB630 Transistor over 0.4 - 4.0 GHz frequency range (V_{ce}=2V., I_c=10mA)

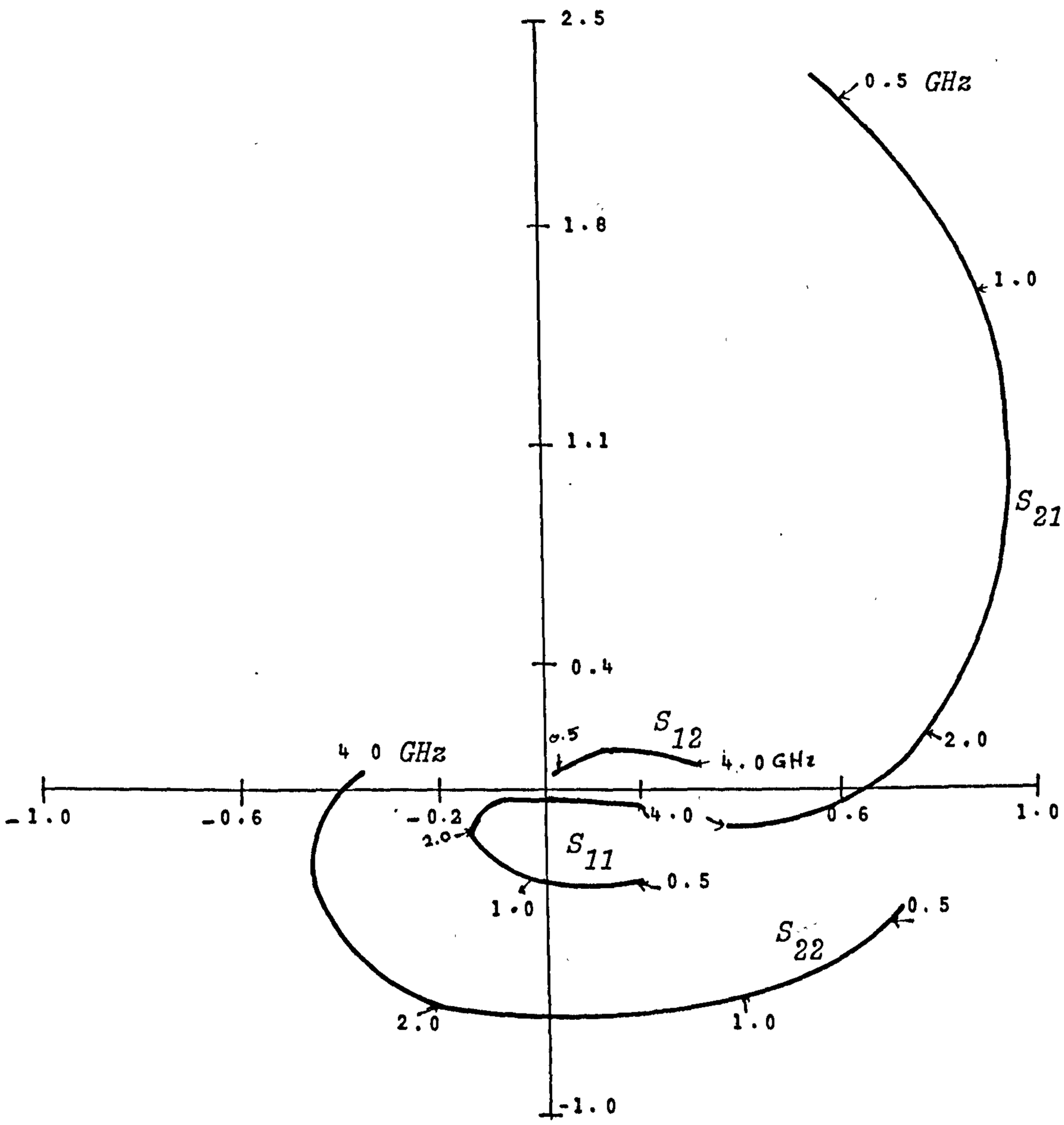


Fig. 6. 12 The S-parameter polar plots of the SB630 Transistor over 0.4 - 4.0 GHz frequency range (V_{ce}=5V., I_c=10mA)

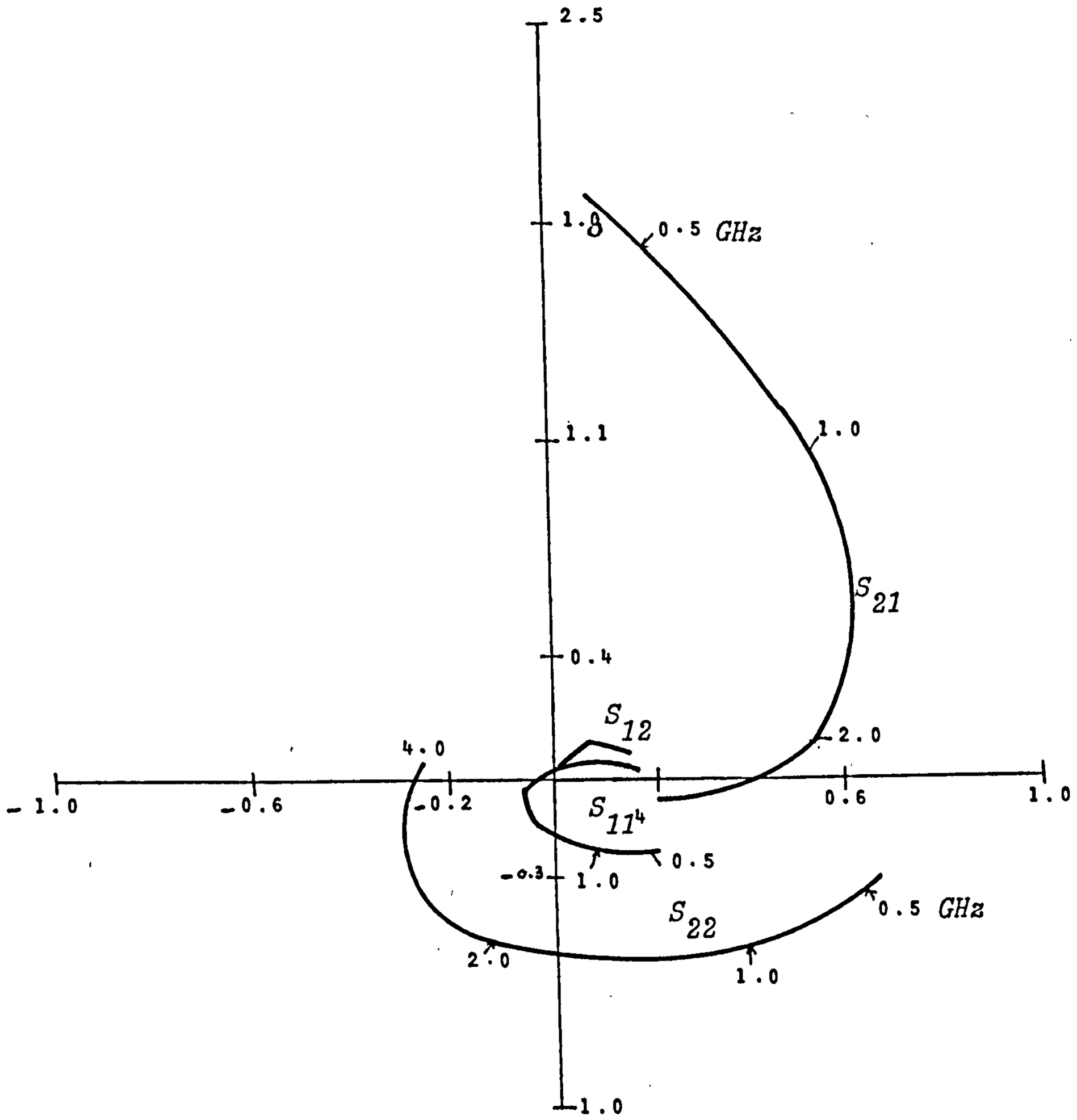


Fig. 6. 13. The S-parameter polar plots of the SB420 Transistor over 0.4 - 4.0 GHz frequency range (V_{ce}=2V., I_c=10mA)

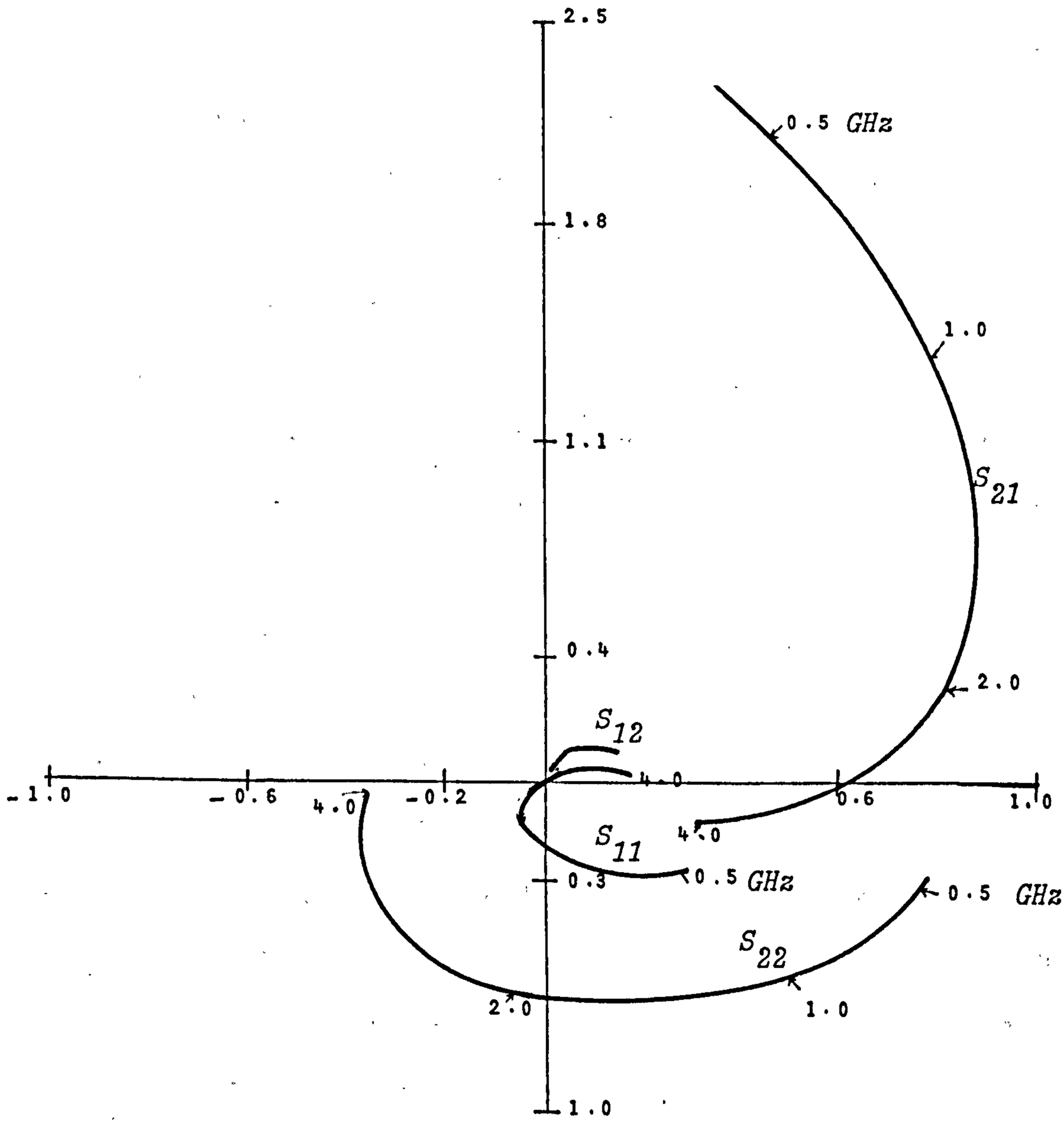


Fig. 6.14. The S-parameter polar plots of the SB420 Transistor over 0.4 - 4.0 GHz frequency range (V_{ce}=5V., I_c=10mA)

6.6. Discussion and Conclusion

The S-parameters of the SB630 transistor have been formulated in terms of its equivalent circuit components. The analysis equations of the S-parameters of the transistor, formulated in this Chapter, will be used in Chapters 7 and 8. This is to formulate an objective function for optimization described also in Chapters 7 and 8.

The calibration pieces required for system calibration, and to maintain a plane of measurement at the device terminals have been successfully mounted on strip line packages identical to those used for the transistors.

The measurement of h_{fe} and the output capacitance of the transistor at three different bias conditions were obtained and they are shown in Figs. 6.8 and 6.9.

The S-parameters of the SB630 and SB420 transistors have been measured at several bias conditions and they are shown in Figs. 6.11 -6.14. They have been shown to be repeatable to within $\pm$ 0.9%.

The author concludes that a standard termination of known impedance - frequency dependence can be used instead of a matched load to terminate the measuring system during calibration. This avoids matched-load difficulties at microwave frequencies. The measured S-parameters of the SB630 and SB420 transistors will be used in the formulation of the objective function in Chapters 7 and 8, and also in Chapter 8 to determine values of the equivalent circuit components for the transistors.

6.7 REFERENCES

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7.1. Introduction

In computer aided studies of complicated transistor equivalent circuits, optimization may take two forms.[7(1-4)] One is basically analytical, in which one may have the properly programmed machines capable of doing a large number of complicated calculations. The other, is a more sophisticated approach usually applying an optimization technique to search for optimum circuit component values under suitable boundary conditions to give reasonable agreement between the measured and optimized results. The equivalent circuit component values are varied until the difference between the measured and optimized results is below a satisfactory limit.

Also, in device modelling, one has to choose an optimization routine which handles several requirements. One of the most important is the upper and lower bounds of the individual circuit components. This is to give reasonable values for circuit components when the agreement between the measured and optimized results is acceptable.

In this chapter, an objective function with suitable boundary conditions will be formulated in terms of the measured S-parameters of the preceeding chapter, and S-parameters theoretically calculated from the equivalent circuit of the transistor.

An optimization routine called "OPTHKJ" using the Hooke-Jeaves Method,[7(5)] will be applied to minimize the objective function and to give optimum values for the equivalent circuit components. Also, in this chapter, an error will be introduced to the calculated S-parameters in chapter 6, in order to investigate the sensitivity of the resulting values.

7.2. Formulation of The Objective Function

In the formulation of the objective function the measured and calculated complex S-parameters were considered. The sums of the difference squared of the corresponding S-parameters over the frequency range up to 4.0 GHz were calculated with suitable weighting factors using the S-parameter analysis equations of Appendix E.

The objective function can now be represented by the following expression,

$$F = \sum_{k=1}^{K=N} \{ \sum_{I=1}^{I=4} W(I) \{ (R_e(S_c(I,K) - S_m(I,K)))^2 + (Im(S_c(I,K) - S_m(I,K)))^2 \} \} \qquad 7.1.$$

in which,

F = Objective function value,

S_c = Calculated S-parameters,

S_m = Measured S-parameter,

R_e = Real part,

Im = Imaginary part,

N = Number of frequency points,

and W = Weighting factor.

7.3. Application of "OPTIIKJ" to Transistor Equivalent Circuit.

The S-parameters analysis equation of Appendix E and the complicated objective function of the proceeding section were computer programmed and included as an analysis subroutine in the complete "OPTHKJ" optimization routine, available in the Computer Science Department. The listing of the final version of this analysis subroutine is shown in Appendix F.

The calculated S-parameters of Section 6.2 were considered here to represent the measured S-parameters. The optimization routine "OPTHKJ" was then applied to minimize the objective function and to give optimum values for the circuit components which gave the calculated S-parameters for frequencies up to 4.0 GHz. This was to ensure that "OPTHKJ" was capable of minimizing the objective function and to give the equivalent circuit component values.

To carry out the optimization procedure, initial values, lower and upper bounds, weighting factors, and step sizes were set up, see Table. 7.1.

The values of Table 7.1 were obtained by experiment, as those giving most rapid convergence compatible with small sensitivity to small errors in the measured S-parameters.

The flow diagram of the complete optimization cycle is shown in Fig. 7.1. The S-parameters were first calculated using the corresponding initial values for the components of the S-parameter's analysis equations of Appendix E. These calculated S-parameters were compared to the measured ones. The circuit component values were altered by the optimization sequence and the resultant S-parameters were then compared to those measured. This cycle was repeated until the difference between the calculated and measured S-parameters was below a certain value ε_0. The set of the equivalent circuit component values which give agreement between the measured and calculated S-parameters were listed. The objective function value at this set of component values was also given.

TABLE 7.1.

The Set-up procedure for Optimization routine ("OPTHKJ")

See Section 7.2.

Circuit Element	Initial Value	Lower Bounds	Upper Bounds	Step Size	Weighting Factors W(I)
$R_{bb'}$	113, Ohms	50, Ohms	250, Ohms	10, Ohms	W(1) = 10
R_e	150, Ohms	50, Ohms	250, Ohms	10, Ohms	W(2) = 5
R_c	250, Ohms	100, Ohms	400, Ohms	10, Ohms	W(3) = 50
R_s	400, Ohms	250, Ohms	600, Ohms	10, Ohms	W(4) = 10
$C_{b'e}$	4.558 pF	2.0 pF	1.0 pF	0.2 pF	
$C_{bc'}$	0.32 pF	0.1 pF	1.0 pF	0.01 pF	
C_o	0.6 pF	0.1 pF	1.0 pF	0.011 pF	

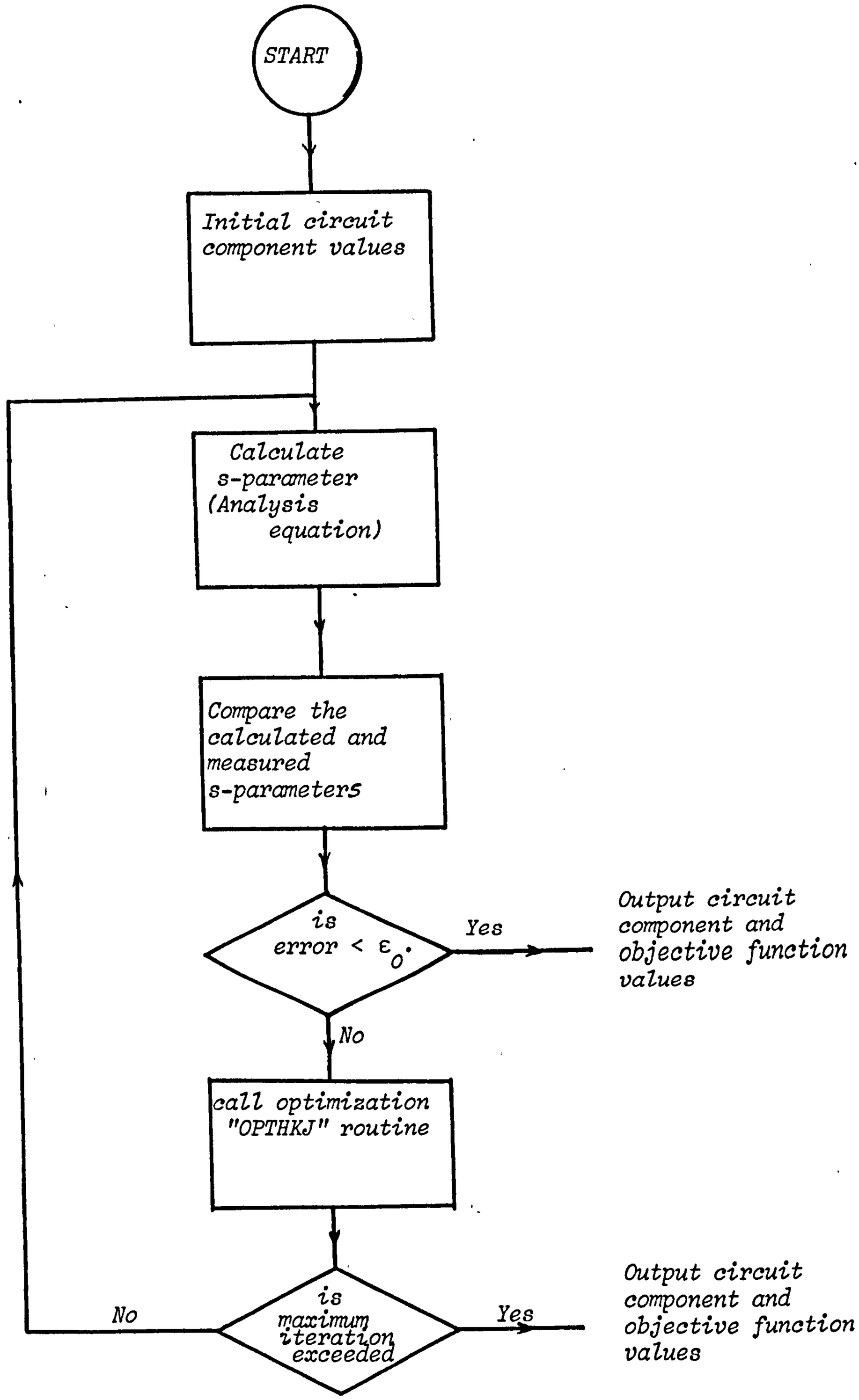

Fig. 7.1. Flow-diagram of the optimization cycle.

It was found that the time taken by the optimization to reach optimum values for the equivalent circuit components, which are reasonably close to the actual values, was approximately 15 minutes. This time is not only large but also very costly. It was found that, in order to speed up the process of the optimization cycle the equivalent circuit components could be reduced to 7 instead of 9. This was done by using the d.c. measurement of β and the low-frequency measurement of the output capacitance C_{ob} as follows.

$$\beta_o = g_m R_e \qquad 7.2.$$

and

$$C_{ob} = C_{bc'} + C_{b'c'} \qquad 7.3.$$

Therefore, g_m and $C_{b'c'}$ may be expressed in terms of R_e and $C_{bc'}$ in the S-parameters' analysis equations. Thus the optimization can be reduced to choosing values for the remaining seven elements, $R_{bb'}$, R_c, R_e, R_s, $C_{b'e}$, $C_{bc'}$ and C_o.

This reduction in the number of equivalent circuit component reduces the time taken by the optimization. The objective function was successfully minimized and the equivalent circuit optimum values were reached in approximately 2 minutes after 60 iterations, using S-parameter measurements at 8-frequency points over the frequency range 0.5 - 4.0 GHz.

The optimization routine was repeated using the calculated S-parameters at the individual frequency points, 0.5 and 2.0 GHz. This was to investigate the possibility of using S-parameter measurements at fewer frequency points and still obtaining optimum values for circuit components agreeing with those expected.

The circuit component optimum values for each case are compared to those which actually gave the calculated S-parameters, used in the optimization, in Table 7.2.

The objective function values at the end of each optimization cycle and the time taken are also given in Table 7.2.

7.4. The Dependance of Circuit Components on the S-parameters

In spite of accurate calibration and correction programmes, the measured S-parameters of a device using the H.P. Network Analyser system usually contain some errors. These errors are normally associated with the components of the Network An alyser. That is, the polar display and the sweep oscillator. These errors are normally $\pm$ 2%.

On this basis, the author introduced a $\pm$2% error to the calculated S-parameters and investigated the resultant variation in the circuit component values. The calculated S-parameters at 1.0 GHz of Section 6.2 were used for this investigation.

The "OPTHKJ" optimization routine was also applied here in order to obtain the corresponding equivalent circuit component values which result from the introduced percentage changes in the S-parameters. Since S_{11} and S_{21} are analogous to S_{12} and S_{22}, only the first two were considered.

Table 7.3 represents the percentage changes in the circuit component values as S_{11} and S_{21} vary between $\pm$2% of their calculated amplitudes. The last two columns were obtained respectively by increasing S_{11} and decreasing S_{21} by 2% simultaneously at 1.0 GHz, and decreasing S_{11} and increasing S_{21} by 2% simultaneously.

From the results of Table 7.3, one can estimate by how much the circuit component values have to be varied in order to meet $\pm$2% errors in the measured S_{11} and S_{21} parameters.

TABLE 7.2-

The Optimized Equivalent Circuit Component Values.*

Circuit Element	Exact Value	Initial Value	Optimized value using 8-freq. points s-parameter measurements	Optimized value using one freq. point s-parameter measurements.	
				0.5 GHz	2.0 GHz
$R_{bb'}$	113 ohms	130 ohms	112.87 ohms	112.76 ohms	112.74 ohms
R_c	150 ohms	190 ohms	149.86 ohms	149.38 ohms	149.27 ohms
R_e	250 ohms	300 ohms	250.24 ohms	250.63 ohms	250.61 ohms
R_s	400 ohms	320 ohms	400.50 ohms	401.52 ohms	402.19 ohms
$C_{b'e}$	4.558 pF	1.57 pF	4.557 pF	4.559 pF	4.558 pF.
$C_{bc'}$	0.32 pF	0.45 pF	0.320 pF	0.32 pF	0.32 pF
C_o	0.6 pF	0.75 pF	0.6006 pF	0.6009 pF	0.601 pF
Objective function value	1.2815E-7	14.775	1.28218E-7	1.2852E-7	1.2836E-7
Time taken and number of iterations.			3 minutes, 100 iterations	2 minutes, 60 iterations	2 minutes 60 iterations

*The remaining circuit components $C_{b'c'}$ and g_m could be found using Equations 7.3 and 7.2 respectively.

TABLE 7.3

The Percentage Change in the Equivalent Circuit Component Values, results of 10 optimization runs.

Circuit Element Values	Percentage change in S_{11}		Percentage change in S_{21}		Percentage changes in S_{11} and S_{21}	
	2%	-2%	2%	-2%	2%,-2%	-2% , 2%
$R_{bb'}$ = 113 Ohms	3.71%	-3%	0.79%	-2.1%	2.78%	-2.94%
R_e = 250 Ohms	-0.5	2.5	2.5	-7.5	-7.8	5.67
R_c = 150 Ohms	0.1	0.3	2.5	5.09	-4.9	2.3
R_s = 400 Ohms	0.02%	-1.2	-3.2	5.1	5.52	-3.6
$C_{b'e}$ = 4,558 pF	1.97	0.87	3.8	2.09	5.09	2.16
$C_{bc'}$ = 0.32 pF	1.56	0.6	0.065	1.85	1.87	1.25
C_o = 0.6 pF	2.17	-0.34	-6.0	7.6	8.6	8.16

The tabulated percentage changes in circuit component values were estimated by applying the "OPTHKJ" optimization routine under the same boundary conditions, and the set of circuit component values which gave an approximately identical objective function value in each case was found.

7.5. Conclusion

From the test using a mathematical model, an optimization program has been developed with a suitable objective function such that parameter values can be estimated with the desired robustness and accuracy. Furthermore, the technique is applicable to the problem of determining the sensitivity of the derived parameters, to the errors in the S-parameter measurements.

It is concluded that this technique can be applied to the modelling of an appropriate range of high frequency transistors. This is investigated in the following chapter.

7.6 REFERENCES

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CHAPTER 8

RESULTS AND DISCUSSIONS

8.1. Introduction

It was stated in Chapter 1 that, the approximated equivalent circuit of Fig.2.7.b would be used to represent the SB630 and SB420 integrated bipolar transistors at frequencies up to an beyond f_T. The S-parameters of these transistors were measured at several bias conditions at microwave frequencies up to 4.0 GHz in Chapter 6 and they are shown in Figs. 6.12-6.15. Also in Chapter 1, it was stated that an optimization routine would be applied to the transistor equivalent circuit components to give the component values of the equivalent circuit. With this in mind, an optimization routine called "OPTHKJ"[7(5)] was applied in the preceeding chapter using the calculated S-parameters of Section 6.2. See Fig. 6.3. This was to ensure the capability of this optimization routine for obtaining the equivalent circuit component values. In Chapter 7, it was concluded that the application of this optimization routine to the equivalent circuit components using the calculated S-parameters was very successful. Hence, with great confidence, the "OPTHKJ" could be applied here to give values for the equivalent circuit components which in turn give S-parameters agreeing with those measured over the frequency range of interest.

8.2. Equivalent Circuit Component Values of Transistors

Here, the author produces values for the components of the equivalent circuit for the measured SB630 and SB420 bipolar transistors of Chapter 6 at two bias conditions. The "OPTHKJ" optimization routine, was also applied here to obtain component values for the equivalent circuit of Fig.2.7b for these two transistors.

TABLE 8.1

The SB630 Transistor Equivalent Circuit Component

Values at

(V_{ce} = 2V, I_c = 5 mA)

β_o = 47.0

Circuit Element	Initial Value	Optimized Value using 8-freq.pts s-parameter measurements	Optimized Values using one-freq.pt (1.0 GHz) s-parameter measurements	Percentage Change in Component Value
$R_{bb'}$	130 Ohms	84.675 Ohms	95.785 Ohms	11.60
R_c	195 Ohms	85.470 Ohms	90.486 Ohms	5.56
R_e	195 Ohms	369.150 Ohms	357.251 Ohms	-3.22
R_s	318 Ohms	285.720 Ohms	296.235 Ohms	3.56
$C_{b'e}$	1.15 pF	7.704 pF	7.434 PF	-3.50
C_{ob}	0.25 pF	0.489 pF	0.490 pF	0.16
$C_{bc'}$	0.15 pF	0.400 pF	0.391 pF	-2.35
C_o	0.75 pF	1.912 pF	1.761 pF	-7.92
$C_{b'c'}$	Calculated from Eqns. 7.2 and 7.3	0.089 pF	0.091 pF	2.20
g_m		0.128 mhos	0.132 mhos	3.03
Objective function values		Initial:3880.5 Opt'zed:59.416	Initial: 8.303 Opt'zed: 0.957	
Time taken (mins.)		5	2	
Number of Iterations		320	140	

TABLE 8.2

The SB630 Transistor Equivalent Circuit Component

Values at

(V_{ce} = 2V, I_c = 10 mA)

β_o = 40.0

Circuit Element	Initial Value	Optimized Value using 8-freq.pts, s-parameter measurements	Optimized Value using one-freq.pt (1.0 GHz) s-parameter measurements	Percentage Change in Component Value
$R_{bb'}$	130 Ohms	95.238 Ohms	92.25 Ohms	-3.14
R_c	195 Ohms	99.602 Ohms	96.160 Ohms	-3.46
R_e	195 Ohms	160.12 Ohms	175.440 Ohms	8.73
R_s	318 Ohms	315.257 Ohms	307.860 Ohms	-1.72
$C_{b'e}$	1.15 pF	9.340 pF	8.960 pF	-4.07
C_{ob}	0.25 pF	0.490 pF	0.510 pF	-3.92
$C_{bc'}$	0.15 pF	0.396 pF	0.385 pF	2.78
C_o	0.75 pF	2.080 pF	1.910 pF	-8.17
$C_{b'c'}$	Calculated from Eqns 7.2 and 7.3	0.094 pF	0.125 pF	1.88
g_m		0.250 mhos	0.228 mhos	-1.67
Objective function Value		Initial: 3288.75 Opt: 59.241	Initial: 8.596 Opt: 0.967	
Time taken (mins)		5	2	
Number of Iterations		320	140	

TABLE 8.3

The SB420 Transistor Equivalent Circuit
Component Values at
(V_{ce} = 2V, I_c = 5 mA)
β_o = 64.0

Circuit Element	Initial Value	Optimized Value using 8-freq. pts s-parameter measurements	Optimized Value using one-freq.pt (1.0 GHz) s-parameter measurements	Percentage Change in Component Value
$R_{bb'}$	130 Ohms	92.950 Ohms	100.840 Ohms	7.82
R_c	195 Ohms	83.704 Ohms	76.743 Ohms	-8.32
R_e	195 Ohms	441.380 Ohms	418.230 Ohms	-5.24
R_s	318 Ohms	279.650 Ohms	286.750 Ohms	2.48
$C_{b'e}$	1.15 pF	4.511 pF	4.265 pF	-5.45
C_{ob}	0.25 pF	0.393 pF	0.416 pF	5.65
$C_{bc'}$	0.15 pF	0.314 pF	0.338 pF	7.10
C_o	0.75 pF	1.480 pF	1.366 pF	-7.70
$C_{b'c'}$	Calculated from Eqns 7.2 and 7.3	0.0785 pF	0.079 pF	0.63
g_m		0.145 mhos	0.158 mhos	8.23
Objective function value		Initial: 5507.27 Opt: 44.625	Initial: 5.844 Opt: 0.559	
Time taken (mins)		5	2	
Number of Iterations		320	140	

TABLE 8.4

The SB420 Transistor Equivalent Circuit Component Values at (V_{ce} = 2V, I_c = 10 mA)

β_o = 52.0

Circuit Element	Initial Value	Optimized Value using 8-freq.pts s-parameter measurements	Optimized Value using one-freq.pt. (1.0 GHz) s-parameter measurements	Percentage Change in Component Value
$R_{bb'}$	130 Ohms	87.721 Ohms	86.091 Ohms	-1.85
R_c	195 Ohms	111.140 Ohms	146.380 Ohms	-4.28
R_e	195 Ohms	196.972 Ohms	215.762 Ohms	8.71
R_s	318 Ohms	324.240 Ohms	312.561 Ohms	-2.88
$C_{b'e}$	1.15 pF	7.182 pF	7.275 pF	1.31
C_{ob}	0.25 pF	0.408 pF	0.390 pF	-4.41
$C_{bc'}$	0.15 pF	0.329 pF	0.320 pF	-2.74
C_o	0.75 pF	1.740 pF	1.672 pF	-3.91
$C_{b'c'}$	Calculated from Eqns 7.2 and 7.3	0.0785 pF	0.070 pF	-10.83
g_m		0.264 mhos	0.241 mhos	3.03
Objective function Value		Initial: 4495.01 Opt: 25.46	Initial: 6.422 Opt. 0.2508	
Time taken (mins)		5	2	
Number of Iterations		320	140	

The objective function analysis subroutine of Appendix F was modified to include the output capacitance C_{ob}, which was to vary from one bias condition to another. That is, the 0.36×10^{-12} term in the analysis subroutine of Appendix F was replaced by C_{ob}. This gives the total of eight components to be optimized.

The boundary conditions of the "OPTHKJ" optimization routine were set up, see Section 7.3, and the objective function was minimized in two ways, firstly using S-parameter measurements at 8-frequency points over the frequency range 0.5 - 4.0 GHz, and secondly using S-parameter measurements at a single frequency of 1 GHz. The circuit component values obtained in both cases are shown in Tables 8.1 and 8.2, for the SB630 transistor and Tables 8.3 and 8.4 for the SB420 transistor. The bias condition at which these circuit component values are valid is also shown in these Tables.

The polar plots of the measured S_{11} and S_{21} parameters and those calculated from the analysis equations of Appendix E, using circuit component values obtained from the optimization using 8-frequency point S-parameter measurements of Tables 8.2 and 8.4, for the SB630 and SB420 transistors at V_{ce} = 2V and I_c = 10 mA bias condition, are compared in Figs. 8.1 and 8.2 at frequencies up to and beyond f_T. This shows the degree of the agreement between the measured results and those obtained from the optimization.

In Table 8.1 - 8.4, the optimum circuit component values using 8-frequency point S-parameter measurements over the frequency range (0.5-4.0 GHz)

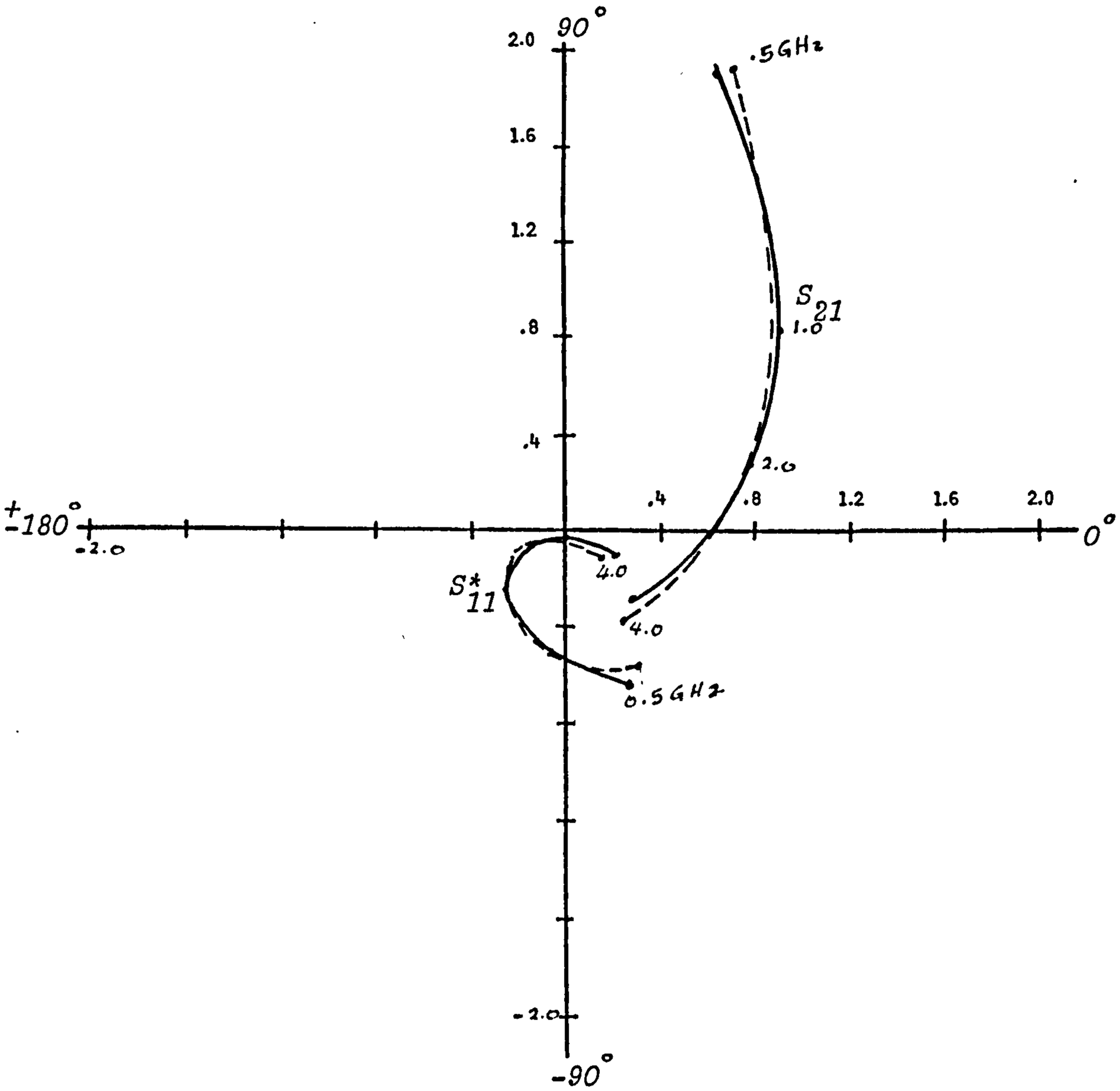

Fig. 8.1. *The polar plots of the S_{21} and S_{11} parameters of the SB630 transistor at (V_{ce} = 2V), I_c = 10 mA)*

——— , *measured*

---- , *optimized*

* , *(The S_{11} actual values are half of those shown)*

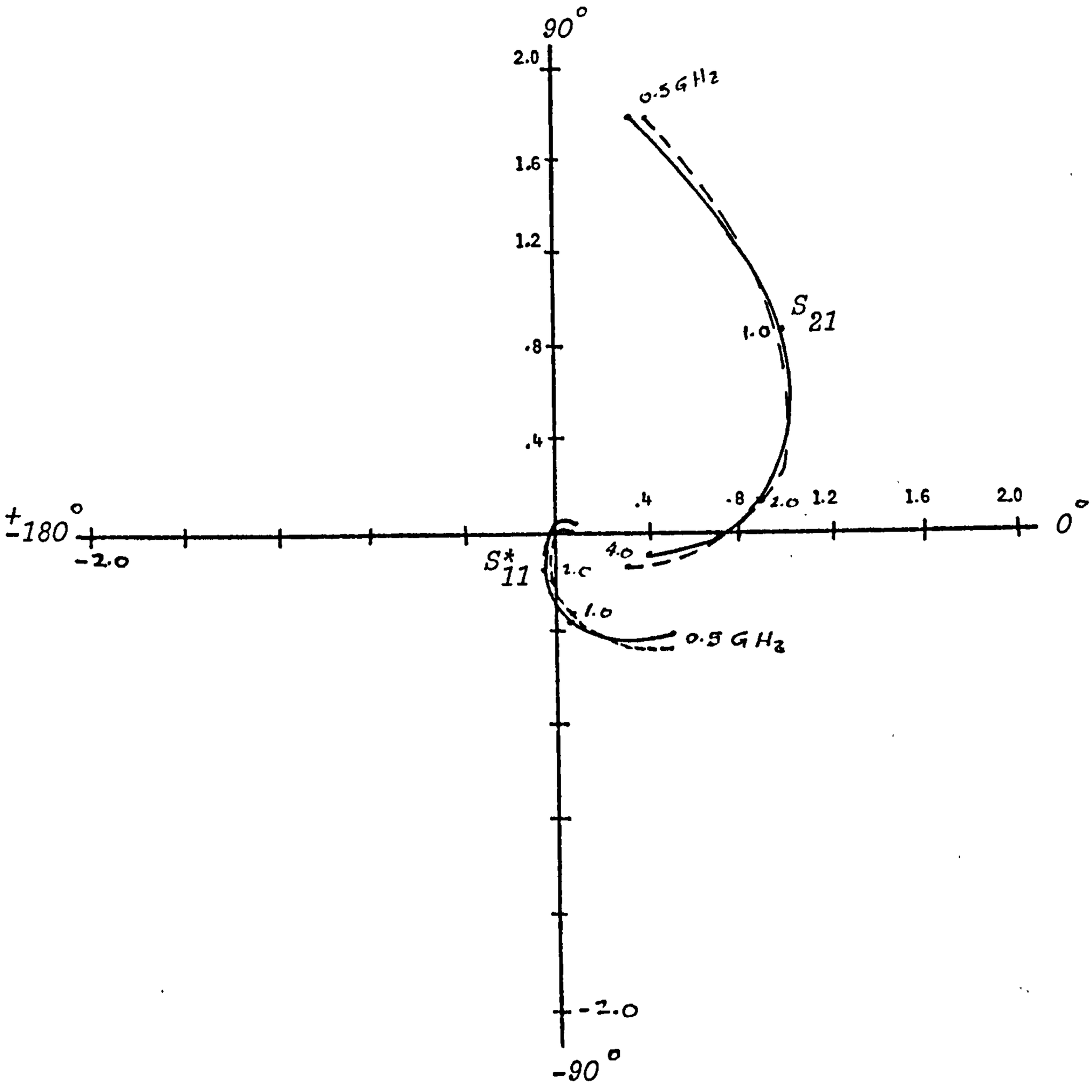

Fig. 8.2. The polar plots of the S_{21} and S_{11} parameters of the SB420 transistor at (V_{ce} = 2V), I_c = 10 mA)

——— , *measured*

----- , *optimized*

* , *(The S_{11} actual values are half of those shown)*

are different from those obtained using only one-frequency point S-parameter's measurements in the optimization. This is because, when using more than one-frequency point S-parameter measurements, the optimization routine will give values for the equivalent circuit components which in turn give a close agreement between the S-parameters, measured and optimized, over the whole frequency range of interest. Hence, the resultant component values will be slightly different in each case. The resultant percentage changes in circuit component values between the two cases are given in Tables 8.1 - 8.4 for each transistor at the specified bias condition.

Here, the author gave larger time and iteration numbers to the otpimization routine to ensure that the objective function had reached its minimum, and therefore the circuit component values at the end of the optimization cycle were valid. The time taken and number of iterations for all the studied cases are also given in Tables 8.1 - 8.4.

8.3. The Transistor Collector Resistance and Output Capacitance

In Section 2.4, the collector resistance R_c was estimated from the output characteristic (I_c vs V_{ce}) displayed on a curve tracer.[2(2)] C_{ob} was measured at relatively low frequencies compared with f_T. The ratio by which C_{ob} was divided between the collector junction and overlap diode capacitances, i.e. $C_{bc'}/C_{b'c'}$, was estimated from the transistor geometry.

The ratio by which C_{ob} has to be divided between its components $C_{bc'}$ and $C_{b'c'}$ has also been calculated, using the optimized results of Tables 8.1 - 8.4.

Using the above technique the collector spreading resistances R_c of the SB630 and SB420 transistors was measured at a relatively large collector current, I_c = 15 mA. Values of 120 and 130 ohms approximately

were obtained for the SB630 and SB420 transistors. If these values are compared with those in Tables 8.1 - 8.4, an average error of at least 30% is envolved.

The measured ratio of $C_{bc'}/C_{b'c'}$ was calculated for both transistors at the two specified bias conditions and it was ranging between 4.0 and 4.5, whereas the transistor geometry gave a value of 8.0. The output capacitance C_{ob} and the overlap diode capacitance values, listed in Tables 8.1 - 8.4, and Equation 7.3 were used in calculating this ratio.

8.4. Conclusion

The optimization routine, successfully tested in Chapter 7, has also been applied in this Chapter in order to obtain the tabulated equivalent circuit component values shown in Tables 8.1 - 8.4. The objective function, formulated in Section 7.2, has been minimized using measurements of the S-parameters at 8-frequency points over the frequency range 0.5 - 4.0 GHz and then using S-parameter measurements at a single frequency of 1 GHz. The circuit component values obtained for each case are shown in Tables 8.1 - 8.4. The percentage changes in circuit component values using S-parameter measurements at a single frequency in the minimization of the objective function are also shown.

The frequency responses of the S-parameters calculated from the optimized circuit component values, and the measured S-parameters have been compared.

The collector resistance of the transistors has been measured using a curve tracer and its value was compared with that obtained by the optimization.

The ratio by which the output capacitance C_{ob} has to be divided between the collector junction $C_{b'c'}$ and the overlap diode $C_{bc'}$ capacitances has been estimated and compared to that used earlier in Section 2.3.[2(2)]

As expected, Tables 8.1 - 8.4 show the following:

1. The base resistance $R_{bb'}$ of the individual transistor is approximately constant with respect to an increase in collector current.
2. The output capacitance C_{ob}, at constant V_{ce}, is directly proportional to the collector current. This is due to a decrease in the effective collector-base junction voltage resulting in a narrower depletion region width as the collector current increases.
3. The dynamic emitter resistance R_e, is inversely proportional to the collector current.
4. The base-emitter junction capacitance $C_{b'e}$, is directly proportional to the collector current for constant collector-emitter voltage.
5. As the emitter diffusion area of an integrated circuit transistor is reduced, the output capacitance C_{ob}, and the base-emitter junction capacitance $C_{b'e}$ is decreased, and the dynamic resistance R_e is increased.

The author concludes that, if the collector resistance R_c measured on a curve tracer is to be used in the equivalent circuit, an error of at least 30% is included in this value. Also, if the transistor geometry is to be used in estimating the ratio by which the output capacitance C_{ob} is divided between $C_{bc'}$ and $C_{b'c'}$, a factor of 2 is included in this ratio. That is, the ratio obtained using the transistor geometry is approximately twice that obtained using the optimization technique. See Section 2.4.

CHAPTER 9

THESIS CONCLUSIONS

The objective of this thesis was to develop a method for measuring bipolar integrated transistors having $f_T \simeq 2.5$ GHz. It was also to establish an equivalent circuit which represents these transistors over the frequency range up to and beyond f_T.

A Miller equivalent circuit was deduced from the equivalent circuit model of the transistor using nodal analysis techniques. The voltage and current gain frequency responses of the transistor, were estimated from the Miller equivalent circuit. A method for calculating the emitter-junction capacitance $C_{b'e}$ from the f_T measurement was developed.[2(3)] A simple equivalent circuit model differing from the conventional hybrid-Π representation was derived.[2(4)]

A computer aided correction programme was implemented and successfully applied for measuring the transistor S-parameters. This programme was modified to overcome the matched load termination difficulties at microwave frequencies.

A thin film resistor was characterized at frequencies up to 8.0 GHz for use as a standard termination in calibrating the network analyser. An equivalent circuit model which accurately represents this resistor was obtained. The discontinuity effects at the plane of measurements was included in this circuit model.

The transistors to be measured in this research were in chip-form. A strip-line package header was designed to fit the H.P. test fixture jig and to hold the various transistor chips.

The S-parameters of the integrated bipolar transistors were measured at several bias conditions using the modified computer aided correction programme. A similar thin film resistor to that characterized was used as a standard termination in calibrating the measuring system, and hence in measuring the S-parameters of the transistors. The measured S-parameters were shown to be repeatable to better than 0.9%.

The Hooke and Jeeves optimization method was used to obtain the transistors' equivalent circuit component values from the measured S-parameters.[7(5)]

An objective function was formulated using the S-parameter analysis equations of Appendix E, and the optimization routine was used to minimize this objective function. The calculated S-parameters in Chapter 6 were used to represent the measured parameters in the objective function to ensure the capability of the optimization method. The exact circuit component values which gave the calculated parameters were obtained by the optimization routine. This showed that the optimization method is satisfactory.

The S-parameters of the transistors were measured at two bias conditions. The Hooke and Jeeves optimization routine was then applied in obtaining the equivalent circuit component values. The equivalent circuit component values for a specified transistor which gave agreement between the measured and theoretical S-parameters at the same bias condition are shown in Tables 8.1 - 8.4. The frequency responses of these parameters were compared. The collector resistance R_c and the ratio by which the output capacitance C_{ob} has to be divided between the collector junction $C_{b'c'}$ and the overlap diode capacitance $C_{bc'}$ were fully discussed.

The author concludes that, if the equivalent circuit represents the measured transistor very accurately, the exact equivalent circuit component values could be obtained using in the optimization S-parameter measurements taken at only a single frequency. The component values obtained will give agreement between the measured and calculated S-parameters over the frequency range for which the transistor was measured. If approximations were involved, it is then adivsable to use S-parameter measurements at several frequency points. This gives a better agreement between the S-parameters at all frequency points over the whole of the frequency range of interest. The values of the collector resistance R_c estimated using a curve tracer includes an average error of approximately 35% and therefore it can not be used in the transistor equivalent circuit. Also, the transistor geometry cannot be used in estimating the ratio by which the measured output capacitance C_{ob} has to be divided between the collector junction and overlap diode capacitances. This is due to the different material under the emitter and base contacts in the formulation of the transistor.

The agreement obtained in this research, between the measured S-parameters and those calculated, using the optimized equivalent circuit component values of Tables 8.1 - 8.4, from the approximated equivalent circuit for the transistors was satisfactory at certain frequency points. At others, the difference between these parameters was not negligible but acceptable.

The author suggests that, a more accurate transistor equivalent circuit has to be found. This is to obtain a better agreement between the measured and calculated S-parameters over the frequency range of interest.

Since the collector resistance, the output capacitance and the ratio by which it can be divided between the collector junction $C_{b'c'}$ and the overlap diode capacitance C_{bc}, could be obtained using optimization, the author concludes that, the low frequency measurements on these components is not essential. This is to avoid approximation in estimating their values.

The circuit designer only needs to measure the S-parameters of the transistor at a few frequency points and include all the possible components of the transistor in its equivalent circuit model. Then, optimization can be used to obtain component values for the complete transistor equivalent circuit.

CHAPTER 10
APPENDICES

APPENDIX A

TRANSISTOR EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit model of the transistor described in Chapter 2 is analysed here in detail. This is to outline the procedure for obtaining the various equations mentioned in Section 2.5. The output circuit is combined in one element to simplify the analysis and hence the solution of the equations involved. See Fig. 2.10

The node current equation at B, B' and C' junctions of the circuit of Fig. 2.10 are repeated here for convenience, therefore:

$$(G_b+j\omega C_{bc'})e_1 - G_b e_2 - j\omega C_{bc'}e_3 = I_1 \qquad A.1$$

$$- G_b e_1 + (G_b + G_e + j\omega(C_{b'e} + C_{b'c'}))e_2 - j\omega C_{b'c'}e_3 = 0 \qquad A.2$$

and, $$-j\omega C_{bc'}e_1+(g_m-j\omega C_{b'c'})e_2 + (G_L + j\omega(C_{bc'}+C_{b'c'})e_3 = 0 \qquad A.3$$

where G_L is given by Equation 2.1 in the main text,

$$G_b = /R_{bb'} \text{ and } G_e = 1/R_e$$

e_3/e_1 and e_3/e_2 ratios are needed to evaluate certain parameters of the Miller equivalent circuit of Fig. 2.11. These ratios can be found from the solution of EquationsA.2 and A.3 as follows:

Equation A.2 gives:

$$G_b e_1 = (G_b + G_e + j\omega(C_{b'e} + C_{b'c'}))e_2 - j\omega C_{b'c'}e_3 \qquad A.4$$

and Equation A.3 gives:

$$j\omega C_{bc'}e_1 = (g_m - j\omega C_{b'c'})e_2 + (G_L + j\omega(C_{bc'} + C_{b'c'}))e_3 \qquad A.5$$

The determinant D of Equations A.4 and A.5 can be formulated, giving:

$$D = (G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))(G_L+j\omega(C_{bc'}+C_{b'c'}))+j\omega C_{b'c'}(g_m-j\omega C_{b'c'}) \qquad A.6$$

e_2 in terms of e_1 can be found as:

$$e_2 = \frac{e_1}{D} \{ G_b(G_L+j\omega(C_{bc'}+C_{b'c'})) - \omega^2 C_{bc'}C_{b'c'} \} \quad \text{A.7}$$

Similarly e_3 in terms of e_1 is:

$$e_3 = \frac{e_1}{D} \{ j\omega C_{bc'}(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))-G_b(g_m-j\omega C_{b'c'}) \} \quad \text{A.8}$$

Equation A.8 gives:

$$\frac{e_3}{e_1} = - \frac{1}{D} \{ G_b(g_m-j\omega C_{b'c'})-j\omega C_{bc'}(G_b+G_e+j\omega(C_{b'e}+C_{b'c'})) \} \quad \text{A.9}$$

e_3/e_2 ratio can be obtained. Hence,

$$\frac{e_3}{e_2} = - \frac{G_b(g_m-j\omega C_{b'c'}) - j\omega C_{bc'}(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))}{G_b(G_L+j\omega(C_{bc'}+C_{b'c'}))-\omega^2 C_{bc'}C_{b'c'}} \quad \text{A.10}$$

By definition, the Miller admittances Y_{m1} and Y_{m2} of the Miller equivalent circuit of Fig. 2.11 are,[2(14)]

$$Y_{m1} = j\omega C_{b'c'}(1 - e_3/e_2) \quad \text{A.11}$$

$$\text{and } Y_{m2} = j\omega C_{bc'}(1 - e_3/3_1) \quad \text{A.12}$$

where (e_3/e_1) and (e_3/e_2) ratios are given by Equations A.9 and A.10 respectively.

The equivalent-transconductance G_{m1} of the Miller equivalent circuit is obtained from the following relationship:

$$G_{m1} = \frac{e_3}{e_2} \cdot G_L \quad \text{A.13}$$

Next, is to obtain equations for the voltage and current gains for the Miller equivalent circuit of Fig. 2.10. Replacement of G_L by the original output combination in the Miller equivalent circuit gives the circuit of Fig. 2.11.

The output voltage can be easily calculated from Fig. 2.11, giving:

$$e_o = - G_{m1} e_2 . Z_L \qquad \text{A.14}$$

where Z_L is the impedance of the external load R_L in shunt with a series combination of C_o and R_S giving:

$$Z_L = \frac{R_L(1 + j\omega C_o R_S)}{1 + j\omega C_o (R_L + R_S)} \qquad \text{A.15}$$

and G_{m1} is given by equation A.13.

The voltage gain A_v is the output voltage e_o and the input e_1 ratio. e_2 in Equation A.14 has to be evaluated in terms of e_1. e_2/e_1 ratio can be estimated from Fig. 2.11, as follows:

The node current equation at B and B' of Fig. 2.11, are:

$$(G_b + Y_{m2})e_1 - g_b e_2 = I_1 \qquad \text{A.16}$$

and

$$-G_b e_1 + (G_b + G_e + j\omega C_{b'e} + Y_{m1})e_2 = 0 \qquad \text{A.17}$$

The solution of Equation A.17 gives:

$$e_2 = \frac{G_b e_1}{G_b + G_e + j\omega C_{b'e} + Y_{m1}} \qquad \text{A.18}$$

The substitutions of Equations A.15 and A.18 into Equation A.14 yields:

$$e_o = - \frac{G_{m1} G_b R_L (1 + j\omega C_o R_S) e_1}{(1 + j\omega C_o (R_L + R_S))(G_b + G_e + j\omega C_{b'e} + Y_{m1})} \qquad \text{A.19}$$

therefore,

$$A_v = \frac{e_o}{e_1} = - \frac{G_{m1} G_b R_L (1 + j\omega C_o R_S)}{(1 + j\omega C_o (R_S + R_L))(G_b + G_e + j\omega C_{b'e} + Y_{m1})} \qquad \text{A.20}$$

Hence, the current gain A_i can be found. By definition,[2(14)]

$$A_i = A_v . \frac{Z_{in}}{R_L} \qquad \text{A.21}$$

Where R_L is the external load, and Z_{in} is the input impedance of the Miller equivalent circuit of Fig. 2.8 and it can be easily calculated from the node current Equations A.16 and A.17, as follows: The substitution of Equation A.18 into Equation A.16 gives:

$$(G_b + Y_{m2})e_1 - G_b\left(\frac{G_b e_1}{G_b+G_e+j\omega(C_{b'e}+C_{b'c'})}\right) = I_1 \qquad \text{A.21}$$

$$e_1 \left\{G_b + Y_{m2} - \frac{G_b^2}{G_b+G_e+j\omega(C_{b'e}+C_{b'c'})}\right\} = I_1 \qquad \text{A.22}$$

By definition, $Z_{in} = \frac{e_1}{I_1}$. Hence, from Equation A.22 Z_{in} is,

$$Z_{in} = \frac{G_b+G_e+j\omega(C_{b'e}+C_{b'c'})}{(G_b + Y_{m2})(G_b+G_e+j\omega(C_{b'e}+C_{b'c'})-G_b^2} \qquad \text{A.23}$$

APPENDIX B

MILLER EQUIVALENT CIRCUIT COMPONENTS SIMPLIFICATION

In Sections 2.5 and 2.6 of the main text, the equations involved in calculating the Miller equivalent circuit components and hence the voltage and current gains are inconveniently complex and tedious to evaluate. The key ratios in these equations are e_3/e_1 and e_3/e_2. The Miller admittances Y_{m1} and Y_{m2} and the equivalent transconductance G_{m1} of the Miller equivalent circuit of Fig.2.11 are dependent on e_3/e_1 and e_3/e_2 ratios.

The e_3/e_1 and e_3/e_2 ratios, given by Equations 2.25 and 2.26 calculated from the equivalent circuit of Fig.2.10, are approximated here by neglecting higher order terms of the time constants in the numerator and the denominator of these ratios. These approximations are as follows: Equations 2.25 and 2.26 are repeated here, for convenience, thus:

$$\left(\frac{e_3}{e_1}\right) = - \frac{G_b(g_m - j\omega C_{b'c'}) - j\omega C_{bc'}(G_b + G_e + j\omega(C_{b'e} + C_{b'c'}))}{(G_b + G_e + j\omega(C_{b'e} + C_{b'c'}))(G_L + j\omega(C_{bc'} + C_{b'c'})) + j\omega C_{b'c'}(g_m - j\omega C_{b'c'})} \qquad B.1$$

and

$$\left(\frac{e_3}{e_2}\right) = - \frac{G_b(g_m - j\omega C_{b'e'}) - j\omega C_{bc'}(G_b + G_e + j\omega(C_{b'e} + C_{b'c'}))}{G_b(G_L + j\omega(C_{bc'} + C_{b'c'})) - \omega^2 C_{bc'} C_{b'c'}} \qquad B.2$$

Let $\left(\frac{e_3}{e_2}\right) = - \frac{N}{D_2}$ and $\left(\frac{e_3}{e_1}\right) = - \frac{N}{D_1}$

where N denotes the numerator of Equations B.1 and B.2, and these numerators are equal. D_1 and D_2 denote the denumerator of Equations B.1 and B.2 respectively. Hence,

$$N = G_b(g_m - j\omega C_{b'c'}) - j\omega C_{bc'}(G_b + G_e + j\omega(C_{b'e} + C_{b'c'})) \qquad B.3$$

Equation B.3 gives:

$$N = g_m G_b - j\omega C_{b'c'} G_b - j\omega C_{bc'}(G_b+G_e) + \omega^2 C_{bc'}(C_{b'e}+C_{b'c'}) \qquad B.4$$

Collecting real and imaginary parts yields:

$$N = g_m G_b + \omega^2 C_{bc'}(C_{b'e}+C_{b'c'}) - j\omega(G_b C_{b'c'} + C_{bc'}(G_b+G_e)) \qquad B.5$$

at frequencies up to 1 GHz

$$1 > \frac{\omega^2 C_{bc'}}{g_m G_b} (C_{b'e}+C_{b'c'}) \qquad B.6$$

Hence, Equation B.5 reduces to:

$$N = g_m G_b - j\omega(G_b C_{b'c'} + C_{bc'}(G_b+G_e)) \qquad B.7$$

Equation B.7 gives,

$$N = g_m G_b \{1 - j \frac{\omega}{g_m G_b} (G_b C_{b'c'} + C_{bc'}(G_b+G_e))\} \qquad B.8$$

at frequencies up to 5 GHz.

$$1 > \frac{\omega}{g_m G_b} (G_b C_{b'c'} + C_{bc'}(G_b+G_e)) \qquad B.9$$

Hence, Equation B.8 reduces to:

$$N \simeq g_m G_b \qquad B.10$$

Next, D_2 is given by:

$$D_2 = G_b(G_L + j\omega(C_{bc'}+C_{b'c'})) - \omega^2 C_{bc'} C_{b'c'} \qquad B.11$$

where G_L, in Equation B.11, is given by:

$$G_L = \frac{1 + j\omega C_o r_1}{r_2 + j\omega C_o r_3^2}$$

where

$$r_1 = R_S + R_L \qquad \text{B.12}$$

$$r_2 = R_c + R_L \qquad \text{B.13}$$

and $$r_3^2 = R_S R_L + R_c(R_L + R_S) \qquad \text{B.14}$$

Substitution of Equation 2.19 into Equation B.11 gives:

$$D_2 = G_b \left(\frac{1 + j\omega C_o r_1}{r_2 + j\omega C_o r_3^2} + j\omega(C_{bc'} + C_{b'c'})\right) - \omega^2 C_{bc'} C_{b'c'} \qquad \text{B.15}$$

Equation B.15 gives:

$$(r_2 + j\omega r_3^2) D_2 = G_b \{1 + j\omega C_o r_1 + j\omega r_2(C_{bc'} + C_{b'c'}) - \omega^2 C_o r_3^2 (C_{bc'} + C_{b'c'})\}$$

$$- \omega^2 C_{bc'} C_{b'c'} r_2 - j\omega^3 C_o C_{bc'} C_{b'c'} r_3^2 \qquad \text{B.16}$$

The R.H.S. of Equation B.16 gives:

$$\text{R.H.S.} = G_b \{(1 + j\omega C_o r_1)(1 + j\omega r_2(C_{bc'} + C_{b'c'})) + \omega^2 C_o (C_{bc'} + C_{b'c'}) r_1 r_2$$

$$- \omega^2 C_o r_3^2 (C_{bc'} + C_{b'c'})\} - \omega^2 C_{bc'} C_{b'c'} r_2 (1 + j\omega C_o r_3^2 / r_2)$$

$$\text{R.H.S.} = G_b \{(1 + j\omega C_o r_1)(1 + j\omega r_2(C_{bc'} + C_{b'c'})) + \omega^2 C_o (C_{bc'} + C_{b'c'})(r_1 r_2 - r_3^2)\}$$

$$- \omega^2 C_{bc'} C_{b'c'} r_2 (1 + j\omega C_o r_3^2 / r_2)$$

$$\text{R.H.S.} = G_b \{(1 + j\omega C_o r_1)(1 + j\omega r_2(C_{bc'} + C_{b'c'})\} + \omega^2 C_o (C_{bc'} + C_{b'c'}) G_b (r_1 r_2 - r_3^2)$$

$$- \omega^2 C_{bc'} C_{b'c'} r_2 (1 + j\omega C_o r_3^2 / r_2) \qquad \text{B.17}$$

we have, in Equation B.17.

$$r_1 r_2 - r_3^2 = R_L^2 \qquad \text{B.18}$$

$$r_3^2 / r_2 \simeq R_S \qquad \text{B.19}$$

Equation B.18 is valid for R_L up to 1 KΩ. The last term of Equation B.17 at frequencies up to 1.0 GHz reduces to $\omega^2 C_{bc'} C_{b'c'} r_2$.

Hence, Equation B.17 reduces to:

$$\text{R.H.S.} = G_b (1 + j C_o r_1)(1 + j r_2(C_{bc'}+C_{b'c'}))$$

$$+ \omega^2 \{C_o(C_{bc'}+C_{b'c'})G_b R_L^2 - C_{bc'}C_{b'c'}r_2\} \qquad \text{B.20}$$

At frequencies up to 1.0 GHz and R_L = 1 KΩ

$$1 > \omega^2 \{C_o(C_{bc'}+C_{b'c'})R_L^2 - C_{bc'}C_{b'c'}r_2/G_b\} \qquad \text{B.21}$$

Hence, Equation B.17 reduces to:

$$\text{R.H.S.} = G_b(1 + j\omega C_o r_1)(1 + j\omega r_2(C_{bc'}+C_{b'c'})) \qquad \text{B.22}$$

Therefore the approximated e_3/e_2 is

$$\frac{e_3}{e_2} \simeq - \frac{g_m r_2(1+j\omega C_o r_3^2/r_2)}{(1+j\omega C_o r_1)(1+j\omega r_2(C_{bc'}+C_{b'c'}))} \qquad \text{B.23}$$

Equation B.23 can be written in a convenient form as:

$$\frac{e_3}{e_2} \simeq - \frac{g_m r_2(1+j\omega T_1)}{(1+j\omega T_2)(1+j\omega T_3)} \qquad \text{B.24}$$

where,

$$T_1 = C_o r_3^2/r_2 \qquad \text{B.25}$$

$$T_2 = C_o r_1 \qquad \text{B.26}$$

$$T_3 = r_2(C_{bc'}+C_{b'c'}) \qquad \text{B.27}$$

we have,

$$D_1 = (G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))(G_L+j\omega(C_{bc'}+C_{b'c'}))+j\omega C_{b'c'}(g_m-j\omega C_{b'c'}) \qquad \text{B.28}$$

Substitution of G_L into Equation B.28 gives:

$$D_1=(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))(\frac{1+j\omega C_o r_1}{r_2+j\omega C_o r_3^2} + j\omega(C_{bc'}+C_{b'c'}))+j\omega C_{b'c'}(g_m-j\omega C_{b'c'}) \qquad B.29$$

Equation B.29 gives:

$$D_1(r_2+j\omega C_o r_3^2)=(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))\{1+j\omega C_o r_1+j\omega(C_{bc'}+C_{b'c'})(r_2+j\omega C_o r_3^2\}$$
$$+ j\omega C_{b'c'}(g_m-j\omega C_{b'c'})(r_2+j\omega C_o r_3^2) \qquad B.30$$

R.H.S. of Equation B.30 yields:

$$= (G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))\ \{(1+j\omega C_o r_1)(1+j\omega r_2(C_{bc'}+C_{b'c'}))$$
$$+ \omega^2 C_o(C_{bc'}+C_{b'c'})r_1 r_2 - \omega^2 C_o(C_{bc'}+C_{b'c'})r_3^2\}$$
$$+ j\omega C_{b'c'}(g_m r_2+\omega^2 C_{b'c'}C_o r_3^2) - \omega^2 C_{b'c'}(g_m C_o r_3^2 - r_2 C_{b'c'}) \qquad B.31$$

Equation B.31 gives:

$$= (G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))\ \{(1+j\omega C_o r_1)(1+j\omega r_2(C_{be'}+C_{b'c'}))$$
$$+ \omega^2 C_o(C_{bc'}+C_{b'c'})(r_1 r_2 - r_3^2)\}$$
$$+ j\omega C_{b'c'}(g_m r_2+\omega^2 C_{b'c'}C_o r_3^2) - \omega^2 C_{b'c'}(g_m C_o r_3^2 - r_2 C_{b'c'}) \qquad B.32$$

In Equation B.32, at 1.0 GHz and R_L = 1 KΩ,

$$g_m r_2 > \omega^2 C_{b'c'}C_o r_3^2 \qquad B.33$$

$$g_m C_o r_3^2 > r_2 C_{b'c'} \qquad B.34$$

$$1 > \omega^2 C_o(C_{bc'}+C_{b'c'})(r_1 r_2 - r_3^2) \qquad B.35$$

and
$$1 > \frac{\omega C_{b'c'}\ g_m r_2}{G_b + G_e} \qquad B.36$$

Hence, Equation B.30 reduces to:

$$D_1(r_2+j\omega C_o r_3)=(G_b+G_e)(1+j\frac{\omega}{G_b+G_e}(C_{b'e}+C_{b'c'}))(1+j\omega C_o r_1)(1+j\omega r_2(C_{bc'}+C_{b'c'}))$$

This gives:

$$D_1 = \frac{(G_b+G_e)(1+j\frac{\omega}{G_b+G_e}(C_{b'e}+C_{b'c'}))(1+j\omega C_o r_1)(1+j\omega r_2(C_{bc'}+C_{b'c'}))}{r_2(1+j\omega C_o r_3/r_2)} \qquad B.37$$

Hence,

$$\frac{e_3}{e_1} = \frac{-g_m G_b r_2(1 + j\omega C_o r_3/r_2)}{(G_b+G_e)(1+j\frac{\omega}{G_b+G_e}(C_{b'e}+C_{b'c'}))(1+j\omega C_o r_1)(1+j\omega r_2(C_{bc'}+C_{b'c'}))} \qquad B.38$$

Equation B.38 can be written as:

$$\frac{e_3}{e_1} = \frac{-g_m G_b r_2(1 + j\omega T_1)}{(G_b+G_e)(1+j\omega T_2)(1+j\omega T_3)(1+j\omega T_4)} \qquad B.39$$

where $T_4 = \frac{(C_{b'e}+C_{b'c'})}{(G_b + G_e)}$ B.40

and T_1, T_2 and T_3 are given by Equations B.25, B.26 and B.27.

we see that $C_{bc'}$ and $C_{b'c'}$ appear separately only in Equation B.40.

P roviding $C_{b'e} > C_{b'c'}$ B.41

then Equation B.40 reduces to

$$T_4 \simeq \frac{C_{b'e}}{G_b+G_e} \qquad B.42$$

The capacitance $C_{bc'}$ and $C_{b'c'}$ now appear as one term ($C_{bc'}+C_{b'c'}$) which is the whole of C_{ob}.

Hence C_{ob} can be placed between the base terminal B and the collector junction C' in the equivalent circuit of Fig. 2.4. See Fig. 2.17. Equation B.41 is valid for most transistors.

APPENDIX C

SIMPLIFIED EQUIVALENT CIRCUIT ANALYSIS

The purpose of this Appendix is to show a deviation for the voltage and current gain responses from the simplified equivalent circuit of Fig. 2.17 and to obtain its Miller equivalent circuit, shown in Fig.2.19 in the main text.

The node current equation at B, B' amd C' of the simplified equivalent circuit of Fig.2.17 can be written as:

$$(G_b+j\omega C_{ob})e_1' - G_b e_2' - j\omega C_{ob} e_3' = I_1' \qquad C.1$$

$$- G_b e_1' + (G_b+G_e+j\omega C_{b'e})e_2' = 0 \qquad C.2$$

$$- j\omega C_{ob} e_1' + g_m e_2' + (G_L+j\omega C_{ob})e_3' = 0 \qquad C.3$$

By definition, the Miller admittance Y_m at the input of Fig. 2.18 circuit is:[2(1,4)]

$$Y_m = j\omega C_{ob}(1 - e_3'/e_1') \qquad C.4$$

and $$G_m = - \frac{e_3'}{e_2'} G_L \qquad C.5$$

where, G_L is given by Equation 2.19

To evaluate Y_m and G_m, e_3'/e_1' and e_3'/e_2' ratios have to be calculated. These ratios can be obtained from the relative solution of Equations C.2. and C.3, as follows:

Equation C.2 gives,

$$e_2' = \frac{G_b e_1'}{G_b+G_e+j\ C_{b'e}} \qquad C.6$$

Substitution of Equation C.6 into Equation C.3 gives:

$$-j\omega C_{ob}e_1' + \frac{g_m G_b e_1'}{G_b+G_e+j\omega C_{b'e}} + (G_L+j\omega C_{ob})e_3' = 0 \qquad C.7$$

Equation C.7 yields:

$$e_1' \{ \frac{g_m G_b}{(G_b+G_e+j\omega C_{b'e})} - j\omega C_{ob}\} = -(G_L+j\omega C_{ob})e_3'$$

then,

$$e_3' = \frac{-(g_m G_b - j\omega C_{ob}(G_b+G_e+j\omega C_{b'e}))e_1'}{(G_b+G_e+j\omega C_{b'e})(G_L+j\omega C_{ob})}$$

therefore,

$$\frac{e_3'}{e_1'} = - \frac{g_m G_b - j\omega C_{ob}(G_b+G_e+j\omega C_{b'e})}{(G_b+G_e+j\omega C_{b'e})(G_L+j\omega C_{ob})} \qquad C.8$$

and

$$\frac{e_3'}{e_2'} = \frac{e_3'}{e_1'} \cdot \frac{e_1'}{e_2'} \qquad C.9$$

The substitution of Equations C.6 and C.8 into Equation C.9 gives:

$$\frac{e_3'}{e_2'} = - \frac{g_m G_b - j\omega C_{ob}(G_b+G_e+j\omega C_{b'e}}{G_b(G_L+j\omega C_{ob})} \qquad C.10$$

Hence, Y_m and G_m of the simplified Miller equivalent circuit of Fig. 2.18 given by Equations 6.4 and 6.5, can be evaluated.

The voltage and current gainsA_v and A_i expressions of the simplified equivalent circuit of Fig. 2.18 can be formulated as follows:

The output voltage e_o' is given by:

$$e'_o = G_m e'_2 Z_L \qquad C.11$$

where G_m is the equivalent transconductance and it is given by Equation C.5. and, Z_L is given by Equation 2.29 of the main text.

e'_2 in terms of e'_1 is given by Equation C.6.

Substitution of Equations 2.11 and C.6 into Equation C.11 gives:

$$e'_o = \frac{-G_m G_b R_L (1 + j\omega C_o R_S) e'_i}{(G_b + G_e + j\omega C_{b'e})(1 + j\omega C_o (R_S + R_L))} \qquad C.12$$

The voltage gain A'_v is e'_o/e'_i. Hence, Equation C.12 gives:

$$A'_v = \frac{e'_o}{e'_i} = \frac{-G_m G_b R_L (1 + j\omega C_o R_S)}{(G_b + G_e + j\omega C_{b'e})(1 + j\omega C_o (R_S + R_2))} \qquad C.13$$

By definition, the current gain A_i is,

$$A'_i = A'_v \cdot \frac{Z'_{in}}{R_L} \qquad C.14$$

In which, Z'_{in} is the input impedance of the simplified Miller equivalent circuit of Fig. 2.18, and it is given by

$$Z'_{in} = \frac{G_b + G_e + j\omega C_{b'e}}{(G_b + G_e j\omega C_{b'e})(G_b + Y_m) - G_b^2} \qquad C.15$$

APPENDIX D

EXPLICIT SOLUTIONS OF THE SCATTERING PARAMETERS OF THE EQUIVALENT ERROR NETWORKS AND THE S-PARAMETERS OF THE DEVICE

To evaluate the error network parameter 10-equations are required. These equations are easily obtained from the calibration procedure outlined in Section 3.2 of the main text. Substituting for these error parameters with their corresponding values into Equations 3.1 - 3.5, the corrected S-parameters of the device under test can be calculated.

The measured reflection and transmission coefficients equations, with the device connected, are repeated here for convenience.

$$M_{R1} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = M_{11} + \frac{1}{D}\ \{M_{21}M_{12}S_{11}(1-S_{22}N_{22})+M_{21}M_{12}N_{22}S_{21}S_{12}\} \qquad 3.1$$

$$M_{T1} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = M_L + \frac{1}{D}\ (S_{21}M_{21}M_{12}) \qquad 3.2$$

and,

$$M_{R2} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = N_{11} + \frac{1}{D}\ \{N_{21}N_{12}S_{22}(1 - S_{11}M_{22}) + N_{21}N_{12}M_{22}S_{21}S_{12}\} \qquad 3.3$$

$$M_{T2} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = N_L + \frac{1}{D}\ (S_{12}N_{21}N_{12}) \qquad 3.4$$

where,

$$D = 1 - S_{11}M_{22} - S_{22}N_{22} - S_{21}S_{12}M_{22}N_{22} + S_{11}S_{22}M_{22}N_{22} \qquad 3.5$$

Since some parameters appear as a product in the above equations, namely $M_{21}M_{12}$, $N_{21}N_{12}$, $M_{21}N_{12}$ and $M_{12}N_{21}$ it is not necessary to determine explicity the scattering parameters of the equivalent error networks. The necessary parameters can be redefined as:

$$x_1 = M_{11}$$
$$x_2 = M_{21}M_{12}$$
$$x_3 = M_{22}$$
$$x_4 = M_{21}N_{12}$$
$$M = M_L$$
$$x_5 = N_{11}$$
$$x_6 = N_{21}N_{12}$$
$$x_7 = N_{22}$$
$$x_8 = M_{12}N_{21}$$
$$N = N_L$$

Equations3.1 - 3.5 then become:

$$M_{R1} = x_1 + \frac{x_2}{D} \{S_{11}(1 - S_{22}x_7) + x_7S_{21}S_{12}\} \quad 3.1$$

$$M_{T1} = M + \frac{x_4}{D} \cdot S_{21} \quad 3.2.$$

$$M_{R2} = x_5 + \frac{x_6}{D} \{S_{22}(1 - S_{11}x_3) + x_3S_{12}S_{21}\} \quad 3.3$$

and,

$$M_{T2} = N + \frac{x_8}{D} \cdot S_{12} \quad 3.4.$$

where,

$$D = (1 - S_{11}x_3)(1 - S_{22}x_7) - x_3x_7S_{21}S_{12} \quad 3.5$$

The equationsrequired to evaluate the necessary error network parameters, discussed in Section 3.2, are:

$$M_1 = x_1 \quad D.1$$
$$M_2 = M \quad D.2$$
$$M_3 = x_5 \quad D.3$$

$$M_4 = N \qquad \text{D.4}$$

$$M_5 = x_1 - \frac{x_2}{1+x_3} \qquad \text{D.5}$$

$$M_6 = x_5 - \frac{x_6}{1+x_7} \qquad \text{D.6}$$

$$M_7 = x_1 + \frac{x_2}{1-x_3} \qquad \text{D.7}$$

$$M_8 = x_5 + \frac{x_6}{1-x_1} \qquad \text{D.8}$$

$$M_9 = M + \frac{x_4}{1-x_3x_7} \qquad \text{D.9}$$

and $$M_{10} = N + \frac{x_8}{1-x_3x_7} \qquad \text{D.10}$$

The error parameters x_1,M, x_5 and N are obtained directly from Equations D.1 - D.4. The remaining parameters can be determined by simultaneous solutions of Equations D.5 - D.10. Thus, Equation 7 gives:

$$x_2 = (M_7 - M_1)(1 - x_3) \qquad \text{D.11}$$

By substitution of x_2 into Equation D.5, x_3 can be obtained, therefore:

$$x_3 = \frac{M_5+M_7-2M_1}{M_7-M_5} \qquad \text{D.12}$$

Equations D.11 and D.12 give:

$$x_2 = \frac{2(M_1-M_5)(M_7-M_1)}{(M_7-M_5)} \qquad \text{D.13}$$

Similarly, Equation D.8 gives:

$$x_6 = (M_8 - M_3)(1 - x_7) \qquad \text{D.14}$$

Substitution of x_6 into Equation D.6 gives:

$$x_7 = \frac{M_8+M_6-2M_3}{M_8-M_6} \qquad \text{D.15}$$

Equations D.15 and D.14 give:

$$x_6 = \frac{2(M_3-M_6)(M_8-M_3)}{M_8-M_6} \qquad \text{D.16}$$

The solution of Equations D.6 and D.10 give:

$$x_4 = (M_9-M_2)(1 - x_3x_7) \qquad \text{D.17}$$

and

$$x_8 = (M_{10}-M_4)(1 - x_3x_7) \qquad \text{D.18}$$

where,

$$x_3x_7 = \frac{(M_5+M_7-2M_1)(M_6+M_8-2M_3)}{(M_7-M_5)(M_8-M_6)} \qquad \text{D.19.}$$

Thus, with the substitution of x_1, M, x_5 and N from Equations D.1 - D.4 and x_3, x_2, from Equations D.13 and D.14 and x_7, x_6, x_4 and x_8 from Equations D.15 - D.19 into Equations 3.1-3.5. The S-parameter values, namely, S_{11}, S_{22}, S_{12} and S_{21} can be obtained.
then,

$$S_{11} = \frac{1}{M_{22}} \{1 - K(1 + d\ N_{22})\} \qquad \text{D.20}$$

$$S_{22} = \frac{1}{N_{22}} \{1 - K(1 + c\ M_{22})\} \qquad \text{D.21}$$

$$S_{12} = eK \qquad \text{D.22}$$

and

$$S_{21} = fK \qquad \text{D.23}$$

where,

$$K = \{(1 + c\,M_{22})(1 + d\,N_{22}) - ef\,M_{22}N_{22}\}^{-1} \qquad \text{D.24}$$

$$c = \frac{M_{R1}-M_{11}}{M_{21}M_{12}} \qquad \text{D.25}$$

$$d = \frac{M_{R2}-N_{11}}{N_{21}N_{12}} \qquad \text{D.26}$$

$$e = \frac{M_{T2}-N}{M_{12}N_{21}} \qquad \text{D.27}$$

and,

$$f = \frac{M_{T1}-M}{M_{21}N_{12}} \qquad \text{D.28}$$

APPENDIX E

EQUIVALENT CIRCUIT S-PARAMETERS CALCULATIONS

The purpose of this appendix is to show a derivation for the S-parameters of the equivalent circuit discussed in Chapter 3. The result is used in Chapter 6.

A two-step procedure is involved.

Step 1. The y-parameters are calculated from the equivalent circuit of Fig. 6.1. as follows.

The node current equations of Fig. 6.1 when $e_o = 0$ are:

$$(e_1-e_2)G_b + (e_1-e_3)j\omega C_{bc'} = I_1 \qquad E.1$$

$$(e_2-e_1(G_b + (e_2-0)(G_e+j\omega C_{b'e})+(e_2-e_3)j\omega C_{b'c'} = 0 \qquad E.2$$

and $$(e_3-e_1)j\omega C_{bc'}+(e_3-e_2)j\omega C_{b'c'}+(e_3-0)G_c+g_m e_2 = 0 \qquad E.3$$

Equations E.1 - E.3 can be written in convenient forms as:

$$x_1 e_1 - G_b e_2 - j\omega C_{bc'} e_3 = I_1 \qquad E.4$$

$$-G_b e_1 + x_2 e_2 - j\omega C_{b'c'} e_3 = 0 \qquad E.5$$

and $$-j\omega C_{bc'} e_1 + x_3 e_2 + x_4 e_3 = 0 \qquad E.6$$

where, $$x_1 = G_b + j\omega C_{bc'} \qquad E.7$$

$$x_2 = G_b + G_e + j\omega(C_{b'e} + C_{b'c'}) \qquad E.8$$

$$x_3 = g_m - j\omega C_{b'c'} \qquad E.9$$

$$x_4 = G_c + j\omega(C_{bc'} + C_{b'c'}) \qquad E.10$$

in which, $G_b = 1/R_{bb'}$, $G_e = 1/R_e$ and $G_c = 1/R_c$

The solution of Equations E.5 and E.6 gives e_2 and e_3 in terms of e_1 as follows:

$$e_2 = e_1 A_2/A_1 \qquad \text{E.11}$$

and

$$e_3 = -e_1 A_3/A_1 \qquad \text{E.12}$$

where, $A_1 = x_2 x_4 + j\omega C_{b'c'} x_3$ E.13

$$A_2 = G_b x_4 - \omega^2 C_{bc'} C_{b'c'} \qquad \text{E.14}$$

and $A_3 = -G_b x_3 + j\omega C_{bc'} x_2$ E.15

By definition, $y_{11} = \left.\frac{I_1}{e_1}\right|_{e_o=0}$ and, $y_{21} = \left.\frac{I_o}{e_1}\right|_{e_o=0}$. Hence the substitution of Equations E.11 and E.12 into Equation E.4 gives:

$$x_1 e_1 - G_b(e_1 A_2/A_1) - j\omega C_{bc'}(-e_1 A_3/A_1) = I_1 \qquad \text{E.16}$$

Equation E.16 yields:

$$\frac{e_1}{A_1}\{x_1 A_1 - G_b A_2 + j\omega C_{bc'} A_3\} = I_1 \qquad \text{E.17}$$

Hence,

$$y_{11} = \left.\frac{I_1}{e_1}\right|_{e_o=0} = \frac{1}{A_1}(x_1 A_1 - G_b A_2 - j\omega C_{bc'} A_3) \qquad \text{E.18}$$

In Fig. 6.1, I_o is given by,

$$I_o\big|_{e_o=0} = -e_3 G_c \qquad \text{E.19}$$

The substitution of Equation E.12 into Equation E.19 gives:

$$I_o = -G_c A_3 e_1/A_1 \qquad \text{E.20}$$

Therefore, $Y_{21} = \left.\frac{I_o}{e_1}\right|_{e_o=0} = -G_c A_3/A_1$ E.21

Now, y_{11} and y_{21} are found. Next, is to calculate y_{22} and y_{12}. These calculations are as follows.

The Node current equations for Fig. 6.1 when $e_1 = 0$ are:

$$(e_o-0)G_s+(e_o-e_3)G_c = I_o \qquad \text{E.22}$$

$$(e_3-e_o)G_c+(e_3-e_2)j\omega C_{b'c'}+(e_3-0)j\omega C_{bc'}+g_m e_2 = 0 \qquad \text{E.23}$$

$$(e_2-0)(G_b+G_e+j\omega C_{b'e})+(e_2-e_3)j\omega C_{b'c'} = 0 \qquad \text{E.24}$$

where G_s is the admittance of the series branch of C_o and R_s at the output of Fig. 6.1. and it is given by Equation 6.14.

Collecting Equations E.22 - E.24 terms give:

$$(G_s + G_c)e_o - G_c e_3 = I_o \qquad \text{E.25}$$

$$-G_c e_o+(g_m-j\omega C_{b'c'})e_2+(G_c+j\omega(C_{bc'}+C_{b'c'}))e_3 = 0 \qquad \text{E.26}$$

$$(G_b+G_e+j\omega(C_{b'e}+C_{b'c'}))e_2-j\omega C_{b'c'}e_3 = 0 \qquad \text{E.27}$$

Equations E.25 - E.27 can be also written in convenient forms as:

$$x_5 e_o - G_c e_3 = I_o \qquad \text{E.28}$$

$$-G_c e_o+x_3 e_2+x_2+x_4 e_3 = 0 \qquad \text{E.29}$$

$$x_2 e_2-j\omega C_{b'c'}e_3 = 0 \qquad \text{E.30}$$

where, $x_5 = G_s + G_c$ E.31

and, x_2, x_3 and x_4 are given by Equations E.8 - E.10 respectively.

Also by definition, $y_{22} = \left.\frac{I_o}{e_o}\right|_{e_1=0}$ and $y_{12} = \left.\frac{I_1}{e_o}\right|_{e_1=0}$

Similarly, the solution of Equations E.29 and E.30 gives, e_2 and e_3 in terms of e_o as follows:

$$e_2 = -j\omega C_{b'c'}G_c e_o/A_1 \qquad \text{E.32}$$

and $$e_3 = G_c x_2 e_o/A_1 \qquad \text{E.33}$$

The substitution of Equations E.32 and E.33 into Equation E.28 gives:

$$x_5 e_o - G_c(x_2 G_c e_o/A_1) = I_o \qquad \text{E.34}$$

Equations E.34 yields:

$$I_o = \frac{e_o}{e_1}(x_5 A_1 - x_2 G_c^2) \qquad \text{E.35}$$

Hence,

$$y_{22} = \left.\frac{I_o}{e_o}\right|_{e_1=0} = (x_5 A_1 - x_2 G_c^2)/A_1 \qquad \text{E.36}$$

In Fig. 6.1, I_1 is given by:

$$I_1\Big|_{e_1=0} = -(G_b e_2 + j\omega C_{bc'} e_3) \qquad \text{E.37}$$

The substitution of Equations E.32 and E.33 into Equation E.37 gives:

$$I_1\Big|_{e_1=0} = -\frac{e_o G_c}{A_1}\{j\omega C_{bc'} x_2 + j\omega C_{b'c'} G_b\} \qquad \text{E.38}$$

$$\text{Therefore, } y_{12} = \left.\frac{I_1}{e_o}\right|_{e_1=0} = -\frac{G_c}{A_1} A_5 \qquad \text{E.39}$$

$$\text{in which, } A_5 = j\omega(x_2 C_{bc'} + G_b C_{b'c'}) \qquad \text{E.40}$$

The y_{11}, y_{21}, y_{22} and y_{12}-parameters of the equivalent circuit of Fig. 6.1 are now given by Equations E.18, E.21, E.36 and E.39 respectively.

Step 2. Knowing the y-parameters, the S-parameters can be found. The following transformation equations are used in calculating the equivalent circuit s-parameters. First, the y-parameters have to be normalized to a 50-Ω as shown in the following transformation equation.[6(1,6)]

$$S_{11} = ((1-y'_{11})(1+y'_{22}) + y'_{21}\ y'_{12})A'_2 \qquad \text{E.41}$$

$$S_{21} = -2y'_{21}/A'_2 \qquad \text{E.42}$$

$$S_{12} = -2y'_{12}/A'_2 \qquad \text{E.43}$$

$$S_{22} = (1+y'_{11})(1-y'_{22}) + y'_{21}\ y'_{12})/A'_2 \qquad \text{E.44}$$

where, $A'_2 = (1+y'_{11})(1 + y'_{22})-y'_{21}y'_{12}$ E.45

$$y'_{11} = 50 \cdot y_{11} \qquad \text{E.46}$$

$$y'_{21} = 50 \cdot y_{21} \qquad \text{E.47}$$

$$y'_{12} = 50 \cdot y_{12} \qquad \text{E.48}$$

and $y'_{22} = 50 \cdot y_{22}$ E.49

APPENDIX F

S-PARAMETERS AND OBJECTIVE FUNCTION ANALYSIS SUBROUTINE

```
      EXTERNAL FUNCT
      DIMENSION X(7), DX(7), BL(7), BU(7)
      COMPLEX SC(4,8), SM(4,8)
      COMMON XY(7), Y(7), W(4),SC,SM, STARIF,NF,FINC
      N = 7
      EPS = 1.0E-9
      ITNO = 500
      FREQ = 20
      READ(5,1) X
1     FORMAT(7E10.4)
      READ (5,2) DX
2     FORMAT(7E10,4)
      READ (5.3)BL
3     FORMAT(7E10.4)
      READ(5,4) BU
4     FORMAT(7E10.4)
      READ (5,5) (W(I),I=1,4)
5     FORMAT (4F10.2)
      READ (5,6) STARIF,NF,FINC
6     FORMAT (3E10.4)
      DO 8 J=1,NF
      READ(5,7) (SM(I,J), I=1,4)
7     FORMAT(8F10.4)
8     CONTINUE
      CALL OPTHKJ(FUNCT,N,X,DX,BL,BU,EPS,ITNO,FREQ,Y,FY)
      WRITE(6,9) Y(I), I=1,7)
9     FORMAT(7E10.4)
      WRITE (6,10) FY
10    FORMAT (E10.5)
      DO 12 J=1,NF
12    WRITE (6.2) (SC(I,J),I=1,4)
20    FORMAT (8E10.4)
      STOP
      END
```

```
      FUNCTION FUNCT(X)
      REAL X(1)
      COMPLEX SC(4,8),SM(4,8),X1,X2,X3,X4,X5,A1,A2,A3,A4,A5,Y11,
      Y12,Y21,Y22
      COMMON XY(7),Y(7),W(4),SC,SM,STARTF,N.F,FINC
      F=0.0
      FUNCT=0.0
      F2 = 0.0
      J=1
      STARTQ=STARTF
   10 F=STARTQ
      OMEGA=6.283185308*F
      X1=X(1)+CMPLX(0,OMEGA)*X(5)*1.0E-9
      X2=X(1)+(7)+CMPLX(0,OMEGA)*(X(4)+0.36E-3-X(5))*1.0E-9
      X3=β0*X(7) - CMPLX(0,OMEGA)*1.0E-9*(0.36E-3 - X(5))
      X4=X(2) + CMPLX(0,OMEGA)*0.36E-12
      X5=X(2)+CMPLX(0,OMEGA)*X(6)*1.0E-9/(1.0+COMPLX(0,OMEGA)*X(6)
     1*1.0E-9/X(3))
      A1=X2*X4+CMPLX(0.OMEGA)*X3*1.0E-9*(0.36E-3-X(5))
      A2=X(1)*X4-OMEGA**2*X(5)*1.0E-18*(0.36E-3-X(5))
      A3=CMPLX(0,OMEGA)*X(5)*X2*1.0E-9 -X(1)*X3
      A5=CMPLX(0,OMEGA)*X(5)*X2*1.0E-9 + CMPLX(0,OMEGA)*X(1)
     1 *1.0E-9*(0.36E-3-X(5))
      Y11=(X1*A1-X(1)*A2-CMPLX(0,OMEGA)*X(5)*A3*1.0E-9)/A1
      Y21 = -X(2)*A3/A1
      Y12 = - X(2)*A5/A1
      Y22 = (X5*A1 - X(2)**2*X2)A1
      A4=(1.0 + 50.0*Y11)*(1.0 + 50.0*Y22) - 2500.*Y21*Y12
      SC(1,J) = ((1.0-50.*Y11)*(1.0+50.*Y22) + 2500.*Y12*Y21)/A4
      SC(2,J) = - 100.*Y21/A4
      SC(3,J) = - 100.0*Y12/A4
      SC(4,J) = ((1.0+50.*Y11)*(1.0-50.*Y22) + 2500.*Y12*Y21)/A4
      DO 100 I=1,4
  100 F2=F2+W(I)*((REAL(Sc(I,J) - SM(I,J)))**2 + (AIMAG(SC(I,J)
     1  -SM(I,J)))**2)
      FUNCT=FUNCT+F2
      J=J+1
      STARTQ=STARTQ+FINC
      IF(J.LE.NF) GO TO 10
      RETURN
      END
```

In which, $X(1) = 1/R_{bb'}$

$X(2) = 1/R_c$

$X(3) = 1/R_s$

$X(4) = C_{be'}$

$X(5) = C_{bc'}$

$X(6) = C_o$

$X(7) = 1/R_e$

X = Initial component values

DX = Step sizes

BL = Low bounds

BU = Upper bounds

SM = Measured values (s-parameters)

SC = Calculated values (s-parameters)

and 0.36E-12 is the output capacitance C_{ob}(measured value).

β_o is the d.c. current gain. W(I) weighting factors.