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Performance Enhancements in Scaled Strained SiGe pMOSFETs with $HfSiO_x$/TiSiN Gate Stacks

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Abstract - The short channel performance of compressively strained $Si_{0.77}Ge_{0.23}$ pMOSFETs with $HfSiO_x$/TiSiN gate stacks has been characterized alongside unstrained Si pMOSFETs. The strained SiGe devices exhibit 80% mobility enhancement compared with Si control devices at an effective vertical field of 1 $MV.cm^{-1}$. For the first time, the on-state drain current enhancement of intrinsic strained SiGe devices is shown to be approximately constant with scaling. Intrinsic strained SiGe devices with 100 nm gate lengths exhibit 75% enhancement in maximum transconductance compared with Si controls, using only ~20% Ge (~0.8% strain). The origin of the loss in performance enhancement commonly observed in strained SiGe devices at short gate lengths is examined and found to be dominated by reduced boron diffusivity and increased parasitic series resistance in the compressively strained SiGe devices compared with the silicon controls. The effective channel length was extracted from I-V measurements and was found to be 40% smaller in 100 nm silicon control devices than in SiGe devices having the same lithographic gate lengths, in good agreement with the metallurgical channel length predicted by TCAD process simulations. Self-heating due to the low thermal conductivity of SiGe is shown to have a negligible effect on the scaled device performance. These findings demonstrate that the significant on-state performance gains of strained SiGe pMOSFETs compared with bulk Si devices observed at long channel lengths are also obtainable in scaled devices if dopant diffusion, silicidation and contact modules can be optimized for SiGe.

***Index Terms* - dopant diffusion, high k, metal gates, mobility, parasitic resistance, scaling, strained SiGe.**

I. INTRODUCTION

Low spin-orbit split-off energy (44 meV) from the valence band degeneracy and a large hole effective mass compared with electrons contribute to the low hole mobility and poor performance of pMOSFETs in bulk silicon compared with nMOSFETs. Using strained silicon-germanium (SiGe) as the channel material has potential as a major performance booster in pMOSFET devices due to increased hole mobility compared with bulk silicon [1]. However, the scalability of the performance gains induced by compressive strain has remained a concern. SiGe pMOSFETs were investigated in [2] and it was shown that the enhancement in maximum transconductance, g_m^{MAX}, compared with bulk Si devices reduced from 50% in 2 µm gate length devices to 10% in 0.25 µm gate length devices. A similar observation was reported in [3], in which strain induced enhancement in g_m^{MAX} was shown to reduce from 75% for 10 µm gate length devices to 10% for 0.15 µm gate length devices. Strained $Si_{0.7}Ge_{0.3}$ pMOSFETs reported in [4] showed that the strain induced enhancement in g_m^{MAX} reduced from 30% for 1.3 µm gate length MOSFETs to 15% for 0.3 µm gate length MOSFETs. Strained $Si_{0.72}Ge_{0.28}$ pMOSFETs with 85% hole mobility enhancement were reported in [5] but the drain current enhancement compared with Si controls was only 55% for 10 µm devices and reduced to 15% for 70 nm devices.

Realizing high performance SiGe pMOSFETs is particularly important in advanced technologies which use heavy halo doping to control short channel effects and high k/metal gate stacks to control gate leakage. Both heavy doping and high-k gate dielectrics reduce channel mobility compared with that obtainable in the conventional Si/SiO_2 system, therefore incorporating high mobility channel materials such as SiGe becomes even more essential. Devices combining high k gate dielectrics, metal gates and compressively strained SiGe have consequently received a lot of attention [6-14]. In [8], compressively strained $Si_{0.8}Ge_{0.2}$ pMOSFETs with HfO_2 gate dielectrics exhibited 65% peak hole mobility enhancement

compared with the Si control devices but 180 nm gate length devices had only 35% drive current enhancement. Compressively strained $Si_{0.72}Ge_{0.28}$ pMOSFETs with HfO_2 gate dielectrics and TiN gates in [10] exhibited 65% mobility enhancement compared with bulk Si controls having the same gate stack. However the 100% enhancement in drain current observed for 1 μm devices was suppressed for 55 nm gate length devices when devices were compared at the same gate overdrive voltage. If compressively strained SiGe channels are to be deployed in deep submicrometer CMOS technology, the reduced gains in drain current and transconductance due to scaling have to be understood and minimized. In this work, the scalability of compressively strained SiGe pMOSFETs is investigated for devices fabricated with $HfSiO_x$/TiSiN gate stacks.

II. EPITAXIAL GROWTH AND DEVICE FABRICATION

Compressively strained SiGe was selectively grown on device active areas with a final thickness of approximately 40 nm. An average Ge composition of 23% in the strained SiGe layer was determined by secondary ion mass spectroscopy (SIMS). Nitrided interfacial layers were used to improve interfacial properties between the high-k gate dielectric and the MOSFET channel [11, 15-18]. The interfacial layers were formed by rapid thermal oxidation followed by nitridation which resulted in SiON on the silicon control wafer and Si(Ge)ON on the SiGe wafer. The $HfSiO_x$ gate dielectric was deposited by atomic layer deposition. Using gate-bulk capacitance measurements on 100 μm^2 area MOS capacitors, the effective oxide thickness was found to be ~1.2 nm for both the Si and SiGe wafers. The effectiveness of the interfacial layer adopted in the devices under investigation was evaluated by calculating the interface trap density (D_{it}) using the conductance method [19]. The gate-capacitance and gate-conductance characteristics were measured on 100 μm^2 MOS capacitors. The mid-gap D_{it} for the Si control and strained SiGe wafer was 8 x 10^{11} $cm^{-2}eV^{-1}$ and 3 x 10^{12} $cm^{-2}eV^{-1}$,

respectively. The higher D_{it} in the SiGe devices was expected due to the presence of Ge at the channel/dielectric interface [20, 21]. Nevertheless, both values are comparable with D_{it} values from similar structures reported in literature [11, 22]. The TiSiN gates were formed by sputtering. After gate definition, source-drain implants were formed by a 10 keV B implantation with a dose of $1.4x10^{15}$ cm^{-2}. Halo doping at 45° was performed using As implantation at an energy of 50 keV and dose of $6x10^{13}$ cm^{-2}. Sidewall spacers were subsequently formed followed by deep source-drain implants using a 20 keV B implantation at a dose of $4x10^{15}$ cm^{-2}. Dopant activation was carried out by rapid thermal annealing at 1000 °C. A self aligned Ni silicidation process was performed by depositing Ni and annealing at 1000 °C for 30 seconds. A standard back-end process completed the fabrication. Fig. 1 shows a TEM image of the processed device and the SiGe channel.

III. RESULTS AND DISCUSSION

The uniformity of the Si control and SiGe wafers was evaluated by measuring all 1 µm gate length devices on both wafers. Fig. 2 shows the distribution of device performance on the wafers in terms of maximum transconductance (g_m^{MAX}) measured at 1 V drain voltage (V_{DS}). The results are identical for smaller drain biases. The Si control and SiGe wafers exhibited standard deviations of 3% and 5% of the median values of g_m^{MAX}. Subsequent analysis was performed on median performing dies for each wafer which are labeled in Fig. 2.

The split CV technique with series resistance correction was used to extract the effective mobility of the strained SiGe and Si control devices. The inversion charge density was calculated from the integration of the gate-channel capacitance whereas the depletion charge density was calculated from the integration of the gate-bulk capacitance [19]. The effective mobility was extracted from 1 µm gate length devices. Fig. 3 shows 80% effective hole mobility (μ_{EFF}) enhancement for the strained SiGe devices compared with the Si control

device at an effective vertical field (E_{EFF}) of 1 MV.cm^{-1}. The mobility enhancement due to compressive strain overcomes any mobility reduction caused by the imperfect SiGe/Si(Ge)ON/$HfSiO_x$ interface in the strained SiGe device [8, 23-25] and there is 60% enhancement in the effective hole mobility compared with the universal mobility curve (Fig. 3) at an E_{EFF} of 1 MV.cm^{-1}. The hole mobility enhancement is greater than that reported in [13] and [8] where $Si_{0.7}Ge_{0.3}$ and $Si_{0.8}Ge_{0.2}$ devices demonstrated 20% hole mobility enhancement compared with the universal mobility curve at an E_{EFF} of 1 MV.cm^{-1}. The mobility enhancement in our work is also comparable with that reported in [10] for devices having higher Ge contents, 28%. Carrier mobilities are affected by the quality of the interface between the gate dielectric and the channel, especially for high-k/metal gate systems. It is known that μ_{EFF} can be reduced by increased scattering due to the interaction between the mobile carriers in the channel and charged traps at the interface as well as surface roughness scattering at high vertical fields. Surface passivation and preparation techniques such as nitridation prior to dielectric deposition have been shown to improve μ_{EFF} in high-k/metal gate devices by reducing D_{it} [11, 15-18]. The inclusion of a nitridation step prior to ALD deposition of the high-k has minimized the impact of D_{it} on mobility for the devices, as confirmed by D_{it} measurements on the devices.

Fig. 4 shows the drain current (I_{DS}) as a function of the drain voltage (V_{DS}) for 1 µm and 100 nm gate length pMOSFETs at a gate overdrive voltage, V_{GS}-V_{TH} of 0.5 V and 1.0 V. V_{GS} is the gate voltage and V_{TH} is the threshold voltage. The gate voltage overdrive is used for I_{DS} comparison because of the lower V_{TH} in the strained SiGe devices as a result of the reduced bandgap due to the valence band offset [14]. The V_{TH} difference between the devices reduces from 290 mV at L_G=1 µm to 50 mV at L_G=100 nm. This is because V_{TH} roll-off is evident in the Si control devices ($V_{TH(1\ \mu m)}$=0.71 V and $V_{TH(100\ nm)}$=0.51 V) whereas V_{TH} remains stable with L_G in the strained SiGe devices ($V_{TH(1\ \mu m)}$=0.42 V and $V_{TH(100\ nm)}$=0.45 V).

The output characteristics in Fig. 4 show that the 75% enhancement in the saturation drain current for the 1 μm gate length strained SiGe device compared with the Si control is lost for the 100 nm devices. Fig. 5 shows the gate transfer characteristics for the same devices. The subthreshold slopes are 75 mV/dec (Si) and 83 mV/dec (SiGe) for 1 μm gate length devices and 95 mV/dec (Si) and 83 mV/dec (SiGe) for 100 nm gate length devices.

Fig. 6 shows the variation in drain induced barrier lowering (DIBL) with gate length for the strained SiGe and Si control devices. DIBL is 10 mV/V for both Si and strained SiGe 1 μm devices but increases more rapidly in the scaled Si devices than in the SiGe devices. For 100 nm gate length devices DIBL is 70 mV/V for the Si pMOSFETs and 45 mV/V for the SiGe pMOSFETs.

The maximum transconductance measured in the SiGe and Si control devices at a drain voltage of 1 V are presented for a range of lithographic gate lengths (L_G) in Fig. 7a. Performance enhancements for the SiGe devices are presented in Fig. 7b and are shown to reach 80% compared with Si controls. In agreement with other reports [2-5, 11], Fig. 7b shows that the enhancements in g_m^{MAX} for the strained SiGe devices decrease as the lithographic gate length is reduced. For L_G below 250 nm no enhancement is evident and for 100 nm devices, the Si control outperforms the SiGe devices by approximately 20%.

To enable strained SiGe pMOSFETs to assist in advanced technology nodes, the on-state performance loss at short lithographic gate lengths must be understood. In this work, boron is used for the source/drain implants. B is known to have suppressed diffusivity in compressively strained SiGe compared with bulk Si [26-28], therefore boron will diffuse by different amounts into the channel region of bulk Si and strained SiGe devices. Consequently the effective channel length should be used in comparisons of scaled Si and SiGe devices. The effective channel length, (L_{EFF}), is an electrical parameter that defines the lateral distance between the source and the drain over which the channel resistivity modulated by the gate-

voltage whereas the lithographic gate length (L_G) is a physical parameter defined on the mask layout. The diffusion length *(ΔL)* is defined as the difference between the lithographic gate length and the effective channel length. The “shift and ratio” method was used to extract the effective channel length using 1 μm and 0.1 μm gate lengths as the long and short channel MOSFET, respectively [29]. The effective channel lengths were found to be approximately 65 nm (Si) and 90 nm (SiGe).

The difference in effective channel length of the Si and SiGe devices was also confirmed using the TCAD process simulator TSUPREM4. The boron implant dose, implant energies, arsenic halo implant energies, tilt angles, doses and activation anneal temperature-time cycles used in the TSUPREM process simulation were identical to those used in device fabrication. Diffusivity data was taken from [28] and the strain was calculated as $(1-a_{Ge}/a_{Si})x$, where a_{Ge} is the lattice constant of Ge, a_{Si} is the lattice constant of Si and x is the Ge mole fraction in the SiGe layer. Raman spectroscopy showed that the average compressive strain in the SiGe channel was about 0.8%, close to the theoretical strain value for 20% Ge. The diffusivity of boron in compressively strained $Si_{0.77}Ge_{0.23}$ is $\sim 0.2D_O$ where D_O is the diffusivity of boron in unstrained Si [28]. As a first approximation, taking $\Delta L \sim \sqrt{Dt}$ where D is the dopant diffusivity and t is the diffusion time, boron will diffuse approximately 55% less in the SiGe devices compared with the Si control devices. This difference in diffusion leads to a shorter metallurgical channel length L_{MET} in the bulk Si devices. The metallurgical channel length (L_{MET}) is defined as the lateral distance between the source and drain over which the substrate arsenic doping is higher than the source/drain doping. L_{MET} correlates with the effective channel length and the lithographic gate length. Fig. 8a shows a 2D profile of B doping contours in a simulated 100 nm processed device whereas Fig. 8b shows the lateral cross section of B between the source and drain 5 nm below the MOSFET surface. The metallurgical channel length is extracted at this position and is found to be approximately 30

nm for the Si device and 40 nm for the SiGe device. The effective channel lengths extracted from I-V data are larger than the metallurgical channel length predicted by the TCAD simulation. This is expected because the lateral straggle of the junction implants [29] and non-abrupt source-drain junction profiles effectively shortens the chemical length between the source and drain. For an ideal junction profile (infinitely abrupt with no lateral straggle), L_{MET} is larger than L_{EFF} due to sheet resistivity only being modulated by the gate voltage inside the metallurgical channel. However for a non-abrupt junction profile, there is a fraction of the channel with the junction implant straggle in accumulation thereby causing L_{EFF} to be larger than L_{MET}.

Both experimental methods and TCAD process simulations show a shorter effective and metallurgical channel length for the Si devices compared with the SiGe devices due to reduced boron diffusivity in compressively strained SiGe. These results also explain the increased V_{TH} roll-off for the Si devices and Fig. 6, where DIBL is seen to be lower in the short channel strained SiGe devices than in the Si control devices. Since DIBL relates to the L_{EFF} through a negative exponential, a small difference in L_{EFF} causes a significant difference in DIBL [30]. The lower DIBL for the strained SiGe devices therefore correlates as expected with the stable V_{TH} roll-off, which is usually due to DIBL. Hence, the reduced B diffusion in compressively strained SiGe results in longer effective channel lengths and better electrostatic integrity.

The g_m^{MAX} data in Fig. 7 are re-evaluated using the effective channel length calculated by the "shift and ratio" method and are shown in Fig. 9. Using the effective channel length demonstrates that strained SiGe devices can offer performance enhancements for all channel lengths greater than 150 nm. In contrast when the devices were analyzed in terms of their lithographic gate length (Fig. 7) performance gains only appeared possible in SiGe devices if the gate length exceeded 175 nm.

Fig. 9 indicates that for effective channel lengths below 150 nm, the Si control devices still out-perform the strained SiGe devices. The series resistance (R_{SD}) was also extracted using the "shift and ratio" method [29] and was found to be 60% higher in the SiGe devices compared with the Si control devices (80 Ω compared with 50 Ω). The higher R_{SD} in the strained SiGe devices was confirmed by silicide sheet resistance (R_{SH}) measurements on test structures, which showed that R_{SH} was approximately 100% higher in the SiGe devices (8.2 Ω/□ in SiGe and 4.2 Ω/□ in Si control). Since the silicide anneal process was optimized for bulk Si and the pMOSFETs have a 40 nm SiGe surface channel layer, high resistance nickel germanosilicides will have formed due to the presence of Ge [31-33]. It was shown in [32] that R_{SH} of Ni silicided $Si_{0.75}Ge_{0.25}$ was 3 Ω/□ at 500 °C but increased abruptly at anneal temperatures above 800 °C. This increase was attributed to the segregation of Ge at the grain boundaries of nickel germanosilicide during the interfacial reactions between nickel and SiGe. In [33], nickel silicided $Si_{0.7}Ge_{0.3}$ and $Si_{0.8}Ge_{0.2}$ films showed a minimum R_{SH} of 3.9 Ω/□ and 3.5 Ω/□ respectively at 400 °C. These values are 50% lower than R_{SH} on the SiGe wafers in this study, and this is likely to be due to the higher annealing temperature used (1000 °C). However under the appropriate annealing conditions, NiSiGe can offer improved R_{SH}. NiSiGe can also improve contact resistance because of the reduced barrier height and higher boron activation compared with NiSi [34, 35].

Process optimization of the silicidation temperature-time cycle for SiGe alloys can prevent the formation of such high resistance films, therefore it is valid to investigate the intrinsic device performance without parasitic resistances. The intrinsic drain current was calculated by correcting for the series resistance using the formula

$$I_{DSO} = I_{DS}\left(1 - I_{DS}\, {R_{SD}}/{V_{DS}}\right)^{-1} \quad (1)$$

where I_{DSO} is the intrinsic drain current. Equation (1) is derived from the strong inversion MOSFET square law model taking series source/drain resistance into account [19, 36-38]. The resulting intrinsic maximum transconductance data are shown in Fig. 10a. The on-state performance of the strained SiGe devices is now found to be improved compared with the Si control devices down to effective gate lengths of 100 nm. The difference between the intrinsic and measured transconductances increases as the gate length reduces due to the increasing impact of series parasitic resistance, which becomes a larger proportion of the total channel resistance in scaled geometries. Comparing the intrinsic g_m^{MAX} in Fig. 10a with the measured g_m^{MAX} in Fig. 9a shows that approximately 50% of g_m^{MAX} is lost in scaled SiGe pMOSFETs. Fig. 10b shows that the intrinsic enhancement in g_m^{MAX} of the SiGe devices reaches 80% at long channel lengths and reduces by only 15% as the effective channel length is scaled from 1 μm to 100 nm. The 65% enhancement in g_m^{MAX} at short channel lengths is the highest reported for SiGe devices using low Ge contents (~20%) to date. In [10], no enhancement in the drain current compared with the Si control devices was reported for 55 nm strained $Si_{0.72}Ge_{0.28}$ pMOSFETs and only 15% enhancement in linear transconductance compared with the Si control was achieved in 130 nm $Si_{0.68}Ge_{0.32}$ pMOSFETs [3]. In [39], 50 nm gate length strained $Si_{0.65}Ge_{0.35}$ pMOSFETs exhibited 35% drive current enhancement compared with Si controls and in [5] 13% drive current enhancement compared with Si controls was reported in 50 nm strained $Si_{0.72}Ge_{0.28}$ devices. Our new results suggest that significantly larger performance gains in strained SiGe pMOSFETs are realizable in deep submicrometer CMOS technology nodes than previously demonstrated if processing is optimized to take account of modified dopant diffusion and parasitic series resistance in the SiGe material system.

Fig. 10(b) shows that the intrinsic performance enhancement of short channel strained SiGe pMOSFETs compared with bulk Si is 15% lower than observed in long channel devices.

This reduction may be due self heating arising from the low thermal conductivity of SiGe [40], strain loss with scaling or the increased impact of halo doping on mobility at short gate lengths. One of the dominating factors behind the compromised drain current and transconductance enhancement in scaled strained Si devices fabricated on relaxed SiGe virtual substrates is self heating [41]. The devices in this study comprise of a 40 nm SiGe surface layer on a Si substrate rather than a thin Si layer on a thick SiGe layer, thus the impact of self heating is expected to be considerably lower. AC drain conductance measurements which remove self-heating effects [42] were carried out on 100 nm strained SiGe devices. Fig. 11 shows there is an increase in drain current compared with DC conditions of only ~3% for the SiGe device when measurements were carried out at 10 MHz. Therefore self heating is not a performance limiting mechanism in scaled strained SiGe pMOSFET devices.

Potential variations in mobility with gate length may also impact performance gains in scaled devices. Unintentional fluctuations in channel strain with gate length scaling due to stresses induced during epitaxial growth, from the silicide and trench isolation may counteract the intentional channel strain. Strain relaxation in the SiGe layers at the source/drain regions may also result from defects caused by ion implantation. These defects together with the loss of strain can cause additional carrier scattering thereby contributing to mobility reduction. Electrically, the impact of these defects and strain relaxation will be manifested as increased series resistance and its relative impact would also increase as the gate length is scaled. Since strain relaxation at nanoscale dimensions cannot be characterised electrically, it is not possible to accurately separate its effect from that of increased series resistance due to silicide sheet resistance. At present the limited availability of nanoscale strain characterization techniques prevents a full understanding of the impact of various strain contributions in deep submicrometer CMOS.

IV. SUMMARY

The scalability of high performance strained SiGe pMOSFETs with $HfSiO_x$/TiSiN gate stacks has been examined. The intrinsic performance of short channel SiGe devices has been shown to exceed that of co-processed Si controls by as much as 65% in 100 nm devices, whereas extrinsic gains are completely diminished for drawn gate lengths below 175 nm. Performance enhancements exceeding 70% in both long and short channel devices are the highest reported gains to date compared with bulk Si using just 20% Ge in the channel region. The dominating factors behind the compromised performance gains observed in the measured short channel strained SiGe devices are found to be differences in the effective channel length due to strain altered dopant diffusion and increased parasitic series resistance. Self heating due to the low thermal conductivity of SiGe was analyzed and shown to have a smaller impact on scaled device performance (~3%). The intrinsic potential of the devices was assessed by correcting for the differing effective channel lengths and source-drain series resistance. After correction, 65% of the long-channel strain induced performance enhancement was maintained at scaled geometries. The work presented suggests a major underestimation of the potential of SiGe for advanced technology nodes. The effective channel length of SiGe devices was 40% larger than that of the Si controls for 100 nm lithographic gate lengths due to suppressed boron diffusivity from the source/drain regions in SiGe. This difference was confirmed by TCAD simulations that showed a 30% increase in the metallurgical channel length for 100 nm SiGe devices. The source-drain series resistance was also 70% higher in the SiGe devices due to silicidation being optimized for bulk Si. While electrical results are convincing, direct comparisons between L_{EFF} and R_{SD} matched strained SiGe and Si pMOSFETs would be even more reliable in evaluating the scalability of the performance enhancements in compressively strained SiGe devices. However, this comparison is only possible if the respective thermal

processes of the devices are customized. The work shows that strained SiGe pMOSFETs are scalable and are suitable for deep submicrometer CMOS technology nodes if series resistance and dopant diffusion can be controlled.

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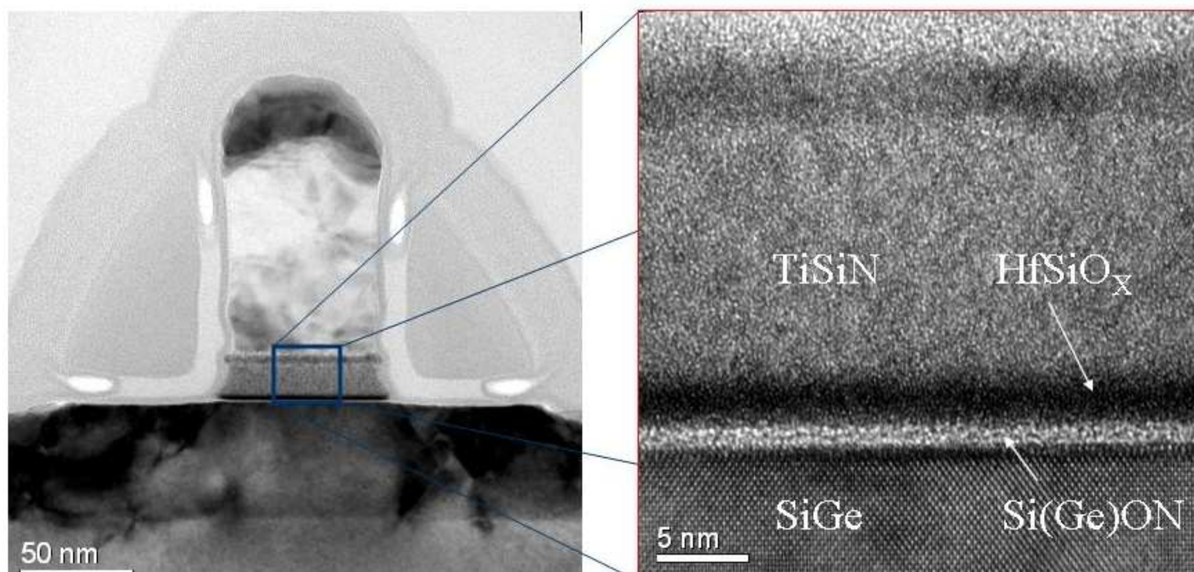

Fig. 1. TEM images of a 70 nm strained SiGe device and the corresponding gate stack/channel.

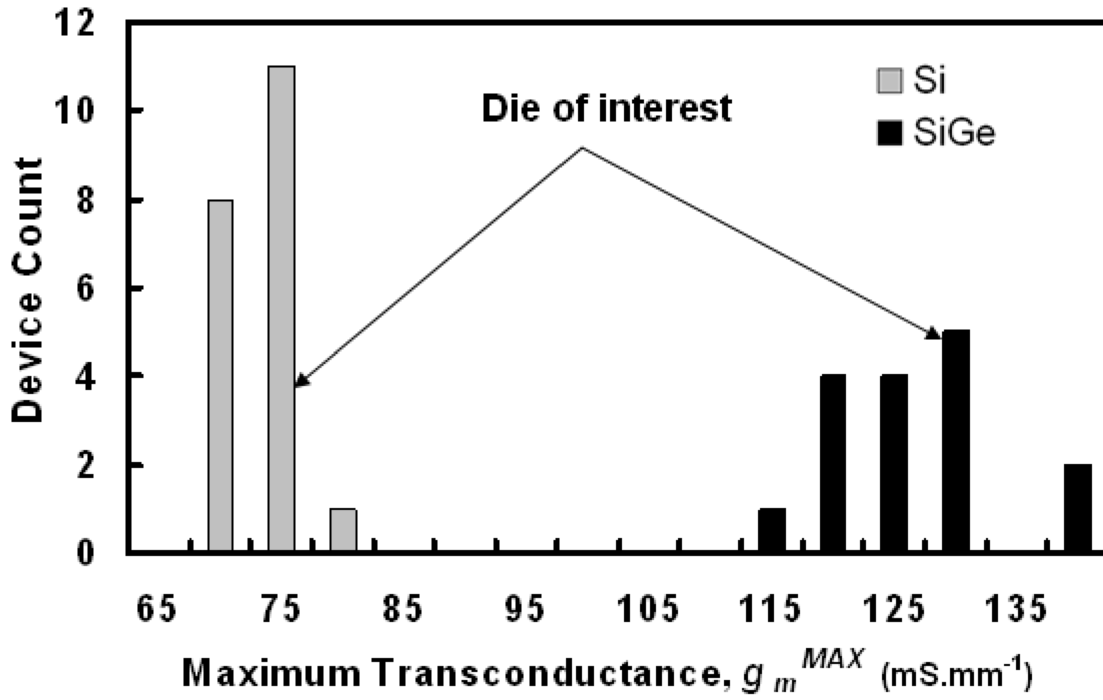

Fig. 2. The distribution of device performance for the 1 μm gate length strained SiGe and the Si control pMOSFETs. g_m^{MAX} is measured at a drain voltage of 1 V.

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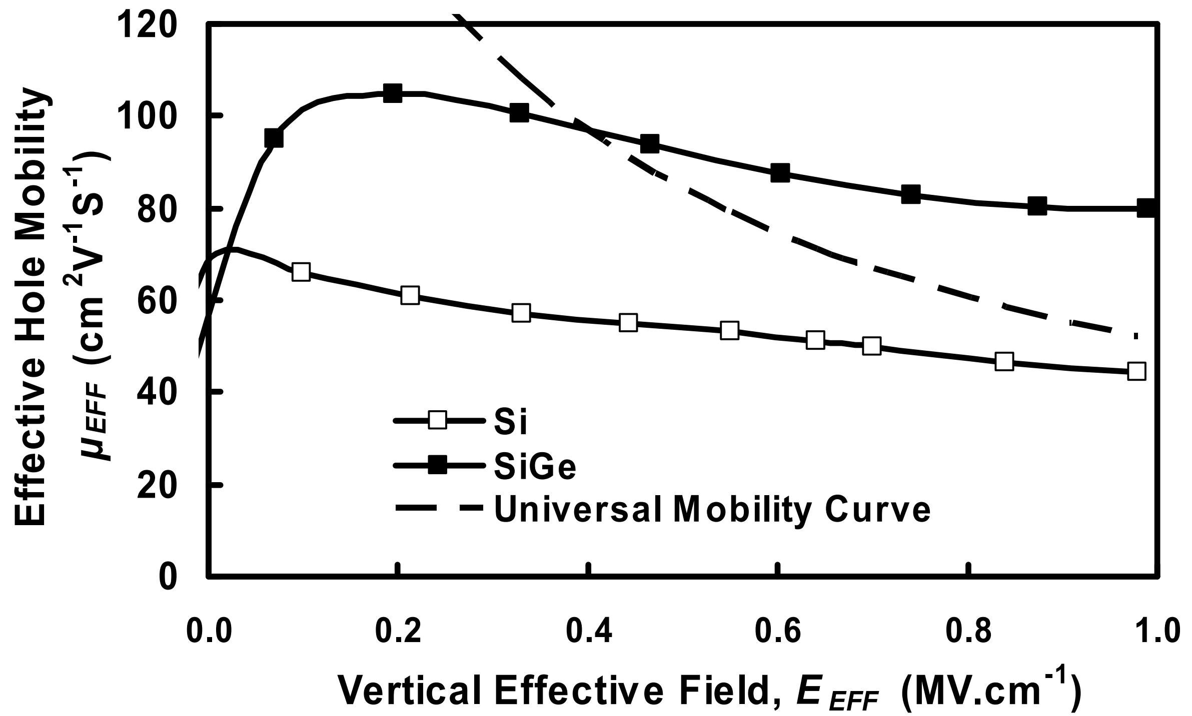

Fig. 3. Effective hole mobility determined by gate-channel capacitances and drain conductance measurements. Hole mobility is increased by 80% compared with the Si control device and by 60% compared with the universal mobility curve at 1 $MV.cm^{-1}$.

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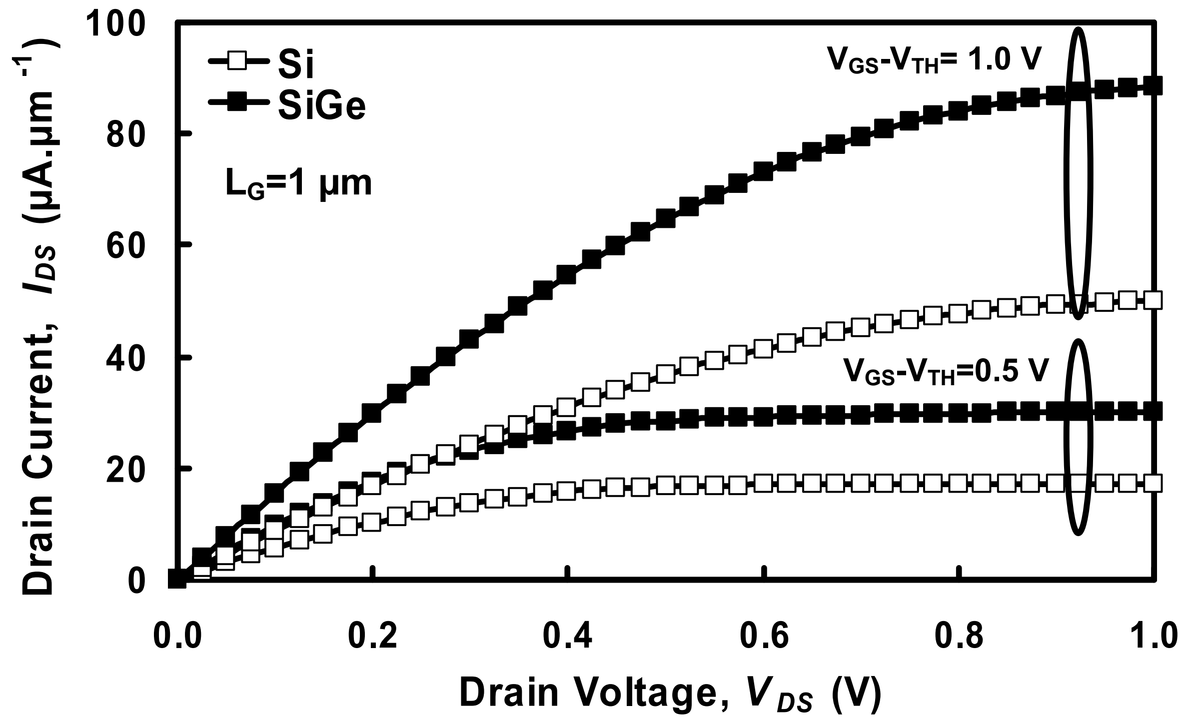

Fig. 4a. Drain current output characteristics of 1 μm pMOSFETs measured at a gate overdrive voltage (V_{GS}-V_{TH}) of 0.5 V and 1.0 V. At a drain voltage of 1 V for both gate overdrives, the drain current is increased by 75% for the strained SiGe pMOSFETs compared with the Si control.

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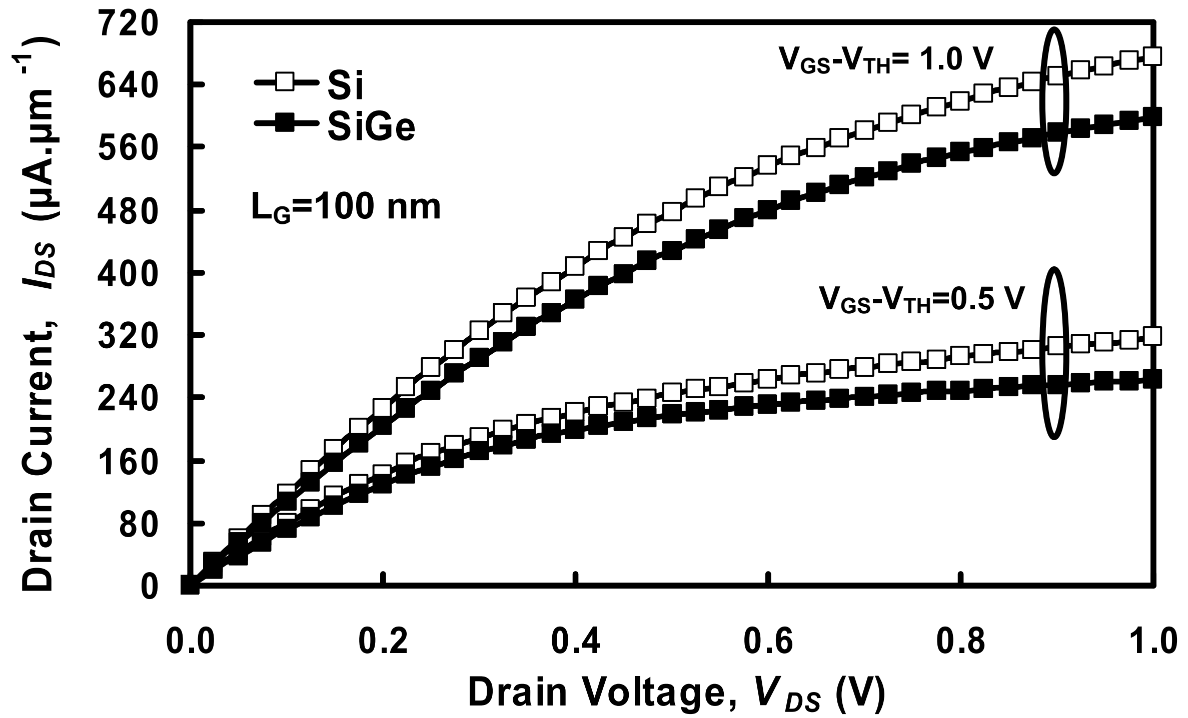

Fig. 4b. Drain current output characteristics of 100 nm pMOSFETs measured at a gate overdrive voltage (V_{GS}-V_{TH}) of 0.5 V and 1.0 V. The Si control exhibits higher drain current than the strained SiGe device.

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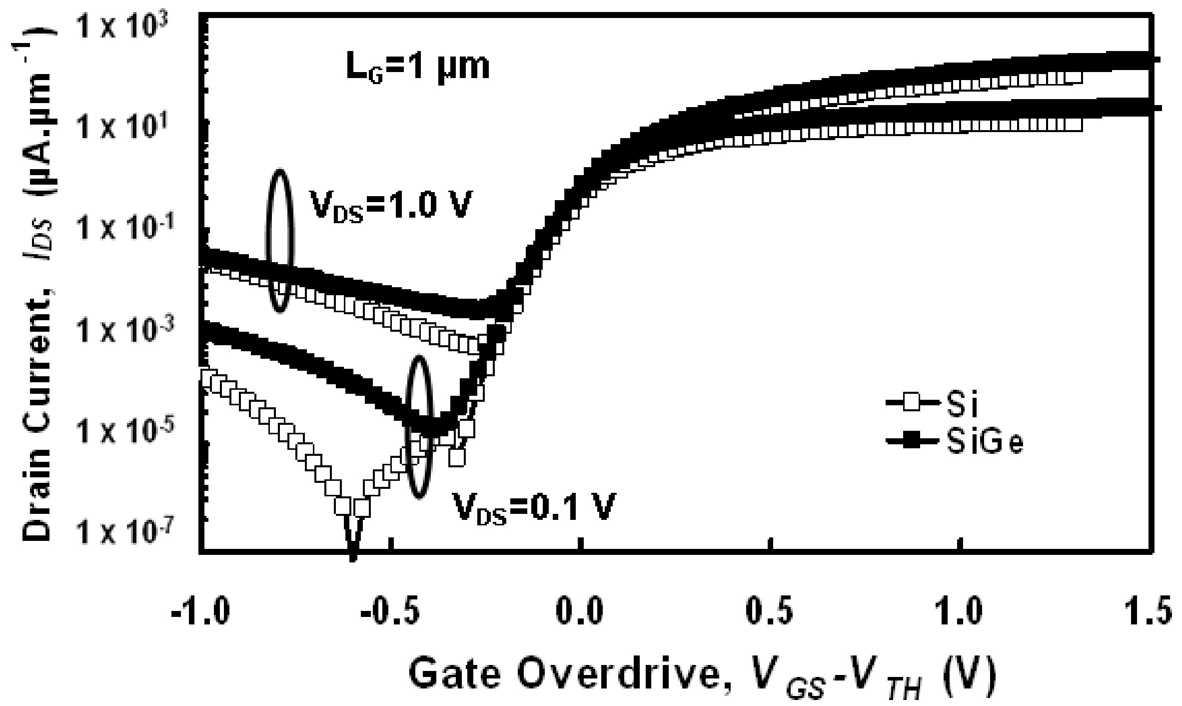

Fig. 5a. The gate transfer characteristics of 1 μm pMOSFETs measured at drain voltages of 0.1 V and 1.0 V. The subthreshold slopes are 75 mV/dec (Si) and 83 mV/dec (SiGe).

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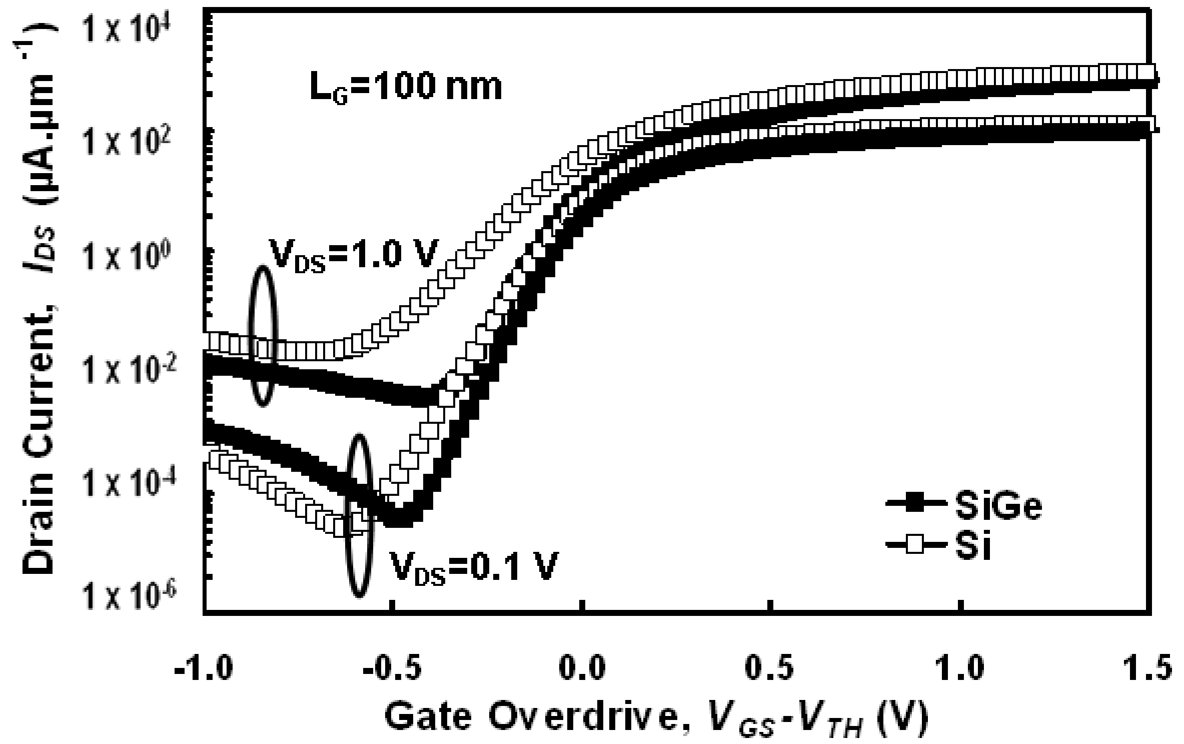

Fig. 5b. The gate transfer characteristics of 100 nm pMOSFETs measured at drain voltages of 0.1 V and 1.0 V. The subthreshold slopes are 95 mV/dec (Si) and 83 mV/dec (SiGe).

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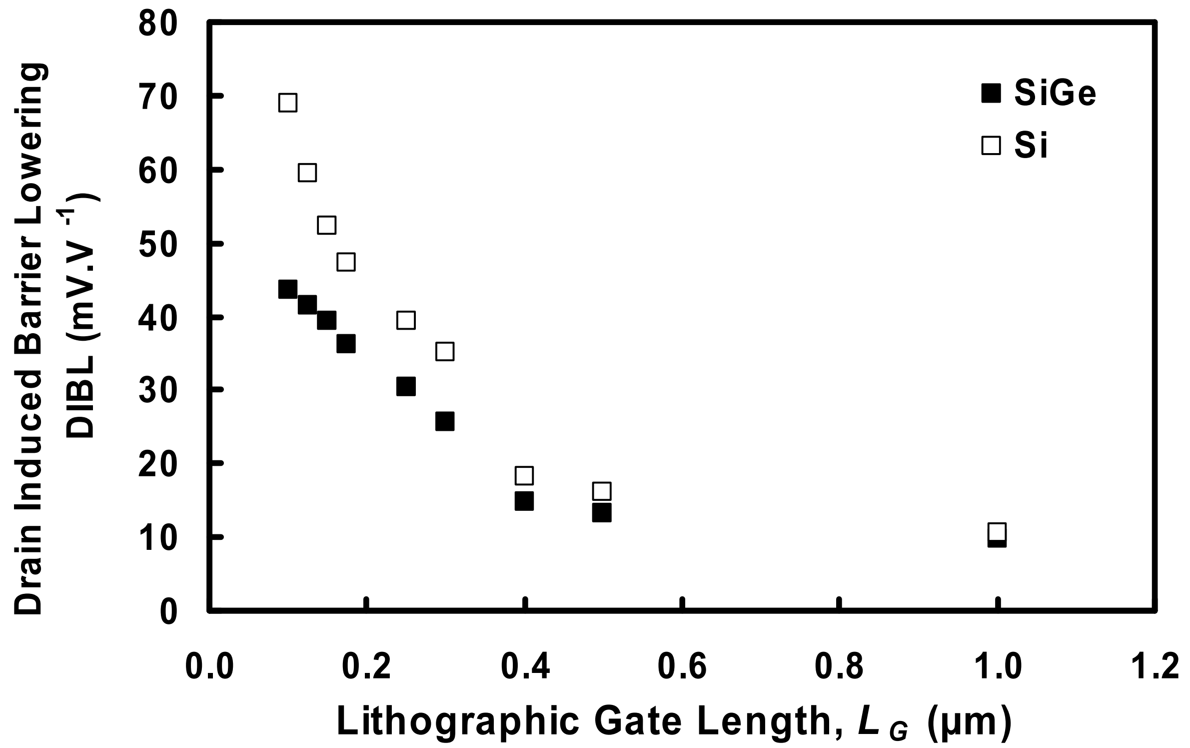

Fig. 6. Variation in DIBL with gate length for the strained SiGe and Si control devices. Strained SiGe devices exhibit better electrostatic integrity in the form of lower DIBL.

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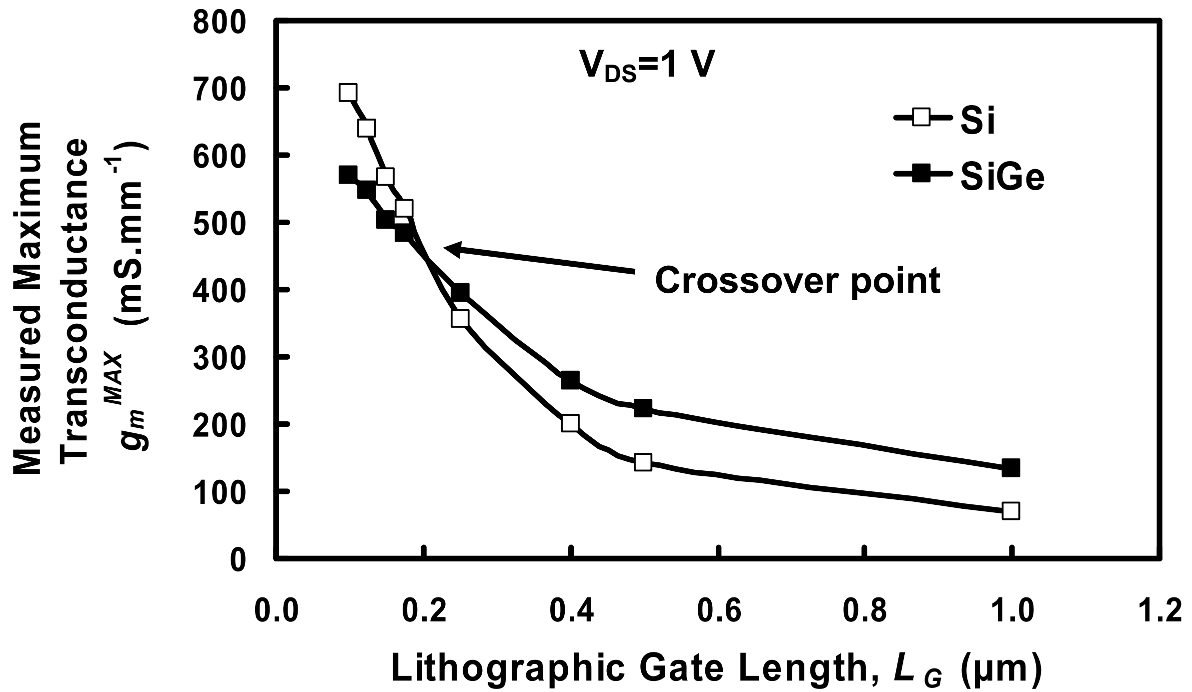

Fig. 7a. Variation in measured maximum transconductance with lithographic gate length for the Si and SiGe devices. The performance gains of the SiGe devices compared with the Si devices evident at large lithographic gate lengths are diminished at gate lengths below ~ 200 nm.

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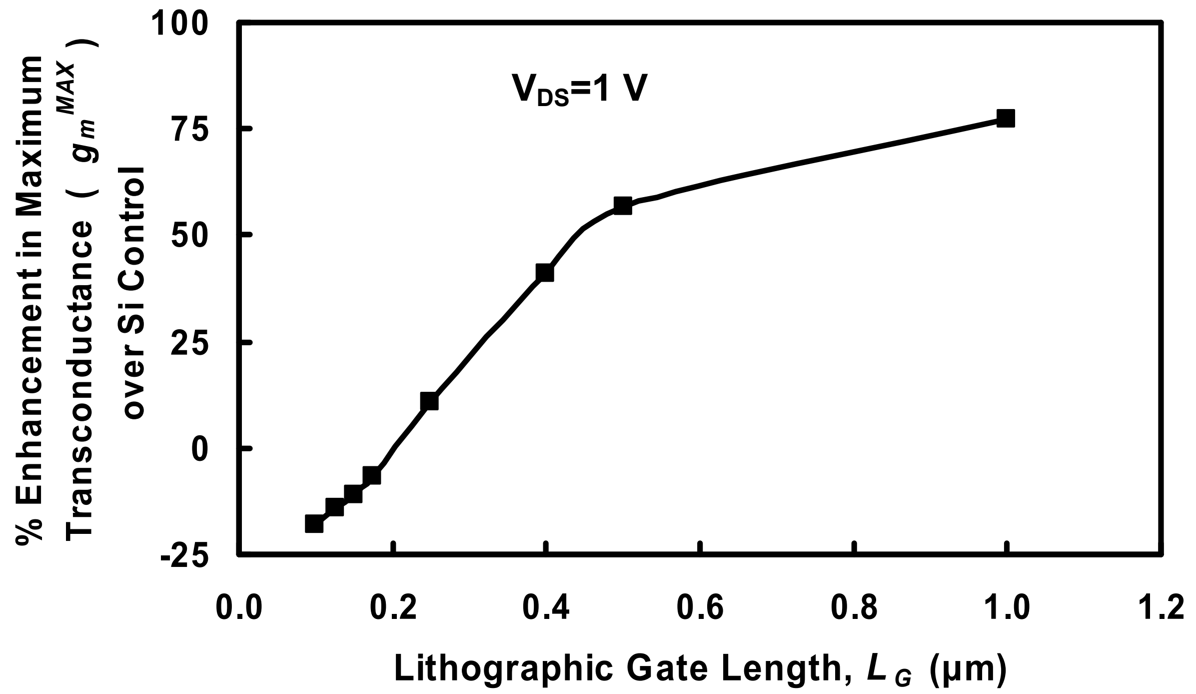

Fig. 7b. The percentage enhancement in maximum transconductance of the SiGe devices compared with the Si controls. Devices were measured at a drain voltage of 1 V.

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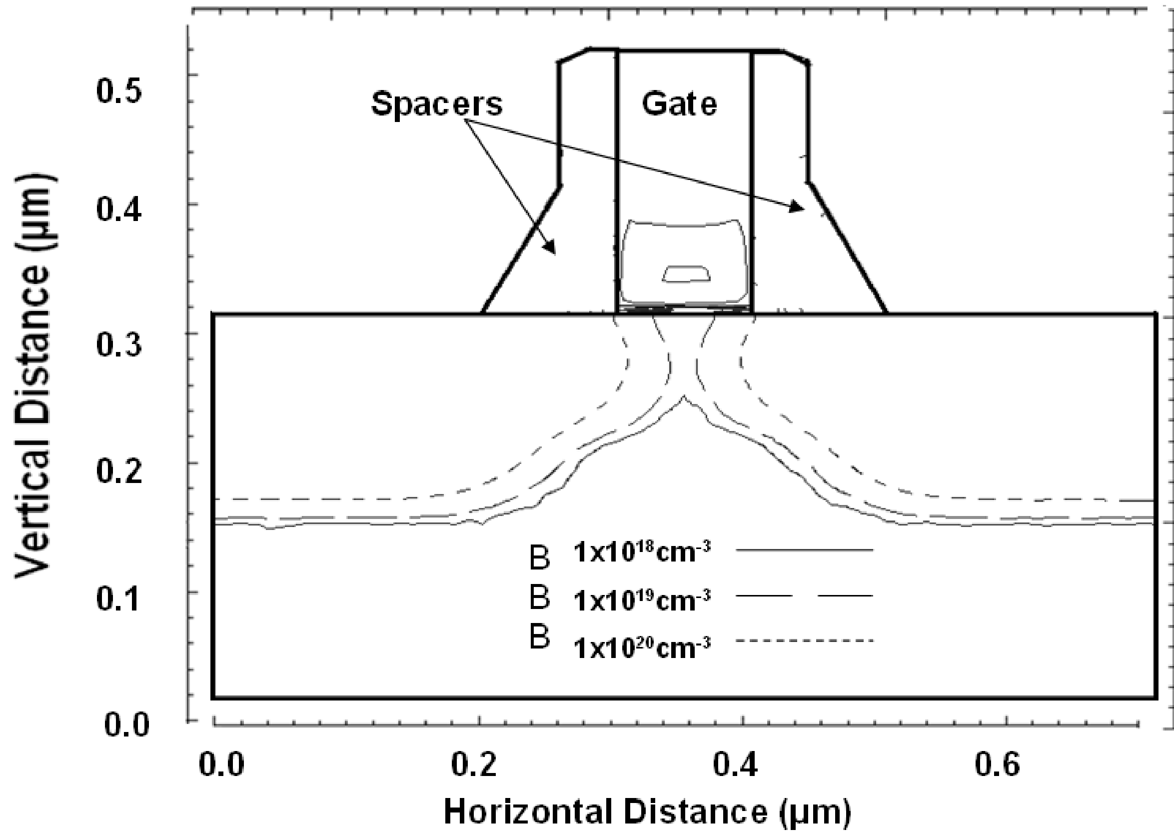

Fig. 8a. The processed device simulated in TSUPREM4 using the actual process parameters. The solid and dashed lines represent contours of boron concentration after annealing and show the extent of boron diffusion.

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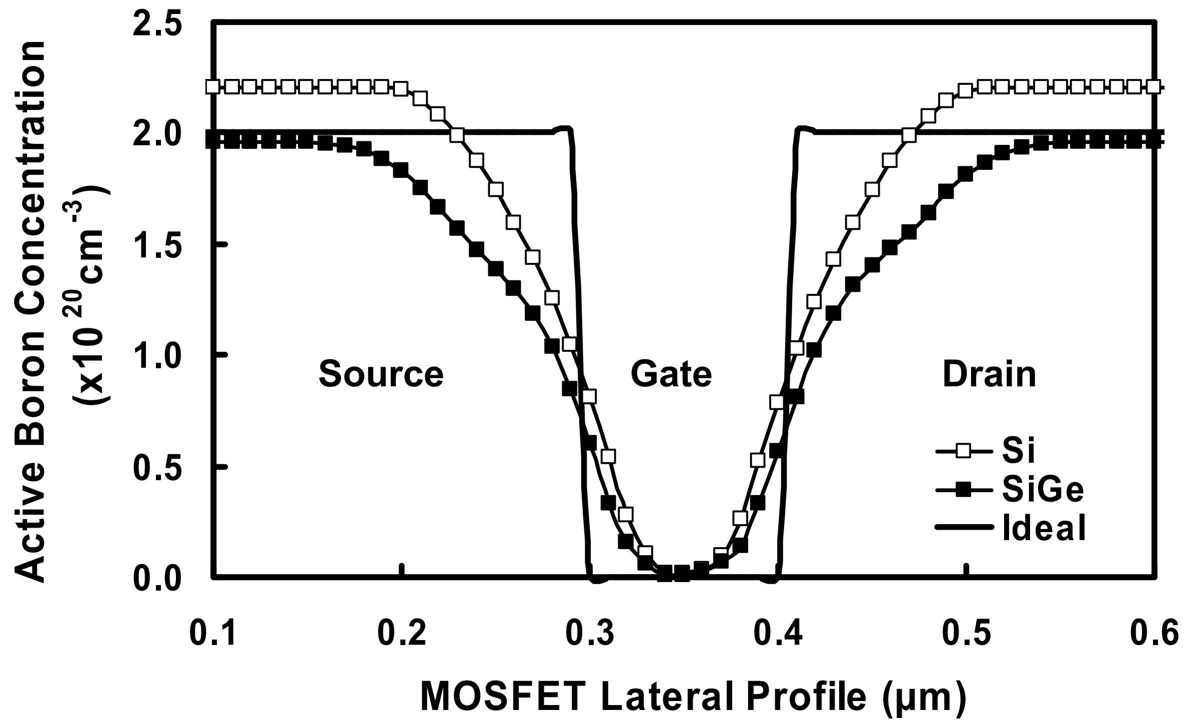

Fig. 8b. Simulated boron concentration 5 nm below the 100 nm MOSFET surface. The boron concentration in the channel is lower in the SiGe devices due to retarded boron diffusivity in compressively strained SiGe compared with bulk Si.

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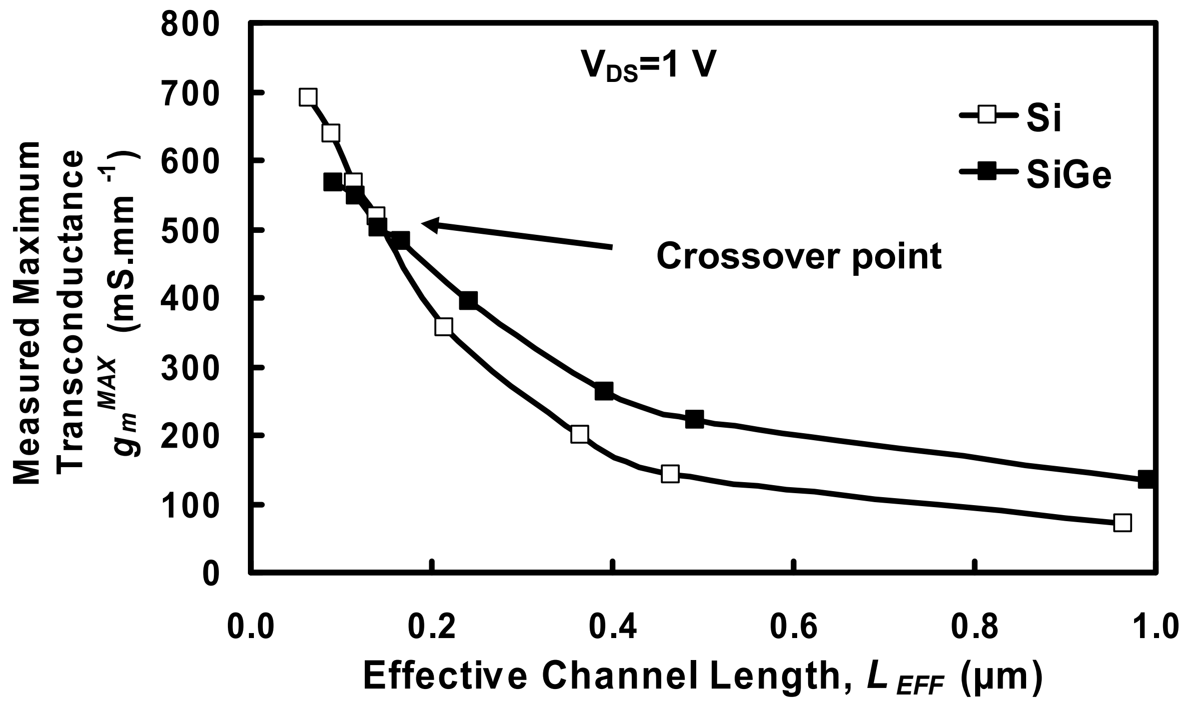

Fig. 9a. Variation in the measured maximum transconductance with effective channel length for Si and SiGe devices. Performance gains are demonstrated down to smaller gate lengths when the effective channel length is used instead of the lithographic gate length. The devices were measured at a drain voltage of 1 V.

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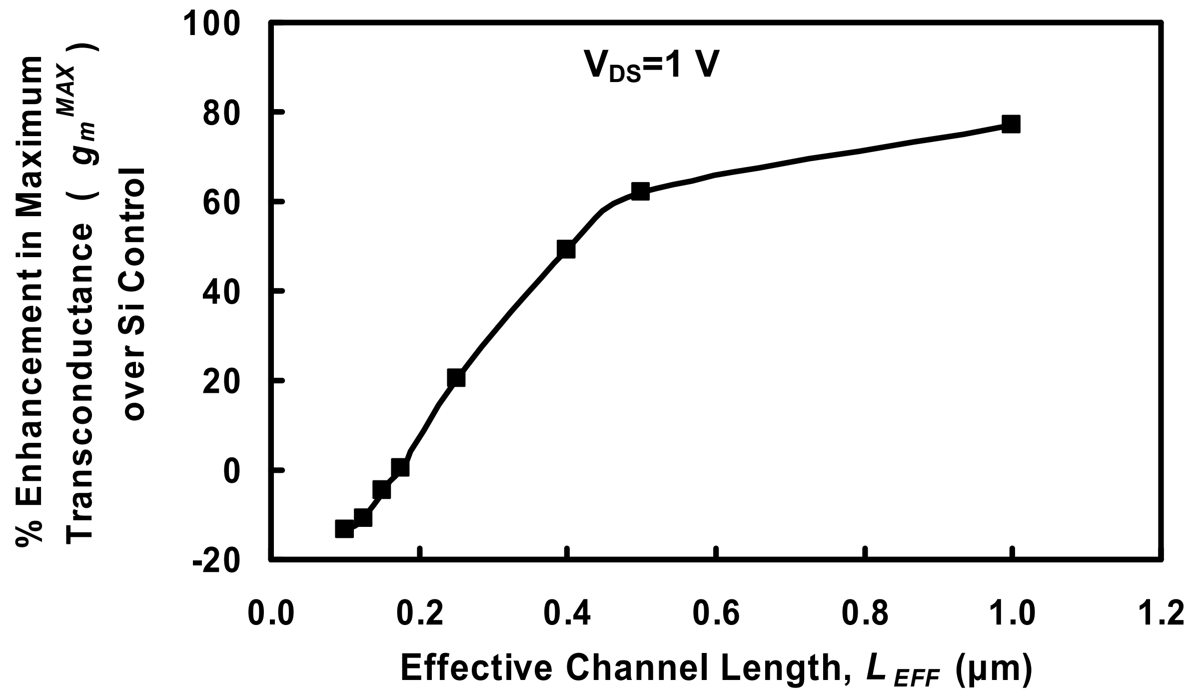

Fig. 9b. Percentage enhancement in measured maximum transconductance for the strained Si devices compared with the Si control devices for a range of effective channel lengths. The devices were measured at a drain voltage of 1 V.

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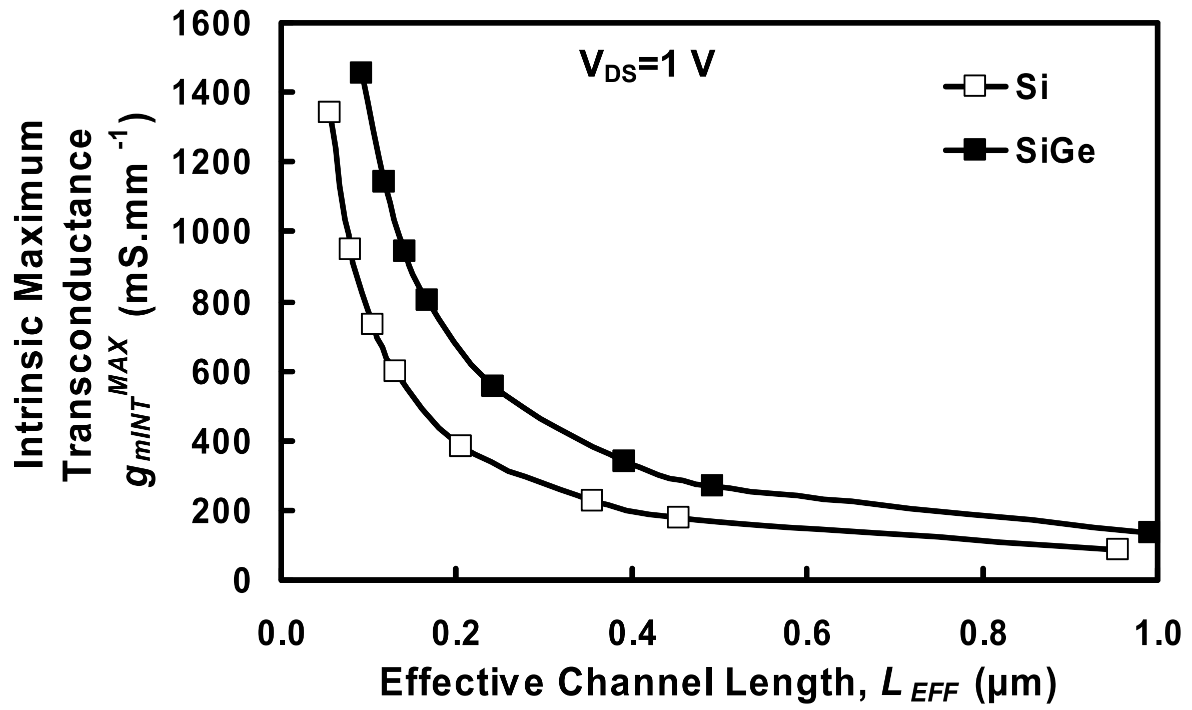

Fig. 10a. Variation in intrinsic maximum transconductance with effective channel length for the Si and SiGe pMOSFETs.

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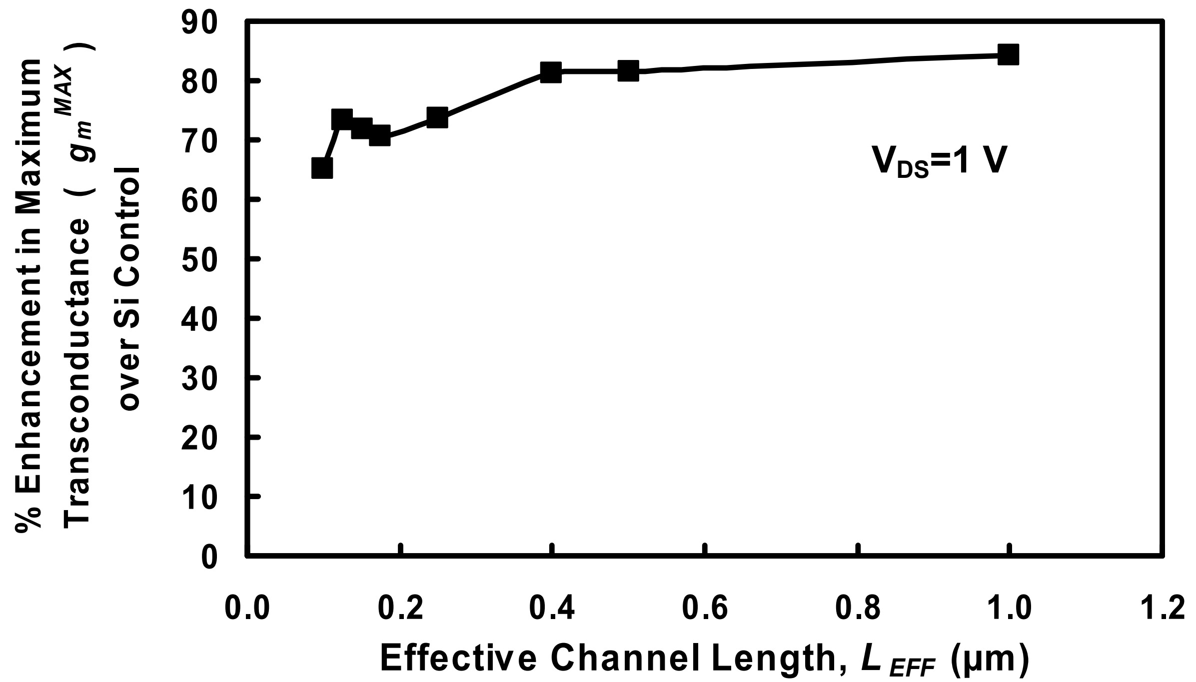

Fig. 10b. Percentage enhancement in the intrinsic maximum transconductance for the strained SiGe devices compared with the Si control devices. The enhancement of the intrinsic SiGe device is only reduced by ~ 15% as the effective channel length is scale from 1 µm to 100 nm.

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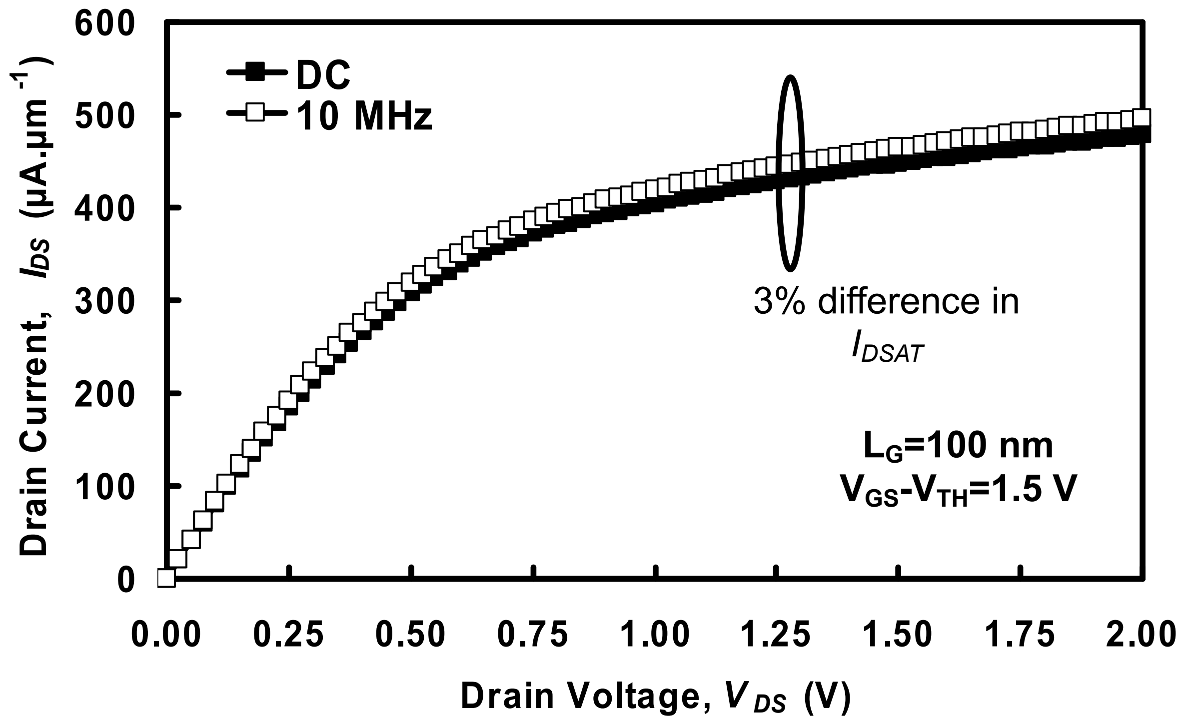

Fig.11. Output characteristics for 100 nm gate length SiGe pMOSFETs measured at a gate overdrive voltage (V_{GS}-V_{TH}) = 1.5 V at DC and 10 MHz. The 3% difference in drain current measured at a drain voltage of 1.5 V using DC and 10 MHz conditions is proportional to device self heating and is considered negligible in the strained SiGe devices.

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