The Impact of Repetitive Unclamped Inductive Switching on the Electrical Parameters of Low Voltage Trench Power nMOSFETs

Olayiwola Alatise, Ian Kennedy, George Petkos, Keith Heppenstall, Khalid Khan, Jim Parkin, Adrian Koh and Philip Rutter

Innovation Research and Development

NXP Semiconductors

Hazel Grove, Stockport, SK7 5BJ, UK

E-mail: olayiwola.alatise@nxp.com

Tel: +44-(0)161-957-5570

Fax: + 44-(0)161-957-5399

***Abstract* – The impact of hot-carrier injection (HCI) due to repetitive unclamped inductive switching (UIS) on the electrical performance of low voltage trench power nMOSFETs is assessed. Trench power nMOSFETs in TO-220 packages have been fabricated and subjected to over 100 million cycles of repetitive UIS with different avalanche currents (I_{AV}) at a mounting base temperature (T_{MB}) of 150 °C. Impact ionization during avalanche conduction in the channel causes hot-hole injection into the gate dielectric which results in a reduction of the threshold voltage (V_{GSTX}) as the number of avalanche cycles (N) increase. The experimental data reveals a power law relationship between the change in threshold voltage (ΔV_{GSTX}) and N. The results show that the power law pre-factor is directly proportional to the avalanche current. After 100 million cycles, it was observed that the power law pre-factor increased by 30% when the I_{AV} was increased from 160 A to 225 A thereby approximating a linear relationship. Stable subthreshold slope with avalanche cycling indicates that interface trap generation is not an active degradation mechanism. The impact of the cell pitch on avalanche ruggedness is also investigated by testing 2.5 µm and 4 µm cell pitch 30 V rated MOSFETs. Measurements showed that the power law pre-factor reduced by 40% when the cell pitch was reduced by 37.5%. The improved V_{GSTX} stability with the smaller cell pitch MOSFETs is attributed to a lower avalanche current per unit cell resulting in less hot-hole injection and hence, smaller V_{GSTX} shift. The 2.5 µm cell pitch MOSFETs also show 25% improved on-state resistance (R_{DSON}), better R_{DSON} stability and 20% less subthreshold slope compared to the 4 µm cell pitch MOSFETs however with 100% higher initial I_{DSS} and less I_{DSS} stability with avalanche cycling. These results are important for manufacturers of automotive MOSFETs where multiple avalanche occurrences over the lifetime of the MOSFET are expected.**

Index Terms: Avalanche current, Avalanche duration, Power MOSFET, Unclamped Inductive Switching

I. INTRODUCTION

MOSFETs in automotive systems can be subjected to events of unclamped inductive switching (UIS) over the lifetime of their application [1, 2]. UIS occurs when the MOSFET is connected to some kind of inductance (lumped element or parasitic) and there is a rapid change in current [2, 3]. Since the inductor is charged up (energy is stored in the magnetic fields of the inductor) when the current is flowing and the current in the inductor cannot change instantaneously, the inductor dissipates its stored energy into the MOSFET. If the inductive energy is sufficiently high, the MOSFET will be driven into avalanche with the source-drain voltage (V_{DS}) rising to its breakdown value (B_{VDSS}) and an avalanche current (I_{AV}) will flow through the MOSFET [4-6]. The MOSFET therefore experiences thermal shock as power (I_{AV}·B_{VDSS}) is dissipated through it. The resulting rise in junction temperature (T_J) of the MOSFET will depend on the transient thermal impedance (Z_{TH}) of the MOSFET as well as the magnitude of the inductance (L), the MOSFET's B_{VDSS} and the I_{AV} [5]. An example of such an application is the anti-lock braking system which is comprised of a low-side power MOSFET switch that connects the brake pump to the battery and is switched by a pressure control system connected to the gate [7]. Every time the MOSFET is switched on and the brake pump is connected to the battery, energy is stored in the inductors of the brake pump. When the MOSFET is switched off, the energy in the brake pump is dissipated through the MOSFET by driving it into avalanche. In the operating life of the vehicle's automotive system, this avalanche event can occur over 50 million times [7].

Two failure mechanisms have been identified in MOSFET failure under a single pulse of UIS [8]. The first failure mechanism is the activation of the parasitic bipolar in the MOSFET which results in localized thermal runaway and the thermal destruction of the device. For the parasitic bipolar to be activated, the conditions of forward biased emitter-base (source-body) and reverse biased base-collector (body-drain) junctions must be fulfilled. This

failure mechanism is associated with avalanche pulses with high current densities. In this case, there must be sufficient internal resistance in the body of the MOSFET to cause a voltage drop that exceeds the source-body junction potential [2, 5]. Since the turn-on voltage of a forward biased *pn* junction exhibits a negative temperature coefficient, the likelihood of parasitic bipolar failure increases with temperature. The second failure mechanism is related to the rise of the MOSFET's junction temperature. As the temperature of the semiconductor increases, the intrinsic carrier concentration increases as a result of the reduced energy bandgap. The temperature at which the intrinsic carrier concentration is equal to the background doping is the intrinsic temperature limit of the semiconductor. If the temperature rise resulting from the avalanche pulse exceeds this intrinsic temperature limit, the MOSFET will be thermally destroyed. This failure mechanism is associated with high avalanche currents as well as long avalanche durations (large inductances).

For applications that are avalanched repetitively as part of the application requirement, power MOSFET manufacturers usually ensure that the avalanche power densities and durations are within the safe operating area (SOA) of the MOSFET [2, 3, 9, 10]. The MOSFET SOA is the range of avalanche power densities and durations that the device can sustain without destruction. However, in repetitive avalanche applications, other potential failure mechanisms are introduced as avalanche pulses, although within the MOSFET SOA, repetitively dissipate power through the MOSFET. Hot-carrier injection (HCI) into the gate dielectric is a well known short-channel effect in deep submicrometer complementary metal oxide on semiconductor (CMOS) technology [11, 12] as well as power MOSFETs [13-15]. HCI has become a major reliability concern in short channel CMOS devices since terminal voltages have not scaled as rapidly as the MOSFET's lateral dimensions. As a consequence, there has been an increase in the internal electric fields between the terminals of the MOSFET [16]. These high electric fields energize the carriers sufficiently to scale the silicon/oxide

energy barrier and generate oxide trapped charges as well as interface trap charges [17]. Impact ionization (through which avalanche conduction is enabled) generates electron-hole pairs in the channel which become hot carriers that can be injected into the gate dielectric [14]. Depending on the gate voltage, the hot carriers can either be electrons or holes. Also, the injection of the hot carriers into the gate dielectric breaks the Si-H bond thereby leaving behind interface traps which increase channel resistance through additional carrier scattering [18]. Although power MOSFETs have much thicker gate dielectrics and larger physical dimensions compared with advanced CMOS devices, the significantly higher breakdown and gate voltages means that comparable electric fields are generated in power MOSFETs. Trench MOSFETs are known to have lower on-state resistances (R_{DSON}) than vertical DMOS devices because higher channel densities can be achieved [19-24]. However, gate oxide layers thermally grown along the trench walls increase the susceptibility of the gate dielectric in trench MOSFETs to HCI since there is more exposure to the channel current compared with the gate dielectrics in vertical DMOS devices [1]. A trench power MOSFET conducting in the avalanche mode will experience high electric fields at the drain end of the channel near the bottom of the trench; hence HCI is critical for repetitively avalanched trench MOSFETs. One of the main effects of HCI is to increase or decrease the threshold voltage (V_{GSTX}) of the MOSFET depending on whether it is hot-electron or hot-hole trapping. Other effects may be the increase in subthreshold slope and R_{DSON}. Like negative-bias-temperature-instability (NBTI) in pMOSFETs, the change in these electrical parameters over the lifetime of the application poses risks against the long–term reliability of automotive power MOSFETs.

In this paper, the ruggedness performance of power MOSFETs is assessed by monitoring the change of the MOSFET's electrical parameters over tens of millions of cycles of repetitive avalanche for different avalanche currents at a mounting base temperature (T_{MB}) of 150 °C. A T_{MB} of 150 °C is chosen because power MOSFETs qualified for automotive

applications are typically operated at such temperatures [2]. Experimental data shows that the relationship between the change in threshold voltage (ΔV_{GSTX}) and the number of avalanche cycles (N) is a power law. The power law model is similar to threshold voltage shift due to hot-carrier degradation with stress time [18, 25] and NBTI. This power law model can be used to predict the V_{GSTX} reduction of the power MOSFET over its lifetime in the application. The impact of the cell pitch on the performance of power MOSFETs is also investigated by assessing the change of the electrical parameters as a function of N for 4 µm and 2.5 µm cell pitch 30 V rated MOSFETs. The next section of the paper describes the MOSFET fabrication and the repetitive avalanche experiment set-up. Section III discusses the experimental results and analysis whereas section IV concludes the paper.

II. DEVICE FABRICATION AND EXPERIMENTAL SET-UP

The MOSFETs under investigation are automotive grade devices rated to 20 V and 30 V source-drain breakdown voltage (B_{VDSS}). 21 mm^2 active area MOSFETs with 2.5 µm and 4 µm cell pitch and 76 nm thick gate oxides are fabricated with 1.5 µm trench depth and room temperature V_{GSTX} centered at 3.5 V and R_{DSON} at 2 mΩ. The cross-sectional SEM image of a typical device is shown in Fig. 1 with the source metal, trench, TEOS passivation, silicon epi-layer and polysilicon gate labeled. The MOSFETs are packaged in standard TO-220 packages comprising of 3 source wires, 1 gate wire and the drain connected to the lead frame.

A custom-built avalanche test equipment is used for repetitive ruggedness testing. Fig. 2(a) shows a picture of the equipment and Fig. 2(b) shows the circuit diagram. The test equipment is capable of testing 16 devices simultaneously. The equipment comprises of 3 high voltage charging MOSFETs (B_{VDSS} of 100 V) connected in parallel to the power supply through the avalanche inductor. The device under test (DUT) is connected in parallel with the high voltage MOSFETs to the power supply through the inductor. High voltage MOSFETs

are used to charge the inductor so as to ensure that the DUT is avalanched alone since the MOSFET with the lower B_{VDSS} always enters avalanche first i.e. an avalanche current always flow through the MOSFET with the lowest B_{VDSS}. The gate terminals of the 100 V charging MOSFETs are connected to a pulse generator whereas the gate of the DUT is grounded as shown in the circuit diagram of Fig 2(b). The period of the pulse generator is used to modulate the mounting base temperature (T_{MB}) at which the MOSFET is tested and is varied until T_{MB} is 150 °C. The magnitude of the voltage pulse is used to set the avalanche current which will be proportional to the gate drive in the charging MOSFETs whereas the avalanche inductor is used to set the avalanche duration. When the input voltage of the pulse generator is high, the 100 V MOSFETs conduct current hence charging the inductor and when it is low, the inductor dissipates the energy into the DUT which is driven into avalanche. Since the gate of the DUT is grounded, the MOSFET never switches on and hence only conducts in avalanche. Fig. 3 illustrates the typical avalanche behavior of one of the DUTs by showing I_{AV} and V_{DS} as functions of time. The amount of time the MOSFET spends in avalanche (avalanche duration, t_{AV}) will depend on the value of the inductor, the avalanche current and the B_{VDSS} rating of the DUT. The avalanche duration in Fig. 3 is approximately 100 µs, the peak I_{AV} is 160 A and the measured B_{VDSS} averages at 25 V. There is an increase in B_{VDSS} as the current reduces within the first 25 µs because of the positive temperature coefficient of B_{VDSS} due to avalanche mean-free-path reduction from increased phonon scattering caused by rising temperature.

III. RESULTS AND DISCUSSION

The two types of defects generated by HCI are interface state defects and fixed oxide charge defects [26, 27]. The electrical impact of increased interface trap generation due to repetitive avalanche would be an increase in the subthreshold slope as a result of increased

interface trap capacitance [26]. Another impact of increased interface state generation would be increased on-state resistance (R_{DSON}) as a result of reduced effective carrier mobility due to increased scattering. On the other hand, the electrical impact of increased fixed oxide charge would a shift in V_{GSTX} in a direction dependent on the polarity of the trapped charge [26]. The traps in the gate oxide could be due pre-existing traps or traps created by the charged carriers. Fig. 4(a) shows the measured V_{GSTX} as a function of the number of avalanche cycles (N) for the 4 μm cell pitch 20 V rated trench MOSFETs. The ruggedness experiment is performed on 16 MOSFETs which show an average of 21% reduction in V_{GSTX} after 100 million cycles of repetitive avalanche thereby indicating positive charge injection into the gate oxide. The V_{GSTX} reduction is due to hot-hole injection into the gate dielectric during impact ionization. Since the MOSFET gate is grounded (V_{GS}=0 V) in repetitive avalanche mode conduction, electrons generated from impact ionization are swept into the drain by the electric field whereas the holes generated from impact ionization are injected either into the gate oxide, can cause parasitic bipolar latch-up and/or recombine in the body of the MOSFET (in a MOSFET with a separate body contact, the holes will flow out as substrate current). If the hole current resulting from impact ionization is large enough, the MOSFET would undergo bipolar thermal runaway in a single pulse of UIS, hence the SOA on the MOSFET's datasheet would reflect the limitations of the device. The observation of hot-hole injection is in agreement with the work of Doyle et al [26, 27] which showed that hole injection dominates the degradation mechanism at low gate voltages (V_{GS}) whereas electron injection dominates the degradation mechanism at high gate voltages. For power MOSFETs, this translates to hot-hole injection being the active degradation mechanism during avalanche operation (V_{GS}=0 V and V_{DS}=B_{VDSS}) and hot-electron degradation being the active degradation mechanism during linear mode operation (V_{GS} and V_{DS} = *High*). Fig. 4(b) shows the log-log plot of the average threshold voltage shift (ΔV_{GSTX}) as a function of the number of avalanche cycles where it can

be seen that the characteristic is a straight line thereby indicating a power law relationship. The average V_{GSTX} has been taken in Fig. 4(b) which shows that the V_{GSTX} reduction during repetitive avalanche can be expressed by the following equation.

$$\Delta V_{GSTX} = A \cdot N^{n} \tag{1}$$

where A and n are empirical parameters that are dependent on testing conditions and MOSFET technology. In Fig. 4(b), A is 1.89 x 10^{-13} and n is 1.5.

Fig. 5 shows the R_{DSON} as a function of N for the same MOSFETs where it can be seen that there is a 20% increase in R_{DSON}. To check if the increased R_{DSON} is due to interface state generation resulting from hot-hole injection, the subthreshold slope is also monitored. The subthreshold slope can be calculated by

$$SS = 2.3\frac{K_B T}{q} m \tag{2}$$

where $m = \left(1 + \frac{t_{OX}}{\varepsilon_{OX}}\left[\sqrt{\frac{qN_A\varepsilon_{Si}}{2\Phi_S}} + qD_{it}\right]\right)$ and $\Phi_S = 2\frac{K_B T}{q}\ln\left(\frac{N_A}{n_i}\right)$

K_B is the Boltzmann's constant, m is the body factor, T is the temperature, q is the electronic charge, t_{OX} is the oxide thickness, ε_{OX} is the dielectric constant of the gate dielectric, N_A is the body doping, n_i is the intrinsic carrier concentration of silicon, ε_{Si} is the dielectric constant of silicon, Φ_S is the surface potential of the MOSFET and D_{it} is the density of interface traps. Fig. 6 shows the subthreshold slope as a function of N where it can be seen that the subthreshold slope is stable through out the UIS experiment. For an ideal power MOSFET with 76 nm gate oxide, body doping of 2 × 10^{17} cm^{-3} and no interface trap density (D_{it}=0 $cm^{-2}\cdot eV^{-1}$), m is 4.2

and the subthreshold slope will be 215 mV/dec. However, typical MOSFETs with thermally grown oxides have D_{it} values between 1×10^{10} $cm^{-2}\cdot eV^{-1}$and 1×10^{12} $cm^{-2}\cdot eV^{-1}$. For the power MOSFETs under investigation with subthreshold slopes between 240 and 300 mV/dec, D_{it} values between 1.2×10^{11} $cm^{-2}\cdot eV^{-1}$and 4.2×10^{11} $cm^{-2}\cdot eV^{-1}$ are required to match the calculated subthreshold slope to the measured subthreshold slope. However, the important observation in Fig. 6 is that subthreshold slope and D_{it} are constant over avalanche cycling hence the increase in R_{DSON} is not due to increased interface trap density resulting from hot-hole injection. Doyle et al demonstrated that the bias conditions for maximum interface state generation is $V_{GS}=0.5\cdot V_{DS}$, because both hot-electron and hot-hole injection occur at this point [26, 27] which is also the point of maximum substrate current. These results, which are in agreement with [26, 27], show that interface state generation is not an active degradation mechanism in avalanche mode operation. Examination of the tested MOSFETs after de-capping revealed that degradation of the source metal and the wire-bond interface with the source metal due to thermal fatigue was responsible for the increased R_{DSON}. The temperature cycling resulting from repetitive avalanche imposes thermo-mechanical stresses on the wire-bonds that degrades the contact resistance which is a component of the MOSFETs R_{DSON} [28, 29].

Repetitive UIS is performed at different avalanche currents so as to investigate the impact of I_{AV} on the V_{GSTX} shifts. The experiments are performed with I_{AV} of 160 A and 225 A at a T_{MB} of 150 °C. Fig. 7 shows the log-log plot where it can be seen that A is 1.9×10^{-13} and 2.5×10^{-13} for I_{AV} of 160 A and 225 A respectively. It is expected that an increase in avalanche current would accelerate the change in V_{GSTX} since higher I_{AV} will cause more impact ionization and hence, more hot-hole injection. It can be seen from Fig. 7 that the power law pre-factor (A) increases approximately linearly with the avalanche current i.e. as the avalanche current is increased by 40%, A increases by 30%. The fundamental theory of HCI

can explain the relationship between A and I_{AV} and why ΔV_{GSTX} is accelerated by increased I_{AV}. The "lucky-electron" model introduced by Hu et al [30] describes the probability of an electron being injected into the gate dielectric as a combination of different probabilities. These are the probability of the electron gaining sufficient energy from the electric field to scale the oxide potential barrier, the probability that the electron is re-directed to the Si/SiO_2 interface by a phonon scattering event, the probability that the electron does not undergo any inelastic collision between the point of re-direction and Si/SiO_2 interface and the probability that the electron is not scattered by the image potential well in the oxide [30, 31]. Using the "lucky-electron" model, the rate of supply of hot electrons into the gate dielectric and the substrate current was shown to be proportional to $I_D \cdot \exp(-\Phi_B/q\lambda E_m)$ and $I_D \cdot \exp(-\Phi_i/q\lambda E_m)$ respectively where I_D is the drain current, Φ_B is the barrier energy at the Si/SiO_2 interface, Φ_i is the minimum energy for impact ionization, λ is the hot-electron mean free path and E_m is the maximum channel electric field [31]. It can be seen from the equations that both the rate of carrier injection into the gate dielectric and the substrate current depend on the concentration of carriers in the channel i.e. the avalanche current. This is in agreement with the experimental observation that the power law pre-factor is proportional to the avalanche current i.e. the rate of ΔV_{GSTX} shifting is proportional to the avalanche current.

The impact of the cell pitch on HCI during repetitive UIS is investigated by avalanche cycling 4 µm and 2.5 µm cell pitch 30 V rated MOSFETs. The results of the experiments are illustrated in Fig. 8 where the ΔV_{GSTX} is shown as a function of N for the different cell pitch devices. It can be seen from the results in Fig. 8 that the smaller cell-pitch MOSFETs exhibit better V_{GSTX} stability. This is due lower avalanche current per unit cell in the smaller cell pitch devices which according to the "lucky-electron" model reduces HCI because the rate of charged carrier supply into the gate dielectric is proportional to the current in the channel. Since power MOSFETs are essentially many trench FETs connected in parallel to common

terminals, reducing the cell pitch is in essence, adding more FETs into the same silicon area. A 2.5 µm cell pitch power MOSFET has 37.5% more trench FETs than a 4 µm cell pitch power MOSFET, hence will be more resistant to ΔV_{GSTX} shifting under the same avalanche current since increasing the channel density by 37.5% has the same effect as reducing the current per unit channel by the same amount. As in the case of Fig. 7 where the power law pre-factor (*A*) responded linearly to a change in avalanche current, *A* in this experiment responded linearly to the change in the MOSFET's cell pitch. As the cell pitch is reduced from 4 µm to 2.5 µm (channel density is increased by 37.5%), *A* is reduced by 40% from 1.94 x 10^{-6} to 0.95 x 10^{-6}. Hence, cell pitch scaling is recommended for MOSFETs that are to be repetitively avalanched in automotive applications.

The I_{DSS} is also monitored as a function of avalanche cycling for the 4 µm and 2.5 µm cell pitch MOSFETs. Fig. 9 shows the I_{DSS} as a function of *N* where it can be seen that the smaller cell pitch device exhibits over 100% more leakage on average. This is due to the higher channel density, hence more leakage paths as the cell pitch is reduced. After 240 million cycles, I_{DSS} increased by 100% and 160% for the 4 µm and 2.5 µm cell pitch MOSFETs respectively. Hence, not only does the smaller cell pitch device exhibit more drain leakage, but the drain leakage appears to be more sensitive to avalanche cycling.

The R_{DSON} is also monitored as a function of avalanche cycling. Fig. 10 shows the R_{DSON} as a function of *N* where it can be seen that the 2.5 µm cell pitch MOSFET exhibited 25% smaller R_{DSON} compared with the 4 µm cell pitch MOSFET. The smaller R_{DSON} with the smaller cell pitch device is expected since there are more source-drain conduction paths in the same area of silicon as the cell pitch is reduced. However Fig. 10 shows that R_{DSON} is less sensitive to avalanche cycling in the 2.5 µm cell pitch MOSFET i.e. the R_{DSON} after 240 million cycles increased by 13% and 2% for the 4 µm and 2.5 µm cell pitch MOSFETs respectively. The better R_{DSON} stability with the smaller cell pitch device is attributed to better

current distribution, hence, better heat distribution along the surface of the die. This better heat distribution possibly lessens the thermo-mechanical stress from temperature excursions that degrade the contact resistance between with the aluminum source metal and the bond wires. Hence, the 2.5 µm cell pitch MOSFETs exhibit better R_{DSON} stability but worse I_{DSS} stability in comparison to the 4 µm cell pitch MOSFETs.

The subthreshold slopes of the 2.5 µm and 4 µm cell pitch MOSFETs are also compared. Fig. 11 shows the measured subthreshold slopes at the different intervals of repetitive UIS. Both MOSFETs show subthreshold slope stability during repetitive UIS however the 2.5 µm cell pitch MOSFET exhibits 20% less subthreshold slope. This can be attributed to a higher gate capacitance since there are more trench-FETs in the smaller cell pitch device.

IV. SUMMARY

It has been shown that hot-hole injection into the gate dielectric is responsible for the reduction of the threshold voltage during repetitive UIS. Impact ionization at the drain end of the channel during avalanche cycling creates electron-hole pairs which become hot carriers that can gain sufficient energy to scale the Si/SiO_2 potential barrier. Since the gate is grounded, the effective field in the oxide at the drain end of the channel encourages hole injection into the gate dielectric while electrons are swept into the drain. The relationship between the change in the threshold voltage and the number of avalanche cycles has been shown to be a power law relationship similar to the NBTI and hot-carrier degradation stress models. Experimental repetitive UIS measurements with different avalanche currents show that the rate of reduction in the threshold voltage is proportional to the avalanche current which agrees with the predictions of the “lucky-electron” model. The results show that the pre-factor in the power law relation responds linearly to changes in the avalanche current. The

increase in the on-state resistance observed is due to electro-thermo-mechanical stresses in the wire-bonds which result from temperature excursions that increase the contact resistance by causing thermal fatigue. The subthreshold slope is also monitored during the repetitive UIS experiments and is shown to be stable thereby indicating that interface trap density is not increased during hot-hole injection. This is in agreement with previous studies which have shown that the conditions for increased interface states require $V_{GS}=0.5V_{DS}$ where there is injection of hot-electrons and holes (and is also the point of maximum substrate current). Repetitive UIS experiments were performed on 4 µm and 2.5 µm cell pitch 30 V MOSFETs which showed that smaller cell pitch devices exhibit better threshold voltage stability. The better threshold voltage stability of the smaller cell pitch devices is due to reduced avalanche current per unit cell, which according to the "lucky-electron" model results in less HCI. The results show that the power law pre-factor also responds linearly to changes in the cell pitch (37.5% reduction in cell pitch caused 40% reduction in avalanche pre-factor) and that reducing the cell pitch has the same effect as reducing the avalanche current. The 2.5 µm cell pitch MOSFET also exhibited 25% improved R_{DSON} with better R_{DSON} stability and 20% improved subthreshold slope although with 100% higher I_{DSS} and worse I_{DSS} stability.

REFERENCES

[1] P. Rutter, K. Heppenstall, A. Koh, G. Petkos, and G. Blondel, "High Current Repetitive Avalanche of Low Voltage Trench Power MOSFETs," *International Symposium of Power Semiconductor Devices & ICs,* pp. 112-115, 2009.

[2] K. Dierberger, "Understanding the difference between standard MOSFETs and avalanche energy rated MOSFETs," *Advanced Power Technology Inc. Application Notes,* vol. APT9402, 1994.

[3] A. Koh, "Power MOSFET Single and Repetitive Avalanche Ruggedness Rating," *Application note AN10273,* 2003.

[4] K. Fischer and K. Shenai, "Electrothermal Effects During Unclamped Inductive Switching (UIS) of Power MOSFETs," *IEEE Trans. Electron Devices,* vol. 44, pp. 874-878, 1997.

[5] T. McDonald, M. Soldano, A. Murray, and T. Avram, "Power MOSFET Avalanche Design Guidelines," *International Rectifier Application Note* vol. AN 1005.

[6] D. Donoval, A. Vrbicky, J. Marek, A. Chvala, and P. Beno, "Evaluation of ruggedness of power DMOS transistor from electro-thermal simulation of UIS behaviour," *Solid State Electron,* vol. 52, pp. 892-898, 2008.

[7] A. Testa, S. D. Caro, S. Panarello, S. Patane, R. Letor, S. Russo, S. Poma, and D. Patti, "Stress analysis and lifetime estimation on power MOSFETs for automotive ABS systems," *IEEE Power Electronics Specialist Conference,* pp. 1169-1175, 2008.

[8] I. Pawel, R. Siemieniec, M. Rosch, F. Hirler, and R. Herzer, "Experimental study and simulations on two different avalanche modes in trench power MOSFETs," *IET Circuits Devices Syst.,* vol. 1, pp. 341-346, 2007.

[9] Fairchild Semiconductor, "A combined Single Pulse and Repetitive UIS Rating System," *Application note AN-7515 (AN9322),* 2002.

[10] Vishay Siliconix, "Unclamped Inductive Switching Rugged MOSFETs for Rugged Enviroments," *Vishay Siliconix Application Notes AN601,* 1994.

[11] E. Rosenbaum, R. Rofan, and C. Hu, "Effect of Hot Carrier Injection on n- and pMOSFET Gate Oxide Integrity," *IEEE Electron Dev Lett,* vol. 12, pp. 599-601, 1991.

[12] I. Crupi, "Hot carrier effects in n-MOSFETs with SiO2/HfO2/HfSiO gate stack and TaN metal gate," *Microelectronic Engineering,* vol. 86, pp. 1-3, 2009.

[13] S. Manzini and A. Gallareno, "Avalanche injection of hot holes in the gate oxide of LDMOS transistors," *Solid State Electron,* vol. 44, pp. 1325-1330, 2000.

[14] P. Moens, G. Bosch, and G. Groesenken, "Hot-Carrier Degradation Phenomena in Lateral and Vertical DMOS Transistors," *IEEE Trans. Electron Devices,* vol. 51, pp. 623-628, 2004.

[15] J. Chen, K. Tian, S. Chen, K. Wu, and C. Liu, "On-Resistance Degradation Induced by Hot-carrier Injection in LDMOS Transistors With STI in the Drift Region," *IEEE Electron Dev Lett,* vol. 29, pp. 1071-1073, 2008.

[16] C. Papadas, N. Revil, G. Ghibaudo, and E. Vincent, "On the threshold voltage shift after hot carrier injection in deep submicron n-channel MOSFETs: a quasi-uniform approach," *Microelectronic Engineering,* vol. 28, pp. 361-364, 1995.

[17] I. Lee, S. Yun, K. Kim, C. Yu, and J. Park, "New Experimental Findings on Hot-Carrier-Induced Degradation in Lateral DMOS Transistors," *Microelectronic Reliability,* vol. 46, pp. 1864-1867, 2006.

[18] H. Kufluoglu and M. Alam, "A Computational Model of NBTI and Hot Carrier Injection Time-Exponents for MOSFET Reliability," *Journal of Computational Electronics,* vol. 3, pp. 165-169, 2004.

[19] K. Shenai, "Optimized Trench MOSFET Technologies for Power Devices," *IEEE Trans. Electron Devices,* vol. 39, pp. 1435-1444, 1992.

[20] D. Ueda, H. Takagi, and G. Kano, "Deep Trench Power MOSFET with Ron Area Product of 160 m.mm2," *in IEDM Tech Dig,* pp. 638-641, 1986.

[21] S. Peake, R. Grover, F. Farr, C. Rogers, and G. Petkos, "Fully self-aligned power trench MOSFET utilizing 1 um pitch and 0.2 um trench width," *in Proceedings of the 14th international Symposium on Power Semiconductor Devices and ICs,* pp. 29-32, 2002.

[22] F. Chien, C. Liao, C. Wang, H. Chiu, and Y. Tsai, "Low on resistance trench power

MOSFET designs," *Electronics Letters,* vol. 44, pp. 232-234, 2008.
[23] P. Goarin, R. Dalen, G. Koops, and C. Cam, "Power Trench MOSFETs with very low specific on-resistance for 25 V applications," *Solid State Electron,* vol. 51, pp. 1589-1595, 2007.
[24] M. Juang, W. Chen, C. Yang, S. Lang, M. Lin, and H. Cheng, "Fabrication of trench gate power MOSFETs by using a dual doped body region," *Solid State Electron,* vol. 48, pp. 1079-1085, 2004.
[25] E. Takeda and N. Suzuki, "An Empirical Model for Device Degradation Due to Hot-Carrier Injection," *IEEE Electron Dev Lett,* vol. 4, pp. 111-113, 1983.
[26] B. Doyle, M. Bourcerie, J. Marchetaux, and A. Boudou, "Interface State Creation and Charge Trapping in the Medium-to-High Gate Voltage Range (Vd/2 > Vg > Vd) During Hot-Carrier Sressing of n-MOS Transistors," *IEEE Trans. Electron Devices,* vol. 37, pp. 744-754, 1990.
[27] B. Doyle, M. Bourcerie, C. Bergonzon, R. Benecchi, A. Bravis, K. Mistry, and A. Boudou, "The Generation and Characterization of Electron and Hole Traps Created by Hole Injection During Low Gate Voltage Hot-Carrier Stressing of n-MOS Transistors," *IEEE Trans. Electron Devices,* vol. 37, pp. 1869-1876, 1990
[28] W. Loh, M. Corfield, H. Lu, S. Hogg, T. Tilford, and C. Johnson, "Wire Bond for Power Electronic Modules - Effect of Bonding Temperature," *International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, EuroSime,* pp. 1-6, 2007.
[29] T. Matsunaga and S. Sudo, "Evaluation of Fatigue Life Reliability and New Lead Bonding Technology for Power Modules," *Technical Reports, Mitsubishi Electric Advance,* pp. 13-16, 2006.
[30] C. Hu, "Lucky Electron Model of Channel Hot Electron Emission," *In IEDM Tech Dig,* pp. 22-25, 1979.
[31] C. Hu, S. Tam, F. Hsu, P. Ko, T. Chan, and K. Terrill, "Hot-Electron-Induced MOSFET Degradation-Model, Monitor and Improvement," *IEEE Trans. Electron Devices,* vol. 32, pp. 375-385, 1985.

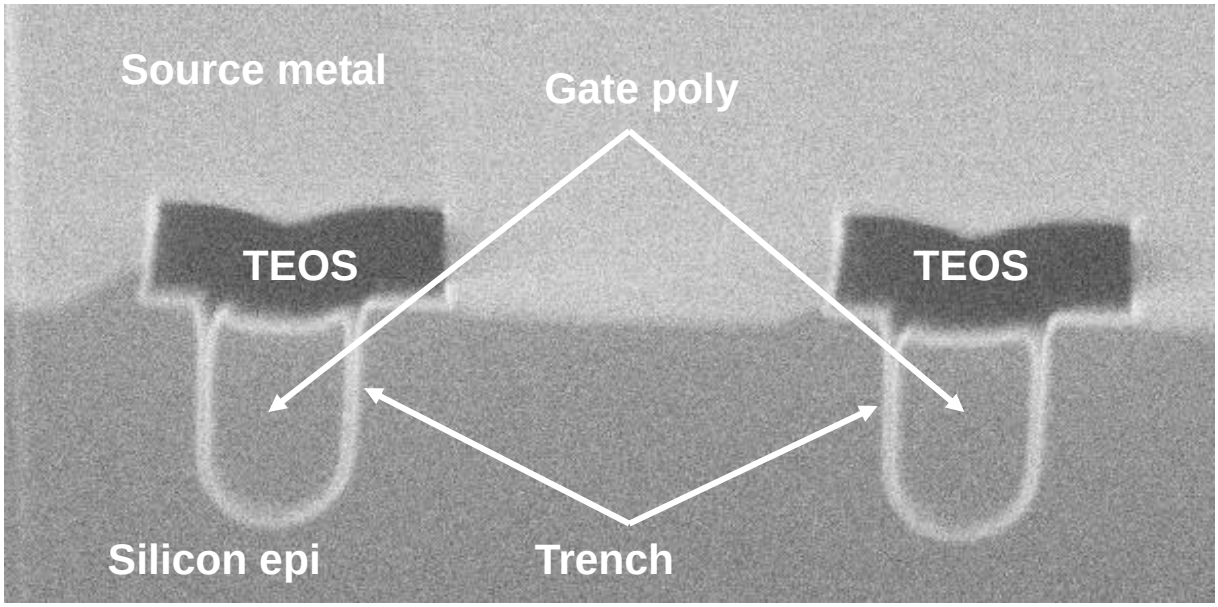

Fig. 1. Cross-sectional SEM of the power MOSFET showing 2 trenches, gate poly, source metal and TEOS passivation.

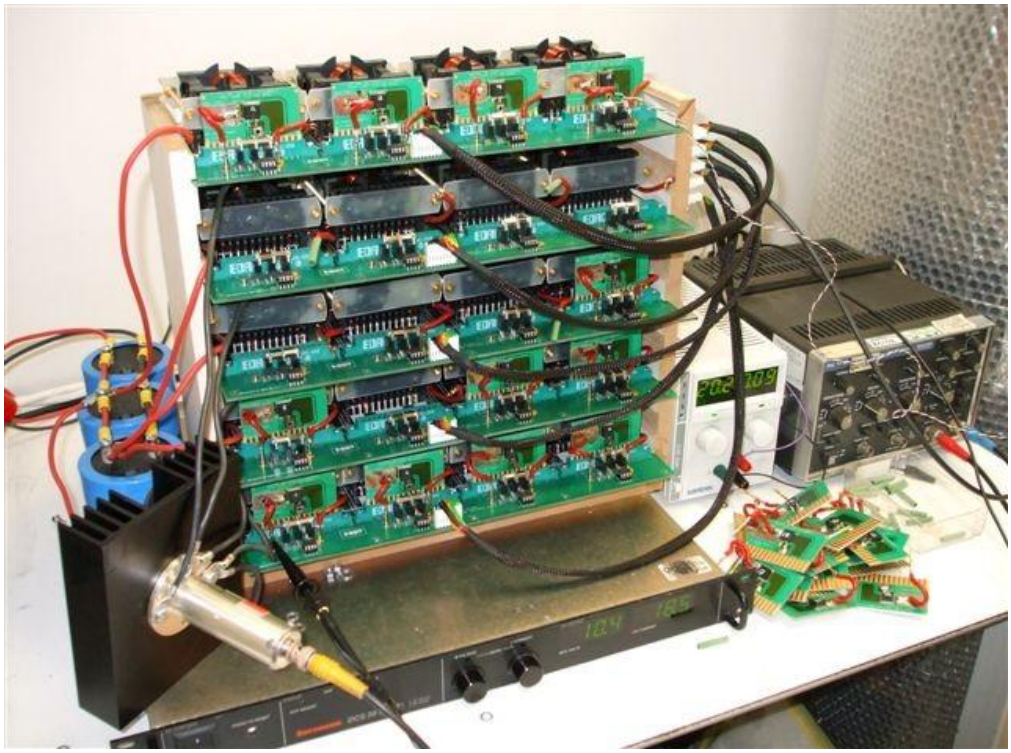

Fig. 2(a). The custom-built repetitive avalanche test equipment capable of testing 16 MOSFETs simultaneously.

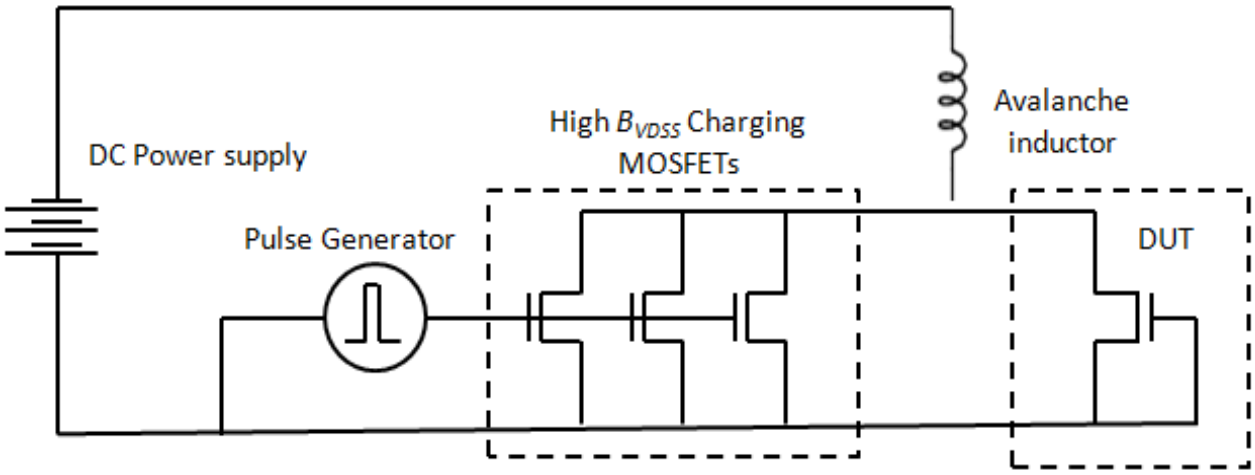

Fig. 2(b). The circuit diagram of the custom-built repetitive avalanche test equipment showing the power supply, pulse generator, high B_{VDSS} charging MOSFETs, the avalanche inductor and the DUT.

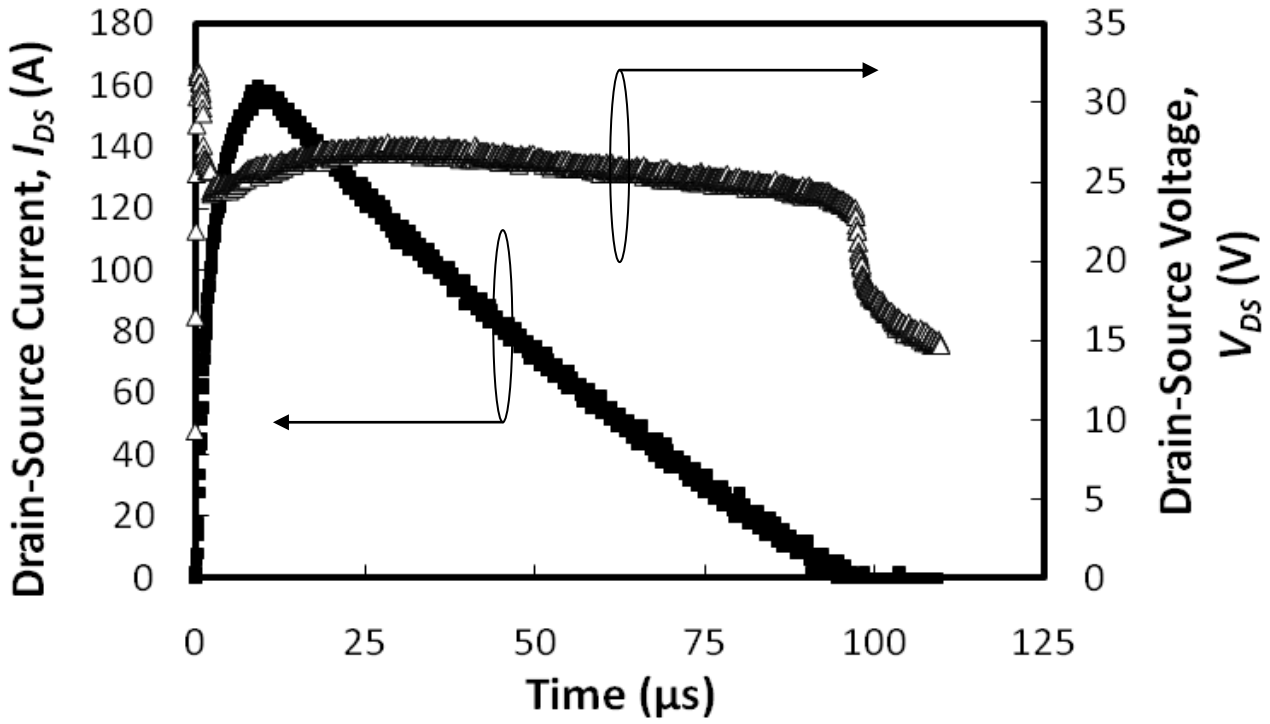

Fig. 3. The drain-source avalanche current and drain source voltage shown as functions of the avalanche time. As the avalanche current flows through, the drain-source voltage rises to the B_{VDSS} until the current reaches zero. The avalanche duration is determined by the avalanche current, MOSFET B_{VDSS} and the magnitude of inductance.

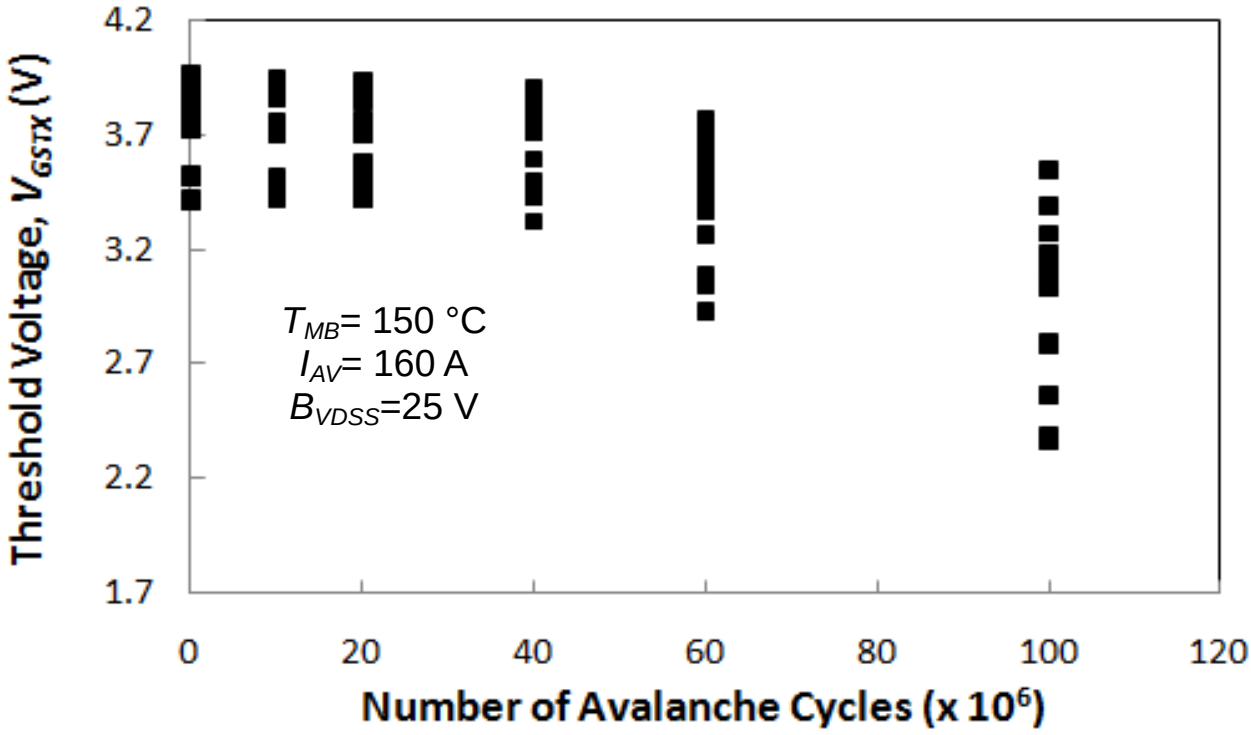

Fig. 4(a). The V_{GSTX} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 µm cell pitch trench devices tested under repetitive UIS. The sample set of devices shows an initial V_{GSTX} ranging from 3.2 V to 4 V with a uniform decrease in V_{GSTX} of about 21% after 100 million cycles.

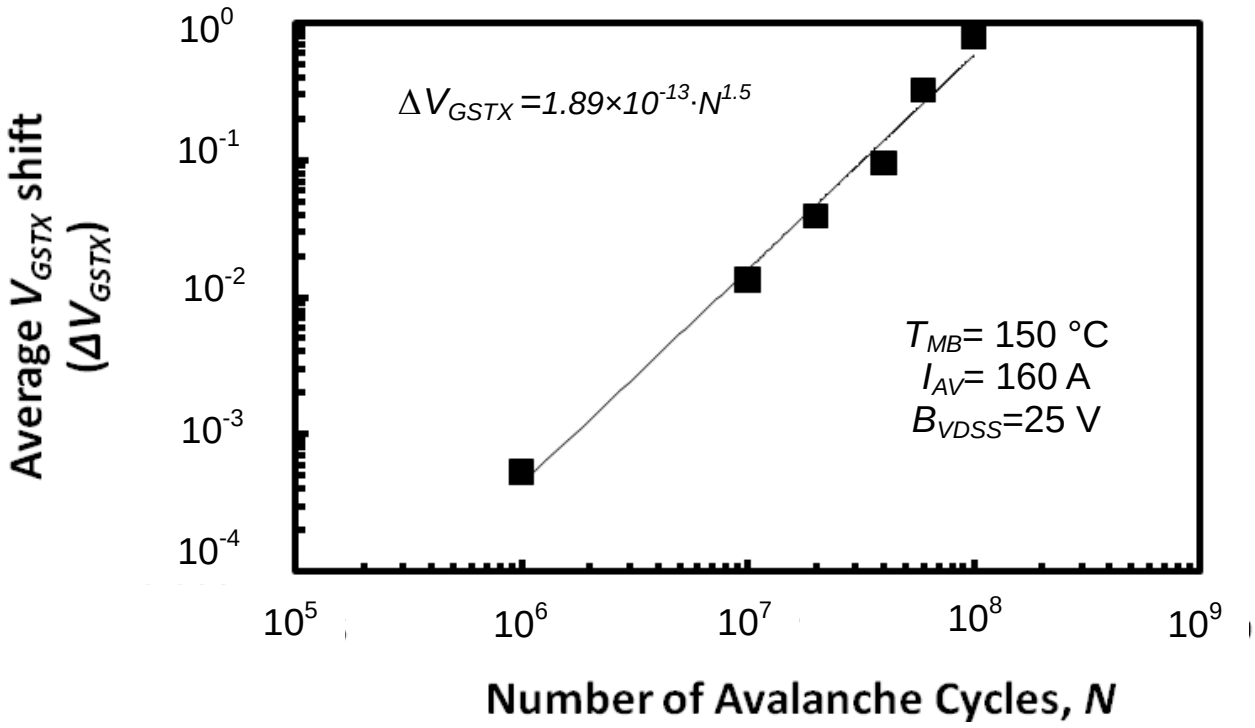

Fig. 4(b). The log-log plot of the average threshold voltage shift as a function of the number of avalanche cycles showing the power law relationship.

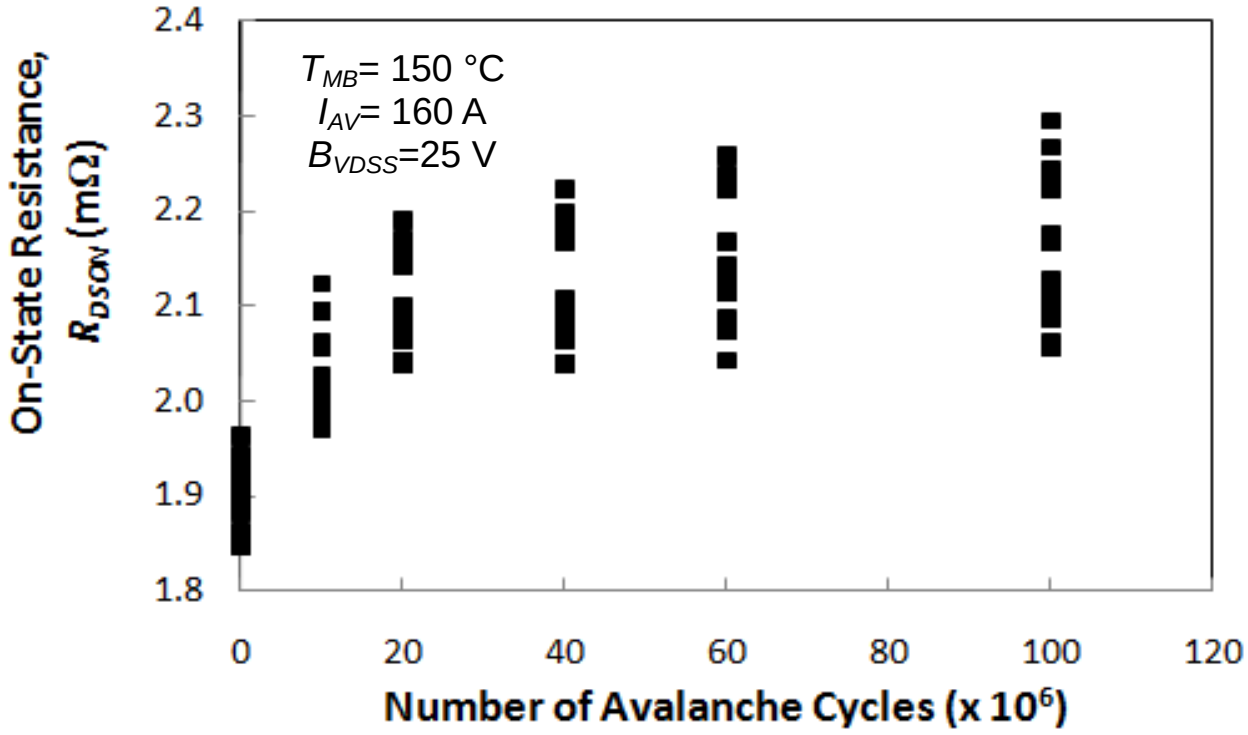

Fig. 5. The R_{DSON} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 µm cell pitch trench devices tested under repetitive UIS. The increase in R_{DSON} is an average of 20% for the MOSFETs and is due to degraded contact resistance between the aluminum source metal and the source wire bonds.

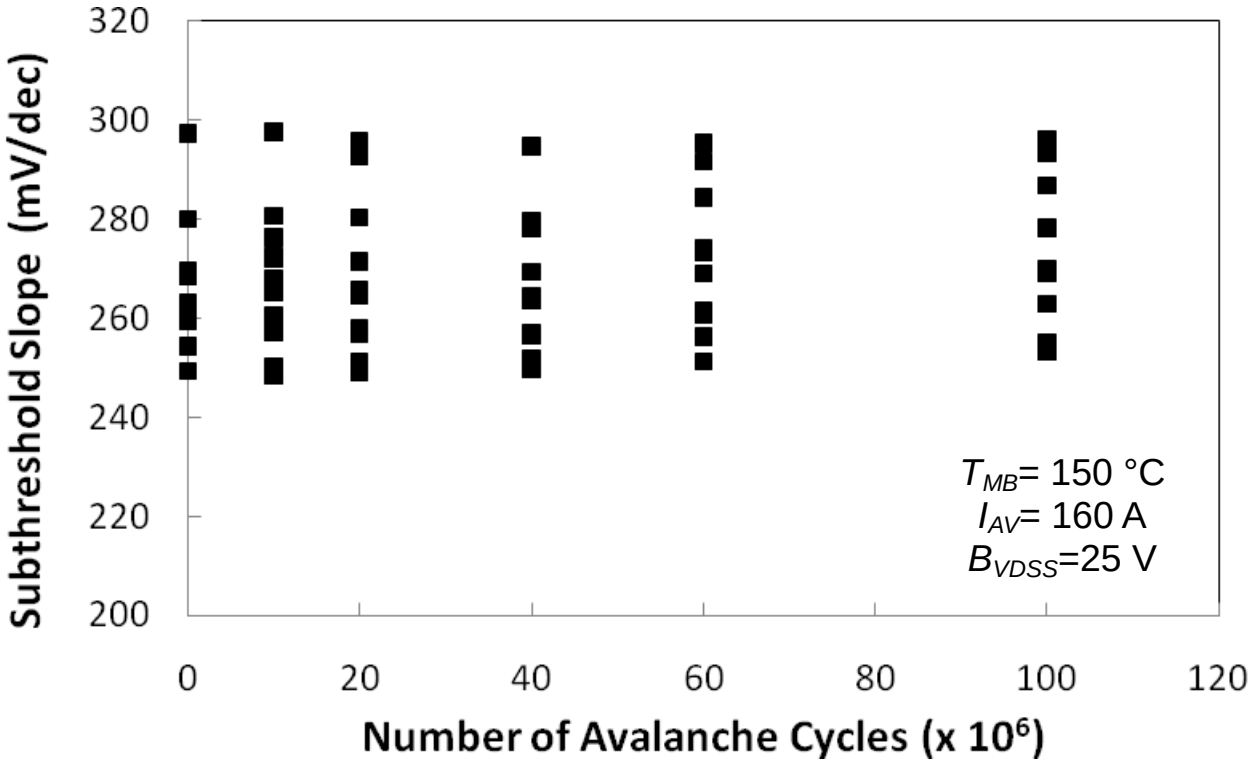

Fig. 6. The measured subthreshold slopes of the MOSFETs at different stages of the avalanche cycling experiment. The stability of the subthreshold slope shows that interface trap generation resulting from HCI is not an active degradation mechanism in repetitive UIS.

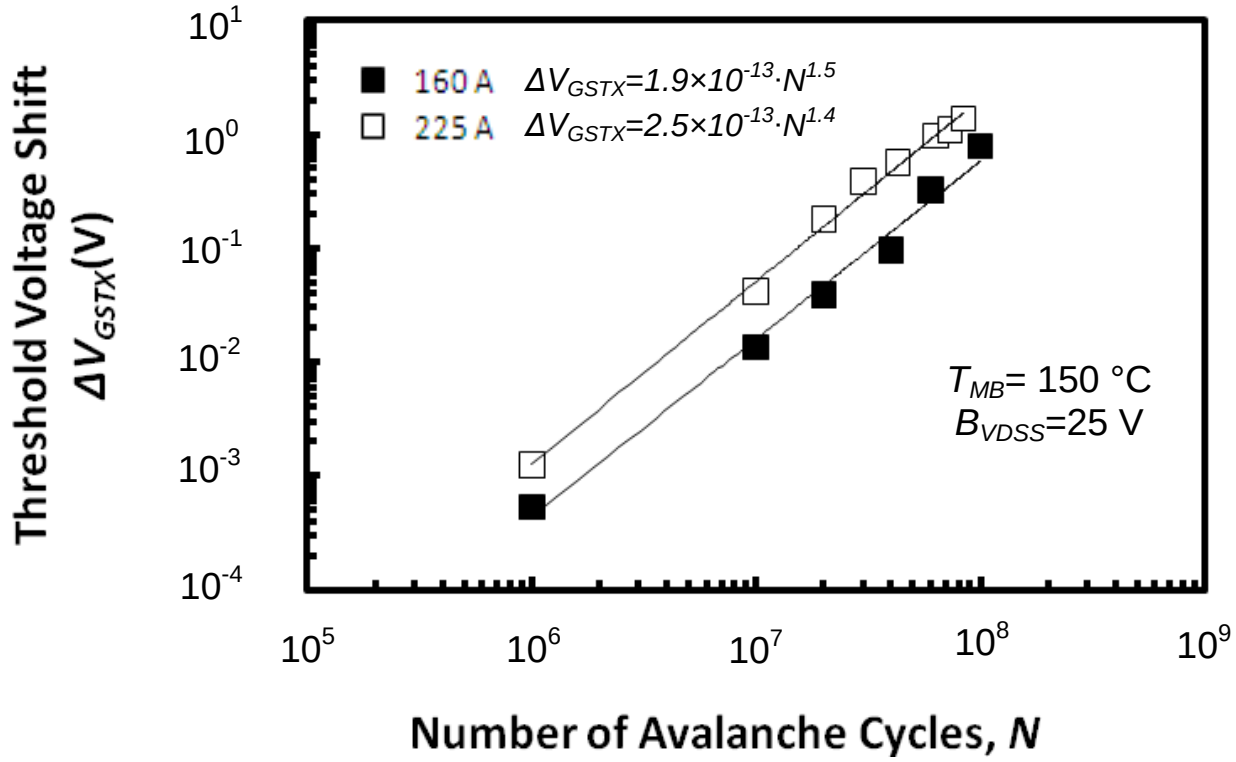

Fig. 7. The log-log plot showing the power law relationship between the change in threshold voltage (ΔV_{GSTX}) and the number of avalanche cycles. A 40% increase in the avalanche current resulted in a 30% increase in the power law pre-factor.

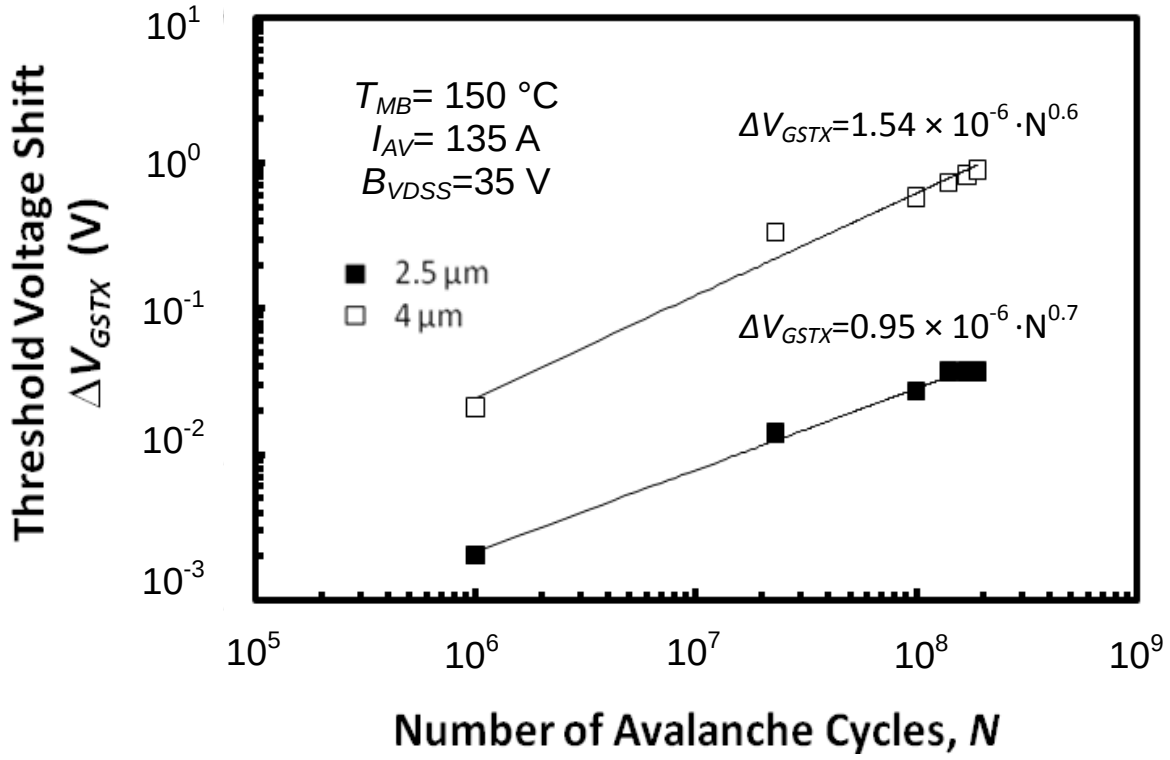

Fig. 8. The log-log plot showing the power law relationship between ΔV_{GSTX} and the number of avalanche cycles for the 4 µm and 2.5 µm cell pitch trench devices tested under repetitive UIS. A 37.5% increase in channel density resulted in a 40% decrease in the power law pre-factor.

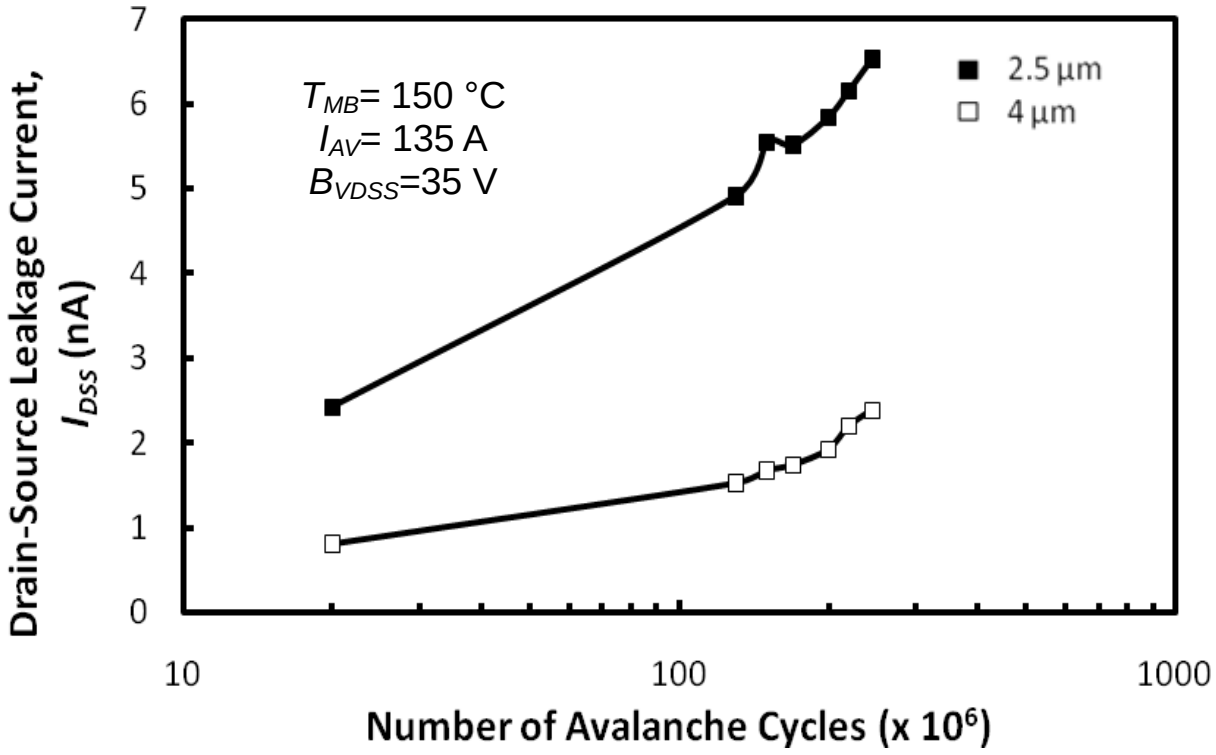

Fig. 9. The I_{DSS} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 µm and 2.5 µm cell pitch trench devices tested under repetitive UIS. The 2.5 µm cell pitch devices exhibit 100% higher due to the greater channel density hence more source-drain conductive paths.

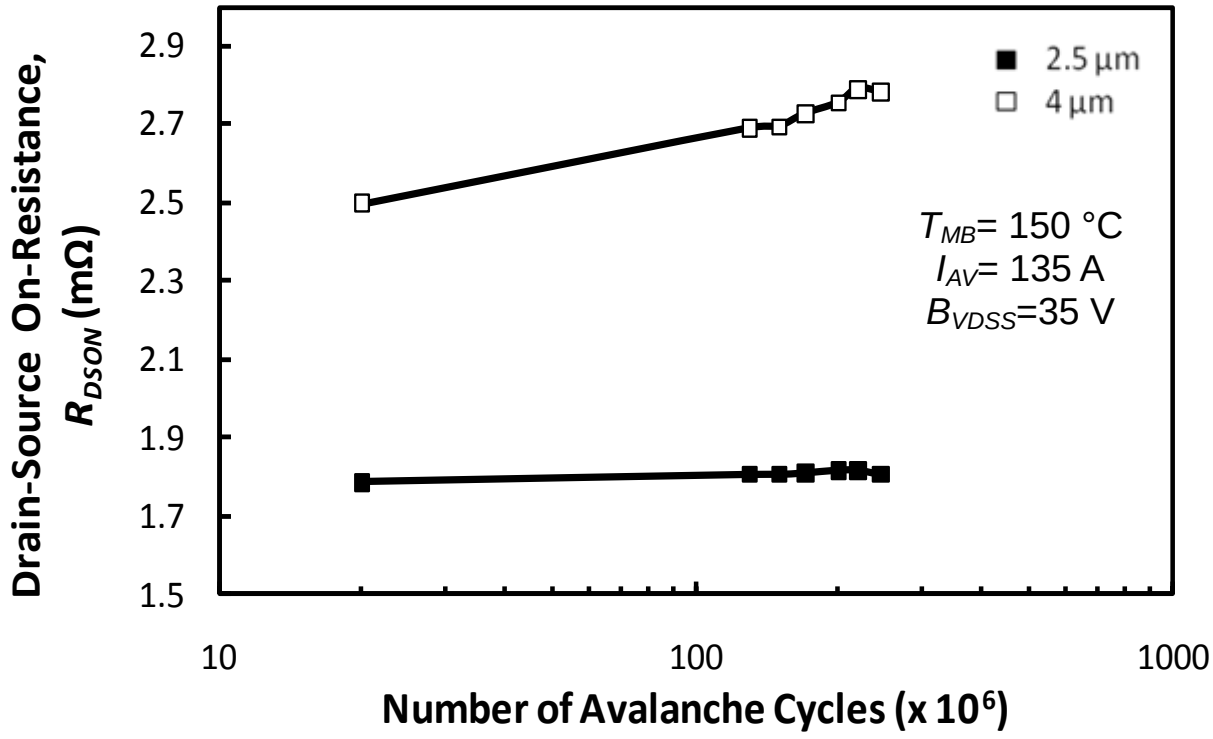

Fig. 10. The R_{DSON} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 µm and 2.5 µm cell pitch trench devices tested under repetitive UIS. The 2.5 µm cell pitch devices show 25% improvement in R_{DSON} and better R_{DSON} stability over the number of avalanche cycles.

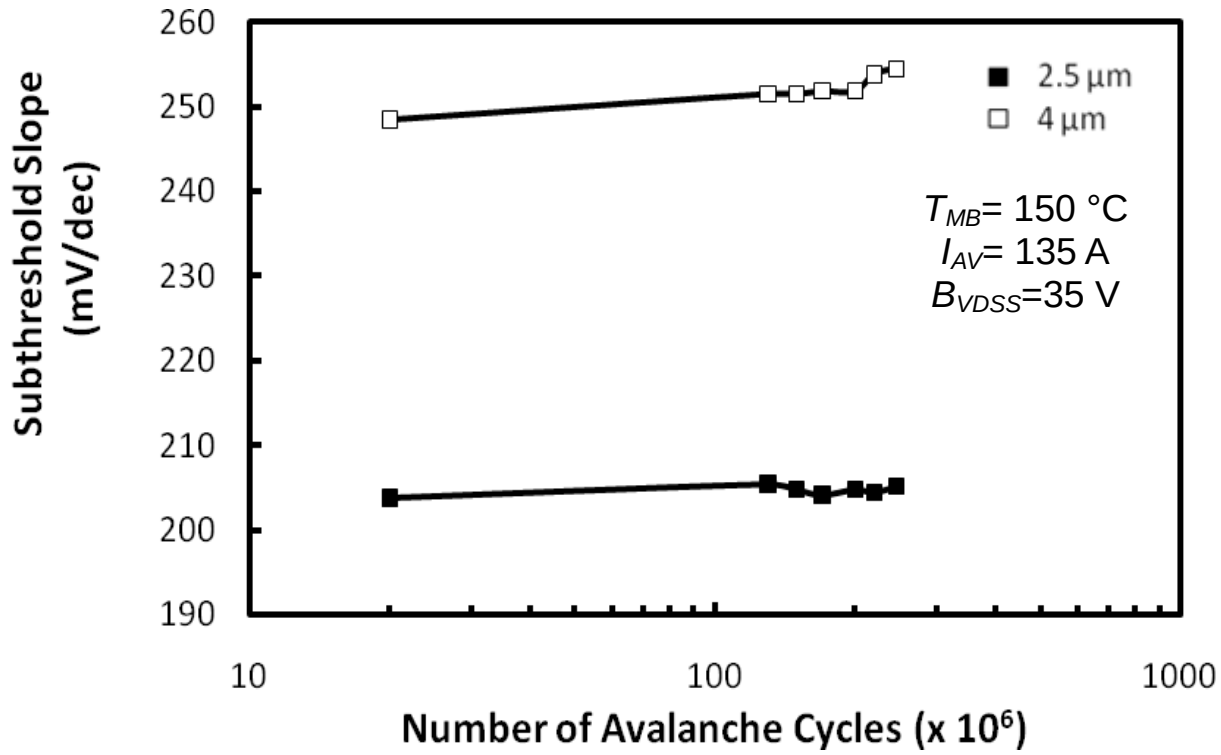

Fig. 11. The subthreshold slopes of the 4 µm and 2.5 µm cell pitch MOSFETs showing 25% improvement in the smaller cell pitch device. This improvement is due to higher gate capacitance from higher channel density and also possibly more fully depleted channels. The stability of the subthreshold slope indicates that interface trap generation is not an active degradation mechanism during repetitive UIS.

Fig. 1. Cross-sectional SEM showing the trenches, gate poly, source metal and TEOS passivation.

Fig. 2(a). The custom-built repetitive avalanche test equipment capable of testing 16 MOSFETs simultaneously.

Fig. 2(b). The circuit diagram of the custom-built repetitive avalanche test equipment showing the power supply, pulse generator, high B_{VDSS} charging MOSFETs, the avalanche inductor and the DUT.

Fig. 3. The drain-source avalanche current and drain source voltage shown as functions of the avalanche time. As the avalanche current flows through, the drain-source voltage rises to the B_{VDSS} until the current reaches zero.

Fig. 4(a). The V_{GSTX} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 μm cell pitch trench devices tested under repetitive UIS. The sample set of devices shows an initial V_{GSTX} ranging from 3.2 V to 4 V with a uniform decrease in V_{GSTX} of about 20% after 100 million cycles.

Fig. 4(b). The log-log plot of the average threshold voltage shift as a function of the number of avalanche cycles showing the power law relationship.

Fig. 5. The R_{DSON} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 μm cell pitch trench devices tested under repetitive UIS. The increase in R_{DSON} is an average of 20% for the MOSFETs and is due to degraded contact resistance between the

aluminum source metal and the source wire bonds.

Fig. 6. The measured subthreshold slopes of the MOSFETs at different stages of the avalanche cycling experiment. The stability of the subthreshold slope shows that interface trap generation resulting from HCI is not an active degradation mechanism in repetitive UIS.

Fig. 7. The log-log plot showing the power law relationship between the change in threshold voltage (ΔV_{GSTX}) and the number of avalanche cycles. A 40% increase in the avalanche current resulted in a 30% increase in the power law pre-factor.

Fig. 8. The log-log plot showing the power law relationship between ΔV_{GSTX} and the number of avalanche cycles for the 4 µm and 2.5 µm cell pitch trench devices tested under repetitive UIS. A 37.5% increase in channel density resulted in a 40% decrease in the power law pre-factor.

Fig. 9. The I_{DSS} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 µm and 2.5 µm cell pitch trench devices tested under repetitive UIS. The 2.5 µm cell pitch devices exhibit 100% higher due to the greater channel density hence more source-drain conductive paths.

Fig. 10. The R_{DSON} of the MOSFETs shown as functions of the number of avalanche cycles for the 4 µm and 2.5 µm cell pitch trench devices tested under repetitive UIS. The 2.5 µm cell pitch devices show 25% improvement in R_{DSON} and better R_{DSON} stability over the number of avalanche cycles.

Fig. 11. The subthreshold slopes of the 4 µm and 2.5 µm cell pitch MOSFETs showing 25% improvement in the smaller cell pitch device. This improvement is due to higher gate capacitance from higher channel density and also possibly more fully depleted channels. The stability of the subthreshold slope indicates that interface trap generation is not an active degradation mechanism during repetitive UIS.