Improved Self Gain in Deep Submicrometer Strained
Silicon-Germanium P-MOSFETs with HfSiO$_x$/TiSiN Gate Stacks

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Abstract- The self-gain of surface channel compressively strained SiGe pMOSFETs with HfSiOₓ/TiSiN gate stacks is investigated for a range of gate lengths down to 55 nm. There is 125% and 700% enhancement in the self-gain of SiGe pMOSFETs compared with the Si control at 100 nm and 55 nm lithographic gate lengths respectively. This improvement in the self-gain of the SiGe devices is due to 75% hole mobility enhancement compared with the Si control and improved electrostatic integrity in the SiGe devices due to less boron diffusion into the channel. 55 nm gate length SiGe pMOSFETs show 50% less drain induced barrier lowering compared with the Si control devices. Electrical measurements show that the SiGe devices have larger effective channel lengths. It is shown that the enhancement in the self-gain of the SiGe devices compared with the Si control increases as the gate length is reduced thereby making SiGe pMOSFETs with HfSiOₓ/TiSiN gate stacks an excellent candidate for analog/mixed-signal applications.

Index Terms- compressively strained SiGe, high K, metal gates, mixed signal, self gain.
I. INTRODUCTION

There has been a lot of focus on the device performance of SiGe pMOSFETs with high-k/metal gate stacks from the perspective of digital metrics [1-4], however, there has been very little attention on the self-gain of such devices. Lindgeren et al [5] reported compressively strained SiGe pMOSFETs with 30% enhancement in the self gain due to mobility enhancement compared with the Si control device, however 0.3 µm gate length devices with poly gates and silicon dioxide gate dielectrics were used. For CMOS implementation in mixed-signal applications, it is important for the self-gain of highly scaled devices in advanced technology nodes to be evaluated. The self-gain ($A_V$), which is the ratio of the transconductance ($g_m$) to the drain conductance ($g_{DS}$), is an important metric used by the international technology roadmap for semiconductors (ITRS) to monitor the performance capability of CMOS devices in analog/mixed signal applications. The ITRS performance projections of analog MOSFETs describe analog speed and precision MOSFETs which are required to have five times ($5L_{G_{min}}$) and ten times ($10L_{G_{min}}$) the gate length of the minimum CMOS feature in the technology node [6]. These are called non-minimum length (NML) MOSFETs designed for higher gain and better low frequency amplification. In this letter, the self gain of SiGe pMOSFETs with HfSiO$_x$/TiSiN gate stacks suitable for use as NML devices in 22 nm technology nodes is reported as well as high speed 55 nm devices with cut-off frequencies over 100 GHz. It is shown that mobility enhancement boosts on-state performance (by increasing $g_m$) and that the electrostatic integrity is improved (reduced $g_{DS}$) by suppressed boron diffusion due to compressive strain.
II. DEVICE FABRICATION

The strained SiGe pMOSFETs under investigation are surface channel devices with approximately 40 nm of compressively strained Si\textsubscript{0.77}Ge\textsubscript{0.23} epitaxially deposited on the active areas. The SiGe surface was passivated by rapid thermal nitridation before depositing HfSiO\textsubscript{x} by atomic layer deposition, resulting in an effective oxide thickness of 1.3 nm. A TiSiN layer was formed by sputtering before the gates were defined by photolithography. A range of gate lengths from 1 µm to 55 nm was etched after which halo and junction implantation is performed. Details of the fabrication process are given elsewhere [7]. Si control pMOSFETs were co-fabricated under the same processing conditions. Fig.1 shows a cross sectional TEM image of a strained SiGe pMOSFETs.

III. ELECTRICAL RESULTS AND DISCUSSION

MOSFET scaling boosts the cut-off frequency ($f_t$) but degrades the self-gain. The MOSFET cut-off frequency increases as the gate length ($L_G$) is reduced whereas the self-gain reduces with $L_G$ due to drain induced barrier lowering (DIBL) [8]. As the MOSFET $L_G$ is scaled, there is an increase in the drain conductance ($g_{DS}$) due to short channel effects like DIBL, channel length modulation and substrate-current induced body effect [8]. Fig. 2 shows the impact of scaling on the cut-off frequency and the self-gain in the SiGe pMOSFETs with HfSiO\textsubscript{x}/TiSiN gate stacks. The cut-off frequency ($f_t$) is calculated from the gate transfer characteristics ($I_{DS}$ Vs $V_{GS}$) as $f_t=g_m/2\pi C_{OX}$ whereas the self-gain ($A_V$) is calculated from differential $I_{DS}$ Vs $V_{GS}$ measurements as $A_V=g_m/g_{DS}$. $C_{OX}$ is the gate dielectric capacitance density. It can be seen from Fig. 2 that as $L_G$ is reduced from 500 nm to 55 nm, the maximum $f_t$ is increased from 3.5 GHz to 100 GHz and the maximum self-gain reduces from 200 to 6. Fig. 3 shows the self-gain of the Si and SiGe devices as functions of $L_G$ in comparison with the ITRS requirements. The self-gain is measured at a gate voltage overdrive
of 200 mV \( (V_{GS}-V_{TH}=200 \text{ mV} \) where \( V_{TH}\) is the threshold voltage) and a \( V_{DS} \) of 0.5 V so as to enable comparison with the near term projections for self-gain in the ITRS analog and mixed signal guide [6]. The short channel strained SiGe devices performed significantly better with the gain enhancement compared with the Si control increasing as the gate length is reduced. The self-gain enhancement of the SiGe device compared with the Si control device is 125% and 700% at 100 nm and 55 nm \( L_G \) respectively. Fig. 4 shows the percentage enhancement in the self-gain of the SiGe device compared with the Si control device as a function of the \( L_G \). Unlike most performance enhancement metrics, the enhancement in the self-gain increases as \( L_G \) is reduced which is very encouraging for the implementation of such devices in mixed-signal RFCMOS.

The improved mixed-signal performance of the strained SiGe devices is due to two factors. These are the improved on-state performance due to hole mobility enhancement from compressive strain and the improved electrostatic integrity from lower subthreshold drain conductance. The effective mobility \( (\mu_{EFF}) \) was extracted from the 1 \( \mu \)m gate length and 10 \( \mu \)m gate width pMOSFETs using the split CV technique. Fig. 5(a) shows \( \mu_{EFF} \) as a function of the effective field where it can be seen that \( \mu_{EFF} \) is 75% higher for the strained SiGe pMOSFETs at a vertical effective field \( (E_{EFF}) \) of 1 MV.cm\(^{-1}\). Fig. 5(b) shows the percentage mobility enhancement of the SiGe device compared with the Si control at an \( E_{EFF} \) of 1 MV.cm\(^{-1}\) for different devices reported in the literature [2, 9-14]. It can be seen from Fig. 5(b) that the mobility enhancement of 75% reported here is optimum for 23% Ge content.

The self-gain can be expressed as the product of the transconductance-efficiency \( (g_m/I_{DS}) \) and the Early voltage \( (V_{EA}=I_{DS}/g_{DS}) \) [15]. The Early voltage \( (V_{EA}) \) is a measure of electrostatic integrity and is inversely related to drain induced barrier lowering (DIBL). It was shown by Huang et al [8] that DIBL is related to the effective channel length \( (L_{EFF}) \) through a negative exponential, hence DIBL increases rapidly as \( L_{EFF} \) is reduced. The parameter \( L_{EFF} \) is
the difference between the lithographic gate length ($L_G$) and the dopant out-diffusion length ($\Delta L$) [16] which in turn dependent on the diffusivity of the junction dopant (boron for pMOSFETs) in the semiconductor. Boron is known to have a suppressed diffusivity in compressively strained SiGe [17-19], hence the $L_{EFF}$ is expected to be longer in the SiGe devices due to less lateral diffusion of the junction implants into the channel. To verify this, $L_{EFF}$ of the devices were extracted using the shift and ratio method [20]. The $L_{EFF}$ extracted for the 100 nm gate length Si and SiGe device was 65 nm and 90 nm respectively. The larger $L_{EFF}$ in the SiGe device results in higher $V_{EA}$ and output resistance [8]. Fig. 6 shows $V_{EA}$ as a function of $I_{DS}$ for the 100 nm and 250 nm strained SiGe and Si control devices. At an $I_{DS}$ of $V_{GS}=V_{TH}$=200 mV, there is 150% and 200% enhancement in the $V_{EA}$ of the SiGe device compared with the Si control at $L_G$=250 nm and 100 nm respectively. The electrostatic integrity of the devices is measured by extracting DIBL. Fig. 7 shows DIBL as a function of the $L_{EFF}$ for the Si and SiGe devices. The percentage reduction of DIBL in the strained SiGe pMOSFET compared with the Si control device increases from 5% at 1 µm $L_G$ to 50% at 55 nm $L_G$. Reduced electrostatic integrity in short channel devices can also result from sub-surface punch-through i.e. subthreshold drain conductance occurring beneath the channel. Sub-surface punch-through is also likely to be reduced in the strained SiGe devices compared with the Si control because sub-surface boron diffusion will be less in the strained SiGe device. Hence, similar to the self-gain, as the devices are scaled, the improved DIBL in the strained SiGe device compared with the Si control becomes more evident. Improved electrostatic integrity in the short channel SiGe devices correlates with improved self-gain.

The increasing performance enhancement in the self-gain of the SiGe device as $L_G$ is reduced is due to two mechanisms. At long gate lengths, the self-gain enhancement is due to higher $g_m$ from enhanced hole mobility and at short gate lengths the self-gain enhancement is due to both higher $g_m$ and lower $g_{DS}$. These results show that highly scaled SiGe pMOSFETs
have good analog potential, which is promising for analog/mixed-signal applications implemented in deep submicrometer CMOS technology.

**IV. CONCLUSION**

SiGe pMOSFETs with HfSiO$_x$/TiSiN gate stacks exhibit 125% and 700% enhancement in the self gain compared with the Si control devices at 100 nm and 55 nm gate length respectively. The enhancement in self-gain is due to 75% mobility enhancement from compressive strain and better electrostatic integrity in the SiGe devices. Electrical measurements show smaller effective channel length in the Si control devices and higher Early voltage in the SiGe devices. Lower boron diffusion in compressively strained SiGe reduces the lateral diffusion of the junction implants and mitigates against sub-surface punch-through and DIBL. SiGe pMOSFETs with HfSiO$_x$/TiSiN gate stacks show good prospects for high performance analog-mixed signal CMOS technologies.
REFERENCES


Fig. 1. TEM images of a 70 nm strained SiGe device and the corresponding gate
stack/channel.

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Fig. 2. The self-gain ($A_V$) as a function of the cut-off frequency ($f_t$) for different gate length strained SiGe pMOSFETs. The self-gain reduces as the gate length reduces and the cut-off frequency increases as the gate length reduces.

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Fig. 3. The self-gain as a function of the lithographic gate channel length for the Si and SiGe devices. The self-gain is measured at $V_{GS}-V_{TH}=200 \text{ mV}$ and $V_{DS}=0.5 \text{ V}$. The enhancement in the self-gain of the SiGe device over the Si control increases as the gate length reduces.
Fig. 4. The percentage enhancement in the self-gain of the SiGe devices compared with the Si control as a function of the lithographic gate length. The impact of scaling on the strain-induced gain enhancement is positive.

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Fig. 5(a). Effective hole mobility determined by gate-channel capacitances and drain conductance measurements. Hole mobility is increased by 80% compared with the Si control device and by 60% compared with the universal mobility curve at 1 MV.cm\(^{-1}\).

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Fig. 5(b). The maximum hole mobility enhancement compared with the Si control for various germanium percentages reported in literature. The 80% hole mobility enhancement demonstrated by the devices here is high for the 23% germanium compared with what has previously been reported.

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Fig. 6. The Early voltage as a function of the drain current at a drain voltage of 1 V for the 100 nm and 250 nm Si control and SiGe devices. There is enhancement in the Early voltage of the SiGe device compared with the Si control over a wide range of drain currents.
Fig. 7. DIBL as a function of the effective channel length for the Si and SiGe devices. SiGe devices show less DIBL which is consistent with larger self gain.

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