**Low-Frequency Noise Characterization of Strained Germanium pMOSFETs**

E. Simoen*, J. Mitard, B. De Jaeger, G. Eneman[2,3], A. Dobbie[1], M. Myronov[1], T.E.Whall[1], D.R. Leadley[1], M. Meuris, T. Hoffmann and C. Claeys[2]

Imec, Kapeldreef 75, B-3001 Leuven, Belgium

[1]Department of Physics, The University of Warwick, CV4 7AL UK

[2]also at E.E. Depart KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

[3]also FWO-Vlaanderen, B-1000 Brussels, Belgium

## Abstract

The low-frequency (LF) noise in strained Ge epitaxial layers, grown on reverse-graded relaxed SiGe buffer layers, has been evaluated for different front-end processing conditions. It has been shown that the 1/f noise in strong inversion is governed by trapping in the gate oxide (number fluctuations) and not affected by the presence of compressive strain in the channel. However, some impact has been found from the type of halo implantation used, whereby the lowest noise spectral density and highest hole mobility is obtained by replacing the standard As halo by a P implantation. At the same time, the omission of the junction anneal results in poor device characteristics, which can be understood by considering the presence of a high density of non-annealed implantation damage in the channel and the gate stack near source and drain.

**Keywords:** low-frequency noise; generation-recombination noise, strained and relaxed germanium; hole mobility

## 1. Introduction.

High-mobility channels are being considered as serious contenders for the development of deca-nanometer CMOS technology nodes [1],[2]. This means in practice that Ge or III-V layers have to be grown by hetero-epitaxy on a silicon substrate, resulting generally in a large density of threading dislocations (TDs) [3]. For p-channel transistors, Ge is one of the prime candidates to replace silicon. However, the ~4 % lattice mismatch results in a small critical thickness for relaxation of Ge epitaxial layers on Si and in a high density of TDs, usually in the range of $10^8$ $cm^{-2}$ which can be reduced to ~$10^7$ $cm^{-2}$ by a post-growth thermal annealing [4]. The presence of such defects may have an impact on the device performance, for example the junction leakage current [5], the threshold voltage ($V_T$) or the inversion-layer mobility [6]. Also the low-frequency (LF) noise increases in the presence of TDs [7]-[9], since dislocations introduce generation-recombination (GR) centers in the band gap of semiconductor materials. In fact, it has been shown recently that this is also the case for pMOSFETs fabricated in relaxed Ge-on-Si epilayers [10],[11], where an increase in the current noise spectral density ($S_I$) is observed in weak inversion. It has been shown that this excess GR noise can be reduced significantly by replacing relaxed Ge-on-Si by a strained Ge (sGe) channel [11], which is fabricated on a reverse-graded strain-relaxed $Si_{0.2}Ge_{0.8}$ buffer (SRB) layer [12], and which has the effect of reducing the TD density.

It is the aim of the present work to investigate in detail the LF noise in sGe pMOSFETs from weak to strong inversion. Wafers with different processing conditions are compared in order to develop a better understanding of the fluctuation mechanisms. It is shown that the $1/f^{\gamma}$ noise ($\gamma$~1), dominant in strong inversion, is governed by number fluctuations, i.e., charge trapping in the gate oxide and is also correlated with the low-field channel mobility. Interestingly, devices

processed without junction anneal (JA) exhibit poor hole mobility and high 1/f-like noise. The latter fact can be interpreted in terms of the model proposed by Malm *et al*. for a channel with a highly localized defect density [9]. The origin of both effects is assigned to residual implantation damage in the Ge channel, causing carrier scattering and trapping.

## 2. Experimental.

Ge pMOSFETs have been fabricated on ~1.5 μm thick relaxed Ge layers deposited by Reduced Pressure Chemical Vapor Deposition (RPCVD) on 200 mm diameter Czochralski (CZ) Si substrates and on 20 nm strained Ge, deposited on a 2.1 μm thick fully relaxed, reverse-graded $Si_{0.2}Ge_{0.8}$ SRB on CZ Si [12]. The density of TDs in the relaxed Ge-on-Si substrates is in the range of a few $10^7$ $cm^{-2}$ after post-growth annealing at 850 $^oC$ for 3 min [4]. The dislocation density was about one decade smaller for the sGe wafers, i.e., about a few $10^6$ $cm^{-2}$.

The gate stack was processed starting from an epitaxial Si passivation layer, which was partially oxidized and on top of which 3.5 nm $HfO_2$ was deposited by Atomic Layer Deposition (ALD) [13]. The resulting Equivalent Oxide Thickness (EOT) is 1.45 nm. The metal gate consists of 10 nm TaN/ 70 nm TiN. For the sGe wafers, process splits have been implemented with respect to the tilted halo implantation, the junction anneal and the Highly Doped Drain (HDD) Pre-Amorphization Implantation (PAI), as indicated in Table I. Finally, NiGe metallization was applied.

LF noise measurements have been performed on wafers in linear operation at a drain bias $V_{DS}$ of -50 mV and on transistors with different widths W and lengths L, using Berkeley Technology Associates hardware under control of ProPlusSolution software. The gate bias $V_{GS}$ has been stepped from weak to strong inversion. In order to have some idea of the LF noise

variability, between 3 and 5 transistors have been measured for each device geometry and for every wafer studied.

## 3. Results and Discussion.

As shown elsewhere, pMOSFETs fabricated on sGe substrates may exhibit a significant performance improvement, whereby the highest long-channel hole mobility is found for the devices without halo, followed by the P halo transistors [13]. In the case of the 10 μm x 0.25 μm p-channel transistors of Fig. 1 receiving the same standard front-end processing, an improvement in the range of 15 to 20 % in the maximum transconductance in the ohmic regime is observed for the sGe devices, compared with counterparts fabricated on relaxed Ge-on-Si substrates. The corresponding current noise spectral density $S_I$ (Fig. 2a) and input-referred voltage noise spectral density $S_{VG}$ ($=S_I/g_m^2$, with $g_m$ the transconductance) (Fig. 2b) at a frequency f=25 Hz is quite similar for drain currents in strong inversion ($I_D$>1 μA). In weak inversion, on the other hand, the current noise power spectral density in the relaxed Ge devices is considerably higher, as has been reported before [11]. This has been attributed to the presence of a high density of TDs, which also gives rise to a higher drain-to-bulk leakage current (Fig. 3). The lower leakage current is partly related to the lower TDD. However, the main factor is the smaller intrinsic carrier concentration ($n_i$) due to the wider band gap of relaxed $Si_{0.2}Ge_{0.8}$ compared with relaxed Ge [13]. This can also contribute to a difference in the GR noise, as both the activation energy, the capture cross section and, hence, the emission and capture time constants of the dislocations can be modified. A study of the GR noise spectra as a function of temperature should clarify this issue. Here, we investigate the impact of varying the substrate bias $V_{BS}$.

*3.a. Impact of substrate bias*

As suggested previously [10],[14], more insight can be gained by studying the LF noise as a function of the substrate bias $V_{BS}$, which also modifies the drain-to-bulk current. At the same time, the channel position with respect to the interface and the halo doping profile will be modified by the substrate bias. A forward $V_{BS}$ should result in an inversion layer deeper in the substrate (higher halo concentration), while the opposite holds for a reverse substrate bias. Figure 4a and 4b represent the input characteristics and the normalized noise spectral density, i.e., $S_I/I_D^2$ versus $I_D$, respectively, for the same sGe pMOSFET at different $V_{BS}$ conditions. The drain current is highest for forward substrate bias (-0.25 V) in Fig. 4a, while the noise is highest for the floating substrate condition. However, as seen in Fig. 4b, the excess GR noise in weak inversion becomes more pronounced for the forward-substrate bias case, which also yields the highest drain-to-bulk leakage current. It again establishes a clear link between both phenomena. This higher excess noise is also found for the relaxed Ge pMOSFET in Fig. 5b.

Another important observation is that for sufficiently large $I_D$ in Fig. 4b, the normalized noise runs parallel with $(g_m/I_D)^2$ for all substrate bias conditions. This applies to a lesser extent to the relaxed Ge transistor (Fig. 5b). From this, it is concluded that the LF noise, which is predominantly 1/f-like for higher drain currents [10],[11],[14] is determined by number fluctuations [15]. This implies that from the flat-band voltage noise spectral density of ~$10^{-11}$ $V^2$/Hz, an oxide trap density $N_{ot}$ in the range of $5.5x10^{18}$ $cm^{-3}eV^{-1}$ can be derived using [15]:

$$S_{VG} = \frac{q^2 kTN_{ot}}{WLC_{ox}^2 \alpha_t f} \quad (1)$$

with q the elementary charge, k Boltzmann's constant, T the absolute temperature, W the device width and L the device length, $C_{ox}$ the gate oxide capacitance density and $\alpha_t$ the tunneling attenuation parameter, usually taken as $10^8$ $cm^{-1}$. This is quite similar to previously obtained values [16],[17] and about a factor 4 times higher than the trap density derived from the 1/f noise at the front interface of GeOI transistors [18].

*3.b. Impact of processing conditions*

Figure 6 represents the flat-band voltage 1/f noise spectral density at 25 Hz and in linear operation for a number of 10 μmx0.25 μm pMOSFETs, fabricated on relaxed or strained Ge substrates, with identical processing, i.e., wafers 5, 8 and 18 of Table I. The average $S_{VG}$ has been calculated for sufficiently large $I_D$ where the excess GR noise is negligible and is represented versus the effective hole mobility $\mu_h$ which is calculated from the slope of the Y-function [19], using:

$$\mu_h = \frac{LH^2}{C_{ox}WV_{DS}} \qquad (2)$$

In Eq. (2), H is the slope of a linear fit to the Y versus $V_{GS}$ curve. It is clear that a typical value for $S_{VG}$ is ~$10^{-11}$ $V^2$/Hz, irrespective of the substrate type. In other words, the 1/f noise which is dominant in strong inversion for these devices and governed by number fluctuations is not sensitive to the Ge-on-Si substrate type but, as will be shown below, may be significantly

affected by front-end processing steps. This also implies that the compressive strain in the sGe channel, while it improves the mobility (Fig. 6), is not influencing the 1/f-like noise. This seems to be a general fundamental tendency, namely, that the impact of mechanical strain on the LF noise is rather subtle [20,21].

Combining the noise data for all sGe processing conditions of Table I, a clear trend develops in Fig. 7 between $\mu_h$ and $S_{VG}$ which has also been noted before for sSi nMOSFETs, for example [22]. It indicates that the traps responsible for carrier scattering are also the cause of the higher 1/f-like noise. The strongest impact is found for the junction anneal: omission of the anneal apparently leads to insufficient removal of the ion implantation damage from the channel, leaving behind scattering and noisy trapping centers. It is also evident from Fig. 7 that lower 1/f noise and better medium-channel $\mu_h$ can be obtained by channel engineering and more in particular the halo processing [13]. Especially replacing As by a P halo yields a noise reduction, which could be explained by assuming a lower residual lattice damage induced by the lighter ion. Another factor could be the higher thermal budget for the annealing of the As halos (550 $^{o}$C) which can give rise to a partial relaxation of the compressive strain in the sGe layer.

Although the pMOSFETs without junction anneal have poor characteristics, a deeper analysis of the noise results may yield some better understanding of the underlying mechanisms. As shown in Fig. 8, the spectra are 1/f-like below 1 kHz in strong inversion, while the plateau of a Lorentzian, associated with defect-assisted GR noise is observed at higher frequencies. The fact that the GR noise level is not changing with gate bias indicates that the underlying defects are in the SiGe depletion region. Interestingly, when analyzing the 1/f noise part at 25 Hz for a sGe pMOSFET without junction anneal in Fig. 9, it is evident that the normalized noise is

nowhere parallel with the $(g_m/I_D)^2$ function. Instead, $S_I/I_D^2$ follows a $1/I_D$ trend, which in the past has been interpreted in terms of mobility fluctuations [14].

It is appealing to adapt this point of view, since also the hole mobility is seriously degraded, linking both phenomena: the scattering at implantation-induced defects in the channel not only causes a reduction of $\mu_h$ but also an increase in the mobility fluctuations 1/f noise. In fact, from Capacitance-Voltage (C-V) measurements on pMOSFETs without junction anneal, a high(er) hysteresis has been found, which points to a higher trap density in the gate stack and at the interface as well. These centers could also contribute to additional scattering, lowering the hole mobility and inducing more fluctuations and, hence, 1/f noise. In addition, slightly higher reverse current has been observed in p-n junctions fabricated without junction anneal, confirming a higher trap density in the depletion region.

However, for the 1/f noise in strong inversion (above $V_T$) there could be an alternative interpretation, which equally produces an $1/I_D$ dependence [9] and is based on the presence of a localized defect-related noise source in the channel. The model predicts the following relationship [9]:

$$S_I \propto \frac{g_{ch}^2 I_D^2}{C_{ox}^2 (V_{GS} - V_T)^2} \tag{3}$$

with $g_{ch}$ the channel conductance ($\sim I_D/V_{DS}$) in the ohmic regime. According to Fig. 10, the normalized noise spectral density above $V_T$ can be reasonably well described by Eq. (3), for a substrate bias of 0 V and -0.25 V. The higher 1/f noise magnitude at forward substrate bias suggests a higher contribution of the drain-to-substrate current, by the presence of non-annealed implantation-induced damage close to the drain.

In summary, Table II gives the main LF noise regimes which have been identified in the Ge pMOSFETs and what is the main technological factor affecting the corresponding spectral density.

## 4. Conclusions

It has been shown that the LF noise in sGe pMOSFETs in weak inversion is lower than for relaxed Ge-on-Si counterparts due to the lower density of TDs, which suppresses the excess GR noise. For higher drain currents, similar levels of number-fluctuations governed 1/f noise are obtained for similar front-end processing, irrespective of the presence of compressive stress in the channel. At the same time, a strong impact of the halo processing and junction anneal has been found for the 1/f noise magnitude, whereby better results have been obtained for devices with a P halo implantation compared with an As one. The role of the presence of residual ion implantation damage in the channel region close to source and drain has been demonstrated by the significantly higher noise observed for the pMOSFETs without junction anneal.

## Acknowledgments

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## Table and Figure Captions

Table I. Processing details for the different wafers studied.

Table II. Summary of the different low-frequency noise mechanisms and the estimated impact of the main processing steps investigated. JA is junction anneal.

Fig. 1. Drain current and transconductance in linear operation of two relaxed Ge-on-Si and two sGe pMOSFETs with identical processing, i.e., from wafer 5 and 8 in Table I.

Fig. 2. Current (a) and input-referred (b) noise spectral density of two relaxed Ge-on-Si and two sGe pMOSFETs with identical processing, i.e., from wafer 5 and 8 in Table I. $V_{DS}$=-0.05 V and f=25 Hz.

Fig. 3. Drain current $I_D$ at $V_{DS}$=-0.02 V and -1 V for a 10 μmx 65 nm pMOSFET fabricated in a relaxed Ge or a sGe substrate.

Fig. 4. Input characteristics in ohmic regime (a); normalized noise current spectral density and $(g_m/I_D)^2$ ratio versus $I_D$ (b) for a 10 μmx0.25 μm sGe pMOSFET, corresponding with different substrate bias conditions ($V_{BS}$=0 V, -0.25 V and floating).

Fig. 5. Input characteristics in ohmic regime (a); normalized noise current spectral density and $(g_m/I_D)^2$ ratio versus $I_D$ (b) for a 10 μmx0.25 μm relaxed Ge-on-Si pMOSFET, corresponding with different substrate bias conditions ($V_{BS}$=0 V, -0.25 V and +0.5 V).

Fig. 6. Average input-referred noise spectral density $S_{VG}$ at 25 Hz versus effective low-field mobility for 10 μmx0.25 μm pMOSFETs fabricated on relaxed Ge-on-Si (■) and sGe (◊,▲).

Fig. 7. Average input-referred noise voltage spectral density at 25 Hz versus effective mobility in ohmic regime ($V_{DS}$=-0.05 V) of 10 μmx0.25 μm sGe pMOSFETs processed with the splits of Table I. The dashed line is a guide to the eye, representing $S_{VG}$~$1/\mu_h$.

Fig. 8. Low-frequency noise spectra for a 10 μmx0.25 μm sGe pMOSFET, fabricated without junction anneal (wafer 12 in Table I), corresponding with different gate voltages.

Fig. 9. Normalized noise spectral density and $(g_m/I_D)^2$ versus drain current at f=25 Hz for a 10 μmx0.25 μm sGe pMOSFET, fabricated without junction anneal (#12 in Table I).

Fig. 10. Experimental (full lines) and calculated (dashed lines) normalized noise spectral density versus drain current for a 10 μmx0.25 μm sGe pMOSFET without junction anneal (#12 in Table I) and corresponding with a $V_{BS}$=0 V and -0.25 V.

Table I. Processing details for the different wafers studied.

| **Wafer nr** | **Substrate** | **Halo** | **HDD PAI** | **Junction Anneal (5 min $N_2$)** |
|---|---|---|---|---|
| 5 | Ge-on-Si | As | yes | 550 $^oC$ |
| 8 | 20 nm sGe | As | no | 550 $^oC$ |
| 10 | 20 nm sGe | P | no | 500 $^oC$ |
| 12 | 20 nm sGe | As | yes | no |
| 13 | 20 nm sGe | As | yes | 550 $^oC$ |
| 14 | 20 nm sGe | As | yes | no |
| 15 | 20 nm sGe | no halo | no | 450 $^oC$ |
| 18 | 20 nm sGe* | As | yes | 550 $^oC$ |

*no 1 nm in-situ doped sGe layer

Table II. Summary of the different low-frequency noise mechanisms and the estimated impact of the main processing steps investigated. JA is junction anneal.

| Noise mechanism | Bias regime | Impact substrate (TDD; $E_G$) | Gate stack | halo |
|---|---|---|---|---|
| GR noise | weak inversion | ++ | o | o |
| 1/ noise (with JA) | strong inversion | o | + | + |
| 1/f noise (no JA) | weak to strong inversion | o | + | ++ |

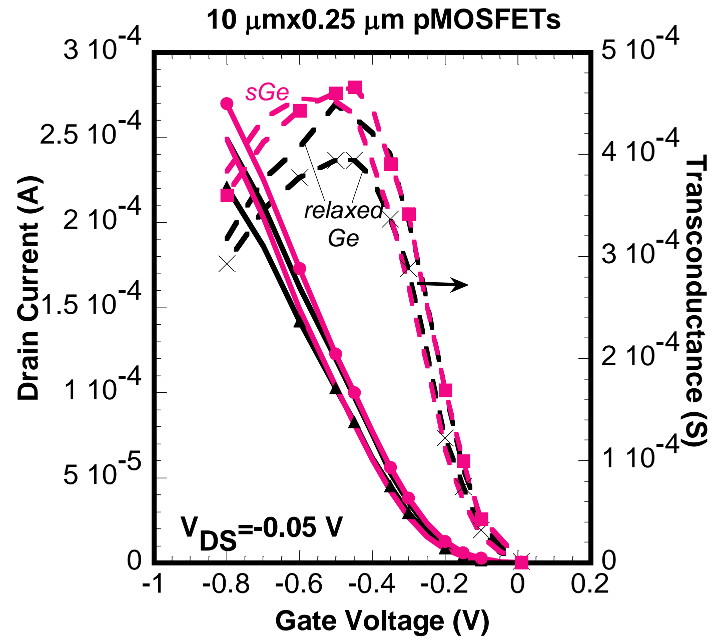


Fig. 1. Drain current and transconductance in linear operation of two relaxed Ge-on-Si and two sGe pMOSFETs with identical processing, i.e., from wafer 5 and 8 in Table I.

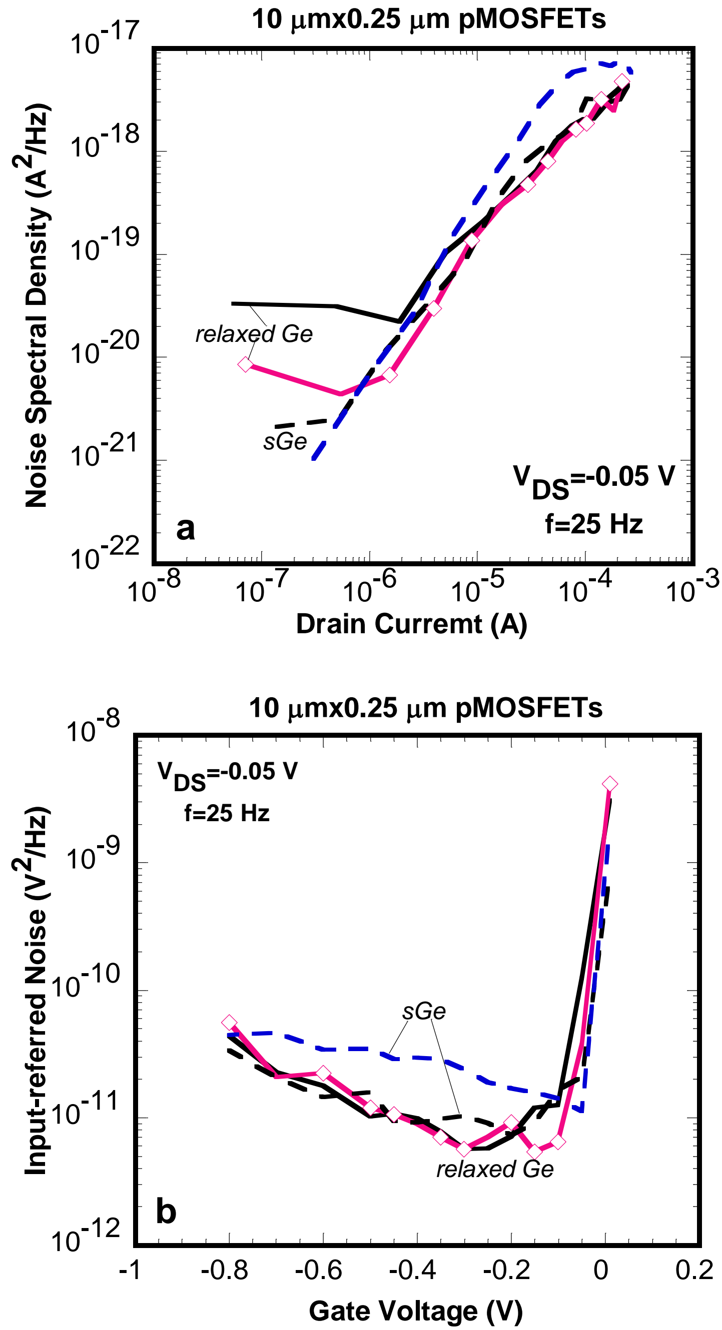


Fig. 2. Current (a) and input-referred (b) noise spectral density of two relaxed Ge-on-Si and two sGe pMOSFETs with identical processing, i.e., from wafer 5 and 8 in Table I. $V_{DS}$=-0.05 V and f=25 Hz.

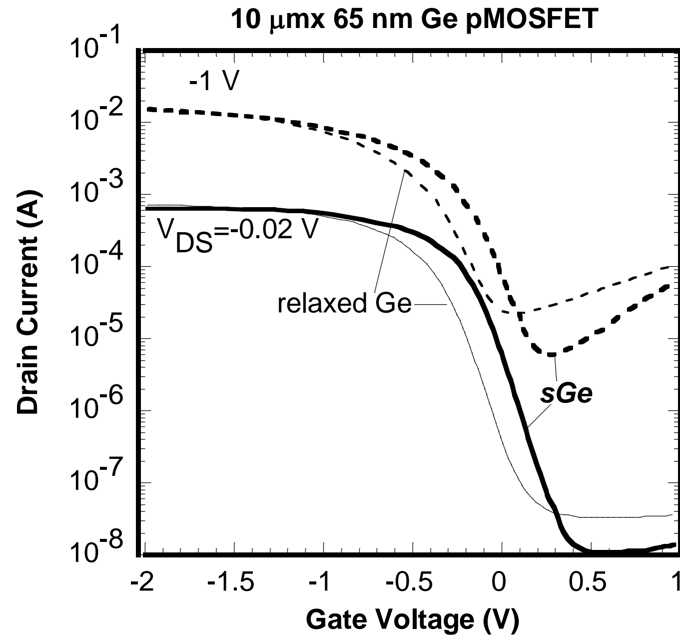


Fig. 3. Drain current $I_D$ at $V_{DS}$=-0.02 V and -1 V for a 10 μmx 65 nm pMOSFET fabricated in a relaxed Ge or a sGe substrate.

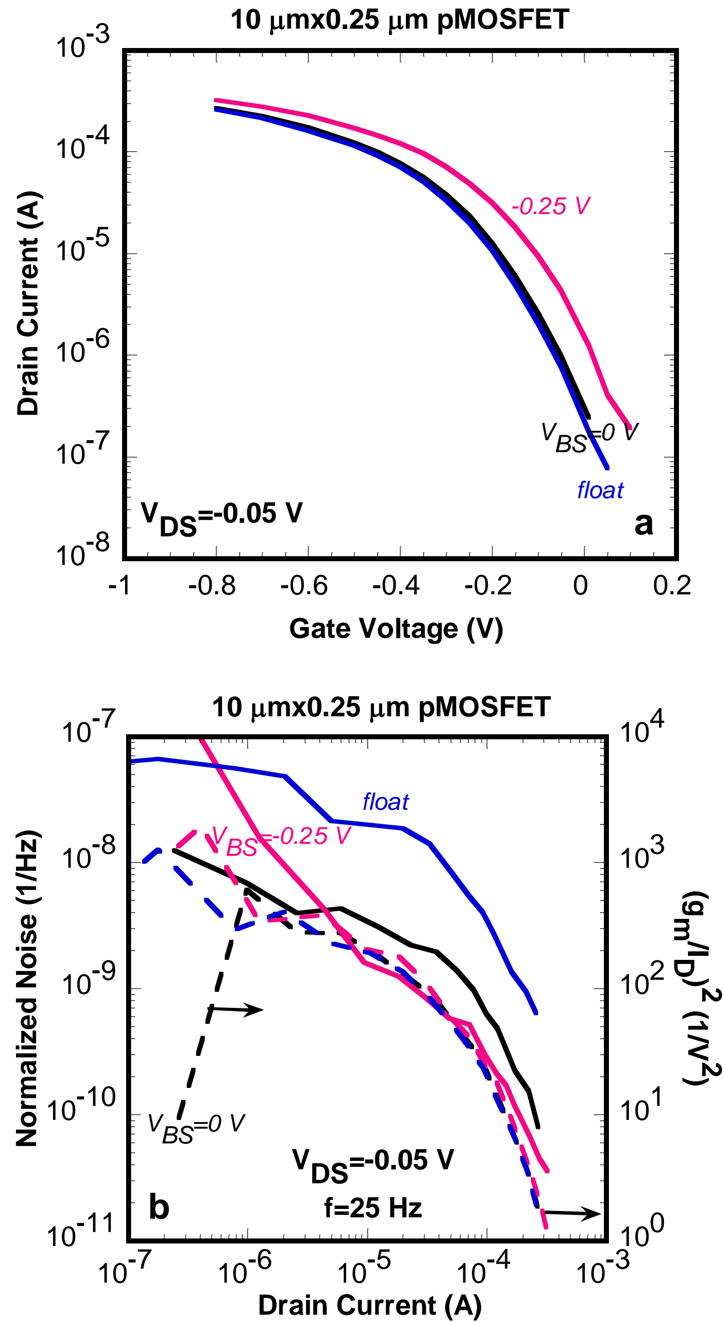


Fig. 4. Input characteristics in ohmic regime (a); normalized noise current spectral density and $(g_m/I_D)^2$ ratio versus $I_D$ (b) for a 10 μmx0.25 μm sGe pMOSFET, corresponding with different substrate bias conditions ($V_{BS}$=0 V, -0.25 V and floating).

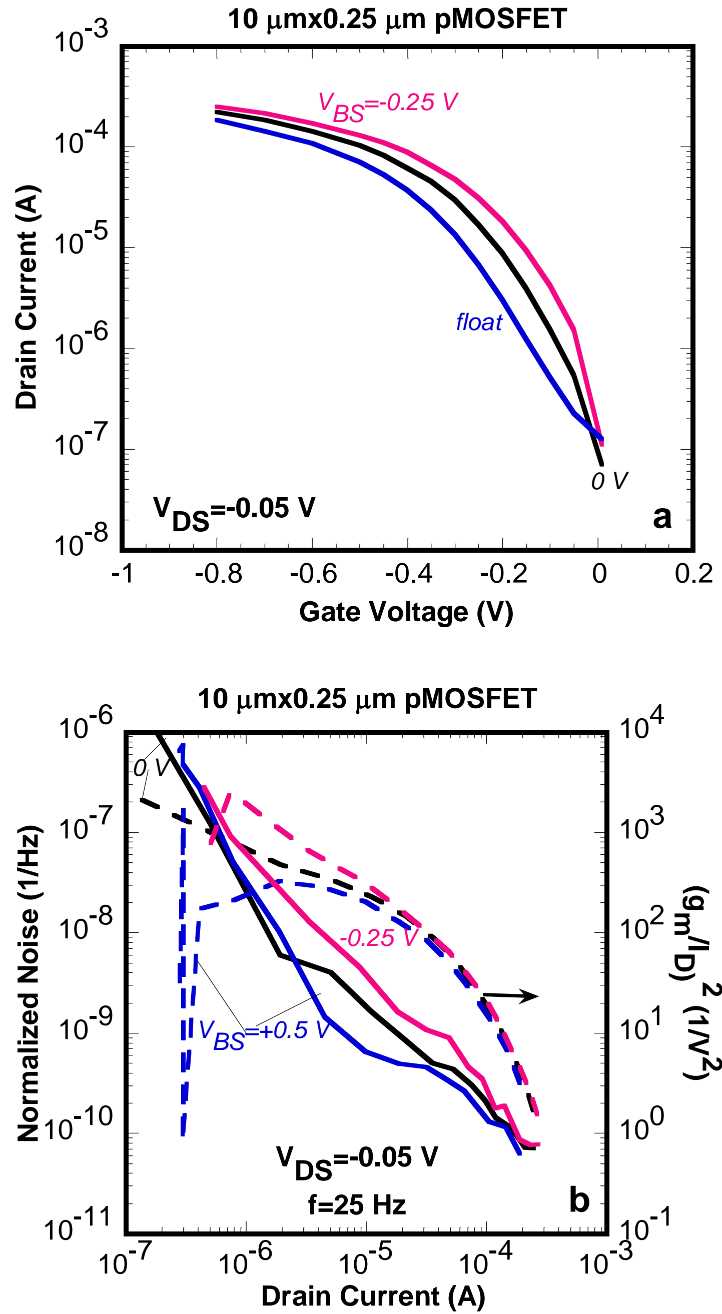


Fig. 5. Input characteristics in ohmic regime (a); normalized noise current spectral density and $(g_m/I_D)^2$ ratio versus $I_D$ (b) for a 10 μmx0.25 μm relaxed Ge-on-Si pMOSFET, corresponding with different substrate bias conditions ($V_{BS}$=0 V, -0.25 V and +0.5 V).

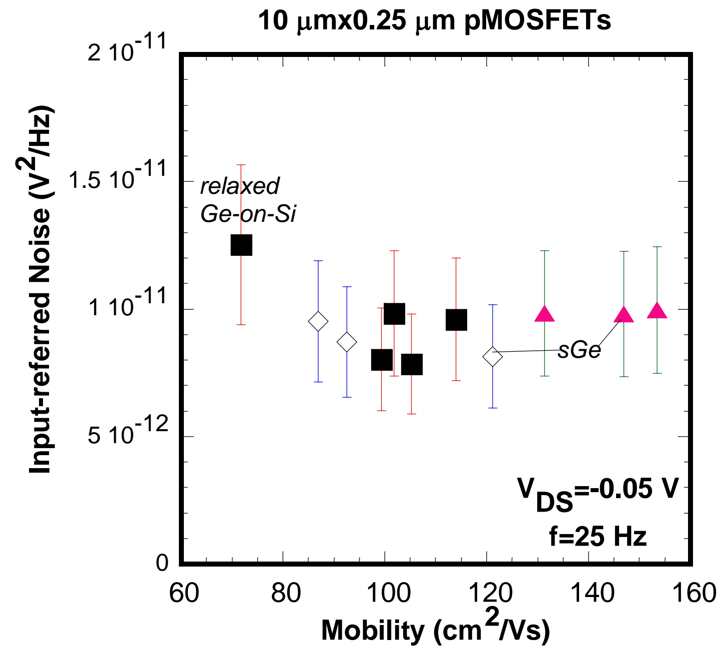


Fig. 6. Average input-referred noise spectral density $S_{VG}$ at 25 Hz versus effective low-field mobility for 10 μmx0.25 μm pMOSFETs fabricated on relaxed Ge-on-Si (■) and sGe (◊▲).

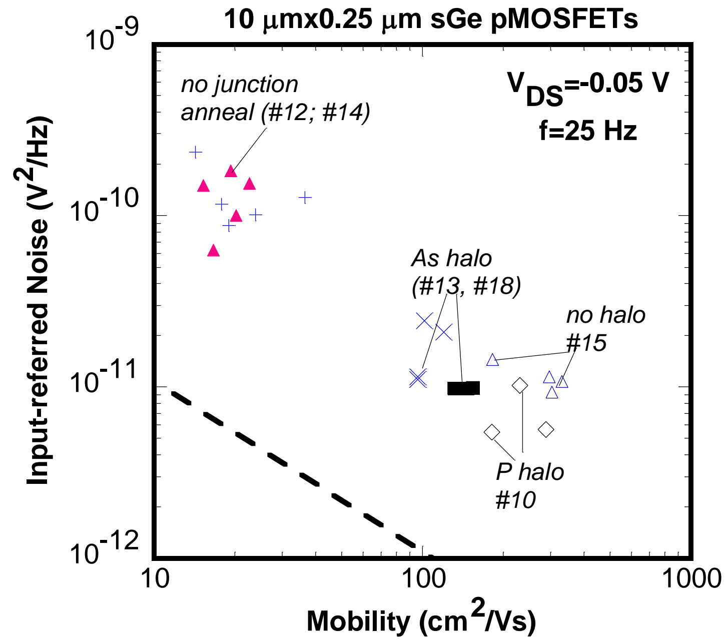


Fig. 7. Average input-referred noise voltage spectral density at 25 Hz versus effective mobility in ohmic regime ($V_{DS}$=-0.05 V) of 10 μmx0.25 μm sGe pMOSFETs processed with the splits of Table I. The dashed line is a guide to the eye, representing $S_{VG}$~$1/\mu_h$.

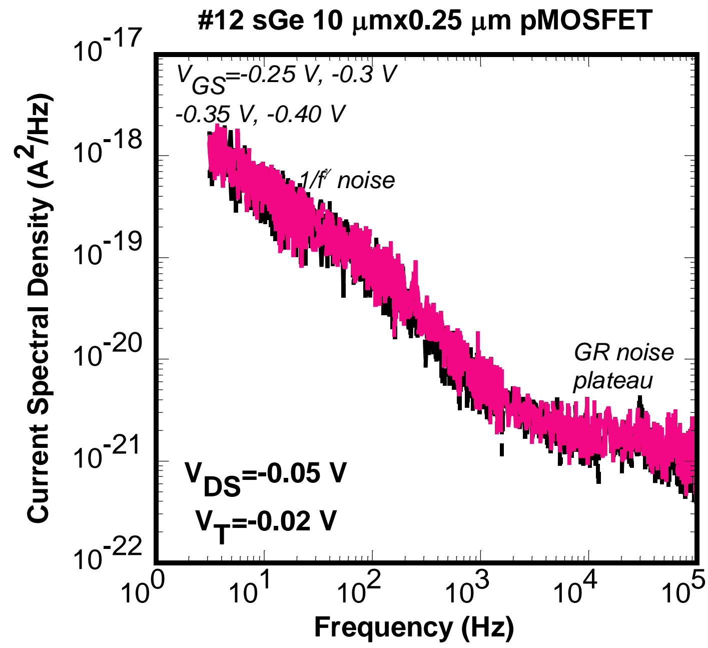


Fig. 8. Low-frequency noise spectra for a 10 μmx0.25 μm sGe pMOSFET, fabricated without junction anneal (wafer 12 in Table I), corresponding with different gate voltages.

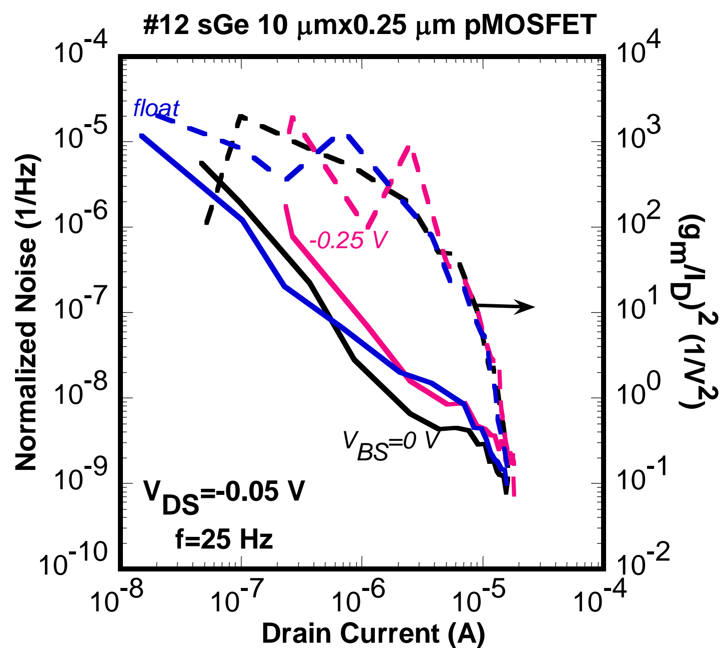


Fig. 9. Normalized noise spectral density and $(g_m/I_D)^2$ versus drain current at f=25 Hz for a 10 µmx0.25 µm sGe pMOSFET, fabricated without junction anneal (#12 in Table I).

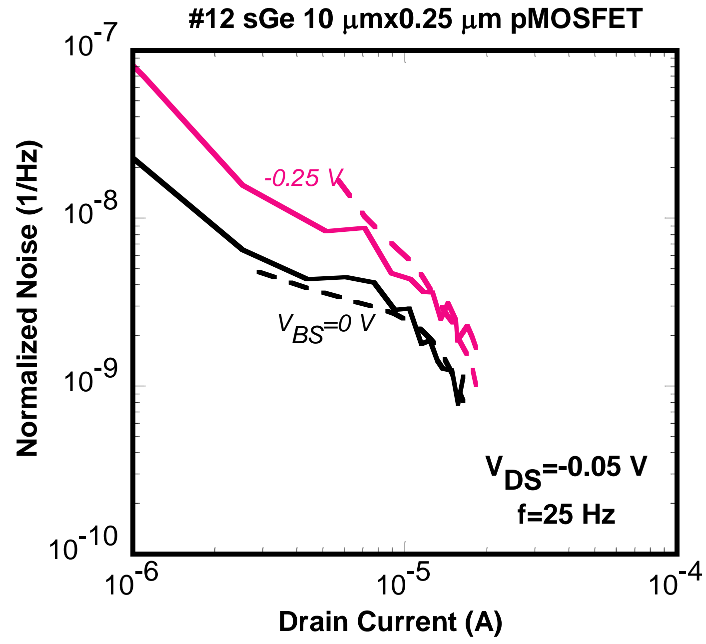


Fig. 10. Experimental (full lines) and calculated (dashed lines) normalized noise spectral density versus drain current for a 10 μmx0.25 μm sGe pMOSFET without junction anneal (#12 in Table I) and corresponding with a $V_{BS}$=0 V and -0.25 V.