POWER-CONTROL DESIGN OF RESONANT CONVERTERS

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Daddy, will you ever know that I have finished my study?

Chiew, please forgive me for putting you through all the suffering and stress over the past three years...

Declaration

The work presented in this thesis is, to the best of the author's knowledge and belief, original and the author's own, except as acknowledged by reference or otherwise. None of the material contained in this thesis has been previously submitted, either in whole or in part, for a degree at the University of Warwick or any other institutions.

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List of Publications

1. H. Pollock, C. L. C. Fu, and C. Pollock, "Load-resonant converter with zero-current switching and variable output power," *Electronics Letter*, vol. 33, no. 25, pp. 2081–2082, Dec 1997.

2. C. L. C. Fu and J. O. Flower, "Load-resonant converter design modification using circuit-scaling laws," *IEE Electronics Letter*, vol. 35, no. 12, pp. 953–955, June 1999.

3. C. L. C. Fu and J. O. Flower, "Power control of converters using novel resonant techniques with applications," in *The 34th Intersociety Energy Conversion Engineering Conference*, Vancouver, BC, Aug. 1999.

4. C. L. C. Fu and J. O. Flower, "Design of electrical circuits using the Gröbner Basis techniques with particular reference to load-resonant converter applications, Part I– Introduction," being reviewed for IEEE Transactions on Circuit and Systems–Part 1

5. C. L. C. Fu and J. O. Flower, "Design of electrical circuits using the Gröbner Basis techniques with particular reference to load-resonant converter applications, Part II– Load-resonant converter synthesis," being reviewed for IEEE Transactions on Circuit and Systems–Part 1.

6. C. L. C. Fu and J. O. Flower, "Outline of Gröbner Basis technique with an Engineering Application," being reviewed for IEE Electronics Letters

Contents

List of Tables

List of Figures

Abstract

Novel design techniques are presented for load-resonant and quasi-resonant converters for use in, for example, arc-welding and fan-load power supplies. Both converters are capable of very high switching frequency over a wide range of output power, with high efficiency and the presentation of near-unity power factor to the primary power supply.

Previous work, by the author and his colleagues, has produced a frequency-domain approach to produce circuit-designs for use in load-resonant converter applications. This design technique, although simple and straight-forward to understand, suffers by requiring some rather tedious trial-and-error algebraic and arithmetic manipulations albeit computer assisted. In this thesis, a systematic way of designing such circuits, based on Gröbner Basis ideas, is explained, developed and compared with the previous best-practice design method. By employing the Gröbner Basis techniques to synthesize electrical circuits, an entirely novel approach to the design of series-parallel load-resonant converter circuits is presented. This has led to the formulation of a new output-power control methodology in the design of the converters. These techniques produce output-power-control designs that have superior properties, compared with other established methods, in the sense of their simplicity, robustness and flexibility.

It is found that the methodology can be further extended to alter any resonant circuits and, hence enables multilevel-output power to be controlled without involving complex control and advanced mathematical theories, while still preserving the desirable characteristics of resonant switching. The technique is, in fact, far more generally useful in the circuit-design/synthesis arena than the specific load-resonant-converter application for which it was developed.

The novel technique used to vary the speed of an induction motor is found to be promising. Various test results are presented based on an experimental system.

Chapter 1

Introduction

1.1 High-power Solid-state Switching

The essential function of power converters is to achieve desired power conditioning in electrical systems. In any power conversion process, it is hoped to have a system that has the smallest internal power loss during energy conversion hence highest efficiency. These cannot be done using linear electronics. Thus, power conversion electronics always uses switching techniques in its operation. However, this imposes a lot of restrictions on those conventional hard-switching power supplies. The situation becomes worse when high power and high operating frequency are required simultaneously. This is because conventional hard-switching power conversion does not only radiate electromagnetic energy, it also creates a lot of unwanted harmonics at high frequency giving rise to a supply problem. Size and weight become other issues particularly as a complex cooling system will be needed. If soft-switching can be employed, then many of the electrical problems can be avoided or eliminated, and cooling requirements are reduced. Soft-switching is generally defined as switching the solid-state components between on and off states at zero-current and/or zero-voltage conditions in order to reduce the power dissipation to a minimum.

The increasing popularity of soft-switching is demonstrated by the research that is being done not only to improve on the design and control techniques, but also to optimize the solid-state devices for resonant switching [1,2].

One of the attractions in soft-switching applications is demanded in pulse-switching for industries like welding [wel,], laser [las,], marine [mar,], battery [bat,], and so on, where some good progress has been made. The assignment that the author's colleagues took on some eight years

ago was to design a welding power-supply equipment that is able to operate at high-switching frequency and to present unity power-factor to the primary supply. This was done using soft-switching techniques.

1.2 Control of Output Power

In the assignment, most of the existing power control methods of resonant converters are not adopted as they face one main problem, i.e. not switching at true resonance due to the employed control algorithms [3–5]. *Resonance* in this thesis is defined as fundamental current and voltage waveforms being in phase.

1.2.1 Original Approach

A new type of power control of resonant converter was hence proposed by Pollock and Flower [3–5]. The power supply incorporates a series-parallel load-resonant converter, inherently capable of restricting short-circuit current and open-circuit voltage. It was intended for the use of arc-welding equipment. These authors have proven the capability of the power converters in efficient operation over a wide range of output power exploiting distinctive multi-resonant frequencies.

The analysis of the series-parallel load-resonant converter was based on *Small Signal Analysis* in the frequency domain, instead of the time domain which has invariably been the main approach of conventional methods like *State Space Analysis.*

The frequency approach enables the characteristics of the converter to be formulated in a fairly simple way, and hence it yields a set of equations reflecting the number of passive elements. Design mathematics was then developed by solving the characteristic equations simultaneously. The design mathematics allows the series-parallel load-resonant converter to be designed with specific resonant frequencies. The authors also claimed that different power levels can be specified during the design process. This formed the basis of the output-power-control method for the resonant converters of this type.

The main advantage of the new power-control method is that the power delivered to the circuit, and hence the load, varies depending on which turning-point frequency the circuit is excited at.

1.2.2 Limitations of Original Approach

The initial design technique, although simple and straight-forward to understand, suffers from requiring some rather tedious trial-and-error manipulations, especially in obtaining different specified

output powers.

It can be seen from [3], that the final desired design was obtained only after several trial-and-error calculations using an interactive computer program.

In addition, there was not much flexibility and controllability of the design algorithm in obtaining varied-output power. The hard-won designs had to be re-designed from the beginning each time even if quite small changes for the resonant converter were required. The design process would not be realistic to proceed with even if the topology becomes slightly more complicated.

From a practical point of view, this method is tedious and time-consuming. Further, it is shown later in this thesis that the solving-simultaneous-equations approach was almost impossible to use when specifying the change of the output-power, causing a major disadvantage. Therefore, a more efficacious, systematic, less-time consuming and, preferably, general method was sought for implementing the design process. It is the development of such a method that is the main contribution described in this thesis.

1.3 Breakthrough Approach

It is the wish to control the output power of resonant converters in a systematic way by being able to specify the different power levels at different corresponding multi-turning-point frequencies, for which a solution is sought. A further desirable goal was to do this in the frequency domain as this is the preferred domain for most electrical engineers.

1.3.1 Novel Design and Power Control Methods

The afore-mentioned aims have been successfully achieved by employing a fairly general approach to electrical-solving methods using mathematics based on the *Gröbner Basis* theory(GB) together with the maxim of letting-the-computer-do-the-work, as far as is possible.

Although the GB methods are not well-known among power electronics engineers, and have their origins in the field of abstract algebra, this hardly matters since programs for doing the associated computational work are readily available in computer libraries.

The essence of the basis lies in the manipulation of polynomials, which will be explained in Chapter 5. These present the problem from both the algebraic and geometrical views. The outcome from using the GB methods is the resonant-converter can now be designed in a systematic, less-time consuming and much simpler way. The converter, as before, is analyzed in small-signals in order to obtain the governing equations of the system. Then the GB theory is used to represent the original

characteristic equations by a simpler and more suitably defined form for possible solutions. This leads to the successful implementation of prescribed output-power changes in the practical system.

The advantages of using this new approach in achieving different output power changes in resonant converters, and yet maintaining the main characteristics of resonant converters, which are operating at true zero-current switching with unity power-factor, are,

- it is a efficacious, systematic, easier and less time-consuming approach,
- increased flexibility and controllability of the design algorithm,
- it can be used for any series-parallel load-resonant topology independent of the complication of the system.

However, the main disadvantage of the GB approach is that to understand it properly, a good understanding of some elements of abstract algebra is needed, and its use, in practice, requires systematic programming techniques to be employed. Not with standing this, having no more than cursory knowledge of these things, allows the use of computer-library routines to be used.

1.3.2 Further Development

The above GB approach was further proven to be a general approach to designing any resonant converter. In addition, output power control without involving complicated feedback loop was successfully implemented using *quasi-resonant converter* on a single-phase induction motor. Modifications of the resonant profiles were also attempted to further improve the performance of the resonant converters.

It should also be stressed that the use of the GB method is not confined to converter-circuit design but can be applied much more generally in electric circuit analysis and synthesis.

1.4 Author's Principle Contributions

The principle contributions of the author in the research work described in this thesis are

1. a thorough classification of resonant converters to an extent never attempted before.
2. the severe limitations of the simultaneous-equation-design procedure while pre-specifying major frequencies of resonant converter were identified. This was shown to be mathematically infeasible and unrealistic to proceed on topologies more complex than the analysis, done by the previous authors [3–6].

3. A new systematic approach, i.e. the *Gröbner Basis* theory, in solving the series-parallel load-resonant converter has been successfully pioneered. The author is unaware of such theory being used in load-resonant-converter designs, or, indeed , network design generally.
4. The GB analysis approach enables the author to develop a simple control method for moving between different output-power levels. This can be done with zero-current switching, presenting near-unity power-factor to the electrical supply and achieving inherent short-circuit and open-circuit protection. More complex circuits, involving more components are readily dealt with.
5. A simple output power control technique leading to variable speed control of a single-phase induction motor was developed successfully. However, more development work is necessary before it is ready for industrial applications.
6. Different modifications of the output performance based on conventional, or novel, methods were adapted, together with the GB theory, to ease and improve the design, building and implementation of resonant converters for industrial applications.

To complete the introduction, a mention of the content of each of the other chapters follows.

Chapter2 Basic Elements involved in Resonant Converters

This chapter outlines the basic principles of resonant converters, starting from various definitions of simple series- and parallel-resonant circuits. Some common semiconductor devices are also presented as they are really the enabling members of converter system.

Chapter3 Classifications of Resonant Converters

A thorough classification of almost all the available resonant converters is given. It is believed that it was high time that such a review was performed.

Chapter4 Impedance Concept and Frequency-domain Analysis

Existing power control and analyses of resonant converters are covered in this chapter. The solving-simultaneous-equations method for analyzing series-parallel load-resonant converters using the impedance concept presented in [3–5] is reviewed in this chapter. Limitations of the method are shown mathematically by taking, as an example, the design of a converter.

Chapter5 The Gröbner-Basis Techniques for Power Control

This is the key chapter of the thesis. This chapter is devoted to presenting the GB technique for solving problems associated with polynomial expressions, and to show, by simple examples, how the technique is useful in the solution of some electrical circuit problems without involving an intensive mathematical explanation. The GB is then applied in serious applications to some

problems found in dealing with the design of resonant circuits for series-parallel load-resonant converters. Simulations results are presented and are compared with the experimental results shown in references [3–5]. This is then followed by the use of the GB in some other different resonant topologies.

Chapter6 Hardware Techniques for Power Control

A new method in controlling quasi-resonant converter to deliver substantial output-power change to achieve variable speed control of induction motor is outlined in this chapter. Practical results are shown. The technique employed shows great promise but needs further development.

Chapter7 Modifications of Performance Profiles

This chapter discusses different conventional and novel techniques employed to ease the design, building and implementation of resonant converters in order to improve the performance and efficiency of the converters.

Chapter8 Conclusion

This chapter draws the conclusions from each of the principle contributions offered from the research work. In additions, discussions of the employed techniques in showing great promise potentially in reducing the weight and size of equipments are also given. Potential future research work is outlined.

Chapter 2

Basic Elements involved in Resonant Converters

2.1 Introduction

Interests in resonant converters arose from the quest for utilizing very high switching frequencies without unacceptable power dissipation in the semiconductor switches. Switching losses can be minimized using resonant system and also very high operating frequency can be employed allowing smaller and lighter power-conditioning equipments to be built. In addition, power density and efficiency of the power conditioning can be increased while reducing the EMC problems [7–11]. The characteristics of resonant converters were analyzed, and were proven having higher power densities and better power factor than conventional converters in [Schutten et al., 1992, Schutten et al., 1998].

The power dissipation in a switch will be zero if either the voltage across the switch or the current going through it is zero during the switching transitions. In resonant circuits, the resonant tank, comprising inductor(s) and capacitor(s), resonates in order to make the current and/or the voltage automatically go through zero at the instants of switching resulting in soft-commutation.

Interest in resonant switching techniques probably arose from attempts to improve high-power SCR converter performance. These have to be turned off by keeping the current through them below a threshold level, to effectively achieve zero-current switching, via an auxiliary 'resonant' circuit that commutates the thyristors [12], [Brambilla, 1999].

Before discussing basic resonant circuits, both the conventional and soft-switching converters are reviewed briefly. This is followed by the discussions of switching conditions.

2.2 Conventional-switching principles

Before the utilization of resonant power converters, there were two essential ways for delivery of electric power from a source to a load in a controllable way, i.e. *linear power conversion* and *switched-mode power conversion.*

The former usually consists of essentially linear dissipative elements and the load, e.g. a basic transistor amplifier. It is highly inefficient even in its ideal form because of the power difference between the output and the input. The basic switched-mode power converter has a switch, in parallel with a capacitor, and the load. By controlling the duty ratio of the switch, more efficient power flow can be obtained by on-off switching of the control devices. The efficiency of the power converter depends very much on the component counts [13].

The forced-commutation means, used in the switched-mode power converters to control the power regulation and transfer process, causes two significant types of problems. The first is the energy dissipated in the switches. Switching loss is encountered during the switching transitions where the current flowing in the switch overlaps with the voltage across the switch due to the finite time associated with the turn-on and turn-off of the switching element. This is depicted in Fig. 2.1 [14]. At turn-on, the device current rises beyond the load current, I_{on} by an amount of I_{rr}, the reverse-recovery current of the freewheel diode. The switch continues to sustain the full-off state voltage while the current is rising, and the voltage across the switch falls only when the diode recovers a reverse blocking capability. At turn-off, the switch voltage rises to the off-state level before the switch current subsides. The current flowing through the switch will be transfered to flow through the diode. There are dissipation losses in the switch due to overlap of voltage and current at the switching instants, and in the diode due to the reverse-recovery transient. The faster the switching frequency, the higher the losses. The rapid change of the switching waveforms causes high electromagnetic radiation.

The second type of the problem is the generated noise caused by virtually unlimited rates of voltage and current changes. The very-high rate of change of current, i.e. $\frac{di}{dt}$, at transistor turn-on gives rise to a high-peak reverse-recovery current. Turn-off noise can be reduced by employing load-line snubber. Furthermore, rapid rates of change in both the voltage and current (the switches are chopping) emits electromagnetic, or EM, radiation. Consequently, there are serious limitations on operating frequencies. Moreover, low-power density and low efficiency of the equipments are undesirable [14, 15].

The three switching loci of resonant, switched-mode and switched-mode with snubbers are

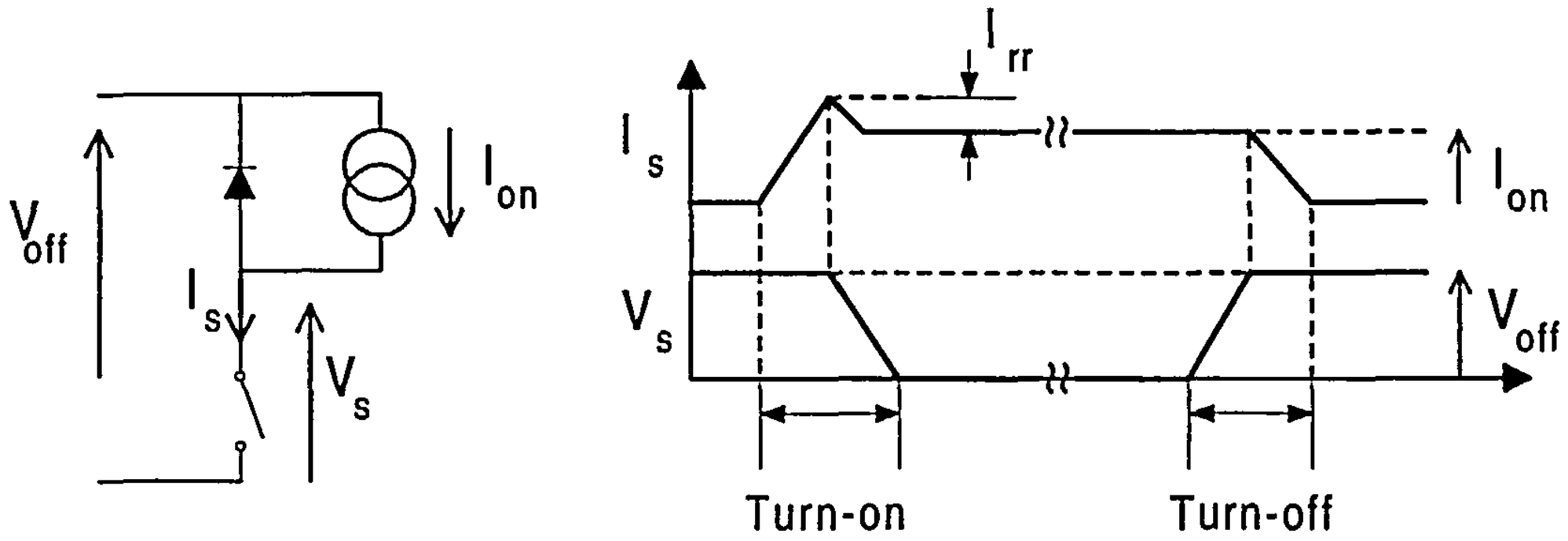

Fig. 2.1: Switching waveforms of conventional switch

depicted in Fig. 2.2 [7]. It can be seen that the load-line trajectory of the hard-switching crosses the high-stress region where the semiconductor devices are subjected to high voltage and current for inductive turn-off and capacitive turn-on. When the snubbers are used, the stress on the switches are minimized. It is also clear that resonant switching operates nearest to the zero-voltage and zero-current areas as its load-line trajectory moves along the axis to avoid high voltage and high current being excited simultaneously.

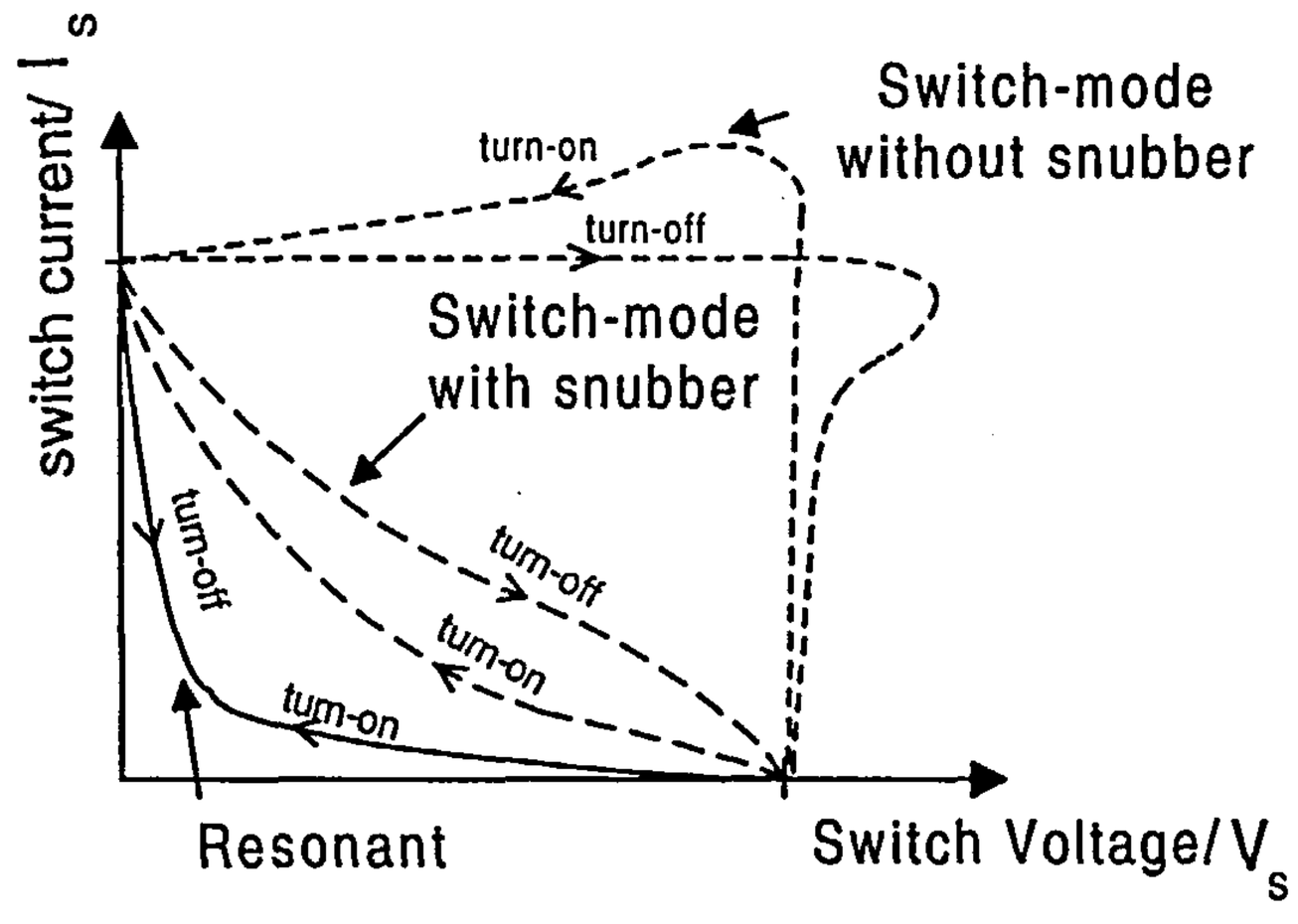

Fig. 2.2: Switching loci of resonant, switched-mode and switch-mode with snubbers

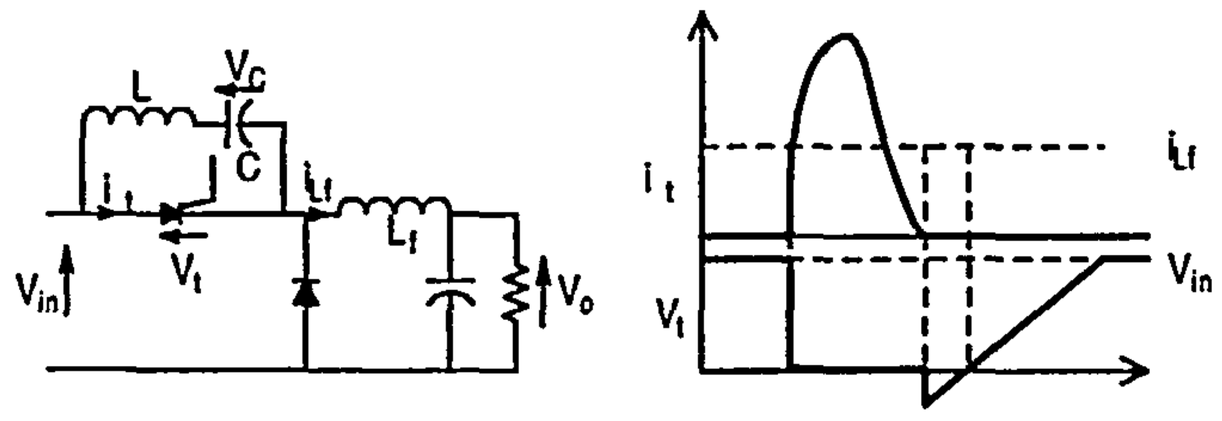

Fig. 2.3: Buck converter and its waveforms of zero-current switching

2.3 Resonant-switching Principles

Zero-current Switching/ZCS

From the waveforms depicted in Fig. 2.3 [16], the switch current is forced to rise at the instant of switch turn-on. It suffers from high turn-on transient similar to the hard-switching, and a severe reverse-recovery transient of the freewheel diode which is usually used in the resonant circuit. At turn-off, the device current crosses zero naturally giving rise to zero-current switching. However, there are losses in the body diode at that instant. The negative spike at turn off is due to the switching-on of the switch while its anti-parallel body-diode still conducts.

Zero-voltage Switching/ZVS

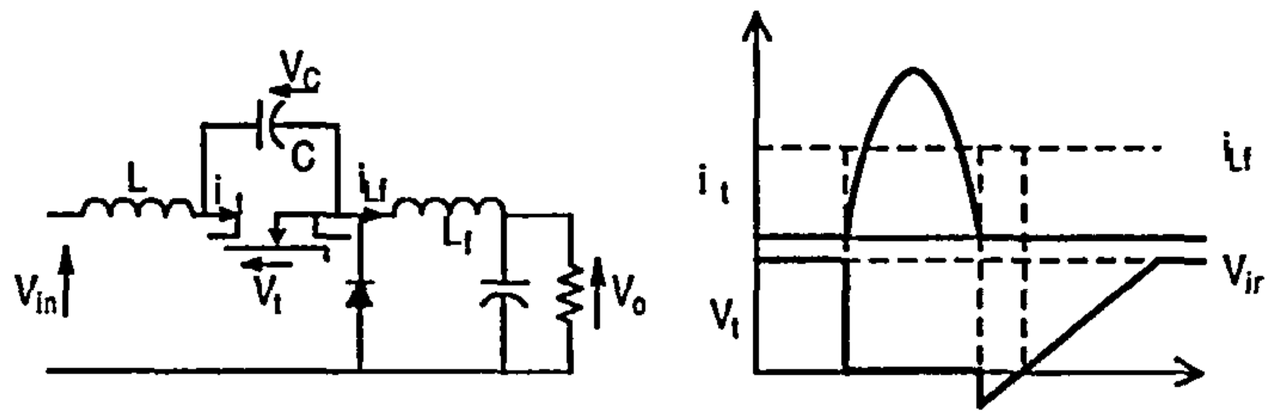

Fig. 2.4: Buck converter and its waveforms of zero-voltage switching

The zero-voltage switching is illustrated in Fig. 2.4 [16]. At the instant of switch turning on, the device current rises from zero eliminating turn-on loss. At turn-off, turn-off loss in the device is minimized to a low value by a suitable choice of resonant capacitor value as the turn-off transient in the freewheel diode is softened.

Zero-current switching vs. Zero-voltage switching

Generally, ZVS is less lossy compared with ZCS as ZVS allows all switching losses to be controlled, diode reverse-recovery is softened and the rates of the change of voltage and current at switching

instants are limited. In contrast, ZCS suffers from switching stress at turn-on and unconstrained rates of change of voltage in the switching waveforms. This not only gives rise to power losses, but also leads to high-frequency parasitic oscillations between capacitances and circuit inductances thereby creating EMC problems.

It is believed that MOSFET devices are well suited to ZVS due their short current fall-time at turn-off without exhibiting long current-tail. However, this is not really the case for IGBT devices which exhibit long current tail at turn-off. Thus, a big snubber capacitor is usually used to suppress the turn-off losses which may result in high energy handling on the circuit. Even so, it is still better than hard-switching [16].

2.4 Basic Resonant Circuit Concepts

2.4.1 Series Resonant Circuit

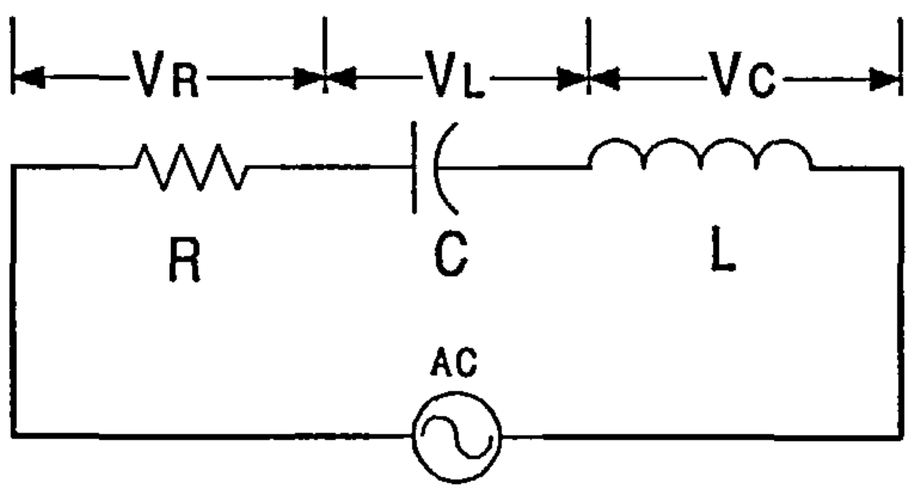

Fig. 2.5: Simple series R-L-C circuit

Graphical Representation of Resonance

If an alternating voltage at constant magnitude is applied to the circuit in Fig. 2.5 of various frequencies, the variations of resistance, inductive reactance, X_L, and capacitive reactance, X_C, with frequency, are shown in Fig. 2.6 [17].

- Resistance, R, is independent of frequency, f, which is shown as a straight line, and it is the effective impedance at resonance.
- Reactances
  - Inductive Reactance, $X_L = \omega L = 2\pi f L$, increases linearly with f.
  - Capacitive Reactance, $X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$, varies inversely with f, and it is shown as rectangular hyperbola in the fourth quadrant.

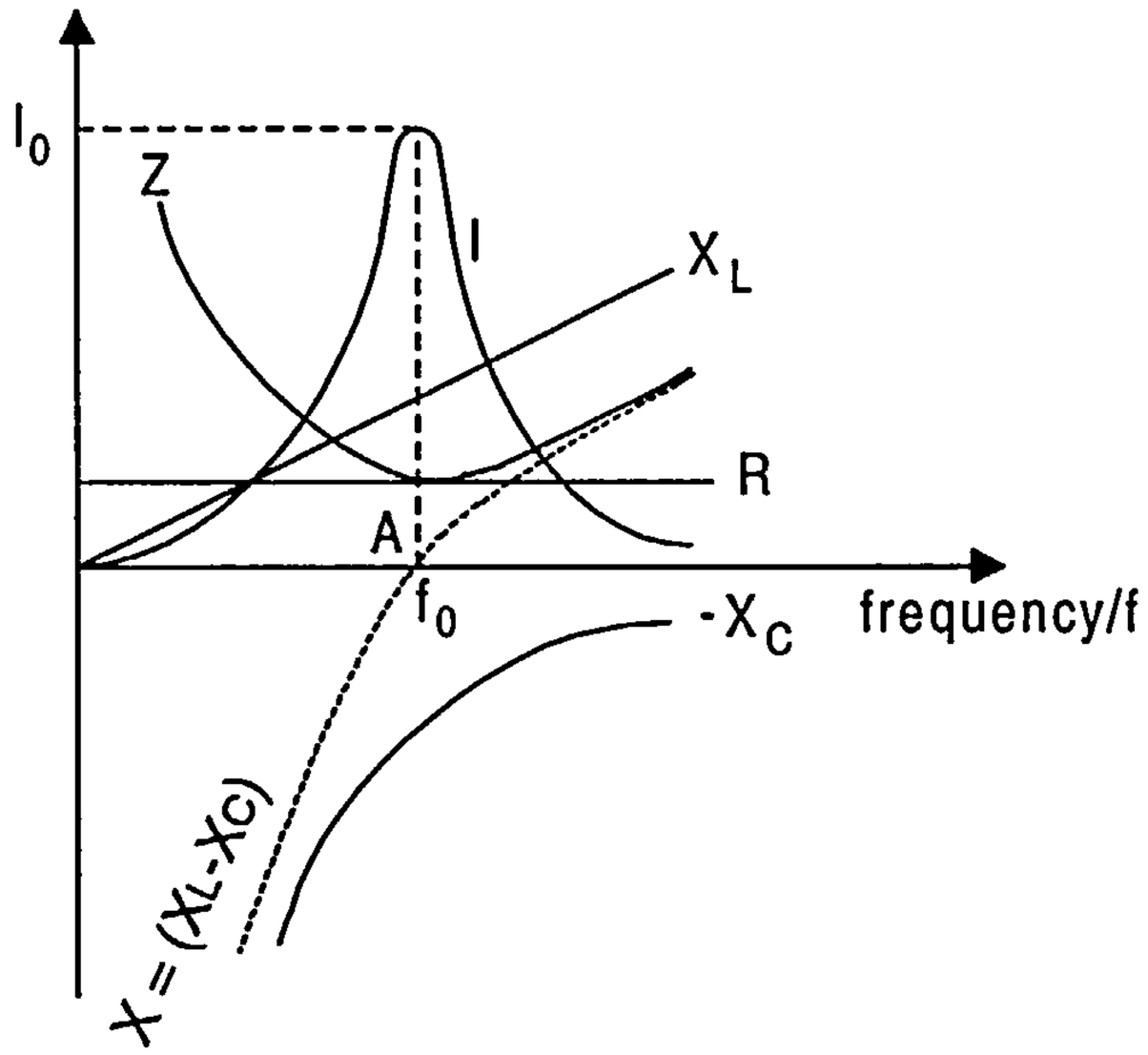

Fig. 2.6: Variation of reactances, X_L, X_C; resistance, R; input impedance, Z; and input current, I with frequency

– Net Reactance, $X = X_L - X_C$, a hyperbolic[1] curve, crosses the X-axis at point f_0, which is called the *resonant frequency.* At resonant frequency, the net reactance, X, is equal to zero due to the cancellation of X_L and X_C because they are 180^0 out of phase. Thus, the circuit appears purely resistive, i.e. the total input circuit impedance, $Z = R$, and the resonant frequency is given by $\omega = \frac{1}{\sqrt{LC}}$. If there is no resistive element in the circuit, then the current would thereby go to infinity at resonance.

- Impedance, $Z = \sqrt{R^2 + X^2}$, approaches infinity at low frequencies, and it is the lowest at resonance. As $X_C > X_L$, the net impedance is capacitive and the power factor is leading when $X_L > X_C$, the net impedance is inductive, and the power factor is lagging. The power factor is unity when $X_L = X_C$.

- Current, I, has maximum value at resonance, where it is the ratio of input voltage, V to resistance, R, and it is denoted by I_0. At resonance, this circuit would take the maximum current, and as such it is called an *acceptor circuit*, and the series resonance is often referred to as *voltage resonance.*

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[1]This can be proved by $ax^2 + bxy + cy^2 + dx + ey + f = 0$, where $D = b^2 - 4ac$; if

$$\begin{aligned} D &= 0, \text{parabola} \\ &> 0, \text{hyperbola} \\ &< 0, \text{ellipse} \end{aligned}$$

In this case, $(C)X\omega - (LC)\omega^2 + 1 = 0 => ax^2 + bxy + cy^2$ and $C^2 - 4(0)(LC) > 0$

Bandwidth

Bandwidth of resonant circuit is defined as the *band of frequencies lying between two points on either side of the resonant frequency, f_0, where the current at both points falls to $\frac{1}{\sqrt{2}}$ of its maximum value at resonance.* Narrower the bandwidth, higher the selectivity or sharper the resonant curve of the circuit and vice versa. This bandwidth, AB, from Fig. 2.7, is given by, $\triangle f = f_2 - f_1$. Over the bandwidth range, the current is equal to or greater than $\frac{I_0}{\sqrt{2}}$.

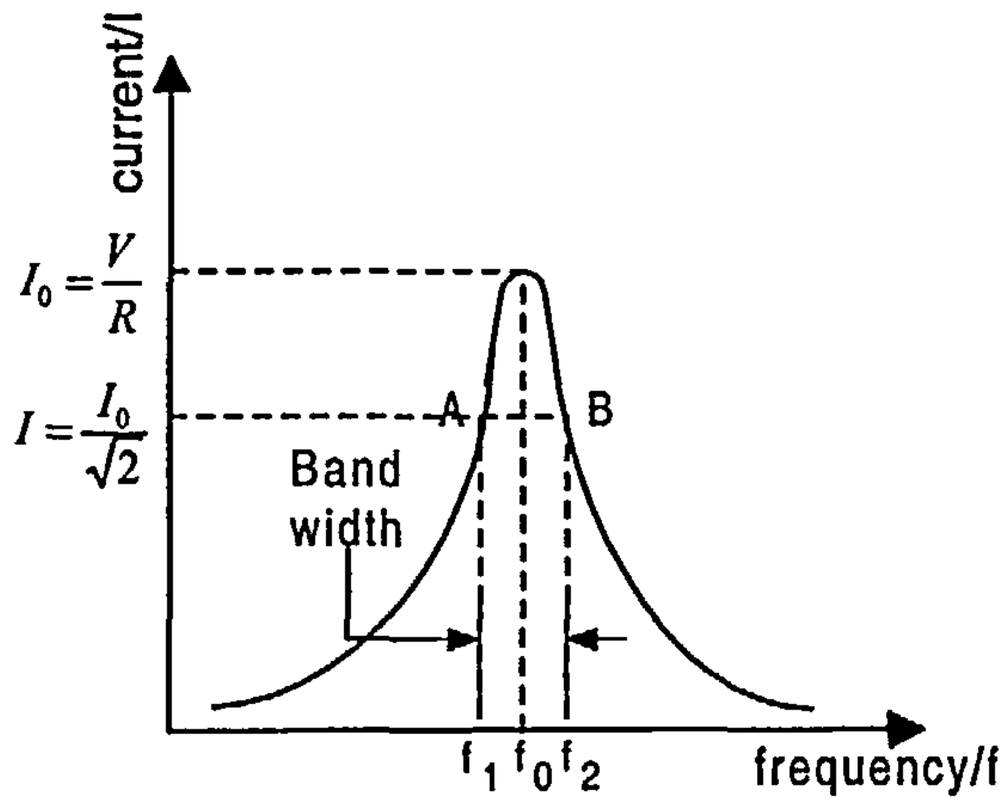

Fig. 2.7: Bandwidth of resonant circuit

Points A and B are referred to as *half-power points*, because the power at these two points is $P_{f_1} = P_{f_2} = I^2R = (\frac{I_0}{\sqrt{2}})^2R = \frac{1}{2} \times$ power at resonance. At half-power points, the net reactance is equal to the resistance. This can be proved by manipulating equations of currents at resonance, at any frequency and at half-power points, which are $I_0 = \frac{V}{R}$, $I = \frac{V}{\{R^2+[\omega L-1/(\omega C)]^2\}^{\frac{1}{2}}}$ and $I = \frac{I_0}{\sqrt{2}}$ respectively. Frequencies at these two points are $f_1 = f_0 - \frac{R}{4\pi L}$ and $f_2 = f_0 + \frac{R}{4\pi L}$.

Quality Factor, Q

Q-factor can be defined as *the voltage magnification in the circuit at resonance*, which is Q-factor $= \frac{V_L}{V} = \frac{X_L}{R} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} = \frac{Z_0}{R} = tan\,\phi$. Q-factor also equals $2\pi \frac{\text{maximum stored energy}}{\text{energy dissipated per cycle}} = \frac{\text{reactive power}}{\text{active power}}$.

The higher the Q-factor, the higher the voltage magnification and also the higher the selectivity.

2.4.2 Parallel Resonant Circuit

Fig. 2.8 shows the simple parallel L-C-R circuit.

Graphical Representation of Resonance

If an alternating voltage of constant magnitude is applied to the circuit in Fig. 2.8 at various frequencies, the variations of conductance, inductive susceptance, B_L, and capacitive susceptance, B_C, with frequency, are shown in Fig. 2.9 [17].

- Conductance, the reciprocal of resistance, $\frac{1}{R}$, is independent of frequency, f, which is shown as a straight line, and it is the effective impedance at resonance.
- Susceptances
  - Inductive Susceptance, $B_L = -\frac{1}{X_L} = -\frac{1}{\omega L} = -\frac{1}{2\pi f L}$, is inversely proportional to the frequency of the applied voltage, and it is shown as rectangular hyperbola in the fourth quadrant.
  - Capacitive Susceptance, $B_C = \frac{1}{X_C} = \omega C = 2\pi f C$, increases with increase in the frequency of the applied voltage. It is therefore represented by a straight line drawn in the first quadrant.
  - Net Susceptance, $B = B_C - \frac{1}{B_L}$, a hyperbolic curve represented by the dotted line in Fig. 2.9, crosses the X-axis at point f_0 when the system is at resonance. At resonant frequency, the net susceptance, B is zero. Hence admittance is minimum, and it is equal to the conductance, G. This causes the line current at point A to be minimum. Inductive susceptance predominates below resonant frequency corresponding to point A, and thus line current lags behind the applied voltage. However, for the frequencies above resonance, capacitive susceptance predominates and, consequently, line current leads. Net susceptance is given by, $\frac{1}{X_C} = \frac{X_L}{Z^2}$, or $X_L \times X_C = Z^2$, or $\frac{L}{C} = Z^2$
- Admittance, $Y = \frac{1}{\sqrt{R^2+X^2}}$, also approaches infinity at low and high frequencies, with the lowest at the resonant frequency. Opposite to the series resonant circuit, at low frequencies, $X_L > X_C$, and the net impedance is inductive resulting in lagging power factor. At high frequencies, when $X_C > X_L$, the net impedance is capacitive, and the power factor is leading.

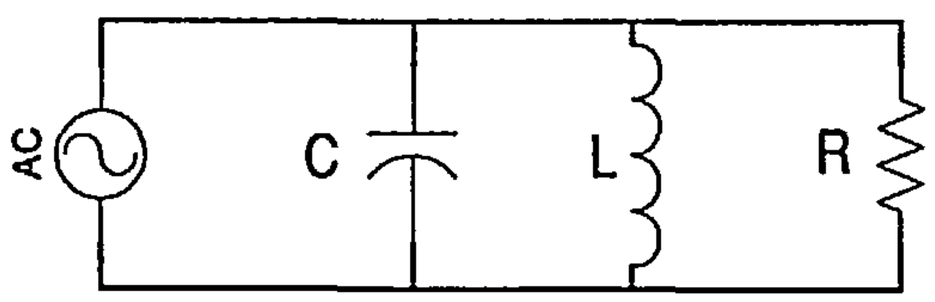

Fig. 2.8: Simple parallel circuit

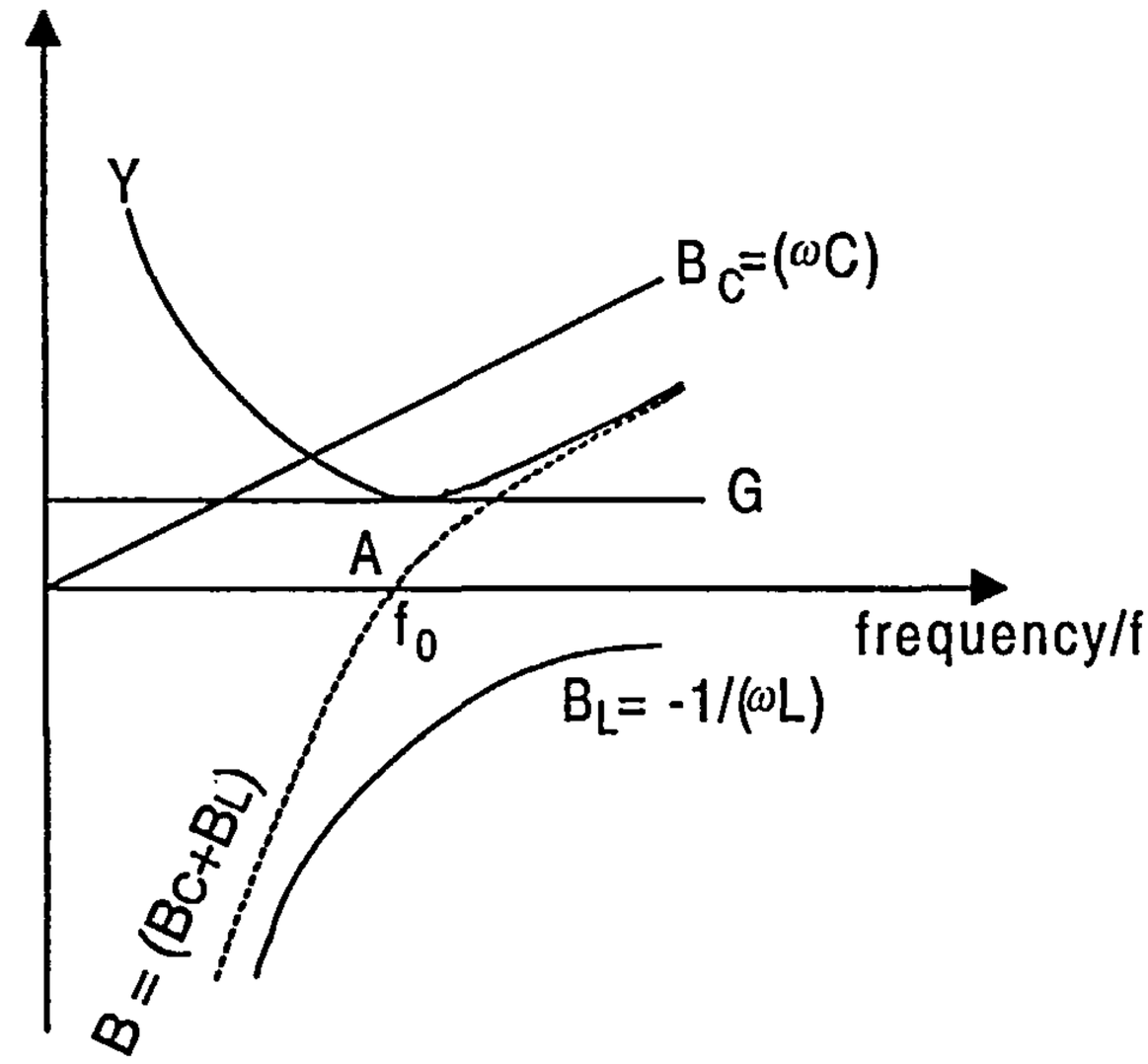

Fig. 2.9: Variation of susceptances, B, B_L, B_C; conductance, G; input admittance, Y; and input current, I with frequency

The power factor is unity when $X_L = X_C$. The dynamic impedance is maximum while the admittance is minimum at resonance.

- Current, I, has minimum value at resonance, and it, circulating between the two parallel branches, is very much greater than the supply line current. Since a parallel circuit rejects, or takes the minimum current of the frequency to which it resonates, it is also called a *rejector circuit.* The parallel resonance is called *current resonance.*

Bandwidth

The two *half-power-point frequencies* are defined as those frequencies at which the magnitude of the input admittance of a parallel resonant circuit is greater than the magnitude at resonance by a factor of $\sqrt{2}$. Current at both half-power points *decreases* to $\frac{1}{\sqrt{2}}$ of its *maximum* value. The bandwidth, AB, from Fig. 2.10, is given by, $\Delta f = f_2 - f_1$. Over the bandwidth range, current is equal to or less than $\frac{I_0}{\sqrt{2}}$.

Quality Factor, Q

Q-factor is defined as the *ratio of the current circulating between its branches to the line current drawn from the supply or simply, as the current magnification at resonance.* It is given by Q-factor $= \frac{I_C}{I}$(or can also equal $\frac{I_L}{I}$, or $\frac{I_R}{I}$) $= \omega_0 CR = \frac{R}{\omega_0 L} = \frac{R}{Z_0} = tan^{-1}\,\phi$, where ϕ is the power factor angle of the coil. Again, Q-factor also equals to $\frac{\text{energy dissipated per cycle}}{2\pi \times \text{maximum stored energy}} = \frac{\text{active power}}{\text{reactive power}}$.

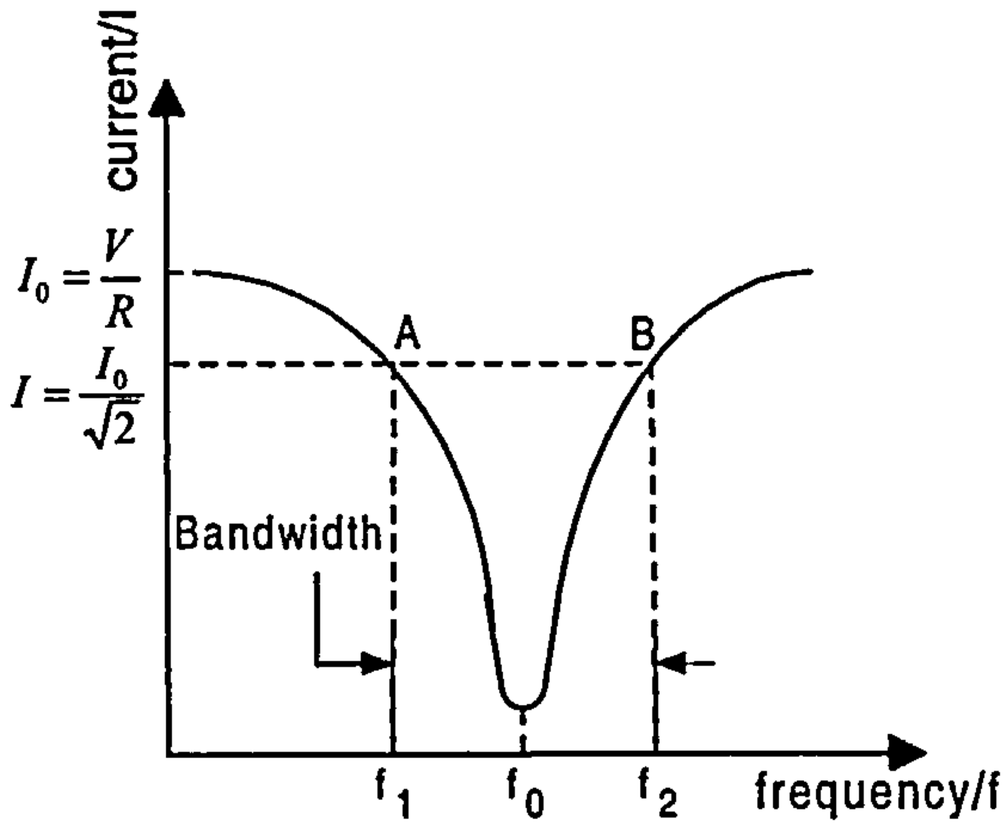

Fig. 2.10: Bandwidth of resonant circuit

2.5 Resonant-switching Conditions

Resonant-switching conditions change dramatically between the frequency above and below the tank natural frequency. A half-bridge series L-C-R network is used as an example to show the switching conditions [14].

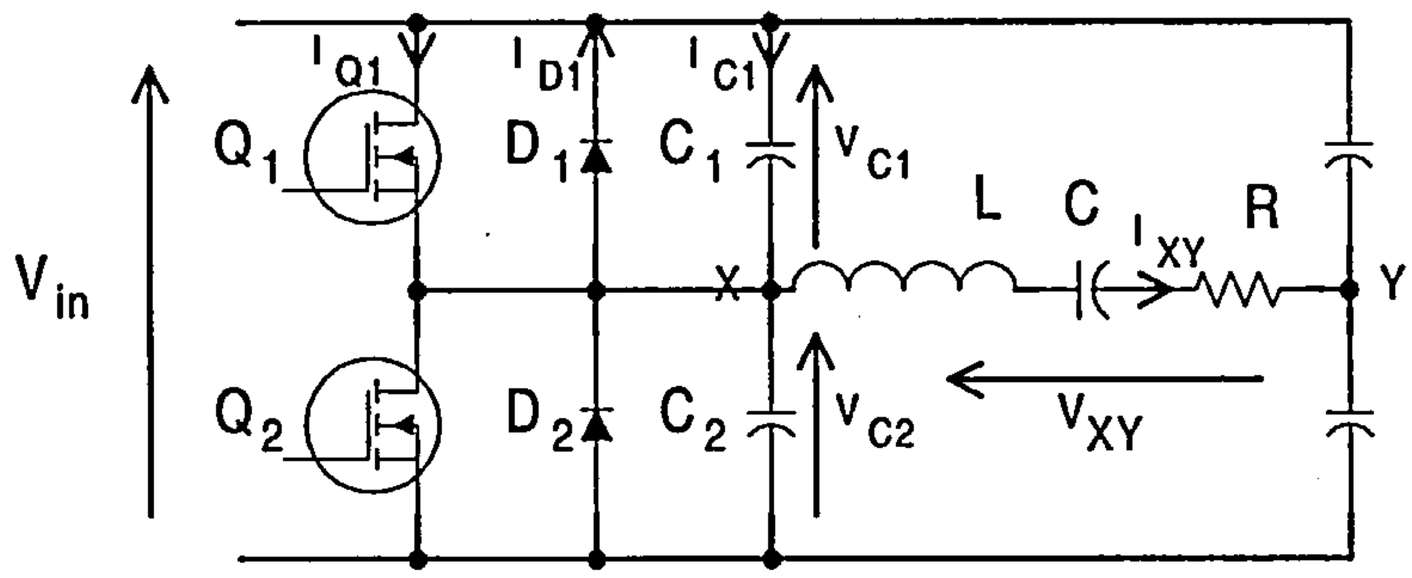

Fig. 2.11: Half-bridge series L-C-R network waveforms for switching-condition illustrations

2.5.1 Switching Below Resonance

From waveforms in Fig. 2.12 [14], it is clear that at turn off, the transistor current falls to zero naturally. Hence, zero-current switching is obtained. However, at turn-on, the transistor current is not zero. Neither is the transistor voltage. Thus, hard switching encountering switching loss occurs at the turn-on instant.

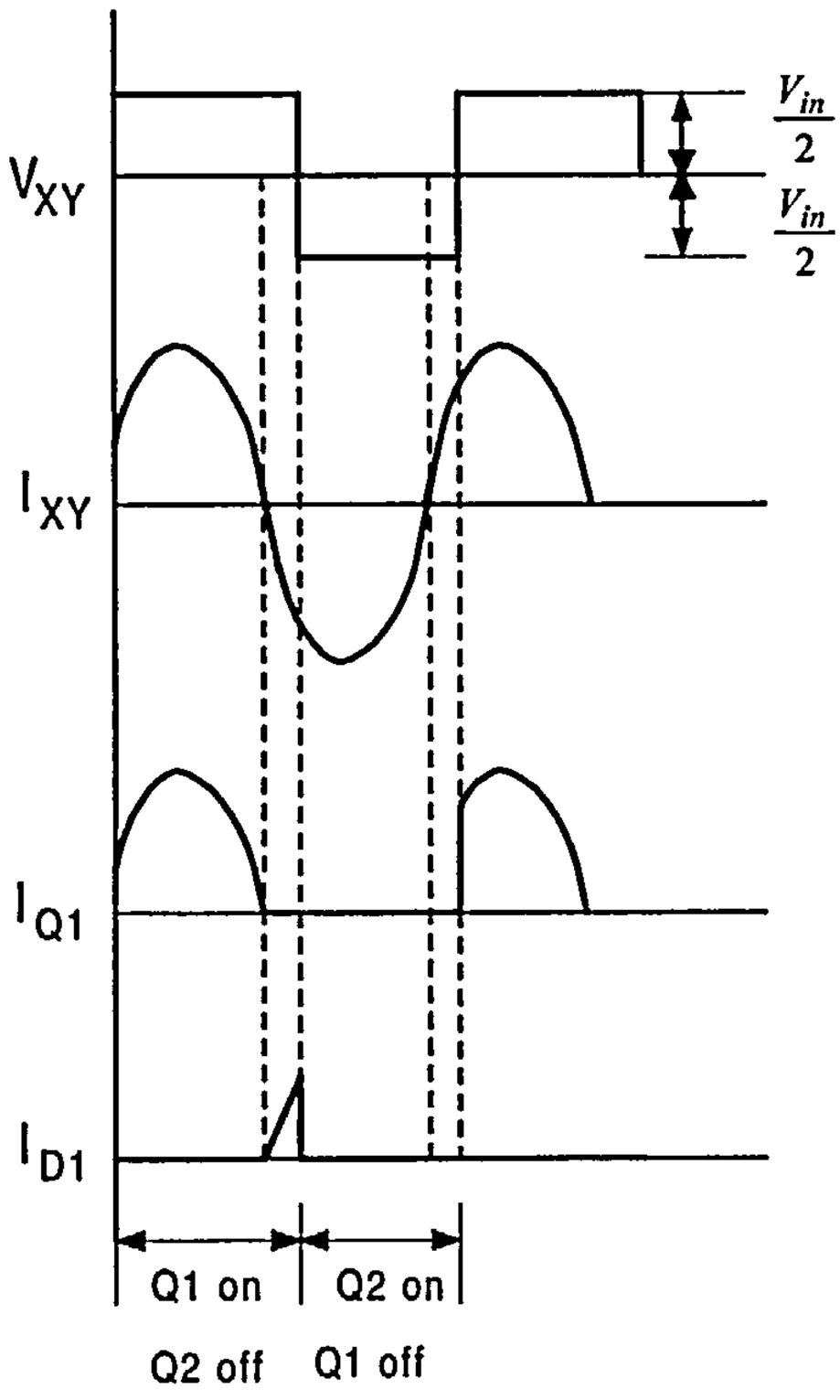

Fig. 2.12: Half-bridge and L-C-R network waveforms for switching frequencies below resonance

2.5.2 Switching Above Resonance

The waveforms depicted in Fig. 2.13 [14] show that at turn-on, transistor current is zero prior to the current flowing through the resonant tank. There is an energy loss at turn-off due to non-zero-current switching at the turn-off instant.

According to most of the literature, it is preferred to operate the resonant converters above resonant frequency as turn-on loss is naturally zero whilst the turn-off loss can be virtually eliminated by inserting a capacitor across each switch, shown as C_1 and C_2, in Fig. 2.11 in order to control the rise of the voltage across the switch or capacitor. Doing so, the switch current would fall to zero before the rise of the switch or capacitor voltage, hence yielding zero-voltage-switching conditions. This phenomenon is depicted in Fig. 2.14.

2.6 Advantages and Disadvantages of Resonant Switching

Major advantages and disadvantages of the soft-switching operations can be summarized as follows [16, 18],

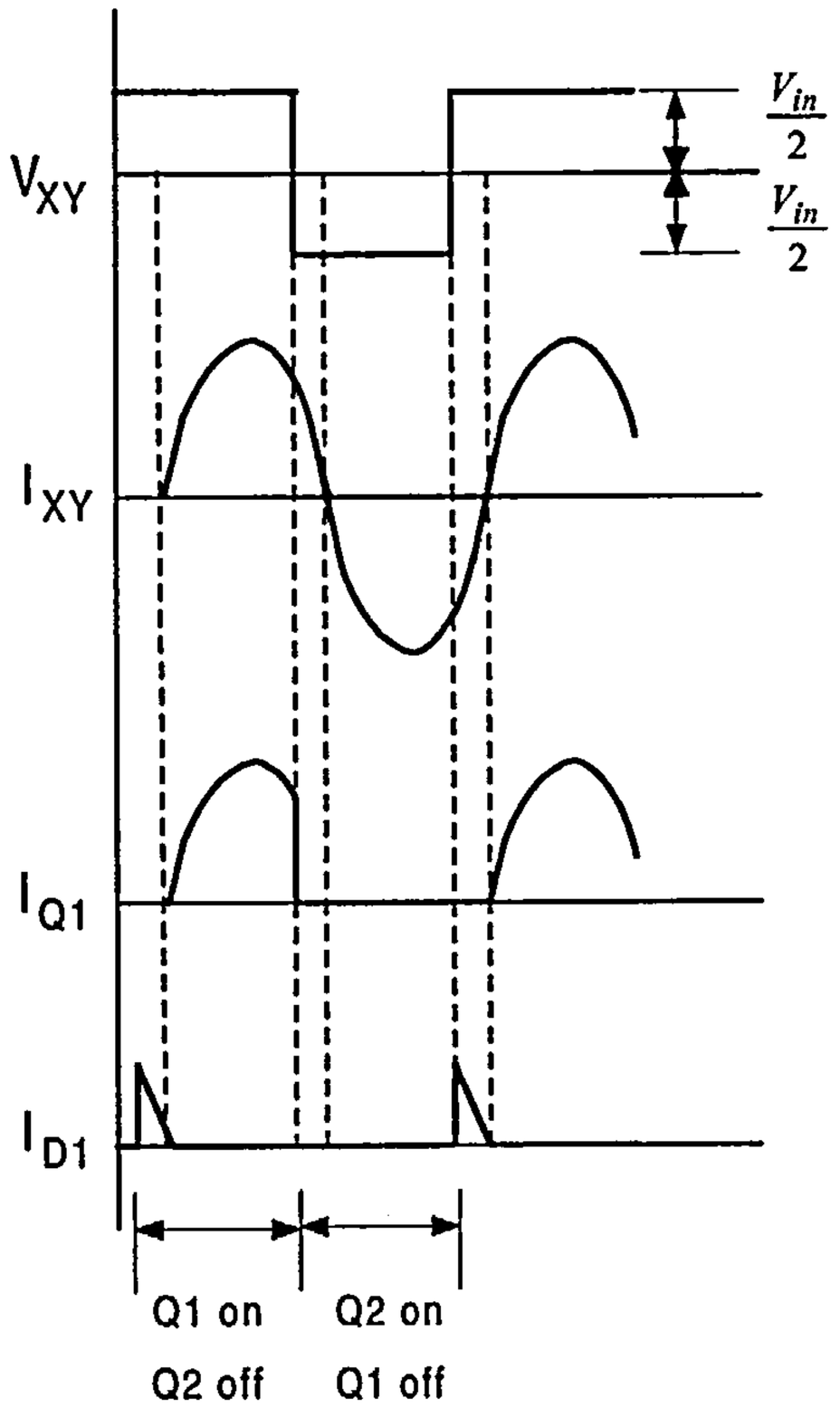

Fig. 2.13: Half-bridge and *L-C-R* network waveforms for switching frequencies above resonance

- The advantages of resonant switching

- absence of switching losses

- improved reliability due to reduced stress

- limited frequency spectrum causing low EMC and losses in passive components

- reduction of weight and volume of the components resulting from high-frequency switching

- high resolution and high power density for the power conditioner

- simple and efficient protection networks can be built

- The disadvantages of resonant switching

- circuit complexity increases

- devices with higher voltage and current ratings are required

- values of voltage and currents circulating in the circuit can be higher than the source and output voltage and current.

- losses in magnetic components are unpredictable

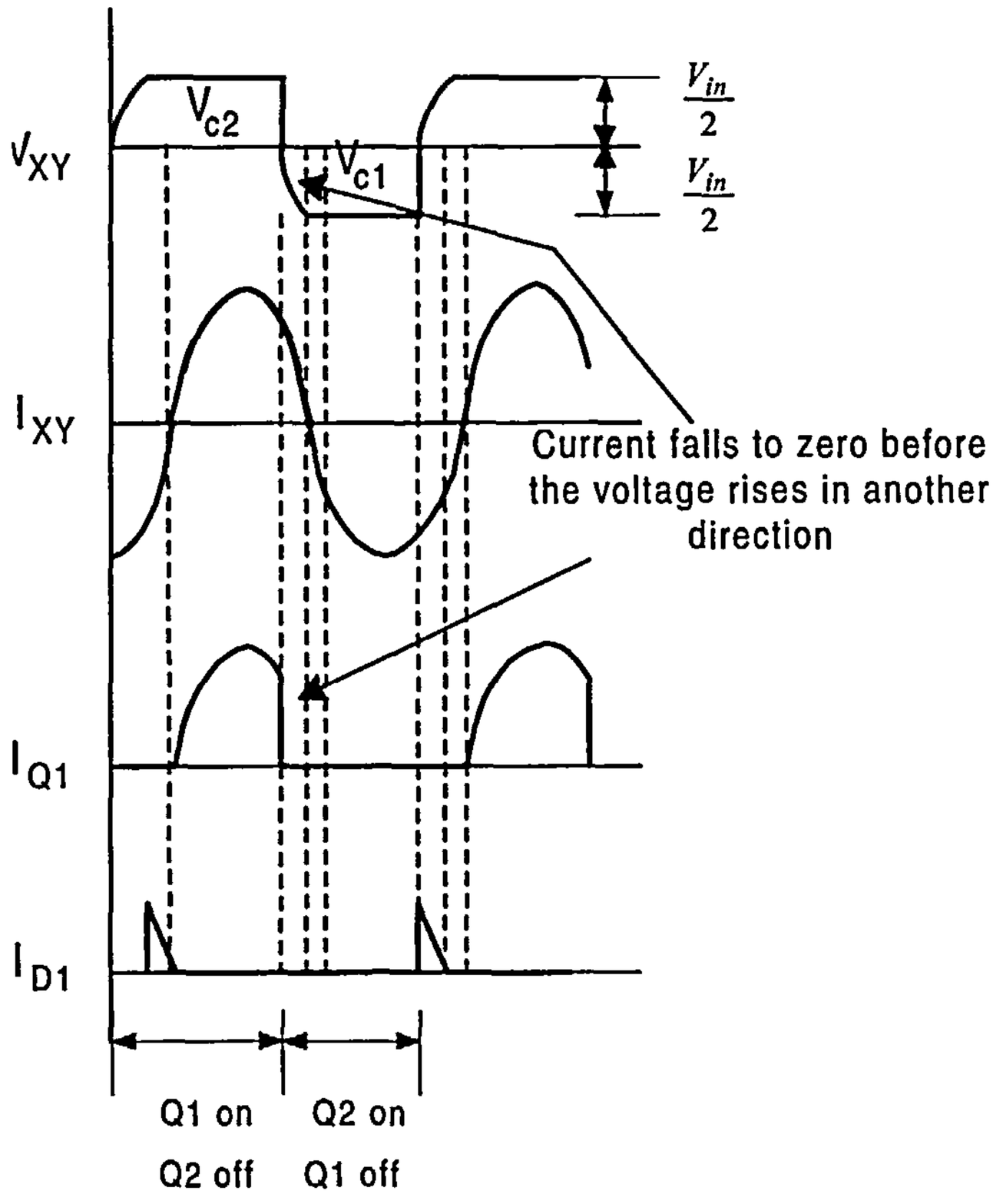

Fig. 2.14: Half-bridge and L-C-R network waveforms for switching frequencies above resonance with snubber capacitor

- the pulse-frequency modulation interferes with the analysis of the control aspects of the conversion systems
- restriction on device switching times causing variable-frequency switching techniques to be used
- sensitivity of operations to resonant component values.

2.7 Semiconductor Devices

Essentially, a power switch exhibits two types of losses during its operation. The losses are *switching loss* which is the loss associating with the switch turning on and off, while *conduction loss* is the loss depending on the device resistance, or voltage drop when the switch is on.

With resonant switching, switching losses are much reduced and higher operating frequency may be utilized. This results in a smaller size of the converters with high-power density and efficiency. However, the resonant action results in increased peak current and/or voltage and hence gives rise to higher conduction loss. The switches are subjected to higher current and voltage. In

addition, most of the semiconductor devices show undesirable and unexpected characteristics, including high turn-off power, high forward voltage drop, dynamic voltage saturation, and significant package inductance, when operated in soft-switching modes. As a result, switches used in resonant converters have to have both the fast switching and higher current and/or voltage capabilities. This leads to the studies and comparisons of commonly available power semiconductor switches. The devices discussed below are based on work reported in [1,7,8,19–23], with particular emphasis on soft-switching.

2.7.1 Metal-oxide-semiconductor Field-effect Transistor/MOSFET

Power MOSFET is a unipolar, majority carrier(electrons)[2], voltage-controlled device. When a positive voltage is applied to the gate, with respect to the source, the p-channel, which is beneath the gate, is converted into an n-channel, connecting the drain to the source, to allow the current to flow through the main terminals. Because the gate is isolated from the p-channel, the power gain is extremely high. Since MOSFET is a majority carrier device, meaning there is no excess minority carriers moving into or out of the device when it is turned on or off, it switches at very high speed, with assured thermal stability. The gate voltage must be removed to turn the device off.

MOSFET has virtually no inherent delay[3] and storage time[4]. However, it has self-capacitance that has to be charged and discharged while switching. The switching speed is therefore determined by the time constant formed by the self-capacitance in conjunction with the gate circuit, together with the drain and source circuit impedances. The typical switching time for MOSFET is around $0.5\mu s$. The absence of storage time permits fast response to overload and fault conditions.

The device is used in high-frequency switching applications because of negligible switching loss. Due to its on-state resistance which increases with voltage rating, causing high conduction loss, it is not commonly used in high-power applications. In addition, its high peak-to-rms current ratio favors it to be used in low-power applications. The typical voltage and current ratings are 500 V and 200 A respectively.

As it exhibits a square and wide safe operating area and possesses a positive temperature coefficient of resistance and a negative temperature coefficient in drain current, snubberless and paralleling of devices operations are allowed. Paralleling of devices increases the current handling

[2]In a p-type material, the number of holes is much more than that of electrons. Thus, holes constitute *majority* carriers and electrons form *minority* carriers.
In an n-type material, electrons are *majority* carriers, and protons are *minority* carriers

[3]*Delay time* - Period between 10% rise of drain current and 10% rise of gate current [23].

[4]*Storage time* - time of charge in the device being removed [23].

capability. The conducted current would drop to restore thermal stability when increased temperature is encountered by one of the MOSFET components. This prevents second breakdown[5] of the device as uniform current density is created.

MOSFET can be damaged by static charge if handled carelessly during testing or installation processes. Excessive gate voltage applied to the device will cause permanent damage to the gate oxide. A typical gate-source rating is $\pm 20V$. The excessive gate voltage is usually caused by the voltage transients in the drain circuit coupling to the gate via the drain-gate self-capacitance. At turn-off, fast-switching speed can cause a drain-voltage transient, due to stray inductance. The body diode can be a problem, at times, due to its longer reverse-recovery time compared with the switching speed of the device. During its recovery period, the body diode has limited dv/dt capability which can cause MOSFET failure if excessive external dv/dt is applied to the device [24, 25].

Three different MOSFET structures were studied in [26]. They are UMOS, VMOS and Lateral channel MOSFET. The critical current-density, the on-state resistance, the body-diode reverse-recovery time, the channel turn-on/turn-off transients, the input capacitance, the off-state capacitance and the breakdown voltage were analyzed and compared. The results show that VMOS has the lowest breakdown voltage, body-diode reverse-recovery time, input capacitance and on-state resistance.

Since MOSFETs are designed to be fast-switching devices in hard-switching, their switching speed no doubt is usually not an issue for most applications. Operating the devices in soft-switching conditions is most likely to reduce the need for heat-sink or to push the operating parameters to further limits. However, when the switching frequency exceeds 10MHz, the parasitic effects in the devices become apparent [27, 28]. Low parasitic effects allow higher switching frequency and lower gate-drive losses.

The MOSFET has three primary parasitic capacitances, i.e. gate-source capacitance, drain-gate capacitance and drain-source capacitance. Parallel combination of gate-source and drain-gate capacitance forms the input capacitance while parallel combination of drain-source and drain-gate capacitance forms the output capacitance. Among these capacitances, the drain-gate capacitance has the dominant effects on the device's switching speed [Gauen, 1989, Gauen, 1985].

At turn-on, the input capacitor is being charged. If it is charged over the threshold voltage of the gate-source, the capacitor appears to be an impedance for the gate-drive circuit resulting in

[5] *Second(ary) breakdown* is a failure mode of some minority-carrier semiconductor devices as a precipitous drop in the collector-emitter voltage at large collector current causing high power dissipation [7].

power loss. Thus, in order to minimize the losses, the gate-drive has to be able to source and sink large currents quickly so that power is not dissipated once the MOSFET is switched [27].

At turn-off, the output of MOSFET becomes a high impedance, and current commutates to its output capacitor in order to charge the capacitor up to input-voltage level. The energy flowing this time is simply stored in the output capacitor. However, this energy is dissipated when the capacitor is discharged at turn-on. The stored energy has to be recovered instead of dissipated at multi-Megahertz range operations [28].

The gate-drive impedance can be made smaller to reduce the Miller effect[6] of the drain-gate capacitance to help increasing the switching speed. The on-state drain-source resistance only contributes to total dissipation below about 1MHz. It has no great effects on power loss at frequency around 10MHz [28].

2.7.2 Gate Turn-off Thyristor/GTO

The GTO is a three-terminal latching, or thyristor-type device, combining the design and structure of the cathode-emitter of a transistor, and the vertical structure of a thyristor.

The GTO retains the basic *pnpn* layers of the conventional thyristor. The major difference is the modifications made in the GTO to achieve a gate-turn-off capability. The gate-turn-off capability is advantageous in that it provides increased flexibility to control power, in converters, without the use of elaborate commutation circuitry. The modifications made also result in a shorter turn-off and forward-recovery time in the GTO compared with the thyristor. Problems of current saturation and di/dt limitation found in the thyristor are overcome in the GTO invention. A higher current turn-off capability and a wider safe-operating area are made possible in the GTO. However, the downside of the modifications is the higher on-state voltage drop, at a given current level, than that for a conventional equivalent thyristor.

The GTO can be activated by a positive gate current and turned off by a negative current pulse, with a small turnoff current gain. The current gain requested depends on di/dt of the reverse gate current. A high rate of change in reverse gate current yields short turn-off times and near-unity current gain, whilst slowly applied di/dt gives rise to higher current gain but longer turn-off times and switching losses.

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[6]According to this effect, when viewed from input gate terminal of drain-source-connected MOSFET, the drain-gate capacitance, C_{dg} appears as $(1 + A_v)C_{dg}$, i.e. the original C_{dg} is amplified by a factor of $(1 + A_v)$, where A_v is the voltage gain of the device [17].

GTOs are sensitive to high rates of rise of the forward current, di/dt, at turn-on and high-forward voltage gradient, dv/dt, at turn-off in general. At turn-on, it exhibits delay and rise-time[7] phases followed by a voltage-tail phase, which are influenced by the rate of the rise of anode current and peak gate current, while at turn-off, it exhibits storage-time, fall-time and tail-time effects. The turn-off storage and fall times are influenced by the anode turn-off current and the rate of rise of turn-off gate current. While current tail-time[8] is dependent on turn-off voltage and junction temperature, the tail-phase also contributes significantly to the turn-off-energy losses. It was mentioned in [Eriksson et al., 1989,Taylor, 1989] that the turn-on and turn-off losses, especially the turn-off ones, actually comprises more-than-half of the total losses in the GTO.

The GTO has either symmetric-voltage or asymmetric-voltage blocking capabilities, i.e. it blocks both the forward and reverse voltage with the symmetric-blocking capability, or it blocks only the forward voltage with the asymmetric blocking capability. However, Alder *et. al.*, in [22] point out that reverse-blocking capability is not needed in most applications since an anti-parallel diode can be used in inverter operation. By using an asymmetric GTO, anode shorting can be achieved internally to further improve the switching characteristics. In addition, an extra n^+ layer in the n-channel, adjacent to the anode-emitter junction, reduces the forward voltage drop. These two features are very much in favor in high-voltage applications.

The GTO has a high switching loss and the typical switching frequency is 500Hz. The ratings are typically 6500 V, 5000 A.

Over-current protection is needed in GTO applications and the common way to achieve this is to turn on a parallel thyristor connected across the GTO, which in turn blows the fuse used in the circuit. This is called the *crowbaring technique.* An alternative is to use a much higher current-rating GTO, which is very costly. The GTO should not be turned on, or off, until it has been off, or on respectively, for a specified minimum time owing to the poor sharing of current characteristics which can result in device destruction otherwise [7]. Yatsou *et. al.* also proposed a way to further reduce the on-state voltage drop and increase the blocking voltage at high temperatures in [Yatsuo et al., 1983]. It is suggested also that a much larger gate current to be used in triggering the GTO to obtain a shorter turn-on time possible. The turn-off time of a GTO can be reduced by the

[7] *Rise time* - period that the current rises from the 10% of its initial value to the 90% of its final value on the current waveform whereas *fall time* - period that the current falls from the 90% of its initial value to the 10% of its final value on the current waveform [23].

[8] At the end of *avalanche breakdown* or reverse breakdown caused by rapid increase in current at the reverse-bias voltage, a small anode current continues to flow between the anode and the negatively biased gate due to the sweep-out of excess-stored charge in the n and p base regions. The time interval during which this current, driven by increases voltage difference between the anode and gate, flows is termed anode *tail-current time* [23].

gate-assisted forward-recovery method where the forward recovery current is directed into the gate, instead of flowing via the gate-cathode junction, to activate the device as a fast thyristor [Mertens et al., 1994], [Holtz et al., 1994].

As is well known, the GTO operates most simply at very-high power and low frequency. In order to utilize it at high frequency with high power, the problems of switching losses, snubber losses and reset time, and stray inductance in the circuit have to be overcome. The best way to do this is to operate it in soft-switching mode. According to [Holtz et al., 1994], under zero-current-switching operation, the GTO behaves in superior ways to when it is operated under conventional hard-switching conditions.

In order to avoid the transient turn-on voltage spike and the turn-on switching loss, the GTO's gate can be driven with a large-enough base current. Under zero-voltage switching condition, current with limited di/dt flows through the device. The resonant inductor(s) in the circuit also helps to suppress the di/dt. Resonant capacitor(s), which resets the stored energy, can also be used to avoid significant stray inductance by placing it close enough to the switch. This is impossible in hard-switching operations as a RCD (resistor-capacitor-diode) snubber circuit is usually used. The snubber gives rise to the stray inductance which then causes a voltage spike at turn-off. The voltage spike limits the turn-off current capability and increases the power dissipation in the device. Reverse-biased second breakdown in voltage can occur.

The rate of rise of the anode-cathode voltage during the GTO's tail-time is lower and the dc-bus overshoot is smaller, leading to lower safe-operating-area requirements and low turn-off loss [29]. It is even suggested in [Millour, 1987, Bornhardt, 1988, Bornhardt and Darmstadt, 1990] that by using a specially designed commutation circuit, operation without a snubber is possible because of the high dv/dt capability of the GTO after turn-off. There is a resonant capacitor serving also as usual snubber capacitor in the circuit.

However, the turn-on losses are not as bad as the turn-off losses. It is believed in [Morris et al., 1989] that even at resonant switching, the operating frequency of GTOs is somehow limited by the tail-current which has long decay time. The losses due to the tail-current happen simultaneously with the re-applied dv/dt. It is possible to reduce the tail current by increasing the carrier lifetime[9]

[9] *Carrier lifetime* [30] is the characteristic decay time or the time constant of the minority-carrier devices. From basic semiconductor physics,

- Carrier lifetime in a region decreases as impurity doping concentration increases
- Transistor gain decreases as base region lifetime is decreased
- Transistor gain decreases as base width is increased

by heavy metal doping and electron irradiation without worrying about the rise in on-state voltage, as the on-state losses are a minimum at soft-switching operation.

2.7.3 Insulated Gate Bipolar Transistor/IGBT

The IGBT is a hybrid semiconductor device combining the attributes of MOSFET, BJT and GTO. It is a voltage-controlled device requiring the continuous application of a gate voltage, similar to MOSFET, but it has lower conduction losses and higher voltage and current ratings. Like MOSFET, it has a high-impedance gate, requiring only a small amount of energy to turn the device on. However, it is a minority carrier device, which makes it slower than the MOSFET. The IGBT has a small on-state voltage even with large blocking voltage rating, similar to the BJT. Like the GTO, IGBT has the capability to block negative voltages.

When continuous positive voltage is applied to the gate, with respect to the emitter, an n-channel is induced in the p-region. This forward biases the base-emitter junction, causing the base current to flow from the emitter to the collector, and hence turns the device on. However, a latching-mechanism effect may be achieved, like in a thyristor, accidentally by exceeding the current and voltage rating. Consequently, over-current could damage the device and ringing could occur at switching. The latching mechanism is usually prevented by proper impurity concentration of p^+ layer that constitutes the base of the parasitic npn transistor.

An IGBT that is subjected to a high dv/dt, in the off-state, may experience a false turn-on charge. This is due to its rising collector voltage charging the junction capacitances. The re-applied dv/dt causes a displacement current[10] to flow into the gate capacitance, thereby affecting the gate conditions. The level of the effect depends on gate-resistance, gate-bias voltage, case temperature, etc.. In any event, the effect has the tendency to turn the device on. In order to prevent this, application of a negative gate-bias voltage is suggested in [Jiang et al., 1993, Finney et al., 1994, McNeill et al., 1998].

The device has a higher current density compared with a MOSFET device, and its input capacitance is significantly less than that of a MOSFET. In addition, the ratio of gate-collector capacitance to gate-emitter capacitance is lower than that in a MOSFET, giving improved Miller-feedback effect during high dv/dt turn-on and turn-off. Similar to a MOSFET, an IGBT does

[10]When the output voltage(usually DC) changes or decreases by an angle of α, the ac input-current also shift by angle α towards the lagging direction. This causes a phase displacement of α between the AC-current and AC-voltage giving rise to a power factor of cos α. The reduction voltage on the DC side by cos α means an additional reduction in the AC-side power factor by the same factor due to the *displacement* of the AC *current*. In the case of latch-up problem, the displacement current is caused by the inductive load which introduce lagging power factor [10].

not have inherent delay and storage time. The typical switching time for an IGBT is 2.5μs. It is shown in [Brambilla et al., 1994] that the switching time of an IGBT is influenced not only by the gate-input capacitance, but also by the driver charge-injection and extraction capability, and its internal stray inductances. The absence of storage time permits fast response to overload and fault conditions.

The device is used in medium high-frequency-switching applications because of the negligible switching losses. Owing to its lower on-state resistance, compared with a MOSFET, it is used in higher power applications. The typical voltage and current ratings are 1500 V and 400 A respectively.

It also exhibits a square and wide safe-operating area, and possesses a positive-temperature coefficient of resistance, like the MOSFET, which allows snubberless and paralleling of device operations. It can withstand high junction temperatures, and it has an on-state voltage that changes little with room temperature. It has a high-maximum junction temperature[11] because it combines the positive temperature-coefficient of a MOSFET and its own negative temperature-coefficient of the voltage drop across the drift region. Like in the IGBT, secondary breakdown is not possible.

The short-circuited capability of the IGBT is usually defined for the short-circuit of IGBT on going from the off-state into the short-circuited state. In this case, the load is already short-circuited when the IGBT is turned on. A question mark remains over the level of stress of the IGBT, turning from the on-state into the short-circuit state, carrying current when the load has not been short-circuited until the device is turned on. This information is not provided in any manufacturers' data book. However, an experimental investigation on the behavior of IGBT, on short-circuiting during the on-state, was done by H. G. Eckel and L. Sack [Eckel and Sack, 1994]. It is also known that a device subjected to a very-high current-surge could limit the magnitude by its own gain. Thus, the lower the IGBT's gain, the longer its short-circuit withstand-time[12], but at the expense of operating frequency. The high-gain IGBT, on the other hand, gives better efficiency but requires external protection circuit, which is usually handy and economical to be built. The destruction of an IGBT under short-circuit condition is always due to an excessive power dissipation generating high temperature beyond the limits of the silicon. Detailed description of the failure mechanism and protection methods can be found in [Chokhawala et al., 1993]. A low-cost IGBT gate-drive

[11] *Junction temperature* is the temperature measured at the *pn* junction of a semiconductor device.

[12] *Short-circuit withstand-time* is a measure of how long a device would survive under specified test condition, e.g. short-circuit condition.

circuit providing short-circuit protection and high dv/dt immunity is also presented in [Quintas et al., 1994].

There are two basic types of IGBT. One is called *punch-through*(PT) type and the other is *non-punch-through*(NPT) IGBT. The punch-through type does not have reverse-blocking voltage capability, and has low conduction loss and slower switching speed. There is usually an in-built anti-parallel body diode. The over-voltage is rather low and it does not increase with decreasing parasitic inductance of the short-circuit during on-state. The latter has an excellent reverse-blocking voltage capability. It has been optimized for switching speed but it has higher on-state or conduction loss. The over voltage can be rather high and it increases with decreasing parasitic inductance of the short-circuit during on-state. The PT and NPT IGBTs are used in dc-input converters and ac-input PWM converters respectively.

Recent researches [Kurnia et al., 1995, Elasser et al., 1996] have shown that IGBTs exhibit different characteristics from the specified parameters in the manufacturers' data sheets when operating at soft-switching conditions. Important differences include an elevated tail current under varying output of dv/dt conditions, resulting snubber dump, and a significant-higher conduction loss under moderate-to-high di/dt conditions. Those undesirable effects contribute to an inductive effect resulting in dynamic-voltage saturation, during turn-on, and excessive forward-voltage drop. These papers show the switching dynamics and impact of IGBT in resonant-switching applications. Comparisons were drawn between hard-switching and soft-switching.

Authors in [Li et al., 1996, Widjaja et al., 1995] specifically pointed out that the bipolar effects, caused by the bipolar transistor in the IGBT, are more dominant than the MOSFET effects on the performance of the IGBT under soft-switching conditions. At turn-on, a physical effect termed *conductivity modulation lag* occurs. This is due to the much slower rate of the minority-carrier injection into the base of the bipolar transistor in the IGBT compared with the modulation rate of the drift-region conductivity. Hence, this leads to an inductive effect resulting in dynamic-voltage saturation and causes excessive forward-voltage drop. At turn-off, the tail-current bump was found to result from an interaction of the electric field and the recombination process. The tail-current phenomenon causes higher turn-off loss for zero-voltage-switching than zero-current-switching operations. The effects are worse with temperature increase. Switching performance can be improved by further narrowing the source region.

One major advantage of applying IGBT under soft-switching conditions is minimum turn-off failure of the device under clamped inductive load. This is because the industrial load, that is

usually inductive, does not subject the device to large turn-off switching stress, as usually happened in hard-switching operations. Here the current crosses zero while the device also, at the same time, supports link/bus voltage [Trivedi and Shenai, 1998, Trivedi and Shenai, 1999]. Thus, thermal runaway[13] can be avoided.

2.7.4 Insulated Gate Transistor/IGT

IGT [14] is a relatively new three-terminal voltage-controlled device combining the advantages of the input characteristics of the MOSFET and the output characteristics of the BJT. The BJT has a speedy turn-off time, but it requires high base-drive current during both turn-on and turn-off. In contrast, the power MOSFET requires low-gate drive current, and it is capable of very-high switching speeds with low and temperature-insensitive conduction losses. However, the MOSFET operates at much-lower current densities than the BJT. The IGT possesses its own distinctive advantage of having more 'flexible' characteristics, to be tailored according to particular applications, for trading off conduction losses with switching losses. It features low on-state loss, slow or fast switching speeds and has wider safe-operating area.

As shown in Fig. 2.15 [33], the IGT is a four-layer device

When the collector is reverse biased, meaning negative bias is applied to the collector, with respect to the emitter, there is no current flow, and thus a device with reverse blocking capability is provided. If the collector is more positive than the gate, having the same potential as the emitter, the device works in its forward-blocking mode. When an appropriate positive gate-to-emitter voltage is applied to the device, the surface of the p-channel underneath the gate is inverted and this causes the current to flow in its forward-conducting state, i.e. from the emitter n^+ region into the n channel. The conducting current has a higher density than that of the MOSFET and BJT. The device would saturate if the gate-to-terminal voltage is much bigger than the required turn-on voltage.

As IGT contains a parasitic thyristor structure, i.e. a four-layer – $n^+pn^-p^+$, it can be latched-on by exceeding the maximum controllable collector current. Generally static latch-up is likely due to improvements made on the device characteristics. However, dynamic latch-up could occur if care is not taken. Displacement currents would flow , under dynamic conditions, i.e. inductive load

[13] *Thermal runaway* is a situation where the power dissipation in a semiconductor device leads to temperature-increase in it, and the rise in temperature further increases the power dissipation and so on.

[14] Other names for IGT are like *Conductively Modulated FET/COMFET* [31] and *Gain Enhanced MOSFET/GEMFET* [32].

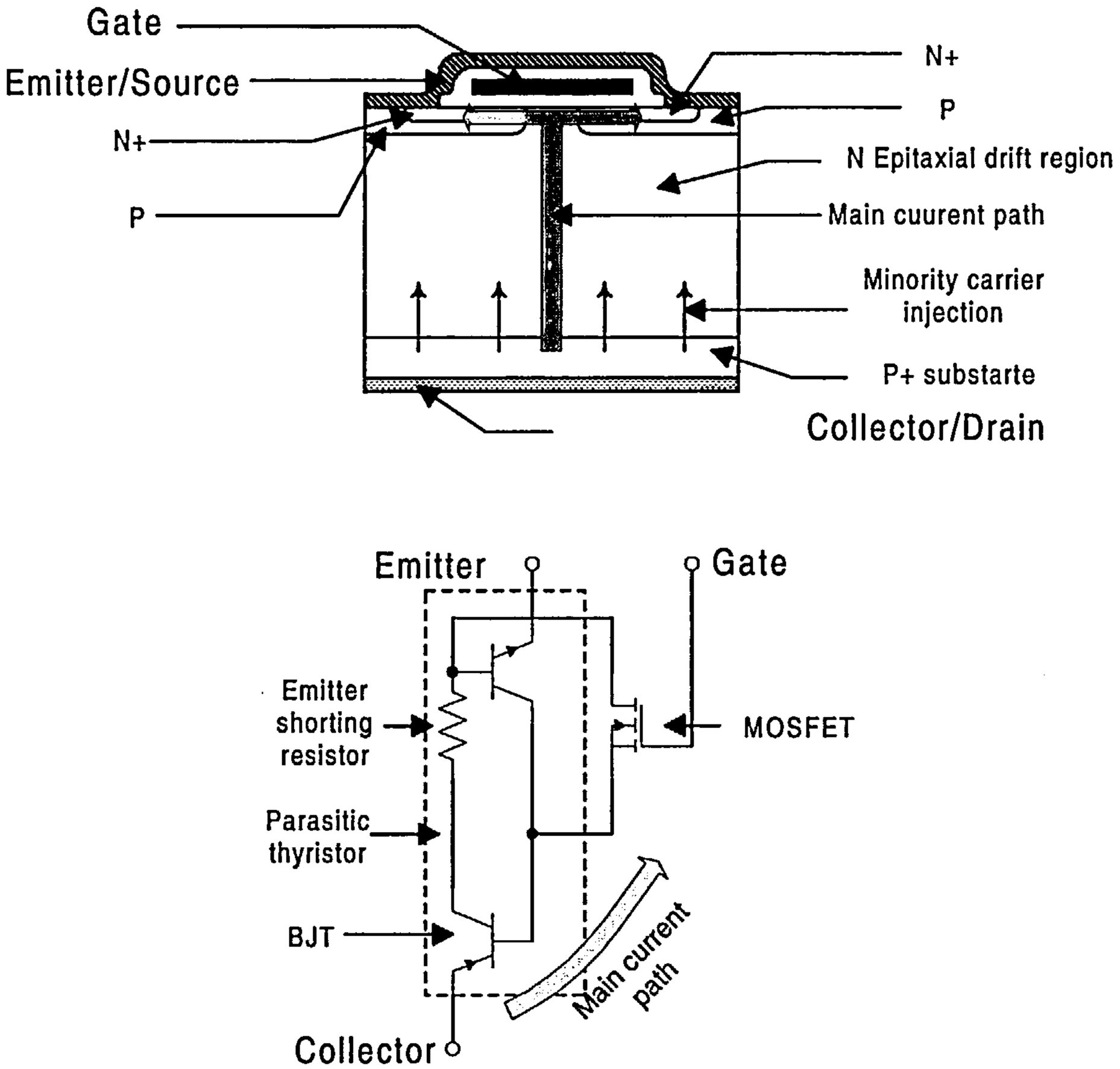

Fig. 2.15: Power MOS IGT-Cross section view & equivalent circuit

forced turn-off condition, through the pn^- junction capacitance and shunting resistance to forward-bias the parasitic *npn* base-junction; thus causing latch-up if the displacement currents are large enough. Dynamic latch-up occurs at turn-off only when the switching current exceeds the current level at which the dynamic latch-up occurs. It is advisable to keep the switching current below the latch-current of the parasitic thyristor which is less than the dynamic latch-up current [Becke et al., 1986]. It has been reported in [Sukumar and Chen, 1986] that the maximum switching-current varies with temperature, gate-impedance and the dv/dt of the drain-source voltage. The maximum switching-current level is inversely-proportional with temperature and dv/dt. A low valued emitter-shorting resistor is used to suppress the action. IGT can be turned off by providing a minimum value of resistor between the gate and terminal in order to provide a discharge path for the gate-to-terminal capacitance.

The resemblance to the MOSFET high-input-impedance gate-control characteristics in IGT allows controlled turn-off and gate-controlled turn-on. Its typical turn-off time, i.e. $10\mu s$, is slower

than the MOSFET. The turn-off time can be further decreased at the expense of reducing its current density and increasing its forward-voltage drop. The switching time of IGT is influenced by the gate-to-terminal impedance. It has lower input capacitance than a MOSFET. It behaves similarly to a MOSFET at turn-on, and does not exhibit significant storage-time at turn-off, but shows a longer fall-time consisting of two time intervals compared with a MOSFET. The time intervals are only noticeable for slow switching applications. The current fall-time is dependent on the gate-to-terminal resistor. This allows IGT to be used from slow-to-fast speed applications. A slow IGT is usually used with minimal gate turn-off current, while the fast one is used with a linear turn-off characteristics. At turn-off, there is a delay caused by the discharge time-constant of the effective gate-to-terminal capacitance and the gate-to-terminal resistor for preventing the latching mechanism. In general, it has a slower switching frequency compared to a MOSFET. The typical switching time of an IGT is $0.2ms$–$20\mu s$.

Parallel operation too can be used in IGT operations, but careful design has to be adopted to balance the magnitude of the individual collector currents in both the static stage and the turn-off, turn-on, and the magnitude of the collector current along the dynamic stage. The IGT has a superior elevated junction-temperature than either the MOSFET or the BJT, implying more increase in on-state voltage with increased junction temperature. It has a positive-temperature coefficient associated with its fall-time.

Due to the IGT's low on-state and temperature-insensitive internal resistance, it is not prone to thermal-runaway. However, this is not true for MOSFET. Thus, the conduction loss in the IGT is lower than the MOSFET

The device is used in applications requiring a wide range of medium switching frequencies. The typical voltage and current ratings are 600 V and 50 A respectively [33].

The problems associated with the IGT in hard-switching, such as turn-off current tailing and turn-off latching, are largely avoided in soft-switching. Over-current may cause the device to latch, but because of the soft-switching operation, IGT unlatches before the current crosses zero. In addition, latching due to turn-off can never occur because of the zero-current turn-off.

According to [Rangan et al., 1987], the limiting factors for an IGT operating at very-high resonant frequencies above 250kHz are the turn-on losses, dv/dt induced power losses and dv/dt induced latching. There are severe turn-on losses at frequencies beyond 500kHz as the device never has chance to turn-off due to the current-tailing of the dv/dt induced current conduction. Power

losses are induced by the high dv/dt. The losses are worsened by an increase in high voltage-spike caused by the reverse-recovery characteristics of the anti-parallel diode, operating frequency, lifetime of the minority carrier and the source-voltage level. dv/dt induced latching on IGT is the least determining factor on the device operating at high resonant frequency.

Under soft-switching operation, the conduction losses dominate the total losses owing to a high current conducted in the device.

2.7.5 Static-induction /SI power devices

The Static-induction device families, capable of operating at high-power and high-speed, are divided into two categories, according to [34], as shown in Fig. 2.16.

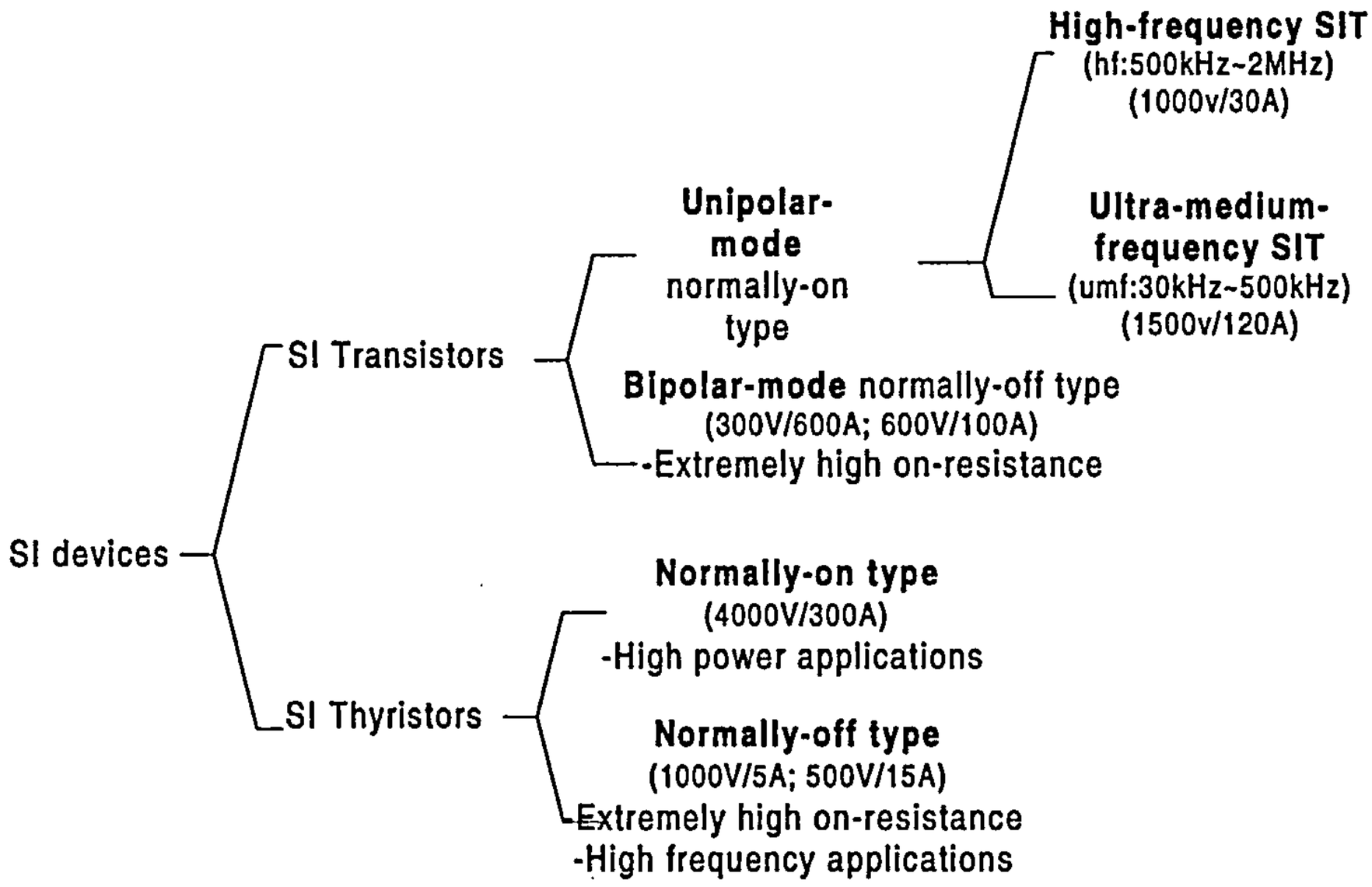

Fig. 2.16: Classification of the SI device families

Static Induction Transistor/SIT

The SIT, a relatively new device, which is actually a variation of *Junction-field-effect Transistor/JFET*, is a high-frequency, high-power device with typical ratings of 30kHz-2MHz, and 1500 V and 120 A. It is essentially the solid-state version of a triode vacuum tube. The SIT has a similar structure to that of the FET except that the SIT has a much shorter conduction channel. In this channel, the current, flowing vertically between the source and drain, is controlled by the height of an electro-statically-induced potential barrier under the source terminal as shown in Fig. 2.17 [1]. The short-channel effect results in an exponential dependence of the drain current on the drain

voltage.

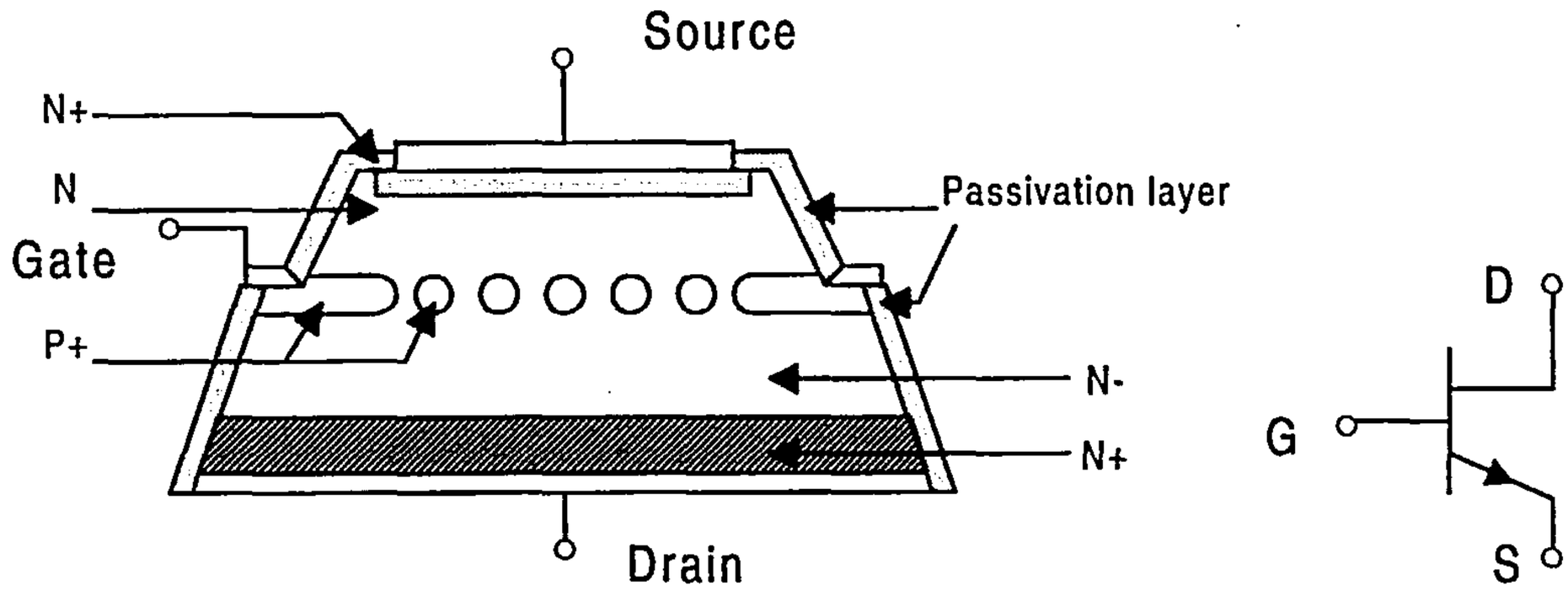

Fig. 2.17: SIT–Cross sectional view and circuit symbol

As the channel current is caused by the majority carriers that travel between drain and source terminals, at maximum saturated velocity, minority-carrier-stored-charge (hole) effects are eliminated, thus yielding a fast switching-time for the SIT. A faster-than-MOSFET-switching-speed SIT is made possible due to the SIT lower equivalent gate-source capacitance and resistance. Pair gates are used to increase the current-carrying capability of the device causing the current to flow through multiple channels through the n-type silicon. This reduces the power losses and the channel resistance, and makes it possible to operate in high-voltage applications. The lower gate-source channel resistance gives a lower gate-to-source negative-feedback effect compared to the FET.

Different to most of the semiconductor devices, it is a normally-on device implying that the device is on when the gate is shorted to earth, due to the absence of resistance to the flow of current between the drain and source. The device is turned off when the gate is negatively charged. Its normally-on feature is undesirable in most applications as large transient currents may flow at system power-up.

The SIT has a negative temperature-coefficient of resistance, and it can operate at high currents under thermally stable conditions [35, 36]. Due to its majority-carrier feature, its safe-operating area is limited by junction temperature. Device paralleling is easy as the SIT has also a positive temperature-coefficient characteristic for the channel resistance.

According to [7], it is possible to operate the SIT in bipolar mode when it is in the on-state. Instead of letting the gate-source voltage be zero at turn-on, the gate-source junction is forward biased which reduces the on-state resistance significantly. This causes significant gate current to flow, similar to a BJT in the on-state.

A normally-on SIT is very similar to a MOSFET in its switching characteristics. The only

difference between the devices is that the SIT needs a negative-going gate-source voltage to turn it off, and a positive-going gate-source voltage to turn it on. If it is operated in the bipolar mode, or fabricated as a normally-off device, it is usually called a *Bipolar Static-induction Transistor/BSIT.*

The BSIT behaves similarly to a BJT but with major differences in the turn-off waveforms. There is only one current-fall-time interval with the BSIT, and the turn-off time is much shorter than the BJT. Although BSIT has a fast switching-speed, its turn-off time is liable to become long due to the storage effect of of minority carriers in the channel injected from the gate region, when the gate-bias voltage is higher than it requires in the forward-bias direction. In order to reduce the storage time at turn-off, reverse-biased gate-voltage has to be increased.

The bipolar-mode device has distinguishing features like high-speed switching, large handling-power capability at high-voltage bus, reduced voltage drop with positive-biased voltage-drive techniques and easiness of several parallel connections [34].

Static Induction Thyristor/SITH

Static Induction Thyristor/SITH [1] is a self-controlled, GTO-like, on-off device. The structure is similar to a SIT except that the p^+ layer has been added to the anode side to remove the problem faced by a SIT in which stored charge is trapped when the collector-base junction, or the emitter-base junction, are reverse biased. The structure is shown in Fig. 2.18 [1]. It is a normally-on device with the n-channel saturated with minority carriers. It is turned off by reverse-biasing the gate with respect to the cathode. The negative current is large and the anode current shows a tail current at turn off. This is similar to a GTO. However, SITH has a lower current-gain than the GTO. It is not suitable for high-speed operation compared to the SIT, as the SITH does not have reverse-blocking capability owing to the emitter shorting. The SITH has a larger conduction drop, higher dv/dt and di/dt ratings and better safe-operating-area than the GTO.

When a power SIT is modified with an injecting-contact at the anode of the SIT, a new device termed *Field-controlled Thyristor/FCT, or Bipolar Static-induction Thyristor/BSITH* is produced [7]. The drain of the SIT is converted into a *pn* junction, and becomes the anode of FCT as shown on Fig. 2.19 [7]. The source of the SIT is termed cathode in the FCT. The FCT has a smaller on-state resistance and on-state voltage, even at high-current, compared to a SIT. It has similar switching characteristics in the forward-bias region to a SIT, although the SIT can conduct much higher currents with the same on-state voltage. The FCT has a reverse-blocking capability, which is independent of the gate-source voltage. It has a considerably slower switching speed than a

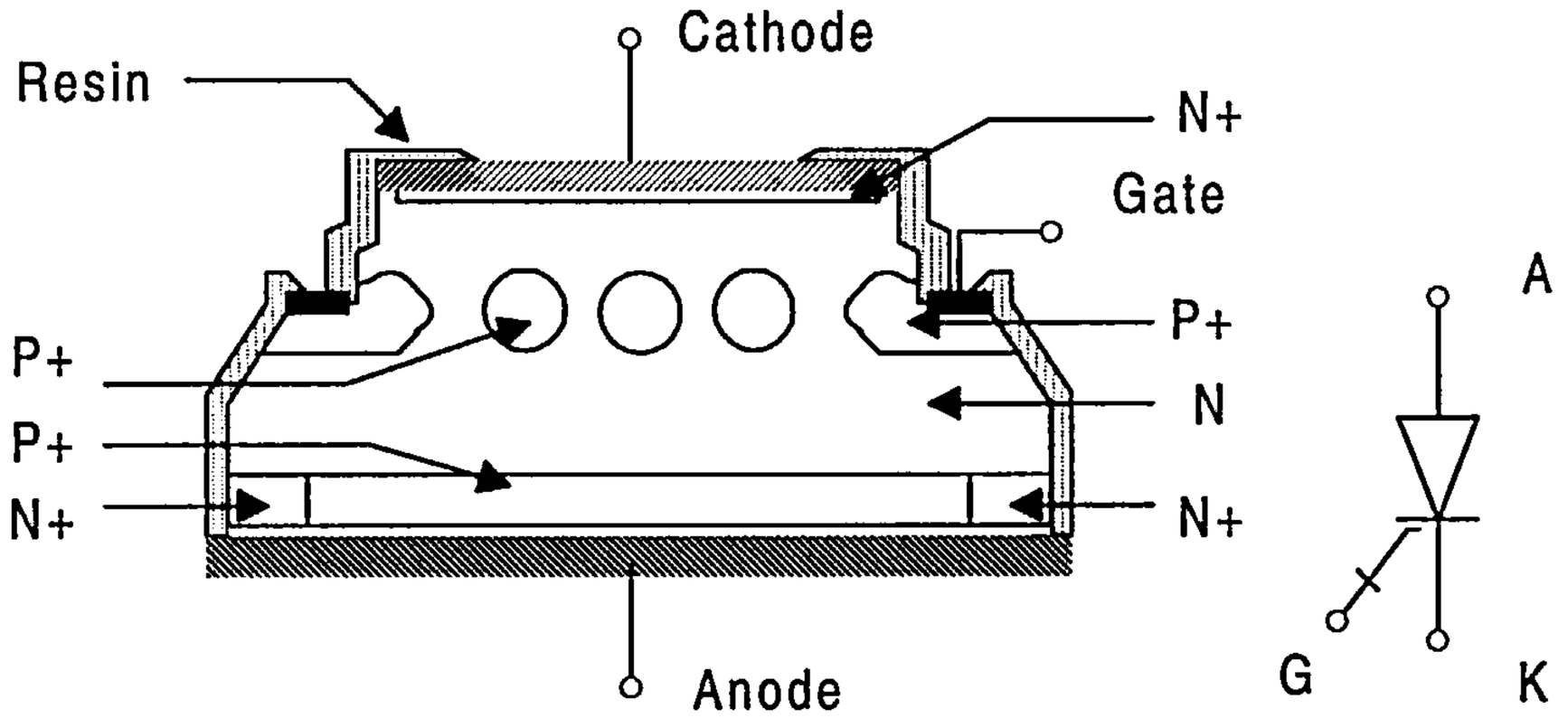

Fig. 2.18: SITH–Cross sectional view and circuit symbol

SIT. The FCT is turned off by applying a large reverse-bias to the gate-cathode terminals, which behaves like the GTO. It is important to note that SIT does not have any latching mechanism. A negative gate-cathode voltage has to be continuously applied to turn the device off.

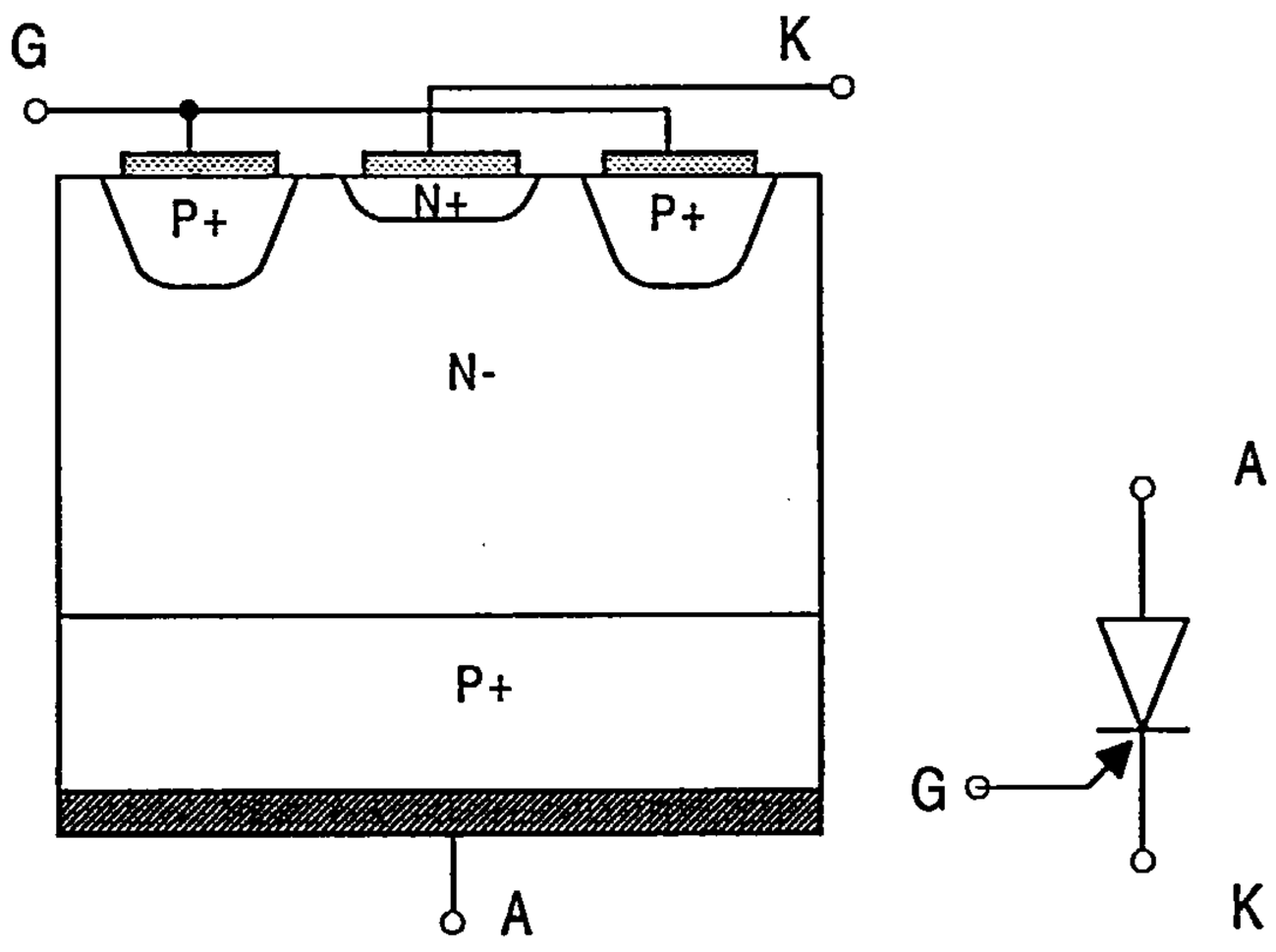

Fig. 2.19: FCT–Cross section view and circuit symbol

Under soft-switching conditions, the static-induction devices do not behave much differently from when they are operating under hard-switching conditions [Nakaoka, 1987,Ogiwara and Nakaoka, 1990,Muraoka et al., 1986,Nishizawa et al., 1986]. Lifetime control based on heavy-metal diffusion is performed for soft-switching operation, and an anode-shorted structure is adopted to reduce the tailing current occurring after turn-off. In addition, two techniques are suggested for use in obtaining even shorter switching-time and lower-forward voltage-drop in the devices with thick high-resistivity regions. The two techniques are reported as a combination of anode-shorting and

proton-irradiation, and dual-proton irradiation in [Kushida et al., 1986].

2.7.6 MOS Controlled Thyristor/MCT

MCT is basically a thyristor-like modern voltage-controlled device with two MOSFETs built into the gate structure. One of the two MOSFETs that is responsible for turning the device on is termed the ON-FET while the OFF-FET is to turn the device off. It consists of a parallel connection of thousands of identical micro-cells on the same chip. MCT combines the low on-state loss, or forward-voltage drop and high-current capability of thyristors with the advantages of MOSFET-controlled turn-on and turn-off with relatively high speed, and its high-input impedance feature.

There are two types of MCTs, the P-MCT and the N-MCT. The symbols 'P' and 'N' mean the blocking-voltage capability of the device depends on the p-region and n-region respectively. Both types have the same *pnpn* structure as a conventional thyristor. In the P-MCT, the p-type region, which is nearest to the cathode, functions as the base of the *pnp* transistor on the two-BJT model of the MCT, and it is the doped region containing the depletion layer of the blocking junction when the device is off; while in the N-MCT, the n-type region serves for the functions and the region is the nearest to the anode of the device. The P-MCT has a p-channel ON-FET and an n-channel OFF-FET located around the anode whereas the N-MCT has an n-channel ON-FET and a p-channel OFF-FET located around the cathode.

Both devices are turned on and turned off in an analogous manner, but with gating signals of opposite polarities. The P-MCT is turned on by applying a negative gate-anode voltage to the ON-FET, so that the gate has a more-negative potential than anode; whilst it is turned off by applying a positive gate-anode voltage, where gate is more positive than anode, to the OFF-FET. The N-MCT is activated by turning on the ON-FET with a positive gate-cathode voltage, and is turned off by a negative gate-cathode voltage.

The current density that can be turned off depends upon the density and the effective resistance of the OFF-FET whereas the turn-on speed and di/dt rating depend upon the density of the ON-FET. MCTs are generally designed to have as many OFF-FETs as possible in order to achieve high-current turn-off capability, and to have relatively few ON-FETs for a reasonably fast turn-on. The MCT has effectively an infinite dv/dt capability for the off-gate voltage, which is itself maintained throughout the off-state period [37].

The tailing effect in the MCT is controlled by proton irradiation to keep the conduction drop small. The MCT appears to have a typical hard-switched waveform, i.e. the anode-cathode voltage

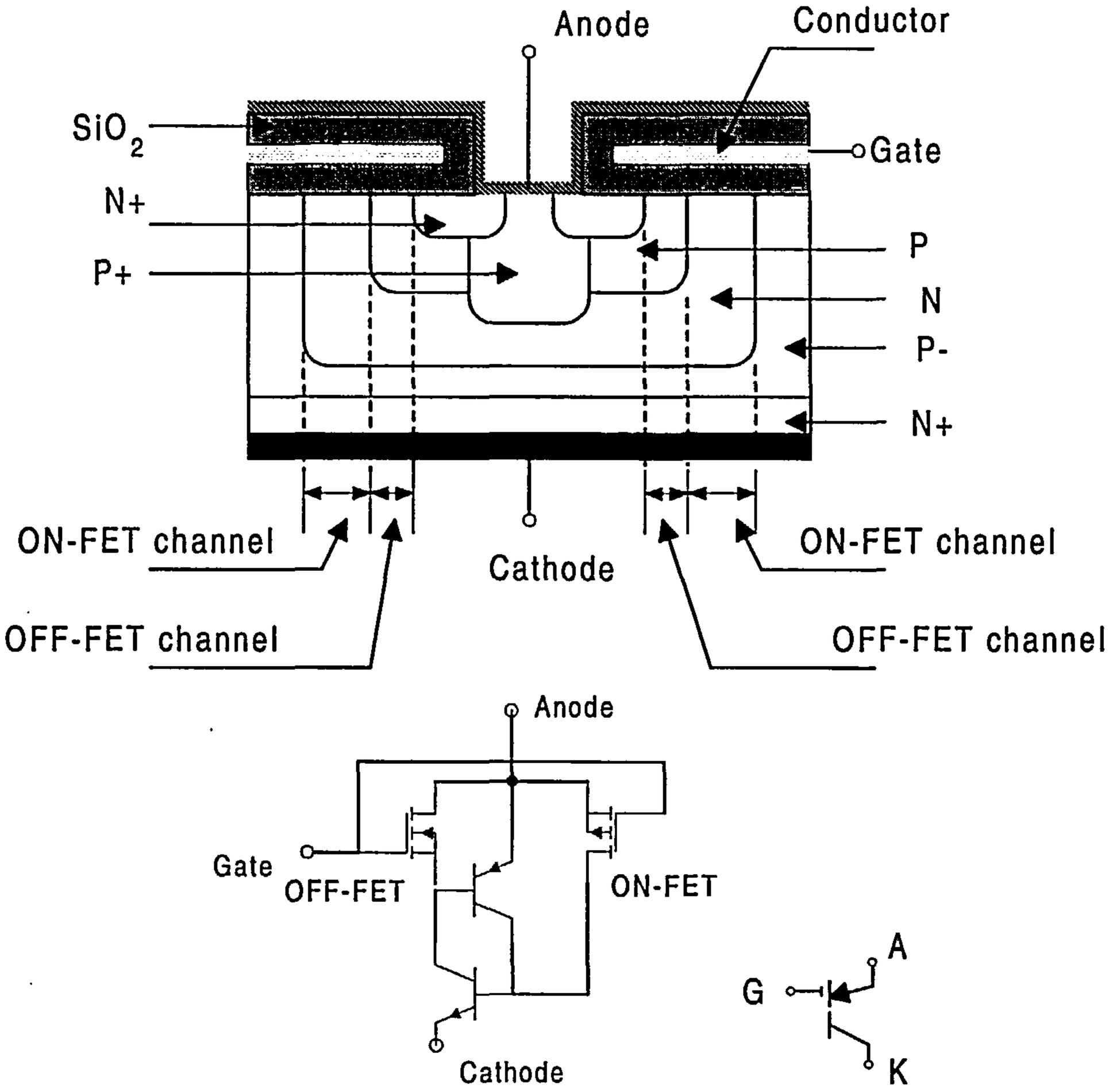

Fig. 2.20: P-MCT – Cross sectional view, equivalent circuit & circuit symbol

rises before the current falls, at turn-off.

As the MCT has a thyristor-like *pnpn* junction, its latching mechanism is similar to that of a conventional thyristor. However, it is advisable to keep the gating signal steady, in both the on and off-states, to avoid unwanted turn-ons, or turn-offs, due to the large dv/dt applied to the anode-cathode terminals of the MCT.

Unlike the MOSFET, the MCT's input capacitance is fixed due to the absence of the Miller effect. At high temperature, problems due to leakage current may occur owing to the higher channel resistance of the OFF-FET. Consequently, the turn-off current capability is reduced.

The typical ratings for the MCT are claimed to be 2500V/200A. Nevertheless, the rating will never match the GTO capabilities as the MCT has a very-dense-cell structure with very-small-feature size. This reduces the current rating of the device. However, the MCT can be easily

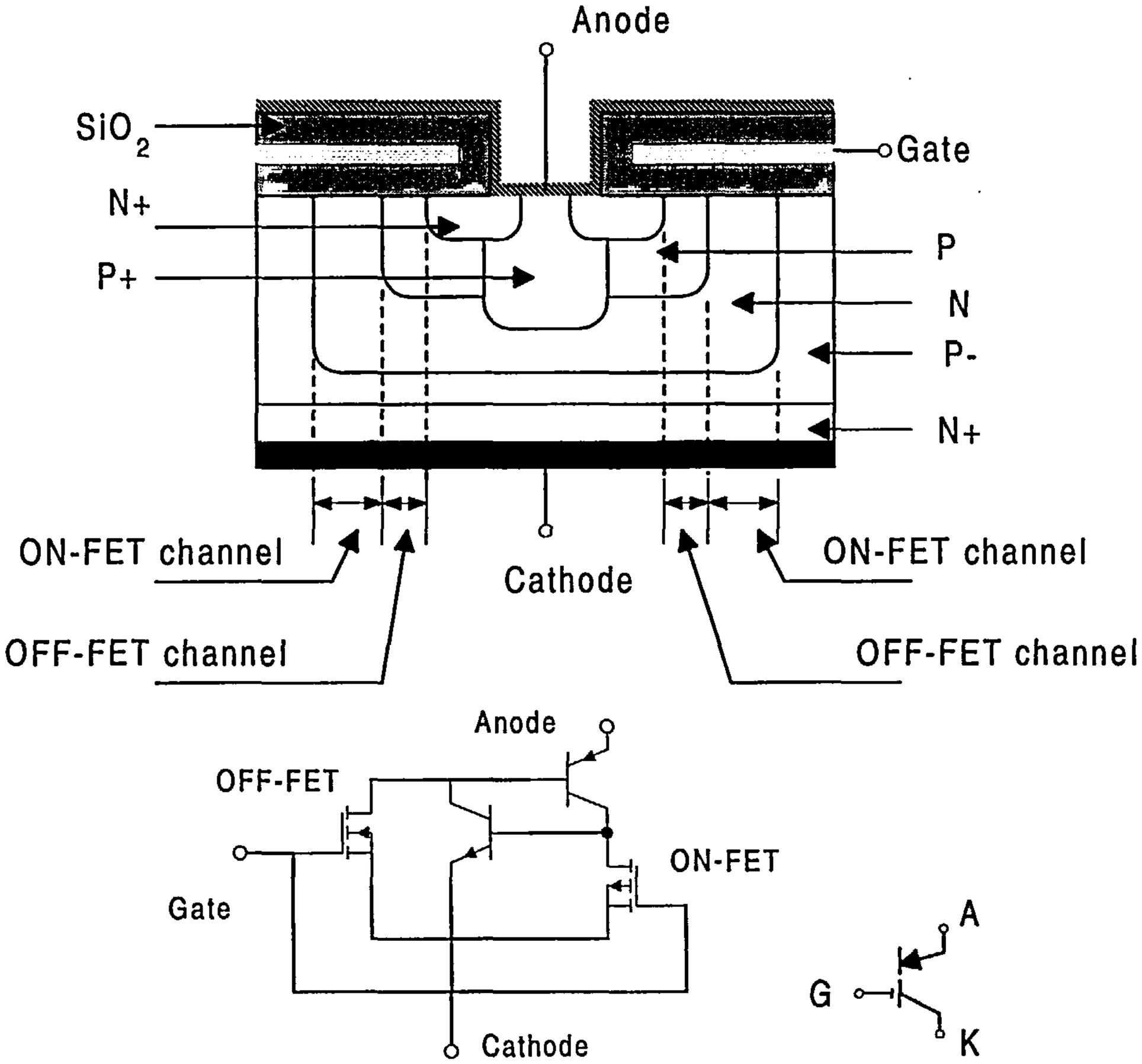

Fig. 2.21: N-MCT – Cross sectional view, equivalent circuit & circuit symbol

connected in series-parallel combinations for higher power requirements. Good static-current sharing can be achieved by paralleling MCT devices with the same forward-voltage drop, while good dynamic current sharing can only be obtained by devices with same turn-on voltage in addition to equal forward voltage drop [38].

The device is an asymmetrical-blocking device, meaning it has little reverse-blocking capability. Its quasi-square safe-operating area is limited by the junction temperature. Its high switching-speed, which depends mainly on carrier recombination-time, device thickness and turn-off di/dt, is comparable to the IGBT, but it has a lower on-state loss than the IGBT. The MCT has a higher di/dt rating than the IGBT.

MCTs do not exhibit extreme differences when used as hard-switching devices or soft-switching devices, as found in the IGBTs. Numerous tests were reported in [30,38]. Nevertheless, when used as soft-switching devices, care must be taken to ensure that high-current spikes do not occur at turn-on. The unwanted phenomena is usually caused by the charging of the resonant capacitor(s)

in the resonant circuit before the MCTs turn-on and subsequent discharging during turn-on of the devices. The high-current spikes can be avoided by having more evenly distributed ON-FETs across the device and/or reducing the charge in the p-region. The switching loss is low at zero-voltage turn-off instant, and it is said to be three times lower than those used as hard-switching devices. Increasing the value of the resonant capacitor slightly, helps to reduce the energy dissipation in the devices. However, this may cause high turn-on switching losses.

Temperature has shown a great effect on the turn-off switching losses of MCTs. Increase in temperature causes less power dissipation at turn-on, but gives rise to turn-off switching losses. This is because, with increase temperature, at turn-on, faster plasma spreads across the devices leading to a faster turn-on process; whilst at turn-off, the minority carrier lifetime increases, resulting in longer re-combination process in the devices.

Another downside when the devices are used in soft-switching is the severe derating of current turn-off capability of MCTs caused by the non-uniform distribution of stray inductance present in the resonant circuit.

2.7.7 Comparisons of the Devices

From [7,8,23,39–44] and the above discussions, comparisons of the devices from the point of view of switching speed and power rating can be summarized in the chart depicted below.

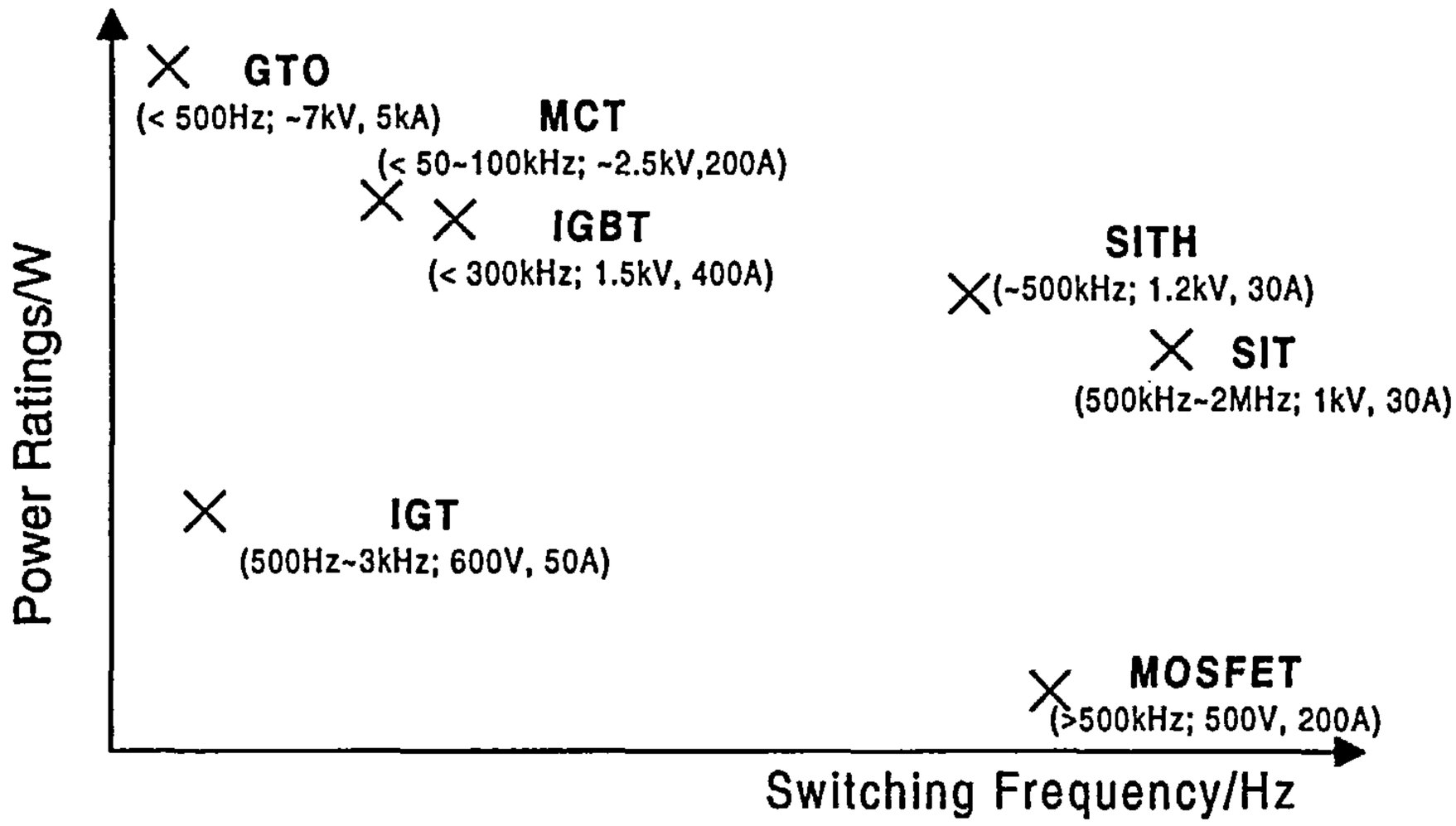

Fig. 2.22: Comparison of devices in terms of their switching speed & power rating

From the chart, it can be seen that, at the high end of the power range of today's electronics, the GTOs are still the main devices for consideration, whereas MOSFETs are preferred at the high

end of the frequency range. Having said that, devices like high-voltage MCTs [29] and SIT may well become viable options in high-power and/or high-frequency applications. There are even devices like the *zero-turn-off-time thyristor/ZTO* [tho, 1987,mar, 1987], which are optimized specially for soft-switching applications at high power levels.

However, in order to fully maximize the capability of the switching devices in soft-switching operations, choices of devices have to be made not only based on the speed and power-rating requirements, but also based on the type on resonant topology, operation above, below or at resonance, the type of resonant methods, i.e. either zero-current-switching or zero-voltage-switching or both[15], effects of the passive elements on the devices and so on to obtain the highest efficiency possible. Thus, it is important to note the different-characteristics of semiconductor devices when used as soft-switching or hard-switching devices. For example, in soft-switching operations, the current waveform with the largest 'current-time' area, i.e. area under the curve of device current plotted against time, does not necessarily generate the highest switching losses, which is definitely true in hard-switching. Moreover, in soft-switching, the voltage waveform during turn-off is highly influenced by the current waveform, which may increase the turn-off energies although the tail-current amplitude decreases [30].

It is expected that more devices will be optimized for resonant applications due to the quest for soft-switching techniques. Some of the attributes of resonant-optimized devices are, for example, absence of tail bump, reduced sensitivity of current to temperature, reduced internal inductance in the device package, less di/dt dependent on the forward drop and increased voltage rating trading-off for safe-operating-area [Widjaja et al., 1995].

2.8 Conclusion

This chapter has covered the basic principles of traditional resonant-switching based on simple series-resonant and parallel-resonant circuits. Simple analyses of the converters were given. This is followed by above- and below-resonant-switching conditions. Basic semiconductor devices were covered and compared. The study has shown that IGBT and MOSFET are currently the two most practical devices to be used in the resonant converters that are considered in the following chapters.

[15]The ZVS condition is a simpler scheme as the switching of the device occurs when the voltage across the device is zero. On the other hand, the ZCS requires more stringent circuit conditions and component values to ensure a zero current before the device is switched [Li et al., 1996].

Chapter 3

Review of Resonant-converter Classifications

3.1 Introduction

Although resonant converters have been around for quite sometime, the literature on converter classifications is relatively scarce. This makes systematic studies on them difficult, especially for newcomers. However, there are review papers on the topic [7,9,18,45–54], which should be credited for the effort of providing overall ideas on a large number of resonant converters. Nonetheless, the reported literature is hardly consistent and is contradictory occasionally, albeit that most of them have been written based on topological analysis. Thus, the aim of this chapter, which itself relies heavily on [7,9,18,45–54], is that by collecting, analyzing and reviewing previous publications, a better and more consistent and complete topological overview on the subject can be presented. Selected circuits are used as examples. The discrepancies in other papers are pointed out whenever appropriate. Even so, it must be remembered that research in this area is still very active, and newly invented soft-switching-converter topologies do tend to take time to mature. Also due to space considerations, detailed analyses of resonant converters are not given. However, relevant references are given to aid further study.

In this chapter, converters are reviewed and categorized according to the following

- combination of the voltage, or current, input-source
- topological location of the resonant network, which may be load, switch and dc/ac bus types
- switching strategies that result in zero-current and/or zero-voltage switching
- series or parallel types of resonance

- other special features possessed by the converters. For example, short-circuit and open circuit protection, regulated output-power etc..

The *Converter* is used as a generic term to refer to any power-conversion stage.

1. **Load Resonant**

   Load-resonant converters use the load as part of the resonant tank to help create the zero-current and/or zero-voltage-switching conditions. The power flow to the load is controlled by the impedance of the resonant tank, basically by the switching frequency, f_s [7].

2. **Switch Resonant**

   Switch-resonant converters place the resonant components around the power switches. The duty ratio of the switch is determined by the period of the resonant cycle [45, 55], unless an additional commutation switch is used.

3. **Link Resonant**

   Link-resonant converters contain the resonant components either in parallel or in series with the supply connected to the converters, and the input bus oscillates in order to allow zero-current and/or zero-voltage commutation [54].

3.2 Load-resonant Converters

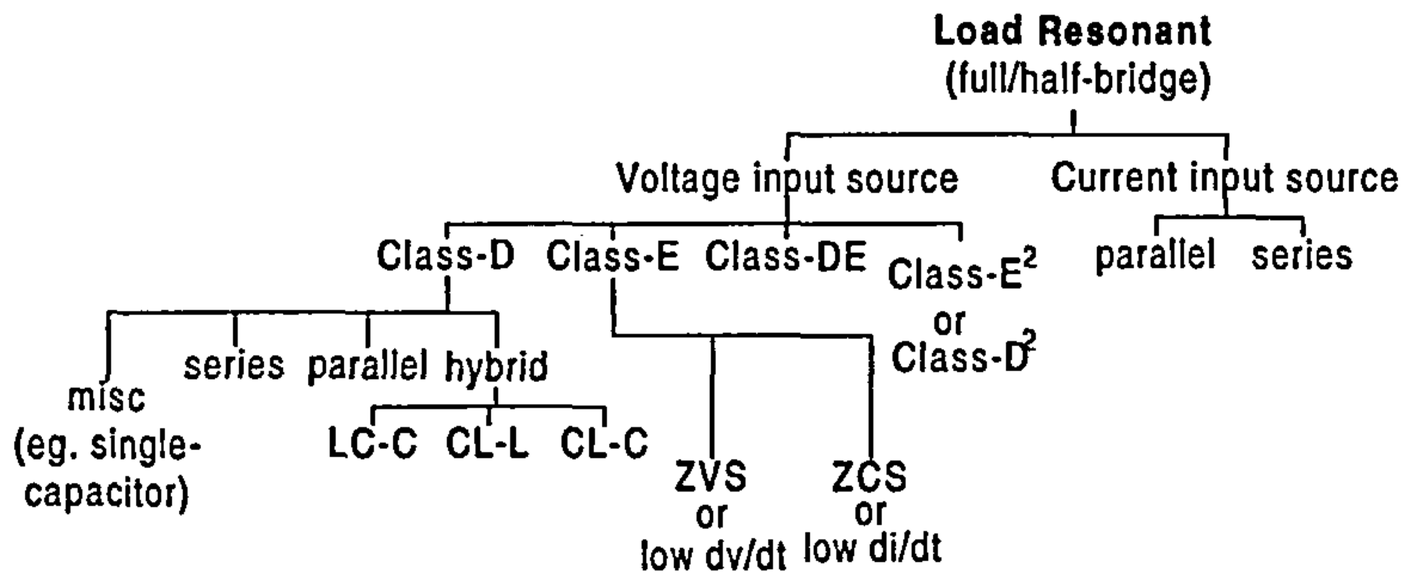

Fig. 3.1: Family of load-resonant converters

There are two main types of bridge configuration, which are the full-bridge and half-bridge. They are classified under *voltage-input source* and *current-input source.* Within the voltage source, there are three common classes, which are Class-D, Class-E, Class-DE and classes cascaded from the class itself, i.e. class-D^2 and class-E^2. Class-D alone can be further divided among *series*, *parallel* and *hybrid.* Class-E consists of *zero-voltage-switching* or *low dv/dt rectifier* and *zero-current-switching* or *low di/dt rectifier.* Class-DE, as the name implies, is a cascade of Class-D

and Class-E.

The family tree of load-resonant converters is shown in Fig. 3.1.

The loaded quality-factor, Q, of load-resonant converters has to be sufficiently high to have both the circuit current and switch current in sinusoidal and in half-wave sinusoidal forms respectively.

3.2.1 Series-load Resonant

Series Load-resonant Inverters

These converters employ the series-resonant circuit discussed in Chapter 2. A basic Class-D half-bridge series-resonant converter is shown in Fig. 3.2 [9].

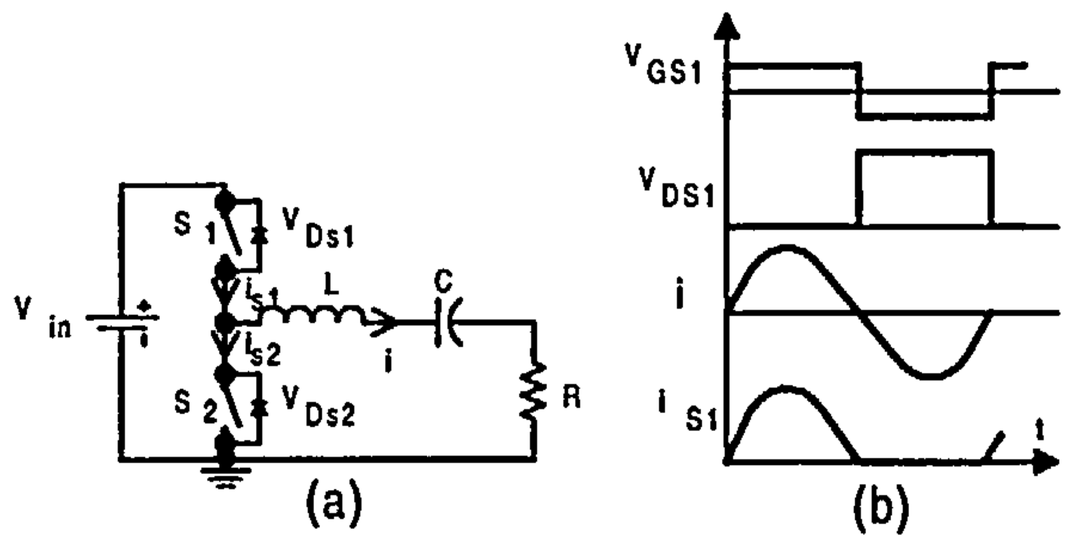

Fig. 3.2: Class-D series load-resonant inverter :- (a) circuit (b) operation waveforms at resonance

It consists of two bidirectional switches, S_1 and S_2; and a series-resonant circuit, L-C-R. If any switch is on, positive or negative current can flow through it. However, at turn-off, current flows through the anti-parallel diode. Each switch is driven with a 50% on and off duty-cycle, by non-overlapping square-wave voltage, v_{GS_1} and v_{GS_2}. *Dead time*[1] is applied between the switch transition. Voltages across the switches are usually low, i.e. equal to the supply voltage, which makes them attractive for high-power applications.

The operation waveforms are depicted in Fig. 3.2, where v_{GS} and v_{DS} are gate-source and drain-source voltages respectively.

When the converter is operated at resonant frequency, both the switches turn on and off theoretically at zero current, and the anti-parallel diodes never conduct. However, in practice, it is not operated at resonant frequency because frequency-modulation[2] techniques are used to control the output voltage or power. Therefore, the circuit is operated above resonance, i.e. in an inductive load condition to achieve zero-voltage turn-on with low switched-input capacitance and Miller

[1] *Dead time* is the time interval when both top and bottom switches are off simultaneously

[2] frequency-modulation technique is a technique where the output voltage is controlled by varying the operating frequency

effect, low gate drive power and high turn-on speed. However, lossy turn-off effect is a problem. At operation below resonant frequency, switching loss, Miller effect and the input capacitance of the switches are high, thus reducing the turn-on speed. Zero-voltage-switching can be achieved for a narrow load-range as the amplitude of the current through the resonant circuit is inversely proportional to the load.

· The output power of the full-bridge configurations is four-time higher than the half-bridge ones at the same load.

The circuit has inherent open-circuit protection, but it could fail if it were short-circuited on the output side.

The inverter can be converted to a rectifier by using the *bilateral inversion* technique[3].

Series Load-resonant dc-dc Converters

The dc-dc converter consists of a resonant inverter and a high-frequency rectifier. Current or voltage-driven rectifiers should be connected to inverters with current output or voltage output respectively.

The circuit is shown in Fig. 3.3 [9].

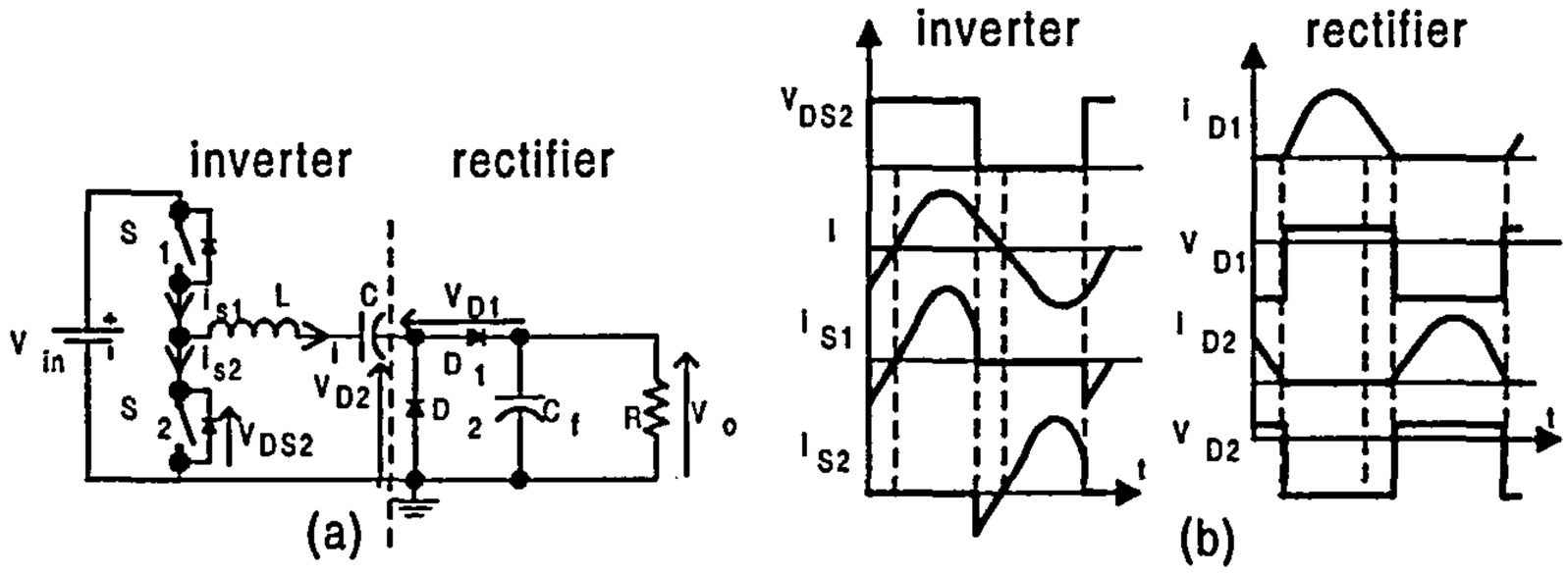

Fig. 3.3: Class-*D* series load-resonant dc-dc converter :- (a) circuit (b) operation waveforms above resonance

It consists of a series resonant inverter, depicted in Fig. 3.2, and a current-driven rectifier that will be discussed in Section 3.2.5. The operation waveforms are also shown in Fig. 3.3. Note that the operation waveforms are different from Fig. 3.2.

The converter is open-circuit proof, but it can only regulate the output voltage over a limited

[3]The principle of the *bilateral inversion* technique to covert a an inverter to a rectifier is as follows,

1. The ac load is replaced by an ac source.
2. The dc source is replaced by a dc load.
3. Switches are replaced by diodes connected in such a way that the current flows in the opposite direction

The rules are reversed for obtaining an inverter from a rectifier

load-range from full load to a reduced load. However, it would fail to regulate at no load and light loads. A preload, like another converter, can be used to obtain the regulation capability at those conditions [Dmowski et al., 1992]. However, this dissipates extra energy.

3.2.2 Parallel-load Resonant

Parallel Load-resonant Inverters

The Class-D parallel load-resonant converter is shown in Fig. 3.4 [9]. Note that C_{dc} is a dc-blocking capacitor.

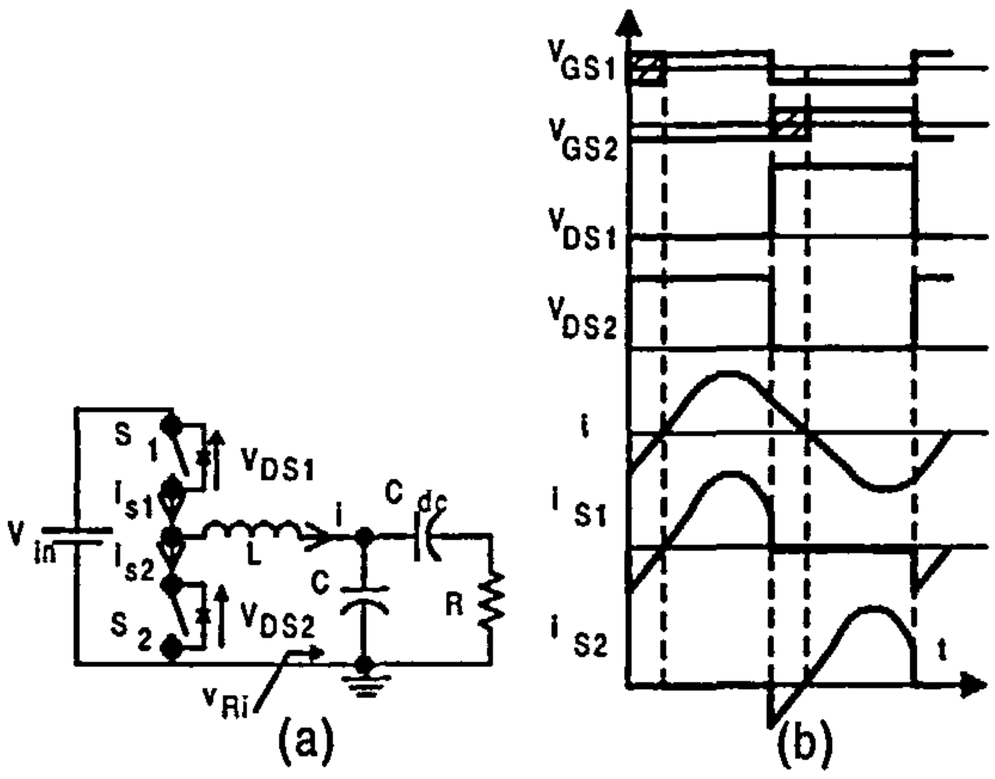

Fig. 3.4: Class-D parallel load-resonant inverter :- (a) circuit (b)operation waveforms above resonance

The operation waveforms are shown in Fig. 3.4. The switches are driven by square-wave voltages, v_{GS_1} and v_{GS_2}, with a 50% duty cycle. The L-C resonant tank effectively converts the square-wave voltage to sinusoidal voltage, v_{R_i}. The dc-blocking capacitor, C_{dc}, stops the dc component of the current going into the load. C_{dc} is placed in series with the resonant inductor, L, to prevent a short circuit of the input source, V_{in}, through the primary winding of the transformer if the upper switch is damaged

Due to the parallel connection of the load with the resonant capacitor, the switch current is almost independent of the load if the load resistance is much higher than the resonant capacitor reactance. However, at open-circuit, excessive switch-current and resonant-capacitor voltage may damage the system. It only offers inherent short-circuit protection as the resonant inductor limits the current in short-circuit conditions. Having said that, it is permissible to operate the converter from short-circuit condition right through to open-circuit condition above resonance. It would act as an impedance inverter at the resonant frequency, transferring high-load resistances to low-input

resistances. Output power increases with increasing load resistances at resonant frequency. Zero-voltage-switching can be achieved for a wide load-range as the amplitude of the current, through the resonant circuit, is nearly independent of the load.

Parallel Load-resonant dc-dc Converters

The converter is a cascaded version of the parallel load-resonant inverter as shown in Fig. 3.3 [9], with a voltage-driven rectifier .

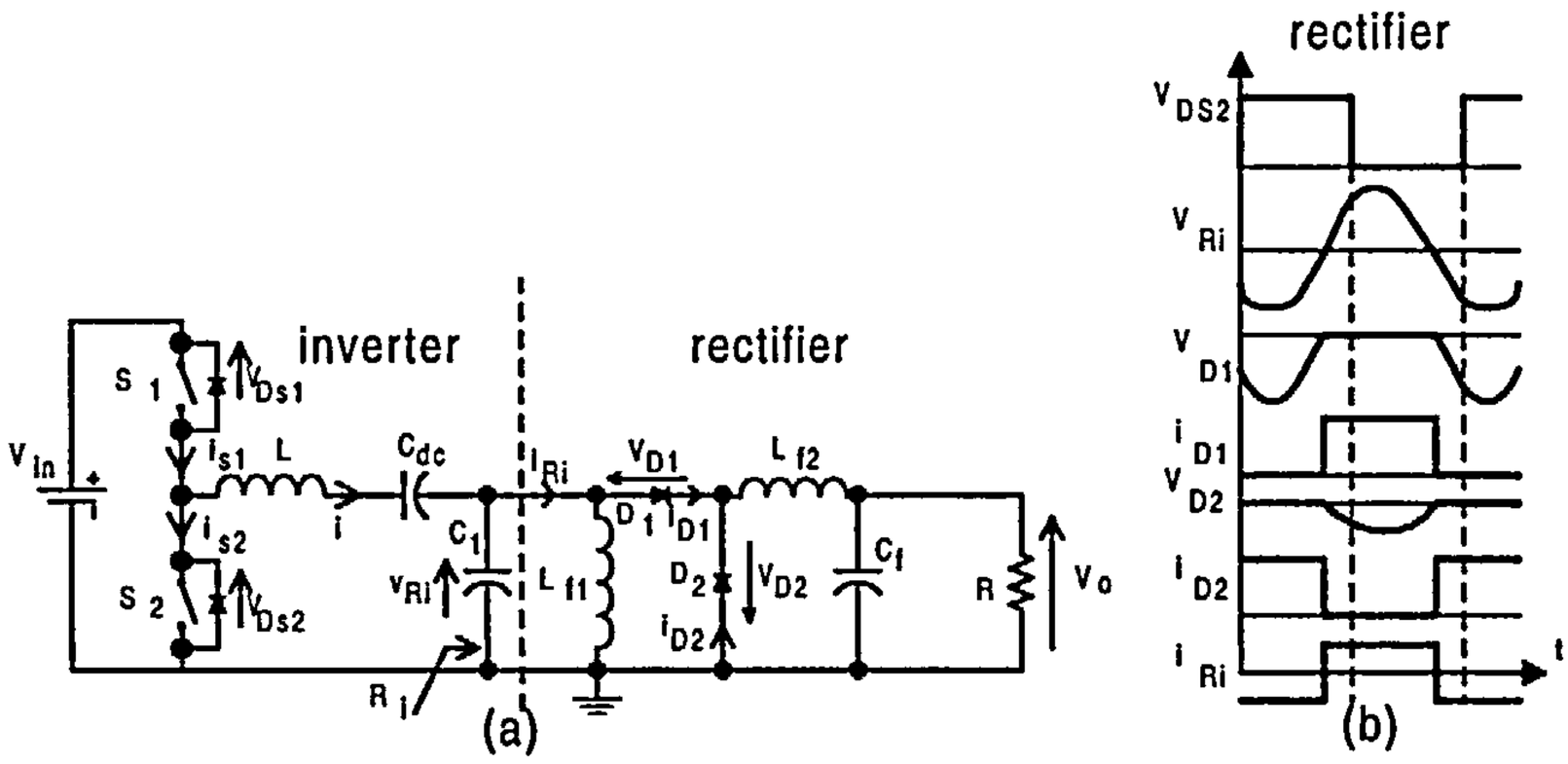

Fig. 3.5: Class-D parallel load-resonant dc-dc converter :- (a) circuit (b) operation waveforms

The rectifier part consists of two diodes, D_1 and D_2, a second order low-pass filter, L_{f_2}-C_f, and a choke, L_{f_1}. The choke could cause a short-circuit on the inverter, which is protected by the dc-blocking capacitor, C_{dc}.

The output voltage or drain-source voltage of any of switches S_1 and S_2, v_{DS}, is a square wave. The circuit current, i, flows sinusoidally through the switch, S_1, during the first-half of the on-cycle of S_1, and through switch S_2 during the second half cycle when S_2 is on. The current then charges up the resonant capacitor, C_1. The dc-blocking capacitor, C_{dc} prevents the dc-component of the current reaching the load. The inverter and rectifier waveforms are drawn in Fig. 3.3(a) and Fig. 3.5 respectively [9].

The instantaneous value of the output voltage of the inverter, which is the input voltage of the rectifier, v_{R_i}, is transferred across either diode D_1 or D_2 depending which one is on. Thus, only a part sinusoid waveform would appear across one diode at a time. The diodes also conduct the dc current flowing via the large inductive choke, L_{f_1}. Square-wave current is produced by the on-off diodes.

The inductive output filter, L_{f_2}, on the load side filters current preferentially to the load path,

instead of charging the filter capacitor, C_f. This, as a result, reduces the conduction loss in C_f.

Turn-off switching loss can be reduced for an inductive load by adding a capacitor in parallel with one of the switches and operating the gate-drive with a dead-time. Turn-off loss is negligible for an inductive load [56].

3.2.3 Hybrid-load Resonant

There are different configurations of hybrid parallel-series load resonant converters including *LC-C*, *CL-L* and *CL-C*. Only these three hybrid load-resonant converters are discussed.

LC-C-typed Hybrid Load-resonant Converters

LC-C Inverters

The topology of this inverter is similar to the series or parallel load-resonant inverters, except for an additional capacitor in parallel with the load, for the former, or an additional capacitor in series with the inductor, for the latter. The circuit is shown in Fig. 3.6 [9].

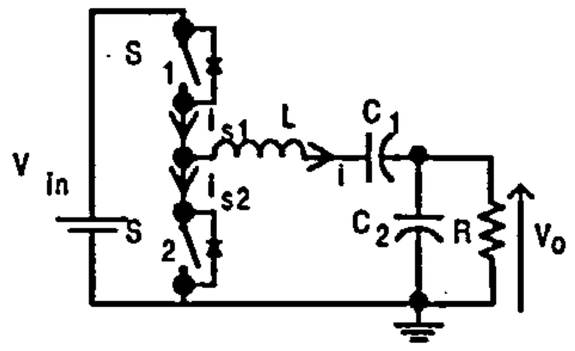

Fig. 3.6: Class-*D* *LC-C* load-resonant inverter

The inverter comprises two bidirectional switches, S_1 and S_2, which each conduct alternately with a 50% duty cycle, and a resonant circuit of L-C_1-C_2-R, where R is the ac load resistance, and v_{GS} and v_{DS} are the gate-source and drain-source voltage respectively. If a transformer is used, C_2 can be placed on either side. For a step-down inverter using a high turn-ratio transformer, a near ideal capacitor has to be used as C_2 to avoid power losses in the parallel capacitor, C_2, as a large current would flow into the C_2 path instead of the big primary inductance. The operation waveforms are similar to Fig. 3.4.

This converter can be turned into a series or parallel load-resonant inverter easily by changing the value of C_1 and C_2. C_1 is made large for a parallel one, and C_2 is made zero for a series one. Note that the transformer version of the series load-resonant inverter is effectively a *LC-C* type as the primary winding exhibits parallel stray-capacitance characteristics at high frequencies. Its

efficiency increases with increasing ratio of $C1/C2$.

The inverter is not inherently safe under the short-circuit and open-circuit conditions. At short-circuit, i.e., $R = 0$, the resonant circuit consists of L and C_1 only, unless it is above resonance, i.e. under inductive conditions. At open-circuit, i.e. $R = \infty$, the circuit comprises of L and the series combination of C_1 and C_2.

LC-C dc-dc Converters

The converter is a cascaded version of the *LC-C* inverter with a Class-*D* voltage-driven rectifier, and the circuit is shown in Fig. 3.7 [9]. It can be seen that the circuit is actually a *LC-C* inverter with the load replaced by a Class-*D* rectifier. The rectifier can be either half-wave or transformer center-tapped, or a bridge-type rectifier.

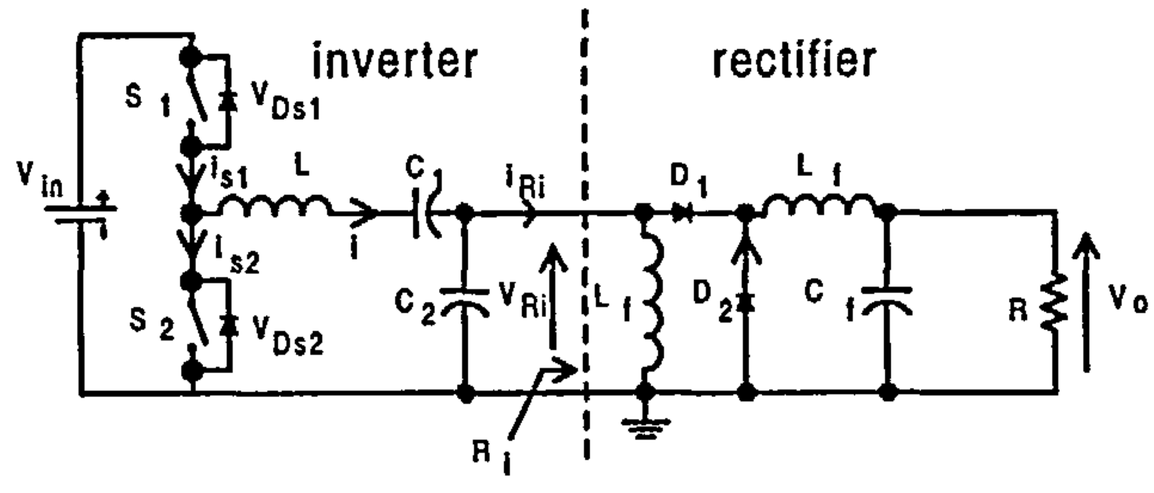

Fig. 3.7: Class-*D* *LC-C* load-resonant dc-dc converter

The inverter can be made to resemble a sinusoidal-voltage source if the reactance of capacitor, C_2, is lower than the input impedance of the rectifier. Its operation waveforms are similar to those shown in Fig. 3.5.

The dc-dc converter is able to regulate the output voltage from no-load to full-load. Neither the short-circuit nor open-circuit condition is inherently safe.

CL-L-typed Hybrid Load-resonant Converters

CL-L Inverters

The converter, shown in Fig. 3.8 comprises two resonant inductors, L_1 and L_2, with L_2 in parallel with the ac load, R, and L_1 in series with the resonant capacitor, C. The two switches, S_1 and S_2 are bidirectional [9].

This inverter is different from the transformer version of series load-resonant converter in magnetizing inductance, which is smaller in the hybrid version. It does not operate inherently-safely

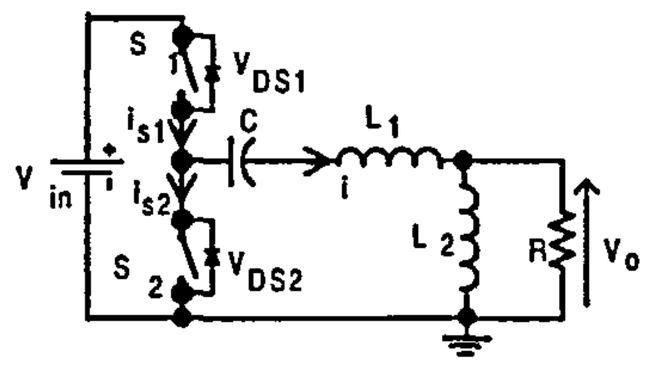

Fig. 3.8: Class-D CL-L load-resonant inverter

under short-circuit nor open-circuit conditions.

Its efficiency increases with increasing ratio of $L2/L1$.

CL-L dc-dc Converters

The converter is obtained by replacing the ac load of the inverter version, shown in Fig. 3.8 with a rectifier depicted in Fig. 3.9. Again, the inverter acts as a sinusoidal-voltage source if the reactance of L_2 is lower than the input resistance of the rectifier. The circuit is shown in Fig. 3.9 [9]. It is not inherently safe to open-circuit and short-circuit conditions.

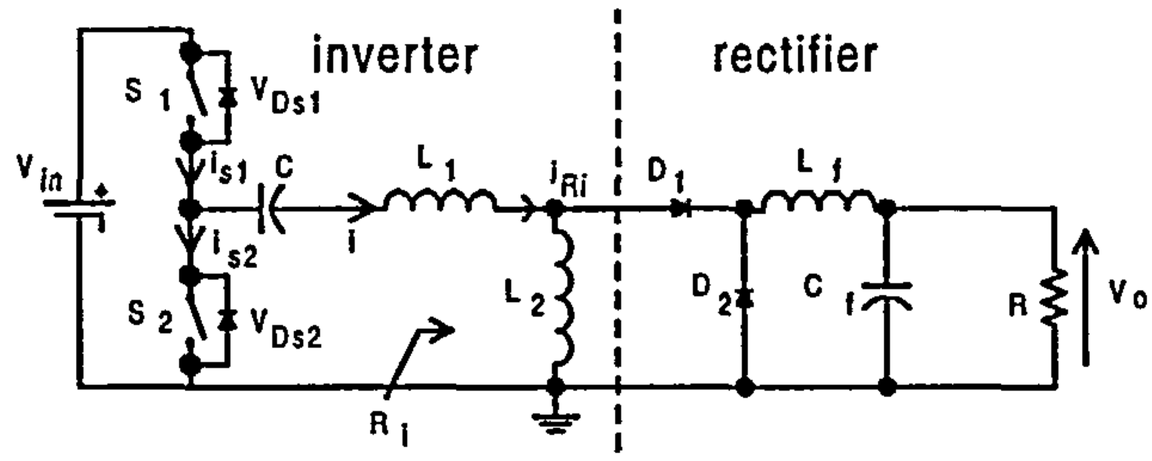

Fig. 3.9: Class-D CL-L load-resonant converter

CL-C-typed Hybrid Load-resonant Converters

This inverter, depicted in Fig. 3.10 [9], is similar to the series version with an additional resonant capacitor, C_1, on the side of either switch. The capacitor can also be divided into two parts, with one in parallel with each switch, to absorb the parasitic capacitances of the switches. The switches are driven alternately by a square-wave voltage, with long off duty-cycle, or long dead time.

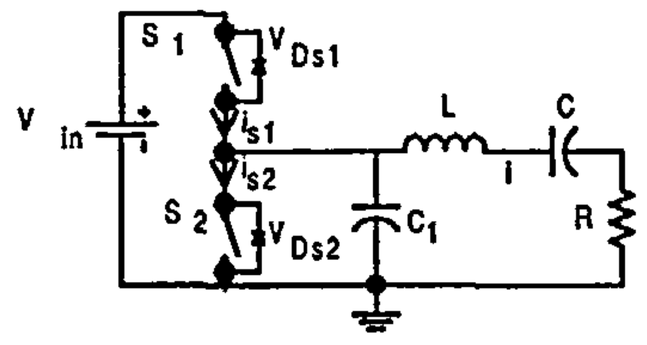

Fig. 3.10: Class-D C-LC load-resonant inverter

The operation waveforms are drawn in Fig. 3.11 [9].

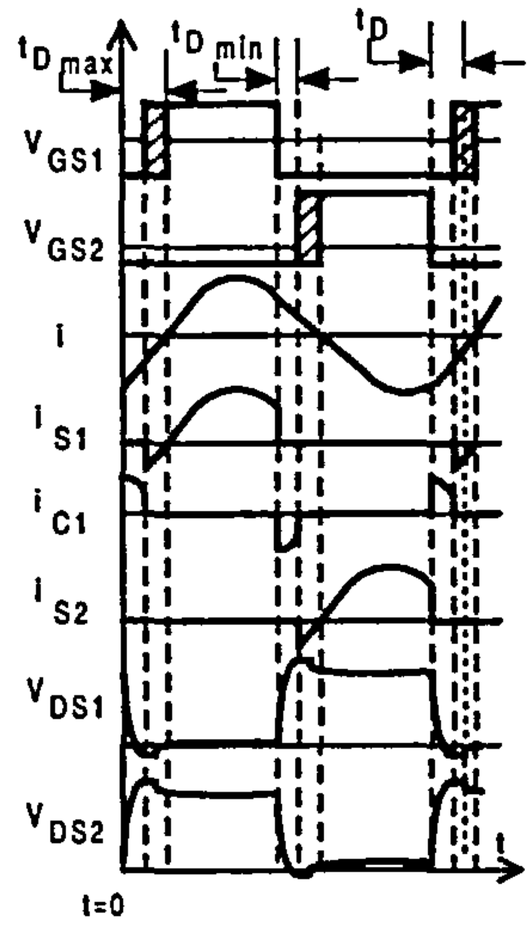

Fig. 3.11: Operation waveforms of Class-D C-LC load-resonant inverter above resonance

Initially, i.e. prior to $t = t_0$, only switch S_1 is on. Current flows via the resonant inductor, L, from the resonant circuit through S_2, shorting C_1. Voltage across S_1 is approximately equal to V_{in}.

When S_2 is turned off by the square-wave gate-source voltage, v_{GS_2}, switch S_1 is still kept off due to the dead time, t_D. All the active and passive switches are off simultaneously. The current flowing through S_2 is diverted to charge-up C_1. This causes the voltage across the capacitor, C_1, and switch, S_2, to gradually increase to V_{in}. The current flowing through S_2, i.e. i_{s_2}, falls to zero when the switch voltage gradually increases, and the voltage still remains near-to zero. Thus, the turn-off transition is at zero-voltage.

When voltage v_{DS_1} reaches the threshold value of diode, D_1, it is turned on. The current charging-up C_1 now flows upwards through D_1, and the drive voltage, v_{GS_1}, is therefore slightly below zero. Prior to turn-on, the voltage approaches zero from the negative value and v_{DS_1} turns the upper switch on at low v_{GS_1}. Thus, the turn-on switching loss is also low. After switch S_1 has turned on, the diode turns off. The diode's reverse-recovery current follows part of a sine-wave, and hence it turns off at very low di/dt.

S_1 is then turned off by v_{GS_1}. As S_2 remains off, capacitor, C_1 discharges through the resonant circuit, decreasing v_{DS_2} and thereby increasing v_{DS_1}. S_2 will be turned on again, and restarts the whole cycle.

Notice that the turn-on transitions are are natural, while turn-off transitions are forced.

The zero-level commutation can be accomplished only when it is operated above resonance so that the input current, i, lags behind the input voltage of the resonant circuit, i.e. v_{DS_2}. The

inductor current is negative during the dead-time, and hence, prior to turn-on, it can discharge the switch's shunt capacitor to bring the voltage to zero. Below resonance, the directions of the current and the input voltage are of opposite signs, and hence the converter does not commutate at zero-voltage level.

3.2.4 Single-capacitor Phase-controlled Converters

Phase-controlled modulation is used to vary the phase-shift between the output currents and voltages of two converters, which are synchronized to the same switching frequency, to control the output power delivered to the same load. Wide load and line variations are catered for.

Operation at fixed frequency allows the converters engaged in the phase-controlled-modulation technique to reduce the noise spectrum, fully utilize the magnetic components and filter the output voltage without involving complex control. These are the advantages over operation using either frequency-modulation or pulse-width-modulation techniques. However a second inductor is needed to achieve phase-controlled modulation.

One of the converters, called a single-capacitor phase-controlled inverter, employing the technique, is depicted in Fig. 3.12 [9].

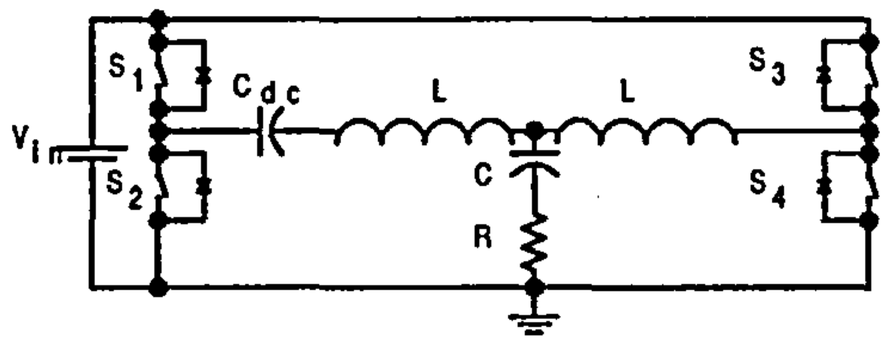

Fig. 3.12: Single-capacitor phase-controlled inverter

It consists of a dc-input voltage source, V_{in}; two switching legs comprising two switches in each leg; two resonant inductors, L; one resonant capacitor, C, a coupling capacitor, C_{dc}; and an ac load, R. The switches in both legs are commutated alternately with a duty cycle of near 50%. Zero-voltage switching is obtained by a dead-time of the switches with inductive load, i.e. above resonance switching.

The inverter is inherently open-circuit and short-circuit protected.

3.2.5 Class-E, -E^2 and -DE

Class-E

In resonant converters, zero-current and zero-voltage switching are particularly effective when zero di/dt and dv/dt also prevail respectively, as in Class-E resonant converters[4] [58–61]. This can hardly be achieved in the Class-D-type converters discussed earlier. Another major difference of Class-D and Class-E converters is Class-D uses two switches where each switch conducts 50% of the cycle while Class-E in its simplest form uses a single switch which can be operated at any duty cycle. This hence avoids the timing problem caused by two-ended, or two switches, converter configurations.

ZVS inverters and Low dv/dt Rectifiers

The basic circuit of a *Class-E ZVS inverter* is shown in Fig. 3.13 [9]. It consists of an L-C-R series resonant circuit where R is an ac load, a shunt capacitor, C_p, with the only switch, S, and a choke inductor, L_f. The shunt capacitance, C_p, includes the switch output capacitance, the choke parasitic capacitance and any stray capacitance. The choke inductor, L_f, is high enough to minimize the ac ripple on the dc supply current. I_{in}

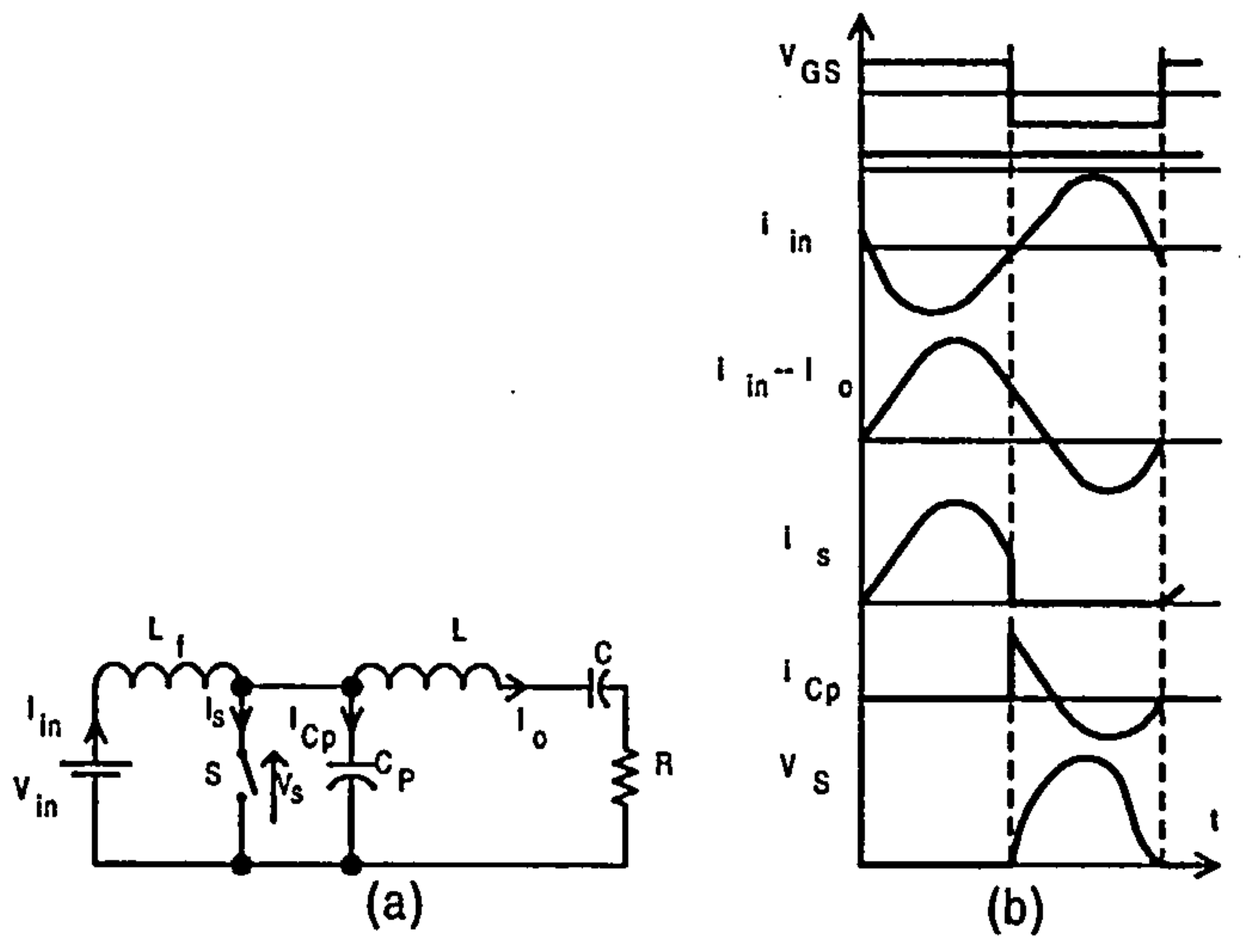

Fig. 3.13: Class-E ZVS inverter :- (a) circuit (b) waveforms in Class-E zero-voltage-switching inverter for optimum operation

The circuit operation is determined by the switch at turn-on and by the transient response of the

[4]Classes-A,B and C transistors act as current-source at non-saturated states; sinusoidal collector voltages are maintained by the parallel-tuned output circuit.

Classes-D and S, which are used interchangeably, contain two(or more) pole switching configurations that define the voltage and/or current without involving the load network. They employ either bandpass or low-pass filtering [57]

load network at turn-off [57]. At turn-on, current flows through the switch, via L_f, short-circuiting C_p, and through the resonant circuit consisting of L-C-R. At turn-off, current flows through C_p-L-C-R. These two phenomenon cause the load network to be characterized by two resonant frequencies, and two loaded quality factors at both turn-on and turn-off. At turn on, $f_{on} = \frac{1}{2\pi\sqrt{LC}}$ and $Q_{on} = \omega_{on}\frac{L}{R} = \frac{1}{\omega_{on}CR}$. At turn off, $f_{off} = \frac{1}{2\pi\sqrt{\frac{LCC_p}{C+C_p}}}$ and $Q_{off} = \omega_{off}\frac{L}{R} = \frac{1}{\frac{\omega_{off}LCC_p}{C+C_p}}$. The typical switching waveforms are shown in Fig. 3.13.

Zero-voltage-switching is obtained at turn-on because the voltage across the switch and the shunt capacitance is zero when the converter is operated between f_{on} and f_{off}, i.e. $f_{on} <$ switching frequency, $f_s < f_{off}$

An *optimum*[5] Class-E resonant converter should have the rise of the switch voltage delayed until after the switch is fully turned-off, while at turn-on, it should be at zero switch-voltage, i.e. $v_s(2\pi) = 0$, and at zero slope of the voltage waveform, i.e. $dv_s/dt|_{\omega t=2\pi} = 0$ [62,63]. The definition for the Class-E converters was extended in [57,64,65] to include any mistuned or non-optimized amplifier containing a switch and a load network to be called *suboptimum*[6] Class-E converters.

The switch current and voltage do not overlap during the switching time intervals to virtually reduce the switching loss to zero, thereby yielding high efficiency.

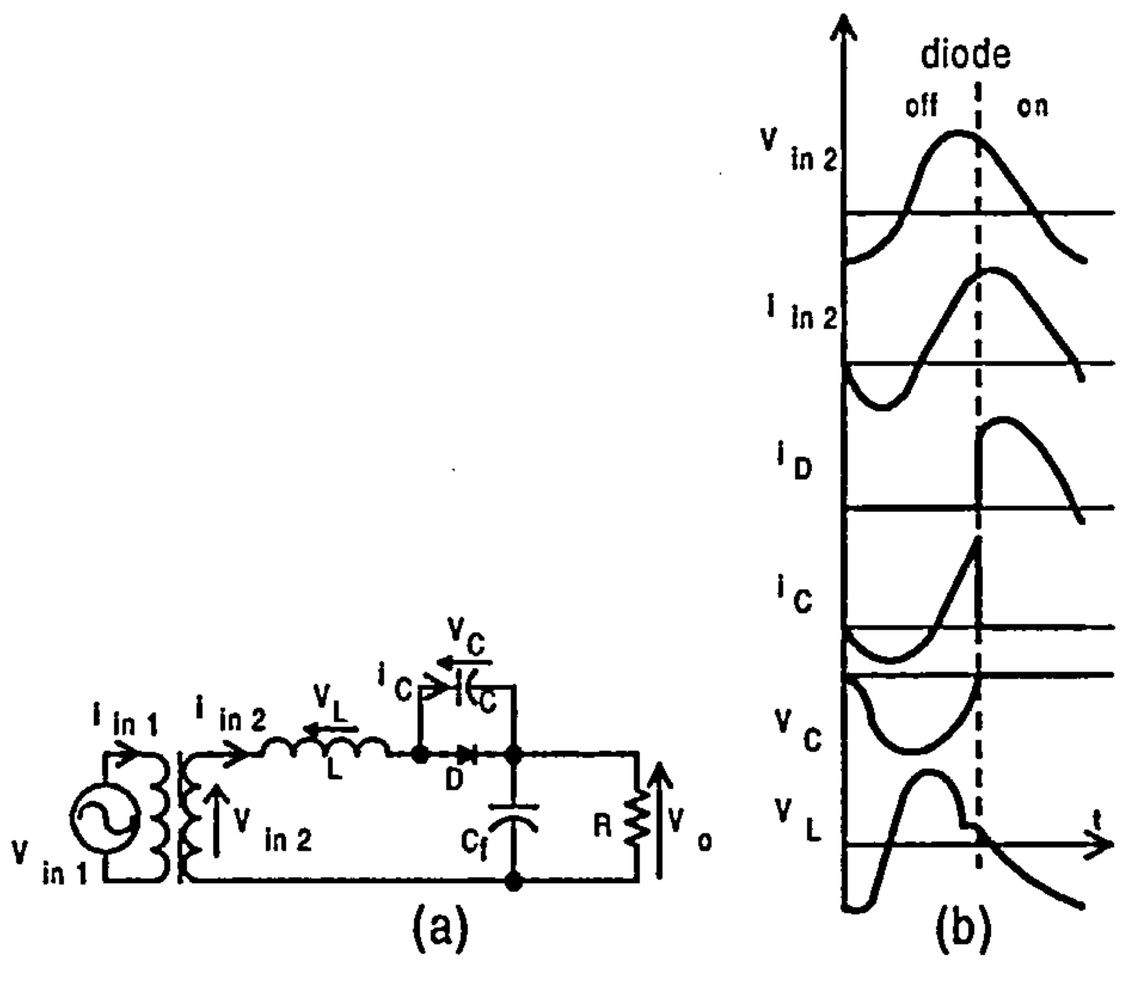

Fig. 3.14: Class-E resonant low dv/dt rectifier :- (a) circuit and models of the rectifier when the diode is off and on (b) current and voltage waveforms

Class-E *resonant low dv/dt rectifiers* [66–70] are the counterparts of the Class-E ZVS inverter

[5] *optimum*Class-E operation exhibits zero-voltage turn-on and zero voltage slope for the switch, and gradually increase of current from zero after turn-on. The switch turn-on is forced by external mechanism

[6] *suboptimum*Class-E operation exhibits zero-voltage turn-on but negative voltage slope of the switch, and negative step-change of the switch current. The switch turn on automatically when the current passing through the anti-parallel diode near to the switch

as the diode current and voltage waveforms are time-reversed images of the inverter. The rectifier shown in Fig. 3.14 [9, 71] comprises a rectifying diode, D, a resonant capacitor, C, connected in parallel with the diode, a resonant inductor, L, connected in series with the parallel combination of the diode and the capacitor, and a first-order low-pass output filter, C_f-R. It is driven by a sine-wave voltage source, v_{in_1}. The filter capacitor, C_f, is there to minimize the the ripple of the output voltage.

At the diode's turn-off, when its forward voltage decreases to zero, the secondary current, i_{in_2}, flows through the resonant inductor, L, and capacitor, C, forming a series-resonant circuit. The current shapes the voltage across the capacitor and diode, where $v_C = v_D$. The capacitor current, i_C, is zero at turn-off causing the derivative of the diode and capacitor voltage, $dv_D/dt = dv_C/dt$, to be equal to zero. When the capacitor current, i_C, crosses zero from negative to positive, the capacitor and diode voltage decrease and reach a minimum point at $i_C = 0$ before rising to zero.

At the diode's turn-on, when its voltage exceeds the threshold level, the capacitor, C, is shorted out. When its current falls to zero, the reverse-recovery current of the diode is low before turn-off as di_D/dt is low.

Because of the low dv_D/dt at both turn-off and on instants, and low di_D/dt at turn-off, switching losses are minimized.

ZCS inverters and Low dv/dt Rectifiers

A *Class-E ZCS circuit* is shown in Fig. 3.15 [9]. It consists of a switch, S, a input inductor, L_{in} connected in series with the dc voltage source, V_{in} and a load network incorporating an L-C-R series-resonant circuit [72–74].

Similar to the ZVS version, the Class-E ZCS converter operation is determined by the switch when it is closed, and by the transient response when it is open. When the switch is open, the inductor current, $i_{L_{in}}$, which is equal to the quasi-sinusoidal output current, i_R, flows through the series-resonant circuit. When the switch is turned on, the inductor voltage, $v_{L_{in}}$ equals to the supply voltage, V_{in}. $v_{L_{in}}$ produces the linearly increasing current, $i_{L_{in}}$.

At *optimum* operation, the converter has to satisfy both the ZCS conditions at turn-off, i.e. $i_s(2\pi) = 0$ and $di_s/d(\omega t)|_{\omega t=2\pi} = 0$. These ensure zero-current turn-off. The turn-on losses become comparable to saturation losses at high frequencies, as the switch current and voltage are simultaneously nonzero at turn-on. At turn-on, the parasitic capacitance of the switch takes time to discharge. During its discharging time, the switch current increases. Thus, one of the shortcomings

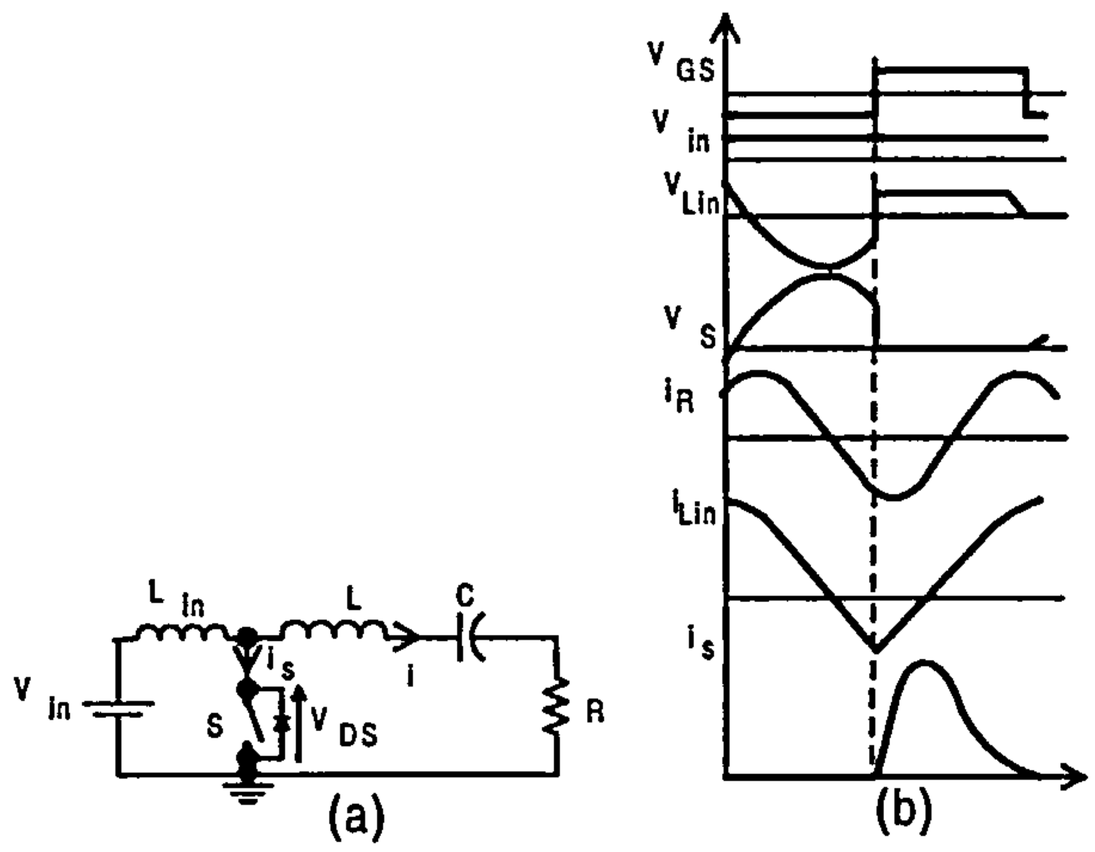

Fig. 3.15: Class-E ZCS inverter :- (a) circuit (b) current and voltage waveforms in the Class-E ZCS inverter for optimum operation

of the ZCS versions compared with the ZVS inverters is that the parasitic capacitance is not included in the inverter topology. Energy stored in the switch output capacitance is dissipated in the switch, limiting high-frequency operations. However, they suffer a lower voltage stress than ZVS inverters.

A Class-E *resonant low di/dt rectifier* with a series inductor is proposed in [75,76]. It is drawn in Fig. 3.16. The inductor, L, shapes the diode current to give the diode zero-di_D/dt turn-on and low-di_D/dt turn-off, reducing the switching losses, noise and reverse-recovery current. A large on duty-cycle of the diode is preferred to reduce the harmonics generated by the diode current pulse. The first-order low-pass filter comprising a filter capacitor, C_f, and a load resistor, R, to smooth out the dc output. The rectifier topology absorbs the diode lead inductance and any other stray inductances that are present in the circuit.

At diode turn-on, v_L and di_D/dt are both zero. Then the diode current rises slowly to reach its positive peak value before it falls linearly reaching zero to turn the diode off. The diode current is at its peak when the inductor voltage crosses zero. Low dv_D/dt is also encountered at turn-on. The diode turns off at low di_D/dt because v_L reaches a negative and finite value just before turn-off. When the diode is off, its junction capacitance, C_{j_D}, and the series inductance, L, form a parasitic series-resonant circuit. Those parasitic effects cause a step change of the diode voltage resulting in a voltage across the junction capacitor. This is followed by current oscillation in the diode, i_D, shown as a dotted line in Fig. 3.16. If the oscillation does not decay before the diode turn-on, switching losses at turn-on, in addition to the turn-off losses, can occur.

Although all sorts of advantages have been mentioned for the Class-E resonant converters, the

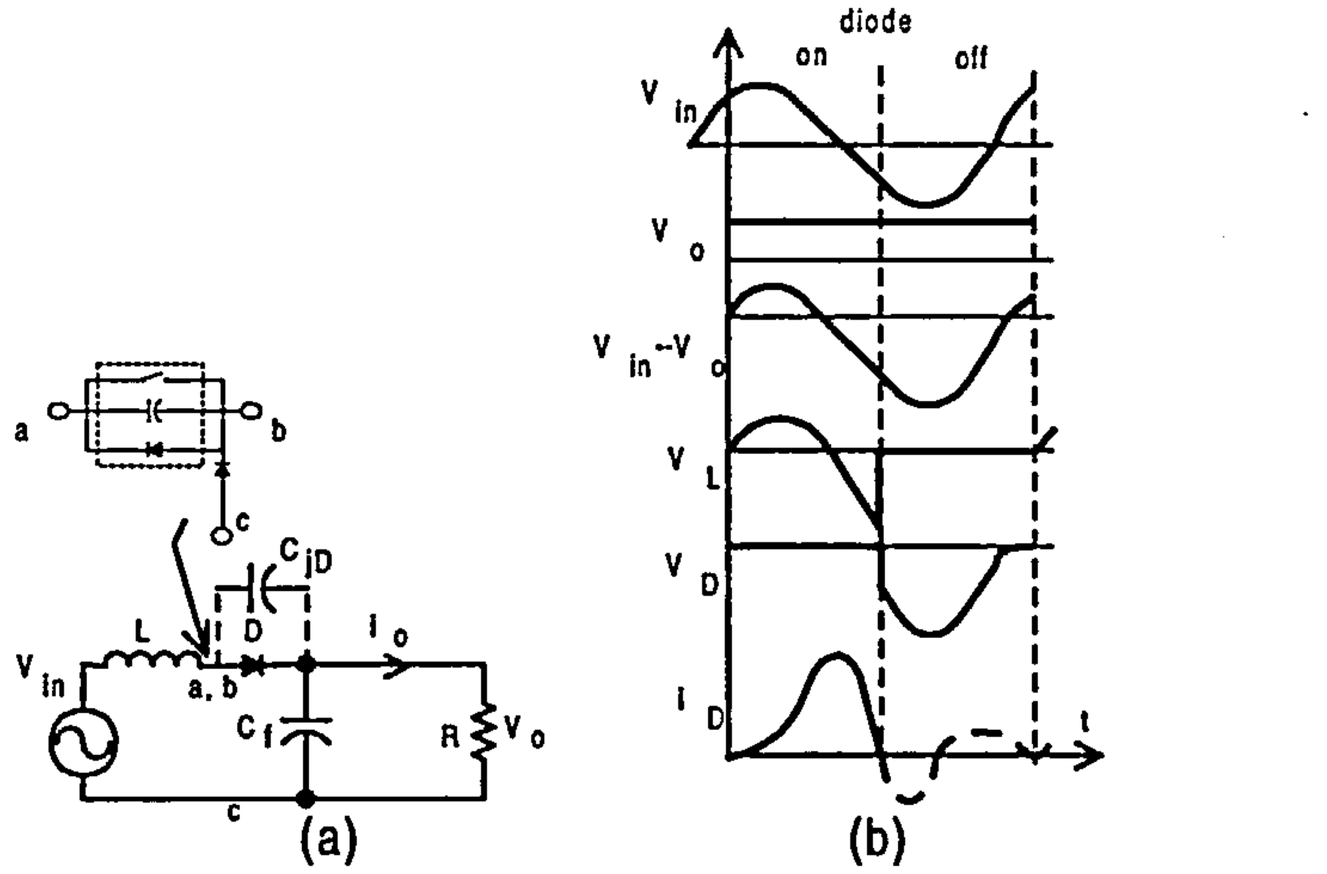

Fig. 3.16: Class-E low di/dt rectifier :- (a) circuit (b) current and voltage waveforms

switch has to be able to sustain high-peak stress, which can go as high as three to four times that of the supply voltage [58]. The authors suggested the use of a cascaded BIMOS as the switch with 60% to 40% off/on duty cycle. Another problem in Class-E converter applications is the inherent difficulty of regulating the output voltage. One of the ways to overcome this is to insert a variable-capacitance circuit consisting of a shunt capacitor and a parallel diode with another switch in series with the series resonant in the load network. This is shown in Fig. 3.16(a) [77].

Class-DE

Class-DE resonant converters can be obtained by cascading any current-output inverter with a current-driven rectifier, or any voltage-output inverter with any voltage-driven rectifier [78, 79].

The Class-DE converter, shown in Fig. 3.17, is composed of a Class-D series-resonant inverter and a Class-E current-driven low-dv/dt rectifier [80].

The Class-E rectifier comprises a diode, D, a capacitor, C_2, connected in parallel with the diode, a large filter capacitor, C_3, and an inductor, L_2. The sinusoidal current going through the series-resonant inverter drives the rectifier. The current through the choke inductor, L_2 is approximately equal to I_o. Only the power at the fundamental frequency is transfered from the inverter to the rectifier. The rectifier input impedance[7] may be represented by a series combination of input resistor, R_i, and an input capacitor, C_i, as shown in Fig. 3.17. The inductor L_2 is large enough to reduce the ripple of the output current. There is no dc component of the diode current flowing through the inductor. The C_2 capacitor absorbs any parasitic capacitance. The on-duty

[7]This input impedance is defined as the ratio of the phasor of the fundamental component of the rectifier input voltage to the phasor for of the rectifier input current

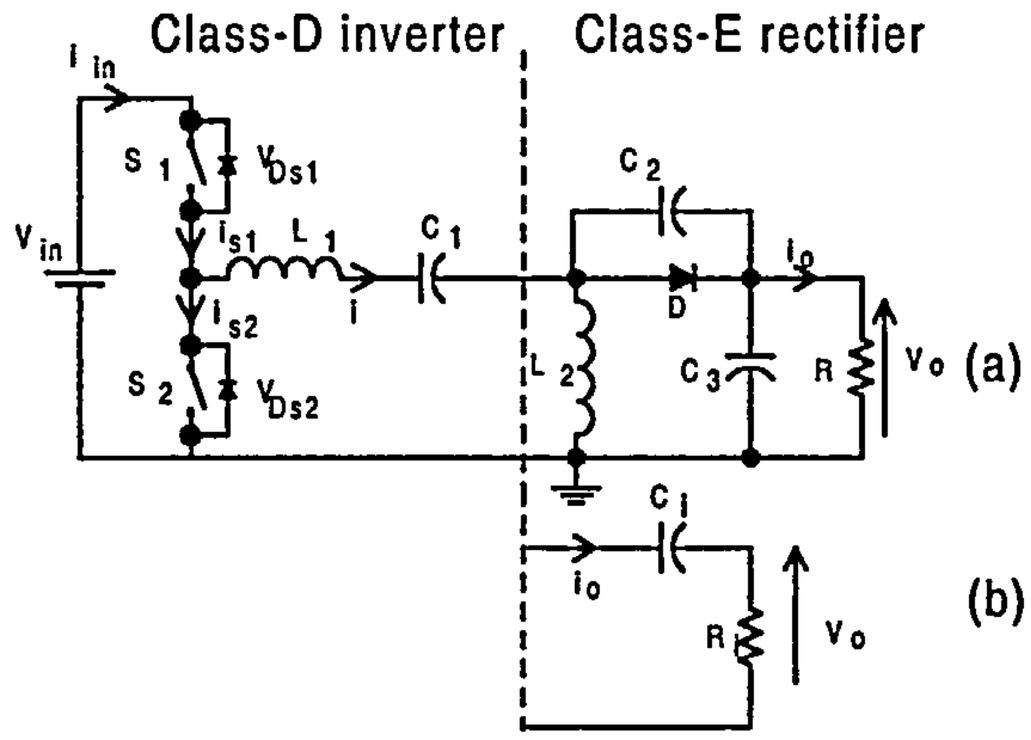

Fig. 3.17: Class-DE resonant dc-dc converter :- (a)circuit (b) basic circuit of Class-D series-resonant inverter

cycle of the diode can be made large, and it is independent of the output-voltage ripple.

The Class-D inverter employs a pair of bidirectional switches, S_1 and S_2, and a series-resonant circuit L_1-C_1-C_i-R_i, where C_i-R_i is the input impedance of the rectifier. The switches switch alternately applying a quasi-square-wave voltage to the series-resonant circuit. The resonant frequency is given by $f_0 = 1/[2\pi\sqrt{L_1 C_1 C_i/(C_1 + C_i)}]$, and the total resistance of the converter is given by the sum of the rectifier input resistance R_i, the switch on-state parasitic resistance and equivalent series resistances of the resonant components. High quality-factor gives rise to quasi-sinusoidal current through the resonant circuit. The advantage of the inverter topology is that the peak voltage of the switches has the lowest possible value, equal to the dc input voltage, V_{in}.

The operation of the system is shown in Fig. 3.18 [9]. At turn-off, the capacitor current, i_{C_2}

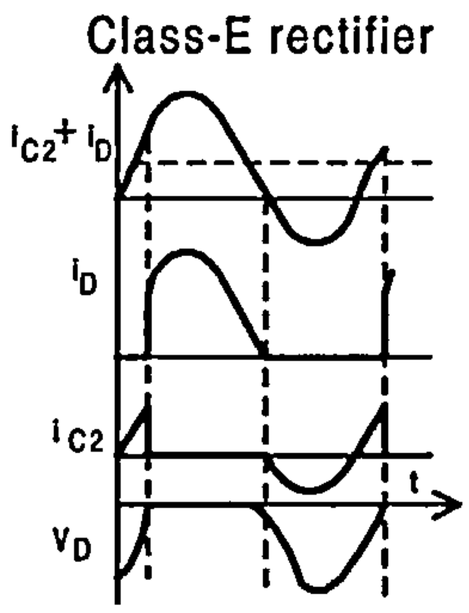

Fig. 3.18: Waveforms in Class-DE resonant dc-dc converter

and the derivative of the diode voltage, dv_D/dt are zero. The diode turns off at low di_D/dt. At turn–on, i_{C_2} is limited by the series-resonant circuit and the choke, L_2, keeping dv_D/dt of the diode low. However, the diode current has a step change at turn-on.

A *half-bridge Class-DE rectifier* and *Class-DE inverter* were proposed in [81] and [82] respectively.

The rectifier circuit drawn in Fig. 3.19 is also insensitive to capacitive effects and diffusion charge storage of the semiconductor devices used in the circuit.

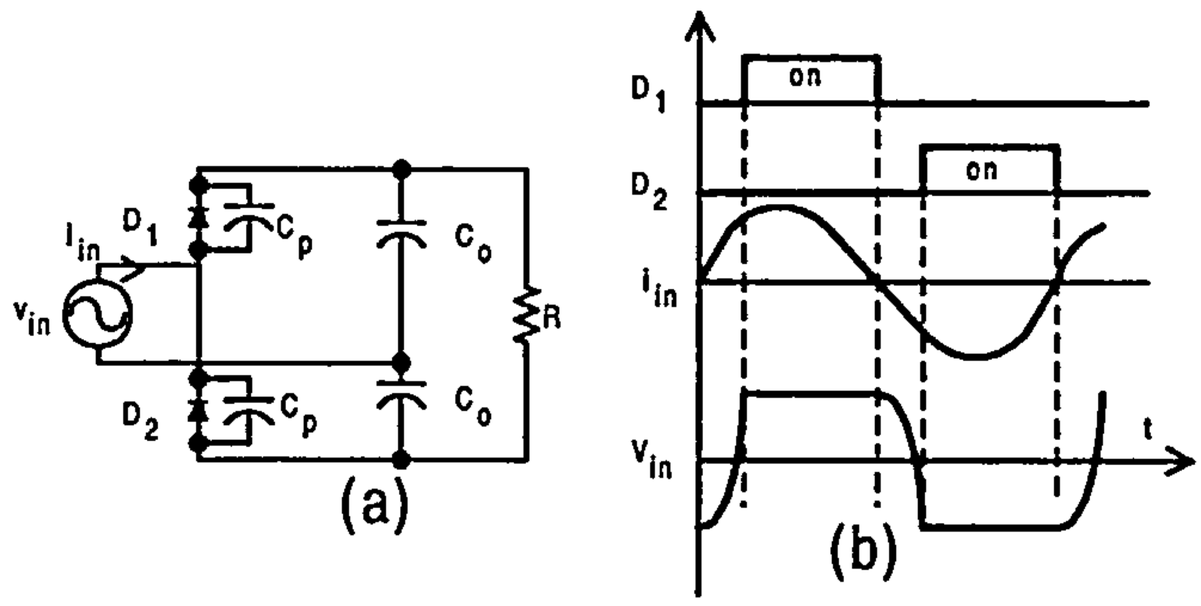

Fig. 3.19: Class-DE resonant rectifier :- (a) circuit (b) voltage and circuit waveforms

It is an ac-voltage-driven rectifier feeding two diodes with each having a shunt linear-capacitor, C_p, two output capacitors, C_o, and a dc load-resistor, R. From the waveforms depicted in Fig. 3.19, it is known that there is a dead-time between the transition states of the two diodes. Within this period, the ac input-voltage, v_{in} changes sign from $-V_o/2$ to $V_o/2$. $V_o/2$ is reached when one of the diodes turns on until the ac input-current, i_{in}, changes sign. The diode then starts to block and this diverts the current to charge up the total capacitance i.e. $2 \times C_p$. The cycle repeats. Note that at $t = 0$, $dv/dt = i/(2 \times C_p) = 0$, giving a Class-$E$ transition. Both diodes turn off when i_{in} crosses zero.

The circuit for a *Class-DE inverter* shown in Fig. 3.20 is a close relative to the Class-DE rectifier in Fig. 3.19.

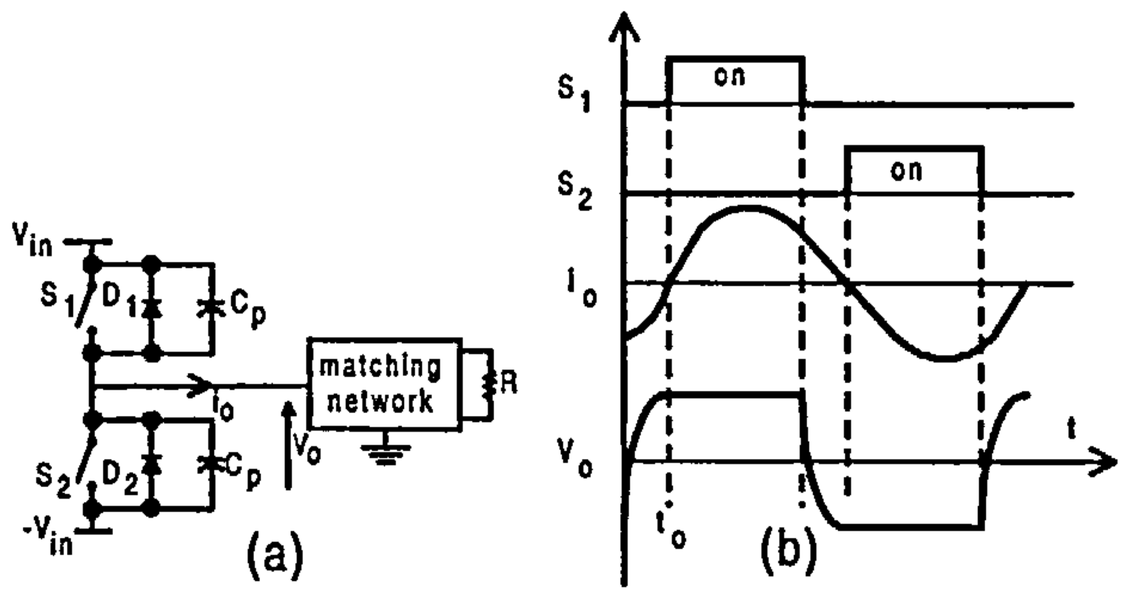

Fig. 3.20: Class-DE resonant inverter :- (a) circuit (b) voltage and circuit waveforms

It is supplied by a $\pm V_{in}$. It has two switches, S_1 and S_2, with each having a shunt capacitor, C_p and a diode, D. At $t = 0$, S_2 opens, the total switch capacitance, $2 \times C_p$ is charged up by the

negative current, i_o raising the inverter output voltage , v_o, from $-V$ to V. The diode D_1 prevents the voltage from rising further. During the 'flat' period, switch, S_1 is turned on at zero dv/dt giving Class-E transition. The matching network is to force the inverter output current waveform, i_o to be almost sinusoidal. Note that the, the switches turn on at zero output current.

Some of the advantages of the Class-DE resonant converters are

- capable of regulating the dc-output voltage for load-resistance ranging from full-load to no-load
- narrow switching frequency is sufficient to regulate the dc-output voltage against the load and line variations [8]
- the maximum peak voltage and current occur at full-load
- the input capacitance of the rectifier reduces with the rise in load resistance, reducing the total resonant capacitance to increase the system resonant frequency.

Class-E^2

A Class-E^2 dc/dc converter comprises a Class-E inverter and a Class-E rectifier [65, 83, 84]. Zero-voltage switching (with low dv/dt) of the switch and zero-current switching (with low di/dt) of the rectifier diode at both turn-on and turn-off transitions are obtained. The high-loaded quality factor of the system enables a narrow range of frequency required for output-voltage regulation when the load varies from full-load to infinity. In order to ensure this is achievable, a frequency-modulation loop controlling the dc output voltage and a pulse-width-modulation loop controlling the switch on-duty cycle can be modified to be used on the converter [61].

The system depicted in Fig. 3.21 is a combination of a Class-E ZVS dc/ac inverter described in Fig. 3.13 and a Class-E ZCS (low di/dt) rectifier [85]. The rectifier is slightly different from the one mentioned in Section 3.2.5, i.e. depicted in Fig. 3.14, as this one has a parallel inductor instead of a series inductor in the load network.

The operation of the rectifier part of the system is explained below, and the waveforms of the cascaded rectifier are shown in Fig. 3.22.

When the diode is on, the inductor current, i_{L_2}, increases linearly with voltage across it, v_L, equal to the output voltage, v_o. The diode turns off when its current reaches zero. During the diode-off period, the voltage across the inductor, v_L or V_o, is part of the sine wave., and the diode reverse voltage v_D is the difference between the output voltage, V_o, and v_L. The diode turns on

[8] if the range of the operating frequency is wide,EMC problem is severe and it is difficult to keep the radiated and conducted wave below acceptable level [77]

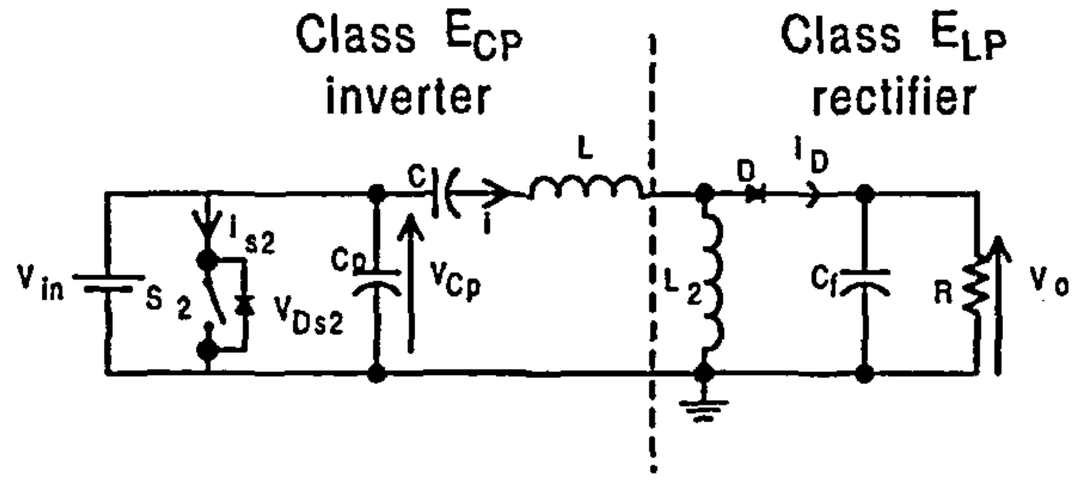

Fig. 3.21: Class-E^2 dc/dc resonant converter

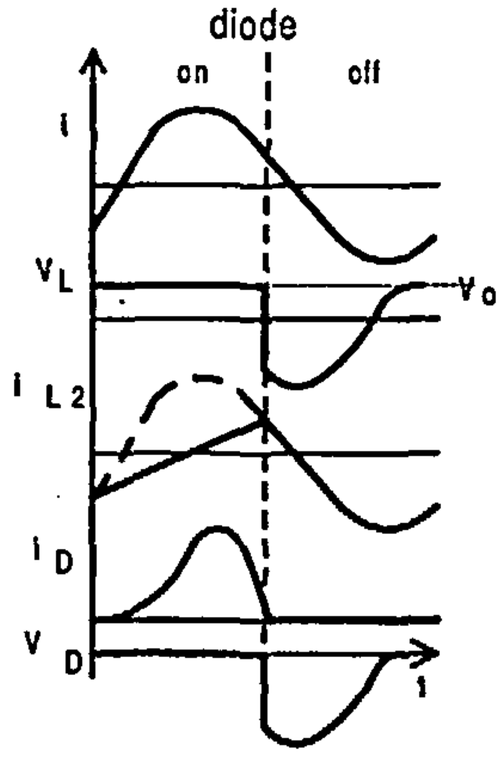

Fig. 3.22: Operation waveforms of Class-E rectifier

when the reverse voltage reaches zero. Note that the derivative of the diode current di_D/dt is zero at turn-on and its value is relatively small at turn-off, while the diode reverse voltage, v_D has a step change at turn-off and a low value of its derivative dv_D/dt at turn-on. Thus, switching losses are minimized at both transitions and the reverse-recovery effect at turn-off is reduced. However, the rectifier topology does not absorb the diode junction capacitance.

Recognize that all the converters presented in this section contain Class-E configuration in cascaded form with either Class-E itself or Class-D topology. However, although it has not been discussed here, all the Class-D types discussed earlier can be cascaded to form Class-D^2 resonant converters [86]. The cascaded converters show better output-voltage regulation and high-frequency at full-load compared with the equivalent non-cascaded form.

3.2.6 Current-source Controlled-resonant Converters

Current-source controlled-resonant converters usually dissipate substantial power in the switches because the voltage across the switches during the current pulse must be bigger than the minimum permissible value. Thus, efficient current-source converters can only be designed with carefully adjusted load network and current-pulse amplitude to obtain a reasonably large ac output voltage

in such a way than the switches remain as high-impedance current sources while the voltage across them approaches zero during current flow [63].

Class-D current-driven Rectifier

Class-D current-driven rectifiers contain two diodes, D_1 and D_2, with a 50% duty-cycle each, a large capacitive first-order output filter, C_f, and a dc load, R. The filtering function of the filter capacitor can be destroyed at very high frequency due to the dominance of its equivalent-series-inductance effect. The dc-output current is directly proportional to the amplitude of the input current. Efficiency can be improved by increasing the load resistance and the dc-output voltage. The three most common types are discussed below [68,70,87,88].

1. Half-wave Rectifier

   - The circuit and operation waveforms are shown in Fig. 3.23 [9]. When $i_{in_1} > 0$, diode D_2 is off and diode D_1 is on, providing a path for the secondary input current, i_{in_2}, to flow through D_1 into the load while charging up the filter capacitor, C_f. When $i_{in_1} < 0$, current i_{in_2} flows through D_1 that is on. The filter capacitor, C_f is discharged through the load resistor, R, maintaining a nearly constant output voltage, V_o.

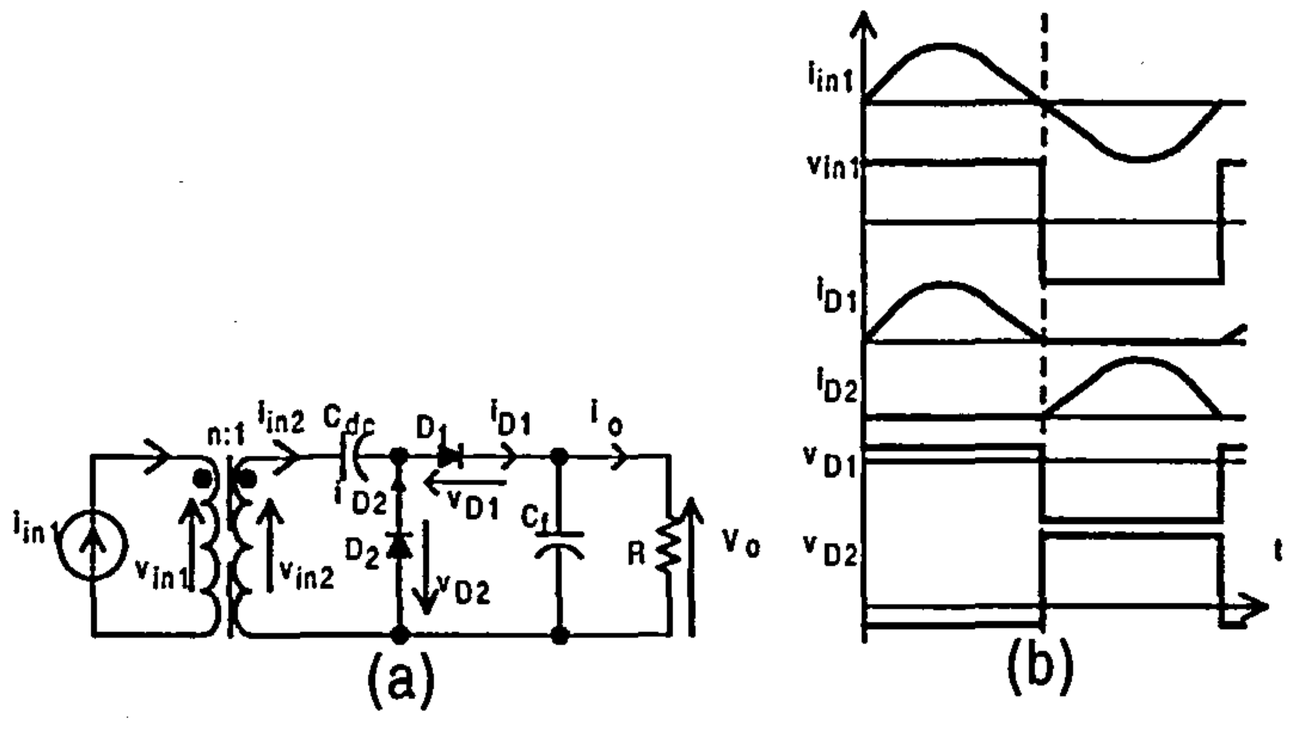

Fig. 3.23: Class-D current-driven half-wave rectifier :- (a) circuit (b) current and voltage waveforms

   - The diodes turn-off at low di/dt reducing their junction reverse-recovery current, but they turn on and off at high dv/dt causing switching losses in the junction capacitances.
   - An advantage of the rectifier is that both the source and the load can be connected to the same ground without a transformer.

2. Center-tapped Rectifier

   - The rectifier circuit driven by an ac-current source is given in Fig. 3.24 [9]. When $i_{in_1} > 0$ and $i_{in_1} < 0$, current i_{in_2} flows through D_1 and D_2 respectively, into the filter. The

waveforms are shown in Fig. 3.24. The load-voltage polarity stays the same in both cases.

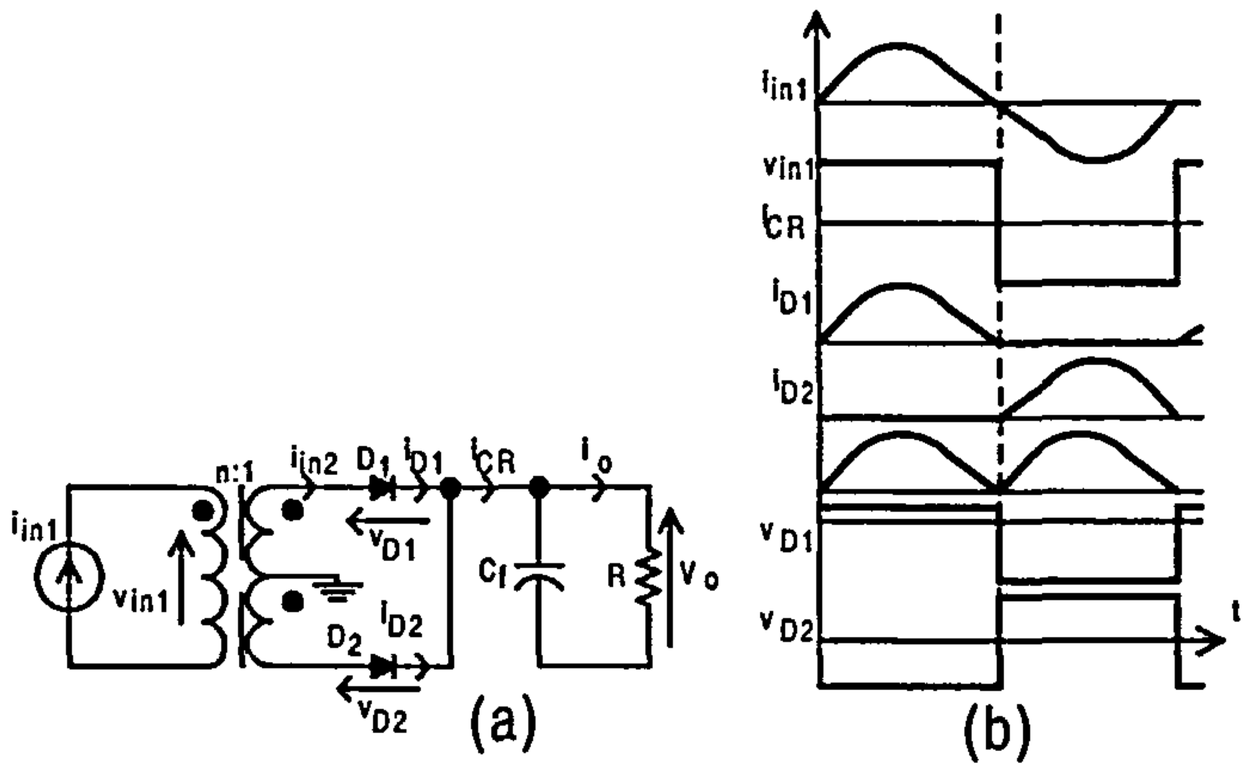

Fig. 3.24: Class-D current-driven center-tapped rectifier :- (a) circuit (b) current and voltage waveforms

3. Bridge Rectifier

- The circuit is given as Fig. 3.25. When $i_{in_1} > 0$, D_1 and D_3 are both on to provide a path for i_{in_2} to flow in the load network. When $i_{in_1} < 0$, both D_2 and D_4 are on. The operation waveforms are similar to Fig. 3.24 [9].

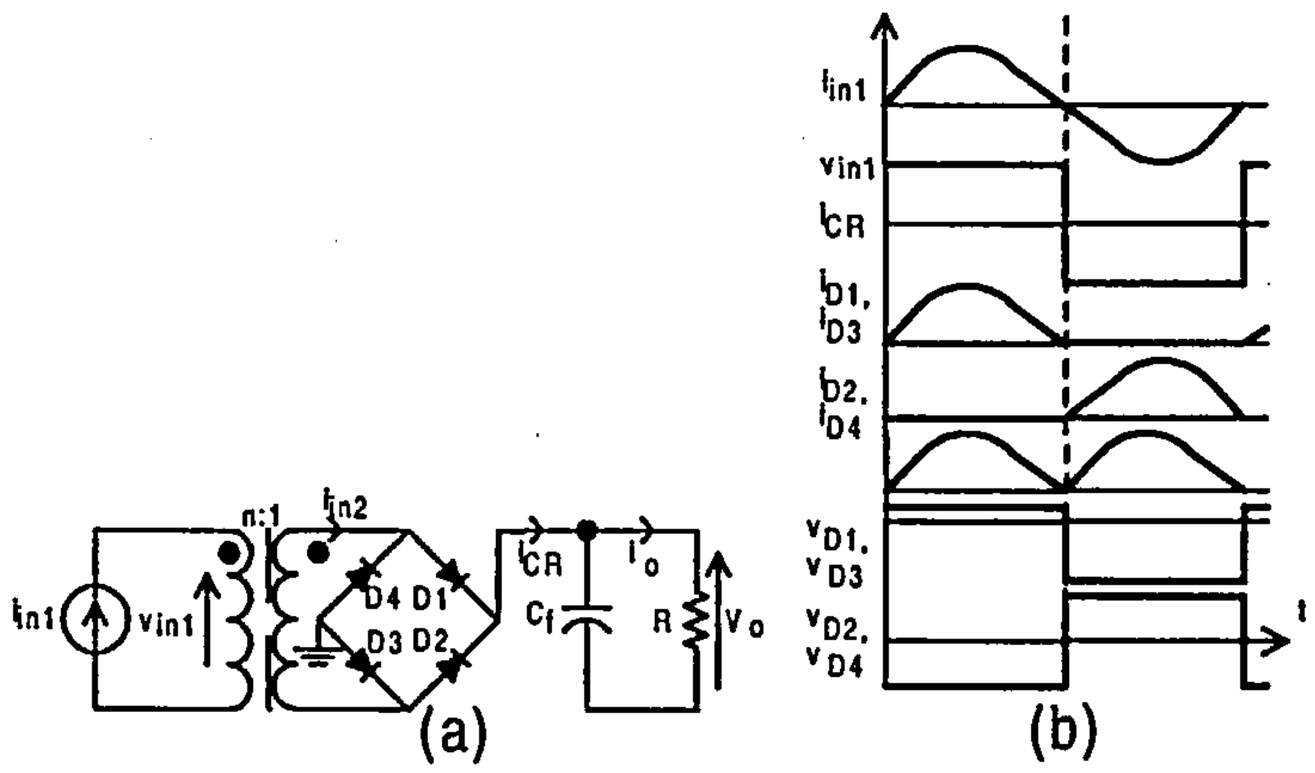

Fig. 3.25: Class-D current-driven bridge rectifier :- (a) circuit (b) current and voltage waveforms

- A transformer is needed for the source and load to be connected to the same ground.

The center-tapped rectifier is the most efficient rectifier even though it has the highest copper loss, whereas the half-wave rectifier is the least efficient. The power loss per diode in a half-wave rectifier is four times greater than the other two. For high-voltage applications, the center-tapped rectifier is not favored because it suffers from higher diode-peak-reverse voltage.

Class-*D* Parallel-current-source Resonant Inverter

In current-source inverters, the current drawn from the dc voltage supply is continuous and constant [89,90].

The circuit shown in Fig. 3.26 consists of a large inductor, L_f, two switches, S_1 and S_2 and an *R-L-C* parallel-resonant circuit.

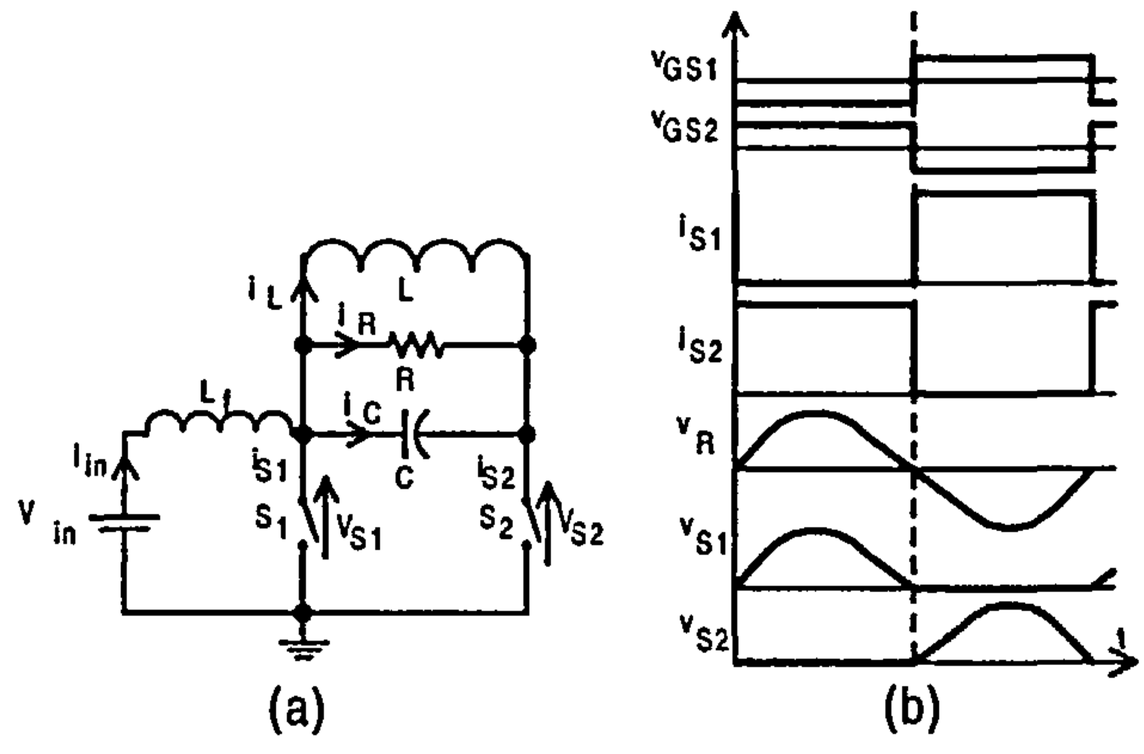

Fig. 3.26: Class-*D* parallel current-source inverter :- (a) circuit (b) operation waveforms at resonance

When switch S_1 is off and switch S_2 is on, the dc-input current, i_{in}, flows into the parallel resonant circuit with the energy transferred into the resonant circuit. When S_1 is on and S_2 is off, S_1 provides the current path, and the energy stored in the resonant circuit is partially discharged into the load. The voltage and current waveforms for the inverter at resonant, i.e. switching frequency, f_s, equals the resonant frequency, f_0, are shown in Fig. 3.26. A quasi-sinusoidal output voltage, v_o, is obtained by neglecting the harmonic impedance at the harmonic frequencies of the input current source in the analysis. At $f_s = f_0$, the input current, i_{in}, which is non-pulsating with a very small ac ripple, is in-phase with v_R providing the switches zero-voltage turn-on and off.

Above resonance, the series-inverter diode turns off at a very high di/dt, causing high reverse-recovery turn-off switching losses. Moreover, turn-on switching loss is encountered at non-zero voltage turn-on of the switches. Zero di/dt at turn off by the inverter diode and low voltage at turn-on by the switches make the operations below resonance more efficient.

Use of thyristor-inverters, in practice, to supply squarewave current to the circuit causes the resonant load to supply capacitive vars back to the inverters restricting the inverter to be operated only above resonance. A small inductor can be used in series with the resonant load to reduce the high di/dt. The output power would decrease if the operating frequency is switched above the resonant frequency by keeping the input current constant. This is a means of controlling the output

power. These types of thyristor-inverters are mostly found in induction-heating applications.

One of the major advantages of current-source parallel-resonant inverters is that the switches are driven by simple gate-drive circuit with respect to ground, and hence reducing the need for an isolation transformer.

Class-D Series-current-source Resonant Inverters

A circuit for a Class-D series current-source resonant converter is drawn as Fig. 3.27 [91]. It consists of a high-frequency symmetrical inverter stage with two input inductors, L_{in_1} and an L_{in_2}, two switches, S_1 and S_2, shunted by diodes, D_1 and D_2, and an L-C series resonant circuit connected between the switches. The ac load, R_{ac}, can be rectified to produce dc output.

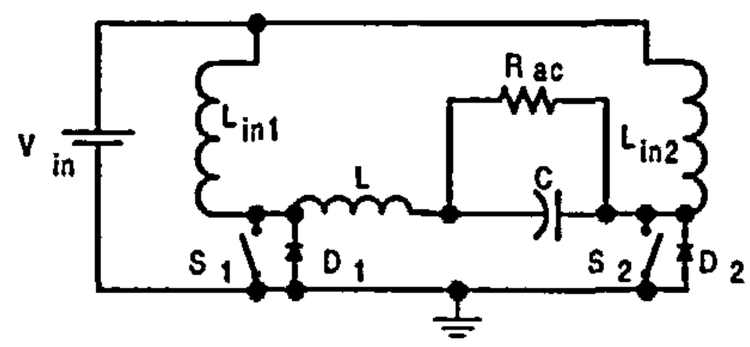

Fig. 3.27: Series-current-source resonant inverters

The detailed operations of the system are explained in [91]. This work is an improvement of the work done by Wolfs [92]. Ivensky *et. al.* proposed the use of resonant switching in the *L-type half-bridge converter* to increase the switching frequency. According to both references, the main advantages are the low input-ripple and the ground reference of the switches. However, it is suspected that the zero-current-switching L-type half-bridge converter suffers from high-voltage stressing. This appears to be the reason that they are only favored in low-to-medium input voltage applications. Each of the two-leg inductors carry half of the input current all the time. This compensates the costs of using two-leg inductors. These converters do not switch at true zero-current either. Although one of the switches turns-on, or turns-off, at its corresponding current crossing zero, the current of another switch that is still on does not go through zero at that instant as there are intervals during which both switches overlap the turn-on period.

Class-D Current-source Resonant dc-dc Converter

The converter, with non-pulsating current, is obtained by replacing the ac load of the parallel resonant inverter described in Fig. 3.26 with a Class-D voltage-driven rectifier [9]. The different types of the circuit are drawn in Fig. 3.28.

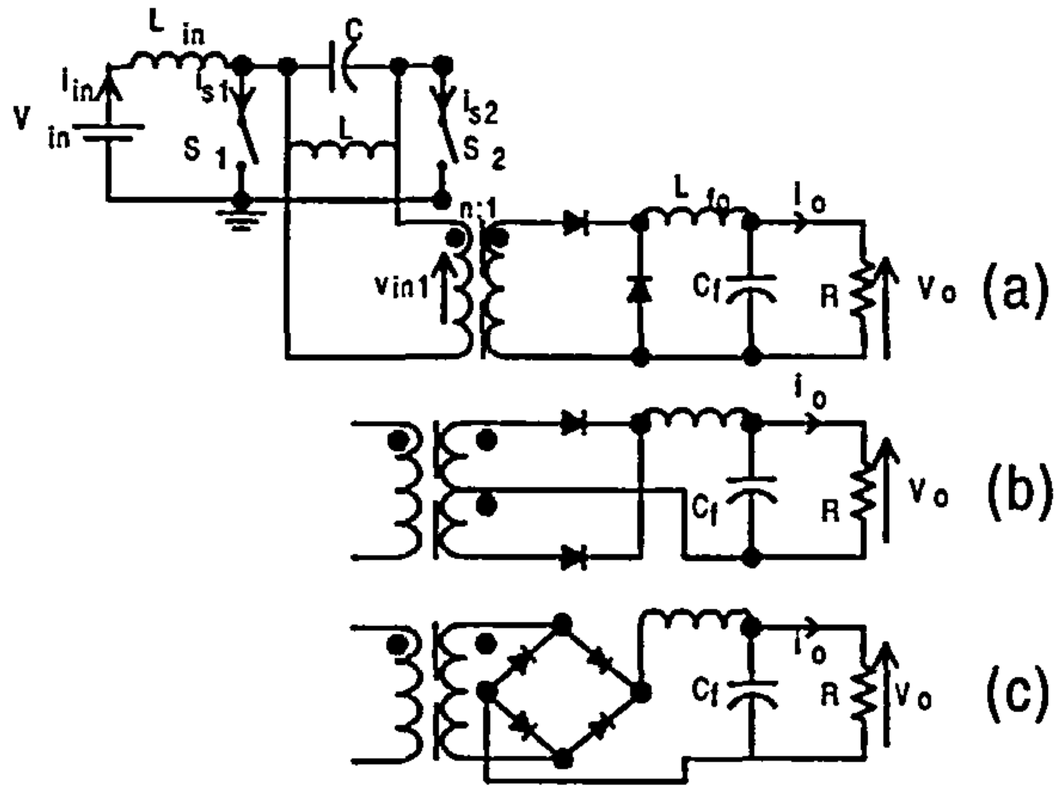

Fig. 3.28: Class-*D* current-source dc-dc converter :- (a) with a half-wave rectifier (b) with a transformer center-tapped Rectifier (c) with a bridge rectifier

One disadvantage of the converter is that the rectifier diodes turn off at a high di/dt causing switching losses while an advantage is that the output voltage can be regulated from full-load to 20% of full-load with a narrow frequency range. There have been papers reported on design [Poon and Pong, 1994] and control [Castilla et al., 1997] methods on current-source converters. Use of sliding-mode control ensures zero-voltage-switching, increased speed of response, high robustness and absence of steady-state errors in the output voltage [Castilla et al., 1997]. Duality transformation has also been used to transform voltage-driven load-resonant converters to current-driven load-resonant converters, and vice versa [Kassakian, 1982,Maixé et al., 1994]. This allows maximum performance of the converters to be achieved.

In general, the current-source converters have the disadvantage of having a low power-to-weight ratio compared to the voltage-source converters. They are mainly used in applications operating at lagging power-factor.

3.3 Switch-resonant/Quasi-resonant Family

Switch resonant converters evolved directly from the old-time thyristor-commutation circuits consisting of *L-C* components plus other auxiliary components. In order to increase the switching frequency and reduce the EMI problem, the thyristors were replaced with controllable switches, thereby shaping the switch-voltage and current to achieve zero-level commutation. Stray, parasitic inductances and capacitances can be absorbed by the resonant-tank placed around the switches [7, 8, 93]. This family was originally introduced by Liu and Lee [94]. The desire is to achieve zero-level commutation by incorporating additional passive elements around the active

switches to shape the switch-voltage and current waveform, to produce quasi-sinusoidal waveforms. That is why *switch-resonant* is also called *quasi-resonant.*

The switch-resonant family is the most 'confusing' family as various classifications have been given in the literature [18,50,53,54,95]. The terms *switch-resonant*, *quasi-resonant* and *resonant-transition* are used in a confusing fashion. For example, papers [53,54], although written by the same groups of authors, define *resonant-transition* and *quasi-resonant* differently, and they are also classified under different families. Other similar differences will be pointed out in the text here.

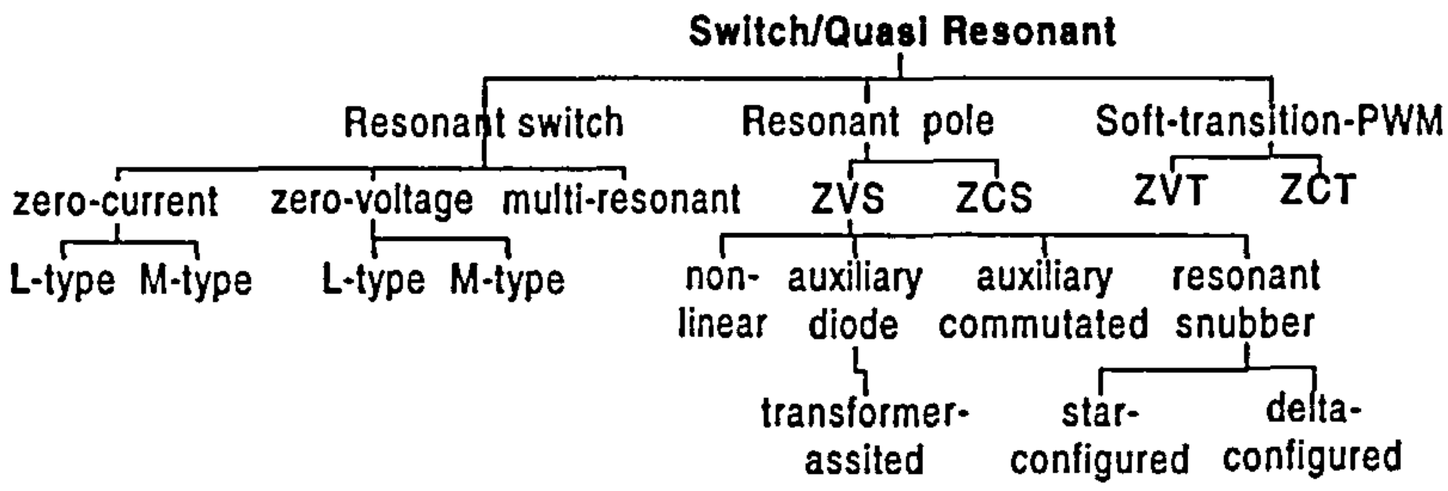

Fig. 3.29: Family of switch-resonant converters

Generally, two main techniques/circuits are adopted to achieve quasi-resonant switching[9], i.e. *resonant-switch* and *resonant-pole.* Resonant-switch is actually a subcircuit consisting of a semiconductor switch and its associated L-C components connected across the converter bridge, whereas resonant-pole consists of switches associated with the resonant components connected in the converter pole/leg. As the switch(s) is part of the resonant circuit, both subcircuits are also referred as a resonant-switch converters, or quasi-resonant converters, and resonant-pole converters respectively. These two subcircuits can be inserted in any PWM converters to obtain *resonant-transition* converters[10], which are also referred as pseudo-resonant converters [96]. Soft-switching is preferred to be combined with PWM techniques due to the advantages of obtaining low switching losses, high and constant frequency operation, reasonably rated reactive components and a wide control and load range [96].

The family tree of switch-resonant converters is shown in Fig. 3.29.

3.3.1 Resonant-switch circuits

The voltage across, or current through, the switch in the resonant-switch circuits is a sinusoidal-wave because of the L-C resonant circuit around the switch, instead of the square-wave obtained

[9] In [53], *quasi-resonant* is used interchangeably with *switch-resonant*, and it is considered as one family of soft-switching, together, with the load-resonant, link-resonant and resonant-transition families. However, in [54], *quasi-resonant* is grouped under resonant-transition families together with the load and link-resonant families

[10] [93] groups *resonant-transition* under quasi-resonant converters whereas [54] classifies them the other way round

in any typical switch-mode converter.

There are two types of resonant-switch, i.e. voltage-mode and current-mode types. Each class can be subdivided into the L-type and M-type switches. In turn, each L-type and M-type switch can be of the half-wave or full-wave variety. They are depicted in Fig. 3.30 and Fig. 3.31 [8].

Zero-current-switching/ZCS

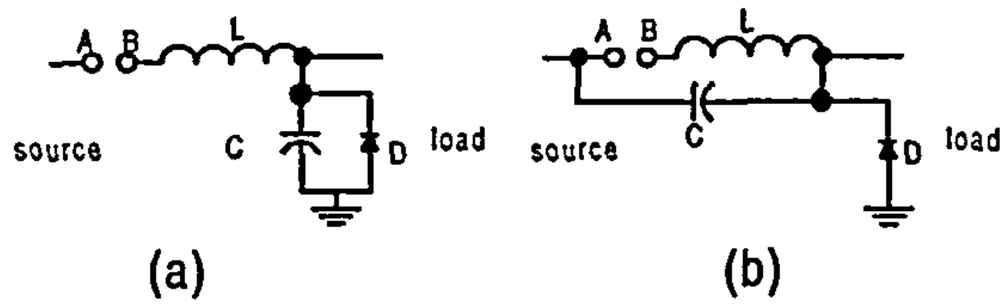

Fig. 3.30: Current-mode resonant switch :- (a) L-type resonant switch (b) M-type resonant switch, where a switch or a switch and anti-parallel diode connected across AB to form half-wave and full-wave respectively

In the L-type switch, the resonant inductor, L, is connected in series with an active switch or an active switch and a clamping diode[11] across AB to form a half-wave and full-wave variety respectively, with the resonant capacitor, C, having one end joined to the inductor, shown in Fig. 3.30. In the M-type switch, the series combination of L and AB is connected in parallel with C to form a half-wave or a full-wave M-types depending the component combination across AB. A rectifier diode, D, can be connected after the resonant inductor.

When the switch is on, the conducted resonant current increases gradually from zero in a sinusoidal-wave-like way. After half a cycle, the current reaches zero and naturally turns off, for it cannot flow in the reverse direction owing to the unidirectional-conduction ability of the switch. However, in the full-wave variety, the anti-parallel diode provides a freewheel path for the current to flow to the source at turn off. Zero-current-switching is obtained in both varieties.

A rectifier can be connected across the resonant capacitor as zero-voltage turn-on and off conditions are possible.

Zero-current resonant-switch circuits minimize the switching losses resulting from the limited di/dt at turn-off. They are insensitive to the leakage inductance of the transformer and the junction capacitance of the converter, i.e. rectifier. However, the active switch suffers from a higher rms and peak current than its switch-mode counterparts. Conduction losses are high in both the switches and resonant circuit.

[11]Diode is a type of passive switch

Zero-voltage-switching/ZVS

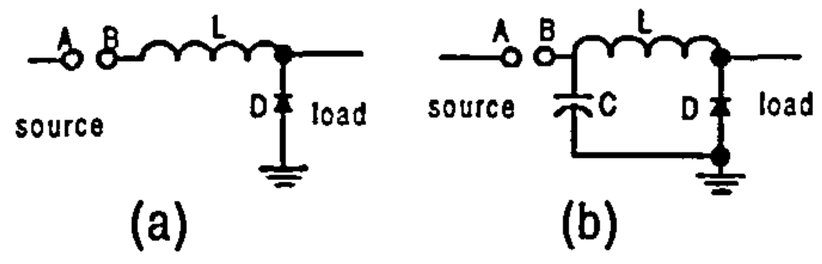

Fig. 3.31: Voltage-mode resonant switch :- (a) L-type resonant switch (b) M-type resonant switch, where a switch or a switch and anti-parallel diode are connected across AB to form full-wave and half-wave respectively

The voltage-mode resonant switches have the resonant capacitor, C, connected in parallel with the switch. The parallel combination of the switch and capacitor, maybe with a clamping diode across AB, is arranged in series with the inductor, L. Again, in the half-wave variety, the clamping diode is there to prevent the voltage across the switch from changing polarity. Consequently, the resonance ends in the mid-cycle. There is no clamping diode across the switch in the full-wave variety.

The resonant process is initiated at turn-off. The voltage across the switch and the capacitor acquires a sinusoidal-like waveform. After half a cycle, the voltage reaches zero, and the switch can be turned on again under zero-voltage conditions. The diode operates with zero-current turn-on and turn-off.

Another advantage of operating the switches in quasi-resonant voltage-mode, besides zero-voltage commutation resulting from the limited dv/dt, is absorption of the output capacitance of the switch and parasitic inductances in the resonant circuit. However, the operation is adversely affected by the parasitic capacitance of the rectifying diode, and capacitive turn-on losses. There is an extensive voltage stress across the switch too.

Multi-resonant-switching

Improved switching conditions are achieved by operating converters in either zero-current or zero-voltage quasi-resonant mode. However, it does not do anything to improve the switching conditions of passive switches, e.g. diodes. Therefore, *multi-resonant switching* is introduced. This combines both the zero-current and zero-voltage switching subcircuits as shown in Fig.3.32. Fig.3.32(a) shows that a parallel combination of a capacitor, C_1 and diode, D, is connected to one end of the inductor, which is in series with AB. To obtain L-type multi-resonant switching with full-wave current and half-wave voltage, a clamping diode is connected across the switch along AB. If there is no diode across AB, an L-type multi-resonant switch with half-wave current and full-wave voltage

is obtained. For M-type, the multi-resonant configurations can exist in two ways, depicted as Fig.3.32(b). Again with a clamping diode across the switch, M-type multi-resonant switches with full-wave current and half-wave voltage are obtained.

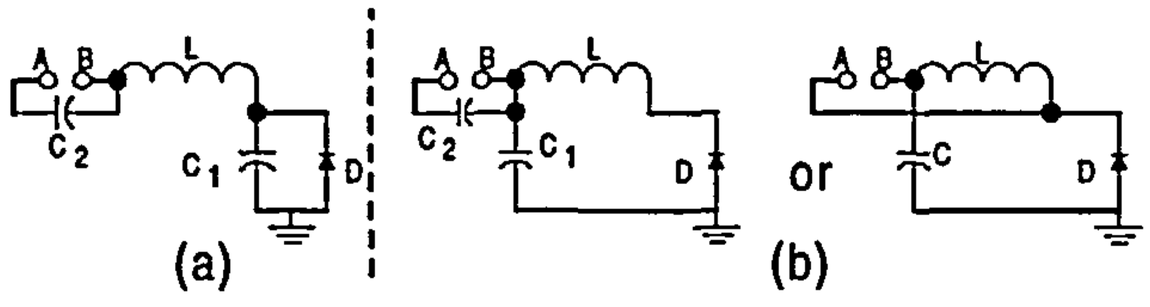

Fig. 3.32: Multi-resonant resonant switches :- (a) L-type (b) M-type

In multi-resonant-switch circuits, all the active and passive switches in the circuits are able to commutate at zero voltage. All parasitic elements are absorbed by the resonant switches. However, higher current and voltage stress are encountered compared with the traditional PWM-switch converters.

Multi-resonant topologies can be obtained by replacing the active and passive switches in PWM topologies with the multi-resonant switch.

3.3.2 Resonant-pole circuits

The resonant pole technique was originally applied on dc-dc converters [96] but it was not that successful compared with a later application on dc-ac conversion [48]. The circuit was operated in zero-voltage-switching mode.

Zero-voltage-switching

The inverter shown in [48] is redrawn here as Fig. 3.33.

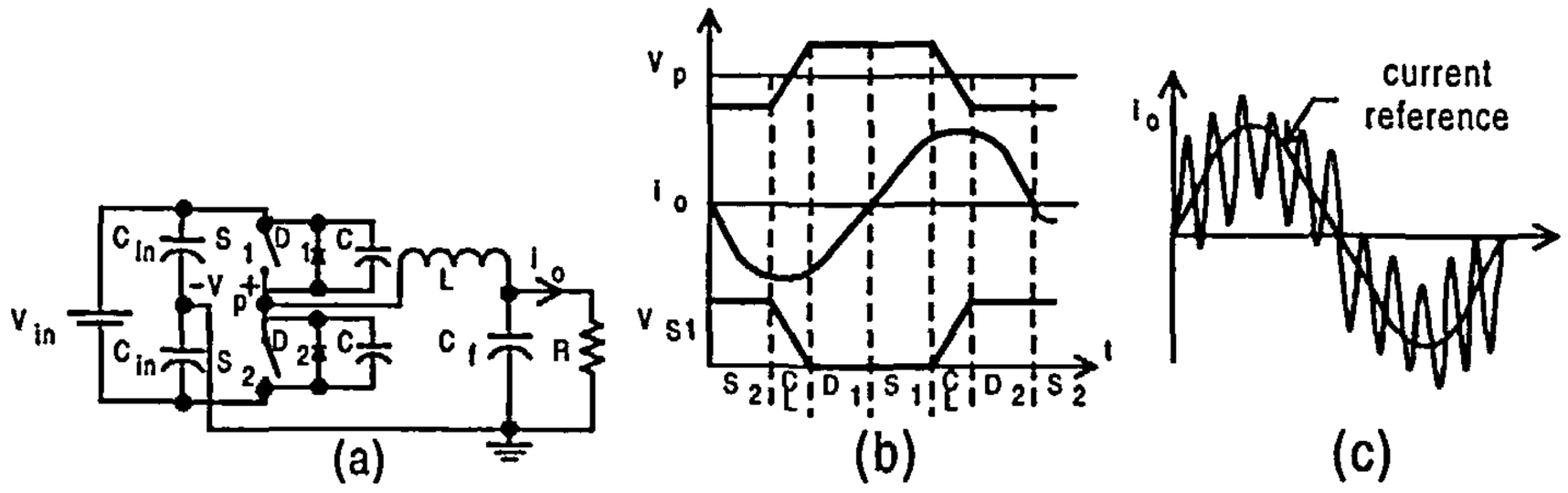

Fig. 3.33: Resonant pole inverter operating in zero-voltage-switching mode :- (a) single phase circuit (b) operation waveforms (c) the desired low-frequency output is synthesized

The resonant tank consists of a resonant inductor, L, on the load side, and one capacitor, C,

around each switch. These resonant capacitors can serve as the output capacitances of the active switches. Another capacitor, C_f, where the load is connected across it, is in series with L for noise-filtering purposes. Decoupling capacitors, C_{in}, are connected across the input link.

Pulse-width-modulation techniques are applied across AB in order to drive the inverter, which in this configuration can also be classified under resonant-transition converters. When PWM is applied across AB, the pole/leg voltage, V_p, is produced, and, for example, before $t = t_0$, S_2 is fully on and S_1 is off initially. In order to activate the converters, S_2 is turned off at zero-voltage-level. The capacitive energy is transferred from S_1 to S_2. Diode D_2 starts freewheeling any excess energy in the system, and D_1 is reverse biased. S_1 is turned on while D_1 is freewheeling the current from the previous cycle. This ensures zero-voltage turn-on of S_1. The output current changes polarity and oscillates going through the resonant inductor, both resonant capacitors and output load. The current crosses zero at the midpoint of the turn-on duration of S_1.

When V_p changes polarity, the current reaches maximum peak and then starts flowing in the opposite direction. Again, it crosses zero this time when S_2 is off. As the system configuration allows the current to flow bidirectionally, it provides sinusoidally-shaped waveforms to the load. The resonant operation only takes part during a small switching period.

One of the shortfalls of the converter is the high stress placed on the active switch as it has to sustain sufficiently large inductor current resetting the capacitive energy to create zero-voltage switching conditions, for the active switches. On the other hand, at light load, when inductor current is not that large, the zero-voltage-switching condition may be a problem. Hence, this restricts the load range capability of the system.

Note that the zero-voltage-switching resonant-pole technique is also termed *quasi-resonant current mode inverter* in [48].

Two of the above-mentioned resonant pole converters can be combined to realize a full-bridge pseudo-resonant converter [96].

There are various topologies that can be classified under zero-voltage-switching resonant-pole inverter.

Nonlinear Resonant-pole Converters This circuit is proposed to reduce the dependence of switching losses of the devices on increase of current or voltage associated with the resonant circuit. The use of inductive and capacitive snubber circuits [McMurray, 1980,Steyn, 1989] requires regenerative snubbers [Zach et al., 1986] to remove the stored energy in these elements in the ultrasonic range. This complicates the power circuit. Nonlinear resonant tanks were then used as

substitute solutions to enhance the soft-switching techniques [Ferreira and van Wyk, 1988,Erickson et al., 1989] [97].

In this topology, the continuous ramping of current is prevented using a saturable inductor. When the inductor is unsaturated, constant current flows through it due to the large inductance. However, when it saturates, the inductance falls dramatically allowing a resonant transition to occur [95].

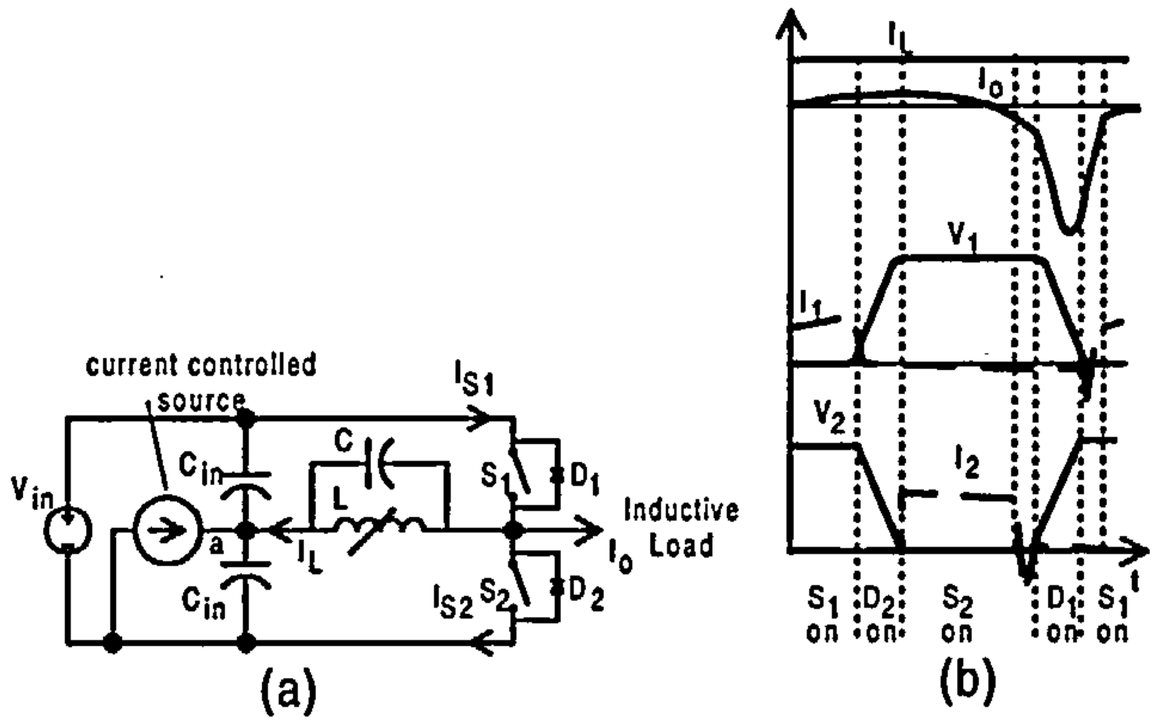

Fig. 3.34: Non-linear resonant-pole inverter:- (a) single phase circuit (b) operation waveforms

The basic circuit is shown in Fig. 3.34 [97,98]. It has a controlled-current source on the input to minimize the average control current through the nonlinear inductor, L, to avoid the rate of change of the voltage at point a proportional to the average inductor current, and hence achieving stable operation. Two smoothing capacitors, C_{in}'s, are built across the supply while two switches, S_1 and S_2, with an antiparallel diode each, are built on the output side. The output of the circuit is a PWM waveform.

The operation of the circuit is also depicted in Fig. 3.34. Switch S_1 is on, and the current flows through the switch, and charges the capacitor, C. When the charge in the capacitor builds up, S_1 is reverse biased, and causes it to soft turn-off. Voltage builds across the switch. When S_1 is on, S_2 is off.

When maximum voltage builds across S_1, and C is fully charged, the current is transferred to the freewheeling antiparallel-diode of S_2. Capacitor discharges. Inductor current builds up, and contributes to the diode current, which now consists of source and inductor current.

When the inductor saturates, the combined current of the source and the inductor changes sign resulting soft turn-on of S_2 due to the flow of current in its anti-parallel diode. After the current has built up sufficiently in the inductor, charging up C, in which the current is already in an opposite direction, S_2 is soft turned off. When the capacitor is fully charged, the freewheeling diode parallel

to S_1 takes over the current. This allows S_1 to be soft turned on anytime. The inductor current decreases rapidly. S_1 is soft turned on again.

Note that there is a dip of the inductor current around the turn-on period of S_1 and turn-off period of S_2, and the switch current is always smaller than the load current although the peak inductor current is large.

A major feature of this topology is that it achieves soft-switching without over-stressing the devices, while keeping the circuit complexity to the minimum.

Auxiliary diode-pole inverter This topology is characterized by an additional inductor current free-wheeling mode, which persists between switching transitions [95]. It is used to shape the voltage waveform for zero-voltage turn-on of the switches and to absorb all the major parasitic components by proper circuit arrangement and switching sequences [99].

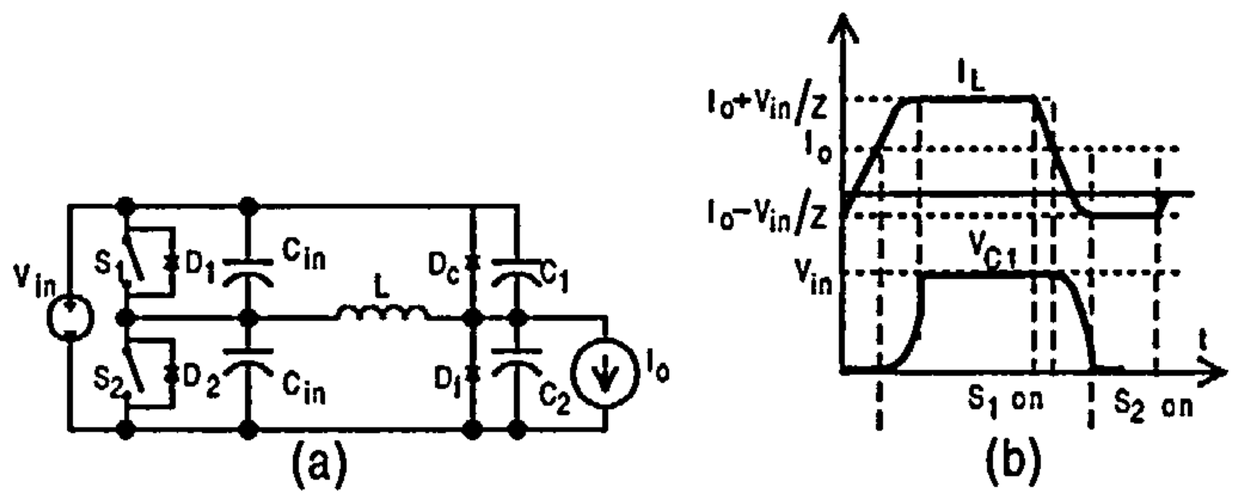

Fig. 3.35: Auxiliary diode-pole inverter:- (a) single phase circuit (b) operation waveforms

The basic circuit is drawn as Fig. 3.35 [99]. It consists of two switches, S_1 and S_2, with anti-parallel diodes, D_1 and D_2. The inductor, L, serves two functions, i.e. as an energy storage element during stationary points and as a resonant element during switching transitions. The resonant tanks comprise two resonant capacitors, C_1 and C_2 and L. A clamping diode, D_c, and a freewheel diode, D_f, are connected in parallel with the capacitors. Capacitors, C_{in}, are lossless turn-off snubbers.

The operation is also shown in the figure, where $Z = \sqrt{L/C}$, i.e. the characteristic impedance of the resonant tank. When S_1 turns-on, resonance between the resonant components ensures that voltage across C_1 equals V_{in}. Diode D_c clamps v_{C_1} at the input voltage level for a controlled duration. When S_1 is turned off, S_2 starts conducting as soon as the voltage across the device becomes zero, where the resonance of the tank starts until v_{C_2} is equal to zero. v_C is clamped at zero by D_f for another controlled duration. This is just a brief description of the operation. As a matter of fact, the operation depends on the load current whether it is positive or negative [99].

Both switches commute at zero-voltage conditions, and S_1 should only turn on if its voltage is zero, implying that S_2 sustains the input voltage and is already off. However, at turn off, switches are protected against excessive losses due to the simultaneous presence of a high current and a high voltage by the resonant capacitors from which energy is fed back to the input source. Both switch body-diodes turn off at zero current whereas the parallel diodes on the output side have low di/dt at turn-off, limited by L; and low applied dv/dt, limited by C.

Auxiliary Resonant-pole Converters Such topologies are intended to operate without the continuous inductor current freewheeling state characteristic of the auxiliary diode-pole inverter topology. The auxiliary circuit of the resonant-pole inverter is activated only during switching transitions, minimizing power loss in the resonant inductor and associated switches.

Two fractional-duty auxiliary switches and one resonant inductor are employed per phase to provide a zero-voltage turn-on condition for those main switches. The inherent natural freewheeling of the inverter can be fully utilized by operating the auxiliary switches in the resonant inductor, freewheeling only in a fractional duty. This gives an added advantage for controlling the operation of each phase individually.

The circuit is depicted as Fig. 3.36, where G_{S_1} and $G_{S_{4a}}$ are gate signals to turn on the switches [100].

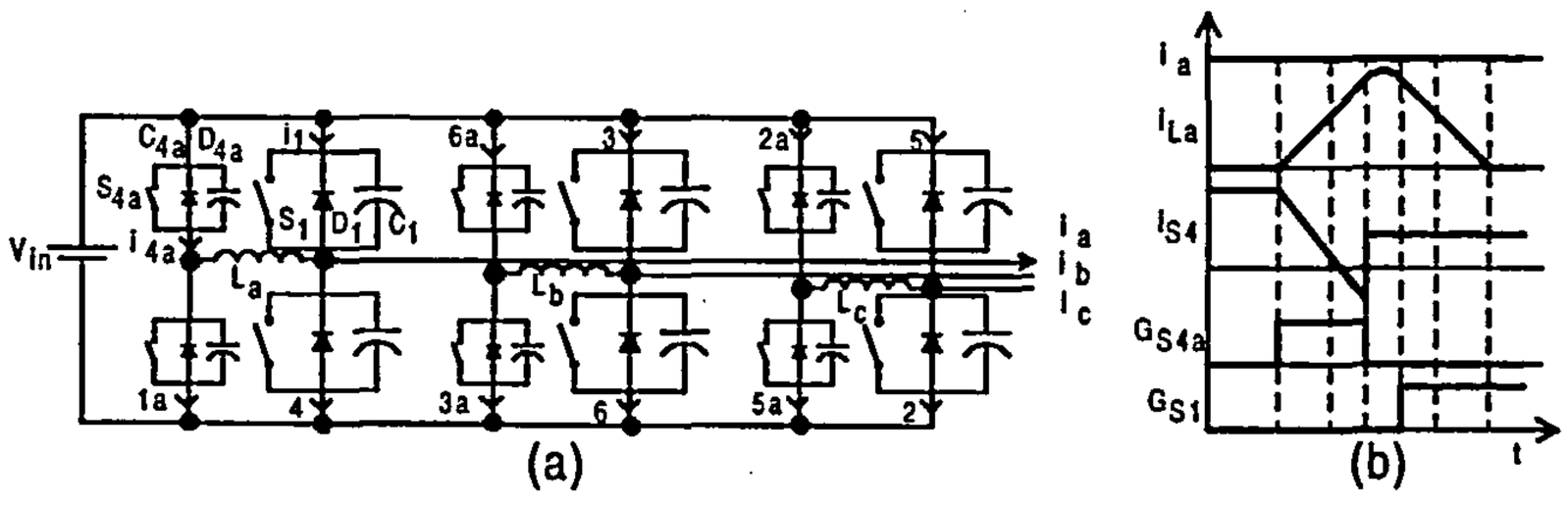

Fig. 3.36: Auxiliary resonant-pole converters:- (a) circuit (b) operation waveforms

Its operation according to [100] can be divided into four different cases of change of the switching state depending on the direction of the phase current, I_a. If $I_a > 0$, the two cases are

1. S_1 *on and* S_4 *off* to S_1 *off and* D_4 *on*

2. S_1 *off and* D_4 *on* to S_1 *on and* S_4 *off*

and if $I_a < 0$, the other two cases are

1. D_1 *on and* S_4 *off* to S_1 *off and* S_4 *on*

2. *S_1 off and S_4 on* to *D_1 on and S_4 off*

However, due to the natural freewheeling process of the circuit, the resonant snubber assisted zero-voltage-switching conditions are needed only when hard-switching is encountered, i.e. the switching state from *D_1 on and S_4 off* to *S_1 off and S_4 on*, and *S_1 off and D_4 on* to *S_1 on and S_4 off*. This is only for short duration, so-called fractional duty.

In order for the switching state to change from *S_1 off and D_4 on* to *S_1 on and S_4 off* at zero-voltage switching, the positive load current is freewheeling via D_4 while S_4 stays on and S_1 is off. S_{4_a} is turned on so that the current through D_4 starts decreasing linearly. At the mean time, inductor current rises linearly. When the resonant inductor current equals the load current, D_4 current reaches zero forcing S_4 current to rise. The resonant inductor current continues to rise, exceeding the load current level, until the stored energy is high enough to charge and discharge the snubber capacitors.

The resonant process between the resonant inductor and the resonant/snubber capacitors, C_1, C_{1_a}, C_4 and C_{4_a} causes the resonant capacitors, C_1 and C_{1_a}, to begin to discharge after S_4 and S_{4_a} turn off while C_4 and C_{4_a} are charged to the input voltage. The resonant inductor freewheeling is carried out via D_1 and D_{1_a} to reduce the inductor current. At this time, S_1 can be turned on at zero-voltage. When the resonant inductor current becomes zero finally, the load current is totally diverted to S_1. Thus S_1 is now on and S_4 is already off. This process is similar when switching changes from *D_1 on and S_4 off* to *S_1 off and S_4 on*.

Auxiliary Commutated-pole Converters In this topology, each of the primary switches is closely paralleled by a resonant or snubber capacitor to force zero-voltage turn-off switching. Auxiliary switches are placed in series with the resonant inductor, L, to ensure zero-current commutation. The circuit is drawn in Fig. 3.37 [101].

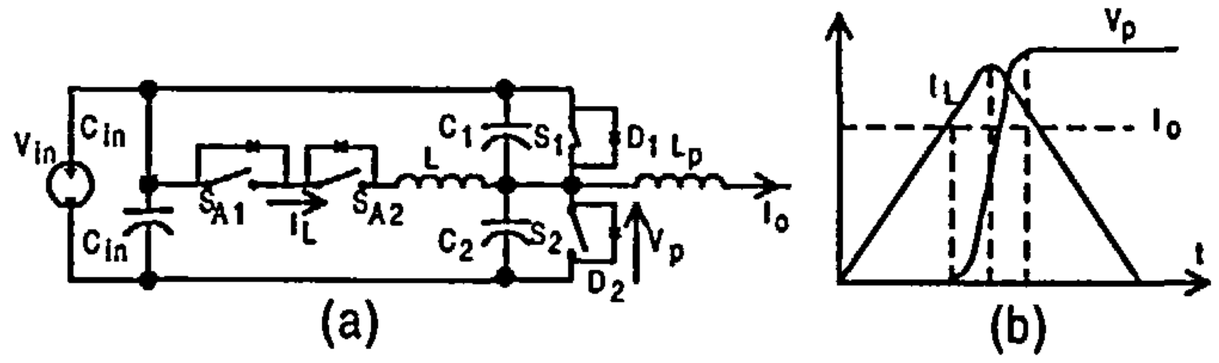

Fig. 3.37: Auxiliary resonant commutated-pole inverter:- (a) single phase circuit (b) operation waveforms

Initially, any of the main switch diodes (e.g. D_2) is turned off by triggering an auxiliary switch (e.g. S_{A_2}), allowing the inductor current, I_L to ramp up to a level determined by the load current

level and direction. Once I_L equals the load current, the resonant process starts and the pole voltage, V_p, swings to the opposite rail enabling a zero-voltage turn-on of the main switch. The resonant inductor current decays to zero and the auxiliary switch is turned off completing the current transition. Analysis on both low and high load-current commutations is given in [101] but according to [95], this topology does not rely on load current for commutation.

Resonant-snubber Inverter The basic principle of such inverters is to use an auxiliary active switching device along with lossless passive snubber components to achieve resonant switching. The parasitic inductance and stray capacitance are utilized as a part of the resonant components. There is no over-voltage or over-current penalty in the main inverter switches.

The main topologies of resonant-snubber inverters are the delta-configured [Lai et al., 1996] and star-configured [Lai et al., 1995] inverters. Delta configuration is proposed to overcome the voltage floating problem in the star configurations. Both of them do not rely on load current for commutation.

Zero-current-switching

This topology is produced by the duality transformation of the zero-voltage resonant-pole inverter in Fig. 3.33. The circuit is depicted in 3.38 [102,103]

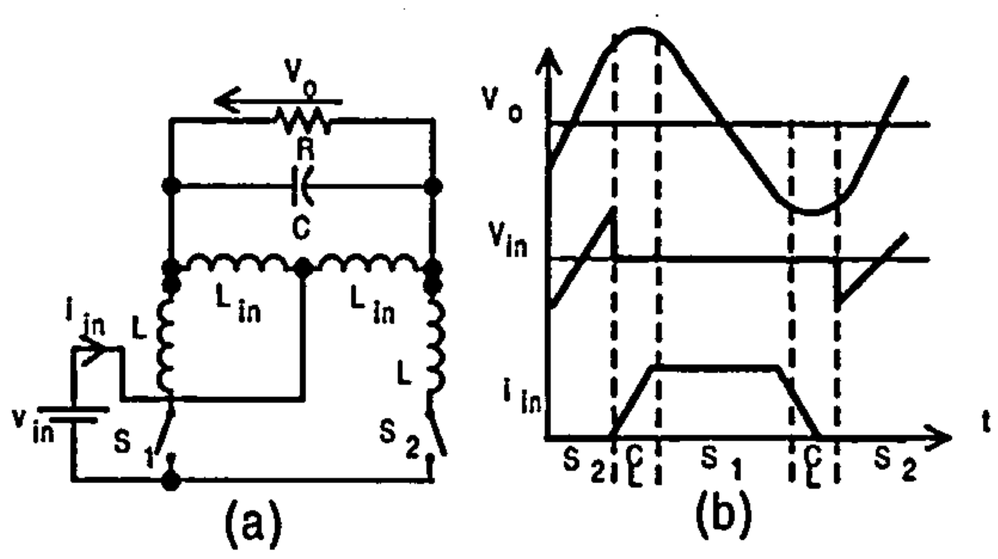

Fig. 3.38: Resonant pole inverter operating in zero-current-switching mode :- (a) single phase circuit (b) operation waveforms

Two small resonant inductors, L, are series connected to the active switches. The resonant capacitor, C, is connected in parallel with source inductors, L_{in}.

The switching sequence of the converter is such that, whenever a switch needs to be turned-off, the complementary switch should be turned-on first. The resonance between the capacitor, C, and the two resonant inductors, L, releases the inductive energy from the off-going switch to the on-coming one to ensure zero-current turn-off each time while the inductors ensure zero-current

turn-on.

When S_2 has been on, the input current flows through both input inductors, L_{in}, with one path going downwards through S_2, via one of the resonant inductors, L, while another current path flows upwards, charging up the resonant capacitor, C. When S_2 needs to be turned off, S_1 has to come on first. During the transition time, the coming on switch, i.e. S_1 diverts the current path flowing upwards, charging C, to flow downwards through the switch, S_1, via L, creating a series-resonant loop. The resonant capacitor discharges through the output load. When C is fully discharged, the current that has been flowing through S_2 is now flowing upwards charging the capacitor in the opposite direction, creating zero-turn-off condition for S_2 to be turned off. Thus, the series resonance between the output of the capacitor, C, and the two resonant inductors, L, releases the inductive energy from the off-going switch to the on-coming one to ensure zero-current turn-off each time, while the inductors ensure zero-current turn-on. The cycle repeats.

3.3.3 Resonant-transition Converters

Resonant-transition converters are formed by employing soft-switching techniques in PWM converters. The inverter bridge operates in pulse-width-modulation mode with a fixed dc-link voltage. An auxiliary circuit is inserted in the system to achieve resonant switching during the transition period only. Its operation has to be synchronized with the PWM control scheme to activate either a zero-voltage or a zero-current transition mechanism.

Zero-voltage-transition/ZVT

A zero-voltage transition dc-ac converter is shown in Fig. 3.39 [104]. There is a switch, S and a

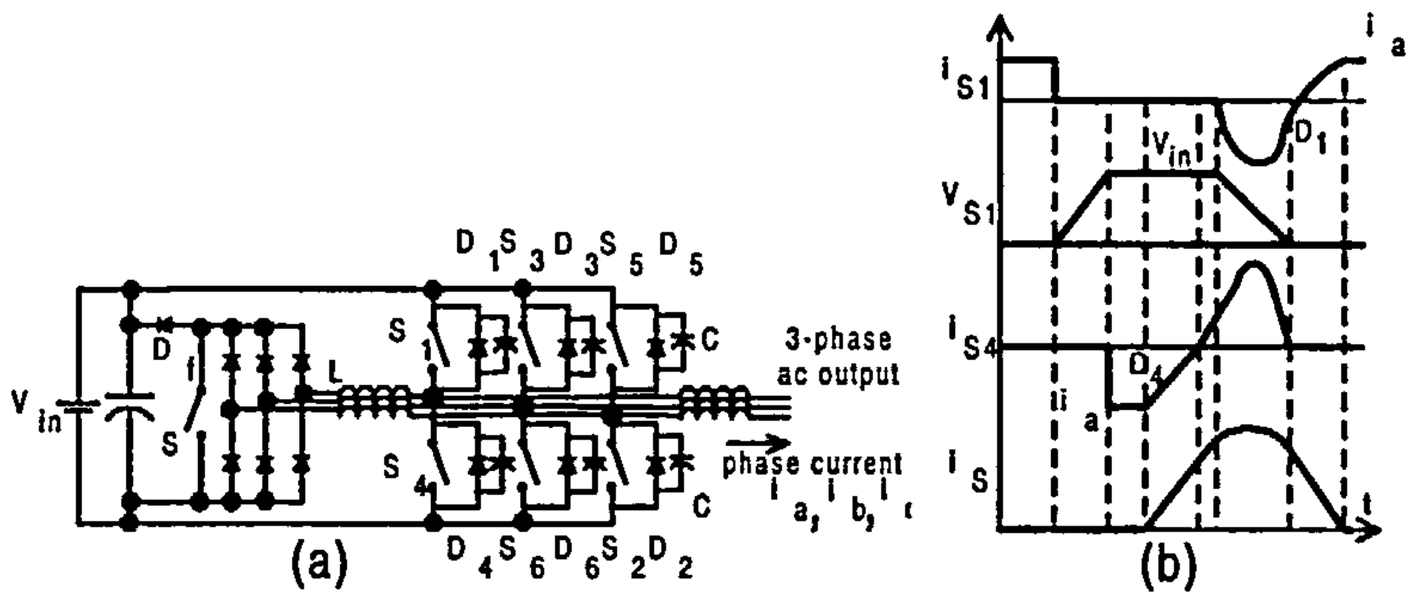

Fig. 3.39: Zero-voltage transition dc-ac converter :- (a) single phase circuit (b) operation waveforms

small-power-level diode, D, in the auxiliary circuit. The switch, S, activates the ZVT commutation of the main switches, and the diode, D, feeds extra inductive energy back to the dc input side. All

the switches commute at zero-voltage conditions while all the diodes turn on and off at zero-current conditions. Six inverter switches with each having a shunted resonant capacitor and body diode are placed after the auxiliary circuit.

Its operation is basically similar to the conventional PWM counterpart, except during the switching transient periods when soft-switching is applied. Assuming S_1, S_2 and S_6 are conducting initially, and current in phase a, i.e. i_a, flows outwards to the load whereas i_b and i_c flow in the inbound direction. Due to the inductive nature of the load, the currents flowing through the switches are constant. The ZVT-PWM operation of S_1, S_2 and S_6 starts with turning off all the active switches at zero-voltage conditions. The goal is to commutate the currents i_b and i_c from diodes D_1 and D_2 to switches S_3 and S_5 while achieving zero-voltage-switching for the active and passive switches.

When the auxiliary switch, S, is closed, the current going through the auxiliary inductors, L, starts to increase from zero, diverting the currents from D_1, D_1, D_6 and D_2 to the commutation circuit gradually. After the current of the auxiliary inductors exceeds the respective phase input current, the main bridge diodes block, and their currents are commutated to their respective body switches.

After there is enough stored energy across the inductors L, the three closed switches are now opened, starting the resonant transition phase. The stored energy in the inductors is used to charge the shunt capacitors, C, in resonant conditions, and hence provides zero-voltage turn-on for S_3, S_4 and S_6.

Turn-on of S_3, S_4 and S_6 reverses the input voltage of the commutation circuit. The inductor's stored energy is returned to the dc-input side. When the auxiliary current reaches zero, the auxiliary switch, S turns off, and the residual energy from L is transferred across the auxiliary circuit near the dc-input side. Switch S_4 is turned off and switch S_1 is turned on at zero-voltage.

Note that the soft-commutation from S_3 and S_5 to S_6 and S_2 respectively takes place naturally without assistance of the commutation circuit. When switches S_3 and/or S_5 turn off, the phase parasitic capacitances are discharged by the respective phase current, providing the switches zero-voltage turn-on.

It is important that the load is inductive to resonate with the resonant capacitors creating zero-voltage switching. The advantage of this topology is that PWM switching occurs at zero-voltage-transition switching. However, as more switching sequences are needed in the ZVT topology compared with its conventional counterparts, implementation of correct switching timing is more

complicated [Mao and Lee, 1994]. Note that ZVT is not available for all switching combinations, for example, when S_1, S_3 and S_5 are all turned on.

As the name implies, the switches of the inverter bridge commute at zero-voltage switching while the diodes are subjected to zero-current switching. When the auxiliary circuit is activated, both the dc bus and the load see a parallel-resonant network.

Zero-current-transition/ZCT

A ZCT-PWM topology shown in Fig. 3.40 comprises a conventional PWM converter and a six-switch auxiliary circuit with series resonant inductors, L, and capacitors, C [54]. Each switch of

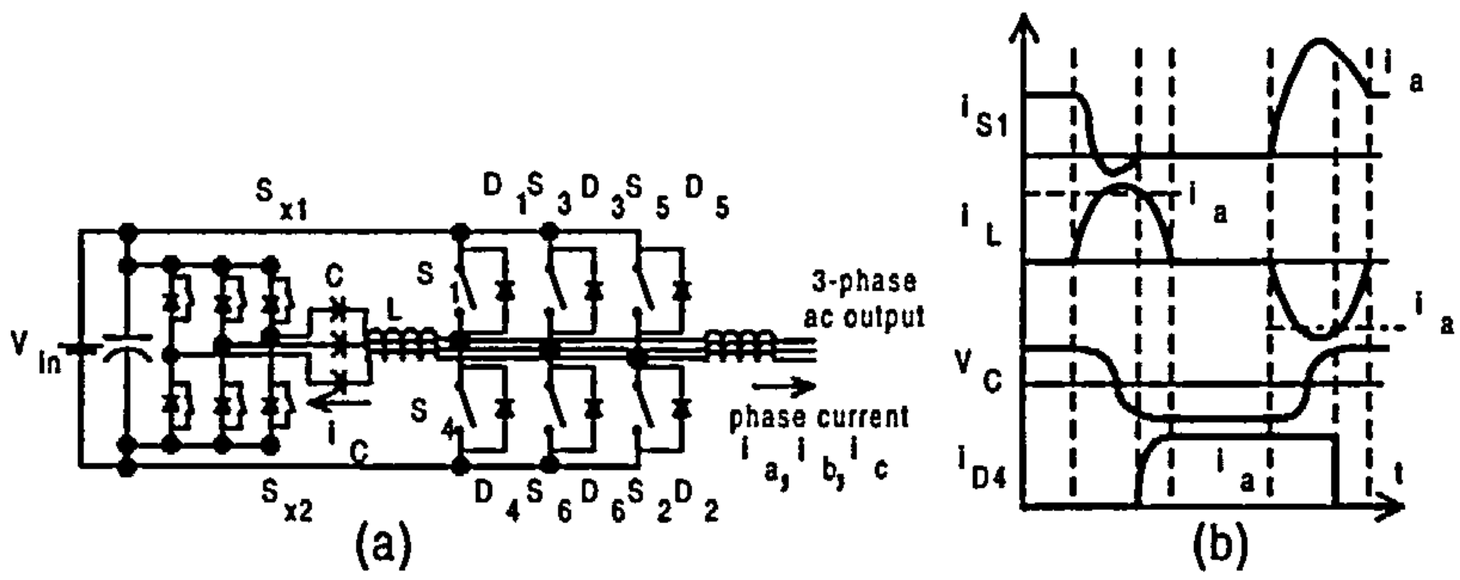

Fig. 3.40: Zero-current transition dc-ac converter :- (a) single phase circuit (b) operation waveforms

the auxiliary circuit provides ZCT operation of the active switch on the corresponding phase leg. Initially, S_1, S_4 and S_6 are on and the resonant capacitors, C, are precharged. Currents going through the switches are constant due to large load inductances. Zero-current-transition operation is initiated by turning on the auxiliary switches which turns off S_1, S_4 and S_6, hence causing series resonance to occur between L and C. This forces current going through L to rise. Phase current, i_a is diverted into the auxiliary circuit.

The active switches, S_1, S_4 and S_6, are turned off at zero-current switching, and their body diodes circulate the remaining inductor current.

The advantage of the topology is the low voltage and current stresses on both the active and passive switches. According to [Mao and Lee, 1994], the energy circulating in the auxiliary circuit can be adjusted to minimize the power dissipation and conduction losses in the auxiliary circuit. However, the diodes of the inverter bridge and the auxiliary switches are hard-switching turned-off at load-current level which turn-off loss can be a serious problem.

Unlike the ZVT-PWM converter, when the auxiliary circuit of the ZCT-PWM is activated, both the dc bus and the load see a series-resonant network. However, duality transformation does

not apply to either circuit to obtain another one.

In short, the quest for resonant converters capable of operating in PWM mode will still continue, as PWM-only operated converters suffer from output signal harmonic content and audible noise and hence excessive switching losses at high switching frequency, besides the shorting of input voltage source whenever a switch is turned on while the adjacent antiparallel switch diode is conducting. Resonant-only operated converters suffer from high stresses on the switching devices, discrete power-flow, requirements of complex control techniques and huge resonant tanks. Thus, it is hoped to combine the advantages of both types of converters by inventing soft-switching converters operating in PWM mode.

3.4 Link-resonant Family

If the link-switching could be ensured to achieve zero-level commutation, the link frequency would then be restricted only by device turn-on, storage and turn-off times. An elegant method to attain zero-switching losses by holding the link voltage, or current, at zero-level for the duration of the switching transient, is to make the link or bus oscillatory [Divan, 1989]. This allows additional devices, i.e. resonant components, connected across the link in between the input source and the PWM inverter, to be also operated at zero-switching crossing if they were commutated at zero-level switching.

There are two types of link-resonant converters, namely dc- and ac-link resonant converters. In the ac link, the link waveforms contain both positive and negative half-cycle voltage or current, to facilitate the use of bidirectional switches, while the dc link comprises a unipolar waveform due to the dc offset in the link-current or voltage oscillation. Thus, only unidirectional switches are used.

Both link-resonant converters can be further subdivided as series and parallel types. In the series-link, the resonant L and C components are connected serially in the path of power flow, to give current pulses at the output, while in the parallel-link, the passive components are connected across the path of power flow, to output-voltage pulses. Zero-level commutation is obtained with the soft-switching techniques employed in both configurations.

The family tree of link-resonant converters is shown in Fig. 3.41.

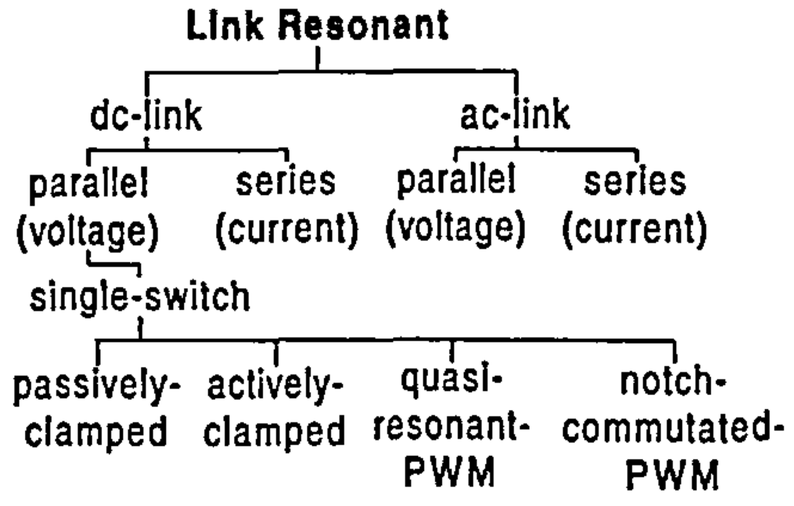

Fig. 3.41: Family of link-resonant converters

3.4.1 dc-link Resonant-converters

Parallel dc-link/dc-voltage link

The parallel dc link circuit shown in Fig. 3.42 [51] consists of a parallel combination of resonant capacitor, C, and inductor, L, with a dc bias capacitor, C_b in series with the resonant inductor. The simplified model is shown next to the complete circuit. The switch in the simplified model represents the operations of two switches from the input rectifier and another two from the output inverter. The output/load current is assumed constant during one frequency cycle due to the internal load inductance. The oscillating link-waveform is obtained by pulsating the input inverter/dc link voltage, v_l, with the L-C components to create zero-voltage switching conditions. That is why it is also called a resonant dc-voltage link.

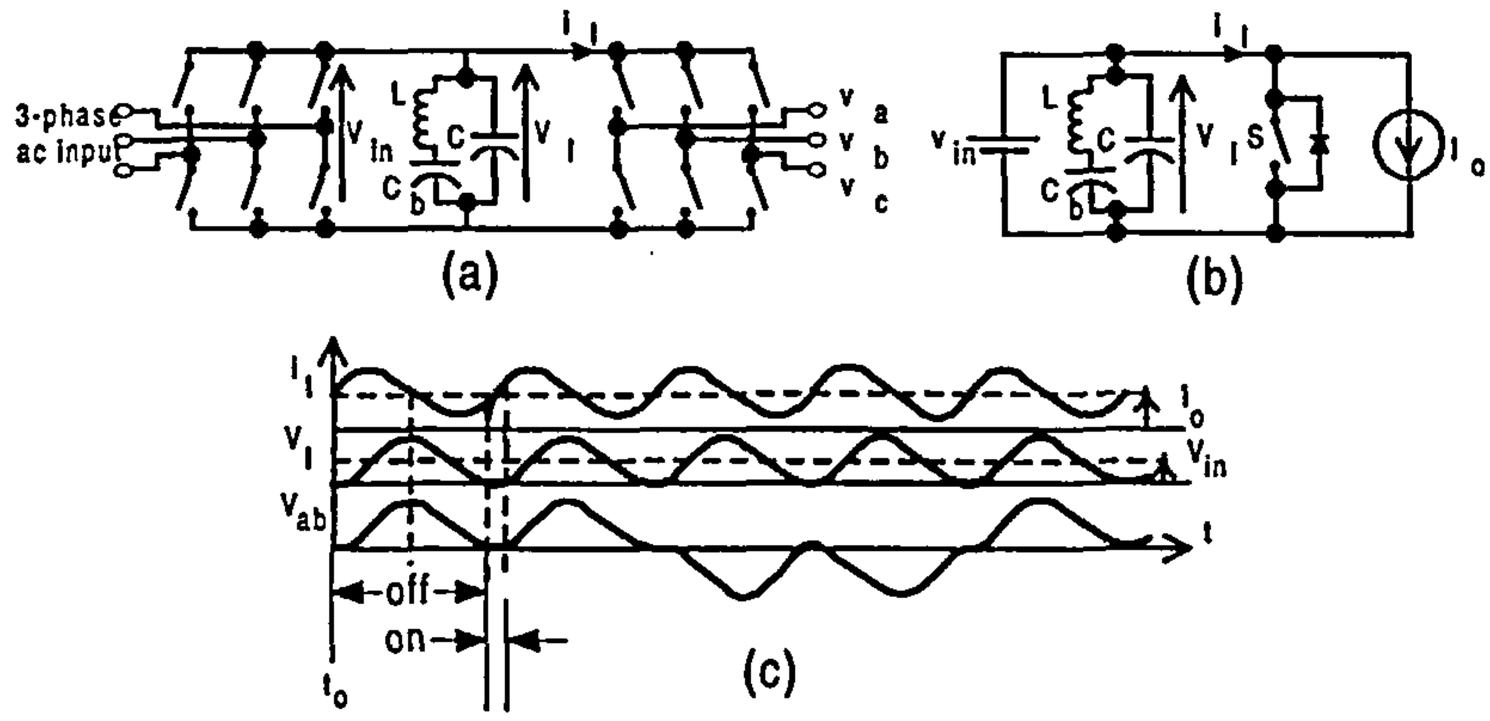

Fig. 3.42: Parallel resonant dc-link converter:- (a) circuit (b) simplified model (c) operation waveforms

From the operation waveforms, it is shown that when the switch is on, current flows through the switch-diode combination in the simplified model. The link current, i_l, builds sinusoidally, and sufficient energy is stored in L before the switched is opened. When the switch is opened at zero-level switching of the link voltage, v_l, at $t = t_0$, v_l starts building up across the switch, reaching

peak value when i_l crosses the I_o value, and going back to zero. It remains zero for the turn-on period of the switch across the link. It is seen that i_l returns to the I_o value, and v_l returns to zero for the next cycle. In any practical situation, there is resistance present along the link in the system. Thus, in order to obtain zero-voltage switching, current flowing through the diode-switch combination has to be controlled properly, to attain the objective, by controlling the switch on-time interval. For, if the on-time is too long, high-voltage stress may build up across the switch.

Voltage regulation can be achieved on the output using parallel-link capacitor-load dc-dc converter, where the resonant inductor is in series with the load of the inverter [105,106].

There are problems associated with the link topology; zero-crossing failures and overshoots in the link voltage, v_l, may occur due to the unstable initial circuit-conditions during each resonant cycle, which is affected by load variation. Thus, in order to solve the problems, the link-resonant network has been modified to reduce the clamping factor and hence the switch stresses, and to introduce the pulse-width-modulation capability. Pulse-width-modulation is believed to have better resolution of harmonic component distribution compared to the discrete-pulse-modulation control modes. Consequently, a *single-switch resonant-link* topology is proposed, and is discussed later as a separate subsection.

Similar to the quasi-resonant and load-resonant converters, the parallel dc-link inverters can have *L-LC* or *LC-C* configurations. The *L-LC*-type is said to have lower voltage-gain than the *LC-C* configuration, which allows a lower turn-ratio transformer to be used on the *L-LC*-type [Batarseh and Lee, 1991].

A current-controlled parallel-resonant dual-converter is described in [Korondi et al., 1994], and a dc-link converter, utilizing a parallel-resonant circuit to separate the conventional voltage link from the three-phase PWM inverter for switching instants, is presented in [He et al., 1990].

Series dc-link/dc-current link Series dc-link converters are the dual of the parallel dc-link resonant converters shown in Fig. 3.42 [107,108]. The series one is shown in Fig. 3.43 together with the simplified model and operation waveforms [54,108]. It is also referred to as a resonant dc-current link as it commutates at zero-current switching. The *L-C* components are connected in series with the power flow to create a zero-current-current-switching feature in the link current, i_l. A large bias-inductor, L_b, provides the dc bias current of the system. V_{in}, shown in the simplified model, is the output voltage of the input rectifier in the three-phase figure but is the input voltage to the resonant tank. The thyristor, *thy*, represents the operation of two devices from the input rectifier and two from the output inverter. The resonant-inductor current, I_L and the resonant-capacitor

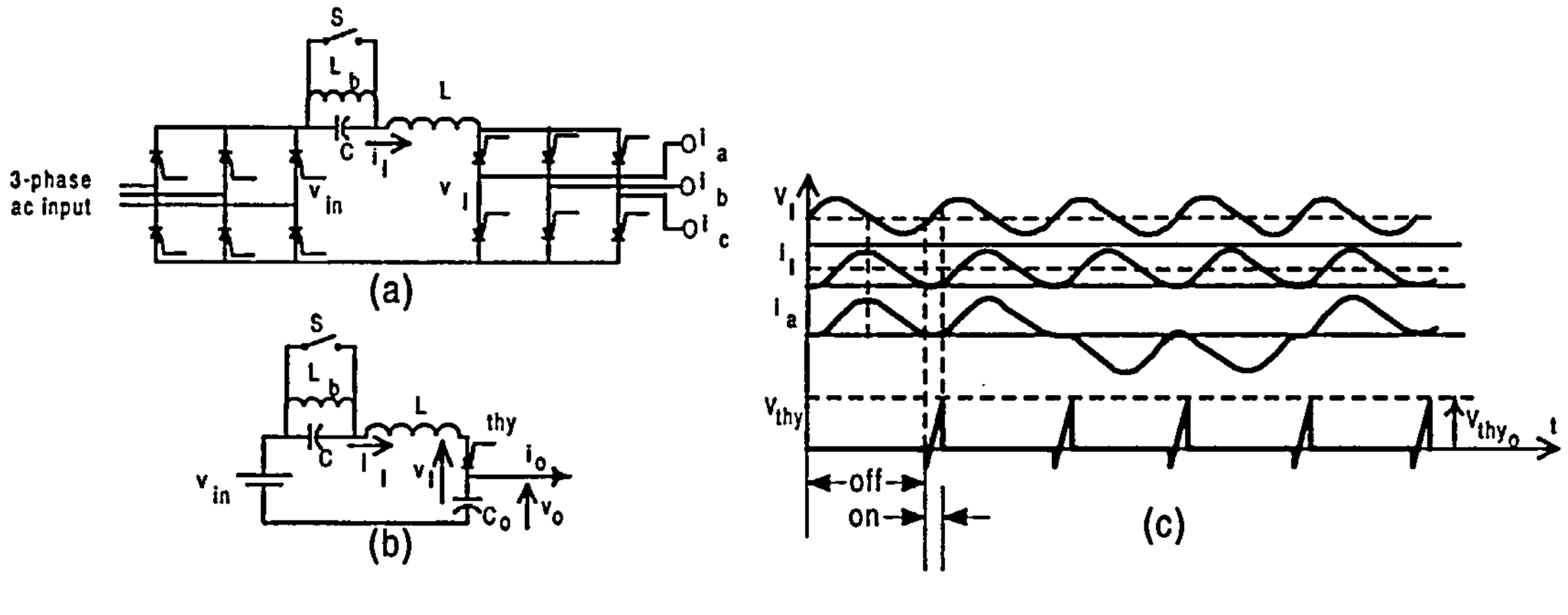

Fig. 3.43: Series resonant dc-link converter:- (a) circuit (b) simplified model (c) operation waveforms

voltage, V_C, are assumed constant, during the resonant period, as the resonant components, L and C are both very large.

When *thy* is triggered, the link current, i_l is initiated to resonate forming a current pulse shown in Fig. 3.43. At turn-off, the thyristor voltage-rise reaches the preset-threshold value, V_{thy_o}, to turn on the switch again. During the turn-off period, the remaining current flowing in the inductor, L, charges up the resonant capacitor, C, and hence the thyristor voltage, v_{thy}, increases linearly. The next current-pulse train is generated when the threshold value is reached. This pulse train is fed into the output-filter capacitor, C_o, keeping the voltage, V_{C_o}, constant. This voltage is fed to the load, V_o.

If the link current flowing through the inductor, i_l, is too big, zero-crossing will be lost. The input voltage, V_{in}, can be controlled in such a way that the extra energy will be removed from the link, thus reducing the link current, i_l [107]; or an extra switch, S, is added to regulate the current pulse level by clipping it before it exceeds the maximum value [109]. The switch can also be used to recirculate the current from the capacitor which could be overcharged [107]. However, the control techniques in both [107,109] are quite complex. A saturable inductor can also be used as the resonant inductor, L to clamp to the current [110,111]. By inserting an inductor at each three-phase inverter output-line, it was shown that the original current pulse was divided into smaller optimal-pulses simultaneously to obtain smoother current flow at the output [108,112]. The modified topology of Fig. 3.43 was again proposed in [113] to employ true PWM control on the inverters.

3.4.2 ac-link Resonant-converter

High-frequency ac-link power converters are viewed as alternatives for conventional dc-link power-conversion systems [Sood and Lipo, 1988]. In the ac-link systems the input to the single-phase or three-phase inverters is a high-frequency sinusoidal ac. A converter is powered with a high-frequency sinusoidal input source, and the output is synthesized to be a low-frequency ac. Bidirectional switches used in the system are turned on and off at zero-crossing. The switches are controlled in a switching sequence such that selected half-cycle and/or full-cycle pulses of the high-frequency link are transferred to the output.

The output pulse can either be positive half-cycles or negative half-cycles or even a combination of both. This allows a low-frequency output to be synthesized to the desired frequency and magnitude, as shown in Fig. 3.44 [7,54]. The number of pulses at the output is determined by the link frequency, the amplitude of the fundamental output component, and the desired-output frequency. This is the basic mode of control called *discrete-pulse modulation*, where only selected half-cycle and/or full-cycle pulses of the high-frequency link are transferred to the output, as shown in Fig. 3.44. It has been applied in cycloconverters for ac drives [114].

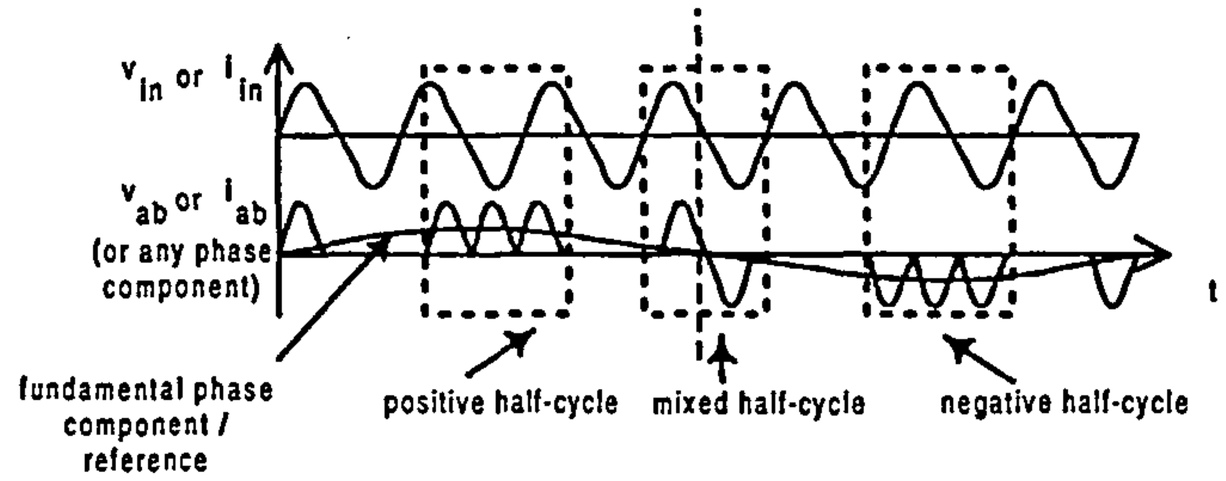

Fig. 3.44: Synthesis of low-frequency ac output in ac-link resonant converters

The waveforms show that the ac-link converters have natural zero-crossings twice in each switching cycle. The switches on the inverter bridge are only activated at those zero-crossing instants.

This concept can be extended to deliver three-phase ac output by either the parallel or series ac-link resonant converters shown in Fig. 3.45 and Fig. 3.46 respectively [54]. If the input and output converters are the same, power transfer can be done easily on either side with unity power-factor and low harmonic and acoustic noise [Sul and Lipo, 1990a].

Parallel ac-link/ac voltage-link

In parallel ac-link resonant-converters, the resonant tank is connected between the current-source dc-link and the inverter-bridge. The reactive components, L and C are connected in parallel to

provide an ac-link voltage to the inverter bridge. The switches of the inverter bridge are turned-on and off only at those zero-voltage instants to reduce switching losses.

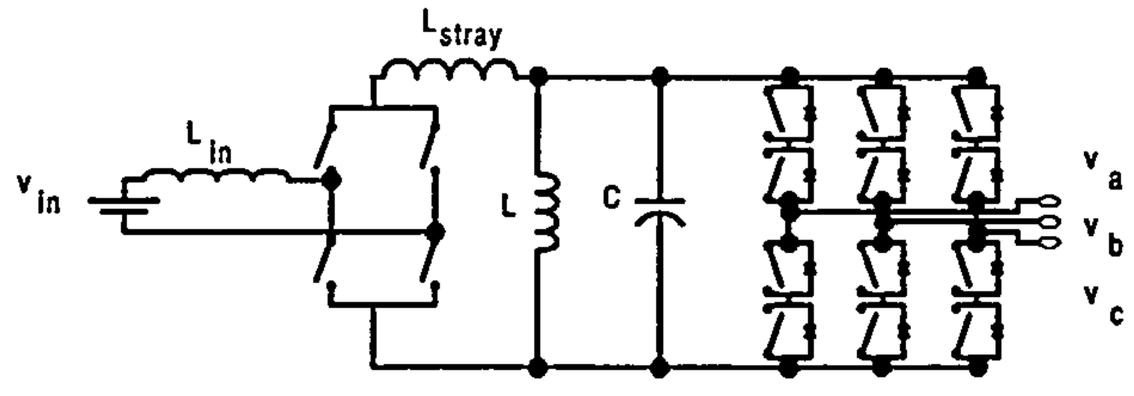

Fig. 3.45: Parallel ac-link resonant converters

The link energy has to be kept as constant as possible to avoid imbalance in the input and output current. If this is not so, the resonant circuit will either be over-excited, i.e. the link voltage exceeds the acceptable level, or under-excited, i.e. the link voltage will collapse.

An additional bidirectional switch can be inserted in series with the resonant tank to improve the coupling of the resonant circuit to the switch matrix during the switching process [18].

Series ac-link/ac-current link

In series ac-link resonant converters, the resonant tank is connected in series on the ac link producing ac link current to the inverter. The link current is either controlled through the rectified input source voltage, V_{in}, or through battery dc-source with a current-controlled stage reported in [115]. A high-link frequency can be obtained by using small resonant-component values.

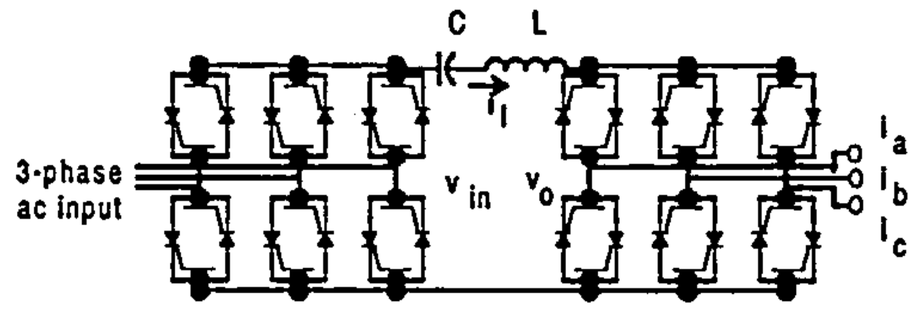

Fig. 3.46: Series ac-link resonant converters

Both circuits are tuned to resonate at the input-source frequency. Thus, the converters do not draw any current from the high-frequency ac input. However, the resonant capacitor, C, provides a low-impedance path to all other frequency components in the input current for parallel configuration, and the input voltage for series configuration. Thus, the converters are not supplied by input voltage(parallel) or input current(series) through the stray inductance L_{stray}.

Generally speaking, compared with ac-link ones, dc-link inverters have the advantages of lesser component counts and ease of decoupling the source from the load. However, dc-link inverters

have to sustain twice the voltage and/or current stress on the switches of the ac-link. This can be overcome by using a modified converter proposed in [Woo et al., 1990]. With the dc arrangement also, besides the balance of the link energy, the charge balance on the bias elements, e.g. capacitors in parallel configurations with inductors, in the series dc-link inverters, have to be also taken care of. Change in output voltage would cause irregular current-peaks to occur in the parallel dc-link converters, or voltage-peaks, in the series dc-link converters. As the resonant tank of the parallel dc-link is not in the main power transfer path, the resonant components can have lower-voltage and lower-current ratings, and hence they introduce less energy loss into the main system. The sensitivity of the parallel configurations is low for parasitics and reverse-recovery phenomena. However, self-commutating devices have to be employed sometimes to ensure zero-level switching. The series configurations are superior in those aspects. As a series-link appears as a high-frequency current source to the load, it is used with small and slow impedance-variation loads [106].

In the case of the ac-link, the energy storage components are smaller compared with its dc counterparts for cost reasons. Average power balance between the load and source has to be done actively. The instantaneous power unbalance is then handled by a tank circuit at the cost of the link-voltage variation, where a moderate-voltage variation is acceptable by building a converter having fast regulation, and ensuring the link voltage is big enough to synthesize the desired reference voltage. Whereas for the current, pulse-density-modulation [Sood and Lipo, 1988], delta-modulation [Kheraluwala and Divan, 1987] or mode-selection control [Sul and Lipo, 1990b] techniques can be used.

Single-switch link-resonant Converters

These types of converters are classified differently by different authors, for example, they are classified as series dc-link in [51] but parallel dc-link in [54]. Due to this unhelpful classification, they are presented separately here, even though, strictly speaking, they should be classified under parallel dc-link resonant converters as voltage pulses are produced at the output, and the resonant elements are not in the main-power-transfer path. The basic topology is shown in Fig. 3.47 [54]. The circuit

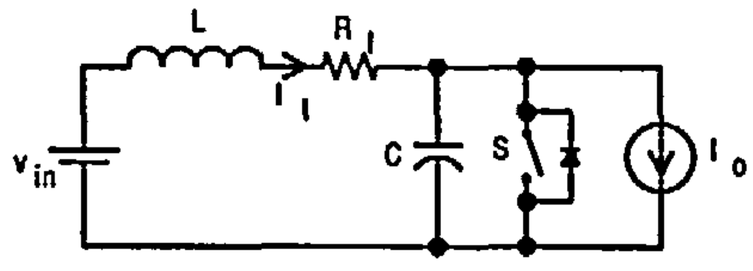

Fig. 3.47: Single-switch link-resonant converter

contains a resonant inductor, L, and a resonant capacitor, C. The capacitor is in parallel with an auxiliary switch shunted by a diode. Constant current, I_o, flows in the output. R_l is the parasitic resistance that is present in the dc-link. The operation waveform is similar to Fig. 3.42.

The variations of the circuit are described as below.

Passively-clamped dc link The link peak voltage is clamped passively, i.e. using an auxiliary circuit comprising a coupled inductor and a diode, in this topology, when the load current decreases suddenly. Energy is extracted from the L-C resonant tank to create the clamping level and is fed back to the input dc source. In order to maintain zero-voltage switching, the clamped circuits have to be operated at twice the input voltage.

The circuit proposed by [116] is depicted in Fig. 3.48.

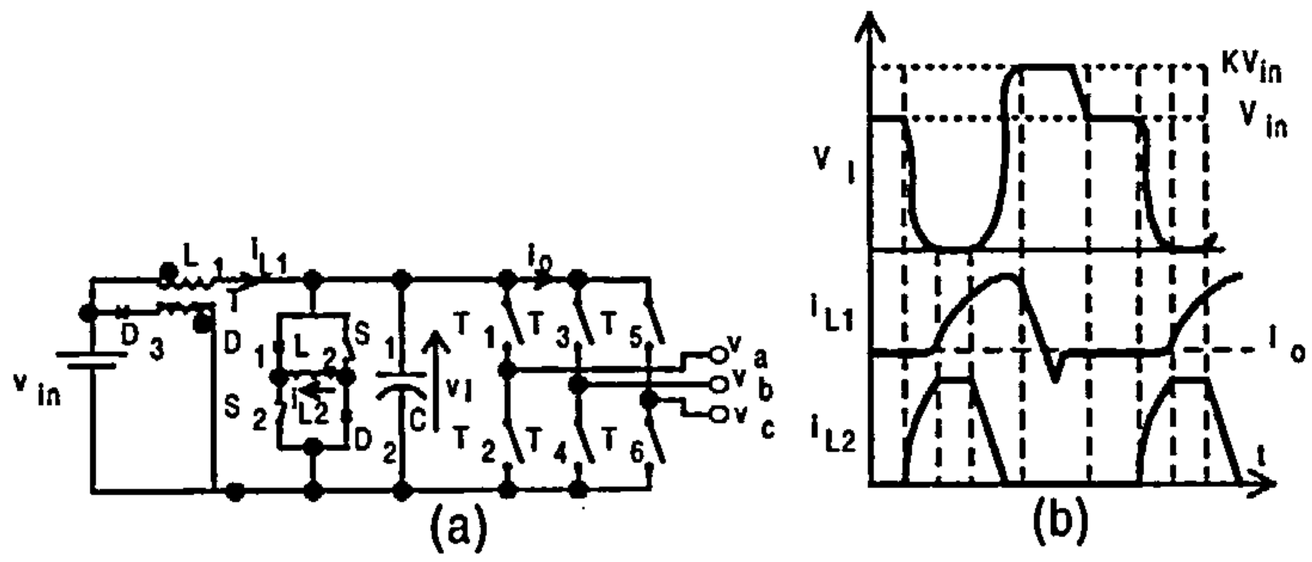

Fig. 3.48: Passively-clamped dc-link resonant inverter :- (a) circuit (b) dc-link voltage and line-to-line output-voltage waveforms

It consists of a resonant capacitor, C and a resonant inductor, L_1. An auxiliary switch is in parallel with the capacitor. A transformer-coupled passive clamped circuit, T is on the input side of the system. The purpose of the T is to contain the peak voltage stress during the resonant cycle under transient conditions, when instantaneous power flows back to the dc supply. Compared with the traditional passively-clamped resonant dc-link circuit, this one has an additional circuit containing a small switched inductor, L_2, two auxiliary switches, S_1 and S_2, driven by the same gating signals, and two diodes, D_1 and D_2. As the switches are parts of the resonant circuit, it is more accurate to refer to it as a passively-clamped quasi-resonant dc-link inverter. PWM switching is used to operate the system.

The operation waveforms are also given in Fig. 3.48. Initially, the link voltage, V_l, is clamped at a voltage between V_{in} and $k \times V_{in}$ with both switches, S_1 and S_2, off disabling the resonance process. The auxiliary inductor, L_2, is reset to zero, and current going through L_1 is equal to the dc link current, I_o. When both the switches are turned on at zero-current-switching, to initiate a

resonant transition, the link voltage, V_l, is applied to inductor L_2 to give rise to its current. The link voltage starts to drop. This process triggers the resonance between L_1, L_2 and C. Energy is transferred from C to L_2, and hence drives V_l towards zero.

When V_l equals zero, the anti-parallel diodes, D_1 and D_2, clamp the link voltage at zero when S_1 and S_2 remain closed. Current in L_2 remains while current in L_1 increases linearly to store sufficient energy for link-voltage ramp-up when the switches are turned off at zero-voltage-switching. Current in L_2 is fed back to V_{in}, and the resonant process drives the link voltage towards twice its value, i.e. $2 \times V_{in}$. The voltage is clamped at $k \times V_{in}$, which is lower than $2 \times V_{in}$. When the link voltage hits the clamped voltage, a voltage equal to V_{in} is produced across the secondary of the transformer, T to forward bias D_3. This allows excessive energy to be fed back to the dc voltage source, V_{in}. The clamp action is relieved after the feeding-back action, and the current in L_1 continues to supply the load current, I_o before the cycle starts.

It is claimed that the circuit removes the high voltage stress on the passive devices, and PWM operation and resonance control become easily fulfilled. In addition, closed-loop regulation of link-energy balance is not required for sustaining the resonance. High current capability can be achieved without the expense of ac current ratings of the resonant components due to its parameter-independent, rather than load-independent, resonant energy.

Other passive-clamping methods were also presented in [116]. A modelling tool using space-vector approach was used to investigate the modulation nonlinearity of the proposed dc-link circuit [117].

Actively-clamped dc link In this topology, an auxiliary switch, S_c, for clamping purposes, and an electrolytic stored-voltage clamp capacitor, C_c are inserted in the conventional parallel-resonant dc-link as shown in Fig. 3.49 [48,54,118]. An antiparallel diode, D_c, should be used with the clamping switch to ensure zero-voltage switching if a device without a body diode is used.

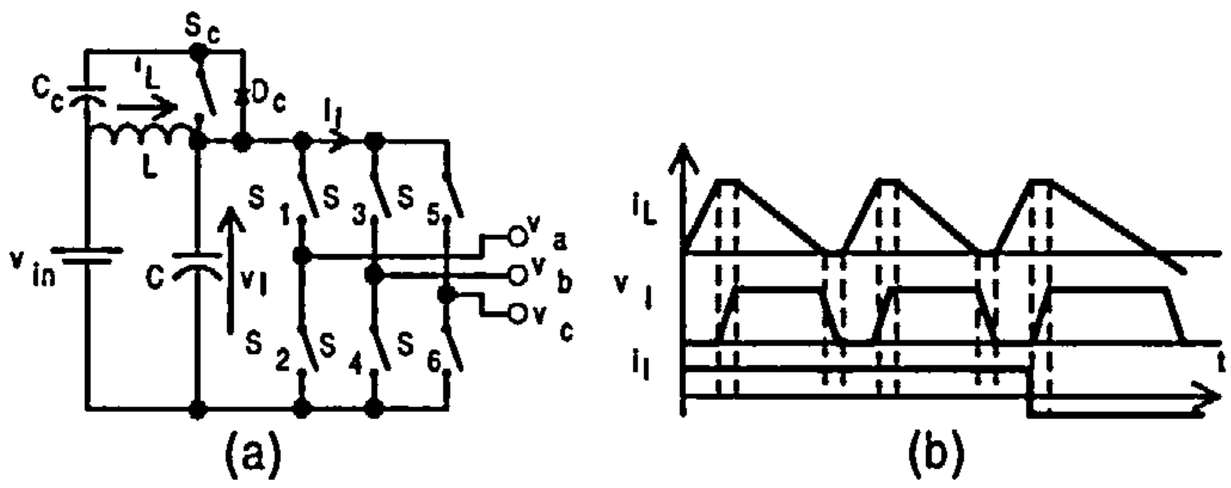

Fig. 3.49: Actively-clamped dc-link resonant inverter :- (a) circuit (b) dc-link voltage and line-to-line output-voltage waveforms

As in the typical dc-link resonant converters, an oscillating dc voltage is generated on the link, and is clamped to a level of the input voltage, V_{in}, with the clamping factor, k, yielding kV_{in}. The principal waveforms are shown in Fig. 3.49.

When any corresponding pair of the switches are turned-on to short-circuit the resonant capacitor, C, giving zero link-voltage, the resonant-inductor current ramps up linearly until the switches are turned-off. The inductor current remains constant before decreasing linearly. During the period when the current is constant, the link voltage resonates up to kV_{in}. On reaching this voltage level, the clamping diode, D_c, comes into conduction to clamp the voltage. The clamping switch, S_c, is then turned on in a lossless manner to reduce the inductor current. The current eventually transfers from the clamping diode to the clamping switch. During the conduction of S_c, the charge transferred to the clamping capacitor and clamping diode is recovered. When the clamping switch is turned off at zero-inductor current, or at the required level with no charge being transferred to the capacitor, the clamped is released. This causes the link voltage to decrease to zero level. At this instant, the body diodes of the switches turn on to allow current in the diodes to flow before the switches come into conduction. The switches are then turned-on while current has been flowing in the body diodes to achieve zero-voltage switching across switches. The next cycle commences, and so on.

Compared with the passively-clamped dc-link, a better clamping level can be achieved in the actively-clamped topology, and there is no net-gain or loss of stored charge. However, in practice, the device storage times are not very predictable, and consequently, additional ac circuitry is needed to handle the charge balance [48]. In addition, this circuit is restrained by the discrete-pulse-modulation operation and pre-charging problem of the voltage-clamping capacitor.

However, all these single-switch resonant topologies either have a limited power range or a large device count, or subharmonic problems resulting from discrete-pulse-modulation. In addition, complex modulation techniques and the impossibility of utilizing true PWM techniques on the above topologies further encouraged the following to be proposed.

Quasi-resonant PWM dc link A low-loss quasi-resonant dc link inverter is proposed in [119], and is redrawn in Fig. 3.50.

It consists of three switches, S_1, S_2 and S_3, with an antiparallel diode each, adding to the conventional six inverter switches, and resonant inductor, L, resonant capacitor, C. Two very large input capacitors, C_{in}, are inserted to hold and to return the inductor energy to reverse the resonant inductor current. All the inverter switches are replaced by a single switch, S, with the antiparallel

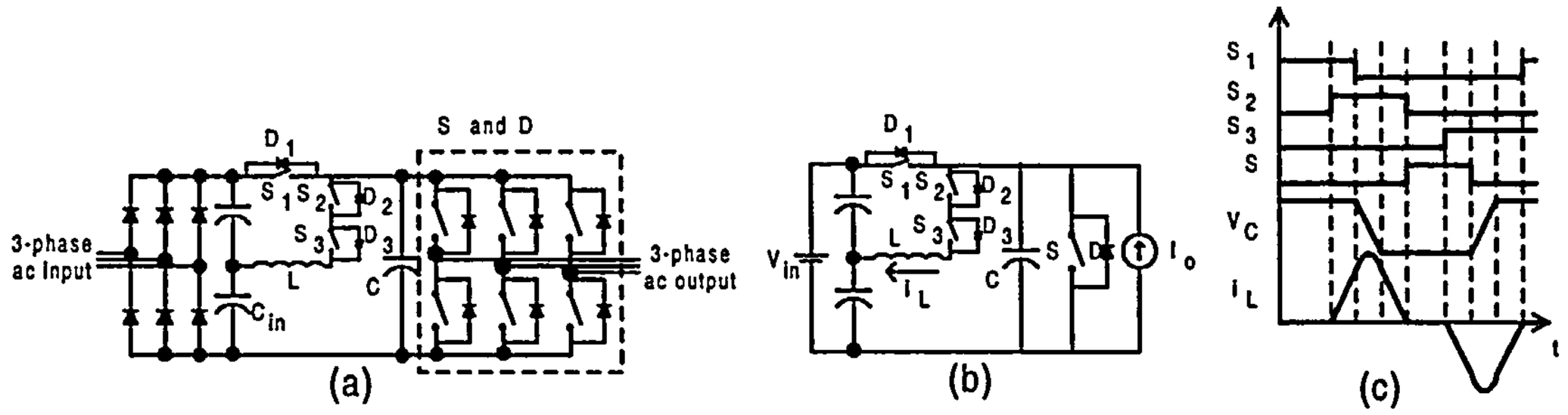

Fig. 3.50: Quasi-resonant PWM dc-link resonant inverter :- (a) circuit (b) simplified model (c) operation waveforms

diode, D, in the simplified model.

Initially, load current, I_o, flows through switch S_1 before S_2 is turned on. The resonant capacitor, C, is fully charged. S_2 is turned on at the zero-current condition to force current to go through L, and increase linearly. S_1 remains on when S_2 is turned on. Turning off S_1 at zero-voltage initiates the resonance between the resonant tank. This causes the capacitor C to discharge to zero via S_2 and D_3. While the capacitor voltage stays at zero, the inductor current falls linearly. The energy which used to be stored in L is now transferred to the bottom input capacitor and freewheel through the inverter switch diode, D. Inverter switch, S, is turned on when zero current flows through L. At the same time, S_2 is turned off. S_3 can be turned on during the on-period of S. As current has been flowing in both D and D_3, S and S_3 can be turned on at the zero-voltage condition. Turning on S_3, energy reserved in the input capacitor C_2 is released, and the direction of the inductor current is reversed, and increases in a negative sense. D_2 is forward-biased. When S is turned off, the current will charge up the parallel resonant capacitor to restart the resonance between L and C. The capacitor voltage increases to the level of the input dc source, V_{in}. When the capacitor is fully charged, the inductor current flows through D_1 and eventually becomes zero. During this period, S_1 can be turned on anytime with zero-voltage condition.

This technique manages to reduce the levels of subharmonics but at the expense of increasing losses, including conduction losses due to increasing number of devices; and device stresses by operating the inverter with PWM switching, which itself is also limited by the energy constraints associated by maintaining the link oscillations; and by the need to conserve charge in the clamp capacitor.

A synchronous PWM dc-link resonant inverter raising the possibility of true PWM operation is presented in [Malesani and Divan, 1989]. However according to [Venkataramanan and Divan, 1992], the control technique presented in [Malesani and Divan, 1989] is rather limited. This causes

another approach combining a conventional dc-link inverter with a three-phase soft-switched PWM input stage to be used in [Venkataramanan and Divan, 1993].

In addition, load-range capability and operating frequency are also limited [Venkataramanan and Divan, 1992].

Notch-commutated PWM dc-link This is essentially a proposal to overcome the problems faced by the Quasi-resonant PWM dc-link by [120] in order to improve the PWM capability and to reduce switch stresses.

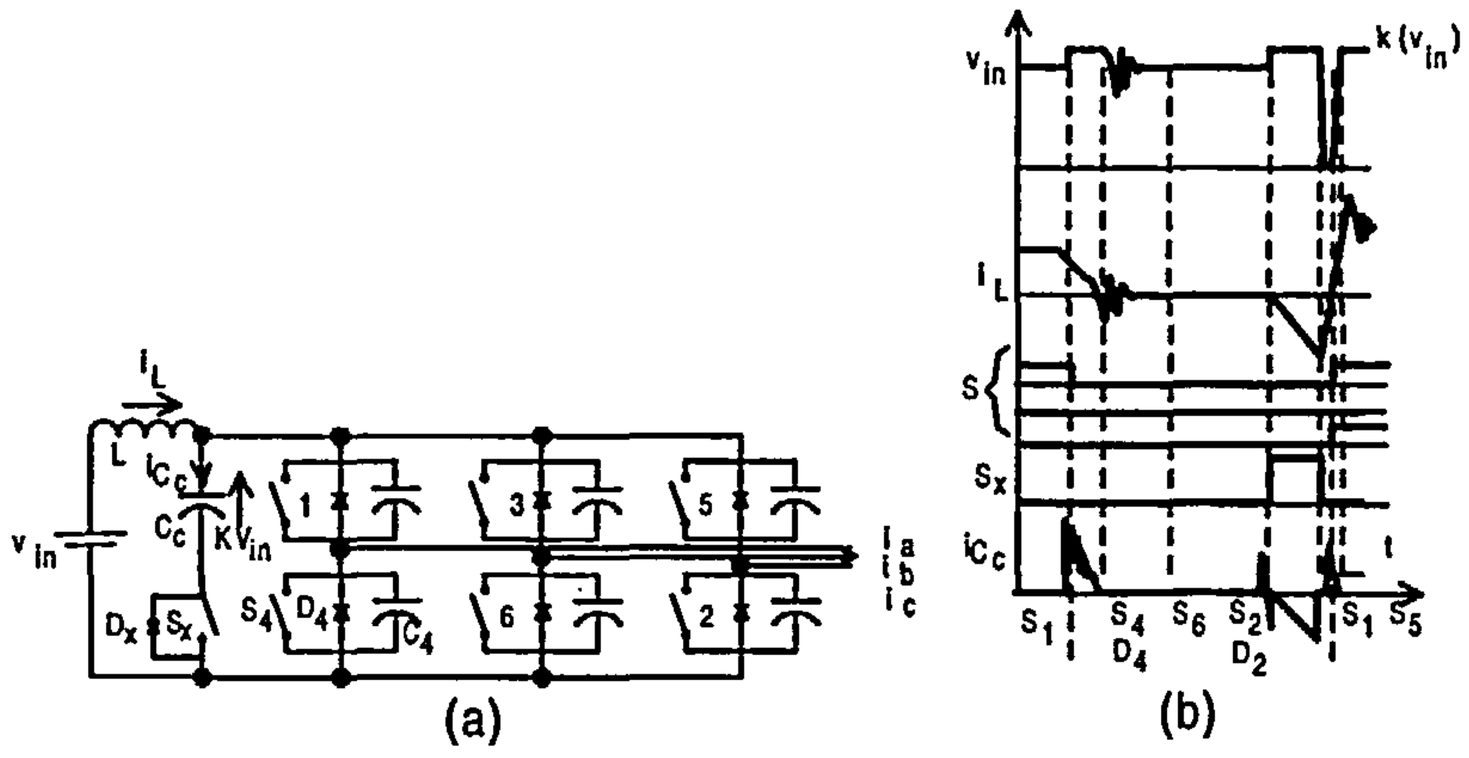

Fig. 3.51: Notch-commutated PWM dc-link resonant inverter :- (a) circuit (b) dc-link voltage

Similar to the quasi-resonant PWM dc-link proposed in [Chen and Lipo, 1995], the dc-link voltage is constant, and the inverter bridge is operating as a conventional PWM type. 'Notches'/short zero-voltage intervals are provided by activating the auxiliary bus commutating network to create soft-switching conditions.

Initially, gating signals are applied to S_1, S_2 and S_6, and the line currents, I_a and I_c, flow downwards but I_b flows upwards. This causes S_1, S_6 and D_2 to conduct. When S_1 is turned off, Fig. 3.51, at zero-voltage condition, as the switch capacitor, C_1, is already discharged, while D_2 and S_6 are still on, the current flowing through the dc-link snubber inductor, L, decreases towards zero. C_4 is discharged to the load and then the anti-parallel diode, D_4 conducts providing soft-switching condition. Energy in L is transferred to the voltage clamp capacitor, C_c, through the forward-biased diode, D_x. The respective top or bottom switch capacitors are charged up to the value of, $K \times V_{in}$.

When all the stored energy in L has been transferred into C_c, diode D_x becomes reverse-biased, and the switch capacitors are discharged from the previous value, KV_{in}, to the dc supply voltage, V_{in}. The dc-link current settles to zero. When the auxiliary switch, S_x, is turned on, energy is

transferred from C_c back to the source via L.

The current flowing through L, i.e. i_L, reverses polarity, and decreases linearly towards a negative value due to the overvoltage of C_c due to a higher voltage across C_c than the dc-link voltage. The on-time of S_x is maintained to achieve a clamp voltage that is slightly higher than the input voltage, V_{in}. After i_L has reversed polarity, S_x is turned off. The negative current flowing through L discharges all the switch capacitors and forces all the anti-parallel diodes to conduct. This provides a zero-volt *notch* across the dc-link, allowing zero-losses turn-on of S_1 and S_6. Zero turn-off is also obtainable due to the *notch*.

The dc bus current rises from its negative value to zero value while zero-volts *notch* is introduced during this short period. The inductor current, i_L, continues to rise reaching the dc-link inverter input current. The dc-link voltage would rise above KV_{in} but it is clamped by C_c which is achieved through D_x, forward-biased by the exceeded voltage. All the extra energy stored in L is transferred to C_c. The current through L finally equals the load current before the next cycle.

The oscillations appearing on the operation waveforms are due to the high-frequency resonance process occurs between L and all the capacitances on the bus.

Besides the above-mentioned single-switch topologies, there is a *fully-controlled boost current converter* presented in [Lai and Bose, 1988]. Additional switches are used compared with Fig. 3.47 to give full control of the inductor current and output voltage. However, the advantages are achieved at the expense of greater circuit and control complexity, besides increasing the system losses due to the hard-switching of the additional switches.

3.5 Conclusion

Resonant converters are classed into three main groups, which are load-resonant, switch-resonant and link-resonant converters. With brief discussion, selected circuits and operation waveforms are presented based on published literatures. The information presented above, although collected from a variety of published sources, represents the first detailed review of resonant-type converters, and as such, will form the basis of a proposed review article.

Chapter 4

Frequency Domain Analysis of Load-resonant Converters using the Impedance Concept

4.1 Introduction

Chapters 2 and 3 discussed the basic semiconductors used in such converters and reviewed most of the topologies of resonant converters. Existing designs of the converters, involving complicated analysis of the dynamic and steady-state stages, are not as straight forward as they might appear. Further, their output powers are controlled in such a way as to operate the converters above resonance conditions on the basis that turn-off loss can be virtually reduced to zero by an extra capacitor placed across the switch, while the turn-on loss is zero naturally. However, that is not a particularly good solution to the problem as the current through the resonant tank does not go through zero simultaneously with the transition of the voltage across the tank. This is clearly indicated in Fig. 2.14. Therefore, none of the existing control methods of resonant converters allows for a wide range of switching frequencies without incurring switching losses, leading to lower operating frequencies than are achievable with the sort of techniques described in Section 1.2 in this thesis.

A new method of power control that exploits the particular frequency characteristics of the series-parallel load-resonant converter has been developed by colleagues. This delivers a wider range of output power levels, while maintaining zero-current switching, maximum efficiency and minimum output-current ripple. This chapter reviews such an approach. This approach to converter

analysis has been done in the frequency-domain. Limitations of this work were discovered by the author at a later stage, and will be discussed later in this chapter. However, before the review is given, it is good to revisit the existing control methods and design analyses, with particular reference to the inverters depicted in Fig. 4.1 and Fig. 4.3

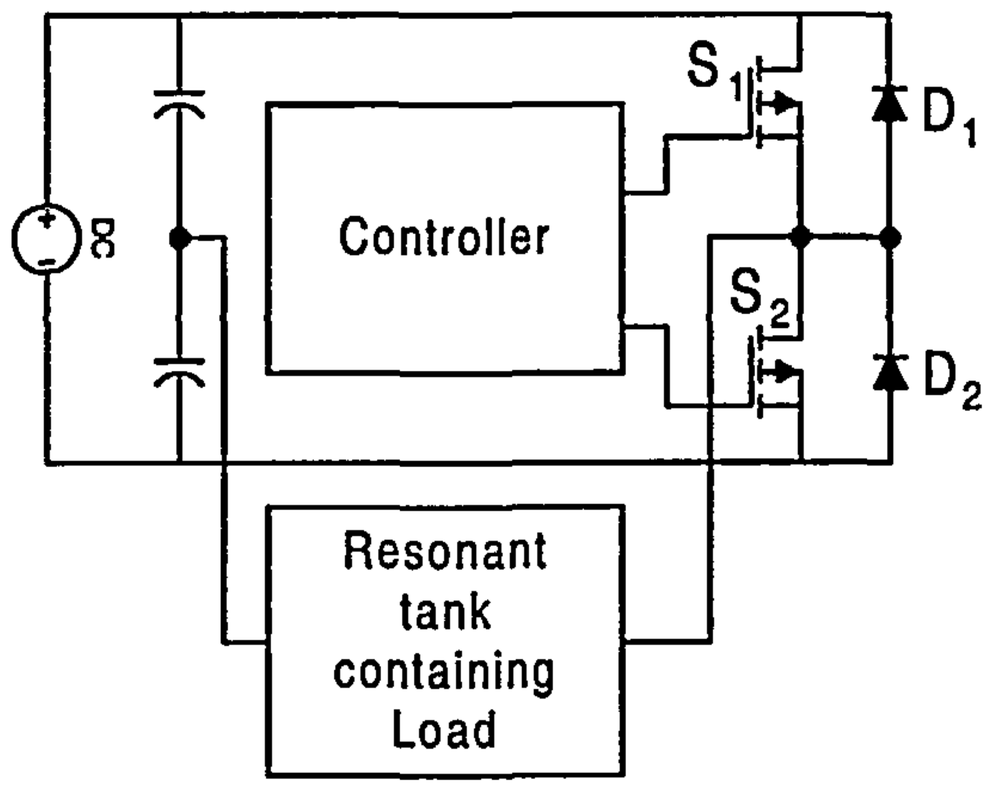

Fig. 4.1: Half-bridge inverter for power control illustration

4.2 Existing Methods of Power Control

The ultimate aim of the power control of resonant converters is to acquire desirable power conditioning while maintaining zero, or near-zero, switching losses. There are three commonly used methods of achieving power control of the converters, namely *variable-frequency control*, *fixed-frequency control* and *dead-time control* [3,11,121].

4.2.1 Variable-frequency Control

One of the popular strategies to obtain variable-frequency control is by operating the converter away from resonance [122]. Adapting a figure from reference [3], and is re-depicted in Fig. 4.2 to show the operation of variable-frequency control.

In this operation, the current is not in phase with the voltage, and only when the voltage and current are 90° out of phase, can the average power be eventually reduced to zero. Thus, there is non-zero-current switching, and a fairly limited range of high operating frequencies. Although the output power is reduced, the conduction loss in the circuit remains high as there is a large reactive current flowing in the circuit. Lossless snubbers, connected directly across the switches, have been proposed to give zero-voltage turn-off when the converter is operated above resonance, meaning the voltage leads the current [123]. However, the snubber capacitors may cause substantial problems

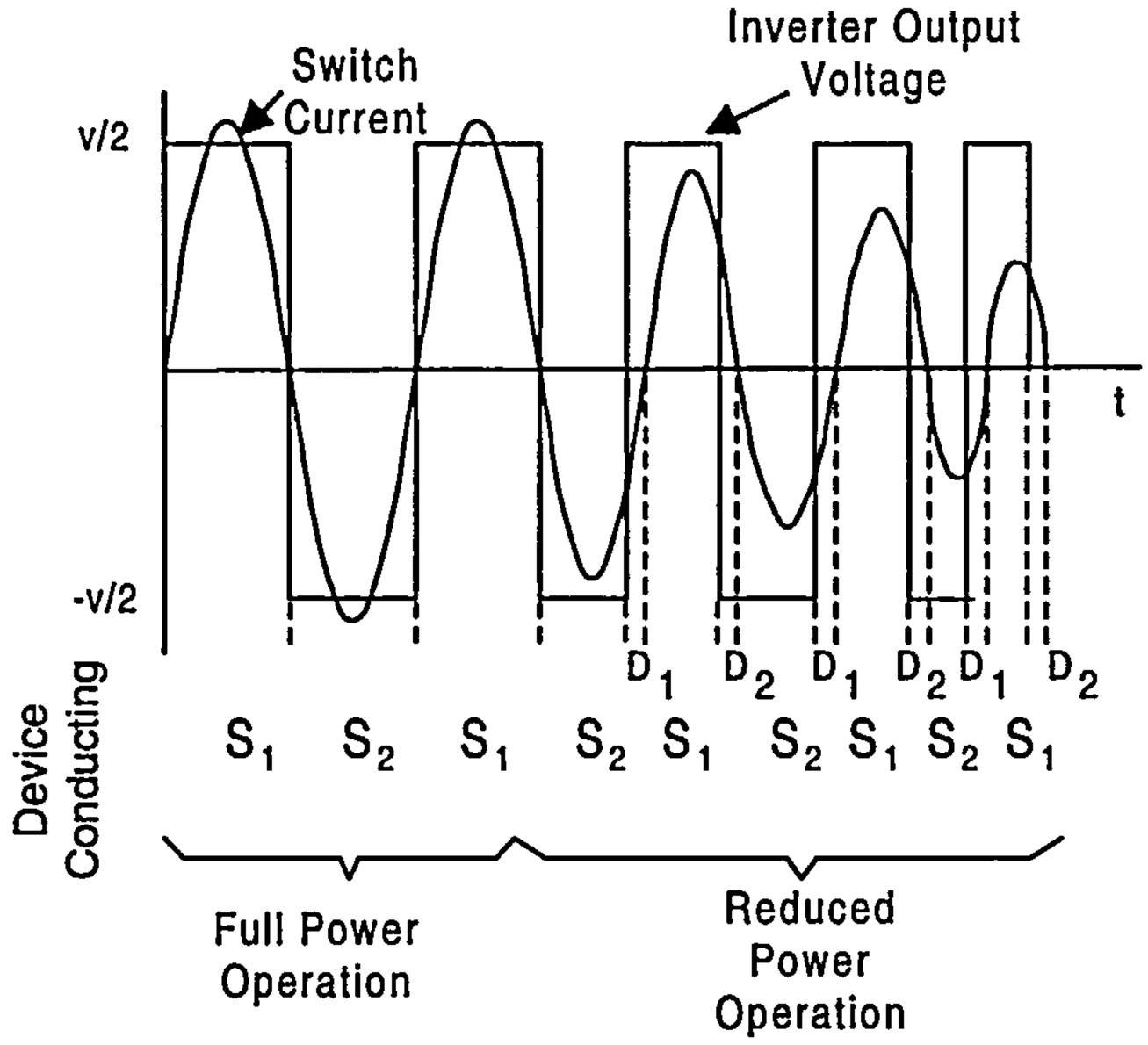

Fig. 4.2: Variable-frequency power control

when the circuit is operated at full power, near to the resonant frequency, as the circuit relies on the load current to charge the capacitor. The problem of above-resonance operation was reported in the LCC-type parallel-resonant converter proposed by Batarseh *et. al.* [124].

The limited-load-range problem is also found in [45], and it is suggested by Tabisz *et. al.* [125] that use of a modified converter, namely a multi-resonant converter, would improve the load range. However, according to Dananjayan *et. al.* [126], owing to the requirement of a wide-band frequency-modulation in obtaining output voltage regulation over a wide range of load and output voltage, the optimal values for filter components are difficult to establish.

There are other different strategies to obtain variable-frequency control. For example, control of the conduction time of the controlled switches, where the turn-off controlled switches are required to cause the commutation of the inverter [AlHaddad et al., 1988, AlHaddad et al., 1989]; control of the switching time by the integral of the difference between a voltage proportional to the full-wave rectified current in the resonant network and a zero reference voltage [Schwarz, 1970, Schwarz, 1976]; and control of the state trajectory in order to continuously monitor the energy level of the resonant tank [127].

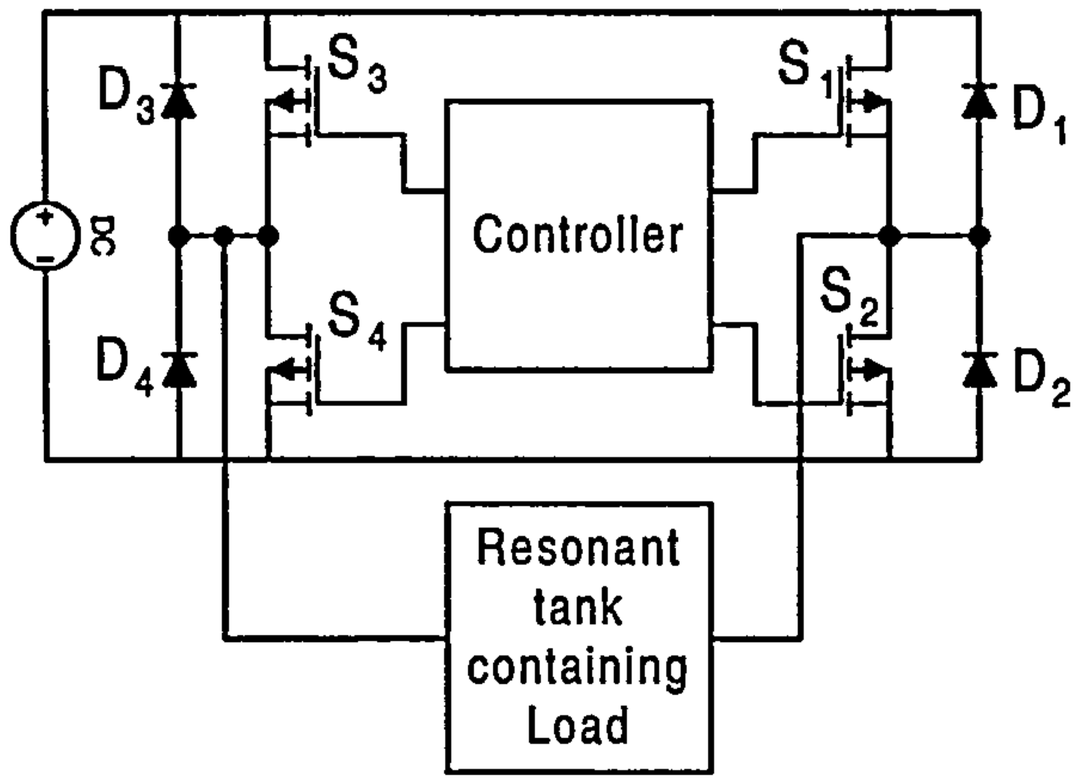

Fig. 4.3: Full-bridge inverter for power control illustration

4.2.2 Fixed-frequency Control

In this method, power control is achieved by *zero-volt loop operation*, where a period of time is introduced around each zero-crossing of the current of any one of the four switches [128]. Again, non-zero-current switching is obtained when the zero-volt loop increases, leading to switching losses in both the switches and freewheel diodes, and, therefore, this limits the maximum operating frequency. As lossless capacitive snubbers cannot be used in fixed-frequency operation due to the excessive current in charging the snubbers [3], Jain [129] later came up with an idea of making use of the parallel-leg of the circuit as a high-frequency filter, and to place snubber capacitors around the switches to minimize the switching losses. However, stray oscillations may become a problem in this case.

The illustration of fixed-frequency operation, adapted from [3], is depicted in Fig. 4.4

Other strategies for fixed frequency control of resonant converters have also been proposed to overcome the problems faced by frequency-modulation quasi-resonant converters. They are well documented in [130–132]. However, constant switching frequencies are maintained only with additional independent complex control. Although Dananjayan *et. al.* [126] have proposed a fly-back constant-frequency zero-current-switching/zero-voltage-switching quasi-resonant converter, the auxiliary switch does not operate at true zero-voltage switching. Further, it is questionable if this switch can sustain the high-voltage stress involved. In addition, the resonant inductor is not optimally utilized during each switching cycle.

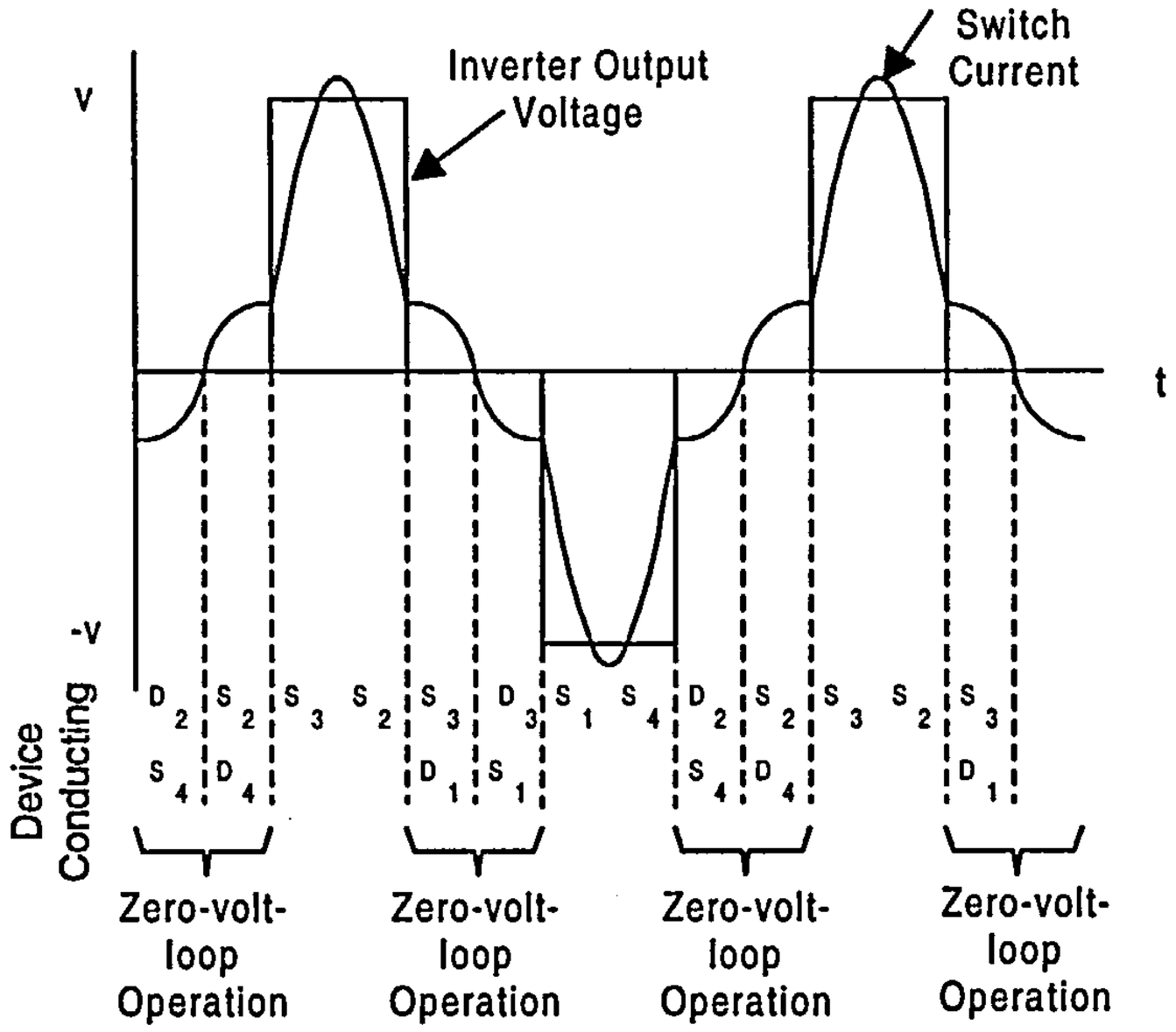

Fig. 4.4: Fixed-frequency power control

4.2.3 Dead-time Control

Dead-time control introduces a delay period between the turn-on time of each switch to obtain reduced power while maintaining zero-current-switching. The excessive current is transferred to the corresponding freewheel diode in the circuit before returning to zero. The zero-current remains until the next switch turns on. Zero-current-switching is maintained at all power levels [109]. The major disadvantages of dead-time control are the high current ripple in reduced-power modes, and the discontinuous load current when it is employed in the load-resonant circuit [3]. This is illustrated by redrawing the diagram as Fig. 4.5.

4.3 Different Analyses of Resonant Converters

Resonant converters are analyzed in either the *time-domain* or *frequency-domain*. Most of the time domain analyses are based on the *state space technique*. Steigerwald derived state-space equations for high-frequency resonant transistor dc-dc converters in [12]. State-space equations were formed for the resonant tank and dc output filter of the converters in order to obtain second-order equations, which were later integrated numerically using the Runge-Kutta algorithm until the voltage polarity of the resonant capacitor is reversed.

Bhat and Dewan [133] analyzed the LCC-type converter in two modes of operation. One mode followed another in a repetitive way as the polarity of the output-capacitor voltage changed.

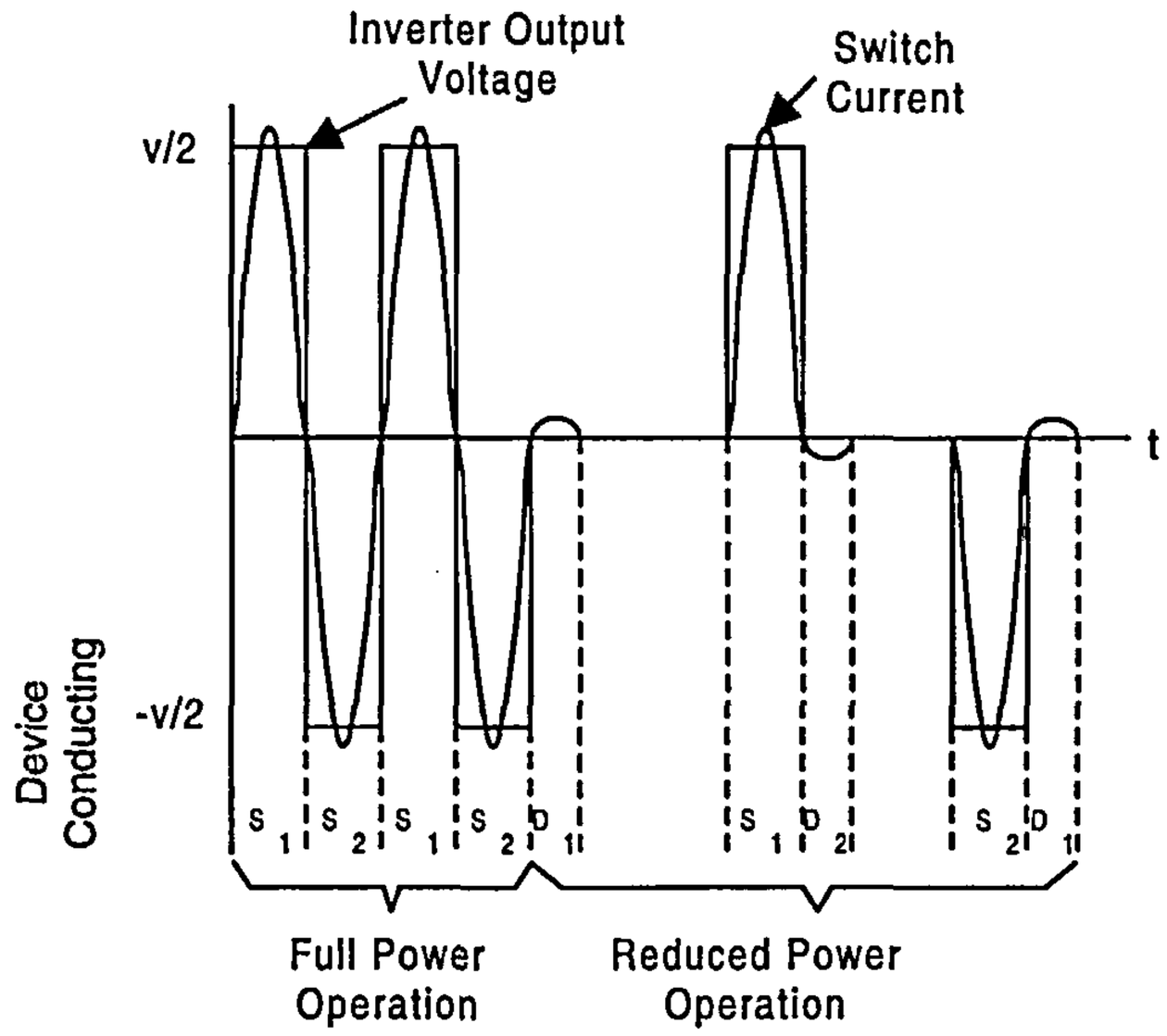

Fig. 4.5: Dead-time power control

State-space equations were formed for the two modes separately. The analysis showed that the LCC inverter could be described by the initial conditions of the passive elements. This led to the evaluation of the steady-state operation of the circuit. In the above two cases, design curves needed to be established to determine the values of the passive components. The same authors [134] analyzed the resonant inverters using *Fourier analysis* in the continuous mode by combining all the commutation schemes into a generalized scheme.

Batarseh *et. al.* [124] designed the LCC-type resonant converter using the *phase-plane approach*, which is an extension of state-space analysis. In the phase-plane analysis, a steady-state trajectory for the circuit was plotted before the design curves were drawn. A similar approach was actually employed in [127, 135].

Due to the lack of information on the dynamic behavior of the converters, when analyzed in steady-state analysis, a paper on the generalized approach to resonant converters using discrete *small-signal analysis* was presented in [136]. The approach is based on *Taylor's series* and the phase-plane diagram. Small-signal analysis [Mattavelli et al., 1997] was also used to obtain the control coefficients, output and input impedance, transfer functions of the circuit, and so on, so that an efficient control strategy can be employed on the resonant converter.

Bhat [137] proposed a simple analysis of PWM high-frequency link series-parallel resonant converters in the frequency-domain. All the basic quantities were expressed in per-unit basis to enable the author to obtain the value of the output voltage, circuit impedance and the current

flowing through the devices. This is actually based on the *ac circuit analysis* done in [46, 138]. Later, the same author published a series of papers on the analysis of series-parallel resonant converters [139–141]. The circuits were simplified to a series resonant converter with only a single resonant frequency. The leakage inductance of the transformer was neglected in these analyses. Similar approaches were adopted in [142–144].

A small-signal model, in the frequency-domain, was given in [Collomb et al., 1993, Collomb et al., 1994] in attempting to deal with the closed-loop behavior of dc-dc series-resonant converters. Linear-control strategies were employed, and their closed-loop performances were compared. A phase-plane diagram was employed to determine all the steady-state quantities.

Hsieh *et. al.* [145] studied an isolated off-line zero-voltage-switched PWM converter in a dc analysis, and small-signal model derivation for the stability issues of the converters. These authors devised the operation states into power transfer, linear charge and discharge, and resonant states before proceeding to the small-signal analysis. A design procedure was outlined.

A comprehensive analysis on series-resonant converters in the frequency-domain was performed by Kazimierczuk *et. al* [146] to study the steady-state operation of the converters. Analytical equations were derived for the performance parameters of the converters operating in the continuous conduction mode using *Fourier analysis.*

All the above-mentioned analyses do not allow the component values of the resonant converter to be determined for the desired frequency response of the circuit in general, and for a specific set of resonant frequencies in particular. This led to the following analysis done by the present author's colleagues.

4.4 Analysis of Load-resonant in the Frequency-domain using Impedance Concept

4.4.1 Series-parallel Load-resonant Converter

Pollock *et. al.* [3–6] analyzed the series-parallel load resonant converter shown in Fig. 4.6 in the frequency-domain by representing the half-bridge converter with a simple ac model depicted in Fig. 4.7.

The dc input, electronic controller and switches are replaced by a simple sinusoidal voltage of fixed frequency. It was shown in [3] that the frequency of the applied voltage is equal to the fundamental frequency of the square-wave voltage, applied in the real converter. The effect of the

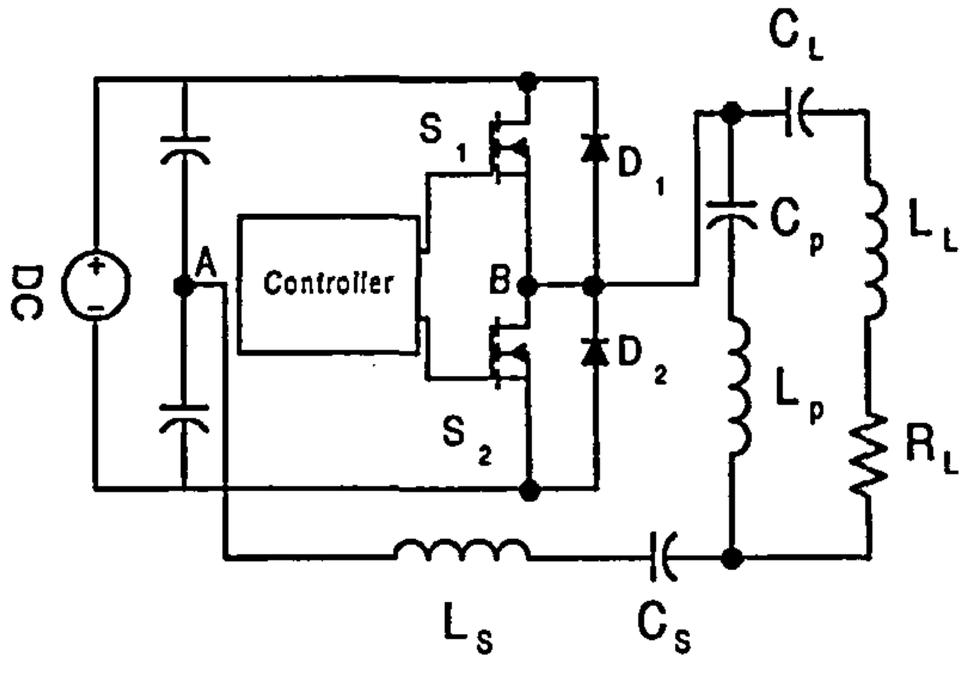

Fig. 4.6: Half-bridge series-parallel load-resonant converter

neglected harmonic component of the square-wave voltage is usually ignored by most researchers, but it was taken into consideration by Pollock *et. al.* [3–6].

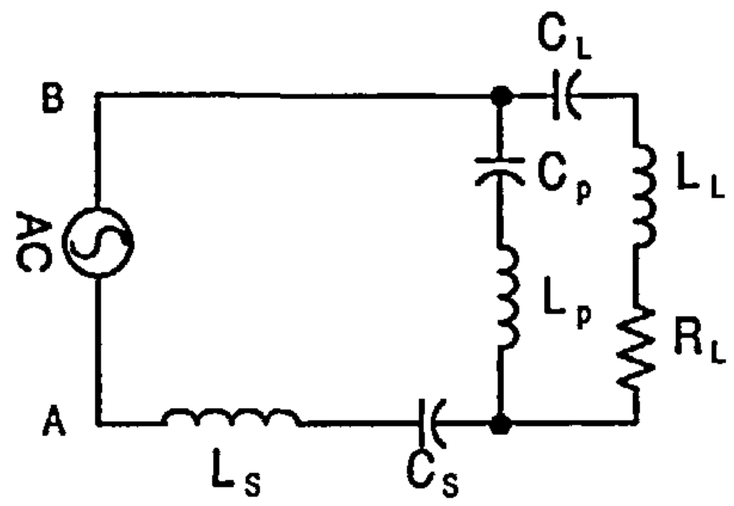

Fig. 4.7: Simplified series-parallel load-resonant converter

The simplified model consists of three legs, namely the series-leg, parallel-leg and load-leg labeled by subscripts, $_s$, $_p$ and $_L$ respectively. Each leg comprises an inductor, L, and a capacitor, C, with an extra load, R, referred to the primary side of the transformer from its secondary side in the load-leg. The inductor in the load-leg is included to represent the leakage inductance of the transformer and any load inductance that may be present whereas the capacitor is there to reduce the possible effective-load inductance if required. The high-frequency transformer was assumed to have zero-magnetising current by Pollock *et. al.*.

4.4.2 Mathematical Analysis of the Circuit

The total input impedance, Z_{tot} of the load-resonant converter, seen by the source can be derived as shown in [3–6],

$$Z_{tot} = \frac{R_L X_p^2 + j(X_s R_L^2 + X_s X_L^2 + 2X_s X_p X_L + X_s X_p^2 + X_p X_L^2 + X_p^2 X_L + X_p R_L^2)}{R_L^2 + (X_L + X_p)^2} \qquad (4.1)$$

and, when Z_{tot} is completely real, the circuit is defined to be operating at a resonant frequency, so that the equivalent input resistance, R_{tot} of the circuit at a resonance is given by,

$$R_{tot} = \frac{R_L X_p^2}{R_L^2 + (X_L + X_p)^2} \tag{4.2}$$

Using ac analysis, which has also been used in [3–5], the impedance of the resonant circuit (4.1) at a particular resonant frequency, ω, can be rewritten as,

$$Z_{tot} = \frac{a_1\omega^5 + a_2\omega^3 + a_3\omega + j(b_1\omega^6 + b_2\omega^4 + b_3\omega^2 + b_4)}{c_1\omega^5 + c_2\omega^3 + c_3\omega} \tag{4.3}$$

where,

$$\begin{aligned}
a_1 &= C_s C_p^2 L_p^2 C_L^2 R_L \ ; \\
a_2 &= -2C_s C_p L_p C_L^2 R_L \ ; \\
a_3 &= C_s C_L^2 R_L \ ; \\
b_1 &= C_s C_p^2 C_L^2 (L_p L_L^2 + L_p^2 L_L + L_s L_L^2 + \\
&\quad L_s L_p^2 + 2L_s L_p L_L) \ ; \\
b_2 &= C_s C_p^2 C_L (-L_p^2 - 2L_s L_L - 2L_p L_L - 2L_s L_p) + \\
&\quad C_s C_p C_L^2 (-L_L^2 - 2L_p L_L - 2L_s L_L - 2L_s L_p) + \\
&\quad C_p^2 C_L^2 (-L_L^2 - 2L_p L_L - L_p^2) + \\
&\quad C_s C_p^2 C_L^2 R_L^2 (L_p + L_s) \ ; \\
b_3 &= C_s C_p (L_p C_p + L_s C_p + 2L_p C_L + 2L_L C_L + \\
&\quad 2L_s C_L - C_L^2 R_L^2) + \\
&\quad C_s C_L^2 (L_L + L_s) + \\
&\quad C_p^2 C_L (-C_L R_L^2 + 2L_L + 2L_p) + \\
&\quad 2C_p C_L^2 (L_L + L_p) \ ; \\
b_4 &= -C_s C_p - C_s C_L - C_p^2 - 2C_p C_L - C_L^2 \ ; \\
c_1 &= C_s C_p^2 (C_L^2 L_L^2 + 2L_p C_L^2 L_L + L_p^2 C_L^2) \ ; \\
c_2 &= C_s C_p^2 (C_L^2 R_L^2 - 2C_L L_L - 2L_p C_L + \\
&\quad C_s C_p (-2C_L^2 L_L - 2L_p C_L^2) \ ; \\
c_3 &= C_s C_p^2 + 2C_s C_p C_L + C_s C_L \ ;
\end{aligned}$$

At resonance, the inductance and capacitance effects are balanced out, which hence makes the imaginary parts of eqns.(4.1) and (4.3) equal to zero. They are given respectively as

$$(X_s R_L^2 + X_s X_L^2 + 2X_s X_p X_L + X_s X_p^2 + X_p X_L^2 + X_p^2 X_L + X_p R_L^2) = 0 \tag{4.4}$$

$$b_1\omega^6 + b_2\omega^4 + b_3\omega^2 + b_4 = 0, \tag{4.5}$$

so the input impedance of the circuit acts like a pure resistor, giving rise to the input resonant resistance of the circuit, R_{tot}, at frequency, ω, as,

$$R_{tot} = \frac{a_1\omega^5 + a_2\omega^3 + a_3\omega}{c_1\omega^5 + c_2\omega^3 + c_3\omega} \tag{4.6}$$

where (4.6) is equivalent to (4.2). Resonance can also be defined as the in-phase input-voltage and input-current conditions in this work.

Eqn. (4.5) was then normalized to become

$$\omega^6 + k_a\omega^4 + k_b\omega^2 + k_c = 0, \tag{4.7}$$

where the coefficients are

$k_a = b_2/b_1$

$k_b = b_3/b_1$

$k_c = b_4/b_1$

By letting $\omega^2 = \Omega$, Eqn.(4.7) becomes

$$\Omega^3 + k_a\Omega^2 + k_b\Omega^1 + k_c = 0, \tag{4.8}$$

The roots of Eqn.(4.8) are $\Omega = \omega_0^2, \omega_1^2, \omega_2^2$, in which case $\omega = \pm\omega_0$, $\omega = \pm\omega_1$ and $\omega = \pm\omega_2$. From the theory of equations, Eqn. 4.9 is obtained.

$$\Omega^3 + k_a\Omega^2 + k_b\Omega + k_c \equiv \omega^6 - (\omega_0^2 + \omega_1^2 + \omega_2^2)\omega^4 + (\omega_0^2\omega_1^2 + \omega_1^2\omega_2^2 + \omega_2^2\omega_0^2)\omega^2 - \omega_0^2\omega_1^2\omega_2^2 \tag{4.9}$$

The equations for k_a and k_c were combined to eliminate ω_2^2 yielding a quadratic equation in ω_1^2

$$\omega_1^4 + \omega_1^2(k_a + \omega_0^2) - \frac{k_c}{\omega_0^2} = 0 \tag{4.10}$$

where ω_1^2 is then given by

$$\omega_1^2 = \frac{-(k_a + \omega_0^2) \pm \sqrt{(k_a + \omega_0^2)^2 + \frac{4k_c}{\omega_0^2}}}{2} \tag{4.11}$$

This allows the third root of Eqn. (4.9), i.e. ω_2^2, to be found by rearranging k_a in the Eqns. (4.7).

$$\omega_2^2 = -k_a - \omega_0^2 - \omega_1^2 \tag{4.12}$$

Clearly, eqns. (4.11) and (4.12) show the possibility of the two turning-point frequencies to be found by knowing the other frequency, ω_0 and the k parameters that are functions of the component values.

It is important to note that the three pairs of turning-point frequencies, i.e. two resonances and one anti-resonance, all correspond to the frequencies at which the series-parallel load-resonant converter appears resistive, and at each of these resonant frequencies, there is a different equivalent input-resistance, R_{tot}, which was given in Eqn. (4.6). Each R_{tot} value is associated with an output power level exhibited by the converter at that turning-point frequency.

It is reported in [5] that the multiplicity of the resonant frequencies, shown in Eqn.(4.9), in the converter according to Pollock *et. al.* was significant in designing the converter, and the circuit is predominantly capacitive at low frequencies, becomes inductive above the first resonant frequency, changes back to being capacitive, before finally becoming inductive above the upper resonant frequency.

4.5 Design Procedure for Calculating the Component Values

The mathematical analysis shows that the frequency characteristics of the load-resonant converter can be predicted by knowing the values of the resonant components. However, the essence of designing resonant converters lies more in the capability of obtaining appropriate passive component values to acquire the required frequency characteristics based on the applications of the converters. To achieve this, the turning-point frequencies together with the referred load resistance, R_L, the load inductance, L_L, the load capacitance, C_L and the desired input resistance of the circuit at resonance, R_{tot}, were pre-specified. This allowed the remaining component values to be found. The following shows the order of equations to be derived based on this analysis. The derived equations

were then written in a reversed order in order to establish the design procedure.

As there were four components, C_s, L_s, C_p and L_p, to be calculated in [3–6], at least four equations were required to find the solutions simultaneously. From the equation of total input impedance of the circuit, (4.1), two basic equations, i.e. (4.5) and (4.6), were obtained at resonant conditions. Further manipulation of equations (4.5) produces the set of three equations, which were given in (4.7). Therefore, four system equations, i.e. one denoted by (4.6) and three given in (4.7) were yielded.

It is known that in the series configuration, the reactance consisting of an inductor and a capacitor can be written as $X = \omega L - \frac{1}{\omega C}$. This allowed the series components in each leg to be written for the associate capacitance, i.e. $C = \frac{1}{\omega(\omega L - X)}$. The corresponding capacitances, C's, were then substituted in the coefficients of (4.7), where the coefficients, k_a, k_b and k_c were given as,

$$\begin{aligned} k_a &= b_2/b_1 = f(C_s, L_s, C_p, L_p, C_L, L_L, R_L) \\ k_b &= b_3/b_1 = f(C_s, L_s, C_p, L_p, C_L, L_L, R_L) \\ k_c &= b_4/b_1 = f(C_s, L_s, C_p, L_p, C_L, L_L, R_L) \end{aligned} \tag{4.7}$$

This produced a new set of equations for k parameters in terms of corresponding reactances, X's, inductances, L's, and primary operating resonant frequency, ω_0, i.e. the set of k equations were expressed as,

$$\begin{aligned} k_a &= f(X_s, L_s, X_p, L_p, X_L, L_L, R_L, \omega_0) \\ k_b &= f(X_s, L_s, X_p, L_p, X_L, L_L, R_L, \omega_0) \\ k_c &= f(X_s, L_s, X_p, L_p, X_L, L_L, R_L, \omega_0) \end{aligned} \tag{4.13}$$

It should be noted that the k parameters are known values related to specified frequencies of the circuit by equations (4.9)

Equations (4.13) were then rearranged into three equations for L_s, i.e. the value of the series

inductance of the converter.

$$\begin{aligned} L_s &= f(k_a, X_s, X_p, L_p, X_L, L_L, R_L, \omega_0) \\ L_s &= f(k_b, X_s, X_p, L_p, X_L, L_L, R_L, \omega_0) \\ L_s &= f(k_c, X_s, X_p, L_p, X_L, L_L, R_L, \omega_0) \end{aligned} \tag{4.14}$$

The three equations given by (4.14) are equated, thereby eliminating L_s's, to yield three quartics in the parallel inductances, i.e. L_p's

$$\begin{aligned} L_p &= f(k_a, k_b, X_s, X_p, X_L, L_L, R_L, \omega_0) \\ L_p &= f(k_b, k_c, X_s, X_p, X_L, L_L, R_L, \omega_0) \\ L_p &= f(k_c, k_a, X_s, X_p, X_L, L_L, R_L, \omega_0) \end{aligned} \tag{4.15}$$

Each of these quartics has four roots for L_p. The coefficient of any L_p term in one equation was equated to the same coefficient of the same term in the other equations to get rid of L_p's, and this process was repeated three times to give a quadratic in series reactance, X_s, which has two solutions, where one of the solutions is $X_s = -X_L$ while another solution is given by

$$X_s = f(k_a, k_b, k_c, X_p, X_L, L_L, R_L, \omega_0) \tag{4.16}$$

All the component values in eqn. (4.16) are known except X_p. Therefore in order to obtain the values of X_s and X_p, the following processes were carried out.

Eqn. (4.4) was rearranged to yield X_s,

$$X_s = -\frac{X_p(X_pX_L + X_L^2 + R_L^2)}{R_L^2 + (X_L + X_p)^2} \tag{4.17}$$

This equation together with (4.2) were combined to produce a second equation for X_s, which is

$$X_s = -\frac{R_{tot}(X_pX_L + X_L^2 + R_L^2)}{(R_L + X_p)} \tag{4.18}$$

Eqns. (4.16) and (4.18) were then equated to produce a cubic polynomial given by

$$f_1(k_a, k_b, k_c, X_p, X_L, L_L, R_L, \omega_0) = 0 \tag{4.19}$$

Rearranging the cubic polynomials for X_p, with each X_p being a function of known design parameters, gives,

$$X_p = f_1(k_a, k_b, k_c, X_L, L_L, R_L, \omega_0) \tag{4.20}$$

These led to three solutions for X_p's.

A design procedure was written based on the reversed order of the above process in obtaining X_p's. By specifying X_L, L_L, R_L, R_{tot}, ω_0, ω_1 and ω_2, a system with unknown X_p, X_s, L_p and L_s was successfully prescribed as ordered. Knowing the values of the reactances, X's, and the inductances, L's, the capacitances, C's in the series and parallel legs were obtained.

The analysis in this chapter was reviewed based on the *solving-simultaneous-equations* method carried out by Pollock *et. al.*. This approach has been used successfully in designing a multi-resonant-frequency load-resonant converter for welding purposes. In addition, the relationship between the frequencies and the component values of the resonant circuit were successfully established. Above all, the method has verified that there is a corresponding resistance, or output power level, associated with each turning-point frequency. By managing the different values of resistances at different turning-point frequencies, yielding different output power levels, power delivered to the load of the converter can be controlled accordingly. This concept was somehow adopted in the design process in an essentially trial-and-error manner to produce required frequency characteristics with significant output power change. Nevertheless, a more systematic method incorporating the 'second' resistance in the design procedure had yet to be found.

The following section is devoted to the description of the failure of incorporating the 'second' resistance in the design procedure using the solving-simultaneous-equations method.

4.6 Limitation of the Solving-simultaneous-equations Method

In order to achieve the aim of controlling the resistance level at each turning-point frequency, and hence the output power of the converter, which was suggested in [3–6], it is necessary to include a 'second' resistance at resonance, R_{tot_b}, in the design procedure.

As has been shown earlier the pure resistance at each resonant frequency is given by,

$$R_{tot} = \frac{R_L X_p^2}{R_L^2 + (X_L + X_p)^2} = \frac{a_1\omega^4 + a_2\omega^2 + a_3}{c_1\omega^4 + c_2\omega^2 + c_3} \tag{4.6}$$

Theoretically, the circuit can be designed with different values of R_{tot} at each of the turning-point frequencies of the circuit to obtain the maximum power change and minimum phase difference between the frequencies. Therefore, eqn. (4.6) can be rewritten for resistances at two different resonant frequencies, i.e. input resistance at resonant frequency ω_0,

$$R_{tot_a} = \frac{R_L X_{p_a}^2}{R_L^2 + (X_{L_a} + X_{p_a})^2} = \frac{a_1\omega_0^4 + a_2\omega_0^2 + a_3}{c_1\omega_0^4 + c_2\omega_0^2 + c_3}, \tag{4.21}$$

and input resistance at resonant frequency ω_1,

$$R_{tot_b} = \frac{R_L X_{p_b}^2}{R_L^2 + (X_{L_b} + X_{p_b})^2} = \frac{a_1\omega_2^5 + a_2\omega_2^3 + a_3\omega_2}{c_1\omega_2^5 + c_2\omega_2^3 + c_3\omega_2}. \tag{4.22}$$

R_{tot_a} and R_{tot_b} need different values of the reactances X's since they are the different equivalent resistance values at two different turning-point frequencies, ω_0 and ω_2

There are now five system equations to solve for the four component values. The five equations can be obtained from (4.7), (4.9),(4.21) and (4.22) and the unknown components are L_s, C_s, L_L and C_L this time.

The same procedure as described in Section 4.4.2 was carried out. Nevertheless, different component values were pre-specified, and the order of solving for the unknowns varied from the previous one. The intended way of solving the component values in a different order is summarized in Fig. 4.8

From the total-input-impedance equation given in (4.1), the parameters k's, shown in (4.7), were obtained. The equations, together with both equations for R_{tot}'s given in (4.21) and (4.22), were rearranged in terms of the reactances, X's, instead of the L's. Thus,

$$k_a = k_b = k_c = f(X_{s_a}, C_s, X_{p_a}, C_p, X_{L_a}, C_L, R_L, \omega_0) \tag{4.23}$$

$$R_{tot_a} = f(X_{p_a}, C_p, X_{L_a}, C_L, R_L) \tag{4.24}$$

$$R_{tot_b} = f(X_{p_b}, C_p, X_{L_b}, C_L, R_L) \tag{4.25}$$

The three equations for the k's, (4.23) were rearranged into three equations for capacitor values,

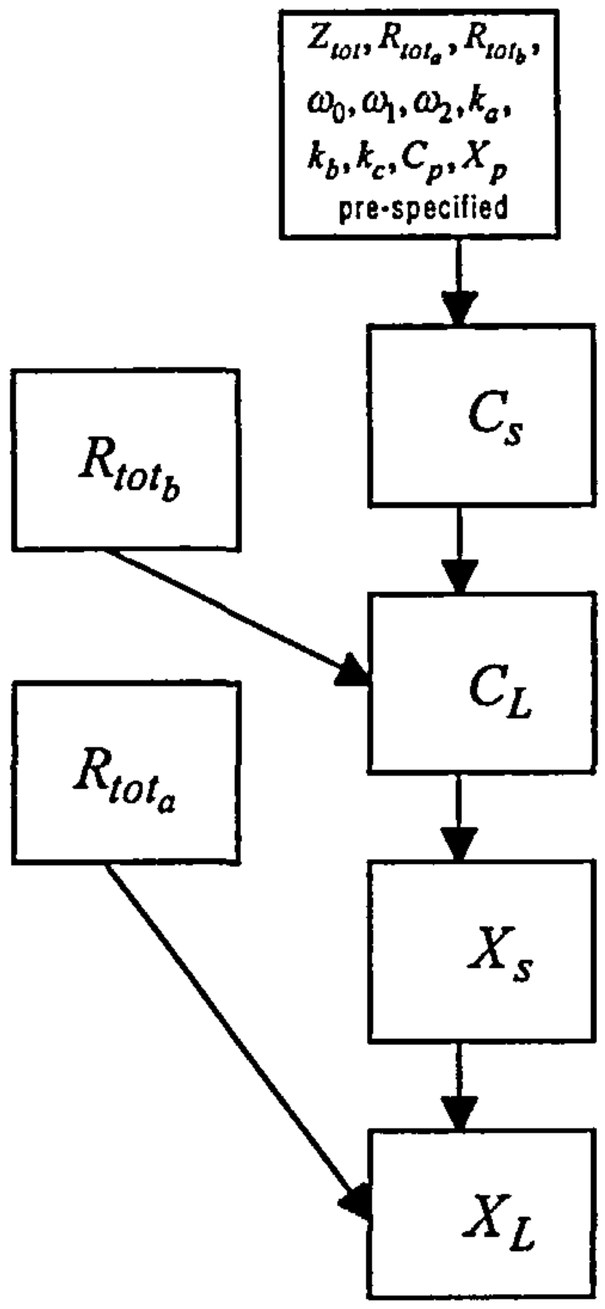

Fig. 4.8: Summary of calculating the component values with a 'second' R_{tot}

C's, to give

$$\begin{aligned} C_s &= f(k_a, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, \omega_0) \\ C_s &= f(k_b, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, \omega_0) \\ C_s &= f(k_c, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, \omega_0) \end{aligned} \tag{4.26}$$

Rearrange the equation for R_{tot_b} given in (4.22) to give

$$R_L^2 = \frac{R_L X_{p_b}^2 - R_{tot_b}(X_{L_b} + X_{p_b})^2}{R_{tot_b}} \tag{4.27}$$

The reactances in Eqn.(4.27) were re-phrased in terms of the values of the inductances, the capacitances and appropriate turning-point frequency, i.e. ω_2. The obtained inductance terms were further replaced by $L = \frac{\omega_0 XC+1}{\omega_0}$. The Eqn. (4.27) may then be written as,

$$R_L^2 = f(X_{p_a}, C_p, X_{L_a}, C_L, R_L, R_{tot_b}, \omega_0, \omega_2) \tag{4.28}$$

The R_L^2 terms, instead of R_L terms, in (4.26) were substituted from equation (4.28) to give,

$$\begin{aligned} C_s &= f(k_a, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, R_{tot_b}, \omega_0, \omega_2) \\ C_s &= f(k_b, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, R_{tot_b}, \omega_0, \omega_2) \\ C_s &= f(k_c, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, R_{tot_b}, \omega_0, \omega_2) \end{aligned} \tag{4.29}$$

These three equations were then equated to eliminate the C_s's, and hence yield three quartic polynomials given as

$$\begin{aligned} f(k_a, k_b, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, R_{tot_b}, \omega_0, \omega_2) &= 0; \\ f(k_b, k_c, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, R_{tot_b}, \omega_0, \omega_2) &= 0; \\ f(k_c, k_a, X_{s_a}, X_{p_a}, C_p, X_{L_a}, C_L, R_L, R_{tot_b}, \omega_0, \omega_2) &= 0; \end{aligned} \tag{4.30}$$

They can be written in the form of

$$\begin{aligned} a_1 C_L^4 + b_1 C_L^3 + c_1 C_L^2 + d_1 C_L + e_1 &= 0; \\ a_2 C_L^4 + b_2 C_L^3 + c_2 C_L^2 + d_2 C_L + e_2 &= 0; \\ a_3 C_L^4 + b_3 C_L^3 + c_3 C_L^2 + d_3 C_L + e_3 &= 0; \end{aligned}$$

respectively.

The coefficients of the quartics could not be equated this time as they do not produce the exact same four roots as obtained before in section 4.4.2. Thus, *Mathematica*, a symbolic mathematical tool, was used to solve the quartic polynomials directly to yield four different expressions for C_L. They are all in terms of the k parameters, reactances, capacitance and resistances, i.e.

$$C_L = f(k_a, k_b, X_s, X_p, C_p, X_L, R_L, R_{tot_a}, \omega_0) \tag{4.31}$$

At this stage, there were still three unknowns, i.e. C_L, X_L and X_s.

The problem of the solving-simultaneous-equation method was confirmed when the mathematics was growing more complicated. No solution has yet been achieved with this method. The basic problem was that radical division was incurred when the equations were attempted to be solved for C_L. In the mathematical sense, when a radical is encountered in a set of polynomials, the approach can give no solution at all to the set. In other words, the analytical method proposed by Pollock *et.al.* may not be suitable for further analysis of the resonant system.

The difficulty may be due to a number of reasons, such as the 'wrong' order of solving the

component values, leading to intractable mathematical complication, or no solution, or no possible solution at all by adding a 'second' resistance to the resonant system from mathematical point of view. Ways of overcoming these difficulties using the *solving-simultaneous-equation* method was therefore abandoned. However, the system was further investigated adopting a better and more efficient approach, using a modern abstract algebra-algorithm based on the *Gröbner Basis*. If the problem was able to be solved by this approach, which, so far as the author is aware has never previously been used in electric network theory, let along power electronics, a novel approach in controlling output power of the load-resonant converter was invented. The next chapter is devoted to an introduction to the approach.

4.7 Conclusion

The solving-simultaneous-equations method proposed by the author's colleague was reviewed in this chapter. The significant finding of the proposed approach is that the realization of managing-the-resistance-level concept could lead to successful control of output power of the load-resonant converter. As its output power change was obtained in a trial-and-error manner, a more systematic approach was hoped for to find the solutions by including a second determining factor, i.e. R_{tot} in the design process. Unfortunately, this approach led to intractable difficulties and was abandoned. An alternative method of attack was sought successfully.

A frequency-domain analysis technique is still adopted in the new approach, mainly because of the following reasons,

- It leads to simple analytical equations relating the circuit performance parameters, e.g. frequency response, to the passive-component values.
- Circuit transfer function can be derived easily.
- It provides easy-to-use design tool which fits well into the new approach.

Chapter 5

The Gröbner Basis Techniques for Load-resonant Power Control

5.1 Introduction

In this chapter, an introduction to a very general method of designing electrical networks is given based on the *Gröbner Basis* theory(GB) [147]. The author is unaware of such theory being used previously in electrical network applications.

Although the GB methods are virtually unknown in the engineering community, and have their origins in what engineers would regard as an arcane field of abstract algebra, this hardly matters since programs for doing the associated computational work are readily available in computer libraries. In practice, it turns out that quite extensive designs can be performed by employing a reasonable understanding of electric-circuit theory together with these programs.

Due to the somewhat-novel concept of the GB technique in the engineering field, this chapter is devoted to presenting the technique for solving problems associated with polynomial expressions. It is then shown, by simple examples, how the technique can be useful in the solution of electrical-circuit problems. The idea of this approach is to give the reader an appreciation as to what the GB is about, without a detailed mathematical explanation. The examples are for illustrative purposes only, and would normally be tackled quite effectively by well-known techniques - one certainly would not employ the GB method in practice here.

This is followed by the application of the GB in solving some problems found while dealing with the design of resonant circuits for series-parallel load-resonant converters. Simulation results, are presented, and these are compared to the experimental results described by the author's colleagues

in [5, 148].

5.2 Background on the GB

There is a considerable literature on the GB [149–153]. Unfortunately, the problem is that most of this work, in this area, is written in abstract algebra fashion and it is not, normally, within the repertoire of most engineers and physical scientists. Nevertheless, the GB leads to very practical and powerful algorithms; some of which are specifically aimed at solving for the zeros of *multivariate*[1] polynomials. The treatment described in the following relies very heavily on the approach of Forsman [154]. This is a reference which itself is very aptly subtitled DON'T PANIC. Others of the more easily understandable works can be found in [155–160].

5.3 An Elementary Algebraic Problem

Suppose it is required to find the solutions of the two simultaneous polynomial equations,

$$f_1 = x^2 + y^2 - 2 \tag{5.1}$$

$$f_2 = xy - 3 \tag{5.2}$$

A way of doing this is to rearrange equation (5.2)[2] in the form

$$x = \frac{3}{y} \tag{5.3}$$

and substitute this into equation (5.1). Then after simple rearrangement, thereby results,

$$y^4 - 2y^2 + 9 = 0, \tag{5.4}$$

i.e. the two equations in two unknowns have been rearranged into a polynomial equation in one unknown.

The y values for the roots can be found straight-forwardly, and then the values of the corresponding x values can be obtained by back-substitution.

---

[1] a *multivariate* polynomial is a polynomial comprising several variables

[2] This is the way polynomials are written in the mathematical literature

Suppose now, it is required to solve the following pair of multivariate polynomials,

$$x^4y - 4 = 0$$
$$x^5y^2 + 2x + 2 = 0$$

After some examination, it is possible that a method different to that above would be attempted. The point is that in tackling this sort of problem, heuristic approaches are normally sought. There is, however, a systematic way of solving the multivariate-polynomial problem, and this way is based on the GB.

5.4 The Gröbner Basis(GB)

For nearly two decades, the GB have been a critical tool in the development of computational techniques for the symbolic solution of polynomial sets of equations. Indeed, even before this time, Buchberger introduced the notion of GB for a polynomial ideal and an algorithm for their computation [Buchberger, 1965], [161]. In effect, the algorithm provides a way of eliminating variables from a set of polynomials and, thereby, represents the original set by a simpler and more suitably defined form for possible solutions. The essentials are illustrated by the following.

Given a set of multivariate polynomials, $F = \{f_1, \ldots, f_n\}$, where,

$$\begin{aligned} f_1 &= 0 \\ &\vdots \\ f_n &= 0, \end{aligned}$$

multiply each of these by other polynomials and add them together to form

$$a_1 f_1 + \ldots + a_n f_n$$

where $a_1, \ldots, a_n$ are polynomial coefficients. Note the a_i's may, themselves, be polynomials. The resulting set of polynomials is said to be an *ideal*, denoted by I, of the generating set, F. Thus, the ideal can be regarded as consisting of all 'polynomial consequences' of the equations $f_1 = f_2 = \ldots = f_n = 0$, under addition and multiplication operations.

The polynomials $f_1, \ldots, f_n$ are called a *basis* of the *ideal* they generate, I in this case, and since F is finite, the ideal I is said to be finitely generated. Thus, the ideal generated by F

consists of the set of linear combinations of the generators, $f_1, \ldots, f_n$, with polynomial coefficients, $a_1, \ldots, a_n$. Note that, there are several bases for an ideal, as other sets of polynomials can generate the same ideal, i.e. generally there are sets of polynomials, $h_1, \ldots, h_m$, and polynomial coefficients $b_1, \ldots, b_m$, such that

$$b_1 h_1 + \ldots + b_m h_m = a_1 f_1 + \ldots + a_n f_n$$

The Gröbner Basis is a particular set of generators, among the many different possible bases for an ideal.

The most important practical ingredients available from the GB usage are the variable-elimination and the GB-algorithm processes. During the elimination, *ranking*[3] of the variables is chosen in order to determine which variables are to be eliminated first. The GB, w.r.t. an elimination-ranking, is in the *triangular*[4] form as far as is possible. New polynomials p are formed from any pair of equations, f_i, f_j, contained in the polynomial set, F, in the following way:

$$p = \alpha f_i + \beta f_j$$

where α and β are polynomial coefficients. The set of all such p is, therefore, an ideal generated by F. This means that all new polynomials formed have at least those zeroes that are common to the original polynomials.

The GB-algorithm,[5] then chooses the α and β in a subtle fashion. Note that p, which is added to the original set, is in the ideal whereas α and β are arbitrary polynomials needed in the computation to produce p and may not necessarily be in the ideal itself.

How the GB-algorithm, i.e. the *Buchberger algorithm*[6] finds α and β is outlined in the following.

The Buchberger algorithm, employs the *S-polynomial* test[7], which is a generalization of the well-known division algorithm, to check whether the polynomial $p = \alpha f_i + \beta f_j$ is superfluous and

---

[3] *ranking* of variables is referred as *term-ordering* in polynomial ideal theory. The ranking determines which variables to eliminate first. For example, if x is to be eliminated first in order to get a polynomial in y only, then x should be higher ranked than y, written $x \succ y$.

[4] *triangular* form of a system is a polynomial set where a polynomial in the set has at least as few variables as the preceding polynomials. This enables variables to be eliminated consecutively, beginning with a polynomial comprising the least variables by extracting its roots and proceeding by back-substituting the result into the one comprising the most variables in the system.

[5] The GB-algorithm is called *Buchberger Algorithm* actually. It is equivalent to *Gaussian elimination* in linear, multivariate polynomial-case and identical with *Euclid's algorithm* in the case of two univariate polynomials

[6] The concept of the GB was introduced by Buchberger in 1965 [Buchberger, 1965]. It is a powerful tool in solving many important problems in polynomial ideal theory. Since 1965, it has been extensively studied, developed, refined ,and it has been implemented in most computer algebra systems

[7] S-polynomial test is a particular operation on a pair of polynomials to reduce the pair to a single polynomial or zero. The non-zero polynomial obtained, is called S-polynomial

therefore does not need to be added to the generating set.

The S-polynomial (see later) of any two polynomials, f_i and f_j, in F, is computed, and is denoted by $S(f_i, f_j)$. If the result of the computation is divisible by F, then the S-polynomial will be ignored. Otherwise, the single polynomial, obtained from the S-polynomial test, will be added to the basis, or the original generating set. Once this S-polynomial is introduced to the basis, the remainder of it, on division by F, will be reduced to zero[8]. This will not change the ideal generated as it is a linear combination of two polynomials of the basis. However, there will now be a new S-polynomial to be considered. The process is repeated for other combinations of any polynomial-pairs in the set.

When the algorithm terminates, it has produced two sets of polynomials; a zero-remainder set and a non-zero-remainder set on division of S-polynomial by the generating set, F. Both sets are consequences of those of the original. However, only the new non-zero-remainder set of polynomials (possibly including some old polynomials) is a GB of F w.r.t. the chosen term-order. Polynomial reduction w.r.t. a GB is canonical, i.e. the same ultimate results are obtained, no matter what term-order operation has been performed.

5.5 Computer-Algebra Packages for GB Computation

Many symbolic-algebraic-software packages for implementation of the above are commonly available. For example, *Mathematica* [162], *Maple* [163], *Reduce* [Hearn, 1991] have built-in functions that compute the GB. In addition to these more general software packages, there are other specialized software packages, written specially for the GB computation, such as *CoCOa*[9] [Capani and Niesi, 1995].

In the work described in this contribution, the *Mathematica* version 3.0, was used.

The built-in function of the GroebnerBasis, in *Mathematica*, has the following syntax:

GroebnerBasis[{polylist}, {vars_req}, {vars_eli}, opt]

where,

- polylist is a list containing the polynomial list of the original problem
- vars_req is a list of the variables of the polynomials, that are to be considered. This list determines the term-order of the variables: the highest term-order variable first and the lowest

[8]This will be proved in 5.6 later

[9]CoCOa is a non-commercial software developed at the University of Geneva, Italy. It is obtainable for free via anonymous FTP at `lancelot.dima.unige.it`.

one last

- vars_eli is a list containing the variables, that are to be eliminated.
- opt [10] gives the flexibility to specify different options for doing GB computations.

Consider solving for the GB of equations (5.1) and (5.2) again, only this time using the GroebnerBasis routine in *Mathematica.*

```
In[1]:= GroebnerBasis[{x^2+y^2-2,x*y-3},
        {x,y},CoefficientDomain ->
        RationalFunctions]
Out[1]= {9 - 2y^2 + y^4, 3x - 2y + y^3}
```

or

```
In[2]:= GroebnerBasis[{x^2+y^2-2,x*y-3},
        {y,x},CoefficientDomain ->
        RationalFunctions]
Out[2]= {9 - 2x^2 + x^4, 2x - x^3 - 3y}
```

Note that two different Gröbner Bases(GBs) have been obtained for the same generating set. Each of these two GB for a generating set was solved w.r.t. the chosen term-order, one solution was ordered in $x \succ y$[11], and another one was ordered in $y \succ x$. However, the final solutions for x and y are still the same for both cases. That is, the *polynomial reduction w.r.t a GB is canonical*, as stated previously, and the GB is not unique in these cases. Note also that each set of the GBs is in triangular form, for example, the first set of GB is {9 - 2y^2 + y^4 , 3x - 2y + y^3}, where y can be solved for first from 9 - 2y^2 + y^4, and this solution can be substituted into 3x - 2y + y^3 to solve for x.

The time and memory required to calculate GB depend very much on the chosen opt argument, and the given variable-ordering in the var_req argument. For further detailed explanation, refer to [162,164]

5.6 Further Explanation

The essence of what the GB technique is about has been explained in a simple manner, without introducing modern commutative algebra. In order to apply the method in designing circuits, that

[10]The default options, opts, are {CoefficientDomain → Rationals, Modulus → 0 ,MonomialOrder → Lexicographic, ParameterVariables → {}, Sort → False} , if opt is ommited. Please refer to [162] for details.

[11]$x \succ y$ does not mean x bigger than y in this case, but it rather means that x to be eliminated before y.

is almost all designers need to know to use the GB. However, many will, undoubtedly, be intrigued to know what is actually happening within the GB-computation, even if it is not required to know this in order to perform GB-computations. Thus, the following should provide some further insight into the GB-computation. Some definitions and amplifications that are helpful follow immediately.

5.6.1 Term-order

The phrase *term-order* merely means that the way variables are ranked or ordered. For example, suppose that x, y and z variables are ordered in a way such that $x \succ y \succ z$, and let α and β be the powers or degrees of the variables. There are three common types of term-orders, and their criteria are listed as follows.

1. Lexicographic(lex) Order,

   In this ordering, a variable dominates the monomials regardless of the degree of the other variables.

   - $x^\alpha \succ y^\alpha$ because $x \succ y$, with the same degrees.
   - $x^\alpha \succ x^\beta$ because $\alpha > \beta$, with the same variables.
   - $x^\beta \succ y^\alpha z^\beta$ because $x \succ y \succ z$ regardless of the total degree of the monomial[12].

   This is called Lexicographic in *Mathematica*

2. Graded Lex Order(glex)

   This ordering first takes into account the total degree of monomials and then orders in an lexicographic way.

   - $x^\alpha \succ x^\beta$ because $\alpha > \beta$, with the same variables.
   - $y^\alpha z^\beta \succ x^\beta$ because $|\alpha + \beta| > |\alpha|$ regardless of the order of the variables, $x \succ y \succ z$.
   - $x^\alpha \succ y^\alpha$ because $x \succ y$ in $x^\alpha \succ y^\alpha$ respectively when the total degree of the variables are equal.

   This is called DegreeLexicographic in *Mathematica*

3. Graded Reverse Lex Order(grevlex)

   This ordering first takes into account the total degree of monomials and then orders in an *inverse* lexicographic way.

[12] a monomial is a product of power of variables, such as x^2yz^3. The sum of all such monomials is a polynomial.

- $x^\alpha \succ x^\beta$ because $\alpha > \beta$, with the same variables. Note that the name of the order, Graded *Reverse* Lex Order.
- $y^\alpha z^\beta \succ x^\alpha$ because $|\alpha+\beta| > |\alpha|$ regardless of the order of the variables, $x \succ y \succ z$.
- $x^\alpha \succ y^\alpha$ because $y^0(\text{in } x^\alpha y^0) \prec y^\alpha$ (in $x^0 y^\alpha$) when the total degree of the variables are equal.

This is referred as DegreeReverseLexicographic in *Mathematica*.

The difference between *glex* and *grevlex* orders in the third criteria is that *glex* looks at the larger variable, x and favors the larger power whereas *grevlex* looks at the smaller variable, y and favors the smaller power.[13]

5.6.2 Buchberger Algorithm

As was explained in Section 5.5, the GB-computation can be easily done using Mathematica. This section gives an overview of the processing taking place in the GB-computation process w.r.t. another term order, namely *Graded Reverse Term Order* or DegreeReverseLexicographic in *Mathematica* as, typically, this order is faster, *but* gives non-minimal output compared with the computation based on lexicographic order discussed in Sections 5.3 and 5.5. Consider the example discussed in Section 5.3.

Rewrite equations (5.1) and (5.2), in *grevlex* order of $x \succ y$, then,

$$f_1 = x^2 + y^2 - 2 \tag{5.1}$$

$$f_2 = xy - 3 \tag{5.2}$$

. Note that the *grevlex* order is the same as the *lex* order in this case.

The *least common multiple* (LCM)[14] of f_1 and f_2 can be found according to $LCM(lt(f_1), lt(f_2)) = x^2y$, where lt is the *leading term*[15].

By running S-polynomial tests on f_1 and f_2, noting that the leading terms for f_1, and f_2, denoted by $lt(f_1)$ and $lt(f_2)$ respectively, are x^2 and xy w.r.t. the *grevlex* order of $x \succ y$, then,

---

[13]The *glex* and *grevlex* are totally different orders although they look 'similar' when their total powers are the same. For examples, $x^3yz \succ_{glex} x^2yz^2$ because the bigger power variable, x appears to have the bigger power. $x^3yz \succ_{grevlex} x^2yz^2$ because the smaller variable, z appears to be a smaller power.

[14]*least common multiple*(LCM) for a set of numbers is the first nonzero common multiple to every number in the set or it is the smallest whole number that is divisible by all the numbers in the set. For example, LCM for 6 and 8 is to find the smallest number that is divisible by 6 and by 8, which is 24

[15]Each separate part of the polynomial that is combined using + and − signs to make up the whole thing is called a term. *Leading term* is the term written in front w.r.t. to the term order.

$$\begin{aligned} S(f_1, f_2) &= \frac{LCM}{lt(f_1)} f_1 - \frac{LCM}{lt(f_2)} f_2 \\ &= \frac{x^2y}{x^2}(x^2 + y^2 - 2) - \frac{x^2y}{xy}(xy - 3) \\ &= y^3 - 2y + 3x \\ &= y^3 + 3x - 2y, \quad \textit{grevlex} \text{ order of } x \succ y \end{aligned} \tag{5.5}$$

The obtained S-polynomial is not divisible by (5.1) and (5.2). Thus, it is added to the original set of f_1 and f_2 to obtain a new set of polynomials, which is,

$$f_1 = x^2 + y^2 - 2 \tag{5.1}$$

$$f_2 = xy - 3 \tag{5.2}$$

$$f_3 = y^3 + 3x - 2y \tag{5.6}$$

This is treated as *the generating set* now. We perform S-polynomial tests on any pair in the set again and check if the result of each pair is divisible by any member in the set, i.e. f_1, f_2 and f_3. As, the remainder of $S(f_1, f_2)$, on division by f_3, in the set is zero, there is no need to perform $S(f_1, f_2)$ again. That is why it was said in Section 5.4 that, *once this S-polynomial is introduced to the basis, the remainder of it, on division by F, will be reduced to zero.*

The S-polynomial of f_1 and f_3 is again obtained as

$$\begin{aligned} S(f_1, f_3) = y^5 - 3x^3 + 2x^2y - 2y^3, \\ \textit{grevlex} \text{ order of } x \succ y. \end{aligned} \tag{5.7}$$

Zero remainder is obtained when (5.7) is divided by f_1, f_2 and f_3. This can be achieved in the following way.

- divide (5.7) by f_3 yields $-3x^3 + 2x^2y - 3xy^2$ remainder.
- divide $-3x^3 + 2x^2y - 3xy^2$ by f_1 yields $2x^2y - 6x$ remainder.
- divide $2x^2y - 6x$ by f_2 yields zero remainder.

Thus, $S(f_1, f_3)$ is ignored.

Repeat the above steps to obtain the S-polynomial of f_2 and f_3

$$S(f_2, f_3) = -3x^2 + 2xy - 3y^2, \qquad (5.8)$$

grevlex order of $x \succ y$.

F divides (5.8), by performing the following actions:

- divide (5.8) by f_1 gives $2xy - 6$ remainder.
- divide $2xy - 6$ by f_2 yields zero remainder.

There is no need to perform the division by f_3 as zero remainder has been obtained, and $S(f_2, f_3)$ again is not added to F.

Therefore, a GB of $f_1 = x^2 + y^2 - 2$ and $f_2 = xy - 3$ is $< x^2 + y^2 - 2,\ xy - 3,\ y^3 + 3x - 2y >$[16] w.r.t. the chosen *grevlex* order of $x \succ y$.

This is a different GB compared with the GBs calculated in Section 5.5 as two different term orders were chosen.

Now compute (5.1) and (5.2) w.r.t. *grevlex* order in *Mathematica*.

```
In[3]:= GroebnerBasis[{x^2+y^2-2,x*y-3},
        {x,y},MonomialOrder->
        DegreeReverseLexicographic]
Out[3]= {-3 + xy, -2 + x^2 + y^2,
         3x - 2y + y^3}
```

This is the same as the results obtained manually.

From the above example, it is clear that the notion behind GB is conceptually no more difficult that many other mathematical algorithms that have been commonly used in engineering. Indeed, it could be argued that the GB use is somewhat analogous to the Gaussian elimination method for solving sets of linear simultaneous equations.

5.7 An Application to the Design of Electrical Circuits

Now consideration is given as to how the GB might be used in a circuit-design situation. The overall scheme, described here, has been used by the authors in a large number of examples of varying complexity.

[16]The symbol of $< \ldots >$ is usually used to denote the *ideal* of the generating set,like $< f_1, \ldots, f_n >$ is the *ideal* generated by polynomials $f_1, \ldots, f_n$. The solution is produced solely to show the steps involved in the Buchberger Algorithm, instead if the minimal output solution

5.7.1 Simple Parallel Circuit

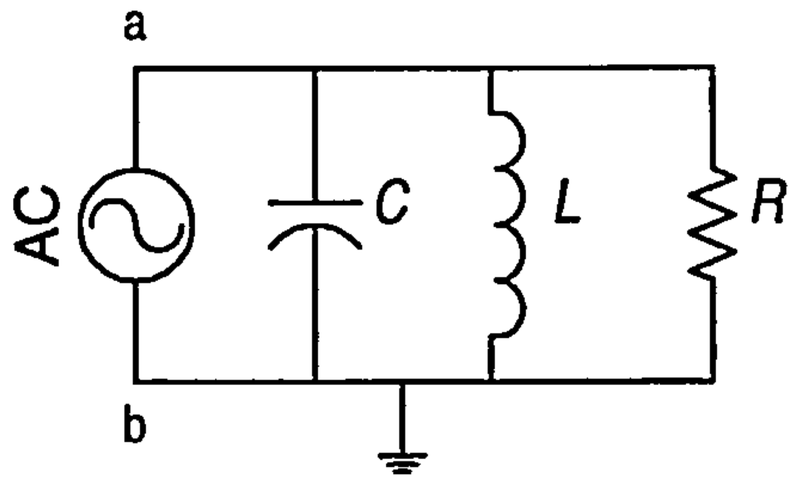

Fig. 5.1: Simple parallel circuit

Fig. 5.1 shows a simple parallel circuit comprising three passive components [147]. The input impedance of the circuit, as seen by the source, at a particular frequency, ω, is

$$Z_{tot} = \frac{a_1\omega^2 + j(b_1\omega^3 + b_2\omega)}{c_1\omega^4 + c_2\omega^2 + c_3} \tag{5.9}$$

where

$$\begin{aligned} a_1 &= L^2R \\ b_1 &= -R^2L^2C \\ b_2 &= R^2L \\ c_1 &= R^2L^2C^2 \\ c_2 &= L^2 - 2R^2LC \\ c_3 &= R^2 \end{aligned}$$

or in transfer-function terms,

$$Z(s) = \frac{\frac{s}{C}}{s^2 + \frac{1}{CR}s + \frac{1}{CL}} \tag{5.10}$$

At resonance, defined here to be the frequency when the circuit impedance acts as a pure resistance, the imaginary part of equation (5.9) is zero. Thus, the input resistance of the circuit, as seen by the voltage source, at the resonant frequency ω is,

$$R_{tot} = \frac{a_1\omega^2}{c_1\omega^4 + c_2\omega^2 + c_3}, \tag{5.11}$$

when,

$$b_1\omega^2 + b_2 = 0 \tag{5.12}$$

The analysis shows that the circuit can either have two real poles or a pair of complex conjugate poles. Only the latter situation can produce resonant-like conditions. The analysis also shows that there are five variables, i.e. ω, R_L, R_{tot}, C_p and L_p. By specifying any, or some of these values, the rest can be found, by using the GB approach as follows.

With the two basic equations, i.e. (5.11) and (5.12), the GB can be used to find the unknowns by the following syntax: GroebnerBasis[{(5.11),(5.12)},{var_req}]

```
In[4]:= GroebnerBasis[{-(L^2*R*w^2) + Rtot*
         (R^2 + (L^2 - 2*C*L*R^2)*w^2 +
         C^2*L^2*R^2*w^4),
         L*R^2*w - C*L^2*R^2*w^3},
         {L,C,R,Rtot}]
Out[4]= {R^5*Rtot - R^4*Rtot^2*w,
         L*R^3*w - L*R^2*Rtot*w^2,
         L*R^4*Rtot - L*R^2*Rtot^3*w^2,
         -(R^4*Rtot) + C*L*R^2*Rtot^3*w^4,
        -(R^2*Rtot) + L^2*R*w -
           L^2*Rtot*w^2 +
           C*L*R^2*Rtot*w^2,
        -(L*R^2*w) + C*R^3*Rtot*w^2 +
           C*R^2*Rtot^2*w^3 +
           C*L^2*Rtot^2*w^5 -
           2*C^2*L*R^2*Rtot^2*w^5}
```

It can be seen that the GB of the generating set, (5.11) and (5.12) is given in a triangular form, where the polynomial in the first row is a function of R_L, R_{tot} and ω, both the second and third row are functions of R_L, R_{tot}, ω and L_p, and the next ones down have more variables and so forth. From the third polynomial, `L*R^4*Rtot - L*R^2*Rtot^3*w^2`, two of the variables may be chosen, which then enables the rest to be found, by the back-substituting technique to establish the rest of the parameters. Note that if the opt is not specified, then default opt is used.

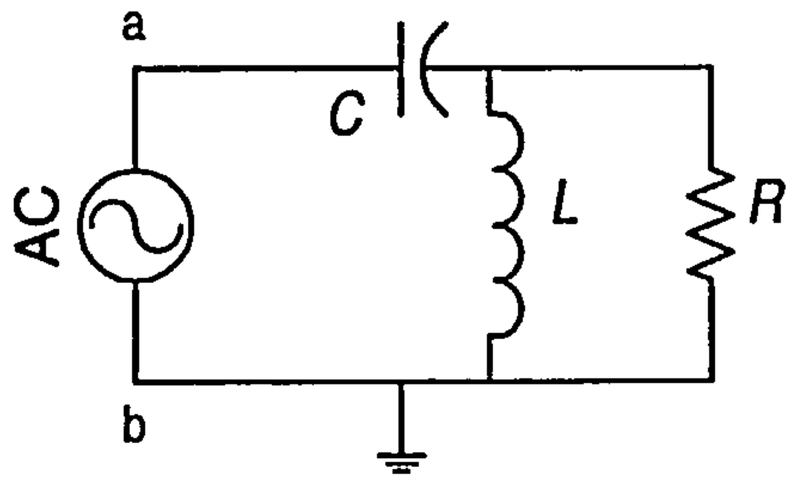

Fig. 5.2: Series-parallel circuit

5.7.2 Series–parallel Circuits

Fig. 5.2 shows a series-parallel circuit comprising two passive components [165]. The input impedance of the circuit can be found as

$$Z_{tot} = \frac{\tilde{a_1}\omega^3 + j(\tilde{b_1}\omega^2 + \tilde{b_2})}{(\tilde{c_1}\omega^3 + \tilde{c_2}\omega)} \tag{5.13}$$

where

$$\begin{aligned} \tilde{a_1} &= RL^2C \\ \tilde{b_1} &= R^2LC - L^2 \\ \tilde{b_2} &= R^2 \\ \tilde{c_1} &= L^2C \\ \tilde{c_2} &= R^2C \end{aligned}$$

or

$$\begin{aligned} Z(s) &= \frac{1}{sC} + \frac{sRL}{sL+R} \\ &= \frac{R(s^2 + \frac{1}{RC}s + \frac{1}{LC})}{s(s+\frac{R}{L})} \end{aligned} \tag{5.14}$$

At resonance, the input resistance is

$$R_{tot} = \frac{\tilde{a_1}w^3}{\tilde{c_1}w^3 + \tilde{c_2}w} \tag{5.15}$$

and

$$\tilde{b_1}w^2 + \tilde{b_2} = 0 \tag{5.16}$$

On solving these two equations, i.e. (5.15) and (5.16), the following GB for the generating set w.r.t. the chosen term-order is obtained,

```
In[5]:= GroebnerBasis[
        {Rtot*(w^3*L^2*C + w*R^2*C) -
              w^3*R*L^2*C,
        w^2*R^2*L*C - w^2*L^2+R^2},
        {Rtot,C,R,w,L},
        CoefficientDomain ->
        RationalFunctions]
Out[5]= {R^2 - L^2*w^2 + C*L*R^2*w^2,
       R^4*Rtot - L^2*R^3*w^2 +
             L^4*R*w^4 - L^4*Rtot*w^4,
        -(R^2*Rtot) + L^2*Rtot*w^2 -
             C*L^3*R*w^4 +
             C*L^3*Rtot*w^4,
        C*R^2*Rtot*w - C*L^2*R*w^3 +
             C*L^2*Rtot*w^3}
```

This produces slightly more complicated results than the example in Subsection 5.7.1. From this set of GB, three variables need to be parameterized to get the rest. This is shown in the first row of the polynomial, i.e. `R^2 - L^2*w^2 + C*L*R^2*w^2`, which is a function of R, L, C and ω. The number of variables that need to be parameterized is restrained by the circuit characteristics.

To get the variables in order to achieve the most efficient computation and simplest results within the limitations, there exists a `Sort` option that sorts the variables to improve the efficiency for the lex ordering process.

Using the circuit in section 5.7.2, as an example, there are five variables, and assigning them to `vars` leads to the following;

`In[6]:= vars={Rtot,L,C,R,w};`, The polynomials were called `polys`, i.e.

```
In[7]:= polys = {Rtot*(w^3*L^2*C+w*R^2*C)
                      -w^3*R*L^2*C,
                w^2*R^2*L*C-w^2*L^2+R^2};
```

Then perform the following,

```
In[8]:= MonomialList[polys, vars, Sort->True]
```

The output is given by

```
Out[8]= {{C*R^2*Rtot*w,
         C*L^2*Rtot*w^3,
         -(C*L^2*R*w^3)},
         {C*L*R^2*w^2,
         R^2,
         -(L^2*w^2)}}
```

Thus, the variable ordering is $C \succ L \succ R \succ\succ R_{tot} \succ \omega$.

This way of sorting the order of variables can be useful in problems that comprise many variables.

5.8 Application of the GB techniques to Load-resonant Converter Circuits

So far, an introduction to the GB has been given together with an explanation of how it may be used in the mathematical programming package, *Mathematica*. Using these techniques and tools, two simple examples of resonant circuits have been solved as illustrations of the power of the method. However, as mentioned earlier, the main purpose of the GB technique, so far as this thesis is concerned, is to apply it to the series-parallel load-resonant converter in order to achieve a required specification. This could not be done, in general, using the solving-simultaneous-equations method [3–6]. Thus, the following sections are focused on the GB technique in load-resonant converter applications.

5.8.1 New Concept of Load-resonant Power Control

A new way of controlling the output-power of the load-resonant converter was made possible because of the realization of different current-levels of operation at each distinct resonant frequency. A single value of referred load resistance, R_L is transformed by the circuit to give a different total input circuit resistance, R_{tot} at each resonance. This enables the power delivered to the circuit, and hence to the load, from a fixed dc supply voltage, to vary depending on the resonant frequency at which the circuit is being excited. This is the basis of controlling the output power of load-resonant converters reported in [5, 6, 148, 166].

Although it provides substantial changes in the output power level, the method actually exhibits a major problem, which is that the power level can be pre-specified at one resonant frequency only. Thereafter the output-current can be prescribed at any operating frequency as it depends on the circuit values that have now been decided upon.

In order to overcome this severe shortcoming, a revised analysis has been carried out on those reported in the literature [5, 6, 148]. The power delivered to the circuit at each of these resonant frequencies is related to the supply voltage and the resistance of the circuit, R_{tot} at the particular frequency. Given a dc supply, V_{dc} to the resonant converter of Fig. 4.6, a square-wave voltage is derived from this, and is applied to the resonant circuit that has fundamental voltage component of RMS value equal to,

$$V_{rms} = V_{dc}\frac{2}{\pi}\frac{1}{\sqrt{2}} \tag{5.17}$$

Contributions by the harmonics have been discussed in detail in [5, 6, 148], and these can be neglected in the present analysis.

The power delivered to the circuit by the inverter at a resonant frequency is,

$$P = \frac{V_{rms}^2}{R_{tot}} \tag{5.18}$$

where R_{tot} can take on a finite number of different values depending on the resonant frequencies of the inverter. These different values of R_{tot}'s imply different values of power delivered to the circuit. Therefore the main aim of controlling the output power is to be able to specify the value of the input resistance at each resonant frequency, i.e. R_{tot}. Major changes in output power can then be controlled by switching among these resonant frequencies.

The relationship between the resistance at the corresponding frequencies and the load-leg resistance is given by Eqn. (4.2).

5.8.2 Design Methodology

The design methodology described [5,148] for establishing component values is, essentially, a trial-and-error process, albeit computer assisted. Even with experience, it is not a process to be lightly undertaken if new topologies are involved. These comments can be appreciated after even a preliminary reading of [5, 148].

In the design methodology advocated here, essentially just two basic properties of the resonant

converter desired need to be established at the resonant frequencies. These are the imaginary part of Eqn. (4.3) written as Eqn.(4.5) and the equation for the input resistance from Eqn.(4.6) of the total input impedance of the converters. This is shown in detail in Section 5.7. However, in practice, resonant converter circuits are rather more complex than the two simple examples described earlier [165]. Owing to the larger numbers of passive components and circuit legs involved, the GB process has to be performed more than once depending on the complexity of the topology. This enables the component values to be obtained consecutively by back-substituting the obtained parameter values in a more efficient, quicker and systematic way.

In fact, the computation time involved is no way approaches those reported in [5, 148] even though more components are involved in the new calculation, with an additional inclusion of R_{tot_b} at $75kHz$. The complication of the older design processes is made even more serious when various R_{tot} values are to be considered. This can be seen from the tedious mathematics, of even just one value of R_{tot}, reported in [3, 4].

5.9 Practical Circuits

5.9.1 Design based on Welding Power Converter

In [3, 6], the design, building and testing of a resonant converter for use in electrical welding equipment was described. The various operating parameters, i.e. component values, are shown in Table 5.1, and the circuit diagram is shown in Fig. 4.6.

In this design, the welding-arc resistance was the load of the converter; the model of the arc was taken to be a voltage drop plus a resistor in series. Such arcs are believed to exhibit very low inductances. The original data, on arc conditions, was taken from [Cook and Merrick, 1975]. The high-power mode of the input power to the circuit was limited to 5kW, and an input power of 1kW was chosen for the low-power mode. Since the arc is the only dissipator, theoretically all the input power is absorbed by the arc.

The above calculated component values were obtained using only the value of R_{tot} in the high-power mode. In order to achieve the desired power-change ratio of 1:5 at 75kHz : 100kHz, both values of R_{tot}, i.e. $72.9\Omega : 15.6\Omega$ have to be satisfied, and hence the original design procedure was run iteratively, until both values of R_{tot} were practically satisfied.

The design has been repeated using the GB approach, which allows both of the R_{tot} values to be specified directly. From equations (4.5) and (4.6), the GB processing can be performed, and the

Welding Power Supply: Operating Parameters
Maximum Input peak-to-peak Voltage $= 600V$,
Referred load resistance, corrected for ac analysis, $R_L = 18.6\Omega$
Resonant frequencies of the circuit, 100kHz, 75kHz and 50kHz
Total circuit resistance at 100kHz, $R_{tot} = 15.6\Omega$
Total circuit resistance at 75 kHz, $R_{tot} = 72.9\Omega$
Load leg inductance, including leakage inductance of the transformer, $L_L = 80\mu H$
Component values calculated by design programme
$C_s = 45nF, L_s = 135\mu H, C_p = 45nF, L_p = 14\mu H$

Table 5.1: Specified operating parameters and calculated component values for welding power supply

various stages used in the calculative procedure are laid out as follows.

```
In[1]:=
GroebnerBasis[{Rtot*(Rl^2 + (Xl+Xp)^2) -
                  Rl*Xp^2,
               Xs*Rl^2 + Xs*Xl^2 +
                  2*Xs*Xp*Xl + Xs*Xp^2 +
                  Xp*Xl^2 + Xp^2*Xl +
                  Xp*Rl^2},
{Xl,Xp,Rl},{Xs},CoefficientDomain ->
RationalFunctions]


Out[1] = {Rl^2*Rtot + Rtot*Xl^2 +
2*Rtot*Xl*Xp - Rl*Xp^2 + Rtot*Xp^2}
```

As there is a second R_{tot} to be specified, (4.5) and (4.6) can be redefined at another resonant

frequency, such as ω_2 to give,

$$b_1\omega_2^6 + b_2\omega_2^4 + b_3\omega_2^2 + b_4 = 0, \tag{5.19}$$

$$R_{totb} = \frac{a_1\omega_2^5 + a_2\omega_2^3 + a_3\omega_2}{c_1\omega_2^5 + c_2\omega_2^3 + c_3\omega_2} \tag{5.20}$$

The GB process is then performed on (5.19) and (5.20) again, to yield,

```
Out[2] = {Rl^2*Rtotb + Rtotb*Xl^2 +

2*Rtotb*Xl*Xp - Rl*Xp^2 + Rtotb*Xp^2}
```

In order to eliminate the referred load resistance, R_L, The GB process is performed on both of the outputs obtained above, i.e.,

```
In[3]:=
GroebnerBasis[{Rl^2*Rtot + Rtot*Xl^2 +
                    2*Rtot*Xl*Xp - Rl*Xp^2 +
                    Rtot*Xp^2,
               Rl^2*Rtotb + Rtotb*Xlb^2 +
                    2*Rtotb*Xlb*Xpb -
                    Rl*Xpb^2 + Rtotb*Xpb^2},
{Xl,Xlb,Xp,Xpb},{Rl},CoefficientDomain ->
RationalFunctions]
```

The output is a function of the input resonant resistances, R_{tot} and R_{tot_b}, reactances in the parallel leg, X_p and X_{p_b} and of the reactances in the load leg, X_L and X_{L_b} at frequencies, ω_0 and ω_2, respectively.

The resonant frequencies, ω_0 and ω_2, and the input resistances at these two frequencies, R_{tot} and R_{tot_b} are required to be pre-specified. Three out of four of the component values, C_L, C_p, L_L and C_L are to be parameterized to get the fourth value. This then leads to the finding of R_L. In order to find the passive components on the series leg, The GB process has to be performed once again on (4.5) and (4.6) to eliminate L_s, for example. Hence, this gives an output as a function of ω_0, R_{tot}, L_p, C_p, R_L and C_s. C_s can then be obtained by knowing the other values.

Thus, a complete set of design details have been obtained. These consists of the three resonant frequencies, ω_0, ω_1 and ω_2, six passive components, two in each of the three legs, two input

resistances, R_{tot} and R_{tot_b} at two different resonant frequencies and the referred load resistance, R_L.

By specifying the ω_0, ω_1, ω_2, R_{tot}, R_{tot_b}, C_p, L_p and L_L, the rest of the components, C_L, R_L, L_s and C_s can be found consecutively to give the desired performance of the converter.

Using the same values as in Table 5.1, the component values were recalculated as follows. It is reported in [5], that by leaving out the calculated value of C_L, which was large, the effect was minimal. However, in this new calculation, this component was taken into account, i.e. $1.47\mu C$, and proceeded. The calculation of the referred load resistance, R_L, was obtained as 21.7Ω. This is larger than the value obtained in the Table 5.1. However, it could be readjusted to obtain the arc resistance of around 0.125Ω by using a transformer with a turn-ratio of 12:1, instead of 11:1 as used before, if this were felt to be worthwide in practice.

The results obtained for the series leg inductance and capacitance were $137\mu H$ and $55nF$ respectively. The component values vary slightly from the original design shown in Table 5.1

The frequency response is plotted as Fig. 5.3 [165].

It is shown that the power change is only $3:1$ at $93kHz:75kHz$, which is not as good as the original design, and the corresponding input resonant resistances are $26.7\Omega:72.9\Omega$. It is noted that in the new calculation, comparing with the old one, the upper resonant frequency has dropped from $100kHz$ to $93kHz$, where the other two are the same as the old ones, i.e. $75kHz$ and $50kHz$. This is probably the major factor causing the discrepancy between the new and old calculations. Other possible reasons are different order of the design procedure being written, or different orders of the component values being calculated with different pre-specified component values, where in the new calculations, L_L, L_p and C_p are prespecified besides the three turning point frequencies and two R_{tot} values as stated in Table 5.1. These then contribute to the differences in subsequent component values. It is possible to match the two calculations more closely, but the present calculation is convenient for the purpose of illustrating the inclusion of the second R_{tot} in the design procedure. Furthermore, the flexibility of the GB-based design method is illustrated more fully and interestingly in the following.

5.9.2 Flexible Changes in Original Power-converter Design

A design, utilizing the same topology, using the GB approach but this time specifying the turning-point frequencies as $60kHz$, $85kHz$ and $110kHz$ respectively, is shown in Fig. 5.4 [165]. The two R_{tot} values were prespecified as 116Ω(at $85kHz$) and 6Ω(at $110kHz$). This then gives a

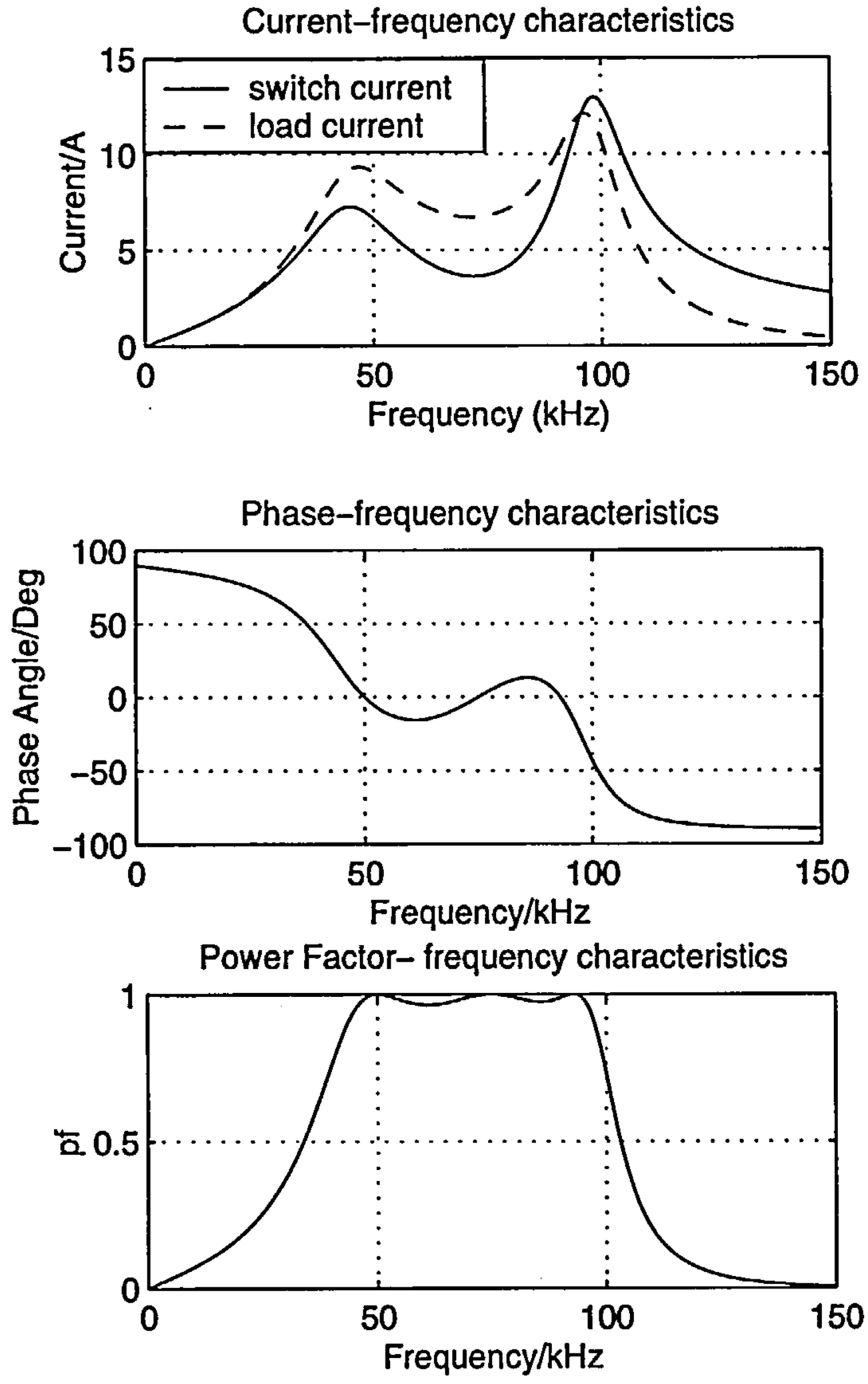

Fig. 5.3: Original frequency response of the resonant converter for welding power supply $L_s = 137\mu H$, $L_L = 80\mu H$, $L_p = 14\mu H$,$C_s = 0.055\mu F$, $C_L = 1.47\mu F$, $C_p = 0.045\mu F$ and $R_L = 21.7\Omega$

maximum-to-minimum power-level-ratio of $(45.3/2.3) = 19.5$, from Fig. 5.4. The three prespecified components are L_L, L_p and C_p. Note that, the power-factor varies between 1 and 0.55 across the frequency range of interest. It is possible to make the design have a better power-factor performance but the present design is convenient for illustrative purposes.

These two designs have shown the advantages of using the GB approach in controlling the output power change of the resonant converter in a much more efficient, effective, systematic and less-time consuming manner.

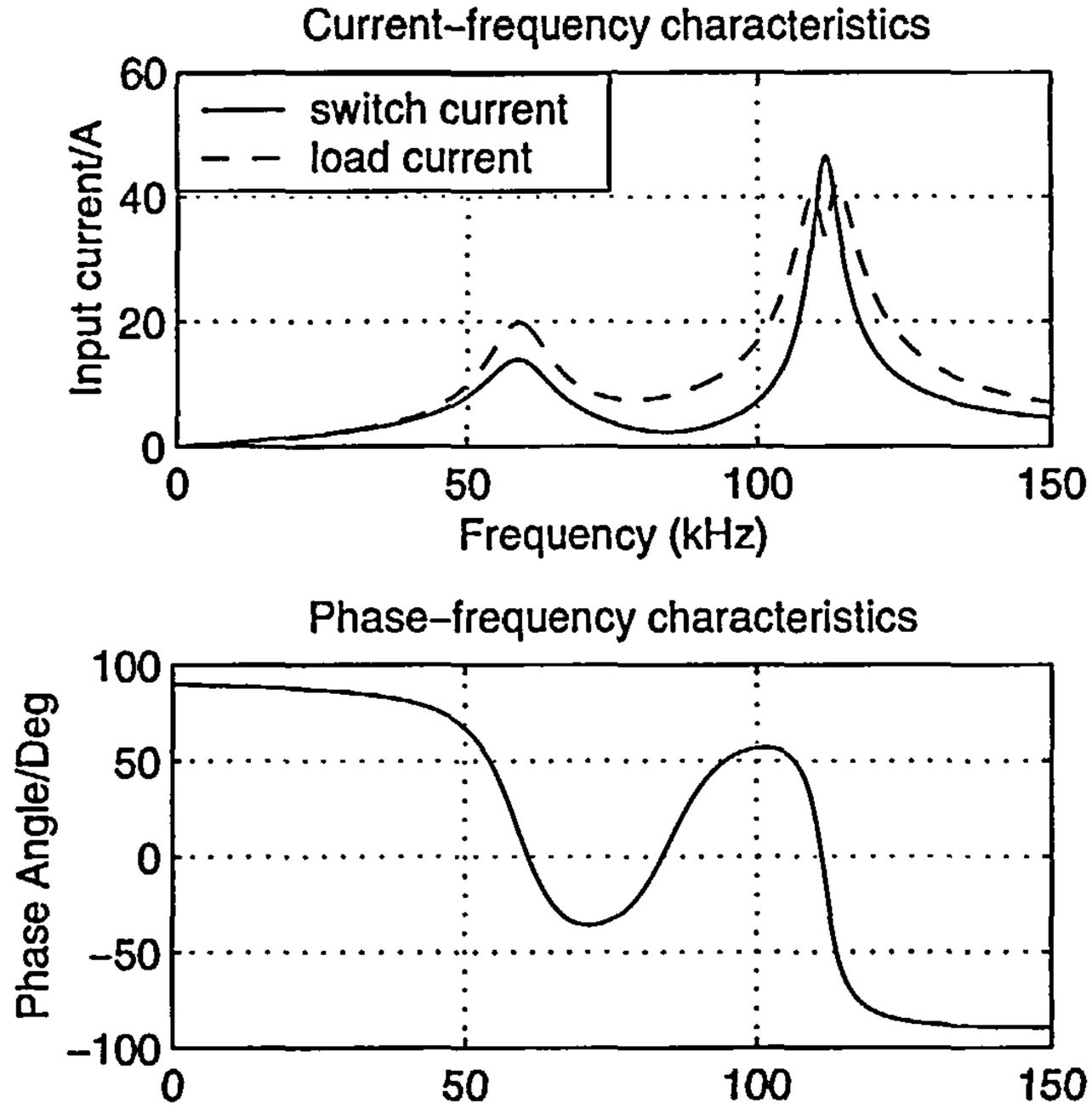

Fig. 5.4: Modified frequency response of resonant converter for welding power supply
$L_s = 100\mu H$, $L_L = 80\mu H$, $L_p = 14\mu H$,$C_s = 0.045\mu F$, $C_L = 0.2\mu F$, $C_p = 0.045\mu F$ and $R_L = 10\Omega$

5.10 Conclusion

In this chapter of the thesis, an introduction to the GB is given together with an explanation of how it may be used in the mathematical programming package, *Mathematica.* Using these techniques and tools, two simple examples of resonant circuits have been solved as illustrations of the procedures and power of the method.

This was then followed by the detail examination of the GB approach to designing resonant-converter circuits. It has illustrated the advantages of this method over previous ones. Among these advantages are speed of calculation, closer specification of more critical parameters, ease of application and the establishment of a systematic procedure. Examples have been given to illustrate

the efficiency and the flexibility of the method.

Although the examples, have been confined to resonant circuits, the approach has general applications in circuit analysis.

Chapter 6

Hardware Techniques for Quasi-resonant Power Control

6.1 Introduction

Previous chapters of this thesis have been focused on *series-parallel load-resonant converter circuits.*

This chapter describes a promising way of controlling the output power of a *quasi-resonant converter* using new and simple hardware techniques. As mentioned in Chapter 3, the quasi-resonant converter is a type of switch-resonant converter placing the resonant components around the power switches. The duty ratio of the switch is determined by the period of the resonant cycle [45, 55], unless an additional commutation switch is used.

The techniques investigated here, have in mind, the possible application of the speed-control of a single-phase induction-motor-driven domestic fan. This work, for controlling the output power of the converter, and hence the speed variation of the induction motor, was essentially , a feasibility [121].

Almost since the time the induction motor was invented, efforts have been spent in devising and developing methods for controlling its speed; these methods have ranged from the pole-amplitude-modulation thyristor controls [Murphy, 1973,Cattermole and Davis, 1975] to the modern techniques like fuzzy logic, sliding mode and other control methods [Fonseca et al., 1999,Hren and Jezernik, 1998]. Moreover, ways have been developed to eliminate speed sensors in such applications. These methods can generally be classified as *closed-loop sensor-less speed control*, where motor speed is estimated from other measurable quantities such as stator voltage and current, and, *open-loop speed control with slip compensation.* In this latter method, motor speed is controlled by compensating

for the change of effect of load torque on the motor shaft [Cattermole and Davis, 1975]. There appears to be no shortage of novel ideas in this area. However, resonant switching techniques in controlling induction motors are rare compared with the traditional hard-switching techniques. Nonetheless, there is a rise in the number of soft-switching applications for induction drive systems. The reasons are, like various advantages of employing soft-switching techniques, the production of fast-switching semiconductor devices, and the availability of digital signal processing tools.

The control techniques employed in the research work described are based on quite-simple and novel control techniques using simple power-electronic circuitry. A brief introduction to the induction motor effectively paraphrasing [167,168] is presented before spelling out the techniques used in the variable-speed control of the drive. *Variable-speed drive* is defined here as a motor in which speed can be continuously varied over a specified range, together with the associated equipment employed.

6.2 Operational Principle of Single-phase Induction Motor

6.2.1 Why Single-phase Induction Motor?

There exists a high demand for fractional horse-power motors, mainly for domestic applications, where only a single-phase ac supply is normally available, and also for industrial applications requiring low-power, low-cost and high-efficiency operations. The single-phase induction motor is a popular choice due to its robustness, reliability, low-maintenance requirements and low-manufacturing cost.

6.2.2 Basic Concept

A single-phase induction motor has only one main winding on the stator as shown in Fig. 6.1 [167]. The main winding comprises a number of concentric coils This is different from the three-phase induction motor which has a a stator winding consisting of three identical bands of coils displaced from each other by 120 electrical degrees.

The air-gap mmf waveform produced by a cylindrical-rotor machine having an N-turn coil and carrying current i is given by

$$F(\theta) = \frac{2iN}{\pi}[cos(\theta) - \frac{1}{3}cos(3\theta) + \frac{1}{5}cos(5\theta) - \frac{1}{7}cos(7\theta)\cdots], \tag{6.1}$$

where θ is in angular position around the machine circumference, measured w.r.t. some convenient

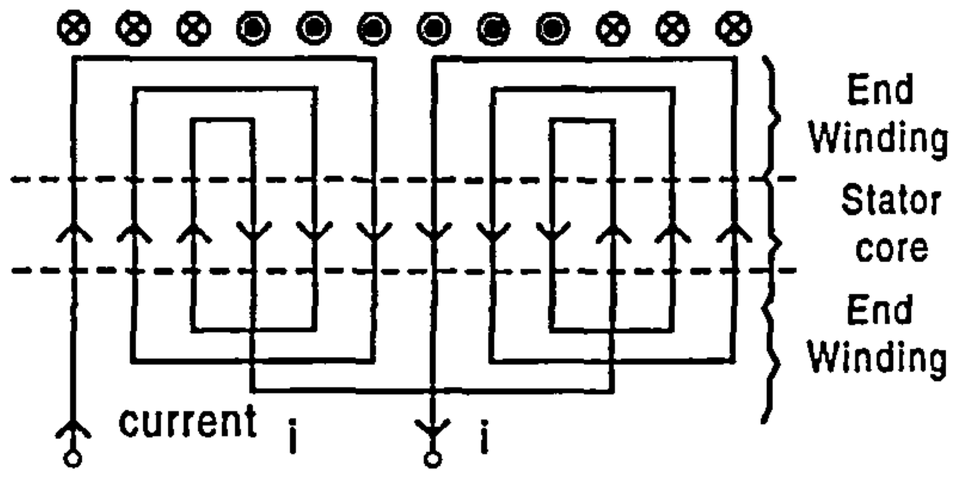

Fig. 6.1: 2-pole, 12-slot concentric winding

datum about which the mmf distribution is even, shown in Fig. 6.2 [167]. Considering only the fundamental component in the above, the fundamental of Eqn.(6.1) approximates to,

$$F = \frac{2iN}{\pi} cos\theta \tag{6.2}$$

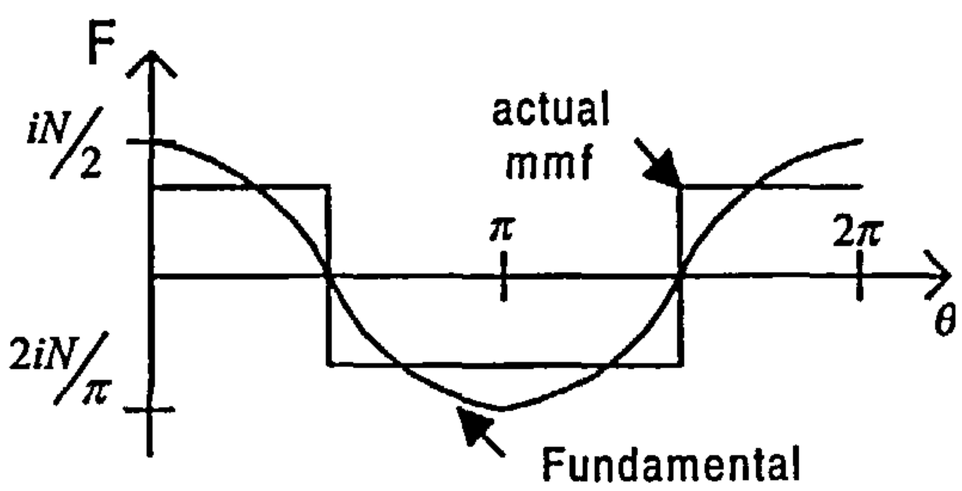

Fig. 6.2: Waveforms of actual and fundamental MMF

When the machine is connected to a single-phase ac-supply producing current, $i = \hat{I}cos(\omega t)$, then Eqn. (6.2) becomes

$$\begin{aligned} F &= \frac{2\hat{I}N}{\pi} cos(\omega t) cos\theta \\ &= \frac{\hat{I}N}{\pi}[cos(\omega t - \theta) + cos(\omega t + \theta)] \\ &= \hat{F}cos(\omega t - \theta) + \hat{F}cos(\omega t + \theta) \end{aligned} \tag{6.3}$$

where,

the peak value of mmf, F, which is, $\hat{F} = \frac{2\hat{I}N}{\pi}$, and,

$\hat{F}cos(\omega t - \theta)$represents a forward-rotating mmf wave, and,

$\hat{F}cos(\omega t + \theta)$represents a backward-rotating mmf wave.

Thus, the pulsating stationary flux can be regarded as two equal-amplitude traveling waves rotating at synchronous speed, ω_s, and the other with synchronous speed, $-\omega_s$. That is there are two equi-amplitude, forward and backward traveling waves in the air-gap.

The accompanying magnetic flux penetrates the rotor, inducing an emf in the winding. If the rotor is stationary, then no net torque, owing to the interaction of the stator field and rotor field, is produced.

However, if the rotor is turning, then the frequency of the induced emfs (and current) arising from the two mmf-traveling waves will differ. The relative frequency of these emfs is sf for the forward-rotating field, and $(2-s)f$ for the backwards-rotating field, where s is the slip.

In order to reduce the *slip speed*, i.e. the relative speed between the rotating flux and the stationary rotor coils, the rotor runs in the same direction as that of the flux. It reaches a rotating speed, ω_r, which is less than the synchronous speed, ω_s of the rotating flux. Note that, if $\omega_r = \omega_s$, there would be no induced voltage in the rotor, and hence no torque.

If the rotor is turning at speed, ω_r in the forward direction, its *slip speed* w.r.t the forward rotating field is,

$$\begin{aligned} s_f &= \frac{\omega_s - \omega_r}{\omega_s} \\ &= 1 - \frac{\omega_r}{\omega_s}, \end{aligned} \tag{6.4}$$

whereas in the backward direction, the backward rotating field has a synchronous speed of $-\omega_s$, and the rotor slip w.r.t the backward-rotating field is

$$\begin{aligned} s_b &= \frac{\omega_s + \omega_r}{\omega_s} \\ &= 1 + \frac{\omega_r}{\omega_s} \end{aligned} \tag{6.5}$$

The impedance caused by the two emfs is different except when the rotor is at standstill, i.e. $s = 1$. Only at this speed, as the two rotor emfs have the same frequency, i.e. the supply frequency, f. The forwards-branch and backwards-branch impedances, in complex form, are

$$\begin{aligned} \bar{Z}_f &= (\frac{R_2'}{s} + jX_2')//jX_{m_f} \\ \bar{Z}_b &= (\frac{R_2'}{s} + jX_2')//jX_{m_b} \end{aligned} \tag{6.6}$$

respectively where X_{m_b} is the magnetising reactance induced by backward rotary field, X_{m_f} is the magnetising reactance induced by forward rotary field, R_2' is the rotor resistance referred to

the stator and X_2' is the rotor leakage reactance referred to the stator. These are added to each magnetising reactance as shown in Fig. 6.3, where $\bar{V}$ is the complex voltage [167].

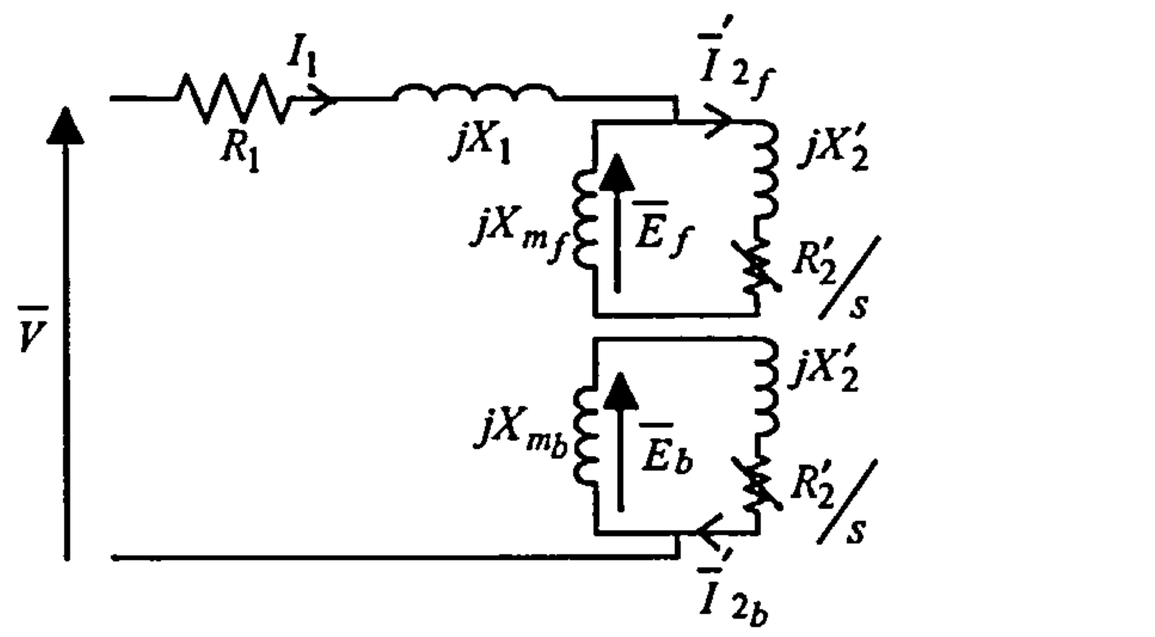

Fig. 6.3: Equivalent circuit with rotor quantities referred to the stator

The power loss in the forward branch is proportional to the forward-acting torque, and that in the backwards branch to the backwards-acting torque. They are given as

$$\begin{aligned} T_f &= \frac{1}{\omega_s}|\bar{I}_1|^2 Re[\bar{Z}_f] \\ T_b &= \frac{1}{\omega_s}|\bar{I}_1|^2 Re[\bar{Z}_b], \end{aligned} \tag{6.7}$$

where the complex current or phasor, $\bar{I} = Ie^{j\phi}$, and I is the rms value whereas ϕ is the current phase angle measured from the complex voltage phasor.

The resultant torque on the rotor is the algebraic sum of the forwards and backwards torques. These are illustrated in Fig. 6.4 [167].

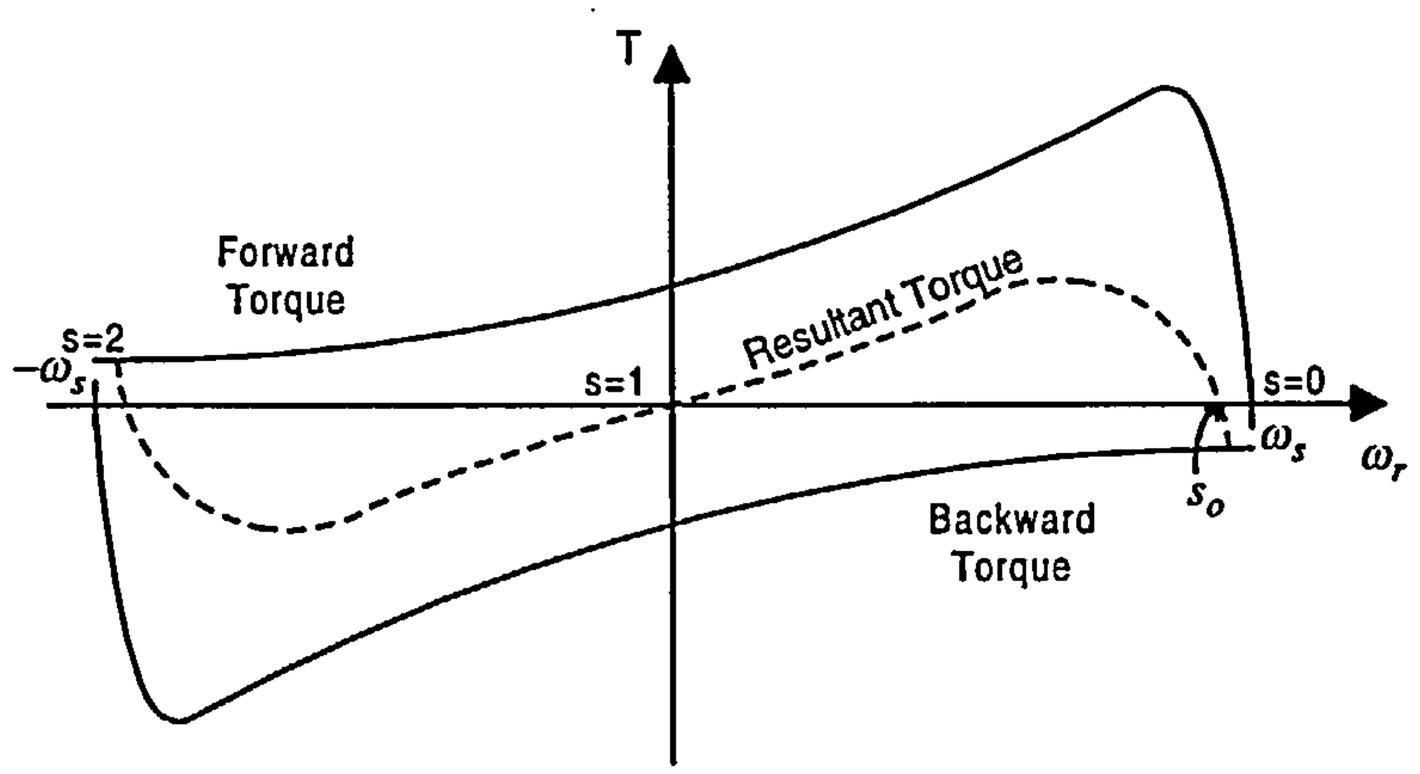

Fig. 6.4: Torque vs. Frequency characteristics

From the figure, it is clear that the resultant torque is zero at standstill, i.e. *no starting torque*, but once started in either direction, a net torque is produced to accelerate the rotor up to normal

speed in that direction. In addition, there is a *finite negative torque* at synchronous speed, so that running light, i.e. $T = 0$, will occur at some speed less that the synchronous speed.

It has to be mentioned that the total sinusoidal field in the air-gap does not rotate as in the three-phase motor, but pulsates at twice the line frequency due to the interaction between the backwards and forwards-rotating fields. This pulsating torque contributes significantly to the noise produced by single-phase machines.

By equating the backwards and forwards torques, when the motor 'runs light' (refer to Fig. 6.4),

$$s_0 = 1 \pm \sqrt{1 - [\frac{R_2'}{X_m + X_2'}]^2}, \tag{6.8}$$

because $Re[\bar{Z}_f] = Re[\bar{Z}_b]$ as the torques are proportional to the power losses in the forwards and backwards branches.

Eqn. (6.8) reveals that there is a running-light speed in each of the forwards and backwards directions, and the motor does not run even if it is given a start in either direction when $R_2' > X_m + X_2'$. Therefore steps should be taken to ensure that, at least, $X_m + X_2'$ is bigger than R_2'.

6.2.3 Starting

In order to provide a unidirectional starting torque to the single-phase induction motor from stand-still, an additional winding is wound on the stator with a spatial displacement of ϕ from the main winding. The current in the 'starter' coil, i.e. the second winding, also has to have a suitable time-phase displacement, ψ from that in the main winding. This would allow the motor to have either a dominant forwards or backwards rotating field depending on the angles ψ and ϕ. This dominant field then provides the motor with the starting torque in a known direction. The maximum starting torque is obtained when both $\psi = \phi = \pm 90$.

Examples of motors that have starting torque are split-phase motors, capacitor-start motors, capacitor-run motors and shaded-pole motors.

6.3 Classical Methods of Speed Control

Speed control of induction motors is obviously desirable, and numerous modern and powerful methods of obtaining stepped-speed or continuous-speed change have evolved, as mentioned earlier. Among these methods are the following;

6.3.1 Variation of Rotor-circuit Resistance

In this case, speed variation is obtained by controlling the impedance ratio,i.e.

$$[\frac{R_2'}{X_m + X_2'}]^2 \tag{6.9}$$

Equation (6.8) also shows that if the impedance ratio is varied, the slip can be changed accordingly.

In addition, by manipulating equations (6.6) and (6.7) further, a relationship between the acting torque and slip can be obtained, e.g.,

$$\begin{aligned} T &\propto Re[\bar{Z}_f] \\ &\propto \frac{\frac{R_2' X_m^2}{s(X_2'+X_m)}}{1+\frac{R_2^2}{s^2(X_2'+X_m)^2}}. \end{aligned} \tag{6.10}$$

The slip at which breakdown torque occurs can also be determined by differentiating Eqn. (6.10) w.r.t. the slip, and the resulting equation is equated to zero, i.e. $\frac{dT}{ds} = 0$ to show the maximum torque.

A family of speed-torque curves for various values of rotor-circuit resistance is given in Fig. 6.5 [168]. T_{loss} and T_L in the figure represent the torque due to rotational loss and the load torque at motor shaft coupling respectively. If the rotor-circuit resistance is made sufficiently large, the

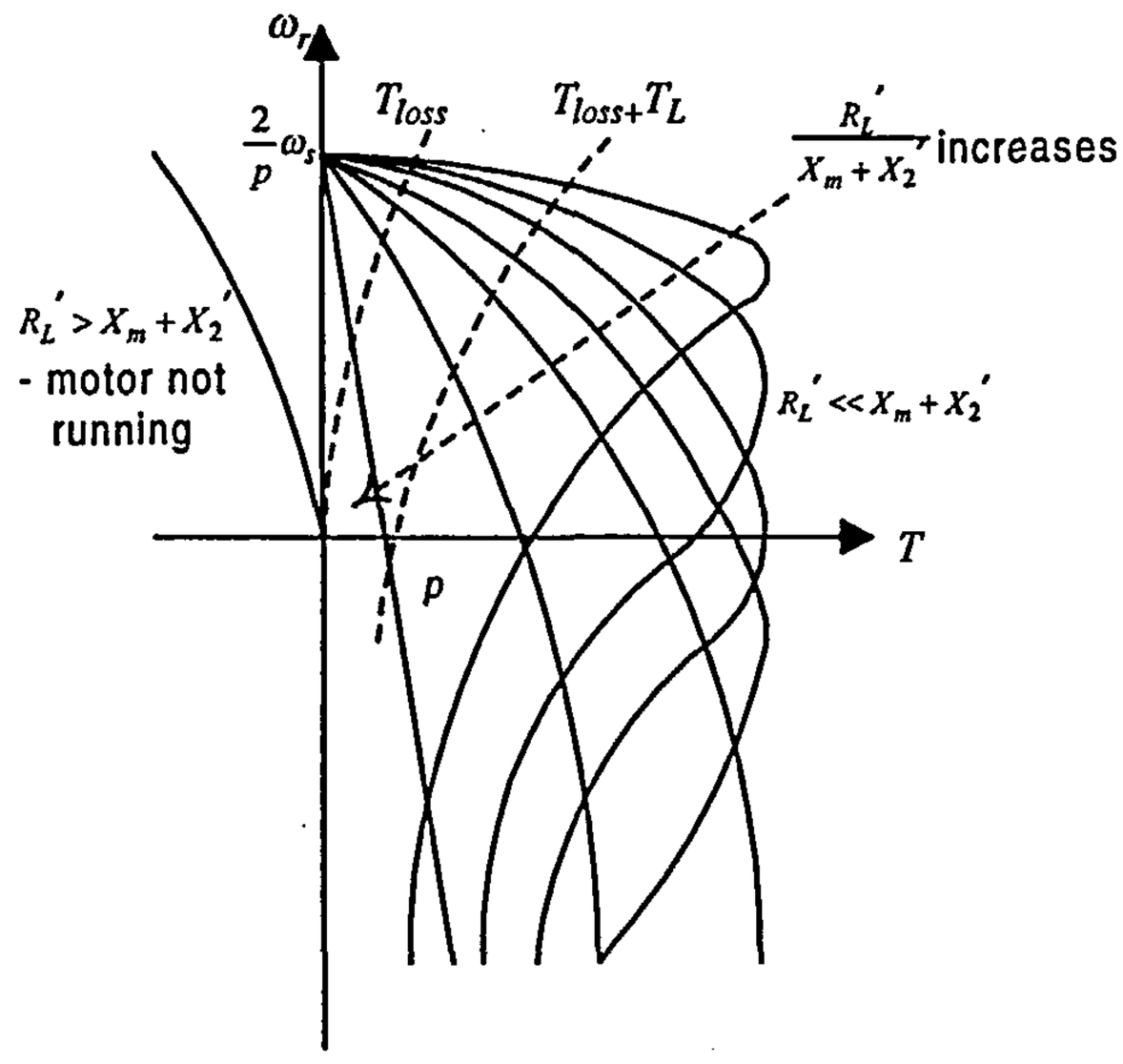

Fig. 6.5: Variation of speed-torque curves for different values of impedance ratio

load may drive the motor backward at an operating point such as p in Fig. 6.5 [168]. At this point, the motor torque is opposing rotation in the desired direction.

If the slip becomes negative in Eqn. (6.10), that is, if the motor is driven at more than synchronous speed, e.g. by a vehicle going down hill, the developed torque becomes negative, and regenerative braking is obtained, where the energy is fed back into the ac supply system.

It should be noted that on no-load, effective speed-control of an induction motor is not obtained because the speed approaches the synchronous speed. It is independent of resistance at no load.

6.3.2 Variable-terminal Current or Voltage

Equation (6.7) shows that the developed torque is proportional to the square of the applied terminal complex-current. Thus, speed control of a loaded motor can be achieved by varying the terminal current or voltage, where the two quantities change proportionally. An externally fixed rotor resistance is usually used in the rotor circuit. The speed-torque curves are shown in Fig. 6.6 [168].

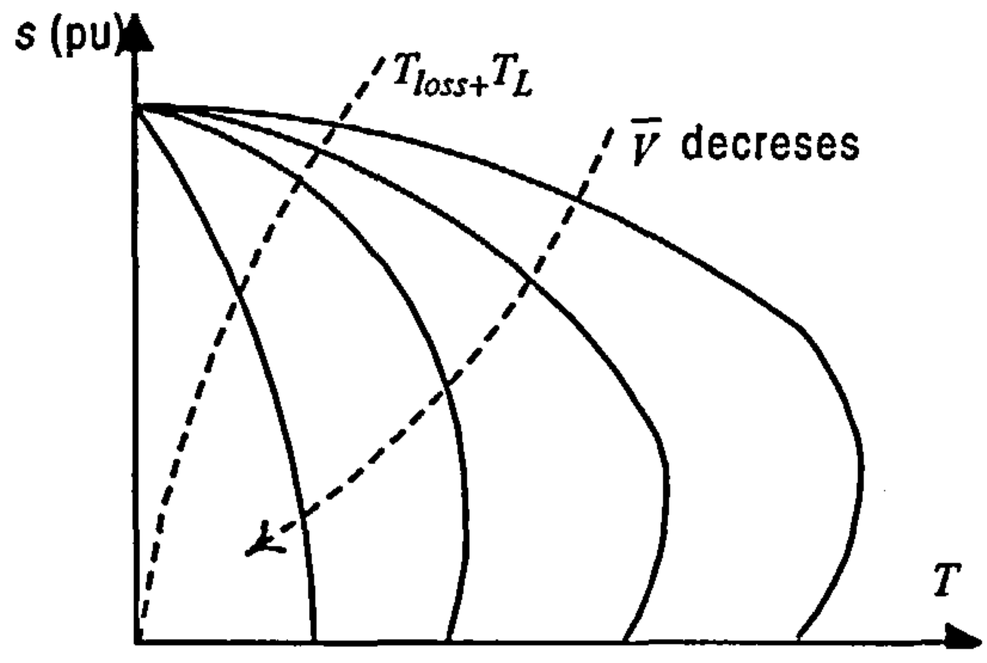

Fig. 6.6: Speed control by variation of potential difference

6.3.3 Variation of Source Frequency

The synchronous speed of an induction motor is given by

$$\omega_s = \frac{2}{p}\omega_{source}, \tag{6.11}$$

where p is the number of poles.

Thus, if the source frequency, ω_{source}, in rad/s, can be varied, so also can the speed of the motor, loaded or unloaded. A simple way of doing this is to supply the motor from an ac generator, which, itself, is being driven by a speed-controlled dc motor. The speed-torque curves are illustrated in Fig. 6.7 [168]. The *base characteristic* in the figure is that for which the source frequency is equal

to the standard power-system frequency, ω_b, for which the motor has been designed.

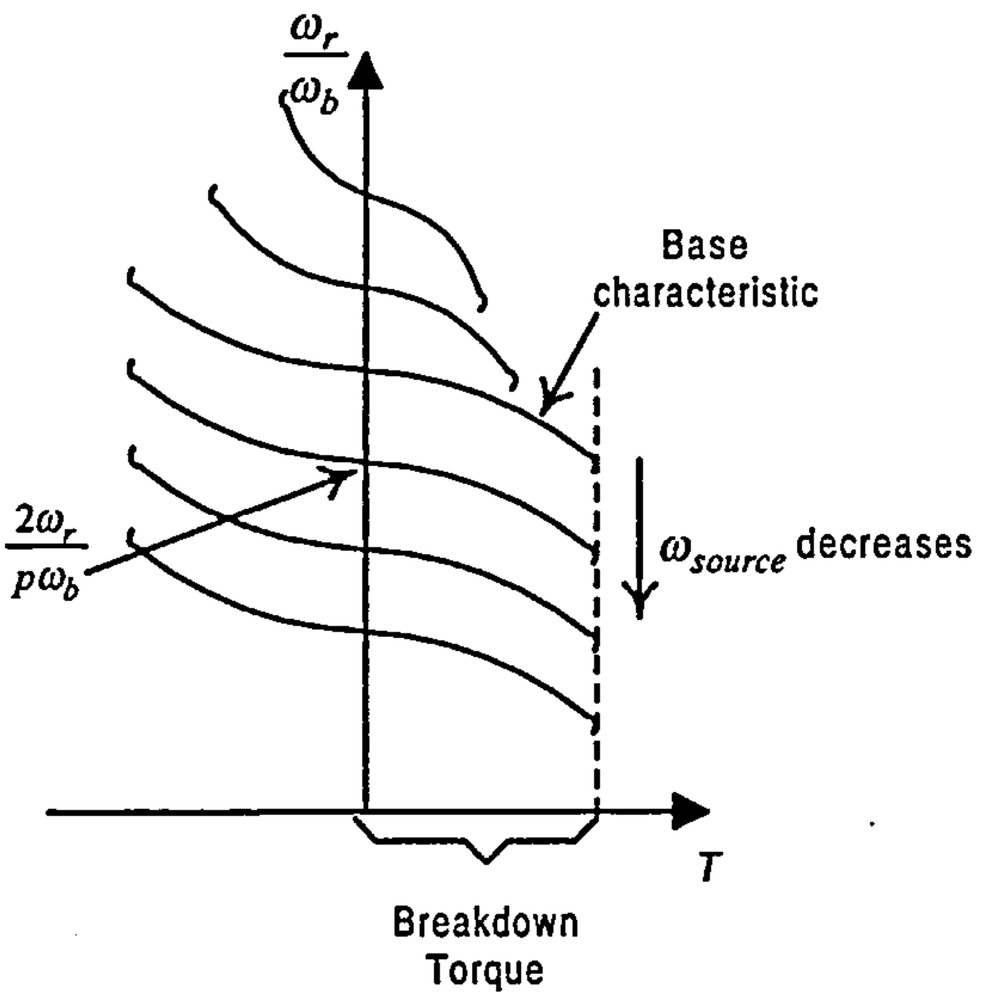

Fig. 6.7: Variable-frequency operation

6.4 Circuit Construction of Quasi-resonant Converter for an Induction Motor

A quasi-resonant circuit was constructed to provide power for a single-phase induction motor to achieve variable-speed control, while maintaining the advantages of resonant technology at zero-current switching. Simple power-electronics circuitry was employed to control the output power of the resonant converter, which, in turn, controls the speed of the induction motor. The initial circuit construction is schematically depicted as solid lines in Fig. 6.8 [121].

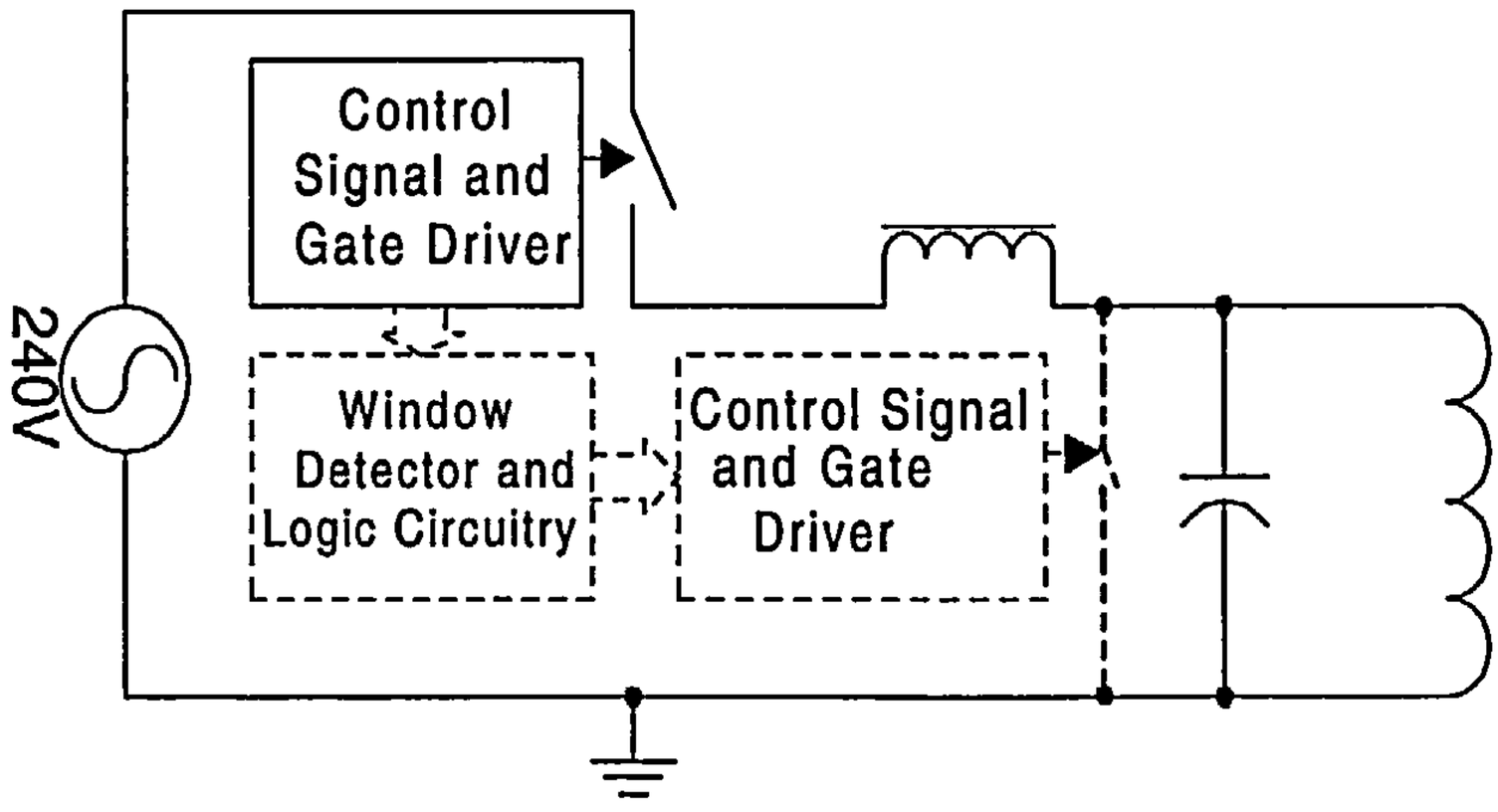

Fig. 6.8: New type of quasi-resonant circuit on induction motor

A two-switch ac-to-ac resonant converter was constructed, and successfully run, using $50Hz$ ac mains modulated with a much higher range of frequency variation, i.e. $50kHz$ to $100kHz$. There were just two resonant components, an inductor of value $130\mu H$ and a capacitor of value $0.022\mu F$ that were arranged as shown in Fig. 6.8. With this combination of passive components, the resonant frequency occurs at $100kHz$.

The switches, that were ultra-fast IGBTs, were arranged back-to-back for the ac operation. They were driven by gate signals from an opto-coupler fed from a signal generator.

6.5 Operational Principle of the System

For the sake of analysis, a simple model of the entire system is given in Fig. 6.9 with the $240V$ ac supply replaced by a square-wave switching to simulate the actual soft-switching of the IGBT switches. The circuit itself can be analyzed in two simple modes, i.e. the mode when the switches are turned on, and the second mode when the switches are off.

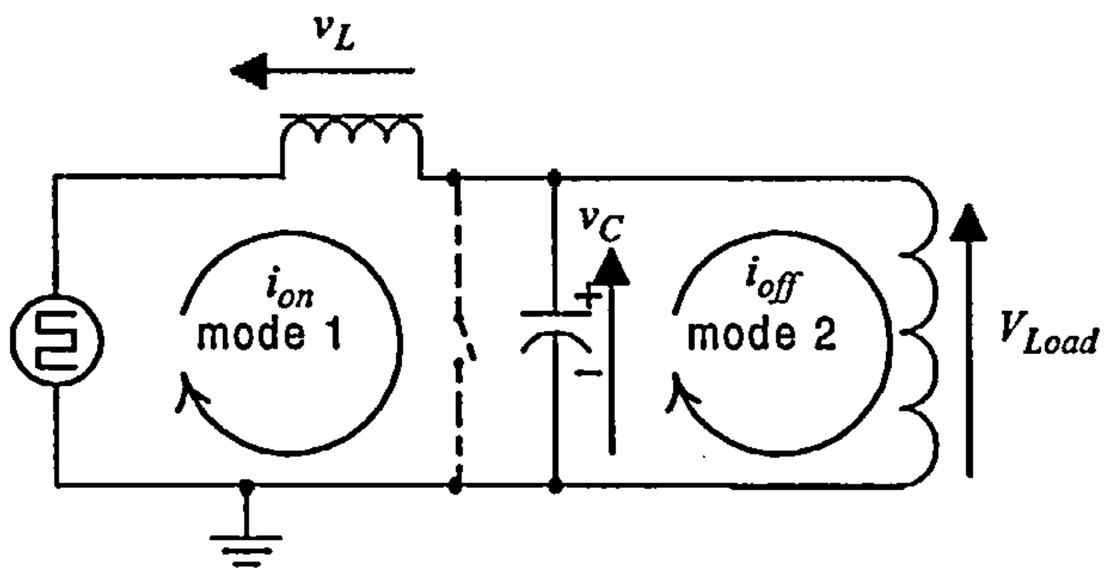

Fig. 6.9: Simplified version of the quasi-resonant circuit

Mode I:- Switches on

When the switches are turned-on, the system effectively behaves like a series-resonant circuit, as has been analyzed in Chapter 2; the only difference is that it is a 'loss-free' series LC circuit. However, there are some losses due to stray capacitance and inductance and also the intrinsic resistance within the passive elements.

The circuit current, or the switch current, i.e. the current flowing through the switches is given

by,

$$\begin{aligned} i_{on}(s) &= \frac{\frac{V}{s}}{sL + \frac{1}{sC}} \\ &= \frac{\frac{V}{L}}{s^2 + \frac{1}{LC}} \\ &= \frac{V}{\omega L} \times \frac{\omega}{s^2 + \omega^2} \quad \text{where } \omega = \frac{1}{\sqrt{LC}} \\ i_t(t) &= \frac{V}{\omega L} sin(\omega t) \end{aligned} \tag{6.12}$$

This shows that the switch-current flows sinusoidally through the resonant inductor, largely 'into' the resonant capacitor owing to the large inductance of the inductive motor compared with the resonant inductor. This operating waveforms are drawn in Fig. 6.10.

The inductor and capacitor voltages are given respectively by

$$\begin{aligned} v_{L_{on}}(s) &= i(s) \times sL \\ &= V \times \frac{s}{s^2 + \omega^2} \\ v_{L_{on}}(t) &= V cos(\omega t) \end{aligned} \tag{6.13}$$

$$\begin{aligned} v_{C_{on}}(s) &= i(s) \times \frac{1}{sC} \\ &= V \times \frac{\omega^2}{s(s^2 + \omega^2)} \\ v_{C_{on}}(t) &= V[1 - cos(\omega t)] \end{aligned} \tag{6.14}$$

From these two equations, it is known that the inductor voltage follows the shape of a cosine waveform. It crosses zero at the peak of switch current, and it is in an opposite polarity when the switch current decreases. The switch current charges up the resonant capacitor to around $2V$, according to Eqn. (6.14). Again, this is also shown in Fig. 6.10.

Mode II:- Switches off

When the switches are turned-off, the capacitor is discharged through the large load inductance. Of course, there may be a little current flowing back to the ac supply through the body-diode in one of the IGBT's. This occurs because the current going through the resonant inductor cannot stop instantly when the switches change state. This is depicted on Fig. 6.9.

The equations governing the discharge-current and charge-voltage during the switch-off are

$$i_{C_{off}}(t) = -\hat{I}e^{\frac{t}{\lambda}}, \tag{6.15}$$

where λ is the time constant of the circuit, i.e. $\lambda = C\times$ resistance in the load inductance, and $\hat{V}$and $\hat{I}$ are peak voltage and current respectively.

$$v_{C_{off}}(t) = \hat{V}e^{\frac{t}{\lambda}} \tag{6.16}$$

Waveforms of the above-described mode 1 and mode 2 operations are given in Fig. 6.10

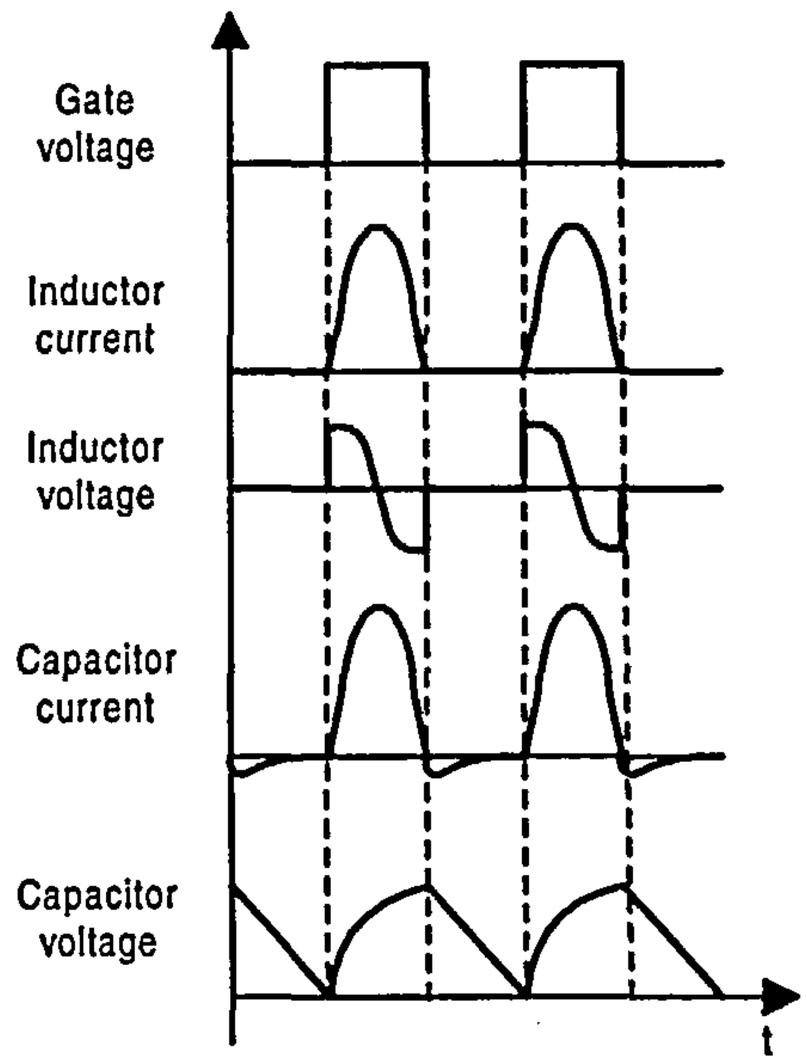

Fig. 6.10: Switching waveforms of the quasi-resonant converter

6.6 Practical Results Obtained and Problems Encountered

In order to achieve variable-speed control, the switching frequency was varied from $50kHz$ to $100kHz$ while maintaining the $5\mu s$ on-time of the switches. With this method, the speed and hence the effective stator voltage and the power delivered to the motor should be able to be controlled by the mark-space ratio of the switches. However, due to the variable nature of the slip-frequency of the induction motor, the peak-to-peak voltage increased inversely with the mark-space ratio of the supplied frequency. This, hardly, gave any variation at all in the speed, as the effective value of speed remained constant. This phenomenon is illustrated in the series of plots at $100kHz$ and $50kHz$ depicted in Fig. 6.11 [121]. It is noted on the plots that the resonant capacitor discharged

in the opposite direction if the switches do not come on before its complete discharge.

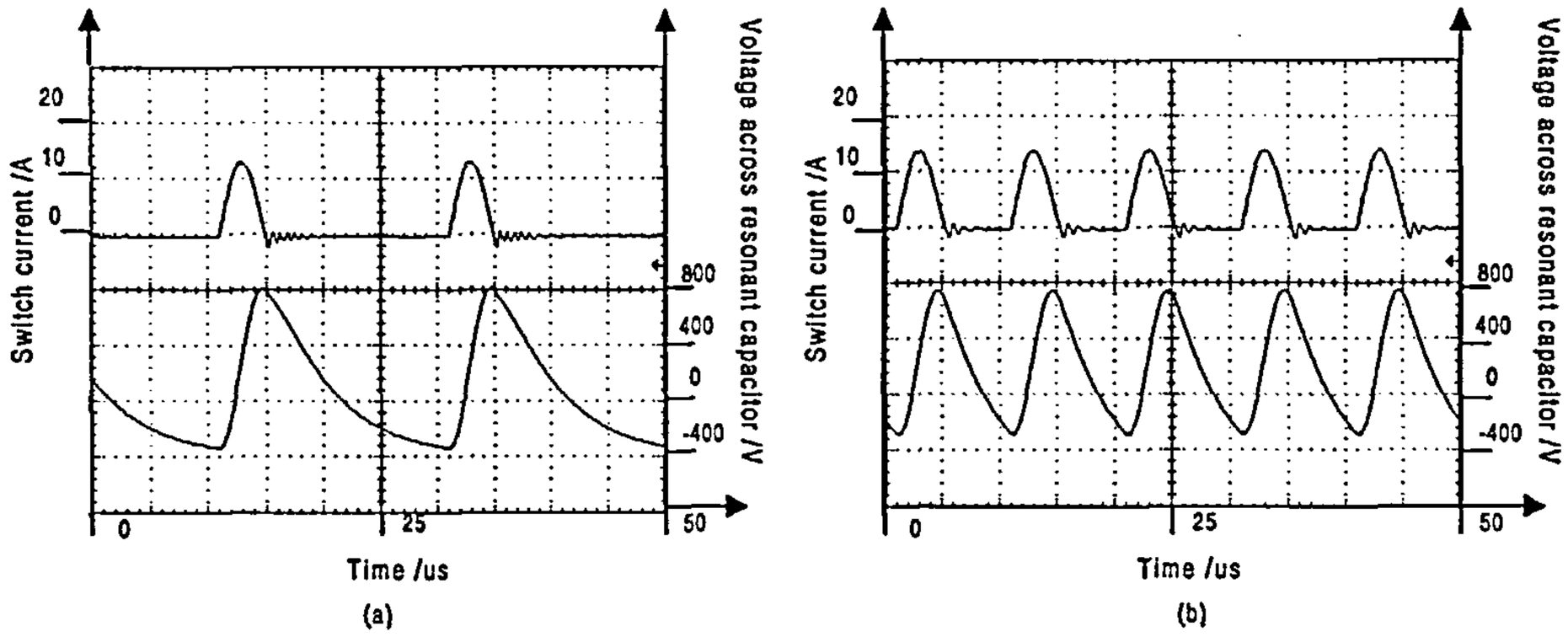

Fig. 6.11: Switch current(top trace) and voltage(bottom trace) across resonant capacitor

6.7 Control-electronic Circuitry

In order to stop the capacitor from being discharged further in the opposite direction so that the motor speed can be varied, the capacitor has to be discharged to ground when the discharging starts. This can be done by inserting another similar arrangement of back-to-back switches in parallel with the resonant capacitor as shown by the dotted line components in Fig. 6.8. The

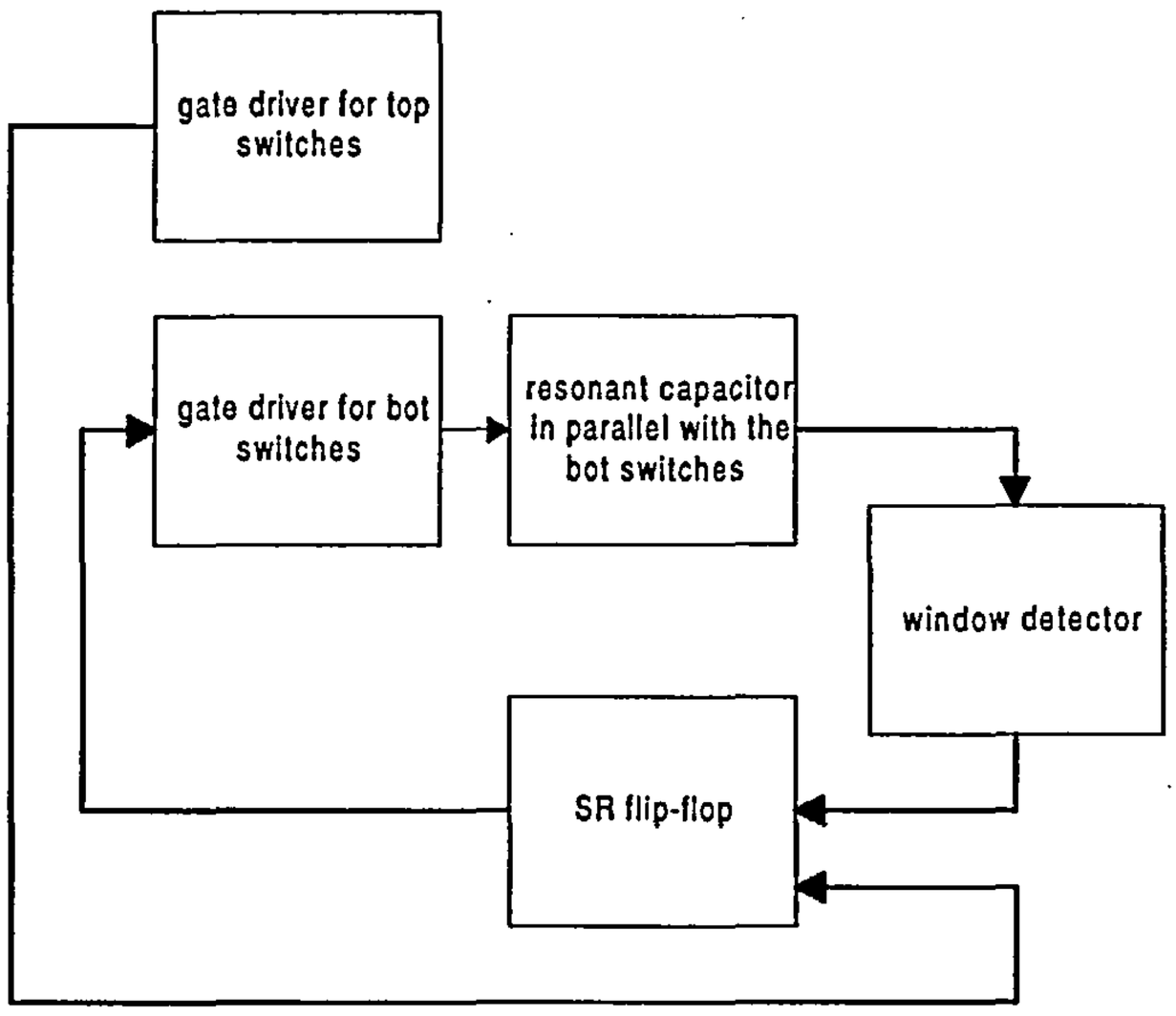

Fig. 6.12: Block diagram of control electronics

switches have to be turned on when the capacitor is discharged near to zero in both directions. Thus, a means to detect the discharge falling within the prescribed limit had to be employed. For

this purpose, a window detector fed by the discharged voltage was used. The lower and upper limits of the window were both set at $-1V$ and $+1V$ respectively. Within this limit, the output triggered by the detector was gated together with the output signal from the signal generator. The output from the signal generator also served as the gate signal into the top switches. The SR-flip-flop then turned on the bottom switches. The pair of bottom switches was only turned on if, and only if, the capacitor voltage fell near to zero in either direction and the top switches were off. At other times, the bottom switches have to remain off. The block diagram of the control circuitry is drawn in Fig. 6.12 [121]. To avoid a long overlapping on-time between the two pairs of top and bottom switches, which could cause a shoot-through, the delay on-time period had to be carefully monitored.

6.8 Practical Results with Variable-speed Control

With the new arrangement of the control-electronic circuit, the quasi-resonant converter was tested again on the induction motor. The results are shown in Fig. 6.13 [121].

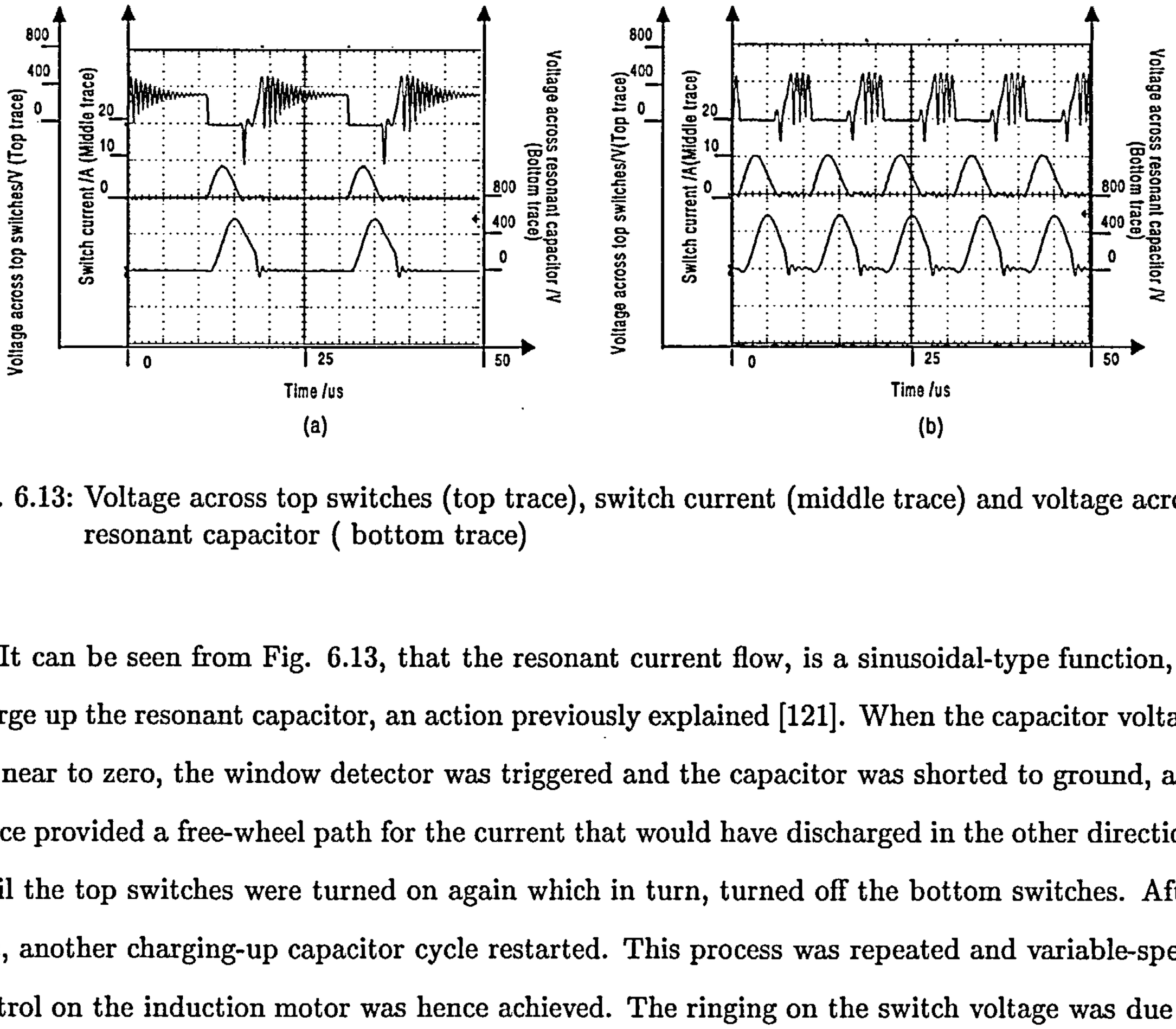

Fig. 6.13: Voltage across top switches (top trace), switch current (middle trace) and voltage across resonant capacitor (bottom trace)

It can be seen from Fig. 6.13, that the resonant current flow, is a sinusoidal-type function, to charge up the resonant capacitor, an action previously explained [121]. When the capacitor voltage fell near to zero, the window detector was triggered and the capacitor was shorted to ground, and hence provided a free-wheel path for the current that would have discharged in the other direction, until the top switches were turned on again which in turn, turned off the bottom switches. After this, another charging-up capacitor cycle restarted. This process was repeated and variable-speed control on the induction motor was hence achieved. The ringing on the switch voltage was due to the large inductive effect being across the switches.

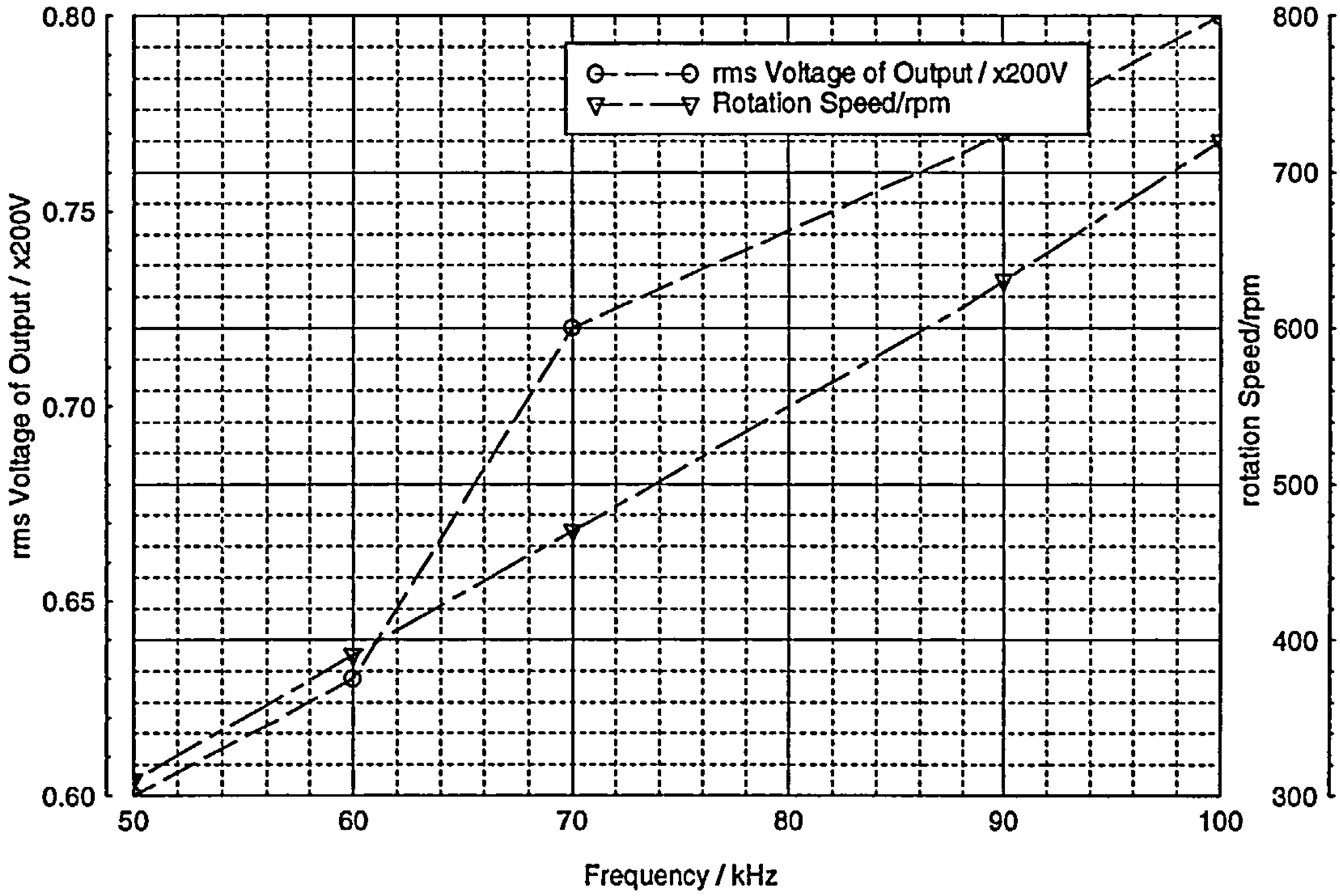

Fig. 6.14: Variation of speed and output voltage of induction motor

Fig. 6.14 shows that variations of nearly 133% of the motor speed with 33% in output voltage were achieved [121]. Further investigations of this problem have yet to be pursued.

6.9 Conclusion

This chapter has presented novel hardware techniques in attaining output power-variation, and hence the speed change of a single-phase induction motor without sacrificing the desirable features of quasi-resonant converter. These techniques employed show potentially great promise in its ability to reduce size and weight of equipment, although further investigations have to be carried out.

Chapter 7

Modifications of Performance Profiles

7.1 Introduction

It has been shown in the earlier chapters that power control of resonant converters can be achieved quite easily by novel and easily understood mathematical algorithms and hardware techniques. Those designs, however, can have their performance modified while using the same topology without repeating the full-design calculations each time.

For the purpose of showing the applications of these design-modification methods, the series-parallel load-resonant system discussed in Chapter 5 is used as the example. It has been demonstrated that the converters are capable of attaining controlled variable-output power while maintaining the desirable properties of soft-switching. The most challenging task in obtaining the design is to establish the non-linear linked properties of the electrical-component values relating to the overall system parameters.

As already explained, establishment of these parameters can be performed using an interactive computing programme. This, however, was a very tedious process and was superseded by adopting the *Gröbner Basis* technique that reduces much of the computation time compared with the initial method. Nevertheless, substantial computation is required by any method adopted, particularly, if much higher-order systems are encountered. The purpose of this chapter is to show how alterations to the initial design can be made easily.

It is necessary to emphasize that all the methods that are due to be presented in this chapter, can be applied to any hard-won prototype designs, before, or after, performing the mathematical and hardwares techniques, so that they can be transformed into a variety of similar designs.

7.2 Circuit-scaling Laws

Using these scaling laws, designs that produce circuits specifying different load currents, circuit impedances and frequency shifts away from the prototype design can be easily performed. The circuit theorems employed in the design modifications were established decades ago but do not seem to have been used much in practice [169].

High-pass, band-pass and low-pass characteristics are achievable while maintaining the desirable properties of the original design, including, for example, inherent short-circuit and open-circuit protection [166].

7.2.1 The Prototype Converter Circuit

The half-bridge series-parallel load-resonant converter described in Fig. 4.6 is taken as the prototype design where the values of the components obtained from the design procedure are re-stated in the legend. The equivalent load-value, in practice, can be obtained using a transformer with appropriate turns ratio before the actual load.

The frequency-response properties of this circuit shown in Fig. 5.4, are redrawn again in Fig. 7.1 for easy comparisons. However, the input peak-to-peak voltage is $340V$. The turning-point frequencies were specified to be at $60kHz$, $85kHz$ and $110kHz$ respectively giving a maximum-to-minimum power-level-ratio of $(25.4/1.3) = 19.5$. Note that the power-factor is unity at these frequencies.

This circuit has a power-factor variation of $1 - 0.53$ across the operating frequency. This range can be improved upon as in Section 5.8, but it has not been done in this case as the main objective is to use this circuit as a model for employing the scaling techniques mentioned above.

7.2.2 Application of the Scaling Laws to the Resonant Converter

The laws are described in detail in reference [169]. The first is the *impedance magnitude-changing law*; this states essentially that, given an impedance written in the general form of

$$Z_g = R_g + j\omega L_g + \frac{1}{j\omega C_g}, \tag{7.1}$$

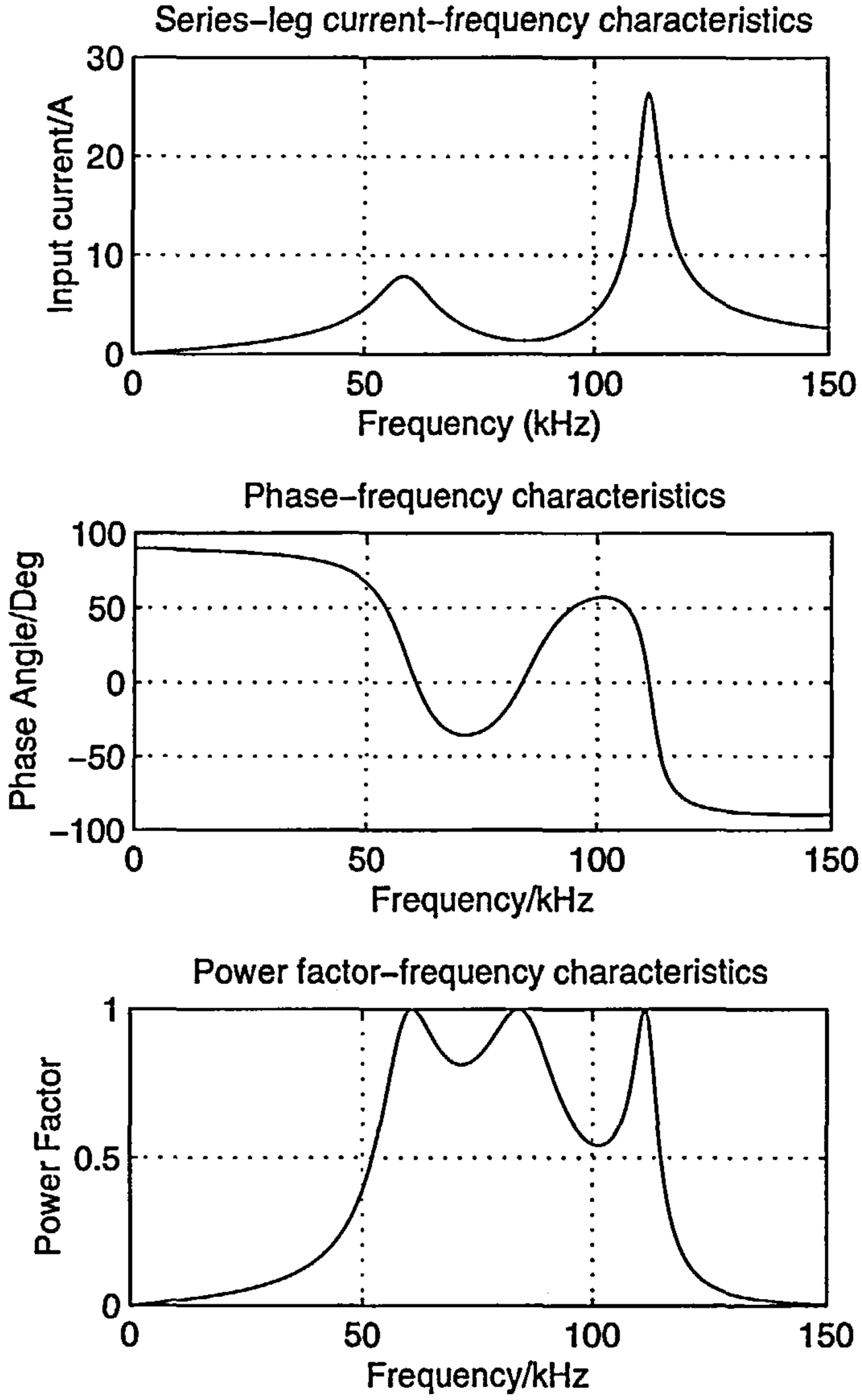

Fig. 7.1: Modified frequency response of resonant converter for welding power supply
$L_s = 100\mu H$, $L_L = 80\mu H$, $L_p = 14\mu H$,$C_s = 0.045\mu F$, $C_L = 0.2\mu F$, $C_p = 0.045\mu F$ and $R_L = 10\Omega$

this impedance, when scaled by a constant, k_z, can be transformed into an impedance of the following form,

$$Z_n = k_z R_g + k_z j\omega L_g + \frac{1}{\frac{j\omega C_g}{k_z}} = k_z Z_g \tag{7.2}$$

i.e. resistor values, inductor values are scaled by k_z and capacitor values scaled by k_z^{-1}. This effectively scales the magnitude of the frequency response by the factor k_z while leaving the phase characteristics unchanged. This is a simple procedure to perform. As an example, suppose it is required to increase the impedance of the above circuit by a factor of $k_z = 2$, then the new values of the components required are $L_s = 200\mu H$, $L_L = 160\mu H$, $L_p = 28\mu H$, $C_s = 0.02\mu F$, $C_L = 0.1\mu F$,

$C_p = 0.02\mu F$ and $R_L = 20\Omega$. The frequency response of the new circuit is shown in Fig. 7.2 where it can be seen that only change is that the magnitude of the input current has been halved at all frequencies as expected [166].

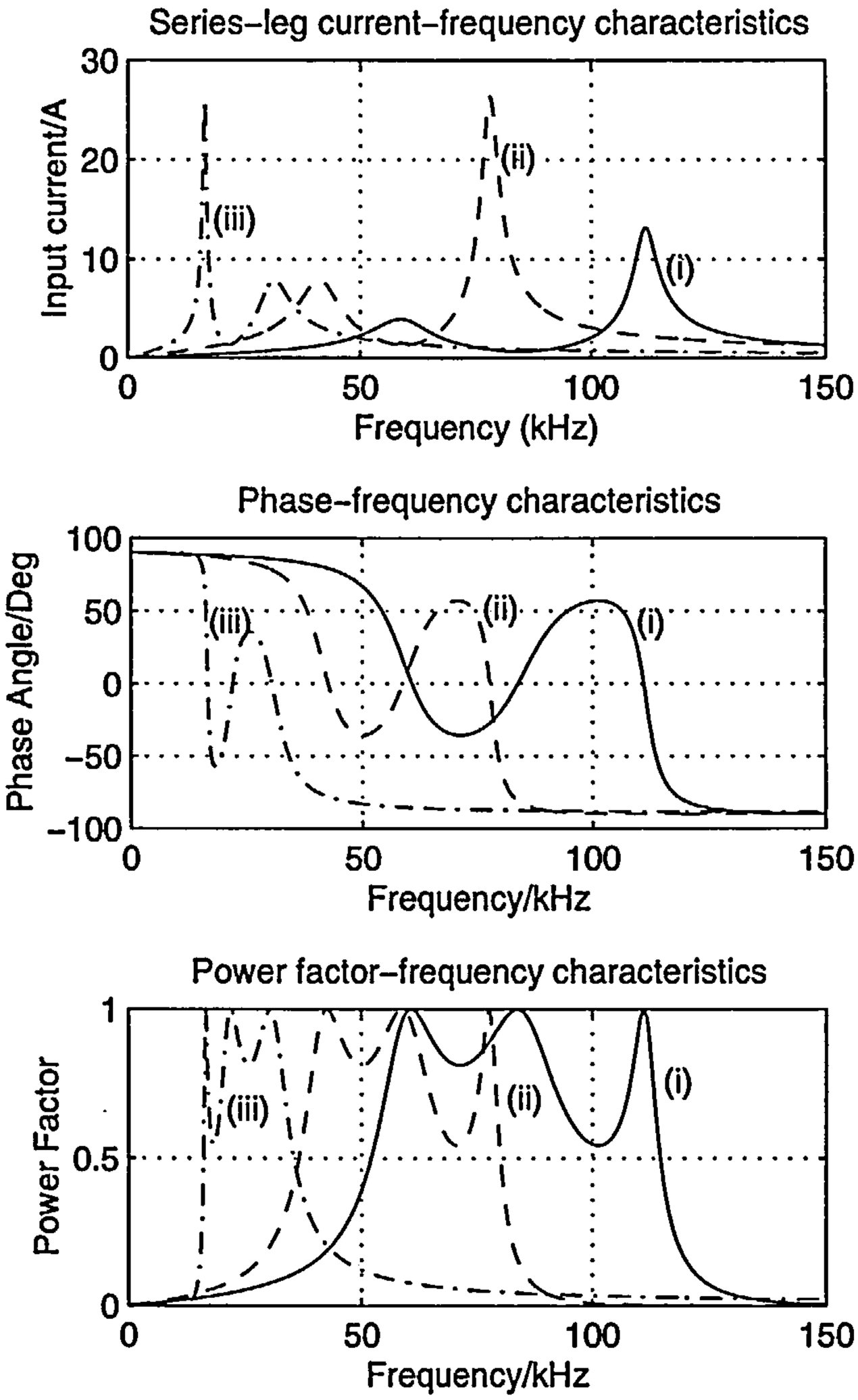

Fig. 7.2: Illustration of frequency response of series-parallel load-resonant circuit using circuit-scaling Laws
(i) after impedance scaling
$L_s = 200\mu H$, $L_L = 160\mu H$, $L_p = 28\mu H$, $C_s = 0.02\mu F$, $C_L = 0.1\mu F$, $C_p = 0.02\mu F$ and $R_L = 20\Omega$
(ii) after frequency scaling
$L_s = 143\mu H$, $L_L = 114\mu H$, $L_p = 20\mu H$, $C_s = 0.06\mu F$, $C_L = 0.3\mu F$, $C_p = 0.065\mu F$ and $R_L = 10\Omega$
(iii) after frequency inversion
$L_s = 304\mu H$, $L_p = 304\mu H$, $L_L = 68.5\mu H$, $C_s = 0.14\mu F$, $C_L = 0.17\mu F$, $C_p = 0.98\mu F$, $R_L = 10\Omega$

The second law to be applied is that of *frequency shifting*. In this case, while keeping the current magnitudes identical to the original design, the frequency is scaled by a factor k_F, according to the

rule

$$Z_n(j\omega) = R_g + j\omega\frac{L_g}{k_F} + \frac{1}{j\omega\frac{C_g}{k_F}} = Z_g(\frac{j\omega}{k_F}), \tag{7.3}$$

i.e. in this case, the resistor values are unchanged, inductor values are changed by a factor k_F^{-1} and capacitor values by k_F^{-1}.

Thus, if it is wished to scale the frequency of the original design by $k_F = 0.7$, the re-scaling component values are $L_s = 143\mu H$, $L_L = 114\mu H$, $L_p = 20\mu H$, $C_s = 0.06\mu F$, $C_L = 0.3\mu F$, $C_p = 0.065\mu F$ and $R_L = 10\Omega$. The three turning point-frequencies now become $43kHz$, $59kHz$ and $78kHz$. The resulting frequency response is shown in Fig. 7.2.

The third law enables the frequency response to be essentially *reflected about any chosen radian frequency, ω_R*. This is done by leaving resistor values unchanged, changing inductor values to $L_n = \frac{1}{\omega_R^2 C_g}$ and capacitor values to $C_n = \frac{1}{\omega_R^2 L_g}$, i.e.,

$$\begin{aligned} Z_n(j\omega) &= Z_g(-\frac{j\omega_R^2}{\omega}) \\ &= R_g + j\omega(\frac{1}{\omega_R^2 C_g}) + \frac{1}{j\omega(\frac{1}{\omega_R^2 L_g})} \end{aligned} \tag{7.4}$$

For example, starting with the original design, suppose it is required to examine the resulting frequency response when the reflected frequency is $43kHz(270krad/s)$. The result is shown in Fig. 7.2. Note that the lead-phase angles of the original design have turned to lag-phase angles and vice-versa. The resulting component-values, for this example, after this transformation, are $L_s = 304\mu H$, $L_p = 304\mu H$, $L_L = 68.5\mu H$, $C_s = 0.14\mu F$, $C_p = 0.98\mu F$, $C_L = 0.17\mu F$, $R_L = 10\Omega$. A very important practical point, in this particular case, is that the highest current available is now at the lower of the two resonant peaks. Thus switching losses are reduced compared to the original design.

7.2.3 Summary

Using one prototype design of a load-resonant converter, that has previously been demonstrated to produce an extremely versatile and practical system, three simple scaling laws have been used to modify the original design in the following ways;

1. raise or lower the input-impedance level while retaining the basic frequency response shape.
2. Scale the frequency so that the effective frequency range, i.e. the prototype frequency-response,

can be expanded or compressed.

3. reflect the original system around a chosen frequency.

The calculations involved in these modifications are extremely simple where as establishing the original design, although simple in principle, is essentially done by trial and error if the *Gröbner Basis* technique is not employed, albeit using a computer.

7.3 Continuous Resonance

The series-parallel load-resonant converter circuits that were presented in Chapter 5 show that they can be operated at zero-current-switching at two, or three, discrete power levels. Nevertheless, as the converters change operation between these discrete power levels, i.e. switching from one resonant frequency to another, switching losses are encountered as shown in Fig.7.3 [3].

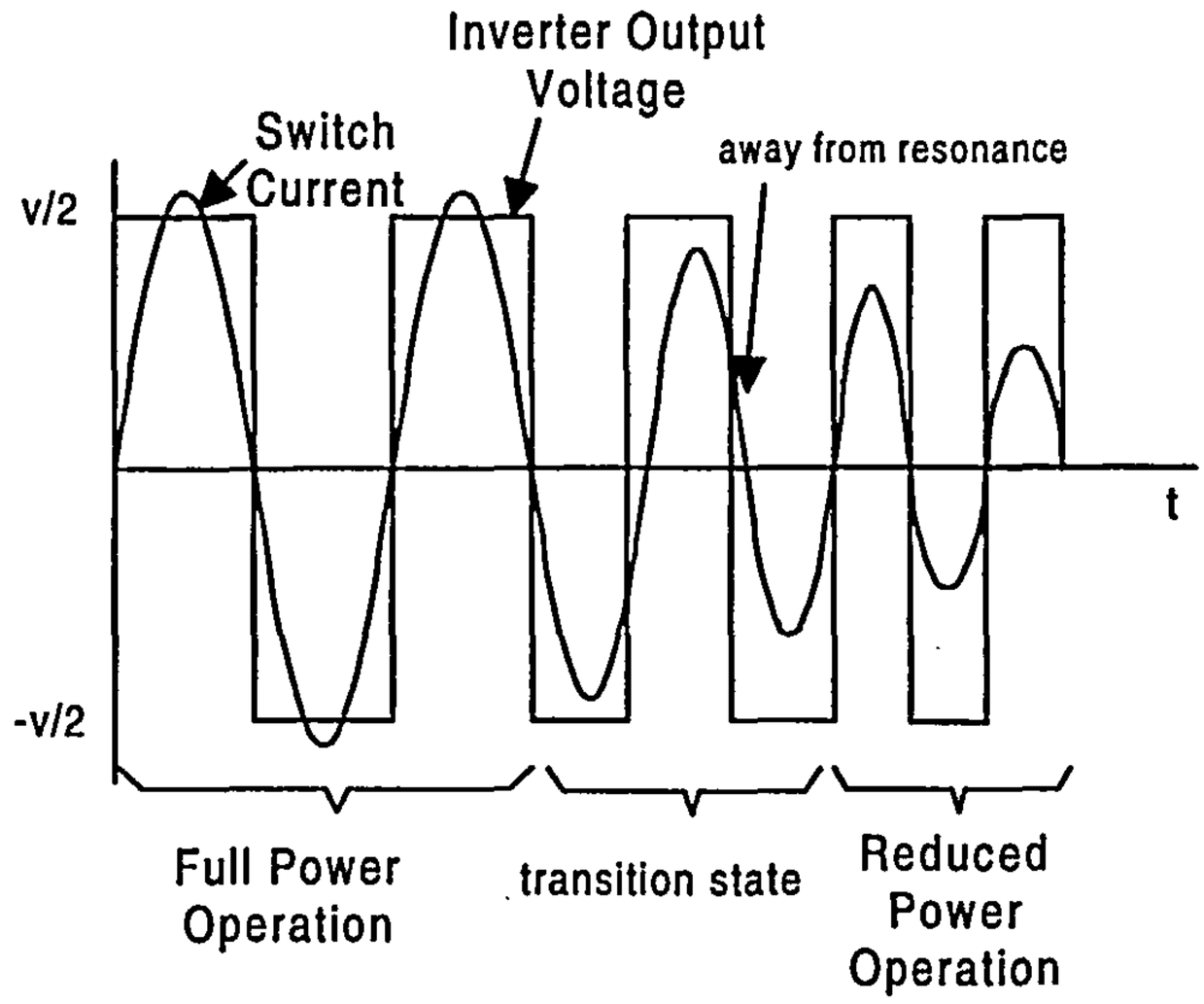

Fig. 7.3: Change in switch current as circuit frequency is varied from high-power to low power operation in discontinuous resonant circuit

In order to avoid the switching losses during the transition from one resonant frequency to another, the circuit can actually be operated near to resonance over a wide frequency range [121]. This then allows the output power of the circuit to be varied continuously over this frequency range resulting in a load-resonant converter with zero current soft-switching over a range of output power. The prototype circuit constructed is actually the same resonant converter design, as described in Chapter 5, but with different component values. It is used to serve as an example of how the 'continuous resonance' works, showing a power variation of $2:1$ over a frequency range of $30kHz$.

7.3.1 Circuit Analysis

The half-bridge series-parallel load-resonant converter, consisting of a series leg, a parallel leg and a load leg containing the load, has been shown in Fig. 4.6. The power switches in the circuit are switched alternately exciting the resonant circuit with a square-wave of voltage.

Using the same analytical technique, i.e. the *Gröbner Basis* technique, the circuit can be designed with different values of R_{tot} at each of the resonant frequencies of the circuit using the same impedance equation given in Eqn. (4.1). In order to obtain a minimal phase difference between the resonant frequencies in practice, the three discrete resonant frequencies were specified close together. This thereby results in a reasonably large frequency range over which the resonant current is practically in phase with the inverter voltage and therefore, the switching losses in the converter are minimal.

The same design procedure was used to derive the relationships among the passive components, resonant frequencies and the two resistance values at two different resonant frequencies. The values that were specified were $\omega_0 = 50kHz$, $\omega_1 = 60kHz$, $\omega_2 = 76kHz$, $R_{tot_a} = 60\Omega$, $R_{tot_b} = 30\Omega$, $C_p = 0.045\mu F$, $L_p = 0H$ and $L_L = 130\mu H$, which then give the values of $L_s = 130\mu H$, $C_s = 0.45\mu F$, $C_L = 0.45\mu F$ and $R_L = 60\Omega$. These values had been rounded to practical values. The circuit designed and constructed with these values, shows a near resonant operation over the range $30 - 80kHz$. L_p was equated to zero to allow more current to flow through the parallel leg, and so that the change of the load in the load-leg would not cause significant effect between the current and voltage phase-angles.

7.3.2 Simulation and Experimental Results

Fig. 7.4 shows how the characteristics of this design vary with frequency. The phase plot remains near to zero from $30 - 80kHz$ while the series-leg current varies from $2.5A$ to $5.5A$, indicating a significant power change in the circuit.

The design was constructed and tested in the half-bridge resonant converter. The load was a resistor and was placed on the output of a rectifier to minimize the effect of the load inductance on the resonance frequencies. The DC supply voltage was $340V$.

Fig. 7.5 shows the voltage across the bottom switch of the converter and the series-leg current at $50kHz$, $60kHz$ and $76kHz$. The DC supply voltage was $340V$. The circuit remains near to resonance throughout the whole frequency range while the magnitude of the current and, hence the power delivered to the load varies.

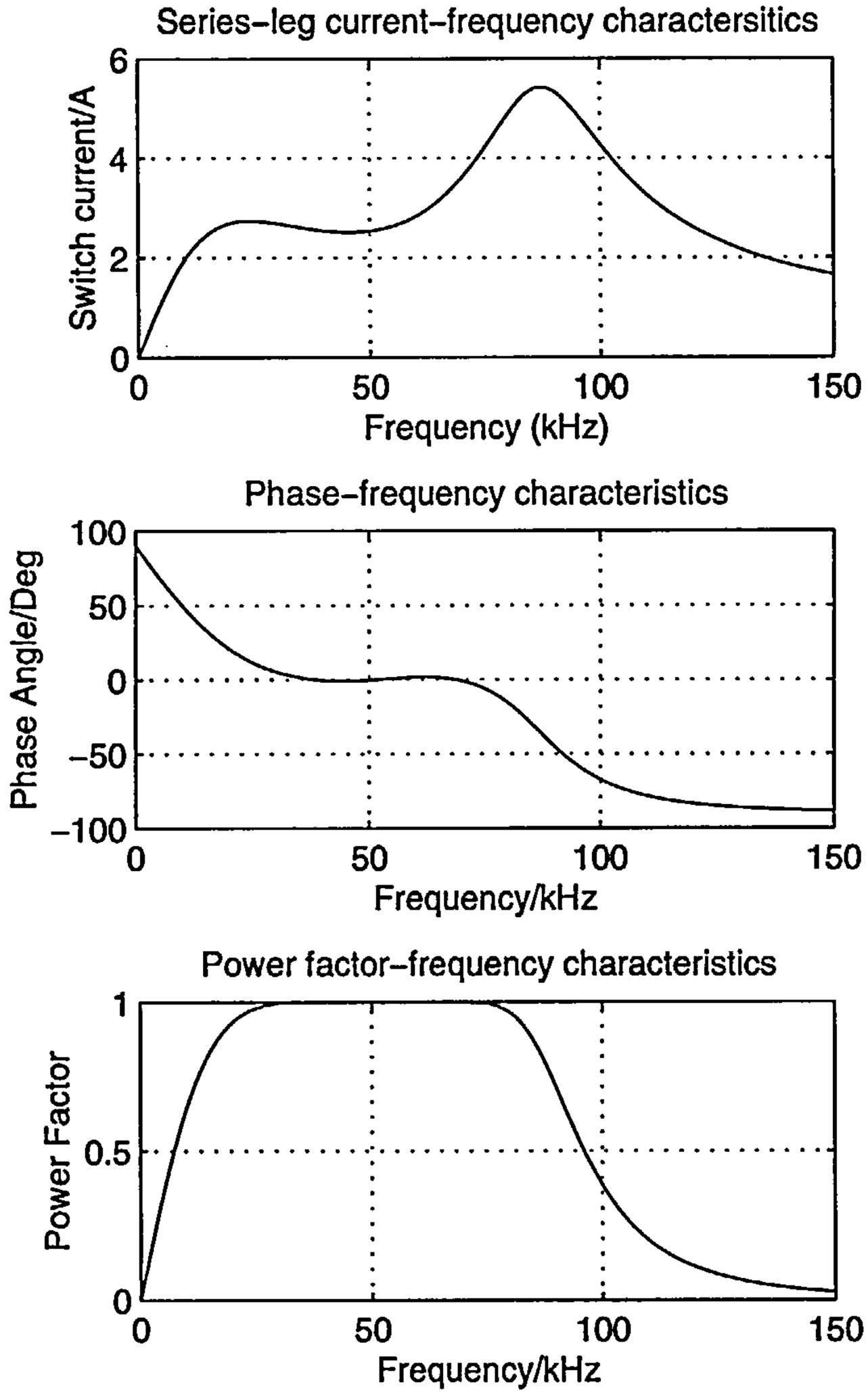

Fig. 7.4: Frequency response of series-parallel load-resonant circuit with minimal phase difference from $30kHz$ to $80kHz$

Fig. 7.6 shows the variation in the input and output power of the circuit with frequency. The efficiency of the converter varies from approximately 88% to 80% over the frequency range of $37-76kHz$. The converter is most efficient at lower frequencies, where both the circulating current and the output rectifier switching losses are smallest.

7.3.3 Summary

A series-parallel load-resonant converter, with near to resonant operation over a wide frequency range, has been demonstrated practically. The resonant circuit has been designed so that over this soft-switched frequency range there is a significant variation in the output power of the circuit. This therefore reduces the switching losses to the minimum at both operations at the resonant

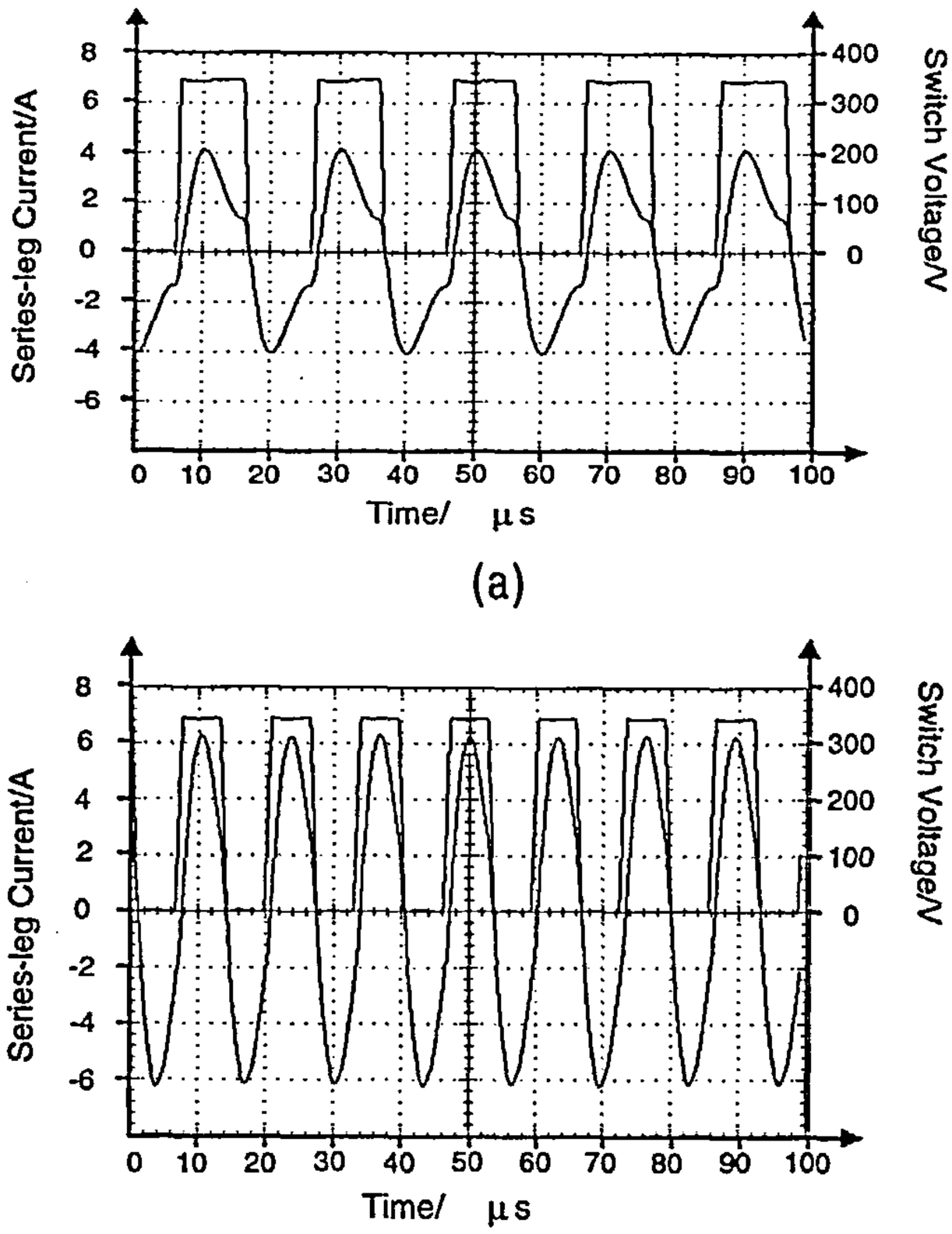

Fig. 7.5: Switch voltage and series-leg current at 50, 60 and $76kHz$

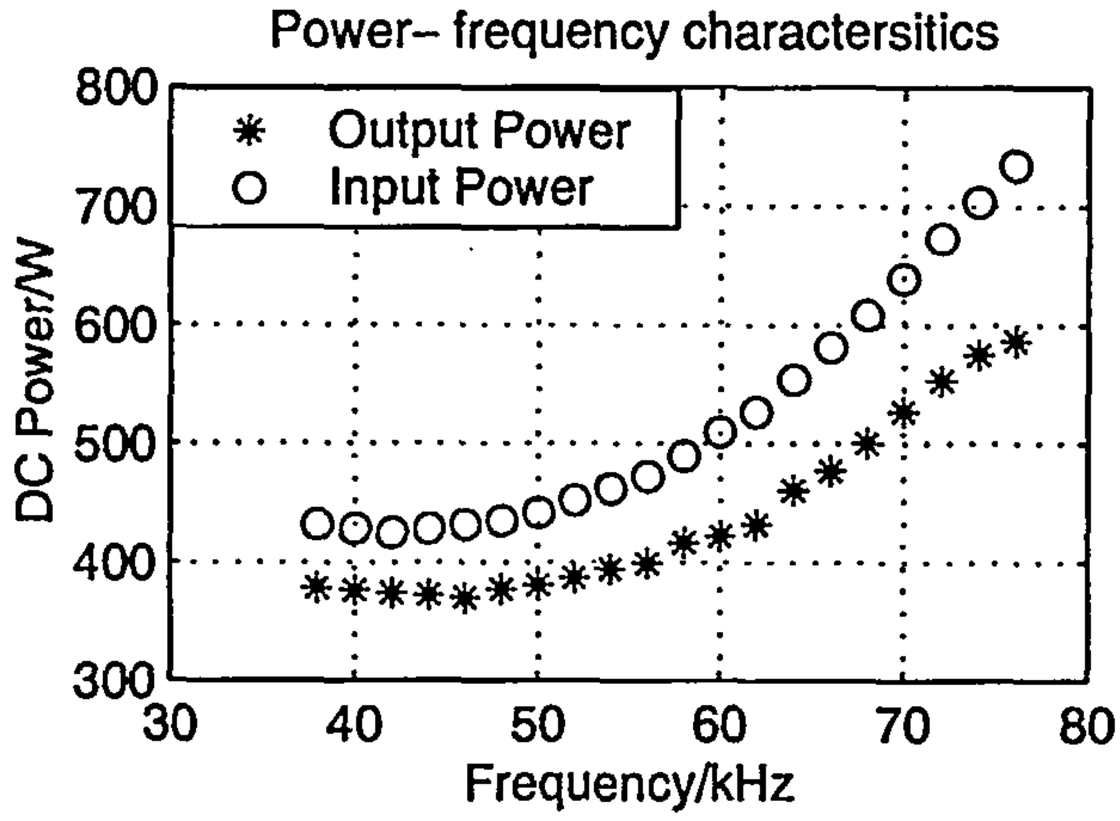

Fig. 7.6: Input power and output power of experimental converter from 35 to $80kHz$

frequencies and at the transition between the frequencies.

7.4 Design Curves

7.4.1 Introduction

Design curves can be used as a simple design tool to produce variations on a built-prototype resonant converter with the same topology but different system performances, e.g., frequency response of the circuit. This can then serve as a guideline for the designers before building the real circuit [121]. This section shows a way of designing resonant converters, with limited power change, without going through any mathematical derivation.

7.4.2 Sensitivity Analysis

In order to obtain the design curves, sensitivity analysis was done on the system shown in Fig. 4.6. Again, L_p was equated to zero based on the reason given in Section 7.3. Of course, there is no reason why it should not be assigned a value.

The values of other components were varied one at a time within 10% of the original component values used in Fig. 4.6. Again, there is no restriction for the percentage change of the component-value range to be used in the analysis. A graph was then plotted as shown below in Fig. 7.7 [121].

From the curves, although it is clear that R_{tot} varies nonlinearly, some patterns can still be perceived. In addition, with the help of these design curves, different circuits can be designed based on the desired percentage change in R_{tot}, to yield the change in power caused by changing each component value in turn. The designs can then be simulated to obtain frequency-response curves. In each case, different graphs showing magnitude of the admittance, phase of admittance, locus of impedance and output power-against-frequency can be plotted as well.

From the study of the design curves depicted in Fig. 7.7 showing the maximum power change, i.e. 50%, the change in L_L was found to have the most significant effect on the percentage change of R_{tot}.

Therefore, in order to see if more power change, i.e. more than 50%, could be obtained, the components in the load-leg, as they were shown to be the most prominent 'elements' giving the bigger power change, were experimented with different ideas, for examples, equating X_L to X_P, X_L to zero, and so on. It was found that when X_L was equated to zero, interesting results were obtained.

In the case, when X_L was equated to zero while other components were given various values, i.e. $L_S = 90\mu H$, $C_S = 0.45\mu F$, $C_P = 0.03\mu F$, $L_L = 130\mu H$, $C_L = 0.07\mu F$ and $R_L = 53\Omega$, it was

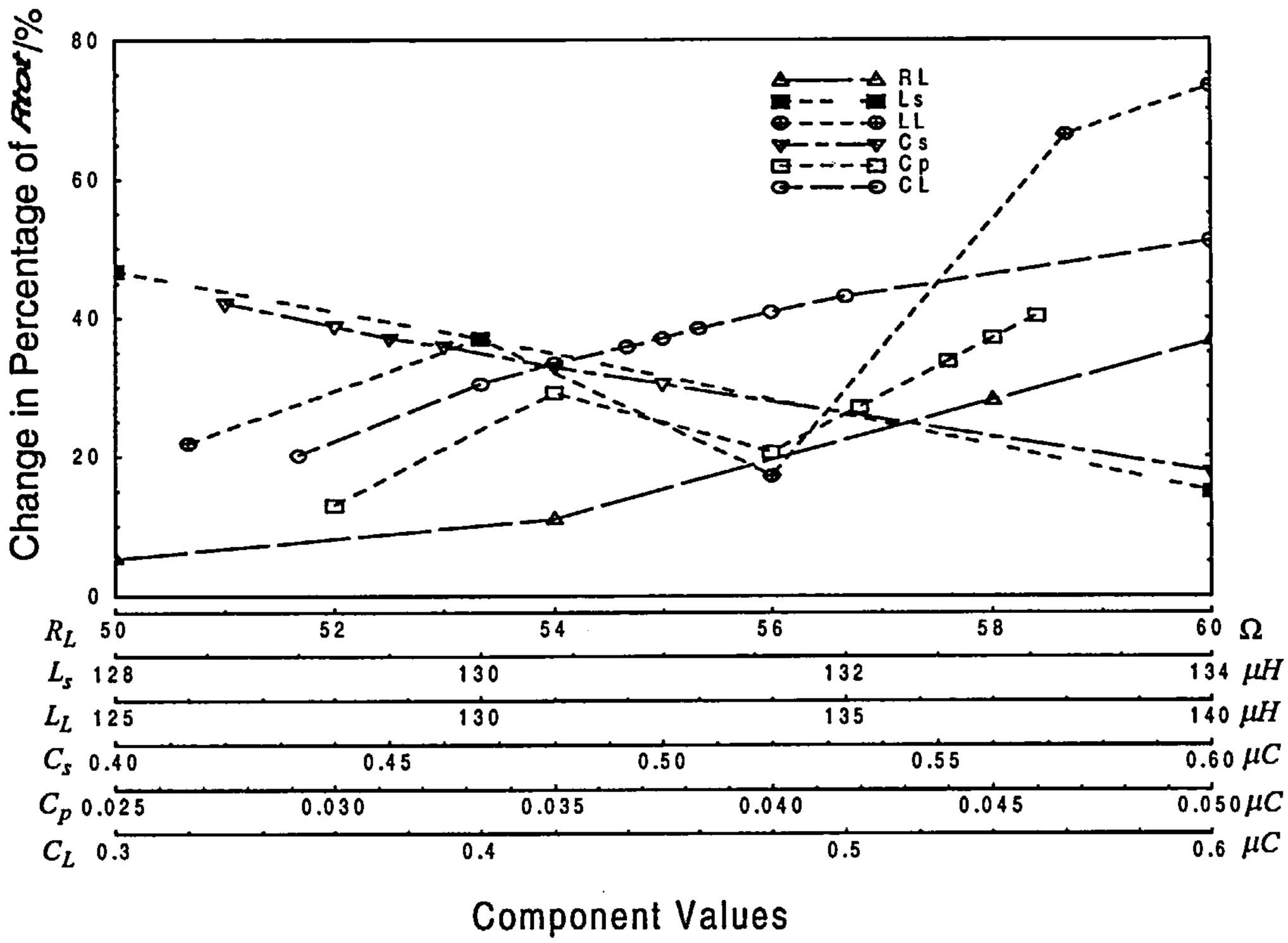

Fig. 7.7: Variation of percentage change in R_{tot} depending on the component values, where L, C and R are inductor, capacitor and resistor respectively, and the subscripts $_s$, $_L$ and $_p$ denote series-leg, load-leg and parallel components

found that the power variation is nearly 80% at the larger frequency range from $50 - 110kHz$, as attached in Fig. 7.8.

7.4.3 Summary

Although the above approach shown here is more a trial-and-error method, it serves as a simple design tool to get required circuit performance when there are no restricted circuit parameters, like necessity of particular resonant frequencies. In addition, design curves give an insight to the effect of individual component change on the circuit characteristics. Nevertheless, if a good and more accurate design is needed to specify the turning-point frequencies to conform to tight specifications, the GB technique should be employed.

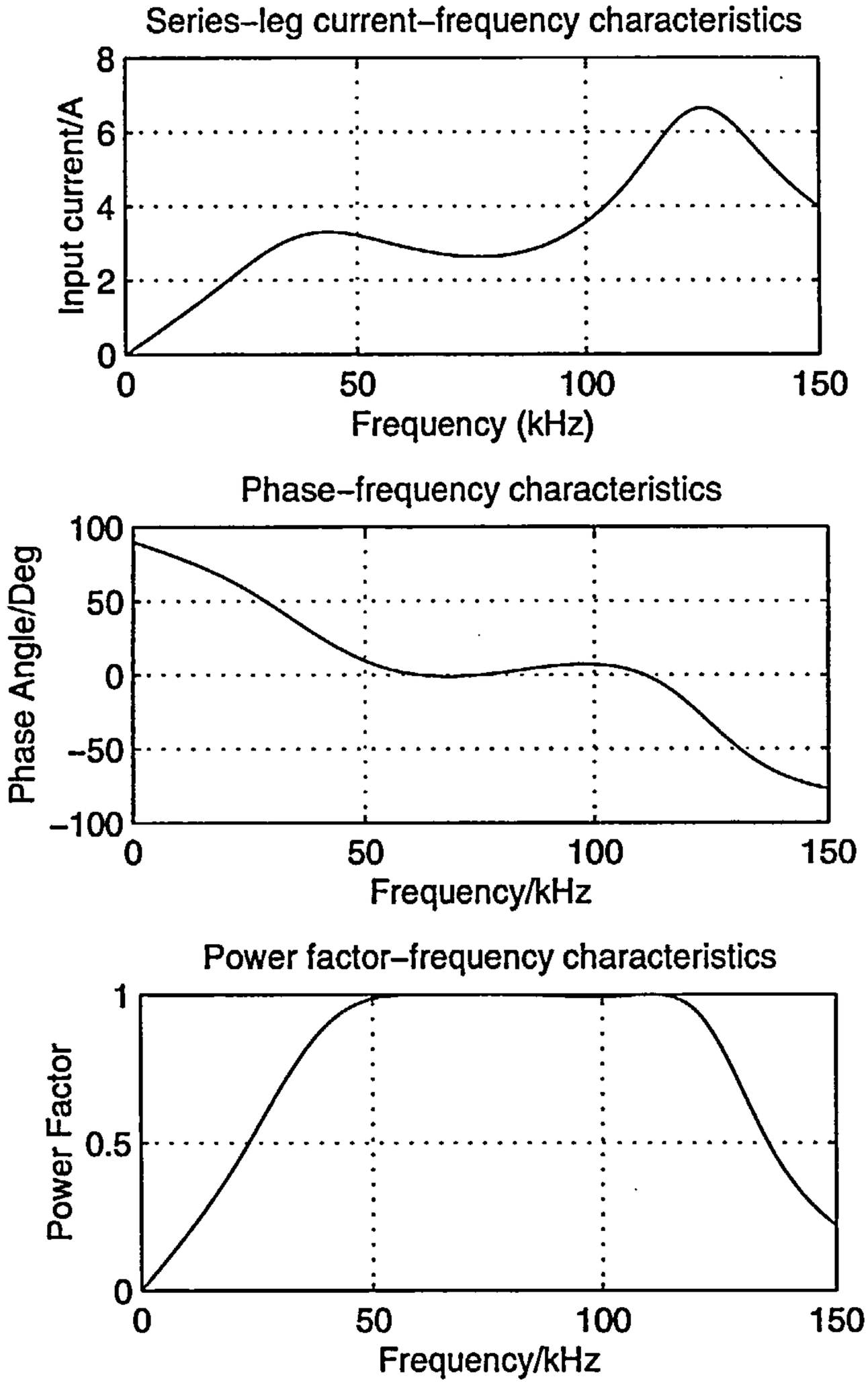

Fig. 7.8: Frequency response of series-parallel load resonant circuit with minimal phase difference from 50 to 110 kHz based on design curves

7.5 Topology Modifications

7.5.1 Introduction

Component-count of an electrical circuit is usually an important factor in equipment-determination. Thus, there is a need to further investigate the resonant converter presented in Fig. 4.6 to determine, for example, whether similar system performance could be obtained with fewer passive components. One way to do this is to modify the existing configuration of the series-parallel load-resonant converter, and examine the effect.

7.5.2 Parallel Load-resonant Converter

Mathematical Analysis

A parallel load-resonant converter is shown as in Fig. 7.9.

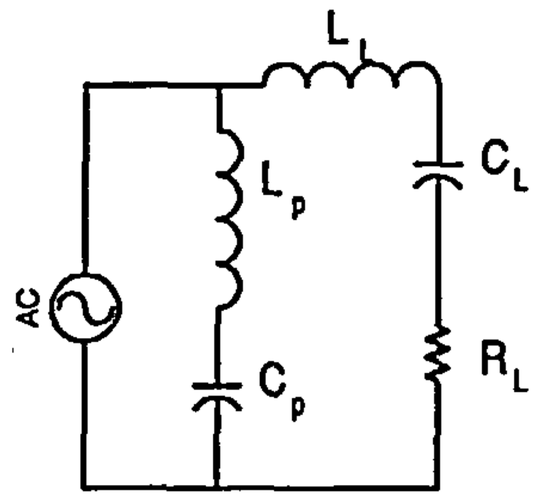

Fig. 7.9: Parallel load-resonant converter

To specify the operating frequencies and the component values, the GB technique is used. In order to do this, once again, the input impedance of the circuit has to be obtained, i.e.,

$$Z_{tot} = \frac{X_p^2 R_L + j\{X_p[R_L^2 + X_L(X_L + X_p)]\}}{R_L^2 + (X_L + X_p)^2} \tag{7.5}$$

This gives,

$$R_{tot} = \frac{X_p^2 R_L}{R_L^2 + (X_L + X_p)^2} \tag{7.6}$$

and,

$$X_p[R_L^2 + X_L(X_L + X_p)] = 0;$$

or,

$$\begin{aligned} X_p &= 0; \\ R_L^2 + X_L(X_L + X_p) &= 0; \end{aligned} \tag{7.7}$$

These two equations, i.e. eqns.(7.6) and (7.7) have to be solved to obtain the GB of the generating set, i.e., eqns. (7.6) and (7.7), using the GB algorithm.

```
In[1]:= GroebnerBasis[{Rtot*(Rl^2+(Xl+Xp)^2)-Xp^2*Rl,
```

```
        Xp*Rl^2+Xl*Xp*(Xl+Xp)}, {Xp},{Xl},
        CoefficientDomain->RationalFunctions]
Out[1]= {-(Rl*Rtot^2*Xp^2) + (-Rl + Rtot)*Xp^4}
```

This gives the output in the function of R_L, R_{tot} and X_p. In order to specify a 'second' R_{tot} at another frequency, eqn. (7.6) has to be specified at another frequency, for example, ω_1. The resulting equation is then

$$R_{tot_b} = \frac{X_{p_b}^2 R_L}{R_L^2 + (X_{L_b} + X_{p_b})^2} \tag{7.8}$$

GB is then obtained for eqns. (7.6) and (7.8), as follows,

```
In[2]:= GroebnerBasis[{-(Rl*Rtot^2*Xp^2) + (-Rl + Rtot)*Xp^4,
        -(Rl*Rtotb^2*Xpb^2) + (-Rl + Rtotb)*Xpb^4},
        {Xpa,Xpb},{Rl},CoefficientDomain->RationalFunctions]
Out[2] = {-(Rtot*Rtotb^2*Xp^2*Xpb^2) +
          (Rtot^2*Rtotb - Rtot*Xp^2 + Rtotb*Xp^2)*Xpb^4}
```

Now, there are only the terms of the capacitance, or the inductance, in the parallel leg left to be found. By parameterizing either of the two terms, another one can be obtained easily by knowing the values of R_{tot}, R_{tot_b}, ω_0 and ω_1. Note that $X_p = \omega_0 L_p - \frac{1}{\omega_0 C_p}$ and $X_{p_b} = \omega_1 L_p - \frac{1}{\omega_1 C_p}$.

In order to get C_L and L_L, the GB on 7.7 at two distinct frequencies has to be found as follows,

```
In[3]:= GroebnerBasis[{Rl^2*Xp + (-(1/(Cl*w)) + Ll*w)*Xp*(-(1/(Cl*w)) +
        Ll*w + Xp),
        Rl^2*Xpb + (-(1/(Cl*wb)) + Ll*wb)*Xpb*(-(1/(Cl*wb)) +
        Ll*wb + Xpb)},
        {Xp,Xpb,Cl},{Ll}, CoefficientDomain->RationalFunctions]
```

In this case, the output given is a function of C_L, R_L, R_{tot}, R_{tot_b}, X_p, X_{p_b}, ω_0 and ω_1. This allows C_L and then L_L to be found. In short, the component values are obtained in the order of C_p, R_L, C_L and L_L with the pre-specified values of ω_0, ω_1, R_{tot}, R_{tot_b} and L_p.

Simulation Results

The frequency response of the resonant converter, given in Fig. 7.9, is depicted in Fig. 7.10.

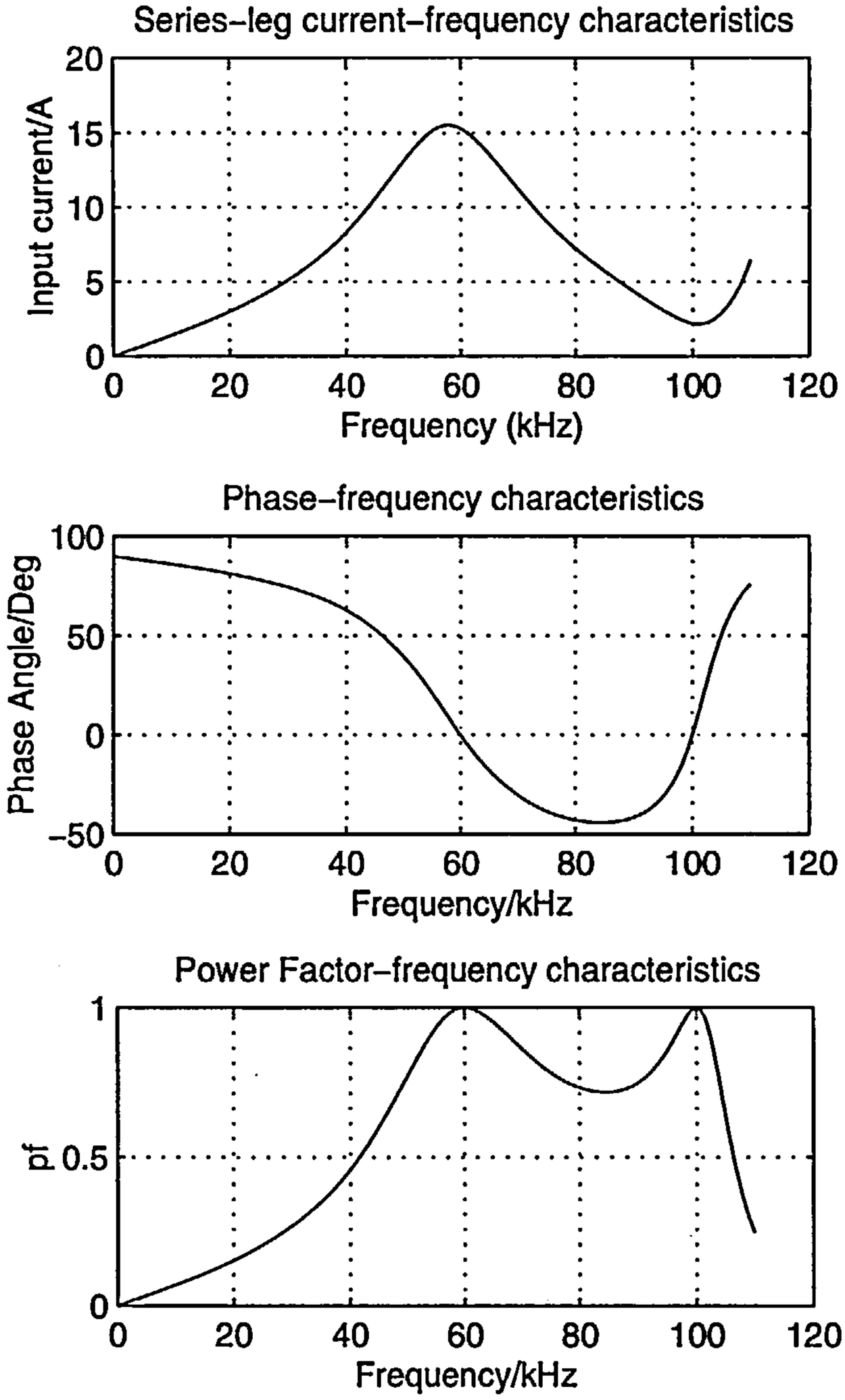

Fig. 7.10: Frequency response of the parallel load-resonant converter
$L_L = 59\mu H$, $L_p = 100\mu H$, $C_L = 0.123\mu F$, $C_p = 0.017\mu F$ and $R_L = 9.9\Omega$

From these plots, it can be seen that, the power change is as much as 1-to-7 with the two turning-point frequencies at $60kHz$ and $100kHz$, over which the power-factor ranges from $0.7 - 1$. This is achieved with only four passive elements. Note that, it is a two-resonant system as there are only two pairs of passive components used. Thus, the continuous-range for this system would be smaller, compared with Fig. (7.4) theoretically, if the parallel-load system were to be made continuous-resonant switching. In addition, it only has inherent open-circuit protection.

7.5.3 Summary

The number of components used in any resonant circuit must be balanced against degraded output performance and cost. The emphasis, whether on the performance or the cost, depends on

the judgment of the designers based on the clients' requirement of the applications. The parallel load-resonant converter shown here is just one example. There may be other topologies, or configurations, that can be used as well.

7.6 Conclusion

This chapter has shown different ways to modify the performance profile of the initial converter topology. Although these techniques were devised in isolation, they can be integrated in an interactive-computing design software; hence this produces a very flexible and powerful design tool to the designer based on the clients' requirements.

Chapter 8

Conclusions and Further Research

8.1 Conclusions

The thesis has discussed the basic features of most resonant converters with particular emphasis on the series-parallel load-resonant and quasi-resonant converters. Design techniques with applications were performed and verified theoretically and practically.

In recent years, resonant-switching techniques have started to receive serious attention due to desirable features that are lacking in conventional switching, although resonant-switching techniques give rise to some shortfalls too. Most of the current power converters are operated above resonance to maximize their performance. Owing to the advancement of semiconductor devices suitable for soft-switching, it is expected that the popularity of resonant-switching techniques will grow rapidly.

A detailed classification of resonant converters has been done successfully, and it is the most up-to-date and comprehensive coverage on resonant converters.

The limitation of the simultaneous-equation-design method in achieving variable output power control of load-resonant converters, while pre-specifying the major frequencies, was also identified. This was due to the non-linear characteristics of the system.

The Gröbner Basis theory was implemented successfully in designing load-resonant converters by pre-specifying the major frequencies to achieve variable-output-power control. More complex and general circuits were also developed based on the method. The method was shown to be capable of generating systems having good performance, but it also achieves this much quicker than the previous method. In addition, this new realization should, in the future, be seen to impact in a major way in applications of electrical network synthesis.

The simple control technique applied to an induction-drive system was demonstrated to be practically feasible. It is believed that interesting results would be obtained should more development be done.

Circuit-scaling theorems, continuous-resonance techniques, resonant-design curve and converter-topology modifications were introduced into the design process enabling prototype designs(via Gröbner Basis) to be easily modified and extended.

Other different design techniques were also produced to modify the complete design done by Gröbner Basis techniques to produce variant resonant converters operating at continuous multi-resonant frequencies, with the least possible component counts and highest output power sensitivity. All these techniques help alleviate the tedious mathematics and excessive computation involved in the re-design process.

8.2 Areas for further work

There are three areas of promise, arising from the work described in this thesis, i.e. output power control of resonant converters, Gröbner Basis capability in both power electronics applications and general electrical circuit analyses and integration of all the above-mentioned design techniques in interactive computing software.

8.2.1 Output-power control of resonant converters

The simple control techniques were done on both load-resonant converters and quasi-resonant converters for use in an arc-welding power supply and in an induction motor with a fan load respectively. Three-phase systems also seem to provide an opportunity for output-power control with the simple control techniques. In addition, by combining the load-resonant converter with the quasi-resonant converter, a direct cycloconverter may be obtained. Other applications like laser and sonar power supplies will surely be of interest.

8.2.2 Capability of Gröbner Basis in the engineering field

It is believed that the Gröbner Basis theory is rarely used in the power electronics field, in particular, and circuit theory areas, in general. Thus, the capability of the theory to be simplified and adapted for practical electrical engineering applications should be worth investigating. One immediate example, in the general circuit theory field, is to adopt the theorem in synthesizing circuit and

frequency responses. However, it can be used in almost any field in which polynomial manipulation, in particular, is required.

8.2.3 Software integration of design techniques

The above-mentioned design techniques, which were devised in isolation, could be integrated in interactive computing software for both commercial and research purposes. This would produce flexible and powerful design tools for the designers.

8.2.4 Other areas

As the frequency response is very sensitive to the value of passive components, a simple feedback control can be adopted to achieve optimum seeking of the frequency response curve. This avoids the difficulty in using passive components with practical tolerance.

One of the problems with resonant converters is increased size of the resonant tank. The overall weight and size of the resonant system can be further reduced if the resonant tank can be made smaller. One way to obtain this is to physically combine the passive components into one integrated component, and to push the operating frequencies as high as possible.

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