The Structural and Electrical Characterisation of SiGe Heterostructures Deposited on Strain Relaxed Virtual Substrates.

BY

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ABSTRACT.

The influence of lateral dimensions on the relaxation mechanism and the resulting effect on the surface topography of limited-area, linearly graded Si$_{1-x}$Ge$_x$ virtual substrates has been investigated for the first time.

A dramatic change in the relaxation mechanism of such buffer layers has been observed for depositions on Si mesa pillars of lateral dimensions of 10µm and below. For such depositions, misfit dislocations are able to extend, unhindered, and terminate at the edges of the growth zone. In this manner, orthogonal misfit dislocation interactions are avoided, yielding a surface free of the problematic surface cross-hatch roughening.

However, as the lateral dimension of the growth zone is increased to 20µm, orthogonal misfit interactions occur and relaxation is dominated by the Modified Frank-Read (MFR) multiplication mechanism. The resulting surface morphology shows a pronounced surface cross-hatch roughening. It is proposed that such cross-hatch roughening is a direct consequence of the cooperative stress fields associated with the MFR mechanism.

It is postulated that the method of limited-area, linearly graded buffer layers provides a unique opportunity, by which 'ideal' virtual substrates, free of surface cross-hatch and threading dislocations, may be produced to any Ge content.

In addition, a unique method by which the electrical performance of low temperature, strained layer depositions may be optimised is discussed. The method relies on the elimination of as-grown lattice imperfections via a post growth thermal anneal treatment. A 25-fold increase in low temperature hole mobility of a Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ heterostructure has been demonstrated using a 30-minute, 750°C in-situ, post growth anneal.
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SCFCTID.
DECLARATION.

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It is presented according to the Department of Physics guidelines (Phys/PG3). The work in this thesis is the result of my own research within the field, except where specifically acknowledged in the text.

Much of the work discussed in this thesis has been published and presented at several conference proceedings.

- Publications:


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1.1 INTRODUCTION.

In recent years the Silicon-Germanium/Silicon (SiGe/Si) heterosystem has attracted much interest within the area of high speed semiconductor device applications and remains, to this day, a 'hot topic' throughout the semiconductor research community worldwide.

Such interest is driven by the ability of the SiGe/Si heterosystem to incorporate the advantages of bandgap engineering, together with conventional, well established, silicon device fabrication techniques (Bean et al 1984).

Recent advances in ultra high vacuum (UHV) growth techniques, such as UHV-chemical vapour deposition (UHV-CVD) and molecular beam epitaxy (MBE) has made possible the growth of SiGe/Si heterostructures to an unprecedented degree of accuracy. Using such techniques it is now possible to grow high quality, defect free epilayers with monolayer interface resolution and compositions accurate to within a few atomic percent (Meyerson 1986).

Due to the inherent lattice mis-match of 4.2% between Si and Ge atoms, the strain derived from the growth of a 'thin' mis-matched epilayer results in a band edge discontinuity that may be employed to confine two-dimensional carrier gases (People et al 1985). The growth of a compressively strained SiGe epilayer results in a valence band discontinuity that enables the confinement of
holes, whilst a tensile strained Si epilayer grown on a relaxed SiGe 'virtual substrate' provides a conduction band discontinuity that may be employed to confine electrons.

By utilizing such band engineering techniques, superior transport properties for both electrons and holes have been reported. To date, record electron and hole mobilities of 500,000 cm$^2$/Vs, and 55,000 cm$^2$/Vs respectively have been demonstrated at 4.2K (Ismail et al 1993, 1994 and Xie et al 1994 respectively). In addition, and very significantly, the electrical properties of the SiGe/Si heterosystem have also demonstrated considerable improvements over conventional Si at room temperatures.

It is expected that the successful realization of both electron and hole quantum wells, with superior transport properties, will enable the monolithic integration of both n and p type SiGe devices on a single Si wafer.

1.2 ECONOMIC SIGNIFICANCE.

The expanding market for wireless and mobile communication systems has resulted in an ever increasing demand for low cost radiowave and microwave devices. Currently, the microwave domain of the semiconductor market is dominated by the III-V compound devices. In particular, the workhorse of the detection and transmission of radio frequency signals is the GaAs based metal semiconductor field effect transistor (MESFET) and the heterojunction field effect transistor (HFET). The low noise performance of the GaAs HFET and the extremely high electron mobility of the GaAs HEMT are unrivaled within the field of conventional Si devices.
However, the GaAs compound semiconductor system does have numerous shortcomings. In particular, the manufacture of large area GaAs wafers, of sufficient quality required for such high frequency applications, has proved problematic and costly. Presently, 'state-of-the-art' GaAs wafers are limited to a diameter of 4-5 inches, whilst many of the Si fabrication lines worldwide are currently converting to 12 inch wafer diameters. This fact alone creates a huge differential in both the device yield and the cost per chip between GaAs and Si components. These factors, in addition to the complexity of GaAs processing techniques, have provided significant barriers to the successful integration of complex monolithic microwave integrated circuits (MMICs) and digital GaAs circuitry. Furthermore, the poor hole characteristics of the GaAs system create difficulties for any complementary circuit functions.

The enhanced carrier mobilities and promising noise performance demonstrated by SiGe/Si based devices, has allowed them to compete favourably with the III-V material system in areas which require low power, high speed circuitry. Recently, SiGe HBT's which utilize the reduced base resistance of a strained SiGe base region, have demonstrated an excellent high frequency performance (Arafa et al 1996). The commercial availability of SiGe-based HBT circuitry is imminent with many companies, notably IBM, Daimler-Benz and Analog Devices close to commercial production. Indeed, an IBM-Analog Devices consortium have recently demonstrated a 12 bit, 1GHz digital-to-analog converter (DAC) based on the SiGe/Si heterosystem. The SiGe DAC runs faster than commercial 12 bit GaAs DAC's yet requires only a quarter of the power (J.A. McDonald 1994).
A further market sector into which SiGe-based devices may possibly encroach is that of digital Si circuitry. Currently, Si metal-oxide semiconducting devices (MOS) and Si complementary MOS (CMOS) are the dominant players for digital switching applications involving very large scale integration (VLSI). However, the inherent compatibility of the SiGe/Si heterosystem with the well established digital Si processing techniques, together with the enhanced electrical performance has created an impetus to further research in this area.

The first operational Si junction transistor was demonstrated in the early 1960’s and the flurry of activity in the subsequent years heralded the birth of the semiconductor electronics industry. In 1965 Moore published his now infamous paper in which it was predicted that the gate dimension of such devices would shrink by a factor of two every two years. The prediction became more familiarly know as ‘Moore’s Law’. As ultraviolet (UV) lithographic techniques matured, Moore’s Law was indeed observed to hold true and by 1984 the first 1µm gate length 1Mbit dynamic random access memory cell (DRAM) was commercially available.

However, it was long accepted that Moore’s device shrinkage law would soon meet its fundamental limits. Prior to 1985 all optical lithography was performed within the UV part of the spectrum. At such wavelengths diffraction effects limit the active device dimensions to approximately 1µm. The fundamental limit was temporarily avoided with the advent of deep UV lithography at 248nm wavelengths. Such techniques enabled further device shrinkage down to approximately 0.25µm. However, it is now generally
accepted that the fundamental limits of deep UV lithography are fast approaching.

In order to further increase the switching speed of conventional Si FET's a further reduction of the active gate lengths to $0.1\mu m$ and below is necessary. Further shrinkage would require a completely new lithographic technique. Recently, Lucent industries have developed an electron beam projection system (Berger et al 1995 and Pfeiffer et al 1995), whilst Intel are pursuing an extreme-UV technique at 130nm wavelengths (Stulen 1995) and IBM have opted for a proximity X-ray approach (Smith et al 1993 and Chen et al 1994). Other companies are also spending a great deal of time and resources in solving the problem of further device shrinkage, but an industry standard cannot be visualised in the near future. For a further insight into the future prospects of nanolithography the reader is referred to the excellent account offered by Taur (Taur et al 1997). However, the improved electrical performance of the SiGe/Si heterosystem may provide an alternative route to enhancing the switching speed of conventional digital circuitry, using well established deep UV processing techniques.

Furthermore, a significant enhancement in the packing density per CMOS wafer may be envisaged using the complementary modulation field effect transistor (CMODFET) proposed by Ismail (Ismail et al 1995 and Sadek et al 1995). Such a CMODFET device fully exploits the band engineering capabilities of the SiGe/Si heterosystem and relies upon the growth of a tensile strained Si channel spatially separated in the growth direction from a compressively strained high Ge content channel. The architecture requires the use of a relaxed, SiGe virtual substrate. Conventional Si-CMOS devices
require the use of separate n and p-channel devices (ie. requiring separate gates). However, the vertical architecture offered by the SiGe/Si CMODFET may be designed to operate under the bias of a single gate, thereby allowing a significant increase in the device packing density per CMOS die.

Presently, the Si based industry monopolises a 98% majority share of a semiconductor manufacturing market whose gross turnover is expected to reach 200 billion US dollars by the year 2000. The remaining share of the semiconductor market is primarily dominated by the GaAs based rf applications. Since SiGe/Si heteroepitaxial technologies offer, to a degree, possible advantages over both market sectors, research within the field remains a priority.

1.3 STATE OF THE ART.

To date, the most mature SiGe/Si heteroepitaxial device is the SiGe heterojunction bipolar transistor (HBT). The enhanced device performance of the SiGe HBT over conventional Si HBT’s may be attributed to the incorporation of a graded SiGe base region which may tolerate an increased doping level and also provides a ‘built-in’ electrical field which aids carrier motion. The increased doping differential between the base and emitter regions acts to reduce the base-emitter capacitance whilst also enhancing the device breakdown characteristics. Recently SiGe HBT’s have been demonstrated with a unity current gain cut-off frequency (f\text{t}) of in excess of 100GHz .

Presently, the research effort into SiGe majority carrier devices, such as field effect transistors (FET’s) is somewhat less mature. Whilst SiGe HBT’s
employ the growth of a strained SiGe layer grown pseudomorphically on a Si substrate, SiGe FET's generally require the use of a strain-relaxed virtual substrate. In order to produce the strain conditions required for electron confinement, a tensile strained Si channel must be grown on such a relaxed buffer layer. Similarly, in order to fully exploit the low effective mass inherent to Ge, a compressively strained high Ge channel may be grown on a relaxed buffer layer. In this manner two-dimensional hole confinement may be realised. Another approach employed to confine hole charge carriers relies upon the pseudomorphic growth of a thin, compressively strained SiGe channel on a Si substrate. However, due to the large strain energies involved, the Ge content of such pseudomorphic two-dimensional hole gases (2DHG's) is generally limited to a maximum Ge content of 40%. Theoretical considerations indicate that the optimum advantages of the SiGe/Si 2DHG heterosystem will be obtained at Ge contents in excess of 70-80% (Fischetti et al 1996). At such high Ge contents the low hole effective mass results in an appreciable increase in the hole mobility. In addition, the magnitude of the valence band offset scales with increasing Ge content allowing an increase in the density of confined charge carriers (Murakami et al 1994). A large sheet carrier density is a particularly important consideration for the current drive characteristics of p-FET's. However, energetic strain considerations again necessitate the use of a relaxed, virtual substrate in such high Ge content 2DHG heterosystems.

Theoretical considerations by O'Neill and Antoniadis predict f_t's in excess of 150GHz for a Schottky gated, 0.1µm n-type SiGe MODFET, whilst predictions for similar high Ge content SiGe p-MODFET's indicate an f_t in excess of 100GHz (A.G.O'Neill et al 1997).
Indeed, Arafa et al have demonstrated a $f_t$ of 70GHz for a 0.1µm self-aligned, Shottky gated, SiGe p-MODFET (Arafa et al 1996). The structure employed a strained 80% SiGe hole confinement channel grown by UHV-CVD on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate. Similarly, Ismail et al have demonstrated a peak room temperature transconductance of 390 mS/mm for Shottky gated 0.5µm SiGe n-MOSFETs, however no ac-device characteristics were presented (Ismail et al 1993).

It has been stressed that in order to fully exploit the SiGe/Si strained layer heterosystem the use of a relaxed, virtual substrate is a vital necessity. However, a method of producing such a high quality relaxed buffer layer has proved to be a formidable task to the SiGe research community. Generally, once a strained epilayer is grown above a certain 'critical thickness' energetic considerations result in the plastic relaxation of the epilayer due to the introduction of misfit dislocations. Strain relieving dislocations are formed along regions of slipped crystallographic planes which allow the growing epilayer to relax back to its unconstrained lattice parameter. However, it should be noted that the ends of a misfit dislocation cannot simply terminate within the bulk crystal- they must terminate at a non-crystalline boundary or they are required to annihilate each other with a similar misfit dislocation. Typically the strain relieving misfit dislocations originate at the epilayer/substrate growth interface and terminate at the growth surface in the form of threading dislocations.

A useful virtual substrate lattice parameter corresponds to that of a relaxed Si$_{0.7}$Ge$_{0.3}$ epilayer, since subsequent growth allows both the confinement of electrons within a tensile strained Si channel, together with the
possibility of hole confinement within a compressively strained, high Ge content, 2DHG channel.

However, in order to relieve the substantial strains associated with the SiGe/Si heterosystem a massive network of misfit dislocations is required. For instance, consider the relaxation of a SiGe epilayer grown on a 4 inch Si substrate. If the lattice mis-match between the epilayer and the substrate is 1% (corresponding to a Si$_{0.75}$Ge$_{0.25}$ film), then in order to achieve complete relaxation, a total misfit dislocation line-length in excess of 10$^6$ m is required. This corresponds to a dislocation line-length of 1000 km over a 4 inch wafer (Hull 1995). Such massive dislocation networks inevitably lead to orthogonal misfit dislocation interactions, which result in the generation of large quantities of threading dislocations. High densities of threading dislocations act as scattering centres which can hinder carrier motion.

The growth of an uniform pseudomorphic Si$_{0.7}$Ge$_{0.3}$ epilayer, which exceeds its critical thickness, typically results in a threading dislocation density of approximately 10$^{11}$-10$^{12}$ cm$^{-2}$. Such a threading dislocation density is far too high for even discrete applications, whilst current state of the art Si-CMOS requires wafers with defect densities in the range 1-100 cm$^{-2}$. A major breakthrough in the reduction of the threading dislocation density of relaxed buffer layers has been demonstrated by LeGoues et al (LeGoues et al 1994 and Fitzgerald et al 1991). The method employed the compositional grading of the Ge content of the epilayer. In this manner, misfit dislocations were spatially separated along different atomic planes of the epilayer. Furthermore, large dislocation pile-ups were observed which resulted in the annihilation of similar, self-aligned threading dislocations. In this manner, the threading
dislocation densities of relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrates were substantially reduced by several orders of magnitude and resulted in a final defect density of approximately $10^6$-$10^7$ cm$^{-2}$. However, the method of compositional grading requires the growth of a 'thick' epilayer, typically 2-5μm, which is both time consuming and expensive to produce.

A further mechanism by which the density of epilayer dislocations may be controlled is that of limited-area epitaxial growth. Fitzgerald et al have demonstrated a large reduction in the density of epilayer dislocations, within both the InGaAs/GaAs and the SiGe/Si heterosystems, for depositions on mesa defined, limited-area pillars or depositions within patterned oxide windows (Fitzgerald et al 1989). In this manner, elastic relaxation effects which occur at the edges of the strained layer growth zone, result in a decrease of the net strain within the growing epilayer. The mechanism has also been demonstrated by numerous authors (Noble et al 1990, Nishida et al 1993 and Stokia et al 1993).

1.4 THE WORK DESCRIBED IN THIS THESIS.

The research effort undertaken in this thesis attempts to further our fundamental understanding of the strained layer SiGe/Si heteroepitaxial system. In particular the work focuses on the structural characterisation of strain relaxed buffer layers and also investigates the electrical optimization of the two-dimensional hole gas system. It has been mentioned previously in this chapter how the use of a relaxed virtual substrate is a necessary requirement which allows the full exploitation of the strained layer SiGe/Si heterosystem. However, current state-of-the-art buffer layers suffer from a high residual
density of threading dislocations and have a significantly non-planar surface topography.

The effects of limited-area epitaxial growth of compositionally graded Si$_{1-x}$Ge$_x$, has been investigated by the present author (Hammond et al 1997). In this work a dramatic change in the relaxation mechanism of the growing epilayer was observed for limited-area depositions of lateral dimensions of 10µm and below. Due to the compositional grading, misfit dislocations were spatially separated on different atomic planes of the epilayer. For lateral dimensions in excess of 10µm, orthogonal misfit interactions occurred and the epilayer relaxation was dominated by the ‘modified Frank-Read mechanism’ typical of infinite-area, compositionally graded buffer layers. However, for depositions of lateral dimensions of 10µm and below orthogonal misfit interactions were avoided, allowing misfit dislocations to extend unhindered to the edges of the growth zone where they terminate at the non-crystalline boundary. By avoiding orthogonal misfit interactions a decrease in the number of misfit pinning events, which result in threading dislocations, is to be expected. Furthermore, the magnitude of the surface cross-hatch due to the deep dislocation pile-ups, inherent to the modified Frank-Read mechanism, was substantially reduced for lateral dimensions of 10µm and below (Lutz et al 1995).

Preliminary atomic force micrographs (AFM) of the surface topography of the limited-area depositions were performed by the author, at Warwick University. However, due to the difficulties encountered whilst precisely orientating the AFM tip on such small areas, it was determined that the use of an AFM/optical hybrid microscope was required. Such apparatus was available
at ETH Zurich and the author wishes to thank Thomas Graf for his invaluable contributions to this work. Unless otherwise stated, all work described in the present study was performed by the author, at the University of Warwick, UK.

Ideally, a continuation on the limited-area theme would have presented the effect of lateral dimensions on the electrical properties of two-dimensional carrier gases. Such work would have demonstrated the effects of surface cross-hatch on the mobility scattering mechanisms. Unfortunately, due to time constraints and complex fabrication issues involved in the electrical characterisation of such non-planar, limited-area buffer layers, work towards this goal must be left to subsequent researchers within this field.

However, the optimisation of the electrical characteristics of the SiGe/Si two-dimensional hole gas heterosystem, deposited on infinite-area relaxed buffer layers has also been investigated. A novel method of post-growth anneals has been proposed and the resulting electrical optimisation is discussed in terms of the structural integrity of low temperature MBE growth.

Chapter 2 discusses the experimental methods used throughout the course of this work. The reader is familiarised with the apparatus required for the molecular beam epitaxial growth of SiGe/Si heterostructures together with the experimental techniques used to characterise the samples, both structurally and electrically. The structural characterisation of limited-area, relaxed buffer layers is demonstrated in detail in chapter 3. Whilst, the techniques employed to optimise the electrical properties of high Ge content 2DHG’s are discussed in chapter 4. In each of these chapters the relative experimental results are discussed, conclusions are drawn and details of further investigations are presented. It should be stressed that all the conclusions that are discussed
throughout the documented research effort are based solely on the experimental results obtained.
CHAPTER 2.

EXPERIMENTAL METHODS.

2.1 INTRODUCTION.

The following chapter discusses the practical experimental methods used throughout the present investigation. In particular, a description of the molecular beam epitaxial (MBE) growth system is presented, together with a detailed discussion on the various experimental techniques employed to suitably characterise the SiGe heterostructures.

2.2 MOLECULAR BEAM EPITAXIAL GROWTH.

Molecular beam epitaxial growth of all heterostructures discussed in the present work was performed using a VG V90S system, developed by Vacuum Generators Ltd. in Maunsell UK. A schematic representation of the system is depicted in Fig 2.2.1. The system and its components are manufactured from either grade 316 stainless steel or from refractory metals. Typically, base pressures of $1 \times 10^{-11}$ mbar were achieved after a week long bakeout at 200°C. Background pressures of approximately $1 \times 10^{-8}$ mbar were sustained during
Fig 2.2.1
Schematic representation of the MBE V90S system used in the present work.
epitaxial deposition and residual gas analysis was performed throughout growth using mass spectroscopic techniques.

The MBE system incorporated a 'load-lock' wafer transfer chamber, allowing base pressures within the growth chamber to be maintained during wafer loading and unloading. Ultra High Vacuum (UHV) pumping was achieved using a combination of turbo pumps, getter-ion pumps, titanium sublimation pumps and liquid nitrogen cryopanels. For a more detailed account of the pumping system and an account of the importance of clean (oil-free) pumping during Si MBE growth the reader is referred to the work of Kubiak et al (Kubiak et al 1988).

Throughout the present work, Si/SiGe heteroepitaxial deposition was performed on clean n'-Si(100) substrates of 4 inch diameter. Prior to growth all substrates were pre-cleaned using a modified RCA wet chemical clean. Such cleans leave a residual surface oxide layer, typically of thickness <1.5nm. The oxide results in a passivated Si surface and was removed immediately prior to MBE deposition by raising the substrate temperature to 860°C, whereby the surface oxide desorbs, leaving a clean Si surface.

During growth, substrates were rotated at approximately 20rpm so as to ensure temperature and growth rate uniformity across the whole wafer. Radiative substrate heating was performed using a graphite heating element and temperature measurements were performed using an optical pyrometer operating at an infra-red wavelength of 1.1µm. In this manner substrate temperatures were determined to within a minimum absolute error of ± 25°C,
with a reproducibility of $\pm 5^\circ C$. Optical pyrometric thermometry has the distinct advantage of being an ex-situ, non-contact method, however at substrate temperatures below approximately 500$^\circ C$ the method is deemed unreliable due to the opacity of Si to infra-red radiation at such temperatures. Growth temperatures below 500$^\circ C$ were achieved by extrapolation of the heater power curve and resulted in an absolute substrate temperature error of approximately $\pm 40^\circ C$, again the reproducibility was estimated to be $\pm 5\%$.

Both Si and Ge deposition/co-deposition was performed using separate electron beam evaporators (e-guns) from solid source Si and Ge charges. Heated tungsten filaments, biased at high voltages, were used to produce an electron beam (e-beam) via thermionic emission. The e-beam was deflected through 270$^\circ$, using an electromagnetic coil, and directed onto the solid source charges. The incident e-beam flux resulted in the heating and subsequent evaporation of the Si and Ge charges. Both charges were water cooled and shielded from the copper hearths using Si crucibles. In this manner, any possible electron beam evaporation of copper contaminants was avoided.

Many of the parameters investigated in the present work are highly sensitive to both the Si and Ge flux rates. However, the relationship between e-gun power and the subsequent flux rate is non-linear and can vary by as much as 100% as the charge gradually depletes. The non-linear behaviour may be explained in terms of the effect of water cooling by the copper hearth as the charges are depleted. In order to obtain an accurate and reproducible growth rate, in-situ flux monitoring was performed during growth using Sentinel III
flux monitors, developed by Inficon NY, together with an electron impact emission spectroscopic (EIES) flux controller and feedback control. Such controllers operate by exciting the incident flux atoms with an electron beam. As the excited ions decay back to their ground states, light of a characteristic frequency is emitted. The intensity of the detected light is directly proportional to the incident flux rate. Using such a technique, individual growth rates may be controlled over a range 0.001 to 0.3 nms\(^{-1}\). In addition, the Si growth rate was calibrated using a surface profiler to determine the absolute epilayer thickness. Unfortunately, since the surface profiler requires relatively thick epilayers, the method cannot be used to calibrate the Ge flux rate due to the poor integrity of thick Ge films grown directly on Si substrates. Instead, Ge contents were calibrated using high resolution X-ray spectroscopy measurements of Si/SiGe superlattices which were grown at a pre-determined Si growth rate. In this manner, the reproducibility of Ge compositions was approximately ±10%.

*In-situ* boron doping was achieved by the co-evaporation of elemental boron from a resistively heated graphite crucible. High purity graphite was used and crucible temperatures in excess of 2200°C were obtainable. Using such a method, boron doping levels of 1x10\(^{20}\) cm\(^3\) were readily attainable. Furthermore, carbon background contamination from the crucible was below the detection limits of secondary ion mass spectroscopic (SIMS) techniques (approximately 1x10\(^{17}\)cm\(^{-3}\)). The boron flux rate was maintained using a constant current source, calibrated against control samples, and allowed doping
reproducibility of approximately ±20%. In all cases, growth rates, epilayer compositions and doping interrupts were achieved using microprocessor controlled shutters.
2.3 TRANSMISSION ELECTRON MICROSCOPY.

Cross-sectional transmission electron microscopy (XTEM) was performed on numerous heteroepitaxial depositions to determine the structural integrity of the epilayers. In particular, the technique was used to determine the dislocation microstructure of the relaxed epilayers.

Firstly, cross sectional specimens were prepared from wafer samples by cleaving orthogonal $<110>$ directions to an approximate sample area of 1x2cm$^2$. Generally, two specimens of each wafer were cleaved and the adjacent epilayers glued together using Araldite at a temperature of 80°C. The sample was then mounted between two Si support blocks (glued to the back of the original Si growth wafer), again using warm Araldite, and the sandwiched specimen clamped in a strong vice for approximately 24 hours so as to allow the glue to cure completely. The use of two adjacent epilayers increased the probability of successfully thinning the region of epilayer of interest. Also, great care was taken to ensure that all three glued interfaces were as thin as possible and that no particulates were sandwiched within the glue layers of the specimen.

The specimen was then mounted on a glass slide using melted wax and mechanically polished on one side using a successively finer grit size. A smooth, highly polished mirror surface was achieved by polishing the ground
sample, firstly using a 6µm diamond grit suspension followed by a light 1µm final polish.

3mm copper grids were then carefully glued onto the polished specimen so as to be central along region of interest. Again, the glue was allowed to cure for approximately 12-24 hours.

The specimen was then carefully removed from the glass slide by dissolving the wax in warm xylene. Using an identical method, the polished side of the sample, together with the mounted copper grids, was then mounted on a glass slide again using melted wax and mechanically thinned to a thickness of approximately 30-50µm. Again, a successively finer grit size was used so as to ensure a smooth surface was obtained. A smooth mirror finish was then obtained by polishing in a 6µm, followed by a 1µm, diamond suspension. The thinned specimen surrounding the copper disk was then carefully chipped away using a sharp scalpel.

Finally, the thinned specimen, together with the copper grids, was removed from the glass slide by dissolving the wax in xylene followed by a warm isopropanol clean.

In order to produce thinned samples, transparent to a high energy electron beam, the specimens were then milled in an argon ion beam until just perforated. The ion milling was performed at a base pressure of approximately 1x10^{-6} mbar, rising to approximately 6x10^{-4} mbar with the introduction of the argon gas. An accelerating potential of 5kV and a beam current of 4mA were used during thinning. For XTEM specimens ion milling was performed
simultaneously on both the front and backside of the specimen, with the incident ion beams at an angle of approximately 65° to the specimen normal. In addition, in order to achieve uniform thinning the samples were rotated at 1 r.p.m. during milling. Typically, ion beam thinning times varied from 2 hours to 24 hours, depending on the original specimen thickness.

Specimens were then characterised using a JEOL JEM-2000fx transmission electron microscope, operating at an accelerating voltage of 200kV.
2.4 VAN DER PAUW ELECTRICAL CHARACTERISATION.

The Hall mobility and sheet carrier densities of the modulation doped SiGe heterostructures, detailed in the present work were determined using Hall techniques employing a Van der Pauw sample geometry.

Ohmic contacts to cleaved specimens were prepared by the sputtering of aluminium dots through a shadow mask, to a thickness of 0.5µm, followed by a 30 minute sinter at 450°C in a nitrogen ambient. Typically the resistance of the resulting contacts was approximately 20-30kΩ at room temperature.

The Van der Pauw geometry was defined by painting a black wax cross, so as to connect four Al ohmic pads. The wax was allowed to dry and the Van der Pauw cross defined by etching the exposed heteroepitaxial region with a HF:HNO₃:CH₃COOH (3:5:5) mixture. An etch depth of approximately 3-4µm was used so as to ensure no parasitic electrical measurements were obtained from the underlying dislocation network of the linearly-graded buffer region. The black wax cross was then removed by boiling in xylene, followed by a vapour clean in isopropanol. In this manner, the contacts were made to the periphery of the specimen, in accordance with the optimum approach discussed by Van der Pauw and avoids errors typically encountered using a Hall bar geometry, such as mis-alignment of the Hall probes (Van der Pauw 1958). In addition, the technique is particularly useful in that no lithographic stages are required.
The temperature variation of the Hall mobility and sheet carrier density were determined from 4K to room temperature using a continuous flow, liquid helium cryostat. The measurement was partially automated with the use of a 486 IBM computer interfaced to a Keithley 705 Scanner (with a switching matrix card) via an IEEE488 interface card. The currents were supplied by a Keithley 224 programmable current source and the consequent voltages measured using a Keithley 182 digital nanovoltmeter. The Hall voltage across the sample was produced via an external magnet, of field strength 0.41T, orientated perpendicular to the specimen and measured using the Keithley 182 digital nanovoltmeter.

2.4 SECONDARY ION MASS SPECTROSCOPY (SIMS).

Both the Si and Ge profiles of the epilayers, together with any remote impurity doping, were determined using Secondary Ion Mass Spectroscopy (SIMS).

The SIMS technique employs a primary low energy ion beam to sputter the sample surface, whilst the emitted secondary ions are monitored. In this manner the elemental abundance of a particular species as a function of sputter depth may be ascertained.

All SIMS analysis detailed in the present work used a primary beam of $\text{O}_2^+$ ions, accelerated to a potential of 500eV using a floating low energy ion source. The sputtered secondary ions were then collected using an extraction
potential and the species identified using a quadrapole mass filtering system. The secondary ion count rate, and therefore the species concentration, was also measured using an ion detector. The base pressure of the specimen chamber was typically $1 \times 10^{-9}$ mbar.

Finally, the depth of the sputtered sample crater was determined using a surface profiler, enabling the elemental concentrations to be determined as a function of epilayer sputter depth.

All SIMS was carried out by the Advanced SIMS Projects group at the University of Warwick, UK using EVA 2000 SIMS profiler.

### 2.5 RAMAN SPECTROSCOPY.

The state of relaxation of the limited area epilayers detailed in the current work was determined using micro-Raman spectroscopy. The technique uses a focused laser beam to excite the Si-Si, Si-Ge and Ge-Ge bonds of the epilayer, whilst the backscattered spectra are collated and analysed. In particular, the technique is non-destructive and is especially useful in the determination of the state of relaxation of very small regions of the heterostructure.

Raman spectroscopic measurements were carried out at Toshiba Cambridge Research Centre, UK. The 488 nm line of an argon ion laser was focused to a spot size of approximately 2 µm using a microscope objective. All samples were cooled to liquid nitrogen temperatures and the spectra of the backscattered light collected using spectroscopic techniques.
Due to the absorption of the laser light in the SiGe heterostructure, the relaxation at a given epilayer depth may be accurately determined. Relaxation measurements were obtained by comparing the energy shift of the Si-Si, Si-Ge and Ge-Ge bond energies of the epilayers to similar infinite-epilayers whose state of strain was previously calibrated using standard X-ray diffraction techniques.
CHAPTER 3.

THE STRUCTURAL CHARACTERISATION OF
LIMITED-AREA, STRAIN-RELAXED Si\textsubscript{1-x}Ge\textsubscript{x}
EPILAYERS.

3.1 INTRODUCTION.

As alluded to in chapter 1, the interest in lattice mismatched semiconductor heteroepitaxy is due to the possibility of creating novel device architectures for both electrical and optical applications, together with the ability to integrate different material systems such as III-V and II-VI semiconductor compounds with existing silicon fabrication technologies.

Recently, intensive research within the field of Si\textsubscript{1-x}Ge\textsubscript{x}/Si heteroepitaxy has yielded many high performance device architectures such as high speed heterojunction bipolar transistors (HBTs) and enhanced performance field effect transistors (FETs). Indeed, strained layer heteroepitaxial Si\textsubscript{1-x}Ge\textsubscript{x} deposition has lead to room temperature electron and hole mobilities, confined within tensile strained Si channels and compressively strained Si\textsubscript{1-x}Ge\textsubscript{x} channels respectively, in excess of five times that of conventional Si-CMOS devices with comparable carrier densities (Nelson \textit{et al} 1993). The acceptable defect density depends, to some extent, on the actual device application. Certain majority carrier devices, such as FETs, can operate with a threading
defect density as high as $\sim 10^7 \text{cm}^{-2}$, whilst minority carrier devices typically require a defect density as low as $\sim 10^4 \text{cm}^{-2}$.

However, in order to fully exploit the Si$_{1-x}$Ge$_x$/Si(001) material system a method of obtaining high quality Si$_{1-x}$Ge$_x$ substrates relaxed to a given lattice parameter is essential. Such relaxed substrates (known as a ‘virtual substrate’) are generally obtained by depositing a thick Si$_{1-x}$Ge$_x$ buffer layer on a conventional Si substrate. Since the Si$_{1-x}$Ge$_x$ buffer layer exceeds a maximum thickness, known as the critical thickness, it relaxes via the plastic introduction of misfit dislocations (Hirth and Loathe 1982). However, in order to be suitable for ‘state of the art’ technological applications such virtual substrates must be thermally stable at device processing temperatures, have a surface morphology which is suitable for sub-micron lithography and have a low threading dislocation defect density in order to produce reasonable device yields. Furthermore, in order to keep manufacturing costs low and maintain a high throughput, the thickness of the epitaxial buffer layer must be kept to a minimum.

3.2. HETEROEPITAXY : THE ACCOMMODATION OF STRAIN

The deposition of an epitaxial layer on a substrate with an identical lattice parameter and a similar crystal structure is known as homoepitaxy. In such cases, depicted in Fig 3.2.1(a), the epilayer may, in principle, be grown to an arbitrary thickness since there are no energetic constraints.
Fig 3.2.1
(a) Homoepitaxial growth in which the epilayer lattice constant equals that of the substrate. (b) Pseudomorphic growth of a strained epilayer, in which the critical thickness is not exceeded. (c) Lattice mismatched growth in which the epilayer critical thickness is exceeded and relaxation occurs due to the introduction of an interfacial misfit dislocation array.
However, in the case of heteroepitaxial depositions the lattice mismatch between the thin epitaxial layer and the substrate may be accommodated by several mechanisms, which are discussed below.

i) ELASTIC DISTORTION OF THE ATOMIC BONDS WITHIN THE EPILAYER.

If the epilayer is thin enough (i.e. grown below the critical thickness) the strain energy due to the lattice mismatch may be accommodated via the elastic distortion of the atomic bonds within the epilayer. This configuration is depicted in Fig 3.2.1(b). In this case the in-plane lattice parameter of the epilayer, is elastically distorted so as to match that of the original substrate. In order to compensate for the in-plane distortion, the lattice parameter perpendicular to the growth interface is also deformed and results in a tetragonal distortion of the epilayer lattice. In the case of strained layer epitaxial growth of Si$_{1-x}$Ge$_x$ on Si(100) substrates (Si, Ge and Si$_{1-x}$Ge$_x$ have a diamond cubic lattice in their bulk, relaxed, unconstrained states) the tetragonal distortion of the strained layer modifies the band-edge discontinuity, enabling 2-dimensional electron and hole carrier confinement within strained layer quantum wells. The band structure of the strained layer Si$_{1-x}$Ge$_x$ system is dealt with in detail in section 4.2.
ii) PLASTIC RELAXATION DUE TO THE INTRODUCTION OF MISFIT DISLOCATIONS.

As the mismatched epilayer growth exceeds the equilibrium critical thickness it becomes energetically favourable to accommodate the large strain energies involved via the introduction of misfit dislocations at the epilayer/substrate interface. This is the prevalent mechanism for strain relief in the Si_{1-x}Ge_x/Si heteroepitaxial system under low strain. The interfacial misfit dislocation array allows the epilayer to relax towards its bulk unconstrained lattice parameter. It is important to mention that misfit dislocations cannot simply terminate within the crystal lattice: they must terminate at either a free surface, a non-crystalline boundary or be annihilated via the interaction with another specific dislocation. Generally, the two ends of the interfacial misfit dislocations terminate at the growth surface via threading dislocations. Such threading dislocations act as scattering centres within any subsequent carrier confinement channel and are thus detrimental to any possible device applications. It is therefore important to understand the origin of such misfit dislocations and attempt to control the threading dislocation density (Ismail et al 1994).

iii) ROUGHENING OF THE EPILAYER SURFACE.

A further mechanism by which the elastic strain energy associated with lattice mismatched heteroepitaxial films may be accommodated is via a roughening process which occurs at the growth surface. 'Ideal' epitaxial
growth occurs via a 2-dimensional process and is described in detail by the classic BCF model after the work of Burton, Cabrera and Frank (Burton et al 1951). In the BCF model epitaxial growth is modelled according to the processes occurring at the immediate growth surface and is described by the nucleation of 2-dimensional Si clusters. 2-dimensional growth is then described by the diffusion of surface adatoms (migration) towards the step edges of the 2-dimensional clusters together with the capture of the migrating adatoms at the step edges (incorporation). In this way the clusters continue to grow laterally, confined to 2-dimensions, until adjacent clusters merge to create a 2-dimensional film one atomic monolayer thick. Growth then continues due to the nucleation of subsequent two-dimensional clusters. This mechanism is theoretically predicted and experimentally observed within the Si$_{1-x}$Ge$_x$/Si heteroepitaxial system at low growth temperatures and low lattice mismatch.

However, at increased growth temperatures and high epilayer mismatch relaxation of the strained epilayer may occur due to the onset of surface roughening. This mechanism is schematically depicted in Fig 3.2.2(a) and is supported by the bright field [110] cross-sectional TEM image of Fig 3.2.2(b), in which a 8nm strained Si$_{0.5}$Ge$_{0.5}$ epilayer is deposited on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate at a growth temperature of 600°C. The mechanism by which relaxation occurs via surface roughening is due to the nucleation of 3-dimensional islanding (Cullis et al 1996). Consider the growth of the compressively strained epilayer depicted in Fig3.2.2(a). Under 2-dimensional growth conditions the epilayer bond lengths are constrained to that of the relaxed substrate (provided that the critical thickness is not exceeded). However, with the onset of 3-dimensional islanding the epilayer lattice bond
Fig 3.2.2
Schematic representation of strain relaxation due to epilayer roughening (a). Cross-sectional TEM micrograph of an 8nm compressively strained Si$_{0.5}$Ge$_{0.5}$ channel deposited at 600°C on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate (b).
lengths at the peak of the 3-dimensional island relax towards that of their unconstrained bulk states. Hence, during 3-dimensional islanding of Si$_{1-x}$Ge$_x$ epilayers, the larger Ge atoms have a tendency to migrate towards the island peaks. This situation is clearly energetically favourable since it results in a decrease in the total energy of the system.

The roughening of the epilayer during growth results in a major scattering mechanism which hinders carrier motion. Furthermore, the preferential Ge segregation towards the 3-dimensional island peaks, result in a periodic bandgap fluctuation. Such a bandgap fluctuation may be realised as a pseudo-potential which is super-imposed upon the confining band-offset and again acts as a scattering mechanism.

It should be noted that the lateral, peak to peak roughening which occurs during growth is generally of the order of 100nm. At low temperatures, this distance is approximately equal to the magnitude of the Fermi wave-vector for charge carriers and thus acts as a major scattering mechanism at low temperatures. On the other hand, the 'cross-hatch' roughening, which is generally associated with the strain relieving dislocations of the buffer layer, has a lateral peak-to-peak separation of the order of microns and is generally not responsible for charge carrier scattering events (Emeleus et al 1992).
3.3 INTRODUCTION TO BASIC DISLOCATION THEORY.

In this section a basic review of the theory of dislocations is undertaken. For a more thorough analysis the reader is referred to the work of Hirth and Loathe (Hirth and Loathe 1982).

Si, Ge and Si$_{1-x}$Ge$_x$ all possess the diamond cubic lattice structure in their unconstrained states. Dislocation extension occurs along specific crystallographic directions whose minimum energy configurations are determined by the Peierls stress (Peierls 1940). Within the diamond cubic system the widest spaced atomic planes, and hence the lowest energy bonds, are the $\{111\}$ sets of atomic planes. Therefore, dislocation glide generally occurs along these planes. The present work involves Si$_{1-x}$Ge$_x$ growth on Si(001) substrates. In this case the four possible $\{111\}$ glide planes intersect the (001) interface along orthogonal in-plane [110] and [1-10] directions. Misfit dislocation segments are generally orientated along these directions with a pair of $\{111\}$ glide planes intersecting each of the in-plane directions. A schematic representation of the system is depicted in Fig 3.3.1(a).

A perfect or total dislocation is a line defect bounding a slipped region of the crystal lattice. The Burgers vector $b$ of a dislocation may be defined as the closure vector of a crystalline circuit drawn clockwise around the slipped region of the crystal. The mechanism is shown in Fig 3.3.1(b). Equivalently, the dislocation Burgers vector $b$, may be defined as the line integral, taken in a right-handed sense relative to the dislocation line direction, of the elastic displacement $\mathbf{u}$ around the dislocation. Whereby,
Schematic representation of the atomic planes involved in dislocation glide within both the Si and SiGe lattice system (a). Cross sectional schematic view of dislocation core, indicating the Burgers vector $b$ of the dislocation (b).
\[ b = \frac{\partial x}{\partial l} \]

Where, \( l \) is the dislocation line length and \( c \) is the dislocation closure circuit.

The character of a dislocation may be classified depending upon the angle between the Burgers vector of the dislocation and its line direction \( u \). If \( b \) is parallel or anti-parallel to \( u \) then the dislocation is of screw character. If \( b \) is perpendicular to \( u \) then the dislocation is of edge character. A dislocation is said to be of mixed character for intermediate configurations.

The Burgers vector of a dislocation must remain constant throughout its length, however its line direction may vary. Therefore the character of a non-linear dislocation will vary along the length of the dislocation.

The Burgers vector of a perfect dislocation is a lattice translation vector. Since the self energy of a dislocation is related to the square of its Burgers vector, it is energetically favourable for the Burgers vector to equal the shortest lattice translation vector. Within the diamond cubic system the shortest lattice translation vector is of the \( a/2<101> \) type, where \( a \) is the lattice parameter. For a given \{111\} glide plane three such Burgers vectors exist. Hence for the diamond cubic lattice system the total number of Burgers vectors are limited to twelve. For instance, consider the (-111) glide plane depicted in Fig 3.3.1. The three possible Burgers vectors are given as \( b = a/2[110], a/2[101] \) and \( a/2[01-1] \). In this case the \( a/2[110] \) and \( a/2[101] \) dislocations are known as 60°-type dislocations, due to the angle made between \( b \) and \( u \). These dislocations are the most important in Si\(_{1-x}\)Ge\(_x\)/Si(001) system since their Burgers vectors lie within a \{111\} glide plane. Such 60°-type dislocations are therefore relatively free to
glide due to the force exerted from the elastic strain of the mismatched epilayer. Hence, 60°-type dislocations are primarily responsible for strain relief within the Si$_{1-x}$Ge$_x$/Si(001) system. The latter case is a screw dislocation and does not experience any lattice mismatch stress and is therefore not responsible for strain relaxation. The present work involves only 60°-type dislocations.

3.4. MATTHEWS-BLAKESEE THEORY OF EQUILIBRIUM CRITICAL THICKNESS.

The critical epilayer thickness for a lattice mismatched heterostructure may be derived following two separate approaches. The first approach, developed by Van der Merwe and co-workers, relies upon energy balance considerations in which the total energy of the interfacial dislocation array may be equated to the reduction in the elastic strain energy of the mismatched epilayer (Van der Merwe 1963 and Jesson et al 1988). A further, more intuitive, approach was developed by Matthews and Blakeslee (Matthews 1975 and Matthews et al 1976). The Matthews-Blakeslee (MB) analysis equates the net force required to form the first misfit segment at the growth interface to the elastic strain energy of the lattice mismatched epilayer.

Both formulations derive similar expressions for the equilibrium critical thickness of a strained epilayer, however the approach used in this work is based on the MB force-balance framework developed from mechanical equilibrium theory. For a more detailed review of equilibrium critical thickness considerations the reader is referred to the works of People and Bean (People et

Consider a pre-existing threading dislocation in the substrate. Generally such dislocations have to terminate at a free surface, which is usually the growth surface. As the strained epilayer continues to grow the threading component experiences an applied force $F_a$. This force results from the lattice mismatch of the epilayer and is depicted in Fig 3.4.1(a). As growth continues the elastic strain energy of the epilayer gradually increases until the applied force on the threading dislocation is sufficient to cause it to glide along the substrate/epilayer interface, creating a misfit segment which will relax the epilayer in the immediate vicinity of the misfit. Inherent to the misfit segment is a self-energy arising from the strain fields within the surrounding 'distorted' crystal lattice. This self-energy is often referred to as the 'line tension' of the dislocation and exerts a restoring force $F_t$ on the propagating threading arm (see Fig 3.4.1(b)). At the condition $F_a > F_t$ the excess strain causes the original threading component to glide and results in the formation of a misfit dislocation segment at the substrate/epilayer interface. This situation is depicted schematically in Fig 3.4.1(c).

The MB equilibrium critical thickness $h_c$ may be defined at the condition $F_a=F_t$. The dislocation in-plane lattice mismatch stress $\sigma_o$, may be obtained from standard isotropic elasticity theory and is defined:

$$\sigma_o = 2G\varepsilon \frac{(1+\nu)}{(1-\nu)} \quad (3.4.1)$$
Fig. 3.4.1(a)
Forces acting upon a strain relieving dislocation at the Si/SiGe interface. (a) epilayer thickness $h$, is less than the Mathews Blakeslee critical thickness $h_c$, and results in a pinned threading segment in which the restoring force $F_t$ exceeds the excess force $F_a$ acting upon the dislocation. (b) The condition $F_t = F_a$ defines the Mathews Blakeslee critical thickness. (c) The excess force $F_a$ exceeds the restoring force $F_t$ causing dislocation extension along the interfacial plane and resulting in a strain relieving misfit segment.
where $G$ is the epilayer shear modulus, $\varepsilon$ is the lattice strain and $\nu$ is the Poisson ratio.

The resolved lattice mismatch stress $\sigma_a$ experienced by the threading arm of the misfit dislocation, of Burgers vector $b$, may be derived from the component of the applied stress resolved onto the dislocation Burgers vector and the dislocation glide plane. The resolution factor is known as the Schmid factor $S$:

$$S = \cos \lambda \cos \phi$$  \hspace{1cm} (3.4.2)

Here, $\lambda$ defines the angle between the dislocation Burgers vector and the direction in the substrate/epilayer interface which is normal to the dislocation line direction. The angle $\phi$ is defined as the angle between the dislocation glide plane and the interface normal. Thus, the applied stress experienced by the dislocation is given by:

$$\sigma_a = 2G\varepsilon \frac{(1+\nu)}{(1-\nu)} \cos \lambda \cos \phi$$  \hspace{1cm} (3.4.3)

Assuming that the threading dislocation takes the shortest path along its glide plane from the substrate/epilayer interface and the free growth surface, then the length $L$ of the threading arm is $h/\cos \phi$, where $h$ is the epilayer thickness.

The applied force $F_a$, may be defined as:
\[ F_a = \sigma_a b L \]  
(3.4.4)

Hence,

\[ F_a = 2Gbh \frac{(1+\nu) \cos \lambda}{(1-\nu)} \]  
(3.4.5)

The dislocation line tension \( F_t \), may be derived from the energy required to create an interfacial misfit segment:

\[ F_t = \left( \frac{Gb^2(1-\nu \cos^2 \theta)}{4\pi(1-\nu)} \right) \ln \left( \frac{ah}{b} \right) \]  
(3.4.6)

where, \( \alpha \) is the dislocation core parameter, and \( \theta \) is the angle between the dislocation Burgers vector and its line direction.

Hence, at the condition \( F_a = F_t \), the MB critical thickness \( h_c \) may be defined:

\[ h_c = \frac{b(1-\nu \cos^2 \theta)}{8\pi(1+\nu) \varepsilon \cos \lambda} \ln \left( \frac{\alpha h}{b} \right) \]  
(3.4.7)

Fig 3.4.2 shows the variation of the MB critical thickness as a function of Ge content for an uncapped \( \text{Si}_{1-x}\text{Ge}_x \) epilayer deposited on Si(001) (after Iyer et al 1989). It should be noted that equation (3.4.7) does not have an analytical solution but may be solved numerically. Also shown in Fig 3.4.2 are comparable experimental data of critical thickness measurements from several groups.
Fig 3.4.2.

Graph of critical layer thickness as a function of Ge content for a strained Si$_{1-x}$Ge$_x$ epilayer grown on a Si(100) substrate, after (a) People et al (1986), (b) Matthews et al (1976) and (c) the theoretical calculations of Van der Merwe et al (1963).
However, it should be noted that at low growth temperatures, the agreement between experimental and theoretical data increasingly diverges. This is due to a metastable regime within the epilayer growth. The equilibrium critical thickness is defined at the onset of dislocation glide. The propagation of dislocations requires shearing of atomic bonds at the heterointerface. This requires dislocation nucleation and propagation activation barriers to be exceeded. At low growth temperatures these mechanisms are kinetically limited and the epilayer growth thickness may exceed the equilibrium critical thickness without plastic relaxation occurring. However, plastic relaxation of such metastable epilayers can occur upon post-growth annealing.

3.5 THE ORIGIN OF THREADING DISLOCATIONS.

In order to fully exploit the Si_{1-x}Ge_x material system an important parameter, which is necessary to control, is the density of threading dislocations. Threading dislocations generally arise due to the interaction of two orthogonal misfit segments.

Consider the case of a uniform Si_{1-x}Ge_x epilayer grown beyond its critical thickness on a Si(001) substrate. A [110] misfit segment may elongate via the glide of its threading arm along a {111} glide plane. Misfit extension arises due to the excess strain within the epilayer. At some point the threading arm of the extending [110] misfit will encounter a pre-existing orthogonal misfit dislocation (i.e. a [1-10] misfit segment) on the same atomic plane. If the excess stress driving the extension of the [110] misfit is not sufficient to overcome the stress field associated with the pre-existing [1-10] misfit
segment, then the threading arm of the [110] segment will become energetically pinned at this point indefinitely. As relaxation of the epilayer continues the excess strain driving the extension of misfit segments gradually reduces. In the latter stages of strain relaxation this inevitably leads to a high density of pinned threading components. Indeed, in the case of a uniform Si$_{0.7}$Ge$_{0.3}$ epilayer grown beyond its critical thickness the residual threading dislocation density is typically of the order of $10^{12}$ cm$^{-2}$. Such a density is far too high to envisage any possible device applications.

3.6 DISLOCATION NUCLEATION SOURCES.

Misfit dislocation nucleation sources may be conveniently grouped into two categories. The first results from nucleation sources which are inherent to the system and are known as homogeneous nucleation sources. Whilst, the second are known as heterogeneous nucleation sources and derive from sources which are not native to the system. A further mechanism is that of dislocation multiplication. Each category will be dealt with separately.

3.6.1 HETEROGENEOUS NUCLEATION SOURCES.

Examples of heterogeneous nucleation sources include pre-existing threading dislocations originating from within the epitaxial growth substrate, impurity precipitates, which occur during growth and create strain fluctuations within the growing mismatched epilayer. Another major nucleation source arises from the incomplete cleaning of the original substrate prior to growth.
This may result in precipitates, such as oxides and carbides, inducing localised strain fluctuations (Perovic et al 1989). The magnitude of such strain fluctuations increase during epilayer deposition and may eventually overcome the kinetic barriers required for misfit nucleation. Metallic contaminants act in a similar manner (De Coteau et al 1992). Indeed, 'flaking' of the Si coating which builds up on the walls of the growth chamber can cause poly-Si inclusions within the epilayer which also act as heterogeneous nucleation sources.

However, with 'state of the art' facilities such sources are controllable, to a degree, and it is generally accepted that such heterogeneous sources are not the major cause of epilayer relaxation.

### 3.6.2 HOMOGENEOUS NUCLEATION SOURCES.

The large elastic energies stored within a lattice mismatched epilayer can eventually overcome the kinetic barriers associated with misfit dislocation nucleation. This subject has been dealt with in detail by Frank and Hirth, who propose that misfit nucleation may be induced into a defect free epilayer via the introduction of half-loops from the growth surface (Frank 1950 and Hirth 1963).

However, in recent years many groups have re-examined the generation of surface half-loops within the Si$_{1-x}$Ge$_x$ system and it has been demonstrated that for strains of less than approximately 4% the energy required to induce a surface half-loop is generally unattainable at typical Si$_{1-x}$Ge$_x$ growth temperatures (Eaglesham et al 1989 and Fitzgerald et al 1989).
In section 3.2(iii) the effect of surface roughening as a mechanism to aid strain relief in a mismatched epilayer was discussed. At mismatches of approximately 1-2%, the large stress concentrations associated with the highly non-planar surface morphology of the epilayer may provide a method by which the kinetic limitations governing the formation of misfit dislocations may be overcome. The strain field associated with a misfit segment induced in this manner causes the 3-dimensional islands of the non-planar epilayer to align along the direction of the dislocation line segment. The high stress fields involved enable further misfit segments to nucleate, thereby increasing the relaxation process. The mechanism of misfit injection from the stress fields associated with a non-planar, ‘rippled’ epilayer has been dealt with in detail by Jesson (Jesson et al 1996).

3.6.3 DISLOCATION MULTIPLICATION MECHANISMS.

The most intuitive candidate for a source mechanism, which has the ability to produce large numbers of misfit dislocations, is a multiplication mechanism. Hagen and Strunk proposed a regenerative mechanism based upon the annihilation of two orthogonal misfit interactions which results in the creation of two corner dislocations (Hagen et al 1978). Due to the repulsive nature of the similar corner dislocations, one of the corners is forced to intersect the surface, allowing the creation of two threading components, which may continue to glide and form two separate misfit segments. However, several authors have questioned the validity of such a mechanism and, to the best of the present author’s knowledge, no convincing experimental evidence
of the Hagen-Strunk multiplication source has been demonstrated within the SiGe/Si heterosystem. (Eaglesham et al 1989, Lefebvre et al 1991 and Hull 1997).

In addition, several authors have proposed further dislocation multiplication mechanisms based on the cross pinning of a single misfit dislocation by two spatially separated, orthogonal misfit dislocations. Such a mechanism was proposed by Tuppen et al, whereby the increasing strain energy acting on the pinned misfit gradually increases during strained layer growth and causes the pinned segment to bow (Tuppen et al 1990). Eventually the bowing results in the pinned region intersecting the surface whereby two threading segments are produced. Each threading segment may then glide and create two further misfit segments.

A further multiplication mechanism, known as the 'Modified Frank-Read Mechanism', has been proposed by LeGoues and is primarily responsible for the relaxation of compositionally graded buffer layers (LeGoues et al 1991 and 1992). The mechanism is described in detail in section 3.7.1.

3.7 MISFIT AND THREADING DISLOCATION REDUCTION TECHNIQUES.

As mentioned in section 3.5 a mechanism by which strain-relaxed Si$_{1-x}$Ge$_x$ virtual substrates may be obtained to any Ge content is highly sought after. In theory, the 'ideal' virtual substrate would consist of a Si$_{1-x}$Ge$_x$ epilayer grown above its critical thickness on a Si(001) substrate. In order to relax the epilayer, misfit dislocations must be generated. Ideally, these misfit segments
would transverse the entire width of the substrate, whereby they could terminate at the wafer edges without leaving any residual threading dislocations. However, as described in section 3.5, orthogonal misfit pinning events prevent complete misfit extension across the substrate and result in an unacceptable density of threading components. The problem has been addressed by many workers and partial solutions have been demonstrated.

A very promising approach is that of compositionally grading the Ge content as a function of epilayer thickness. This method was demonstrated by LeGoues et al and resulted in a reduction in the threading dislocation density of the order of 6-7 orders of magnitude compared to that of a similar uniform deposition (LeGoues et al 1991).

A further approach is that of limited-area epitaxy (i.e. growth on mesa pillars or within oxide windows). This method was originally demonstrated within the InGaAs/GaAs(100) system by Fitzgerald (Fitzgerald et al 1989). By reducing the lateral dimension of the growth zone the probability of an extending misfit segment encountering a pre-existing orthogonal misfit is reduced. Hence, due to the reduction in orthogonal misfit pinning events a reduction in the density of threading dislocations is to be expected.

Each of these important methods of reducing the threading dislocation density will now be addressed in turn, together with a number of similar reduction techniques.
3.7.1 COMPOSITIONALLY GRADED BUFFER LAYERS - THE MODIFIED FRANK-READ MECHANISM.

A comprehensive study of the effect of compositional grading of the Ge content in a $\text{Si}_{1-x}\text{Ge}_x$ epilayer has been undertaken by LeGoues (LeGoues et al 1991, 1992(a) and (b)). Generally, the Ge content of the buffer layer is increased linearly as the epilayer is deposited. In this manner the strain energy of the mismatched epilayer is distributed uniformly throughout the linearly graded region. This results in misfit nucleation occurring upon different atomic planes within the linearly graded region.

In the case of a uniform $\text{Si}_{1-x}\text{Ge}_x$ epilayer grown above its critical thickness, the majority of misfit dislocations nucleate at the substrate/epilayer interface. This creates a large number of orthogonal misfit pinning events, which result in a massive density of threading dislocations.

However, in the case of a linearly-graded $\text{Si}_{1-x}\text{Ge}_x$ epilayer misfit extension occurs along different atomic planes. This mechanism provides an extra (vertical) degree of freedom for misfit dislocations to propagate past each other. In this manner the number of orthogonal misfit pinning events is reduced. Hence, misfit dislocations may extend laterally a much greater distance and the resulting threading dislocation density is dramatically reduced.

An important parameter to consider is the rate of compositional grading. An infinite grading rate corresponds to uniform deposition and results in a massive threading dislocation density. Whilst a grading rate of zero would result in a defect free virtual substrate but is practically unrealistic.
Typically, the grading thickness of such linearly-graded virtual substrates varies from pure Si to an atomic fraction of 30% Ge over 2-5 microns and results in a threading dislocation density of approximately $10^5\text{cm}^{-2}$. This represents an improvement of 6-7 orders of magnitude over a similar uniform deposition. However, such linearly-graded buffer layers are both time consuming and expensive to produce due to their thickness.

The mechanism by which relaxation occurs in such linearly-graded buffer layers is known as the 'Modified Frank-Read (MFR)' mechanism. A brief explanation of the MFR mechanism is given here, however for a more comprehensive description the reader is referred to the work of LeGoues et al and Fitzgerald (LeGoues et al 1991, 1992(a and b) and Fitzgerald et al 1991).

At the relatively low mismatch stresses in question, misfit nucleation is limited due to the sparse density of heterogeneous sources and homogeneous nucleation is not applicable. The MFR mechanism is a regenerative multiplication source, which results in the nucleation of many misfit dislocations on different atomic planes within the linearly-graded region of the buffer layer.

Consider an 'original' extending misfit dislocation $D_1$, which has nucleated at some heterogeneous source and intersects a pre-existing orthogonal misfit dislocation $D_2$ upon the same atomic plane. Both dislocations must possess identical Burgers vectors. A schematic representation of the system is depicted in Fig 3.7.1(a). Such a configuration is unstable and results in the annihilation of the misfit segments, creating two corner dislocations, $C_1$ and $C_2$ (Lefebrve et al 1991). Since the two dislocations are of the same Burgers vector repulsive forces exist between the two corner
Fig 3.7.1(a).

Fig 3.7.1(b).

Fig 3.7.1.
Schematic representation of the modified Frank-Read (MFR) dislocation multiplication mechanism. (a) and (b) depict a cross sectional view of the initial orthogonal misfit interaction and the resulting dislocation pile up respectively.
Fig 3.7.1.
Plan view schematic of the initial ‘self-aligned’ MFR interaction (c) and the planar microstructure resulting from the annihilation of multiple interactions (d).
dislocations, causing one to bow into the substrate (C1) whilst the other corner dislocation (C2) remains pinned. As growth continues, the excess strain forces C1 further into the substrate along a \{111\} glide plane and results in the formation of a dislocation half loop. The half loop gradually expands simultaneously along the original glide planes of D1 and D2 and eventually reproduces the original corner dislocation C1'. Once the expanding half-loop intersects the growth surface, it forms a pair of threading dislocations. These threading components are then free to glide away form the original misfit intersection along their individual glide planes, resulting in the formation of two misfit segments M1 and M2 (see figure 3.7.1(b)).

However, the repulsive force between the newly formed corner dislocation C1' and the original pinned corner dislocation C2 again forces C1' to bow into the substrate. By the same process, a half-loop is formed and the mechanism repeats. In this way another pair of orthogonal misfit segments, M1' and M2', may be formed which extend away from the original misfit intersection. It is important to note that the MFR mechanism revolves around numerous dislocation pile-ups penetrating deep into the Si substrate which all occur along a single unique direction.

Furthermore, each pile-up results in the formation of a pair of orthogonal misfit segments. Each of these misfit pairs (i.e. M1, M2 and M1', M2') lie along a given lateral atomic plane and are spatially separated in the growth direction from those generated in the next pile-up. A schematic view of the resulting dislocation microstructure is depicted in Fig 3.7.1(b).

Subsequent analysis by LeGoues has demonstrated that the reduction in the total threading dislocation density of MFR relaxed buffer layers is due to
the annihilation of threading components from ‘self-aligned’ MFR sources (LeGoues 1994). Such self-aligned sources provide each threading dislocation with a matching threading component from another source and since the respective Burgers vectors are non-similar, each threading component may then annihilate each other. Fig 3.7.1(c) represents a plan view of three independent MFR sources. Consider source A to be the first to operate, misfit segments along [110] and [1-10] directions may travel ‘indefinitely’ since no strain has been relieved. As source B becomes operational, misfit segments along [110] may also travel long distances since they propagate through a strained region of the epilayer. However, the threading arms of the [1-10] misfits have to propagate through a region of the lattice which is already relaxed due to the activity of source A, hence these threading components become pinned. Similarly, the threading arms of the [110] misfit dislocations, created at source C, also become pinned at source A. However, the pinned threading segments created at sources B and C have anti-parallel Burgers vectors. Such dislocations are mutually attractive and result in the annihilation of the threading components at the ‘self-aligned’ source A. A plan view of the final dislocation network is shown in Fig 3.7.1(d).

3.7.2 COMPLIANT SUBSTRATES.

An alternative approach to obtaining a high quality, relaxed virtual substrate is to employ the use of a compliant substrate. In this manner, the lattice mismatch strain between the epilayer and the substrate is taken up by the compliant substrate, resulting in all the strain relieving misfit dislocations, and
their corresponding threading components, being confined to the compliant buffer layer. Dislocations which terminate in this manner do not interfere with any subsequent electrical confinement channel.

The two compliant substrates most commonly used within the SiGe/Si heterosystem are silicon on insulator (SOI) and silicon on sapphire (SOS). Both systems require the physical bonding of a silicon substrate to a silicon dioxide or a sapphire wafer respectively. The Si is then ‘etched back’ to a thickness of around 10nm, thus forming the compliant substrate, and any subsequent Si$_x$Ge$_{1-x}$ layer deposition results in strain relieving misfit segments penetrating into the compliant substrate.

However, the technique has proved problematic due to the practical difficulties encountered in the production of a thin, single crystal Si film. For a more detailed introduction to the use of compliant or plastic substrates the reader is referred to the article “Substrate Engineering with Plastic Buffer layers” by Leo J. Schowalter, MRS Bulletin, p 45-49, April 1996 and the references therein.

3.7.3 STRAINED LAYER SUPERLATTICES

A further approach by which ‘ideal’ virtual substrates may be realised was proposed by Matthews and utilises the use of strained layer superlattice dislocation filtering (Matthews 1975). The method relies on the growth of a buffer layer, grown slightly above the critical thickness, followed by a thin, strained layer. The growth structure is then repeated, with an increasing Ge content sandwiched between the strained layers. In this manner, threading
dislocations arising from the original buffer layer film encounter a series of strained layers. The excess force due to the strained layers causes the threading components to glide along the strained layer interface, whereby they eventually terminate at the wafer edges.

However, such structures are generally of the order of microns thick and again are both time-consuming and expensive to produce.

3.7.4 SUBSTRATE PATTERNING GEOMETRIES.

A novel method of reducing the density of threading dislocations has been proposed by Hull (Hull et al 1992). The technique involves the patterning of a Si(001) substrate, prior to Si$_{1-x}$Ge$_x$ deposition, with a large array of square oxide mesa pillars (approximately 2x2 μm$^2$). Each of the oxide pillars are staggered slightly in the in-plane <110> directions with respect to their neighbours. The oxide pillar arrangement is depicted schematically in Fig 3.7.4.

Since the oxide mesa pillars are staggered slightly along the misfit dislocation line directions, any extending misfits must eventually propagate into one of the pillars, whereby the threading component would terminate at the crystalline/amorphous boundary. In this manner a reduction in the density of threading dislocation of the order of two orders of magnitude was observed, compared to identical depositions on non-patterned wafers. However, only low mismatch, uniform Si$_{0.85}$Ge$_{0.15}$ depositions were investigated and a total threading dislocation density of $10^5$cm$^{-2}$ was reported compared to $10^6$-$10^7$cm$^{-2}$ for corresponding depositions on un-patterned wafers.
Fig 3.7.4
Schematic plan view representation of the novel substrate patterning geometry employed by Hull et al. The squares represent small area oxide mesa pillars. Each of the pillars are staggered in the (110) directions and result in the eventual termination of any propagating misfit segments (M).
However, the non-planar surface morphology of such epilayers may prove to be problematic for integration with conventional device fabrication techniques.

3.7.5 LIMITED-AREA EPITAXY.

Many workers have demonstrated a reduction in the density of misfit dislocations as the lateral dimension of the growth zone is decreased. This method was originally demonstrated within the In$_x$Ga$_{1-x}$/GaAs(100) system by Fitzgerald (Fitzgerald et al 1989(a)). Prior to In$_x$Ga$_{1-x}$ deposition the GaAs substrate was patterned to form mesa columns of lateral dimensions ranging from 400µm to 67µm. As the lateral dimension of the growth zone was decreased, a linear decrease in the density of misfit dislocations was observed. This was attributed to a reduced probability of encountering a pre-existing substrate defect as the area of the growth zone was decreased. Such defect sites act as heterogeneous nucleation sources for dislocations. Since, the number of misfit nucleation sources was limited, low misfit density, metastable films were observed which may be grown above the critical thickness of the corresponding ‘infinite-area’ depositions. Due to the reduction in misfit dislocation density, a 100% reduction in the threading dislocation density of the smaller limited-area depositions was observed. However, such depositions were metastable in nature and not relaxed, although an insight into the kinetics of dislocation formation in strained layers was proposed (Fitzgerald et al 1989(b)).
A similar study within the Si$_{1-x}$Ge$_x$/Si system was performed by Noble (Noble et al. 1990). In this case, limited-area depositions were obtained by deposition within oxide windows of lateral dimensions ranging from millimetres to tens of microns. Si$_{1-x}$Ge$_x$ deposition was performed using chemical vapour deposition. A reduction in the misfit dislocation density of at least a factor of twenty was reported for depositions of lateral dimensions of tens of microns compared to depositions on a scale of millimetres. Again, the reduction was attributed to a reduced probability of encountering heterogeneous nucleation sources within the deposition region. Furthermore, dislocation multiplication events are more likely to occur within the larger areas since misfit interactions are more probably. Nishida et al. have also investigated this system for Si$_{0.8}$Ge$_{0.2}$ epitaxial films and observed a rapidly decreasing linear misfit dislocation density as the lateral dimension of the growth zone was decreased below 7x7 µm$^2$ (Nishida et al. 1992). Indeed, for depositions of lateral dimensions of 2.5 x 2.5 µm$^2$, no misfit dislocations were observed. This data is supported by the work of Stoica and Vescan, who observed zero misfit dislocations in growth zones of lateral dimensions of 10x10 µm$^2$ (Stoica and Vescan 1993). The small discrepancy in the lateral transition dimensions may be attributed to the reduced strain effects within the Stoica work, in which case Si$_{0.88}$Ge$_{0.12}$ epitaxial films were investigated.

A theoretical account of the effect of lateral growth dimensions within the Si$_{1-x}$Ge$_x$/Si system has been performed by several authors. The general consensus of such work shows that as the lateral dimension of the limited area zone decreases below approximately 10x10 µm$^2$ (depending on the Ge content of the epilayer) then the film may elastically relax along the in-plane growth
direction (Luryi and Suhir 1986, Fischer and Richter 1992, Atkinson et al 1995 and Stoica and Vescan 1993). The effect of this elastic relaxation is to reduce the total energy of the growing epilayer. It is therefore possible, at small enough lateral dimensions, to grow a lattice mismatched epilayer to an 'infinite' thickness without overcoming the energy required to nucleate misfit dislocations. In this manner the critical thickness constraints employed by the Matthews-Blakeslee theory may be avoided.

To date, the vast majority of limited-area Si$_{1-x}$Ge$_x$/Si work has concentrated on the effect of lateral dimensions on the misfit dislocation density of uniform depositions, allowing limited-area depositions far in excess of the Matthews-Blakeslee critical thickness to be obtained. However, since misfit dislocations are able to terminate at the edges of the growth zone, orthogonal misfit interactions are dramatically reduced. Such interactions result in the generation of threading dislocations (see section 3.5). In the present work the ability to produce high quality relaxed virtual substrates by utilising the limited-area technique is investigated.
3.8 THE EFFECT OF LATERAL DIMENSIONS ON THE RELAXATION MECHANISM OF COMPOSITIONALLY GRADED Si$_{1-x}$Ge$_x$ BUFFER LAYERS.

3.8.1 INTRODUCTION.

Prior to the current work and to the best of the present author's knowledge, the effect of lateral dimensions on the relaxation mechanism of compositionally graded Si$_{1-x}$Ge$_x$ virtual substrates was an un-investigated field of research. In this section we present the findings of such work and conjecture possible, future device applications.

3.8.2 EXPERIMENTAL PROCEDURE.

In order to investigate the effects of compositionally graded, limited-area Si$_{1-x}$Ge$_x$ depositions, large arrays of square mesa pillars were anisotropically plasma etched to a depth of 2µm on 4" Si(001) substrates. A mesa etch depth of 2µm was necessary so as to ensure independent Si$_{1-x}$Ge$_x$ growth between the top of the mesa pillars and the etched base regions. Firstly, a blanket coverage of SiO$_2$ was deposited to a thickness of 200nm using a low temperature oxidation technique. Oxide deposition was performed at a temperature of 450°C. The blanket oxide was then patterned using a standard contact mask, photolithographic technique and etched using a dilute hydrofluoric (HF) acid wet etch. The patterned SiO$_2$ acted as a mask for the Si plasma etch. The
anisotropic Si(001) etch consisted of a Cl₂, SiCl₄, N₂ plasma and provided a high degree of anisotropy. The sidewalls of the resulting Si mesa pillars were nominally inclined at an angle of 3-degrees to the substrate normal (Emeleus 1996). The patterned SiO₂ mask was then removed using a HF wet etch.

The square Si mesa pillars were orientated along <011> directions and were of lateral dimensions 3, 4, 6, 10 and 20 µm. The individual mesa arrays covered a wafer area of 1 x 1cm², each with 25% mesa coverage. Also included was a region of wafer, of area 1x1cm², which was not etched and acted as an effectively ‘infinite’ area control sample.

To study the effect of limited-area, compositionally graded epitaxy, the etched wafers were cleaned using a modified RCA procedure directly before loading into the MBE chamber. Prior to MBE Si₁₋ₓGeₓ deposition the patterned wafers underwent an in-situ Si flux clean at a temperature of 850°C.

To further ensure a clean surface for SiGe deposition, growth was commenced with a 100nm pure Si buffer region. The buffer was followed by a compositionally graded Si₁₋ₓGeₓ buffer region, with x varying linearly from 5% to 23% over 500nm. A 200nm uniform Si₀.₇₇Ge₀.₂₃ epilayer followed by a 10nm tensile-strained pure Si channel and a 50nm uniform Si₀.₇₇Ge₀.₂₃ layer completed the structure. In order to ensure that the thickness of the epilayer growth was kept to an absolute minimum, the linearly graded region commenced with a Ge fraction equal to 5%. Under these conditions the critical thickness of the equivalent Si₀.₉₅Ge₀.₀₅ ‘infinite area’ deposition is effectively infinite and therefore plays no part in the relaxation process (Iyer et al 1989). All MBE deposition was performed at a substrate temperature of 550°C so as

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to inhibit three-dimensional growth. The wafer described in this work was catalogued 49/04.

The limited-area, compositionally graded $\text{Si}_{1-x}\text{Ge}_x$ epilayers were characterised by the present author using a JEOL JEM-2000fx transmission electron microscope (TEM) operating at an accelerating voltage of 200kV. Scanning electron micrographs (SEM) were obtained using a JEOL JSM 6100 system and atomic force micrograph (AFM) images were obtained at ETH Zurich using a M5 Park Scientific Instruments microscope. Cross-sectional TEM samples were prepared by mechanical thinning followed by Ar-ion sputtering. The degree of relaxation of the individual limited-area depositions was determined using micro-Raman spectroscopy at Toshiba Cambridge Research Centre. The 488nm line of an Ar-ion laser was focused to a spot size of diameter less than 2 $\mu$m using a microscope objective. In addition the maximum Ge content of the epilayer was determined using high and low incidence X-ray [115] rocking curves.

3.8.3 RESULTS.

Fig 3.8.1(a) shows a SEM image of the compositionally graded buffer layer deposited on a Si(001) mesa pillar of lateral dimension 10 $\mu$m. The analogous image of the buffer layer deposited on a 20 $\mu$m wide mesa pillar is depicted in Fig 3.8.1(b). The micrographs indicate a stark contrast in the surface morphology of the epilayer, the 'cross-hatch' topography of the 20 $\mu$m mesa deposition is characteristic of infinite-area, linearly graded depositions. Indeed, the morphology is identical to that of the 'infinite-area' control sample.
Limited area deposition of the compositionally graded buffer layer on mesas of lateral dimensions 10µm (a) and 20µm (b) respectively.
However, the 10 µm limited-area deposition shows a smooth surface morphology. The smooth surface morphology of the 10µm deposition, depicted in Fig 3.8.1(a), is typical of depositions on mesa pillars of lateral dimensions of 10 µm and below. It should be noted that a cross-hatch surface topography was also evident for depositions around the base of the mesa pillars. However, due to the focal length of the microscope, such a topography is not evident in Fig 3.8.1.

Further confirmation of the differing surface morphologies, between the mesas of lateral dimensions of 10 µm and below and the 20 µm depositions is evident from the AFM images of Fig 3.8.2. and Fig 3.8.3. Fig 3.8.2(a) shows the plan view surface morphology of the compositionally graded deposition on a 6 µm mesa, whilst Fig 3.8.2(b) depicts the corresponding height profile across the mesa surface. A maximum peak to trough variation of approximately 2nm is apparent over a 2.5µm scanned region. However, as the lateral dimension of the growth zone is increased to 20 µm a high degree of surface cross-hatch is observed. Fig 3.8.3(a) shows the corresponding plan view AFM image of the 20µm mesa deposition. Again, the surface height profile across the mesa pillar is depicted in Fig 3.8.3(b). In this case, the maximum peak to trough variation across the mesa is of the order of 6nm, a factor of 3 increase over the identical deposition on a mesa column of 10 µm and below.

In order to ascertain the relaxation mechanisms which prevail within such limited-area, compositionally graded depositions, cross-sectional TEM images of the various limited-area buffer layers were obtained.
Fig 3.8.2:

(a) Atomic force micrograph depicting the surface morphology of the 'non-MFR' relaxed, limited-area deposition on a Si mesa pillar of lateral extent 6µm. Fig 3.8.2(b) depicts the corresponding height profile across the mesa centre.
Fig 3.8.3: Atomic force micrograph depicting the surface morphology of the MFR relaxed, limited-area deposition on a Si mesa pillar of lateral extent 20µm (a).

Fig 3.8.3(b) depicts the corresponding height profile across the mesa centre.
Fig 3.8.4(a) depicts a cross-sectional TEM image of the relaxed epilayer deposited on a mesa pillar of lateral dimension 10µm. The electron beam direction was aligned along the [110] crystallographic direction. The nomenclature Si, G and U correspond to the regions of the original Si substrate growth mesa, the compositionally graded Si<sub>1-x</sub>Ge<sub>x</sub> region (500nm) and the uniform Si<sub>0.77</sub>Ge<sub>0.23</sub> (200nm) regions respectively. Due to the compositional grading of the buffer layer, the strain field is spread uniformly throughout the linearly-graded region. Hence, the misfit dislocations required to relax the epilayer occur on different atomic planes within the graded region. Such a misfit dislocation microstructure is clearly visible in Fig 3.8.4(a).

The corresponding [110] cross-sectional TEM micrograph of an identical epilayer deposited on a 20µm mesa pillar is depicted in Fig 3.8.4(b). In this case a large number of dislocation pile-ups are clearly visible penetrating deep into the actual growth mesa pillar, denoted Si. Such dislocation pile-ups are characteristic of the MFR multiplication mechanism (see section 3.7.1) and clearly demonstrate a different relaxation mechanism in operation compared to that of the 10 µm depositions. It should be noted that such observations are typical of numerous limited-area deposition across the entire wafer.

Fig 3.8.5 shows the Si-Si Raman spectra obtained from the centre of the individual limited-area depositions. Due to the penetration depth of the laser light (~120nm), such back-scattered spectra arise primarily from the uniform 200nm Si<sub>0.77</sub>Ge<sub>0.23</sub> layer of the heterostructure. The Si-Si peak positions of the 3 and 4µm mesa depositions are seen to coincide with the spectra obtained from the ‘infinite-area’ control depositions and correspond to approximately 77% relaxation (Dietrich et al 1993). However, a frequency shift in the Si-Si
Fig 3.8.4(a).
Cross sectional TEM image of the Si/SiGe heterostructure deposited on a 10um wide Si mesa pillar. The misfit dislocations are clearly confined within the linearly graded region (denoted G) with no dislocations penetrating the growth mesa (Si) or the uniform Si$_{0.77}$Ge$_{0.23}$ buffer layer (U).
Fig 3.8.4(b).
Cross sectional TEM image of the heterostructure depicted in Fig 3.8.4(a), except deposited on a Si mesa pillar (Si) of lateral dimension 20µm. Note the massive dislocation network penetrating deep into the actual Si growth pillar, again U denotes the uniform Si$_{0.77}$Ge$_{0.23}$ layer.
Fig 3.8.5:
Si-Si raman shift of the uniform 200nm Si$_{0.77}$Ge$_{0.23}$ epilayer deposited on the limited-area, linearly graded buffer layers as a function of lateral growth dimension. The dashed line corresponds to 77% relaxation, whilst the residual strain within the 10µm deposition corresponds to 50% relaxation.
peak is observed for limited-area depositions of lateral dimensions 6, 10 and 20 µm, indicating an increased residual strain remains within the epilayers. The maximum residual strain occurs within the 10 µm mesa deposition and corresponds to approximately 50% relaxation. It should also be noted that a broadening of the Si-Si peak is evident as the growth dimensions are reduced.

3.8.4 DISCUSSION

A finite number of misfit dislocations are required, per unit area, to relax the epilayer. Due to the linear variation in the strain field associated with the graded region of the limited-area, compositionally graded buffer layers, misfit dislocations are spread evenly on different atomic planes throughout the graded region. For limited-area depositions of lateral dimensions of 10 µm and below, misfit dislocations are able to traverse the whole of the limited-area growth zone, without encountering orthogonal misfits on the same, or neighbouring atomic plane. In this manner, misfit dislocations are able to terminate at the edges of the growth zone. Such a ‘non-MFR’ relaxation is clearly evident from the cross-sectional TEM image of Fig 3.8.4(a). Since orthogonal dislocation interactions are avoided, orthogonal pinning events, which result in threading dislocations, cannot arise. Estimates of the threading dislocation densities of the limited-area buffer layers are not deemed reliable from TEM images due to the limited thickness of the sample, together with the limited lateral extent of the growth zone.

As the lateral extent of the growth zone is increased from 10 to 20 µm an increased number of misfit dislocations are required to traverse the mesa in
order to relax the structure. Since a finite number of atomic planes are associated with the graded region of the buffer layer, this leads to an increased probability of an extending misfit encountering a pre-existing orthogonal dislocation on the same, or neighbouring atomic plane. As was discussed in section 3.7.1 the MFR is a direct consequence of such interactions. The MFR pile-ups are clearly visible within the epilayer deposition of lateral dimension 20 µm and are demonstrated in the cross-sectional TEM image of Fig 3.8.4(b).

The co-operative stress fields associated with such MFR pile-ups considerably influence the surface morphology of the relaxed epilayer. The effect of such stress fields are demonstrated in the AFM images of Fig 3.8.2 and Fig 3.8.3 and have been studied by various groups. Fitzgerald et al propose that the cross-hatch roughening associated with compositionally graded Si_{1-x}Ge_x buffer layers may be attributed to the spatially non-uniform growth rates caused by the inhomogeneous strain fields associated with the misfit dislocations (Fitzgerald et al 1992). However, Lutz et al have demonstrated that a single 60° dislocation at the epilayer/substrate interface results in an atomic step at the intersection of the associated glide plane and the epilayer growth surface (Lutz et al 1995). Further, since the MFR mechanism results in a massive dislocation pile-up along a common, or closely spaced (111) glide plane the resulting surface morphology is simply the sum of the individual surface step displacements of the dislocations involved in the pile-up. Typically a MFR pile-up is composed of approximately 10-20 individual dislocations. This theory is further supported by the work of Shiryaev et al. In this work metastable linearly-graded epilayers underwent a post-growth anneal in order to introduce dislocations and relax the film (Shiryaev et al 1994).
this manner the authors were able to distinguish between dislocation induced mechanical effects and the surface kinetics occurring during growth. The work clearly demonstrated that 'the shear plastic displacements caused by the dislocation glide process result in dramatic roughening of the epilayer surface'.

The 3 and 4µm mesa depositions together with the 'infinite-area' deposition all show approximately 77% relaxation (see Fig 3.8.5). However, as the lateral dimension of the growth zone increases from 6 to 10 µm an increased residual strain is observed. The maximum residual strain occurs within the 10µm deposition and corresponds to approximately 50% relaxation. This increase in residual strain energy may be attributed to the decreasing number of heterogeneous dislocation nucleation sources as the limited-area growth zone is reduced. Furthermore, since orthogonal misfit interactions are avoided, a mechanism by which dislocations may multiply is not available. An identical areal density of nucleation sources is also available within the smaller limited-area depositions and therefore a similar degree of relaxation is to be expected. However, as the lateral dimension of the growth zone is decreased from 6 to 3 µm elastic relaxation effects must be taken into account. The broadening of the Si-Si Raman peak is evidence of the elastic relaxation effects occurring within such depositions. Since the diameter of the laser spot size is of the order of 2µm, inevitably, analysis of the elastically relaxed edge effects will occur. Since the epilayer depositions are not confined within the in-plane growth direction, elastic relaxation occurs at the mesa edges. Such an elastic relaxation effect will result in a gradual increase in the bond lengths (and therefore a gradual decrease in the bond energies) across the limited-area
deposition from the mesa centre to the elastically free mesa edge. This results in a broadening of the Si-Si Raman peak, as observed in Fig 3.8.5.

The maximum residual strain occurs within the 10µm mesa deposition. As the lateral dimension of the growth zone increases to 20µm, there is an increasing probability of orthogonal misfit interactions occurring and relaxation is further aided by the onset of the MFR mechanism. At this point, misfit multiplication occurs which results in further relaxation. However, due to the limited lateral extent of the 20µm growth zone only a finite number of orthogonal misfit interactions are probable. Hence, a limited number of MFR multiplication sites may be activated, again limiting the amount of relaxation. As the growth zone is further increased to an 'effectively infinite' deposition, an increased number of MFR sites will be activated and maximum relaxation will occur.

3.8.5 CONCLUSIONS.

In summary, an 'ideal' mechanism by which Si$_{1-x}$Ge$_x$ epilayers may relax has been identified for the first time. By incorporating both the methods of limited-area epitaxy and compositional grading of the buffer layer, complete misfit extension is observed across the growth zone. In this manner, misfit extension occurs along different lateral atomic planes within the graded region and misfit dislocations may traverse the total extent of the growth zone without encountering any orthogonal misfits on the same atomic plane. The resulting non-MFR relaxed depositions show a very smooth surface topography and the characteristic cross-hatch surface morphology may be avoided. Furthermore,
since orthogonal misfit interactions are avoided a dramatic reduction in the threading dislocation density of such limited-area, linearly graded depositions is to be expected.

It is proposed that such a method of limited-area, linearly graded epitaxy has very important possible device applications. In this manner both the problematic threading dislocation density and the surface cross-hatch morphology, characteristic of current 'state of the art' virtual substrates, may be avoided. At present, compositionally graded buffer layer are typically grown to a thickness of 2-5µm. However, the resulting virtual substrates suffer from a high degree of surface cross-hatch roughening (typically 1-5nm height fluctuations) and sustain a residual density of threading dislocations of the order of $10^5$cm$^{-2}$.

The method of limited-area, linearly graded virtual substrates offers a substantial reduction in the actual thickness of the buffer layer and crucially results in the elimination of both the surface cross-hatch roughening and the residual threading dislocation density. Indeed, it is the present authors opinion, that the method of limited-area, linearly graded buffer layers provides a simple mechanism for obtaining the 'perfect' virtual substrate. The approach should enable high quality, strained layer quantum wells to be produced. This topic is dealt with in more detail in chapter 4.

It is also proposed that an increase in the degree of relaxation may be obtained, whilst preserving the surface morphology of the limited-area depositions, by simply applying a high temperature post-growth anneal. In this manner complete extension of any residual threading components, pinned due
to elastic relaxation edge effects, may occur. Further work within this area is required in order to determine the maximum state of relaxation.

It is proposed that limited-area, linearly graded buffer layers should enable high quality virtual substrates to any Ge content to be grown. By increasing the growth thickness and maintaining the present grading rate (34% atomic Ge fraction per µm), relaxed virtual substrates to any Ge content may be obtained within lateral dimensions of 10µm and below. Again, such buffer layers should be free of threading dislocations and possess a smooth surface topography. Such virtual substrates may have highly desirable applications within the field of opto-electronics since they will enable the complete epitaxial integration of III-V compounds with standard Si fabrication techniques.

3.8.6 FURTHER WORK.

Although limited-area, compositional grading facilitates the production of virtual substrates, the use of Si mesa pillars implicates a profound difficulty to current Si processing techniques, namely its inherent non-planarity. Conventional Si device fabrication techniques rely on highly uniform, planar geometries. Although the Si_{1-x}Ge_x material system offers unique improvements over conventional Si devices it must be compatible with conventional Si processing techniques. As the active gate device dimensions are reduced further to 0.1µm, planarisation is critical. It is the present author’s opinion that the 2µm step edge used in current work is not practical for MOS processing techniques and a method of planarisation is essential.
Two methods of increased planarisation may be envisaged. The first relies on a method in use in current field of CMOS fabrication, namely that of deep trench isolation. In this manner a deep trench etch may be used to define the limited-area growth zone. These trenches are then ‘back-filled’ with SiO₂. The method would result in the total planarisation of the limited-area growth surface. A second approach is that of Si₁₋ₓGeₓ deposition within oxide defined windows, and is used in some existing CMOS fabrication techniques—namely LOCOS. In this manner a thin (say 10nm) oxide film may be patterned prior to MBE deposition. The growth within the oxide windows would be of high crystalline quality, whilst the surrounding deposition on the patterned oxide would result in a poly-Si₁₋ₓGeₓ oxide overgrowth. The crystalline/non-crystalline boundary would again provide a ‘sink’ allowing misfit termination to occur. This method is more readily accessible. However, it remains non-planar to a degree and the effect of the crystalline/non-crystalline boundary must be ascertained, since it may induce further dislocations and/or stacking faults within the limited-area growth zone.

However, an advantage inherent to both methods is that of increased device isolation. If the Si₁₋ₓGeₓ material system is to make an impact over conventional Si devices this will occur at the high frequency end of the device spectrum. A major obstacle at such frequencies is that of device isolation which reduce unwanted parasitic capacitance.
3.9 THE EFFECT OF GRADING RATE ON LIMITED-AREA, COMPOSITIONALLY GRADED BUFFER LAYERS.

3.9.1 INTRODUCTION.

In order to fully quantify the effect of lateral dimensions on the relaxation of linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers, further experiments involving the effect of the grading rate of the compositionally graded region were performed. In this manner, the influence of orthogonal dislocation interactions within the compositionally graded region could be ascertained.

3.9.2 EXPERIMENTAL.

In order to determine the effect of grading rate on the relaxation of limited-area, linearly graded buffer layers further $\text{Si}_{1-x}\text{Ge}_x$ depositions were performed on patterned substrates using MBE. The exact experimental procedure and epilayer growth structure has been described in section 3.8.1. However, in the current work the thickness of the linearly graded region was varied from 250nm, 500nm and 750nm, the wafers were catalogued 52/35, 49/04 and 52/36 respectively. In all cases the Ge content at the base of the graded region corresponds to 5% atomic Ge fraction and the terminating Ge fraction was 23%. Again, all MBE deposition was performed at a substrate
growth temperature of 550°C and the surface morphology of the resulting limited-area depositions was determined using atomic force micrographs (AFM) obtained from a M5 Park Scientific Instruments microscope.

3.9.3 RESULTS.

Figs 3.9.1, 3.9.2 and 3.9.3 depict the planar AFM profiles of the various limited-area depositions of lateral extent 6, 10 and 20µm, respectively and correspond to a grading thickness of 250, 500 and 750nm.

The surface profiles of each of the 6µm mesa depositions show a smooth surface topography and no surface cross-hatch is evident. This may be attributed to a reduction in orthogonal misfit interactions together with the ‘smoothing effects’ of the elastically relaxed epilayer edges (see section 3.8.4).

The corresponding AFM surface profiles, for depositions of lateral extent 10µm are depicted in Fig 3.9.2. Fig 3.9.2(a) shows a highly cross-hatched surface morphology and corresponds to a grading thickness of 250nm. As the thickness of the graded region is increased the density of the surface cross-hatch is significantly reduced. Indeed, in the case of a grading thickness of 750nm, the surface morphology of the 10µm deposition is completely smooth.

As the lateral extent of the growth zone is increased to 20µm all the mesa depositions show, to some extent, a degree of surface cross-hatch. However, as the thickness of the graded region is increased from 250nm to 750nm, the density of the cross-hatch morphology is again decreased.
Fig 3.9.1:
AFM surface morphology of the limited-area, linearly-graded buffer layers deposited at 550°C on a Si mesa of lateral extent 6µm. Each represents a scanned area of 3x3μm². (a) grading thickness of 250nm. (b) grading thickness of 500nm. (c) grading thickness of 750nm.
AFM surface morphology of the limited-area, linearly-graded buffer layers deposited at 550°C on a Si mesa of lateral extent 10µm. Each represents a scanned area of 6x6µm². (a) grading thickness of 250nm. (b) grading thickness of 500nm. (c) grading thickness of 750nm.
Fig 3.9.3:
AFM surface morphology of the limited-area, linearly-graded buffer layers deposited at 550°C on a Si mesa of lateral extent 20µm. Each represents a scanned area of 6x6µm². (a) grading thickness of 250nm. (b) grading thickness of 500nm. (c) grading thickness of 750nm.
3.9.4 DISCUSSION.

The variation in thickness of the linearly graded \( \text{Si}_{1-x}\text{Ge}_x \) regions of the various limited-area mesa depositions provides strong evidence as to the origin of the pronounced surface cross-hatch morphology. Such a morphology is characteristic of large area, linearly graded buffer layers. As was postulated in section 3.8.4, orthogonal misfit interactions, resulting in a MFR-dominated relaxation process, play an important role in defining the final surface topography. The stress fields associated with the MFR dislocation pile-ups create slip-lines at the intersection of the common pile-up glide plane and the growth surface. An increase in the thickness of the linearly graded region results in a decreasing probability of orthogonal misfit interactions occurring. Hence, the probability of activating a MFR multiplication site is similarly reduced.

Fig 3.9.1 depicts the AFM surface profile of the 6\( \mu \)m mesa depositions with a graded thickness varying from 250nm, 500nm and 750nm. In all cases the resulting surface profile shows a smooth topography. Due to the small area, the probability of an extending misfit segment encountering a pre-existing orthogonal misfit along the same lateral atomic plane is correspondingly low and relaxation is dominated by the complete, unhindered extension of misfit dislocations. Such a relaxation process results in a smooth surface morphology.

It is evident from Fig 3.9.2 and Fig 3.9.3 that an increase in the thickness of the linearly graded region results in a pronounced decrease in the density of the surface cross-hatch. Indeed, the 10 \( \mu \)m mesa deposition with a total grading thickness of 750nm shows a completely smooth surface morphology (Fig
3.9.2(c)), whilst the corresponding deposition with a total grading thickness of 250nm depicts a high degree of cross-hatch. Similar results are obtained from the 20 µm mesa depositions of Fig 3.9.3.

3.9.5 CONCLUSIONS.

The effect of grading rate on the relaxation of limited-area, linearly graded Si$_{1-x}$Ge$_x$ buffer layers has been investigated. As the thickness of the graded region is increased, corresponding to a decrease in the grading rate, it is evident that the number of orthogonal misfit interactions occurring within a given limited-area growth zone decreases. In this manner, the MFR multiplication mechanism is avoided and the lateral dimension of the limited-area growth zone may be increased without the onset of the MFR roughening occurring. The method should allow an increase in the maximum dimension of the 'ideal' virtual substrate.

3.9.6 FURTHER WORK.

As was discussed in section 3.8.5, it is proposed that the method of limited-area, compositionally graded Si$_{1-x}$Ge$_x$ buffer layers offers the opportunity of obtaining high quality relaxed virtual substrates to any Ge content within a lateral growth dimension of 10µm and below. Such buffer layers may be obtained by simply increasing the total thickness of the graded region, whilst maintaining a constant grading rate of 34% atomic Ge fraction per micron. Furthermore it is proposed that high quality relaxed, buffer layers
of lateral growth dimensions in excess of 20µm may be obtained to any Ge content by reducing this grading rate (see Fig 3.9.3). Further work is necessary within this field in order to fully exploit the concept of limited-area, linearly graded heteroepitaxy.

3.10 THE EFFECT OF GROWTH TEMPERATURE ON LIMITED-AREA, COMPOSITIONALLY GRADED BUFFER LAYERS.

3.10.1 INTRODUCTION.

The temperature at which Si_{1-x}Ge_{x} epitaxial layers are deposited is also known to have a pronounced effect on the relaxation of strained heteroepitaxial layers. The excess energy available at high growth temperatures allows the kinetically-limited nucleation process to be overcome at reduced strain energies. This results in a reduced critical thickness at higher growth temperatures. Furthermore, the excess energy available results in an increase in the glide velocity of the extending misfit dislocations. For a more detailed overview on this subject the reader is referred to the work of Hull and Bean and Perovic and Houghton (Hull and Bean 1992 and Perovic and Houghton 1995). In this section, the effect of growth temperature on the relaxation of limited-area, compositionally graded buffer layers is investigated.
3.10.2 EXPERIMENTAL.

In order to determine the effect of growth temperature on the relaxation of limited-area, linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers further MBE depositions were performed on patterned substrates. The experimental procedure used to define the patterned substrates is identical to that described in section 3.9.2. Indeed a similar epilayer deposition was performed employing a nominal 100nm pure Si buffer, followed by a compositionally graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer. The heteroepitaxial deposition was completed with a 10nm tensile-strained pure Si channel and a 50nm uniform $\text{Si}_{0.77}\text{Ge}_{0.23}$ layer. The Ge content of the compositionally graded region was again varied from 5% atomic Ge fraction to 23% over 500nm. However, the growth temperature of the whole epilayer deposition was varied from 500°C, 550°C and 600°C and the wafers were catalogued 52/37, 49/04 and 52/38 respectively. The maximum growth temperature was limited to 600°C so as to avoid 3-dimensional island growth (Bean et al 1984). The surface morphology of the resulting limited-area depositions was again determined using AFM.

3.10.3 RESULTS.

The resulting surface morphologies of the limited-area, growth temperature variation trials are depicted in the AFM surface profiles of Fig 3.10.1, Fig 3.10.2 and Fig 3.10.3. The growth temperatures depicted in these figures are 500°C, 550°C and 600°C respectively.
AFM surface morphology of the limited-area, linearly-graded buffer layers deposited on a Si mesa of lateral extent 6µm. In each case the thickness of the linearly graded region is 500nm. Each represents a scanned area of 3x3µm². (a) growth temperature of 500°C. (b) growth temperature of 550°C. (c) growth temperature of 600°C
AFM surface morphology of the limited-area, linearly-graded buffer layers deposited on a Si mesa of lateral extent 10µm. In each case the thickness of the linearly graded region is 500nm. Each represents a scanned area of 6x6µm². (a) growth temperature of 500°C. (b) growth temperature of 550°C. (c) growth temperature of 600°C.
AFM surface morphology of the limited-area, linearly-graded buffer layers deposited on a Si mesa of lateral extent 20μm. In each case the thickness of the linearly graded region is 500nm. Each represents a scanned area of 12x12μm². (a) growth temperature of 500°C. (b) growth temperature of 550°C. (c) growth temperature of 600°C.
Fig 3.10.1(a) shows the AFM surface profile of the 500°C deposition on a 6µm mesa. The corresponding surface profiles of the 6µm depositions at a growth temperature of 550°C and 600°C are depicted in Fig 3.10.1(b) and Fig 3.10.1(c) respectively. In all cases the limited-area depositions of 6x6µm² show a smooth surface morphology. Again this may be attributed to misfit dislocation propagation along different lateral atomic planes, leading to misfit termination at the edges of the growth zone without orthogonal misfit interactions occurring.

However, for limited-area, compositionally graded depositions of lateral dimensions of 10µm an increase in the density of the surface cross-hatch is observed as the growth temperature is increased from 500°C to 600°C (see Fig 3.10.2). The cross-hatch surface morphology of the 10µm deposition at 600°C (Fig 3.10.2(c)) is in stark contrast to the smooth surface morphology of the identical epilayer growth deposited at 500°C (Fig 3.10.2(a)).

A similar increase in the density of surface cross-hatch as the growth temperature is increased is evident from the AFM surface profiles of the limited-area depositions of lateral dimensions of 20µm. The situation is depicted in Fig 3.10.3. Again, Fig 3.10.3(a) corresponds to a growth temperature of 500°C, whilst Fig 3.10.3(b) and Fig 3.10.3(c) correspond to a growth temperature of 550°C and 600°C respectively. A high density of surface cross-hatch is evident at both a growth temperature of 550°C and 600°C, whilst the identical deposition grown at 500°C shows a smooth surface morphology. Again, the surface cross hatch topographies may be attributed to the onset of the MFR multiplication mechanism and are a direct result of orthogonal misfit interactions.
3.10.4 DISCUSSION.

At first sight, the increased density of surface cross hatch roughening observed as the growth temperature is increased seems counter-intuitive. At higher growth temperatures dislocation glide velocities are increased, allowing misfit extension to occur more quickly (Hull et al 1989). Since, in all cases the growth rate remained constant, the increase in dislocation glide velocity would result in a decreasing probability of orthogonal misfit interactions occurring within the same atomic plane. A slow moving misfit dislocation extending across the growth zone would allow a finite duration of time for an orthogonal misfit to extend and relax the strained crystal region ‘in-front’ of the original misfit, thus increasing the likelihood of orthogonal misfit pinning. However, at increased glide velocities this ‘window’ would be reduced, resulting in a reduced probability of orthogonal misfit interactions occurring along a given atomic plane. Hence, a decrease in the MFR-roughening would be expected at elevated growth temperatures. The experimental results of Fig 3.10.2 and Fig 3.10.3 are clearly contrary to this assumption.

In order to explain the observed experimental results the effect of growth temperature on the nucleation of misfit dislocations must be considered. The nucleation of a misfit dislocation requires a finite amount of energy to shear the neighbouring atomic bonds. In the case of lattice mismatched heteroepitaxy, the total nucleation energy available is composed of the epitaxial strain energy, together with the thermal energy available. At increased growth temperatures the strain energy required to nucleate a misfit dislocation is reduced. This
results in a reduction of the critical layer thickness at elevated growth temperatures.

Consider the case of the limited-area, linearly graded buffer layers, in which the strain energy of the epilayer gradually builds up as growth continues. At a growth temperature of 600°C a preliminary misfit dislocation will nucleate at a point 'lower' in the compositionally graded region compared to an identical deposition at a growth temperature of 500°C. This is due to the increased strain energy required to nucleate a dislocation at a reduced growth temperature. Hence, at high growth temperatures the total number of atomic planes which separate sequential misfit nucleation sites is reduced. The overall effect results in an increased probability of orthogonal misfit dislocation interactions occurring within the higher temperature deposition, compared to an identical deposition grown at a reduced temperature. The situation may be represented by a simple analogy: 'stray cattle have much more chance of falling through a cattle grid with widely spaced rungs!'

The experimentally observed increase in the density of the surface cross-hatch roughening with increasing growth temperature is consistent with the above discussion. For a given limited-area growth zone, an increased growth temperature results in an increased probability of orthogonal misfit interactions occurring along the same, or neighbouring atomic plane of the compositionally graded region, ultimately yielding a cross-hatched surface topography. However, due to the increased number of misfit dislocations, which occur at higher growth temperatures, an increase in the degree of epilayer relaxation is to be expected.
3.10.5 CONCLUSIONS.

In summary, the effect of growth temperature on the relaxation of limited-area, compositionally graded buffer layers has been investigated. The study revealed that an increase in growth temperature of 100°C successfully increases the activation of MFR sources and results in a deterioration in the surface morphology of depositions of 10x10µm² and above. Obviously, the growth temperature plays a significant role in the production of defect free virtual substrates. Due to the finite amount of energy associated with misfit dislocation nucleation, an increase in the growth temperature of identical linearly graded buffer layers results in a reduction in the spatial separation between subsequent misfit dislocations in the growth direction. This spatial reduction leads to an increased probability of orthogonal misfit interactions occurring within a given atomic plane and gives rise to an increased probability of MFR multiplication sites being activated.

The method of growth temperature variation of linearly graded, limited-area depositions provides an extra degree of freedom by which the onset of MFR roughening may be controlled. Furthermore, the work has demonstrated a new and effective approach to enable the production of useful virtual substrates.

3.10.6 FURTHER WORK.

It has been demonstrated in section 3.8 that the primary source of surface cross-hatch roughening, characteristic of infinite-area, linearly graded buffer
layers, may be attributed to the stress fields associated with the MFR dislocation multiplication pile-ups. In section 3.9 it was demonstrated that the probability of such MFR sources becoming activated is reliant upon the probability of orthogonal misfit interactions occurring along a given atomic growth plane. Indeed, the activation of such MFR sites may be controlled by varying the grading rate of the compositionally graded region. In this manner, the lateral dimension at which the onset of MFR roughening occurs, may be controlled. Furthermore, in section 3.10 the effect of growth temperature on the relaxation of compositionally graded, limited-area buffer layers was investigated. In this manner a further degree of freedom by which the onset of MFR roughening may be controlled was described. It is also proposed (section 3.9.6) that by simply increasing the thickness of the compositionally graded region, whilst maintaining a constant grading rate, high quality virtual substrates to any Ge content may be obtained.

It is the present author's opinion that by combining the methods of grading rate variation and growth temperature variation, the lateral dimension at which the onset of MFR relaxation occurs may be increased beyond 20μm-well in excess of that required for state-of-the-art FET's. The optimum conditions are proposed to be a low temperature deposition with a low grading rate. To further aid the magnitude of the relaxation, a study of the effect of high temperature post-growth anneals should be ascertained. In this manner, high quality, relaxed virtual substrates with a minimal density of threading dislocations and a smooth surface topography may be achieved. Indeed, the maximum thickness of the compositionally graded region in the current work was 750nm. Whilst, conventional infinite-area, compositionally graded buffer
layers are of the order of 2-5µm. Combining these factors, high quality buffer layers to any Ge content on a scale easily accessible to current device fabrication techniques may be envisaged.

The method of linearly graded, limited-area buffer layers provides a simple and highly flexible approach to obtaining the ‘ideal’ virtual substrate. Research should continue within this field.
CHAPTER 4.

THE ELECTRICAL CHARACTERISATION OF Si$_{0.5}$Ge$_{0.5}$ TWO-DIMENSIONAL HOLE GAS SYSTEMS DEPOSITED ON VIRTUAL SUBSTRATES.

4.1 INTRODUCTION.

A major limitation of conventional Si-CMOS devices is the comparatively low hole mobility inherent to the p-MOSFET. In order to achieve improved performance and increased integration levels, the gate lengths of CMOS devices are constantly being reduced. Current state of the art devices possess an operational gate length of approximately 0.25µm, with a further reduction to 0.15µm envisaged by the year 2004 (SIA Roadmap 1995). However, the ability to achieve further reductions look increasing uncertain due to the wavelength of the UV light used in conventional photolithographic fabrication techniques.

The low hole mobility within conventional Si-CMOS devices may be attributed to the high effective mass of holes inherent to Si, compared to the electron mass. In addition, the relatively poor interface quality of the Si/SiO$_2$
confinement channel results in a large degree of carrier scattering. In recent years many workers (see review by Whall 1995 and references therein) have demonstrated an improved hole mobility by incorporating a buried, strained heteroepitaxial SiGe channel within the standard Si process using epitaxial growth techniques. The bandstructure of the heteroepitaxial layer may be specifically tailored, enabling the confinement of high mobility holes within a two-dimensional carrier channel which is spatially separated from the ‘rough’ oxide interface (Meyerson 1986). In this manner, inter-valley phonon scattering events are reduced due to the strain-induced splitting of the degenerate valence band. This results in a mobility enhancement. In addition, the incorporation of Ge produces a decrease in the hole effective mass.

The theoretical implications of incorporating a strained SiGe channel have been assessed by O’Neill and an improvement in the room temperature cut-off frequency of a factor of 3 was demonstrated over a conventional Si p-MOS device at a gate length of 0.1µm (O’Neill et al 1995, 1996).

<table>
<thead>
<tr>
<th>Percentage Ge content, x (%)</th>
<th>Hole Mobility (cm²/Vs)</th>
<th>Carrier Sheet Density (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 %</td>
<td>19,800</td>
<td>6.0 x 10¹⁰</td>
</tr>
<tr>
<td>13 %</td>
<td>11,100</td>
<td>1.8 x 10¹¹</td>
</tr>
<tr>
<td>20 %</td>
<td>6,000</td>
<td>3.0 x 10¹¹</td>
</tr>
<tr>
<td>40 %</td>
<td>1,500</td>
<td>2.8 x 10¹²</td>
</tr>
</tbody>
</table>
Table 4.1. Low temperature ‘State-of-the-art’ hole mobilities in Si$_{1-x}$Ge$_x$/Si modulation doped pseudomorphic heterostructures grown by solid source MBE.

The measured 4K hole mobility and sheet carrier density of several systems are presented in Table 4.1.1. Experimentally, a gradual reduction in the low temperature hole mobility is observed as the Ge content of the alloy channel is increased. However, it should be noted that for digital applications the important parameter is the total current drive of the device and not simply the carrier mobility. The total current drive is a function of both the carrier mobility and their corresponding sheet density. An increased sheet carrier density offers the system a greater current drive, this is also the case for an increased carrier mobility. Generally, as the total Ge content of the p-channel is increased, the associated band offset is similarly increased, allowing the confinement of a greater number of carriers within the 2-dimensional channel (Murakami et al 1994). This topic will be dealt with in more detail in section 4.2.

The complete optimisation of the strained layer 2-dimensional hole gas (2DHG) system is a complicated procedure due to the large number of scattering mechanisms which limit the hole mobility. As will be discussed in section 4.2, in order to achieve a large sheet carrier density, a large mismatch is required between the confinement channel and the surrounding buffer layer. However, as was discussed in section 3.2(iii), the growth of a highly mismatched epilayer at a high temperature can result in a substantial roughening of the epilayer surface. It has been demonstrated that at high sheet
densities the major hole-mobility limiting mechanism within highly mismatched structures may be attributed to the compositional non-uniformities associated with surface roughening (Kiehl et al 1993, Whall et al 1993). On the other hand, in section 4.3 it is demonstrated that a high temperature deposition is desirable so as to ensure a high quality epitaxial layer which is free of as-grown lattice defects, which pose another mobility limiting mechanism. Hence, prior to the present work, the complete optimisation of the Si$_{1-x}$Ge$_x$/Si 2DHG heterosystem relied upon a compromise between several 'necessary evils' involving surface roughening effects produced during high temperature growth, together with an increase in the density of lattice defects which occur during the low temperature depositions required for planar surfaces.

The complete optimisation of the 2DHG system is a crucial factor if the SiGe heteroepitaxial architecture is to make an impact over conventional Si CMOS devices. In the present chapter two mechanisms by which this optimisation can be achieved are addressed, namely that of growth temperature optimisation and the effect of post-growth anneals.

4.2 THE BANDSTRUCTURE OF THE SiGe/Si HETERO SYSTEM.

4.2.1 INTRODUCTION.

The following section provides a brief insight into the band structure and band offsets associated with the SiGe heteroepitaxial system. Due to the
difference in band gap energies between pure Ge and Si, the issue of band edge alignment throughout a composite heterostructure is addressed. In addition, the effect of the Ge content on the valence band offset of such heterostructures is discussed.

Secondly, the effect of strain on the electronic properties of such lattice mismatched heterostructures is considered and the possible advantages of such systems are discussed. Finally, the reader is introduced to the various scattering mechanisms, which ultimately limit the performance of SiGe/Si technologies.

4.2.2 BAND ALIGNMENT.

Due to the difference in the band gap energies between Si and Ge, 1.11eV and 0.664eV respectively, the growth of a Si$_{1-x}$Ge$_x$ layer on a similar Si$_{1-y}$Ge$_y$ epilayer with a different Ge content, results in a discontinuity in the valence and/or conduction band edge. Such a band offset may be employed to confine charge carriers within a two-dimensional channel.

In recent years several authors have undertaken a rigorous theoretical analysis of the effect of strain and Ge content on the band edge discontinuities within the SiGe heterosystem. People and Bean incorporated the phenomenological deformation potential theory, developed by Kleiner and Roth, together with the self-consistent ab-initio pseudopotential results of Van der Walle and Martin to estimate the indirect band gap energies of SiGe alloys in three distinct cases (People et al 1986, Kleiner et al 1959 and Van der Walle et al 1985):
a) The band gap of coherently strained Si$_{1-x}$Ge$_x$ on <001> Si substrates.
b) The band gap of coherently strained Si on <001> Si$_{1-x}$Ge$_x$ substrates.
c) The band gap of coherently strained Si$_{1-x}$Ge$_x$ alloys on <001> Si$_{1-x}$Ge$_{x/2}$ substrates.

The results of such theoretical considerations are depicted in Fig 4.2.1. Also, included are the effects of strain on the valence subbands. This will be dealt with in more detail in section 4.2.3.

More recently, Van der Walle and Martin revised their theoretical calculations to include the effects of strain induced spin-orbit splitting (Van der Walle et al 1986 and Murakami et al 1994).

The magnitude of the valence band offset $E_v$, in electron volts (eV), of various <001> SiGe heterosystems may be described using the following relations, where $x$ denotes the Ge content of the strained confinement channel and $x_s$ corresponds to the Ge content of the buffer layer:

a) $\Delta E_v = 0.84x$ for Si/ Si$_{1-x}$Ge$_x$ on (001) Si substrates.
b) $\Delta E_v = 0.84 - 0.53x_s$ for Si/Ge on (001) Si$_{1-x_s}$Ge$_{x_s}$ substrates.
c) $\Delta E_v = (0.84 - 0.53x_s)x$ for Si/ Si$_{1-x_s}$Ge$_x$ on (001) Si$_{1-x_s}$Ge$_{x_s}$ substrates.
d) $\Delta E_v = 0.31(1-x)$ for Si$_{1-x}$Ge$_x$/Ge on (001) Ge substrates.

The present work investigates the electrical properties of a 2DHG, confined within a compressively strained Si$_{0.5}$Ge$_{0.5}$ channel grown on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate. Using the relations defined above, such a
Fig 4.2.1.

Bandgap of bulk and strained $\text{Si}_{1-x}\text{Ge}_x$ alloys as a function of Ge content $x$. The strain induced splitting of the valence band edge, into the heavy hole and light hole subbands are also shown. (People 1985)
heterostructure results in a valence band discontinuity in excess of 340meV. Such a valence band discontinuity is far in excess of the typical thermal energies encountered at room temperatures (approximately 25meV) allowing effective hole confinement to be achieved at room temperatures.

It should be noted that the magnitude of the valence band offset of the Si$_{1-x}$Ge$_x$/Si$_{1-x}$Ge$_x$ heterosystem depends critically upon both the Ge content of the strained confinement channel, $x$, and the Ge content of the relaxed buffer layer, $x_r$. Generally, as the Ge content of the confinement channel is increased, the resulting band-offset is increased accordingly.

The magnitude of the sheet carrier density of a confined 2DHG is directly proportional to the magnitude of the valence band offset (Ando et al 1982). This is a particularly important consideration for the current drive capabilities of p-FET applications. Furthermore, the reduced access resistance obtainable at high sheet carrier densities allows an increase in the p-FET switching speed.

Typically, the valence band offset of a 2DHG confined within a compressively strained Si$_{0.8}$Ge$_{0.2}$ channel grown pseudomorphically on a Si substrate is of the order of 170 meV. The corresponding sheet carrier density for a 2DHG confined within such a pseudomorphic channel is approximately $2 \times 10^{11}$cm$^2$, although this may be varied under gate bias conditions (Emeleus et al 1992).

In comparison, an order of magnitude increase in the sheet carrier density of a 2DHG confined within a Si$_{0.5}$Ge$_{0.5}$ channel grown on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate may be realised, even though the magnitude of the actual strain within the two heterostructures remains equal.
Ismail et al. have demonstrated a record room temperature hole mobility of in excess of 1000 cm\(^2/V\)s within a compressively strained Si\(_{0.2}\)Ge\(_{0.8}\) confinement channel grown using UHV-CVD on a relaxed Si\(_{0.7}\)Ge\(_{0.3}\) buffer layer (Ismail et al, 1994). The corresponding sheet carrier density of the gas was determined to be 3\(\times\)10\(^{12}\)cm\(^{-2}\), resulting in a record low sheet resistivity of 2.4\(\times\)10\(^{4}\)\(\Omega\)cm. This value represents a factor of four increase over state-of-the-art Si p-MOS devices and has considerable implications to both future p-MOS and CMOS applications.

4.2.3 THE EFFECT OF STRAIN.

In unconstrained, bulk Si and Ge the valence band edge is 3-fold degenerate in the absence of quantum mechanical spin issues. The inclusion of the spin-orbit interaction results in a subband splitting and the formation of a heavy hole subband \((J = 3/2, m_j = \pm 3/2)\) and a light hole subband \((J = 3/2, m_j = \pm 1/2)\), together with a spin-orbit doublet \((J = 1/2, m_j = \pm 1/2)\). In both Si and Ge the heavy hole and light hole subbands are degenerate at the Brillouin zone centre.

The commensurate growth of of Si\(_{1-x}\)Ge\(_x\) strained layer on a relaxed Si\(_x\)Ge\(_y\) epilayer, in which \(x\) exceeds \(y\), results in a biaxial in-plane lattice compression of the Si\(_{1-x}\)Ge\(_x\) alloy layer and a uniaxial lattice extension along the interface normal. People (1985) included the effects of the uniaxial strain component and demonstrated that such a tetragonal lattice distortion results in
the splitting of the degenerate heavy hole and light hole subbands at the centre of the Brillouin zone.

Due to the effect of strain, the ground state heavy hole subband lies lowest in energy and results in a reduction of the hole effective mass, the effect is depicted in Fig 4.2.1. The situation is highly advantageous for device applications, since the magnitude of the mobility of such carriers is inversely proportional to the carrier effective mass. In addition, the effect of subband is also advantageous to the electrical properties of the system, due to a reduction in elastic scattering events due to phonons, impurities etc.

4.2.4 SCATTERING MECHANISMS

In this section, the major scattering mechanisms, which ultimately limit the carrier transport properties of the SiGe/Si heterosystem, are addressed. Generally, for hole transport confined within a strained layer SiGe quantum well, such scattering mechanisms may be categorised as:

- Coulombic impurity scattering.
- Interface roughness scattering.
- Interface impurity scattering.
- Alloy scattering.
- Lattice vibrations.

The effect of such scattering mechanisms on the electrical transport properties of strained layer SiGe/Si heterostructures will now be considered in
For a more rigorous analysis the reader is referred to the work of Ando et al 1982 and Emeleus et al 1993 and

4.2.4.1 COULOMBIC IMPURITY SCATTERING.

A distinct advantage that may be realised using modulation doped heterostructures is the reduction in the magnitude of ionised impurity scattering. This reduction is due to the spatial separation of the confined carrier gas from the ionised dopant impurity atoms. The charge associated with ionised impurity atoms result in local fluctuations in the periodic lattice potential, which hinder carrier motion. The affect of such an impurity scattering mechanism on the carrier mobility $\mu_n$, may be approximated using the relation (Ando et al 1982):

$$
\mu_n = 32\sqrt{2\pi} \frac{e}{h} \frac{n_s^{3/2}}{N_A} \left( \frac{1}{(L_s + w)^2} - \frac{1}{(L_s + w + l)^2} \right)^{-1}
$$

Where, $e$ and $h$ denote the electronic charge and the modified Plank constant respectively, $n_s$ denotes the confined sheet carrier density, $N_A$ is the concentration of impurity ions, $L_s$ denotes the spatial separation between the confined carrier gas and the ionised impurity atoms, $w=3/b$ and $l$ is the ionised impurity depletion width. The factor $b$, is known as the ‘variational parameter’ and is defined:

$$
b = \left[ \frac{12m*e^2}{\hbar^2\varepsilon_0\varepsilon_r} \left( N_{Dopt} + \frac{11}{32}n_s \right) \right]
$$
Where, $\varepsilon_0$ and $\varepsilon_r$ represent the absolute and relative material permittivity respectively, whilst $N_{D_{ex}}$ and $n_c$ represent the charge arising from background doping depletion and the confined sheet carrier density respectively.

4.2.4.2 INTERFACE ROUGHNESS SCATTERING.

Generally, the effects of interface roughness scattering may be categorised into two distinct cases. The first mechanism is due to the transitional layer between the strained confinement channel and the relaxed buffer. Typically, such a transitional region results in a random Ge distribution of the order of one or two monolayers. The non-abrupt profile results in a slight spreading of the carrier wavefunction into the relaxed buffer region and results in further carrier scattering (Ando et al 1982). The second, and more dominant, scattering mechanism results from the non-planar growth of the two-dimensional confinement channel. In section 3.2(iii) the effect of increased growth temperature and the resulting transition from planar two-dimensional epitaxial growth to three-dimensional 'islanding' growth was discussed. An inappropriate choice of growth conditions can result in a substantial roughening of the strained confinement channel. In both cases, the associated variation of the potential well thickness causes a perturbation of the carrier eigenstate energies and gives rise to an effective scattering potential.

Generally, the analysis assumes a Gaussian correlation, of length $\Lambda$ and height $\Delta$, between such random channel thickness fluctuations. Following the formalism of Gold et al 1986, the carrier mobility due to interface roughness scattering may be defined:

$$
\mu_{IR} \approx 0.48 \frac{e \hbar}{m^* \Lambda^2 \Delta^2 k_f^4 E_f^4} \left( 1 + \frac{2N_{\text{Depl}}}{n_s} \right)^{-2} \left( F(2k_f)[1 - G(2k_f)] + \frac{2k_f}{q_s} \right)^2
$$

Where, $m^*$ is the hole effective mass, $k_f$ is the Fermi wave vector, $N_{\text{Depl}}$ and $n_s$ represent the charge arising from background doping depletion and the confined sheet carrier density respectively, $e$ and $\hbar$ represent the electronic charge and the Plank constant respectively, $E_f$ denotes the carrier energy and $G(q)$ represents the local field Hubbard correction (Emeles et al 1993)

The finite width of the two-dimensional carrier gas may be defined, using the form factor $F(q)$, as:

$$
F(q) = \frac{\left( 1 + \frac{9q}{8b} + \frac{3q^2}{8b^2} \right)}{\left( 1 + \frac{q^3}{b} \right)^3}
$$

The value of the 'variational parameter' is defined in section 4.2.5.
4.2.4.3 CHARGED INTERFACE IMPURITY SCATTERING.

The incorporation of charged impurity ions during growth also provides a further mechanism by which carrier mobilities may be degraded. Typically, MBE deposition occurs at a pressure of approximately $10^{-9}$ mbar. However, even under such 'clean' environments, the incorporation of some impurity contaminants is inevitable. Indeed, at the elevated temperatures required for the deposition of high quality strained layer heterostructures, the diffusion of any metallic contaminants poses a particular problem (Smith et al 1992). In particular, the strained layer hetero-interface may act as an efficient gettering site and accumulate impurities.

The Coulomb field associated with such impurity ions again acts to scatter charge carriers in a similar manner to that described in section 4.2.4.1. However, in the case of charged interface impurity scattering at the heterointerface, the reduced proximity between the carrier gas and the charged impurity ions results in considerable degradation to the confined carrier mobility.

4.2.4.4 ALLOY SCATTERING.

The random distribution of Ge atoms within the two-dimensional confinement channel gives rise to potential fluctuations on an atomic scale. Such random potential fluctuations act as scattering sites, which hinder carrier motion and result in a degradation of the carrier mobility. Bastard (1984)
assumed such Ge compositional fluctuations to vary about a mean value $x$, and derived a general expression for the mobility $\mu$, due to such alloy scattering:

$$\mu = \frac{16e\hbar^3 N_o}{3(m^*)^2 (\Delta E)^2 x(1-x)b}$$

where, $m^*$ represents the effective hole mass, $N_o$ the atomic concentration, $\Delta E$ the scattering potential and $b$ denotes the variational parameter defined in section 4.2.4.1.

4.2.4.5 LATTICE VIBRATION (PHONON) SCATTERING.

A further mechanism by which confined carriers may be scattered may be attributed to the inherent atomic vibrations of the actual crystalline lattice. The longitudinal vibrations of the crystalline lattice, known as phonons, affect the lattice periodicity and result in local changes in potential on the atomic scale. A theoretical description of phonon scattering is beyond the scope of the current work, however the reader is referred to the work of Bardeen and Shockley (1950). It should be noted that the magnitude of phonon scattering events is markedly decreased at the low temperatures discussed in the present study, however the mechanism has a pronounced effect on carrier transport at room temperatures.
4.3 THE EFFECT OF GROWTH TEMPERATURE ON THE ELECTRONIC PROPERTIES OF THE $\text{Si}_{0.5}\text{Ge}_{0.5}/\text{Si}_{0.7}\text{Ge}_{0.3}$ HETEROSYSTEM.

4.3.1 INTRODUCTION.

In the present section the effect of growth temperature on the low temperature (4K) electronic properties of the strained layer $\text{Si}_{0.5}\text{Ge}_{0.5}/\text{Si}_{0.7}\text{Ge}_{0.3}$ 2DHG heterosystem is addressed. Since phonon scattering events are reduced, the low temperature mobility provides a useful determination of the material quality of such heterostructures. Previous workers have demonstrated an increase in the hole mobility of various $\text{Si}_{1-x}\text{Ge}_x$ pseudomorphic depositions as the growth temperature is increased, however at higher growth temperatures a decrease in the magnitude of the hole mobility is observed. This is generally associated with the onset of 3-dimensional strained layer roughening which provides an important scattering mechanism (see section 3.2iii). This scattering mechanism is particularly prevalent at the high sheet densities required for device applications (Whall et al 1997). The effect of growth temperature on the electrical properties of strained layer, pseudomorphic 2DHG structures of atomic Ge content 6-8%, and 12-14% and Ge contents of 20% and 30% have been investigated previously (Basaran et al 1994 and McGregor 1997 respectively). As mentioned previously there is a significant advantage in using alloy structures of high Ge contents. However, there have been no previous
studies of the effect of growth temperature within the Si$_{0.7}$Ge$_{0.3}$/Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ 2DHG heterosystem deposited by MBE.

The current work sets out to extend these studies to Ge contents of 50%. However, at the large strain energies involved in the pseudomorphic growth of Si$_{0.3}$Ge$_{0.7}$ alloy layers, a critical thickness of approximately 2-3nm is imposed (see section 3.4). A two-dimensional carrier gas, confined within such a thin channel, will experience significant scattering due to the overlap of the carrier wavefunction with the relaxed layers. In order to overcome this issue, the strained Si$_{0.5}$Ge$_{0.5}$ confinement channel was deposited on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate. In this manner, the reduced mismatch strain allows the commensurate growth of a significantly thicker confinement channel. Table 4.3.1 shows the optimum growth temperature as a function of strained layer Ge content for various pseudomorphic 2DHG heterostructures grown by solid source MBE (after Basaran et al. 1994 and McGregor 1997).
<table>
<thead>
<tr>
<th>Ge Fraction (%</th>
<th>Optimum Mobility (cm²/Vs)</th>
<th>Sheet Density (cm²)</th>
<th>Optimum Growth Temp (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6-8</td>
<td>17,800</td>
<td>6 x 10^{10}</td>
<td>900</td>
</tr>
<tr>
<td>12-14</td>
<td>7000</td>
<td>3 x 10^{11}</td>
<td>850</td>
</tr>
<tr>
<td>20</td>
<td>6100</td>
<td>3 x 10^{11}</td>
<td>650</td>
</tr>
<tr>
<td>30</td>
<td>2510</td>
<td>5 x 10^{11}</td>
<td>530</td>
</tr>
</tbody>
</table>

Table 4.3.1:
Depicts the optimum growth temperature of various pseudomorphic 2DHG structures grown by solid source MBE. Low temperature (4K) mobility data and the corresponding sheet carrier densities are also given.

4.3.2 EXPERIMENTAL.

In order to determine the effect of growth temperature on the low temperature (4K) hole mobility of the Si_{0.5}Ge_{0.5}/Si_{0.7}Ge_{0.3} 2DHG heterosystem, various depositions were performed using solid source MBE on relaxed, linearly-graded virtual substrates. The relaxed, linearly-graded virtual substrates were deposited, to the present authors specifications, using a
commercially available UHV-CVD reactor at NRC, Canada (Lafontaine et al 1996b).

The growth chamber of the reactor consists of a quartz tube, evacuated by a turbomolecular/roots blower/rotary pumping system. Base pressures of approximately $1.5 \times 10^{-9}$ mbar are typical. Substrate heating occurs using a ‘hot wall’ technique in which the whole growth chamber is surrounded with a heated shroud. In this manner, a highly uniform substrate temperature occurs throughout the reactor. $\text{Si}_{1-x}\text{Ge}_x$ deposition occurs due to the introduction of Silane, $\text{SiH}_4$ (100%) and Germane, $\text{GeH}_4$ (10% in Helium) gases, typically at a flow rate of 30 sccm and 10-20 sccm respectively. The working pressure during growth was approximately $10^{-3}$ mbar (Lafontaine 1997). This results in a growth rate of approximately 5 nm/min. Using the UHV-CVD reactor, deposition may occur on a maximum of 25 4” Si(001) wafers simultaneously. Typically a variation in Ge content of up to 2% occurs across the 25 wafers, whilst each wafer has a maximum Ge variation of $\pm 0.15\%$ (Lafontaine et al 1996b).

Prior to UHV-CVD deposition of the virtual substrates, the Si(001) 4” wafers were cleaned using a modified RCA procedure followed by a 10 second dip in 10% dilute hydrofluoric acid (HF). The growth of the relaxed, linearly-graded virtual substrates commenced with the deposition of a compositionally graded $\text{Si}_{1-x}\text{Ge}_x$ region, with $x$ varying linearly from 0% to 30%. The total thickness of the buffer layer was approximately 2 µm. The structure was then terminated with the deposition of a uniform $\text{Si}_{0.7}\text{Ge}_{0.3}$ region to a thickness of 0.5 µm. All UHV-CVD deposition was performed at a substrate temperature of
525°C. The virtual substrates were characterised using Atomic Force Microscopy (AFM) and Auger Electron Scattering (AES).

The deposition of the active device region of the Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ 2DHG heterosystem was performed using solid source MBE at Warwick. Prior to MBE deposition the virtual substrates were again cleaned using a standard RCA procedure, dipped in 10% HF and spun dry. In all cases, the electrically active 2DHG region consisted of the deposition of 250nm Si$_{0.7}$Ge$_{0.3}$ buffer layer, followed by a 7nm Si$_{0.5}$Ge$_{0.3}$ compressively strained 2DHG confinement channel and a 15nm Si$_{0.7}$Ge$_{0.3}$ relaxed, spacer layer. The 2DHG carriers were provided by the growth of a 50nm Si$_{0.7}$Ge$_{0.3}$ layer, doped with boron to a concentration of $2 \times 10^{18}$ cm$^{-3}$. The MBE deposition was terminated with a 3nm tensile strained Si cap layer.

In order to determine the effect of growth temperature on the electronic properties of the Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ 2DHG heterosystem the growth temperatures were varied from 450, 500, 550 and 600°C.

The electrical characteristics, from 4K to room temperature, of the Si$_{0.7}$Ge$_{0.3}$/Si$_{0.5}$Ge$_{0.3}$/Si$_{0.7}$Ge$_{0.3}$ 2DHG samples were determined using a Van der Pauw geometry in a helium cryostat. The method is described in section 2.4. Cross sectional TEM samples were obtained via mechanical thinning of the wafer to a thickness of approximately 30μm, followed by Ar-ion sputtering until the sample was electron transparent (approximately 200nm thick). The method is described in section 2.3. The 2DHG heterostructure was structurally characterised using a JEOL JEM-2000fx transmission electron microscope operating at an accelerating voltage of 200keV.
4.3.3 RESULTS.

The surface morphology, as determined by AFM, of the UHV-CVD relaxed, linearly-graded virtual substrates is depicted in Fig 4.3.1. The image was taken *prior* to MBE heteroepitaxial deposition of the electrically active Si$_{0.5}$Ge$_{0.5}$ 2DHG region. The image depicts the surface morphology of the virtual substrate over an area of 10x10µm$^2$ and shows a highly developed cross-hatch roughening in the growth direction. Surface height fluctuations of approximate magnitude 2nm are evident. The origin of such cross-hatch roughening has been dealt with in detail in section 3.8 and is due to the cooperative stress fields associated with the Modified Frank-Read (MFR) dislocation pile-ups in the underlying relaxed buffer layer. It should be noted that the surface height fluctuations of the 'thick' UHV-CVD buffer layers are of a similar magnitude to those of the 10µm limited-area buffer layers described in section 3.8. However, the infinite-area buffer layers are expected to be significantly more relaxed.

Fig 4.3.2 depicts the variation in the low temperature (4K) hole mobility of the Si$_{0.7}$Ge$_{0.3}$/Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ 2DHG heterostructure as a function of growth temperature. In common with the pseudomorphic work of Basaran *et al* and McGregor a gradual increase in the low temperature hole mobility is observed as the growth temperature is increased. A mobility peak is then observed at a particular growth temperature and any subsequent increase in the growth temperature results in a decrease in the hall mobility of the 2DHG. It is evident from Fig 4.3.2 that the mobility peak in the
Fig 4.3.1
Atomic force micrograph (AFM) of the surface morphology of a relaxed, linearly graded virtual substrate grown by UHV-CVD. The terminating Ge content of the buffer was 30%. The image represents a scanned area of 10x10µm and shows RMS surface height fluctuations of approximately 2nm.
Fig 4.3.2: Variation in low temperature (4K) hole mobility and sheet carrier density as a function of growth temperature of a Si$_{0.5}$Ge$_{0.5}$ 2DHG deposited by MBE on a relaxed, linearly-graded Si$_{0.7}$Ge$_{0.3}$ virtual substrate grown by UHV-CVD.
Si$_{0.7}$Ge$_{0.3}$/Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ 2DHG heterosystem occurs at a growth temperature of approximately 550°C and results in a maximum hole mobility of 1820 cm$^2$/Vs at a sheet carrier density of 5.2x10$^{11}$ cm$^{-2}$.

Figs 4.3.3 and 4.3.4 depict cross sectional TEM images of the heterostructures deposited by MBE on UHV-CVD relaxed virtual substrates at a growth temperature of 450°C and 600°C respectively. A highly uniform, smooth Si$_{0.5}$Ge$_{0.5}$ 2DHG confinement channel is observed at a growth temperature of 450°C, whilst the identical channel deposited at 600°C shows a significant degree of surface roughening.

However, it is evident from Fig 4.3.2 that low temperature hole mobility of the 'roughened' 600°C 2DHG, 1280 cm$^2$/Vs is far in excess of the corresponding 2DHG mobility, 77 cm$^2$/Vs, of the 'smooth' 450°C deposition. Clearly, the dominant mobility limiting mechanism in the present work cannot be attributed to interface roughness scattering.

4.3.4 DISCUSSION.

In general, solid source MBE (SSMBE) is not the ideal epitaxial growth technique required for the growth of the 'thick' epitaxial layers (eg relaxed buffer layers) used in the present work. Prior to SSMBE deposition, the growth flux evaporated from each of the Si and Ge source charges are calibrated at a given e-beam power density. However, as the source charges (particularly the Si source) are depleted during growth, the original calibration standard becomes increasingly less accurate. This may be attributed to the evaporating
Cross sectional TEM image of a 7nm compressively strained $\text{Si}_{0.5}\text{Ge}_{0.5}$ 2DHG confinement channel (dark band) grown by MBE on a relaxed $\text{Si}_{0.7}\text{Ge}_{0.3}$ virtual substrate. The growth temperature of the confinement channel was 450°C.
Cross sectional TEM micrograph of a 7nm compressively strained Si$_{0.5}$Ge$_{0.5}$ 2DHG confinement channel (dark band) deposited by MBE on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate. The channel deposition was performed at 600°C.
e-beam flux producing uneven erosion of the originally smooth source charges. This results in a variation in the original growth rate calibration. In the case of the thick depositions, of the order of microns, which are required to provide the high quality virtual substrates used in the present work, such a growth rate variation provides a formidable obstacle to the SS-MBE grower. Furthermore, since the growth of single wafers is only available within the MBE chamber at any one time, the deposition of single virtual substrates is expensive.

In order to overcome such problems the use of virtual substrates deposited using UHV-CVD provides a promising option. During UHV-CVD growth a constant gas source is available and hence the original calibrated deposition rate is reliable throughout the deposition of thick buffer layers. Furthermore, since a total of 25 wafers may be placed within the growth chamber at any one time, the deposition of such thick buffer layers is much more cost effective and less time consuming.

At the time of the present study and to the best of the present author's knowledge, the deposition of electrically active regions using SSMBE on UHV-CVD virtual substrates remained an un-investigated field of research.

The union of SSMBE and UHV-CVD in a hybrid growth technique provides a unique opportunity to investigate the electrical properties of the Si_{0.7}Ge_{0.3}/Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3} 2DHG heterosystem as a function of growth temperature. In particular, the deposition of the relatively thin electrically active regions using SSMBE enables the growth temperature to be varied independently of the growth rate whilst the calibrated growth rate remains consistent. Such an option is not available during UHV-CVD deposition since
in the latter case the growth rate is particularly sensitive to the growth temperature.

Fig 4.3.2 depicts the low temperature 2DHG mobility and sheet density as a function of growth temperature for the Si_{0.7}Ge_{0.3}/Si_{0.5}Ge_{0.5}/Si_{0.7}Ge_{0.3} heterosystem; the results are summarised in table 4.3.2.

<table>
<thead>
<tr>
<th>Growth Temperature (°C)</th>
<th>Hole Mobility (cm²/Vs)</th>
<th>Sheet Density (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>450</td>
<td>77</td>
<td>4.5x10¹¹</td>
</tr>
<tr>
<td>500</td>
<td>760</td>
<td>5.3x10¹¹</td>
</tr>
<tr>
<td>550</td>
<td>1820</td>
<td>5.2x10¹¹</td>
</tr>
<tr>
<td>600</td>
<td>1275</td>
<td>6.1x10¹¹</td>
</tr>
</tbody>
</table>

Table 4.3.2:

Low temperature (4K) hole mobility and corresponding sheet density of the Si_{0.7}Ge_{0.3}/Si_{0.5}Ge_{0.5}/Si_{0.7}Ge_{0.3} heterosystem as a function of growth temperature.

As the growth temperature of the active 2DHG region is increased from 450°C to 550°C the hole mobility is observed to increase by in excess of an order of magnitude from 77cm²/Vs to 1820cm²/Vs. It is the present author’s opinion that the reduced mobility of the low temperature deposition may be attributed to high densities of as-grown imperfections within the crystalline lattice.
In section 3.2, the BCF theory of planar two-dimensional epitaxial growth was introduced. In particular, the migration and incorporation of surface adatoms was determined to play a crucial role in such planar growth modes. Due to kinetic considerations, the surface adatom mobility is reduced at reduced growth temperatures, thereby limiting adatom migration. Furthermore, migrating adatoms, which are unable to incorporate at a terrace edge, may be incorporated at an 'incorrect' lattice site by subsequent depositions. As a result of such a micro-defective lattice, carrier scattering events are increased and are indicative of the observed reduction in the low temperature hole mobility of the confinement channel deposited at 450°C.

Fig 4.3.4 depicts a high magnification, cross sectional TEM image of the Si_{0.5}Ge_{0.5}/Si_{0.7}Ge_{0.3} heterostructure, which was deposited at a growth temperature of 600°C. It is evident that such a confinement channel suffers from a high degree of roughening. The origin of such roughening has been discussed in section 3.2 and may be attributed to the onset of three-dimensional growth. (see Fig 3.2.2(c)). The mobility limiting mechanism, which is most prevalent at the high sheet densities used in the present work, is generally associated with roughness scattering.

It is postulated that although the confinement channel is of superior crystalline quality, the low temperature hole mobility of the 600°C channel is limited by interface roughness scattering.

The peak hole mobility, observed for the 550°C deposition, may be considered as the optimum compromise between crystalline quality and roughness dominated scattering events. Fig 4.3.5 depicts the variation in hole
Fig 4.3.5: Variation in mobility and sheet carrier density as a function of temperature for a \( \text{Si}_{0.5}\text{Ge}_{0.5} \) 2DHG deposited by MBE at an optimised growth temperature of 550°C on a relaxed, linearly-graded UHV-CVD virtual substrate.
mobility and sheet carrier density as a function of temperature for a Si$_{0.5}$Ge$_{0.5}$ 2DHG deposited by MBE at an optimised growth temperature of 550°C, on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate.

As the growth temperature is increased, a similar mobility peak has been observed in carrier confinement channels of various Ge contents. Basaran et al have investigated the effect of growth temperature on the hole mobility of pseudomorphic confinement channels of Ge contents 7% and 13% (Basaran et al 1994). A similar investigation has been undertaken by McGregor et al, in which 20% and 30% pseudomorphic confinement channels were studied (McGregor et al 1998). The results are summarised in Fig 4.3.6. In all cases, a peak in the low temperature hole mobility is observed as the growth temperature of the heterostructure is increased. Above this peak a decrease in mobility is observed at increasingly higher growth temperatures.

Furthermore, it is evident from Fig 4.3.6 that the mobility peak of the various heterosystems occur at an increased growth temperature as the Ge content of the pseudomorphic confinement channel is reduced. Such a trend is consistent with the observations of the present work. As the Ge content of the pseudomorphic confinement channel is increased, the increased lattice mismatch strain induces strain relief, via the onset of three-dimensional growth, to occur at a reduced growth temperature. As a result of the associated roughness scattering, the mobility peak of the individual systems occur at reduced growth temperatures as the Ge content of the channel is increased. Furthermore, as a consequence of the reduced growth temperature, the increased incorporation of lattice imperfections is inevitable. Again, such
Fig 4.3.6:
Low temperature (4K) hole mobility versus growth temperature for various psuedomorphic and virtual substrate Si/SiGe heterostructures. □ x=7%, \(N_s=6\times10^{10}\, \text{cm}^{-2}\); ▲ x=13%, \(N_s=3\times10^{11}\, \text{cm}^{-2}\); O x=20%, \(N_s=3\times10^{11}\, \text{cm}^{-2}\); ● x=30%, \(N_s=5\times10^{11}\, \text{cm}^{-2}\) and ○ x=50% Ge, \(N_s=5\times10^{11}\, \text{cm}^{-2}\) fraction on a relaxed \(\text{Si}_{0.7}\text{Ge}_{0.3}\) virtual substrate. (□, ▲ psuedomorphic after Barsaran et al; O, ● psuedomorphic after McGregor; ○ virtual substrate current work)
imperfections degrade carrier performance and a general decrease in the individual mobility peaks is observed as the growth temperature is reduced.

The mobility variation of the pseudomorphic Si$_{0.8}$Ge$_{0.2}$ heterostructure provides an interesting comparison with the present work. Due to the identical lattice mismatch between the Si$_{0.8}$Ge$_{0.2}$/Si system and the Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ heterosystem discussed in the present work, the mobility maxima may be expected to occur at similar temperatures. However, the mobility peak of the Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ is observed to occur at a significantly lower growth temperature than that of the Si$_{0.8}$Ge$_{0.2}$/Si system (550°C and 700°C respectively). It is evident from Fig 4.3.1 that the relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate suffers from a significant degree of cross-hatch roughening due to the underlying misfit dislocations. It is the present author's opinion that the strain fields associated with the cross hatch roughening may act as a pre-cursor, promoting three-dimensional growth at a reduced growth temperature. In addition, the effect of Ge content on the surface adatom mobility may also play an important role, but is beyond the scope of the present work.

4.3.5 CONCLUSIONS.

A systematic study of the effect of growth temperature on the electrical properties of the Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ heterosystem has been undertaken. A maximum low temperature hole mobility of 1820 cm$^2$/Vs at a sheet carrier density of $5.2 \times 10^{11}$ cm$^{-2}$ was observed for depositions at 550°C. In common with the work of Basaran and McGregor, a decrease in the confined hole
mobility was observed at growth temperatures in-excess of the optimum 550°C deposition. Similarly a decrease in hole mobility was observed as the growth temperature was reduced below 500°C.

The reduced hole mobility at growth temperatures in excess of 550°C may be attributed to surface roughness scattering events, due to the onset of 3-dimensional strained layer surface roughening (see Fig 4.3.4). In addition, it is postulated that the observed decrease in mobility, as the growth temperature is reduced below 550°C, may be attributed to an increase in as-grown lattice imperfections.

The result may have implications to the possible integration of such heterostructures within p-MOS and CMOS devices. In section 4.2.2 the requirement of high sheet density, low resistance heterostructures for use within such devices was discussed. The results discussed in the current work indicate that in order to avoid the effects of 3-dimensional growth roughening, the growth temperature of highly mis-matched confinement channels must be reduced. However, at low growth temperatures it is postulated that reduced adatom migration results in an increase in as grown lattice imperfections. Such imperfections again act as scattering sites and cause a decrease in the confined carrier mobility.
4.4 THE EFFECT OF POST GROWTH ANNEALS ON THE ELECTRICAL PROPERTIES OF THE $\text{Si}_{0.5}\text{Ge}_{0.5}/\text{Si}_{0.7}\text{Ge}_{0.3}$ HETEROSYSTEM.

4.4.1 INTRODUCTION.

In the present section the poor electrical characteristics of the low temperature (450°C) $\text{Si}_{0.5}\text{Ge}_{0.5}/\text{Si}_{0.7}\text{Ge}_{0.3}$ 2DHG depositions are discussed and a method by which the elimination of as-grown lattice defects via post-growth, thermal anneal treatments is investigated. Various post-growth anneal trials, both ex-situ and in-situ, were performed and the electrical performance of such samples ascertained. Explanations for the observed variation in the electronic properties of the 2DHG are given, as a function of both anneal temperature and duration.

The section concludes by explaining the limitations of the current epitaxial growth system and provides a number of suggestions which, in the authors opinion, should be investigated in detail so as to achieve the complete, optimised $\text{Si}_{0.5}\text{Ge}_{0.5}/\text{Si}_{0.7}\text{Ge}_{0.3}$ 2DHG heterostructure.

4.4.2 EXPERIMENTAL.

The electrically active region of the heterostructure was again deposited by SS-MBE at a growth temperature of 450°C, in the manner described in
section 4.3.2. However, in this case, MBE deposition commenced with a 3nm Si channel which acted as a marker channel, enabling the UHV-CVD/MBE interface to be determined using cross-sectional TEM. The tensile-strained Si channel has a negligible valence band offset and is not deemed to be responsible for any hole confinement at low temperatures (Bean et al 1984). The wafer was catalogued 54/41.

The wafer was structurally characterised using cross-sectional TEM (XTEM) to determine the magnitude of the strained layer roughening, the method is described in section 2.3.

Post growth ex-situ anneals were performed at temperatures of 650, 700, 750, 800 and 850°C for a duration of 5, 15 and 30 minutes in a N$_2$ ambient. The electrical characterisation of all samples, including the as-grown un-annealed performance, was determined using a Van der Pauw geometry in a low temperature (10K) closed-cycle helium cryostat. The method is described in section 2.4.

Once the optimum ex-situ, post-growth anneal conditions had been determined, an exact replica of the 2DHG heterostructure was deposited using MBE, again on a UHV-CVD virtual substrate. In this case an in-situ, post-growth anneal was performed under the optimum conditions determined from the ex-situ anneal trials. The in-situ anneal was performed at a base pressure of approximately 5x10$^{-9}$mbar. In this manner, the effect of contamination which may occur during the high temperature ex-situ anneal could be ascertained. This wafer was catalogued 55/36. The in-situ substrate temperature was determined using an optical pyrometer measurement located outside the MBE
chamber. The substrate was viewed through a quartz window. Due to the large distance between the substrate and pyrometer, together with the absorption which occurs within the quartz window (un-calibrated at the time of going to print), a finite amount of radiation emitted from the heated substrate remains undetected. This results in a temperature measurement error of approximately ±40°C (Parry, Phillips and Naylor 1997). Both the as grown, un-annealed wafer (54/41) and the in-situ annealed wafer (55/36) were characterised using secondary ion mass spectroscopy (SIMS) in order to determine the magnitude of Ge and B out diffusion which may occur during the high temperature anneal treatment.

4.4.3 RESULTS.

Fig 4.4.1 shows the cross-sectional TEM micrograph of the electronically active region of the Si_{0.5}Ge_{0.5}/Si_{0.7}Ge_{0.3} 2-dimensional hole gas heterostructure grown by MBE on a relaxed virtual substrate. The darker band represents the actual 7nm compressively strained Si_{0.5}Ge_{0.5} 2DHG confinement channel. A highly planar strained layer deposition is observed due to the 2-dimensional growth mode, which occurs at the low growth temperature of 450°C. Generally, no threading dislocations were observed during XTEM characterisation, confirming that the threading dislocation density was below the observable limits of the XTEM technique (approximately 10^6 cm^{-2}).

The Hall mobility of the as-grown sample was determined to be 77 cm^2/Vs at 10K with a corresponding sheet carrier density of 5 \times 10^{12} cm^{-2}. 

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High magnification cross-sectional transmission electron micrograph image of a 7nm compressively strained Si$_{0.5}$Ge$_{0.5}$ confinement channel (dark band). The channel was deposited at 450°C, using SSMBE, on a relaxed Si$_{0.7}$Ge$_{0.3}$ virtual substrate. The growth was completed with the deposition of a 50nm Si$_{0.7}$Ge$_{0.3}$ cap layer.
This poor result cannot be attributed to strained layer roughening effects, since a highly planar 2-dimensional growth mode is evident from the cross-section TEM micrograph of Fig 4.4.1.

The effect of the various ex-situ anneals on the electronic properties of the Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ 2-dimensional hole gas heterostructure are depicted in table 4.4.1 and the corresponding hole mobility and sheet carrier densities as a function of ex-situ, post growth anneals are presented in Fig 4.4.2.

A maximum mobility of 818 cm$^2$/Vs and a corresponding sheet carrier density of $1.5 \times 10^{12}$ cm$^2$ is achieved for an ex-situ, post growth anneal of 750°C for 30 minutes. This represents an increase in the Hall mobility of in excess of an order of magnitude over the as-grown result.

A further MBE growth was performed replicating the optimum post-growth anneal conditions of 750°C for a duration of 30 minutes (wafer 55/36). However, in this case the anneal was performed in-situ immediately after the completion of the MBE deposition. Fig 4.4.3 depicts the temperature variation in hole mobility and the corresponding sheet carrier density for the in-situ, post-growth annealed sample. A maximum mobility of 2044 cm$^2$/Vs and a sheet carrier density of $5.0 \times 10^{11}$ cm$^2$ is achieved at 4K. This represents a 25-fold improvement in hole mobility compared to the identical deposition which did not undergo any post-growth anneal treatment.

However, a large decrease in the sheet carrier density of the annealed 2DHG is observed, typically from $1.7 \times 10^{12}$ to $5 \times 10^{11}$ cm$^2$. Such a decrease in the confined sheet carrier density of the in-situ annealed 2DHG may be attributed to the out-diffusion of Ge from the confinement channel. Fig 4.4.4
Fig 4.4.2:
Depicts the effect of ex-situ, post growth anneals on the mobility and the corresponding sheet density variation of a Si$_{10}$Ge$_{0.5}$ 2DHG grown by MBE on a relaxed, linearly graded UHV-CVD buffer layer. Post growth ex-situ anneals of durations 5 minutes (a), 15 minutes (b) and 30 minutes (c) were performed.
Fig 4.4.3:
Variation in mobility and sheet carrier density as a function of temperature for a Si$_{0.5}$Ge$_{0.5}$ 2DHG deposited by MBE on a relaxed, linearly graded Si$_{0.7}$Ge$_{0.3}$ UHV-CVD virtual substrate at a growth temperature of 450°C. The wafer underwent an optimised post growth, in-situ anneal of 750°C for a duration of 30 minutes.
Fig 4.4.4
Secondary Ion Mass Spectroscopy (SIMS) profile depicting the effect of post growth anneal treatment on the Ge content of the 2DHG confinement channel. The SIMS profile was performed at an energy of 500eV using a $O_2^+$ beam.
depicts the SIMS analysis of both the 2DHG deposited at 450°C (wafer 54/41) and a similar sample which underwent an in-situ, post growth anneal of 750°C for 30 minutes. It is evident from such data that the in-situ anneal results in a significant amount broadening of the Si$_{0.7}$Ge$_{0.3}$ quantum well, producing a substantial reduction in the Ge content of the confinement channel and a corresponding decrease in the confined sheet carrier density (see section 4.2.2).
<table>
<thead>
<tr>
<th>Ex-situ anneal</th>
<th>In-situ growth anneal</th>
<th>Hole mobility (cm²/Vs)</th>
<th>Sheet carrier density (cm²)</th>
</tr>
</thead>
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<tr>
<td>(wafer 54/41)</td>
<td>(wafer 55/36)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5mins 650°C</td>
<td></td>
<td>127</td>
<td>5.00 x 10¹²</td>
</tr>
<tr>
<td>5mins 700°C</td>
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<td>5.00 x 10¹²</td>
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<td>5mins 750°C</td>
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<td>278</td>
<td>2.80 x 10¹²</td>
</tr>
<tr>
<td>5mins 800°C</td>
<td></td>
<td>492</td>
<td>2.10 x 10¹²</td>
</tr>
<tr>
<td>5mins 850°C</td>
<td></td>
<td>492</td>
<td>1.90 x 10¹²</td>
</tr>
<tr>
<td>15min 700°C</td>
<td></td>
<td>366</td>
<td>1.94 x 10¹²</td>
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<tr>
<td>15min 750°C</td>
<td></td>
<td>630</td>
<td>1.70 x 10¹²</td>
</tr>
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<td>15min 800°C</td>
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<td>670</td>
<td>1.74 x 10¹²</td>
</tr>
<tr>
<td>15min 850°C</td>
<td></td>
<td>603</td>
<td>1.70 x 10¹²</td>
</tr>
<tr>
<td>30 min 600°C</td>
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<tr>
<td>30 min 750°C</td>
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</tr>
<tr>
<td>30 min 800°C</td>
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<td>556</td>
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</tr>
<tr>
<td>30 min 750°C</td>
<td></td>
<td>2044</td>
<td>5.0 x 10¹¹</td>
</tr>
</tbody>
</table>

Table 4.4.1.

Measured low temperature (10K) hole mobilities and their respective sheet carrier densities for samples having undergone various ex-situ and in-situ anneals.
4.4.4. DISCUSSION.

The effect of post-growth anneals on the structural properties of a pseudomorphic Si$_{0.7}$Ge$_{0.3}$ 2DHG has been investigated by Lafontaine et al using photoluminescence (PL) techniques on UHV-CVD material grown at 525°C. A large shift in the PL spectrum was observed following a rapid thermal anneal (RTA) at 850°C for a duration of 300 seconds, when compared to the as-grown sample. However, no shift was observed in the PL spectrum for samples which underwent a long pre-anneal stage of 600°C for 24 hours followed by an identical RTA anneal. In this case, an identical PL spectrum was observed compared to the as-grown sample. The PL spectrum of the pre-annealed sample also coincided with that of the as-grown deposition, providing strong evidence that the initial interdiffusion of the RTA sample was not primarily aided by a strain driven mechanism. It was concluded that the initial interdiffusion was greatly reduced after the pre-anneal stage due to a reduction in the concentration of as-grown point defects within the strained quantum well. Such defects provide interstitial sites, which aid the out-diffusion of Ge from the SiGe confinement channel. Furthermore, 'It was concluded that material grown at a lower temperature will contain more point defects at a given growth rate, because of the reduced surface adatom mobility' (Lafontaine et al 1996a).

In the current work a gradual increase in the hole mobility is observed as the anneal temperature and duration is increased to a optimum of 750°C for 30 minutes. In agreement with the work of Lafontaine et al (Lafontaine et al 1996 see also Grasby et al 1998), this increase in hole mobility during the high
temperature anneal treatment may be attributed to the elimination of point defects from within the Si$_{0.5}$Ge$_{0.5}$ 2DHG channel. This occurs via the movement of point defects away from the quantum well region. Such point defects act as scattering sites and result in a reduction in the mobility of the 2DHG. It is evident from Fig 4.4.2 that the hole mobility gradually increases as the ex-situ, post growth anneal temperature is increased.

As the temperature and duration of the ex-situ anneal treatment was increased in excess of the observed optimum conditions a reduction in the carrier mobility was eventually observed. This may be attributed to enhanced dopant diffusion towards the confinement channel. Since the ionised boron dopant atoms have a net negative charge, charge carriers within the 2DHG channel experience a Coulomb attraction towards the ionised impurities. The magnitude of the Coulomb attraction is inversely proportional to the square of the spatial separation of the 2DHG carriers and the dopant impurity ions. The enhanced dopant diffusion which occurs at higher temperatures and increased anneal durations results in an increase in the magnitude of ionised impurity scattering, again hindering carrier motion and resulting in a reduction of the confined hole mobility.

The identical 2DHG system which underwent an optimised in-situ, post growth anneal of 750°C for 30 minutes shows a 25-fold increase in hole mobility when compared to an identical deposition with no post growth anneal. However, the corresponding sheet carrier densities were observed to decrease from 1.7x10$^{12}$ to 5.0x10$^{11}$cm$^{-2}$. Indeed, a large shift in the energy band profile has been observed during PL measurements of 2DHG systems having
undergone a post growth anneal of 850°C for 300 seconds when compared to an identical sample with no post growth anneal (Lafontaine et al 1996). As was discussed in section 4.4.2, the accuracy of the pyrometric substrate temperature measurement used in this work is approximately ±40°C. The reduction in the observed sheet carrier density of the in-situ post growth annealed sample may be linked to this inaccuracy. Furthermore, due to the large thermal mass of the in-situ substrate heater, it is likely that the substrate underwent a post growth anneal for a duration far in excess of the intended condition. Again, this would result in the increased Ge diffusion from the confinement channel.

4.4.5 CONCLUSIONS.

Generally, the carrier mobility in strained layer SiGe/Si quantum wells grown by UHV-CVD are greater than those of identical depositions performed using MBE. The divergence between the two growth techniques is particularly prominent in the case of low temperature depositions. It is the present author’s opinion that the poor mobility obtained from low temperature MBE depositions may be attributed to an increased concentration of as-grown lattice defects. Typically, the growth rate of MBE (6-10nm/min) depositions is much greater than that of similar UHV-CVD (approximately 1 nm/min) depositions (Lafontaine et al 1996b). A 3-fold decrease in the magnitude of boron incorporation has been observed as the MBE growth rate is increased from 0.1nm/s to 2.8nm/s at identical growth temperatures (Parry et al 1991). Clearly,
the growth rate is a very important parameter to be considered during MBE depositions.

A reduced growth rate allows more time for surface adatom migration and incorporation at lattice sites. This results in a reduction in the density of as-grown lattice imperfections. In addition, due to the nature of solid source MBE deposition using electron beam evaporation, a large number of energetic Si and Ge ions are produced. Should the substrate becomes electrically charged during growth, ions may be attracted towards the substrate. Indeed, scintillations have been observed during MBE deposition on insulating silicon-on-insulator (SOI) substrates, this may be attributed to ionic bombardment. Such a bombardment may be a cause of lattice damage during growth and result in defective epilayers (Parry 1997).

Recently, the effect of hydrogen surfactant sources on the growth of strained layer SiGe quantum wells using MBE techniques has gained much interest. Generally, sharper atomic interfaces are obtained in the presence of the surfactant source (Lambert et al 1997), this is attributable to a reduction in the adatom surface mobility (Lafontaine 1997). Furthermore, strained layer surface roughening effects (see section 3.2iii) may be suppressed in the presence of a surfactant source (Lambert et al 1997). Again, this may be attributed to the reduction in adatom mobility since the surface adatom, particularly Ge, migration to the strain-relaxed surface peaks is suppressed (see section 3.2iii). However, as was discussed in section 4.3, a reduction in surface adatom mobility may suppress strained layer roughening, but results in degraded electrical characteristics of the quantum well system. This is due to an increase
in the density of as grown lattice imperfections. Indeed, in the present work, a simple post-growth anneal treatment has been shown to improve the electrical characteristics of the 2DHG system dramatically. The post-growth anneal treatment enables a reduction in the density of as-grown defects as lattice heating takes place.

It is the author’s opinion that the crucial factor, which is required for the growth of high quality, strained layer 2DHG systems is to maximise the surface adatom mobility. Whilst a hydrogen surfactant source may result in an improvement in the interface abruptness this is a direct consequence of the decrease in adatom mobility. A method of increasing the surface adatom migration is required for low temperature depositions. In this manner the deposited adatoms have the opportunity to bond to their correct crystalline lattice site. This may be achieved by drastically reducing the growth rate. However, a direct consequence of increasing the surface adatom migration, be it by the reduction in growth rate or the introduction of an ‘exotic’ surfactant source, will be the increased tendency for surface roughening to occur at a given temperature. Furthermore, as the Ge fraction of the quantum well region is increased to enable an enhancement in the density of the confined carriers, the associated strain will again promote further surface roughening. Again, the optimisation of such depositions will rely on a compromise between several ‘necessary evils’. Work should continue in this field.

It may be concluded from the present work on post-growth anneal treatments, that the optimum electrical properties of the Si_{0.5}Ge_{0.5}/Si_{0.7}Ge_{0.3} 2DHG system relies crucially on density of as-grown point defects, the out-
diffusion of Ge from the quantum well region and the diffusion of ionised impurities towards the confinement channel.

4.5 FURTHER WORK.

In current chapter, the effect of growth temperature on the electronic properties of the Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ heterostructure was ascertained. It was concluded that, in order to avoid the adverse effects of 3-dimensional roughness scattering and the incorporation of as grown lattice imperfections, an optimum compromise in the growth temperature must be used. Due to time constraints, the growth temperature of the individual depositions studied in the present work, were varied by 50°C. It is the author’s opinion, that further work is required in order determine the true optimum growth temperature. In particular the effect of growth temperature variations of ±10°C and ±20°C should be determined around the optimum deposition temperature of 550°C observed in the present study.

Furthermore, the effect of post growth anneal treatments on the electronic properties of the strained layer Si$_{0.5}$Ge$_{0.5}$/Si$_{0.7}$Ge$_{0.3}$ 2DHG heterosystem provides strong evidence of the detrimental effects of as-grown lattice defects. A major factor by which the density of such defects may be controlled may be attributed to the rate of deposition of the strained layer quantum well region of the heterostructure. In all depositions studied in the present work a nominal growth rate of 0.1nm/s was used. By reducing the growth rate, the effective
surface adatom migration may be increased. This enables adatoms to locate and bond to their correct lattice sites, rather than being ‘trapped’ at their deposited, non-crystalline location by the subsequent layer overgrowth. However, there will be an increased tendency for surface roughening to occur which again provides a further scattering mechanism by which the electronic properties of the Si\textsubscript{0.5}Ge\textsubscript{0.5}/Si\textsubscript{0.7}Ge\textsubscript{0.3} 2DHG heterosystem will be degraded.

An assessment of the effect of growth rate at a given growth temperature on the electronic properties of the Si\textsubscript{0.5}Ge\textsubscript{0.5}/Si\textsubscript{0.7}Ge\textsubscript{0.3} 2DHG heterosystem is a crucial issue which must be addressed. In this manner the effect of adatom migration may be determined at a given growth temperature. The use of an atomic hydrogen surfactant source may also provide valuable information with regard to the effect of decreasing atomic migration on the electrical properties of the 2DHG system.

The elimination of as-grown lattice defects via post-growth anneal treatments should also be addressed. In this manner, the low temperature deposition of highly planar, 2-dimensional carrier channels may be obtained and the as-grown point defect density may be reduced via anneal treatment. The use of a low temperature 600°C in-situ, post growth anneal for a duration of 24 hours provides a particularly promising option since the out-diffusion of both Ge and B would be inhibited.

Analysis of the high temperature anneal treatments using SIMS should enable the effect of Ge out-diffusion from the strained layer quantum well region to be assessed. Similarly the effect of B diffusion towards the 2DHG channel may also be determined as a function of post growth anneal treatment.
A method of eliminating B diffusion towards the 2DHG carrier channel may be envisaged by performing the anneal treatment prior to the deposition of the B doped supply layer. However, the accumulation of contaminants during this growth interrupt should be addressed. Furthermore, the linearly graded virtual substrate may relax further due to misfit extension along the base of the strained layer quantum well region (Iismail et al 1994). This relaxation effect will be more prevalent in the case of a high temperature anneal treatment prior to the deposition of the B doped supply layer. In this case, the threading arm of the elongating misfit dislocation is only pinned by the thickness of the relaxed (15nm) spacer region. However, in the case of the post-growth anneal treatment after the deposition of the B doped supply layer, the threading arm is pinned by a much greater thickness of relaxed over growth (i.e. the 15nm spacer layer and the 50nm B doped supply layer). In this case relaxation of the strained layer channel is energetically more difficult.

A further improvement to the post growth, in-situ anneal treatment may be envisaged through the use of an accurate substrate heating system. Throughout this work the error in the substrate temperature was some ± 40°C. At the time of going to print, such a substrate heating system was being commissioned within the MBE chamber. This substrate heater should allow the growth temperature to be controlled with a much greater degree of accuracy.
REFERENCES.

(in alphabetical order)


C.J. Emeleus, personal communication 1996.


relaxed, limited-area $\text{Si}_{1-x}\text{Ge}_x$ buffer layers” Appl. Phys. Lett. 71(17), 2517-2519 (1997).


R. Hull “Silicon Germanium High Speed Electronics” NATO Advanced Study Institute, Erice, Sicily Italy (1995).


F.K. LeGoues, B.S. Meyerson, J.F. Morar and P.D. Kirchner, ‘Mechanisms and conditions for anomalous strain relaxation in graded thin films and superlattices’, J. Appl. Phys. 71(9), 4230 (1992(b)).


J.A. McDonald “SiGe: Promise into reality” Elsevier Science Ltd 7(3) p38-41 (1994).


R. People ‘Indirect Bandgap of coherently strained Ge\textsubscript{x}Si\textsubscript{1-x} bulk alloys on <001> silicon substrates’ Phys. Rev. B 32(2), pg 1405 (1985).

R. People and J.C. Bean ‘Band alignments of coherently strained Ge\textsubscript{x}Si\textsubscript{1-x}/Si heterostructures on <001> Ge\textsubscript{y}Si\textsubscript{1-y} substrates’ Appl. Phys. Lett. 48(8), p538 (1986).


R. People, ‘Physics and Applications of Ge\textsubscript{x}Si\textsubscript{1-x}/Si Strained Layer Heterostructures’ IEEE J. of Quantum. Electronics 22(9), p1696 (1986).


S.Y. Shiryaev, J. Fleming and L.W. Petersen,’ On the nature of cross-hatch patterns on compositionally graded Si\textsubscript{1-x}Ge\textsubscript{x} alloy layers’ Appl. Phys. Lett. 64(24), 3305 (1994).


K.L. Wang, S.G. Thomas and M. O'Tanner, ‘SiGe Band Engineering for MOS, CMOS and Quantum Effect Devices’ to be published.

