Interface characteristics of $n-n$ and $p-n$ Ge/SiC heterojunction diodes formed by MBE deposition

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In this article, we report on the physical and electrical nature of Ge/SiC heterojunction layers that have been formed by MBE deposition. Using X-ray diffraction, atomic force microscopy and helium ion microscopy, we perform a thorough analysis of how MBE growth conditions affect the Ge layers. We observe the layers developing from independent islands at thicknesses of 100 nm to flat surfaces at 300 nm. The crystallinity and surface quality of the layer is shown to be affected by the deposition parameters and, using a high temperature deposition and a light dopant species, the layers produced have large polycrystals and hence a low resistance. The p-type and n-type layers, 300 nm thick are formed into Ge/SiC heterojunction mesa diodes and these are characterised electrically. The polycrystalline diodes display near ideal diode characteristics ($n < 1.05$), low on resistance and good reverse characteristics. Current-voltage measurements at varying temperature prove that all the layers have two-dimensional fluctuations in the Schottky barrier height (SBH) due to inhomogeneities at the heterojunction interface. Capacitance-voltage analysis and the SBH size extracted from I-V analysis suggest strongly that interface states are present at the surface causing Fermi-level pinning throughout the bands. A simple model is used to quantify the concentration of interface states at the surface.

I. INTRODUCTION

Silicon carbide (SiC) is a wide bandgap semiconductor that is a leading candidate to supercede Si in the power electronics market due to its superior physical properties. Twenty years of material development has seen many of the processing techniques mature and the quality of the substrates significantly improve, such that the substrates supplied today achieve a low defect density suitable for electronic devices. As far as devices are concerned, commercial Schottky Barrier diodes are now available[1]. However, metal-oxide-semiconductor field-effect transistor (MOSFET) devices are being held back by the lack of a reliable SiC-oxide solution. SiO_2 is commonly used as the gate oxide for SiC because, being the native oxide of SiC, it can easily be formed by oxidising the SiC surface. However, the build up of carbon[2,3] at the interface leads to a high density of interface traps causing a very low channel mobility[4].

A solution to finding a carbon-free interface was proposed whereby the SiO_2 is formed on the surface of a SiC/Si heterojunction, thus removing any carbon clusters[5,6]. A SiO_2/Si/SiC MOSFET would benefit from a carbon free SiO_2/Si interface which would therefore have minimal scattering events in the MOS channel[7]. With SiC making up the blocking region of the device, it would maintain superb blocking capabilities[8]. We have previously reported on the physical nature of the Si/SiC heterojunction interface which behaves like a Schottky Barrier diode; the Si having been formed by Molecular Beam Epitaxy (MBE)[9,10] and by Wafer Bonding (WB)[11].

More recently, we have reported on Ge/SiC heterojunctions[12,13] due to the materials even higher mobility (especially in p-type where the hole mobility is 5 times that of Si and 21 times that of SiC) and the development of very good Ge/High-K dielectric interfaces[14]. With the Ge having been deposited via MBE and given ohmic front and back contacts, Schottky-like behaviour was demonstrated with the structures displaying a turn-on voltage of only 0.3 V and an ideality factor less than 1.1. However, the thin 100 nm layers of Ge used grew in distinct islands resulting in a patch contact with resistive forward characteristics, an unacceptable situation were these structures to be used as a MOS channel.

In this paper, we will demonstrate the feasibility of MBE Ge/SiC heterojunction structures by physically and electrically characterising a new generation of the heterojunctions, with thicker 300 nm Ge layers heavily doped p-type and n-type. Using atomic force microscopy (AFM), helium ion microscopy (HIM), and X-ray diffraction (XRD), the physical analysis will concentrate on how the mismatched materials form during MBE growth, and how the variables of dopant type, layer thickness and deposition temperature, play a part in the formation of the layer.

In the electrical analysis, the current-voltage (I-V) re-

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sults from the layers are compared after circular transmission line measurement (CTLM) structures are used to compare the resistivity of the Ge layers. The Schottky-like characteristics of the diodes are analysed over a range of temperatures (-50^oC to 175^oC) in order to characterise the inhomogeneous nature of the interface, as originally described for the metal-semiconductor (M-S) interface by the Tung model[15–17]. C-V analysis suggests that interface states are present at the SiC surface. Hence, in the final part of this paper, a simple model is used to understand the nature of these states and their impact on the Fermi-level pinning of the SBH.

II. EXPERIMENTAL DETAILS

An n-type (0001) Si face, 4^o off axis, 4H-SiC wafer, purchased from Cree Inc with a 10 μm, lightly n-type doped ($1.4 \times 10^{15} cm^{-3}$) epitaxial layer, was used in this work. This was diced into 10×10 mm samples before germanium films were deposited using V100S MBE system. Prior to deposition, the wafer was cleaned using a RCA2 clean[18] (H_2O:HCl:H_2O_2, 5:1:1) followed by a hydrofluoric acid dip to remove any oxide formed during the RCA2 process. This cleaning process has been demonstrated[10] to be of high quality, providing minimal reverse leakage current. This was followed by a high temperature bake within the MBE system to desorb any remaining oxide and other contaminants. Layers of highly doped germanium, both n-type and p-type ($N_{D,Ge}, N_{A,Ge} = 5 \times 10^{19} cm^{-3}$), 300 nm in thickness, were deposited onto the SiC substrates at a rate of 0.1 $\AA s^{-1}$ with antimony and boron as the dopants. Growth temperatures of 200^oC and 500^oC were used for each doping type to form amorphous and polycrystalline layers respectively, and 600 nm of Ni was sputtered onto all the Ge surfaces (Ni has been shown[19] to form a low-resistance ohmic contact to Ge on a gallium arsenide substrate). The resulting layer was then patterned and etched into circular transmission line measurement (CTLM) structures and dots 200 μm and 400 μm in diameter. The dots were then formed into mesa diode structures by etching the remaining Ge, whilst the CTLM structures were protected from this step. Similarly, back contacts with CTLM structures were formed by sputtering Ni onto the back SiC surfaces where the doping is higher ($1 \times 10^{18} cm^{-3}$). The structures were further annealed at 300^oC in nitrogen ambient for 5 minutes.

Capacitance-Voltage (C-V) measurements were taken at room temperature using an Agilent Technologies B1500A Semiconductor Device Analyzer connected to a Materials Development Corporation 802-200 mercury probe. The same parameter analyzer was employed to carry out the CTLM measurements. The diodes were also subject to I-V analysis at varying temperature (IVT), from -50^oC to 175^oC (225-450 K) at 25^oC intervals. With the diodes placed in a Tenney environmental chamber, wire bonding directly to the nickel dots allowed heat proof wires to be run out to the Agilent Semiconductor Device Analyzer, which recorded the results. The temperature was controlled and monitored in the chamber by a Watlow Series 942 temperature controller, and verified using a Fluke 52 II Thermometer.

III. RESULTS AND DISCUSSION

A. Physical Analysis

For fabricating a heterojunction MOS device, the ideal Ge layer would be entirely crystalline with an atomically flat surface, a state which we cannot achieve due to the large lattice mismatch between the Ge and SiC (45%), that prevents the required layer by layer growth mode. Therefore the layers formed are polycrystalline, though the size and quantity of the polycrystals is dependent on the growth conditions. When performing epitaxial growth via MBE, there are many variables that have an influence on the quality of the finished layers. Here we will explore the effect of varying layer thickness, deposition temperature and dopant type. The benchmark layer for these tests is the n-type layer grown to a thickness of 300 nm at 500^oC. Against this standard layer, the significance of each MBE variable can be understood. Starting with layer thickness, we can build a clear picture of how the lattice-mismatched epitaxial layers form.

Figure 1 shows the AFM images of the Ge layers, formed epitaxially on SiC. The AFM micrographs show the surface quality on a reasonably large scale (25×25 μm). The surface roughness values (R_q) over this area for all the 300 nm heterojunction layers are summarised in Table I.

The thinnest heterojunction layer is shown in Figure 1b, where the layer was grown at high temperature to a thickness of only 100 nm. We previously carried out a full analysis on this layer[12], citing the Stranski Krastanov growth mode as the reason why the large islands form, with gaps almost down to the SiC between them. By comparing this image with Figure 1a, we can see that there is substantial improvement in the layer quality as it gets thicker. The islands have grown to the point where they have merged, with increasing Ge deposition filling in the gaps between the islands. To achieve a good Ge/oxide interface, the surface of the Ge would need to be as smooth as possible. With a surface roughness of only 6.7 nm the polycrystalline layer could easily be polished to a flat from here.

Figure 1c shows an n-type 300 nm layer that has been grown at only 200^oC, compared to the rest that have been grown at 500^oC. A trade off exists in selecting deposition temperature, as we first reported for 100 nm layers[12]. The raised deposition temperatures give polycrystalline layers, with low resistance but poor surface morphology, forming good contacts. Lower deposition temperatures give amorphous structures, which come close to achieving flat surfaces, but with poor contact resistance. Here,

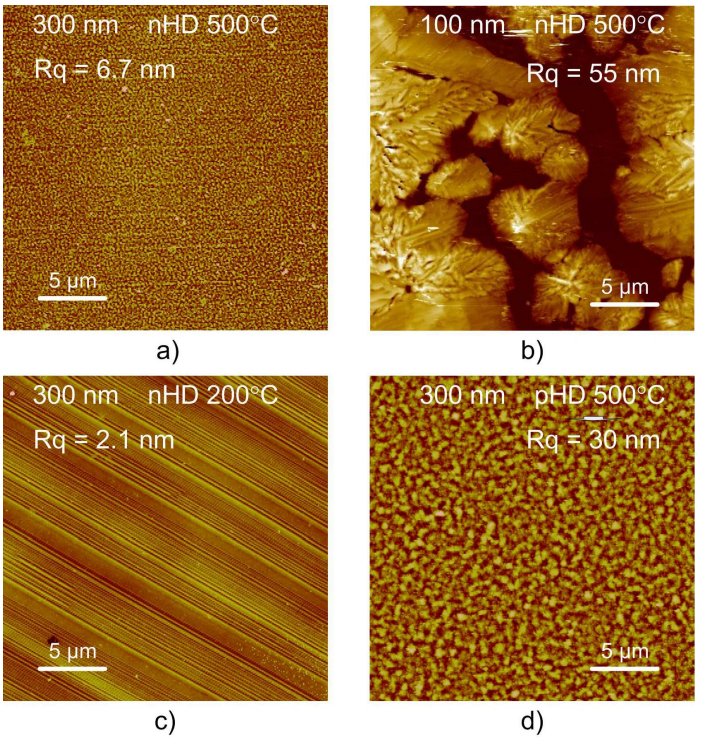

FIG. 1. AFM micrographs of the Ge/SiC layers, a study whereby a single MBE growth variable has been changed from the benchmark in each case. a) is the benchmark layer, 300 nm of n-type Ge grown at 500°C. b) is 100 nm of n-type Ge grown at 500°C. c) is 300 nm of n-type Ge grown at 200°C. d) is 300 nm of p-type Ge grown at 500°C.

in the micrograph of the 300 nm, low temperature deposition, SiC polishing marks may be seen despite the deposition of the Ge layer. This suggests a very uniform deposition that has done little to alter the SiC's original surface roughness of approximately 2 nm. The surface roughness value taken from this micrograph was 2.1 nm. By contrast, Fig. 1a is the micrograph of the n-type higher temperature deposition that displays only faint evidence of the scratches beneath, with a roughness of 6.7 nm and the bumpy looking surface indicative of polycrystalline deposition.

To appreciate the deposition temperature contrast at a sub-micron resolution, HIM was employed[20]. Fig. 2a and 2b show the surface features of the n-type layers at 500 nm and 1 μm fields of view respectively. Again, the contrast between the surface roughnesses is visible, though at this magnification the difference in individual crystal size also becomes apparent. The amorphous layer of Figure 2a shows some order with approximately 20 nm 'dimples' occurring on the surface, suggesting very small poly-crystals. Much clearer are the larger poly-crystals of the higher temperature deposition, with crystal grains appearing on the surface up to 200 nm in size.

Finally a comparison of dopant type has lead to an interesting physical attribute encountered in these layers.

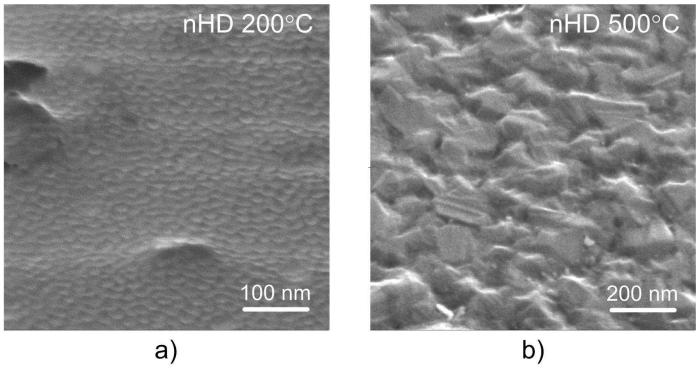

FIG. 2. a) and b) are respectively helium ion microscope (HIM) images of the low- and high temperature depositions, both being n-type and 300 nm thick.

Figure 1d shows the boron doped, p-type layer. Visual inspection alone identifies that the poly-crystal size in this layer is larger than in the antimony doped, n-type layer of Figure 1a. The polycrystals of the p-type layer are approximately 500 nm in size, with the surface roughness of this layer up at 30 nm, all of which suggest a greater crystallinity in these layers. To confirm this layers of both dopants grown at both high- and low-deposition temperatures were analysed via X-ray diffraction (XRD) to verify their crystallinity.

The results of the XRD analysis analysis may be seen in Figure 3. SiC is evident in all the samples, however, the cubic Ge content is sample specific. All the Ge layers deposited at high temperature have evidence of polycrystallinity, with five different cubic Ge crystal orientations appearing. The low temperature depositions show little evidence of crystallinity, the n-type layers having no crystalline peaks at all, the p-type layers having some smaller peaks notably in the (220) and (311) orientations, though much reduced compared to the higher temperature depositions.

What is evident from Figure 3, is that the p-type layers have X-ray intensities greater than the n-type layers, supporting the notion of greater crystallinity. We predict that the reason for this is due to the relative size of the dopant atoms, with boron, the p-type dopant, being much lighter and smaller than Ge, making the incorporation of the Boron into the lattice easy, with minimal stress being added to the layers. Antimony, on the other hand, is much bigger and heavier than Ge, adding stress to the Ge polycrystals. This causes a greater concentration of dislocations to propagate as it is growing, limiting the size of the crystals that can grow.

We can summarise this section by returning to the physical qualities of our ideal layer, which should be crystalline and atomically flat. With this in mind we can immediately rule out the 100 nm layer as this is too rough to polish, and no good contact could be made. As we will see evidence of in the next Section, the low tem-

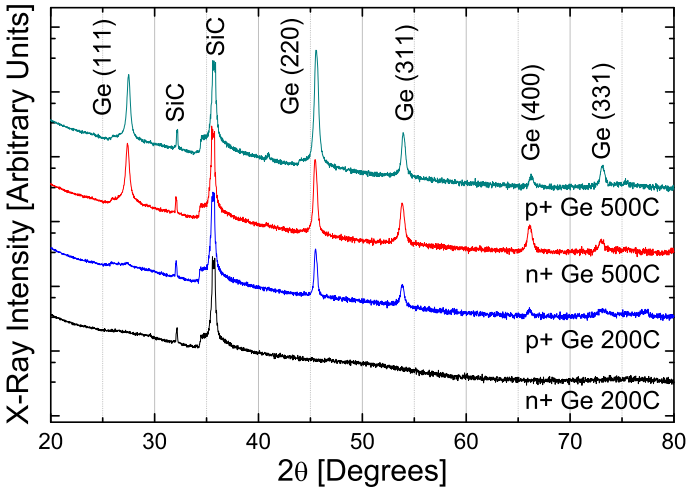

FIG. 3. XRD $\theta - 2\theta$ scans of the MBE Ge layers deposited on 4H-SiC.

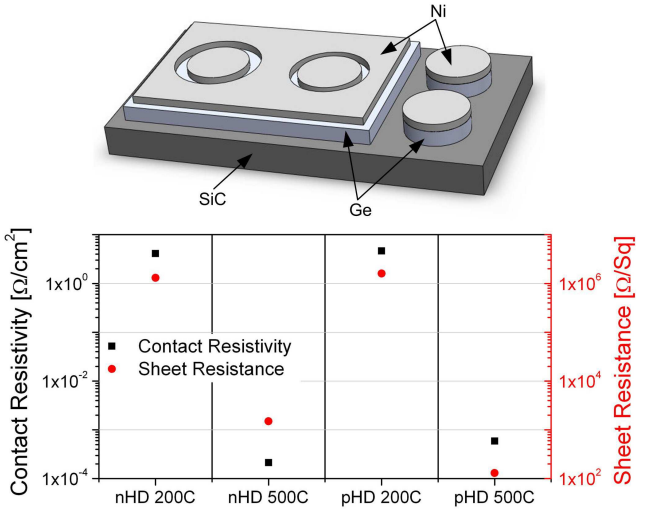

FIG. 4. Top: The layout of the Ni/Ge/SiC mesa diodes and CTLM Structures. Bottom: The contact resistivity and sheet resistances of the four Ni/Ge layers as extracted using CTLM structures.

perature layers, though very flat, suffer greatly due to the substantial quantity of grain boundaries an electron must cross. Hence we are left with the p-type and n-type layers, neither of which are atomically flat, though something approaching this could be achieved by growing the layer too thick and having it polished back to the desired thickness. In this case, the bigger the polycrystals, the better, and this is achieved by using the lightest dopants, which in n-type might be nitrogen or phosphorous. The absolute choice of p-type or n-type should make no difference to the physical properties of the layer.

B. Electrical Analysis

The heterojunction layers were made into mesa Schottky diodes by forming ohmic contacts on the SiC and Ge out of Ni. In this section the many rectifying properties of the heterojunction interfaces will be investigated with I-V analysis, extracting parameters including ideality factors, Schottky barrier heights and breakdown voltage. I-V analysis at varying temperature proves the inhomogeneous nature of the heterojunction and C-V analysis is used to verify the presence of surface states at the interface. First, however, the CTLM structures were used to verify the ohmicity of the front and back contacts.

CTLM Analysis

Verifying the ohmicity of the metal-semiconductor interfaces can confirm that all the rectifying action within the devices happen at the Ge/SiC interface. The CTLM technique measures the resistances associated with current passing from one metal contact into a semiconductor and back into another contact. The contact resistivity (ρ_c) of the M-S interfaces is used here primarily as an indicator of ohmicity, because if this was a rectifying interface, this value would be exceedingly large due to the reverse bias of one of the two Schottky M-S contacts. The sheet resistance (R_{sh}) of the semiconductor layer between the M-S contacts is also extracted via the CTLM technique. Both values are extracted from I-V measurements taken from each of the CTLM structures. The details for extracting these figures have previously been explained[13,21,22].

The Ni-SiC back contacts are ohmic with a contact resistivity of the order of $1\times10^{-3}\ \Omega cm^2$. The contact and sheet resistance of all the Ni-Ge front contacts considered here are displayed in Table I and shown graphically in Fig. 4. The results divide along crystallinity lines with the polycrystalline layers forming the interfaces with the lowest resistance. The sheet resistance of the p-type layer is over 25 times less than that of the n-type layer. We suggest that this is due to the greater incorporation of the dopant within the lattice and the greater crystal size, which facilitates less grain boundaries.

The front and back contact resistivities presented here are reasonably high, contributing to the $R_{on,sp}$. The large values are due to the relatively low temperature anneal carried out. A higher temperature anneal[23] (900-1000^{o}C) could reduce the contact resistivity of the Ni/SiC interface to a value as low as $1\times10^{-6}\ \Omega cm^2$. However, a higher temperature anneal would affect the physical characteristics of the Ge layers, reducing the effects of the MBE deposition temperature, which we are here trying to observe.

Proving that the Ni/Ge and Ni/SiC contacts are ohmic facilitates the presumption that all the rectifying action takes place at Ge/SiC boundary. The heterojunction

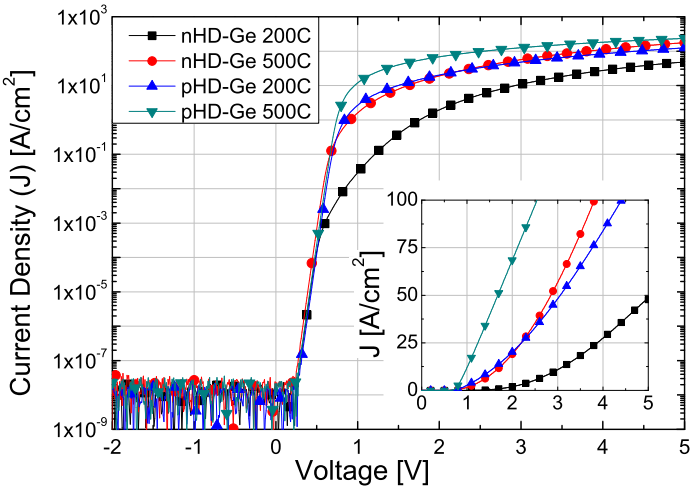

FIG. 5. The logarithmic and linear (inset) current-voltage curves taken at 25^{o}C.

diodes being unipolar (as we will see from I-V analysis), this means that the conduction band offset at the interface between the Ge and SiC determines the rectifying properties of the devices. This is referred to throughout this paper as the SBH, a term usually used to describe the barrier at a M-S interface. This is because the degeneracy of the Ge allows us to presume that it acts like a metal, with minimal band bending.

I-V Analysis

Typical current-voltage (I-V) results, taken from the Ge/SiC heterojunction diodes at 25^{o}C, are shown in Fig. 5. From this data the ideality factors and Schottky barrier heights have been extracted using the techniques described elsewhere[21], and summarised in Table I. All the heterojunction diodes approach perfect ideality factors (n), 1.1 being the highest value, with both the polycrystalline diodes having values under 1.05. The barrier heights (Φ_B) were all between 1.05 and 1.15 eV, whilst in separate tests, the breakdown voltage (V_B) of the polycrystalline diodes were over 300 V, with this expected to vastly improve with the addition of passivation and proper junction termination. The specific on-resistance ($R_{on,sp}$) of the polycrystalline diodes, found using Cheung's method[24], was below 20 $m\Omega - cm^2$, whilst the amorphous n-type layer was up at 67 $m\Omega - cm^2$. With the resistivity of the thick SiC bulk (8 $m\Omega - cm^2$) and the back contact a constant value for all the samples here, it is the contributions from the Ge bulk and the Ni/Ge and Ge/SiC interfaces that separate the specific on-resistance values. The differing values of ρ_c and R_{sh} found previously are indicative of the differing contributions from the amorphous and polycrystalline Ge layers.

Fig. 5, displays the strongest argument for opting for the polycrystalline layers formed from the higher deposition temperature of 500^{o}C. The amorphous layers have a much larger specific on-resistance due to the large number of grain boundaries that slow the progress of an electron through the material. A better solution for overcoming the surface roughness seems to lie in post deposition polishing, such as has been carried out on SiC surfaces[25].

In comparing the dopant types, what is most interesting about the differing dopant types is the lack of differences between the two. They both turn on at the same time, in a distinctly unipolar, Schottky manor. The unipolar action in the p-type devices can be attributed to a high barrier to holes, similar to that reported in Si/SiC heterojunction devices[6,8]. Other factors that could affect the bipolar action include interface/bulk traps, which act as recombination centres, or the poor activation/incorporation of the dopants within the Ge polycrystals. Assuming a barrier to electrons of 1.1 eV, a Ge bandgap of 0.66 eV and a SiC bandgap of 3.26 eV, the hole barrier should be approximately 1.5 eV. The fact that all the devices turn on at the same time can be attributed to the very similar SBHs of all the devices. However, given the opposite extremes of doping, one might expect differing SBHs due to the band bending required to align the Fermi levels. The fact that this doesn't happen may suggest that Fermi level pinning is occurring, something we shall investigate in the C-V analysis and the final section.

Further to the basic I-V measurements at room temperature, I-V tests were conducted at varying temperature (IVT) ranging from -50^oC to 175^{o}C. The purpose of these tests was to assess the homogeneity of the heterojunction interface, and extract accurate SBH values, free from the errors that inhomogeneities often introduce into the traditional Richardson plots. The original theory in this field[15–17] introduced the idea that a two dimensional variation of the SBH exists at a M-S interface and that this affects the extraction of the Richardson constant and the SBH. Further work[26] modelled the current as it passed over the interface and found that the IVT curves could be simulated using a lower effective SBH value and an area 1-2% that of the actual area. This suggests that at an inhomogeneous layer, the current will pass predominantly over those barriers at the low end of the lateral SBH distribution in order to seek the path of least resistance. This explains the difference between C-V and I-V analysis of the SBH, where the first technique averages all the SBH values and the second measures the actual flow of the current over the lower barriers. It also explains why the Richardson plot is inaccurate, as they use the traditional device area rather than this smaller effective area. We have elsewhere[13], expanded further on this work, relating it to the heterojunction interface, using a model to fit the thermionic emission equation to the IVT data using effective SBHs and areas.

Using this method, we have proven that all the Ge/SiC interfaces are inhomogeneous, with the effective SBH (Φ_{eff}) and effective area (A_{eff}) values summarised in Table I. The current through the polycrystalline Ge lay-

TABLE I. Properties of the Ge/SiC heterojunction diodes. The diode names refer to the doping type (n or p) and the deposition temperature (200 °C or 500 °C).

Diode	***n*200**	***n*500**	***p*200**	***p*500**
R_q (nm)	2.1	6.7	3.5	30
ρ_c $(\Omega - cm^2)$	2.8	4.93e-4	5.8	1.37e-3
R_{sh} $(\Omega/\square)$	2.1M	1262	1.8M	48.8
n	1.103	1.039	1.071	1.047
Φ_B (eV)	1.085	1.094	1.119	1.127
$R_{on,sp}$ $(m\Omega - cm^2)$	66.9	11.6	19.2	18.5
V_B (V)	200	300	250	300
Φ_{eff} (eV)	-	1.033	1.012	1.028
A_{eff}	-	3%	1.5%	3%

ers were both modelled using a SBH of around 1.03 eV over an effective area 3% that of the actual size.

C-V Analysis

The degeneracy of the Ge layer allows many parallels to be drawn between the extensive research carried out on M-S junctions[27] and these heterojunction diodes. Similar to a M-S interface, the space charge region can be presumed to be entirely on the lower-doped SiC side due to the huge doping differential. This allows us to apply to this work the theory of C-V analysis, another method used to verify the SBH, whilst it is also used to verify the bulk doping level, in this case that of the SiC.

The original theory of the technique[21,28] states that, for an abrupt junction, a linear relationship will exist between an applied voltage (V_A) and the inverse square of the capacitance $\left(C^{-2}\right)$, such that,

$$\frac{dC^{-2}}{d\left(V_{bi} - V_A - \beta\right)} = \frac{2}{K_S \varepsilon_0 A^2 N_D}, \qquad (1)$$

where V_{bi} is the built-in potential, β the thermal voltage, K_S the dielectric constant, ε_0 the permittivity of free space, A the area of the device and N_D the doping of the SiC epitaxial layer. Thus, a $C^{-2} - V$ plot could be used to extract N_D and V_{bi} by analysing the gradient and the x-intercept. Fig. 6 shows the $C^{-2} - V$ plot as taken for the polycrystalline n-type layer, and this is typical of all the layers reported here. A linear fit to this data has been plotted to satisfy Eq. 1, resulting in an estimated V_{bi} of over 2 eV. This appears to be grossly over estimated when compared to the V_{bi} of 0.855 eV, which is what the SBH extracted from I-V analysis equates to.

The reason for the failure of this method is down to the presence of interface traps at the heterojunction interface, as originally discussed for M-S interfaces[27,29], but also fairly applied here. Eq. 1 is derived from a situation where all the charge contributing to the capacitance at an interface comes from the space charge region (Q_{SC}) alone. Interface charges (Q_{GS}) at the surface were not included in this model, leading to a situation where Eq. 1 only holds true under homogeneous and intrinsic conditions.

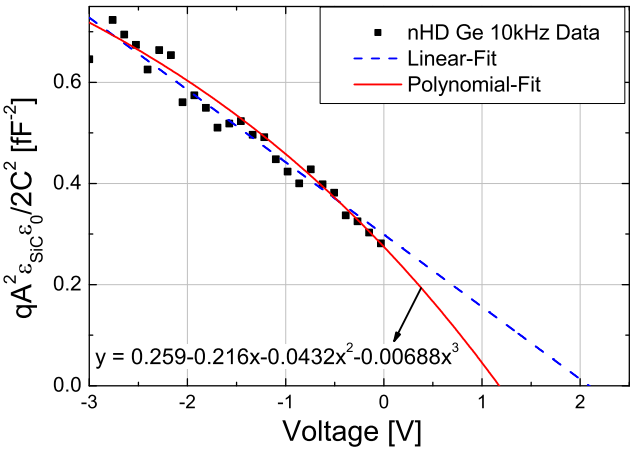

FIG. 6. A $1/C^2 - V$ plot for a polycrystalline n-type layer, with linear and quadratic fits to the experimental data.

The accuracy of the linear fit to the experimental data can be brought into question by visual inspection alone. However, using the residual sum of squares (RSS) as an indicator of the best fit, a third order polynomial was found to produce the tightest fit to the data, which can also be seen in Fig. 6. The V_{bi} extracted from this method is much closer to the SBH provided by the I-V analysis, however, V_{bi} is largely dependent on the frequency of the C-V measurement varying from 0.978 eV at 1 kHz to 1.175 eV at 100 kHz. The doping can only be estimated with tangents to this curve, a situation that produces doping levels ranging from 3.2×10^{15} cm^{-2}, closest to x-axis, to 1.0×10^{16} cm^{-2} nearest the y-axis. The doping of the SiC epitaxial layer was stated by the manufacturer as being 1.4×10^{15} cm^{-2}, and this was confirmed using majority carrier density profiles[21].

Models attempting to include interface charges, Q_{GS}, into metal-semiconductor C-V analysis are non-trivial. They can have unique solutions depending on whether or not the metal and/or the semiconductor contribute charge to the interface, and whether or not the charge on either side of the interface can follow the AC signal, and any combination of the above[29]. This is further complicated by the knowledge that these models presume that some interfacial layer has formed between the metal and the semiconductor due to processing defects. The validity of such a model has been brought in to question[27], due to the reliance of this model on the original Schottky-Mott equation when the materials come in direct contact.

Suffice to say, it is summed up well[27] by saying that the capacitance method cannot be used to deduce the SBH in the presence of interface states. However, the C-V analysis is very useful as it proves that interface states are prominent at the heterojunction interface.

C. Fermi Level Pinning

Fermi level pinning is another subject that has attracted much research in the determination of M-S SBH behaviour[27,30–32], and we suggest that the same techniques may be applied to the degenerate Ge/SiC interface. Pinning is attributed to a large density of surface traps present in the materials and the non-linear nature of the C-V data has suggested that they are present in the heterojunction devices. A method that quantifies the density of traps at a M-S Schottky barrier interface[33] uses C-V analysis at varying frequency. However, this model relies on the presumption that the materials are separated by a thin interfacial layer, with little provision for its absence, as in the fixed separation model criticised elsewhere[27]. Regardless of the validity of this method, we will here equate the measured band offsets of our heterojunction layers with the density of surface states without including an interfacial layer.

Evidence of Fermi level pinning originated in the I-V analysis of the heterojunction diodes. The turn on voltages and the extracted SBH values of all the heterojunction interfaces were very similar regardless of doping type suggesting that the influence of the dopants was minimal on the formation of the barriers. Another peculiarity is the absolute size of the SBH. All the heterojunctions had a SBH of approximately 1.1 eV. This value is clearly too large to support a theory based on the classic Schottky-Mott principal[34,35], which states that the vacuum levels will align, leaving the electron affinities to dictate the offset. With n-type doping in both semiconductors, and nearly equal electron affinities, the Ge-SiC offset would be closer to 0.2-0.3 eV under this principal. Hence, we will investigate the idea that the Fermi level has been pinned at the surface of the SiC.

The surface of a semiconductor can be seen as an abrupt end to a uniform crystal lattice structure, giving way to the atmosphere or another material, be it insulating or conducting. As such, electronic states unique to the semiconductor surface exist, which have no equivalent within the bulk. These surface states exist in the bandgap of the semiconductor and here they will be treated as uniform across the entire bandgap surface. It is these surface states that pin the Fermi level in maintaining charge neutrality.

Charge neutrality occurs when the conduction band is devoid of charge and the valence band filled. Any state (be it interfacial, surface or defect) that exists within the bandgap will add to the overall charge by being there.[30] By occupying a state in the bandgap close to the valence band, a very small negative charge is added. If it is not filled it contributes a large positive charge. The opposite is true near the conduction band. The charge neutrality level (E_{CNL}), an intrinsic property of the semiconductor in question, indicates the point at which the influence on that charge from valence and conduction bands is equal, where occupation of the state would contribute the same negative charge as positive charge from it being empty.

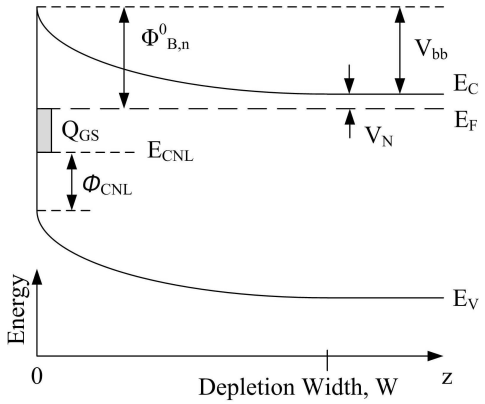

FIG. 7. The band diagram of a semiconductor experiencing Fermi level pinning due to the existence of surface states.

At 0 K, the Fermi level will indicate the point within the bandgap where filled surface states give way to empty ones. If this does not coincide with E_{CNL} then a net charge will exist at the semiconductor surface. If the Fermi level is closer to the conduction band than E_{CNL} then there will be an excess of electrons and a negative net charge; this is the case in Fig. 7. If the Fermi level is closer to the valence band then a net positive charge will exist. This net charge (Q_{GS}) can be defined as,

$$Q_{GS} = qD_{GS}\left(\Phi^0_{B,n} + \phi_{CNL} - E_G\right) \tag{2}$$

where q is the electronic charge, D_{GS} is the density of surface states, $\Phi^0_{B,n}$ is the energy difference between the Fermi and conduction bands at the surface, E_G is the bandgap energy and ϕ_{CNL} is the energy difference between the valence band and E_{CNL}. ϕ_{CNL} (also known as the branch point energy) of SiC and Ge are reported[31,32] as 1.44 and -0.28 respectively. At the surface, the Fermi level will align with E_{CNL}, if there is no charge from within the space-charge region (Q_{SC}) that requires neutralising, i.e. under homogeneous and intrinsic circumstances[27]. The charge in the space-charge region is given as

$$Q_{SC} = \sqrt{2\varepsilon_s N_D q\left(\Phi^0_{B,n} - V_N\right)} \tag{3}$$

where ε_s is the permittivity of the semiconductor and V_N is the energy difference between the Fermi and conduction bands within the bulk. In practically all real semiconductors, $Q_{SC} \neq 0$ and there will necessarily be some deviation of the Fermi level from the CNL at the surface to maintain the charge neutrality between Q_{SC} and Q_{GS}. This interdependency leads to the combination of Eq. 2 and 3,

$$qD_{GS}\left(\Phi^0_{B,n} + \phi_{CNL} - E_G\right) + \sqrt{2\varepsilon_s N_D q\left(\Phi^0_{B,n} - V_N\right)} = 0. \tag{4}$$

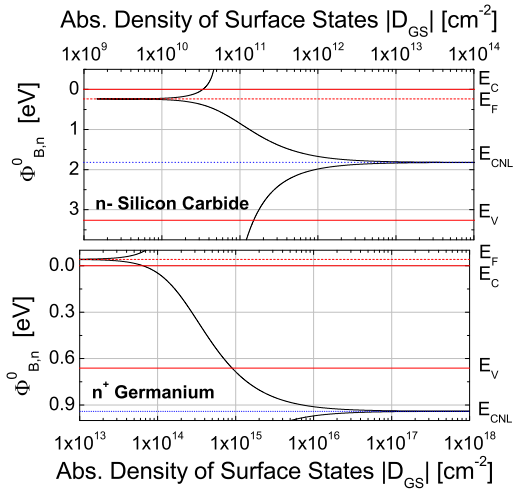

FIG. 8. The energy difference between the Fermi and Conduction levels at the semiconductor surface ($\Phi^0_{B,n}$) plotted against the density of surface states (D_{GS}) in the SiC and Ge of a n-type Schottky diode.

A rearrangement of Eq. 4 allows a plot of D_{GS} against $\Phi^0_{B,n}$ as seen in Fig. 8 for a n-type heterojunction diode. The Fermi levels of both semiconductors can be seen to be pinned at $\Phi^0_{B,n} = E_{CNL}$, when D_{GS} is large. As D_{GS} tends to 0, the Fermi levels return to the their bulk positions. The doping of the Ge is so great that the quantity of surface states required to move the Fermi level from its bulk position are greater than the amount required to completely pin the SiC Fermi level at E_{CNL}. We therefore presume that the Ge remains unpinned at its bulk position, helping to justify the assumption that the degenerate Ge acts as a metal in these devices.

An unclear picture of the exact SBH makes the precise determination of D_{GS} and $\Phi^0_{B,n}$ impossible. Previous work[13], indicated that due to the inhomogeneous nature of the interface, a two-dimensional array of varying SBH will exist, and hence the SBH value extracted depends on the measurement techniques and the analysis applied to it. Taking the effective SBH of the two polycrystalline diodes, 1.03 eV, and assuming that the Ge acts as a metal, then $\Phi^0_{B,n}$ will be equal to the SBH minus $V_{N,Ge}$, thus $\Phi^0_{B,n} = 0.991\ eV$. Reading from Fig. 8, this equates to a surface state density of $D_{GS,SiC} = 1.3 \times 10^{11}\ cm^{-2}$.

Fig. 8 and the above calculations equate D_{GS} and $\Phi^0_{B,n}$, without involving any interfacial layer, separating the semiconductors. However, the absolute values attained must be treated only as estimates due to the assumptions made. The value of $\phi_{CNL} = 1.44\ eV$ for the bulk material of SiC is essential to determining where the Fermi level is pinned. The source of this figure[31,32] seems somewhat hazy, with the specific SiC polytype on which this is based not mentioned. Another limiting factor is not knowing the exact SBH value, a problem that could be overcome through Ballistic Electron Emission Microscopy (BEEM), as has been done with other Schottky barrier diodes[36].

IV. CONCLUSIONS

$n-n$ and $p-n$ Ge/SiC heterojunction mesa diodes have been fabricated and characterised. Physical analysis of the layers showed a marked improvement in the surface quality after the Ge islands merge. Amorphous layers made by low temperature deposition provide flat surfaces, though this is at the expense of the forward resistance which is very high. Higher temperature deposition results in a poly-crystalline layer with a lower on-resistance.

The differences in doping type were surprisingly few, most likely due to the Fermi pinning phenomena. The key difference lay in the crystal size formed at both low and high temperature depositions. In both cases, the AFM analysis proved that the p-type layers were rougher, with bigger individual grain sizes. This translated to a lower sheet resistance. This is attributed to the greater ease at which the lighter, smaller Boron impurities can be incorporated into the Ge lattice during deposition.

After front and back metallisation with Ni, the layers were electrically tested, proving that the heterojunction diodes behaved like conventional metal-semiconductor Schottky diodes. Good ideality factors, specific forward resistance, reverse leakage and breakdown properties, were witnessed aside problems usually faced at a metal-semiconductor interface rather than a heterojunction. Current-voltage measurements at varying temperature proved that all the layers had two-dimensional fluctuations in the SBH due to inhomogeneities at the heterojunction interface. C-V analysis and the SBH size extracted from I-V analysis suggested strongly that interface states were present at the surface causing Fermi-level pinning throughout the bands. A simple model was employed to quantify the concentration of interface states at the surface.

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