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Simulations of a lateral PiN diode on Si/SiC substrate for high temperature applications

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Abstract. Simulations are presented of a lateral PiN power diode on a Si/SiC substrate for harsh environment, high temperature applications. Thermal simulations compare the Si/SiC solution to SOI, Si/SiO_2/SiC, bulk Si and SiC, showing that the Si/SiC architecture, with its thin Si film intimately formed on SiC, displays significant thermal advantages over any other Si solution, and is comparable to bulk SiC. Detailed electrical simulations show that in comparison to the same device in SOI, a Si/SiC PiN diode offers no deterioration of the on-state performance, improved self-heating effects at increased current and can potentially support higher breakdown voltages.

Introduction

It is necessary for power, CMOS, photonics and sensors to operate reliably and predictably in high temperature, hostile environments such as those found in downhole, space, automotive and aerospace applications. The dominant materials technology in the harsh environment field is silicon-on-insulator (SOI), which has enabled silicon device operation beyond 300°C by confining the active device within a thin silicon layer, minimising device leakage [1]. However, the buried oxide (BOX) insulating layer also causes self-heating, which can impact device performance, cause thermal runaway and shorten device lifetime. A high thermal conductivity and low intrinsic carrier concentration make silicon carbide an ideal candidate for high temperature power devices [1,2], while CMOS implemented entirely within 4H silicon carbide (SiC) has been tested up to 400°C [3]. However, at voltage ratings below 600 V, the material's wide bandgap inevitably introduces a high turn-on voltage, and its low channel mobility induces high on-state resistance when compared to Si.

The combination of a silicon thin film with a SiC substrate could potentially combine the benefits of both SOI and SiC CMOS platforms. The combination of these materials via wafer bonding has been considered with a BOX to make Si/SiO_2/SiC [4, 5], and without one, thus forming an intimate Si/SiC platform [6-10]. By implementing a direct Si/SiC interface, the SiC serves as a thermal path to dissipate heat direct from the active area of the Si. Moreover, the use of semi-insulating SiC minimises potential leakage currents that could occur due to the low heterojunction band offsets between the materials. Therefore, the Si/SiC heterostructure behaves like SOI with better thermal conductivity, thereby minimising self-heating effects.

In this paper, we present simulations of a lateral PiN diode on a Si/SiC substrate using SILVACO. Planar PiN diodes on SOI, Si/SiO_2/SiC and bulk Si and SiC are modelled for comparison.

Simulation Setup

The simulation consists of two parts. The first simplifies a PiN diode down to a 100x100x1 μm^3 heat source on a 300x300x100 μm^3 domain representing the substrates of interest. Thermal modeling

is performed on these structures, where thermal conductivities of materials are adjusted to be power functions of temperature and assigned to corresponding regions. The model is solved by the heat transport equation independent of time and neglects the effects of thermal radiation and hot carriers. Therefore, the results represent the lattice temperatures in a steady state.

The second simulation considers the detailed layout of a lateral PiN diode in SOI and Si/SiC architectures. The peak doping of 1.5×10^{19} cm^{-3} was set for both ohmic regions, which decreased laterally and vertically according to Gaussian functions. As a result, the junction area is about 10x0.5 μm^2 with curvature profile. The drift region has a uniformly p-type doping density of 3×10^{15} cm^{-3} and its dimensions (length and thickness) were altered to suit different simulations. No parameter (e.g. fixed charges and traps) was configured along the Si/SiC and Si/Oxide interface for fair comparison.

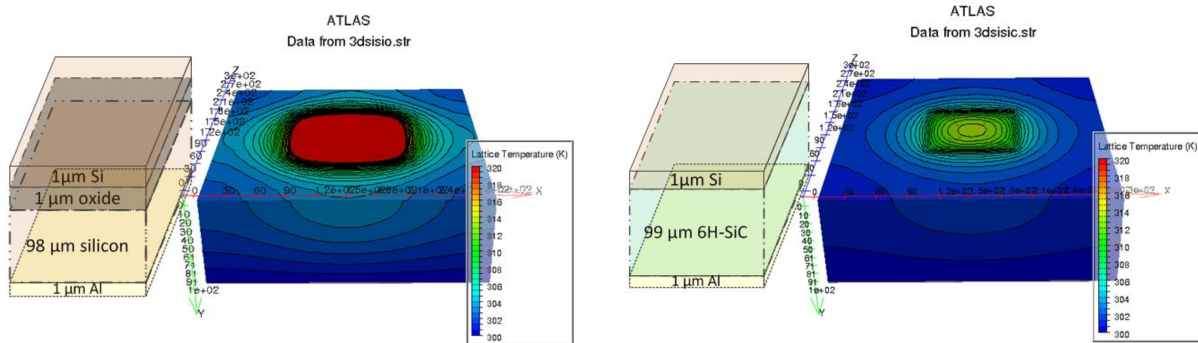

Fig. 1. The SOI (left) and Si/SiC (right) simulation models showing temperature distributions with a range of 300-320K. Their maximum temperatures are 403K (left) and 314K (right) repectively.

Results and discussion

Thermal simulations of the substrates. Figure 1 shows the temperature gradients of the substrates in which each PiN diode is dissipating 1W of power and the temperature of the Al back contact is 300 K. The temperature in the SOI structure reaches a maximum of 403 K, whereas the Si/SiC reaches just 314 K. This difference is explained by the presence of the BOX layer that acts as a thermal barrier impeding heat transfer. This causes self-heating in the Si as insufficient heat is passed vertically, increasing the temperature of the Si film. This effect is exacerbated by the temperature dependence of thermal conductivity, which drops as the temperature rises, worsening the situation. The bulk Si beneath the oxide has little influence on thermal performance.

In the Si/SiC simulation, the 6H-SiC works as a heat sink and directs most of the heat down to the Al layer. It reduces not only the device temperature but also the lateral spread of heat that will affect neighbouring components (see Fig.1). Therefore, the Si/SiC is beneficial to the development of dense and reliable high temperature circuitry.

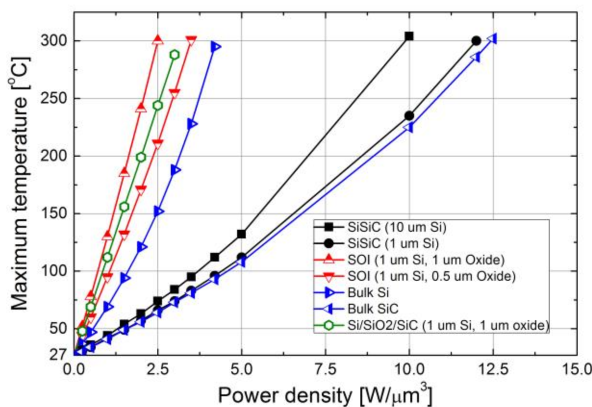

Fig. 2: Simulated max temperatures (27-300°C) vs. power density for different structures

Figure 2 displays the relationship between the power density and the maximum temperature for all the different substrates considered. Bulk SiC is shown to be the best solution for dissipating the heat, with the Si/SiC substrate close behind. These are able to dissipate around 4 times the power density than the SOI device can at 250°C. However, other temperature-related attributes (e.g. reverse currents and breakdown voltages), also limits the system operations and should be considered and estimated.

On-State Behaviour. For the electrical simulations, a PiN diode with a 30 µm drift region

was defined within a 1 μm thick Si layer, implemented either directly on bulk SiC or as SOI, on a 1 μm thick oxide on bulk silicon. Positive voltage was applied at the anode while the cathode and substrate were held at zero bias. All three electrodes were defined as thermal contacts to consider horizontal and vertical heat dissipation. Both isothermal and non-isothermal simulations were performed. The isothermal model considers the device at a fixed temperature (300 K) and is used herein for validation of the comparative electrical characterstics. Within the non-isothermal simulation self-heating is reintroduced, as temperature is iteratively updated due to the power dissipated, effecting the properties of the semiconductor including thermal conductivity.

Figures 3 shows the on-state I-V curves of these two diodes and their device temperatures. The isothermal model shows that if temperature effects are ignored, there is little difference between the two diodes, both being limited by similar drift region resistance. However, this relationship only holds true within a small region of the non-isothermal simulations. Self-heating effects are observed in both diodes, but the Si/SiC one suffers less performance penalty. Its linear region is longer and the heat transfer ability is much better. Specifically, at 3 V, the increased current in the Si/SiC device means more power is being dissipated than in the SOI device. However, its temperature is approximately 75 ^{o}C, about two times lower than its counterpart.

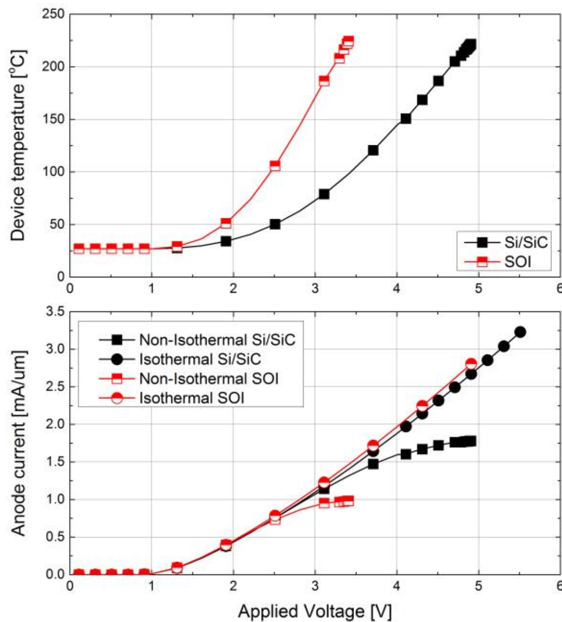

Fig. 3: Applied Voltage vs. Device temperature (top) and Anode current (bottom) for the Si/SiC and the SOI

Off-State Behaviours. In this simulation, a negative voltage was applied to the anode of the PiN diode structures previously defined to compare leakage currents and breakdown voltage. Furthermore, the geometry of the top Si and the oxide film were varied and the effect on breakdown voltage analysed.

Figure 4 demonstrates the I-V curves of the PiN diodes under reverse bias in the Si/SiC and SOI structures, both having a Si layer 1 μm thick. It can be seen that the Si/SiC can support -175 V whereas its counterpart breaks down at -87 V. The leakage current in SOI is much higher even with a better insulating layer. This can be explained by using an additional SOI structure, with its oxide thickness increased to 298 μm. This extension makes the curve much softer and similar to the Si/SiC response, while the leakage current becomes smaller than that of the Si/SiC substrate. This indicates that in thin-film SOI, the potential is supported by the oxide layer and the vertical breakdown is dominant. By increasing the thickness of the oxide, the crowding effect of the electrical field near the anode is relaxed and its distribution in the structure is changed. As a result, it leads to the variation of the recombination current which is the major part of the reverse current.

Figure 5 displays the relationship between the drift region length and the breakdown voltage for both structures with different thickness of the top Si layer. Each curve has a linear section where the breakdown voltage rises with longer drift region. After that, the breakdown voltage is not highly related to the length and is determined by the thickness of silicon. More importantly, the Si/SiC PiN diode supports more voltage with a thinner silicon layer, while the opposite is true in SOI. As such thinner Si films used in Si/SiC will be most favourable for high temperature operation as they support higher breakdown voltages and have less self-heating effects, improving on-state performance. Conversely, the approach for increasing breakdown voltage in SOI is to thicken the top Si and buried

oxide layer. However, this will worsen self-heating effects due to increased heat generation and thermal resistance.

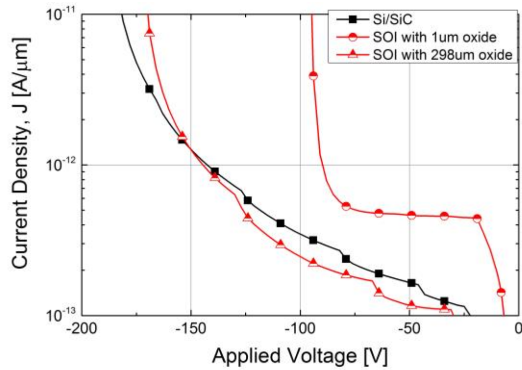

Fig. 4 Reverse I-V curves for Si/SiC and SOI structures

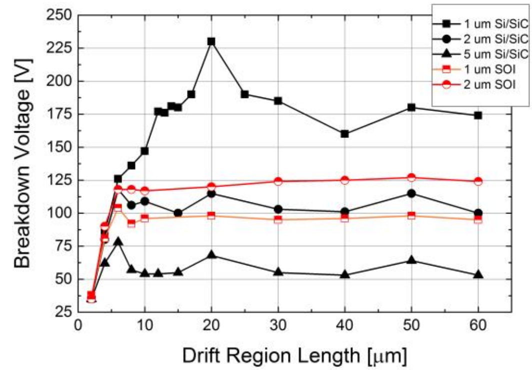

Fig.5 Intrinsic region length vs. Breakdown volatge

Conclusions

Thermal modelling is performed on Si/SiC, SOI, Si/SiC, Si/SiO2/SiC, bulk Si and SiC structures. The results show that the thermal performance of a Si/SiC architecture, with a thin Si film, is comparable to bulk SiC. Additionally, the lateral spread of heat is reduced in this solution compared with SOI, making it more suitable for dense and reliable high temperature circuitry.

Forward and reverse bias simulations are carried out on a lateral PiN diode implemented in SOI and Si/SiC substrates. Self-heating effects are reduced in the Si/SiC substrate and its forward performance is more robust than the counterpart. The breakdown voltage is found to be higher in the proposed Si/SiC structure. For both architectures, the relationship between breakdown voltage and the length of the drift region, the thickness of the top Si and the oxide layer is demonstrated. The outcome indicates that thin-film Si/SiC structure can be used for achieving high temperature, high voltage devices with minimal self-heating.

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