Improved Electrothermal Ruggedness in SiC MOSFETs Compared With Silicon IGBTs

Petros Alexakis, Olayiwola Alatise, Ji Hu, Saeed Jahdi, Li Ran, and Philip A. Mawby

***Abstract*— A 1.2-kV/24-A SiC-MOSFET and a 1.2-kV/30-A Si-IGBT have been electrothermally stressed in unclamped inductive switching conditions at different ambient temperatures ranging from −25 °C to 125 °C. The devices have been stressed with avalanche currents at their rated currents and 40% higher. The activation of the parasitic bipolar junction transistor (BJT) during avalanche mode conduction results from the increased body resistance causing a voltage drop between the source and body, greater than the emitter–base voltage of the parasitic BJT. Because the BJT current and temperature relate through a positive feedback mechanism, thermal runaway results in the destruction of the device. It is shown that the avalanche power sustained before the destruction of the device increases as the ambient temperature decreases. SiC MOSFETs are shown to be able to withstand avalanche currents equal to the rated forward current at 25 °C, whereas IGBTs cannot sustain the same electrothermal stress. SiC MOSFETs are also shown to be capable of withstanding avalanche currents 40% above the rated forward current though only at reduced temperatures. An electrothermal model has been developed to explain the temperature dependency of the BJT latchup, and the results are supported by finite-element models.**

***Index Terms*— Ruggedness, SiC MOSFETs, unclamped inductive switching (UIS).**

I. Introduction

ELECTROTHERMAL ruggedness is an important reliability metric that quantifies the ability of the power semiconductor device to withstand electrothermal stresses. This electrothermal stress can result from the conduction under avalanche mode, where there is simultaneously high current flowing through the device and a high voltage across it. Some circuits purposely use MOSFETs in unclamped inductive switching (UIS) mode, but these are mainly automotive applications where the devices drive inductive loads without antiparallel free-wheeling diodes to commutate the current when the device is switched OFF [1]–[4]. Avalanche mode conduction can also be triggered by high *dV/dt* transients that coupled with parasitic capacitances can cause a body current to flow, thereby forward biasing the emitter–base junction of the parasitic bipolar junction transistor (BJT) [5].

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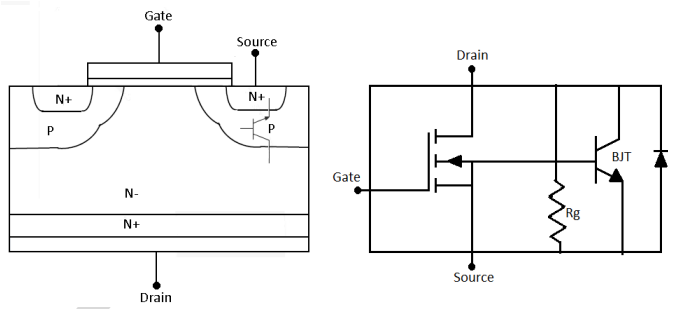


Fig. 1. MOSFET schematic diagram and equivalent circuit showing the antiparallel diode and n-p-n transistor.

The body current is usually generated by the charging of a depletion capacitance during voltage switching. MOSFETs can also suffer severe electrothermal stresses in forward mode conduction if biased in the linear mode (high-current and high-voltage conditions) [6]. It should be noted that linear mode bias refers to the saturation mode bias in MOSFETs ($V_{DS} > V_{GS} - V_{TH}$); however, because the condition was first considered for BJTs, the term linear mode (which for a MOSFET is the ohmic or triode region) has repeatedly been used for MOSFETs as well. Linear mode conduction can also occur during switching transients when the bias point of the device moves across the load line. However, since the electrical switching time constant is much smaller than the thermal time constant, it is less of a problem for reliable switch mode power MOSFETs.

All power MOSFETs, by virtue of their physical design, have antiparallel diodes as well as parasitic n-p-n BJTs. Ideally, the p-body of the MOSFET should be shorted to the source either by a high p-body implant dose away from the MOSFET channel (so as not to increase the threshold voltage excessively) [7] or by a moat structure with metal deposition shorting the n-source to the p-body. The purpose of shorting the body to the source is to ensure that there is no forward voltage drop between the body and the source. In reality, there is always some resistance between the source and the body, and this resistance will increase with temperature. Fig. 1 shows the schematic diagram of a vertical DMOSFET and the corresponding circuit model, showing the additional antiparallel diode and n-p-n parasitic BJT [8].

When current is flowing from the drain to the source through the channel, sufficient stray current flowing through the source-to-body resistance can cause the voltage drop across the source–body junction to forward bias the

emitter–base junction of the parasitic BJT. The likelihood of this increases with temperature because of the positive temperature coefficient of the body resistance and the negative temperature coefficient of the in-built voltage across the source–body junction of the MOSFET (emitter–base junction of the parasitic BJT) [9]. Because BJT collector currents have a positive temperature coefficient, they are inherently unstable at high temperatures as a result of thermal runaway, i.e., a positive feedback process between current and temperature. In reality, power MOSFETs comprise numerous smaller FET cells sharing the same terminals. In ideal conditions, these smaller FET cells should share current equally. However, process-induced nonuniformities mean that there is always some current maldistribution. Therefore, process-induced electrical and thermal nonuniformities across the MOSFET cells will further enhance thermal runaway through current crowding. To mitigate this, UIS tests are usually done in the production line to screen out defective devices with process-induced nonuniformities that may compromise electrothermal ruggedness [5], [10].

In this paper, a 1.2-kV/24-A SiC MOSFET and a 1.2-kV/30-A silicon IGBT have been tested in UIS circuits at different temperatures. The devices have been tested to destruction at different ambient temperatures. Section II presents an electrothermal model that describes avalanche induced bipolar latchup. Section III describes the experimental setup as well as the results derived from the experiments. Section IV presents finite-element models of the devices, while Section V concludes this paper.

II. Electrothermal Model for Bipolar Latchup

An electrothermal model has been developed for the purpose of explaining the process of thermal runaway of MOSFETs conducting current in avalanche. The model uses an electrical input to calculate the temperature, which in turn is used to estimate temperature-dependent MOSFET parameters [11]. These MOSFET parameters (body voltage drop and in-built body potential) determine whether or not the parasitic bipolar has latched. The output is then fed back into the temperature model in a cyclical process. The model is based on an inductor forcing current through the MOSFET from the drain to the source, and assumes that the inductor has been precharged to a defined current. The current flowing through the MOSFET is described as

$$I_{(t)} = I_{\mathrm{AV}} - \frac{V_{(t)}t}{L} \tag{1}$$

where I_{AV} is the peak avalanche current, $I_{(t)}$ is the current flowing through the MOSFET, $V_{(t)}$ is the voltage across the MOSFET, L is the value of the inductor, and t is the time. The avalanche current is the peak current, and depends on how much current is initially stored in the magnetic field of the inductor. The inductance determines the peak value of the avalanche current together with the charging duration. The current determined from (1) is used to calculate the junction temperature of the MOSFET using

$$T_{(t)} = T_{\mathrm{AMB}} + R_{\mathrm{TH}} I_{(t)} V_{(t)} \left(1 - e^{-\frac{t}{R_{\mathrm{TH}} C_{\mathrm{TH}}}}\right) \tag{2}$$

where $T_{(t)}$ is the junction temperature of the MOSFET, T_{AMB} is the ambient temperature, R_{TH} is the thermal resistance of the MOSFET, and C_{TH} is the thermal capacitance of the MOSFET. The calculated junction temperature in (2) is used to calculate the built-in source to body p-n junction potential using [12]

$$\Phi_{\mathrm{bi}} = \frac{K_{\mathrm{B}} T_{(t)}}{q} \ln\left(\frac{N_{\mathrm{E}} N_{\mathrm{B}}}{n_{\mathrm{i}}^2}\right) \tag{3}$$

where Φ_{bi} is the built-in junction voltage of the parasitic BJT, K_{B} is the Boltzmann constant, q is the electric charge, N_{E} is the emitter (source) doping of the parasitic BJT (MOSFET), N_{B} is the base (body) doping of the parasitic BJT (MOSFET), and n_{i} is the intrinsic carrier concentration. The intrinsic carrier concentration has a temperature dependency that is material dependent and is different for silicon and SiC. Since SiC has a wider bandgap, it will have a lower intrinsic carrier concentration, and hence a higher built-in junction voltage (Φ_{bi}). For example, at 300 K SiC has an intrinsic carrier concentration of 1.5×10^{-8} cm^{-3}, whereas it is 1.5×10^{10} cm^{-3} for silicon. As a result, the built-in junction voltage for 4H–SiC will be approximately three times that of silicon [12]. As a consequence, the parasitic BJT will be harder to turn-ON in SiC since a greater voltage is needed to forward bias the emitter–base junction. The body resistance of the MOSFET is calculated using

$$R_{\mathrm{PB}} = \frac{l}{A N_{\mathrm{B}} q \mu_P} = \frac{l}{A N_{\mathrm{B}} q \cdot 495 \left(\frac{T}{300}\right)^{-2.2}} \tag{4}$$

where l is the length, A is the area, and μ_P is the hole mobility [12]. The voltage drop across the body resistance is calculated using

$$V_{\mathrm{PB}} = \frac{I_{\mathrm{C}}}{\beta} R_{\mathrm{PB}} \tag{5}$$

where I_{C} is the collector current of the parasitic BJT and β is the gain of the BJT. The condition for bipolar latchup is set by comparing V_{PB} to Φ_{bi}. The parasitic bipolar latches when $V_{\mathrm{PB}} > \Phi_{\mathrm{bi}}$. In this case, the current through the MOSFET is calculated using the following equation, which is originally derived for BJTs [12]:

$$I_{(t)} = qA \frac{D_{\mathrm{B}} n_{\mathrm{i}}^2}{W_{\mathrm{B}} N_{\mathrm{B}}} \left(e^{q \frac{V_{\mathrm{PB}} - \Phi_{\mathrm{bi}}}{K_{\mathrm{B}} T}} - 1\right). \tag{6}$$

If $V_{\mathrm{PB}} < \Phi_{\mathrm{bi}}$, the parasitic bipolar does not latch and the current through the MOSFET is determined by (1). Fig. 2 shows a schematic diagram illustrating how the electrothermal model works. Fig. 3(a) shows the trend of calculated normalized currents using the model in Fig. 2 at different ambient temperatures. Fig. 3 shows that the parasitic bipolar latches for higher ambient temperatures, but this is not the case for lower ones. The process of latching is characterized by a rising current, which in reality will be limited by the power supply, as will be demonstrated experimentally later on. Fig. 3(b) shows the calculated junction temperature of the MOSFET obtained from Fig. 2. It can be observed in Fig. 3(b) that there is a temperature rise resulting from the peak avalanche power. However, for the case of latchup, there is a subsequent temperature rise during the cooling period, which is due to

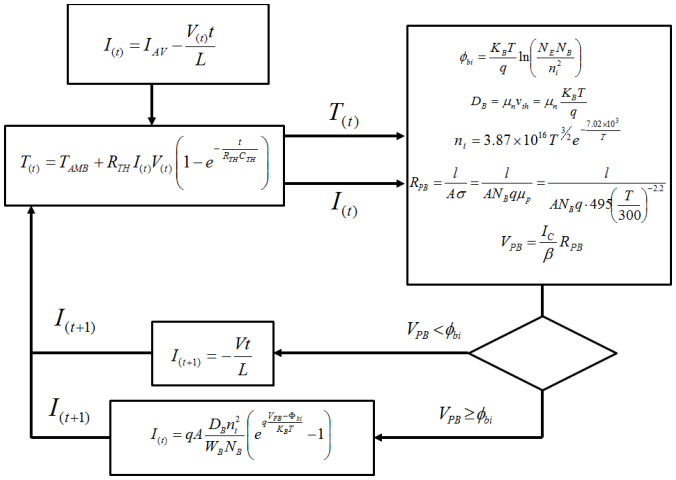


Fig. 2. Electrothermal model for parasitic BJT latchup for MOSFET in avalanche.

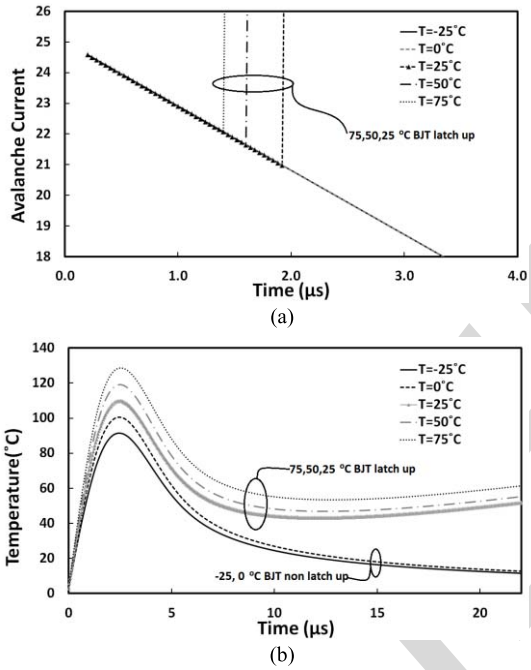


Fig. 3. (a) Calculated device current as a function of time at different ambient temperatures. (b) Calculated junction temperature as a function of time at different ambient temperatures.

the rising current from the activation of the parasitic BJT [1], [11]–[15]. With the detailed knowledge of device dimensions and process parameters, the calculations in Fig. 3(a) and (b) can be used by the designer as a predictor of BJT latchup for a specific device.

III. Experimental Measurements

A. Avalanche Performance at Fixed Currents

Fig. 4 shows the experimental setup and the circuit diagram that includes a gate-drive circuit, the environmental chamber, test enclosure, power supplies, and oscilloscopes. When the device under test (DUT) is switched ON, the inductor is charged to the peak avalanche current that is proportional to

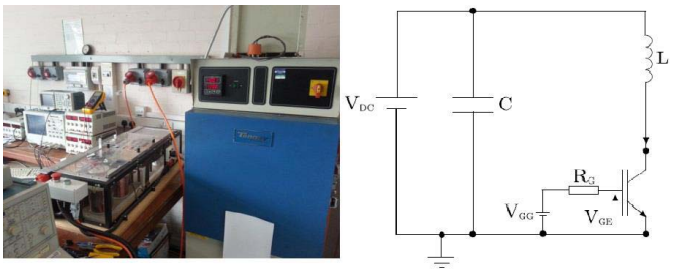


Fig. 4. Experimental setup showing UIS test and the circuit schematic diagram.

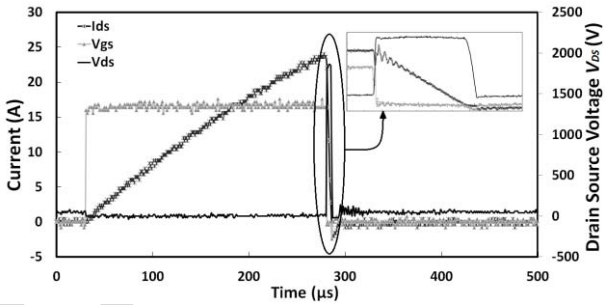


Fig. 5. V_{GS}, V_{DS}, and I_{DS} as functions of time for an SiC MOSFET under UIS.

the duration of the gate pulse. When the DUT is switched OFF, the current flowing through the inductor is interrupted, thereby causing the inductor to force current through the DUT. Since the DUT is OFF, current flows from the drain to the source through avalanche mode conduction. The drain–source voltage rises to a value that reaches the breakdown voltage as the current flows through the device [5], [16]. Fig. 5 shows the experimental measurements of the gate–source voltage (V_{GS}), the drain–source current (I_{DS}), and the drain–source voltage (V_{DS}) as functions of time for an SiC MOSFET undergoing UIS.

The devices used in the experiments were the 1.2-kV/24-A CREE SiC MOSFET with datasheet reference CMF10120D and the 1.2-kV/30-A Fairchild silicon IGBT with datasheet reference FGA15N120ANTD. The test was conducted at six different temperatures, namely −25 °C, 0 °C, 25 °C, 50 °C, 75 °C, and 100 °C. The performance of the device was examined under two different avalanche currents (24 and 35 A). The 35-A test exceeds the maximum forward current rating of the SiC MOSFET by 40% and the maximum current rating of the IGBT by 16%, thereby putting the SiC MOSFET under more electrothermal stress. Fig. 6(a) shows the drain–source voltage of the SiC MOSFET under UIS at the rated current for different temperatures.

Fig. 6(b) also shows the avalanche current characteristics of the SiC MOSFET at different temperatures. Fig. 6(c) shows the collector–emitter voltage of the IGBT under UIS, whereas Fig. 6(d) shows the collector–emitter current of the IGBT under UIS. The SiC MOSFET demonstrates temperature invariant characteristics and withstands all temperatures, whereas the silicon IGBT does not withstand the avalanche current at 100 °C, as can be observed in Fig. 6(c) and (d).

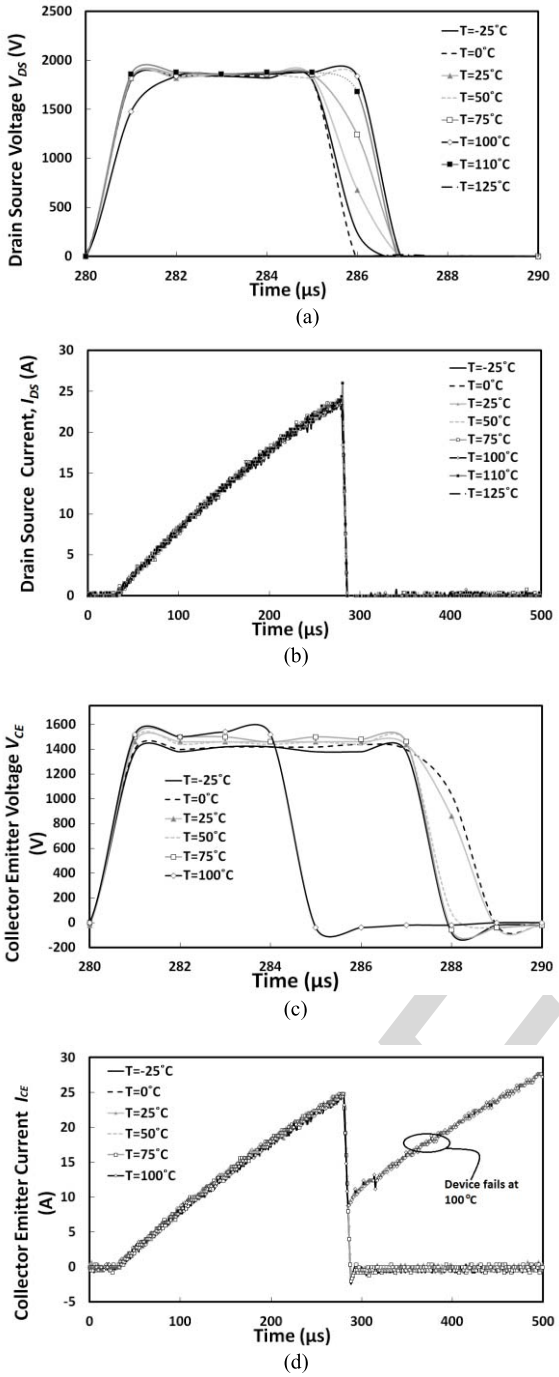


Fig. 6. (a) Drain–source voltage for the SiC MOSFET under UIS at different temperatures. (b) Drain–source current for the SiC MOSFET under UIS at different temperatures. (c) Collector–emitter voltage for the Si IGBT under UIS at different temperatures. (d) Collector–emitter current for the Si IGBT under UIS at different temperatures. Test current $I_{\mathrm{L}} = 24$ A.

In Fig. 6(c), the V_{CE} of the IGBT collapses to zero at the moment the short circuit across the device occurs. In Fig. 6(d), the current through the IGBT at 100 °C rises uncontrollably, thereby indicating BJT latchup. Subsequent tests on the device show that all the terminals were short circuited and the device was damaged.

Next, the SiC MOSFET was tested at 40% beyond its current rating, whereas the IGBT was tested at 16% beyond its current rating to ascertain the electrothermal ruggedness.

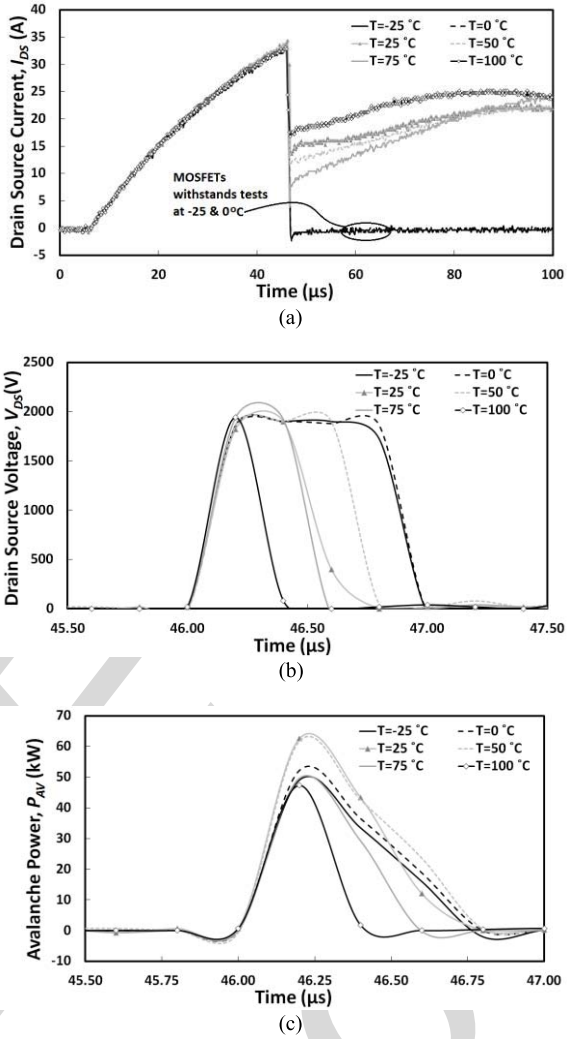


Fig. 7. (a) Drain–source current for the SiC MOSFET under UIS at different temperatures showing BJT latchup above 0 °C. (b) Drain–source voltage for the SiC MOSFET under UIS at different temperatures showing BJT latchup above 0 °C. (c) Avalanche power dissipated in the SiC MOSFET. Test current $I_{\mathrm{L}} = 35$ A.

Fig. 7(a) shows the avalanche current characteristics of the SiC MOSFET under different temperatures. The MOSFET withstands the test at the low temperature measurements (−25 °C and 0 °C). For temperatures above 25 °C, the current rises and is limited by the power supply, i.e., the MOSFET goes into thermal runaway. Subsequent tests on the devices showed that they are shorted between all three terminals, indicating that the devices had failed. The mechanism behind the temperature dependency of the devices ability to withstand UIS can be explained by Figs. 2 and 3. Fig. 7(b) shows the corresponding drain–source voltage (V_{DS}), where it can be seen that V_{DS} falls to zero more quickly as the temperature is increased. This occurs as a result of the fact that the voltage across the device collapses once the bipolar has latched.

Fig. 7(c) shows the avalanche power dissipated by the SiC MOSFET at different ambient temperatures. The amount of power dissipated by the device before the onset of the BJT latchup increases as the temperature decreases. This can be explained by the fact that dissipated power contributes to

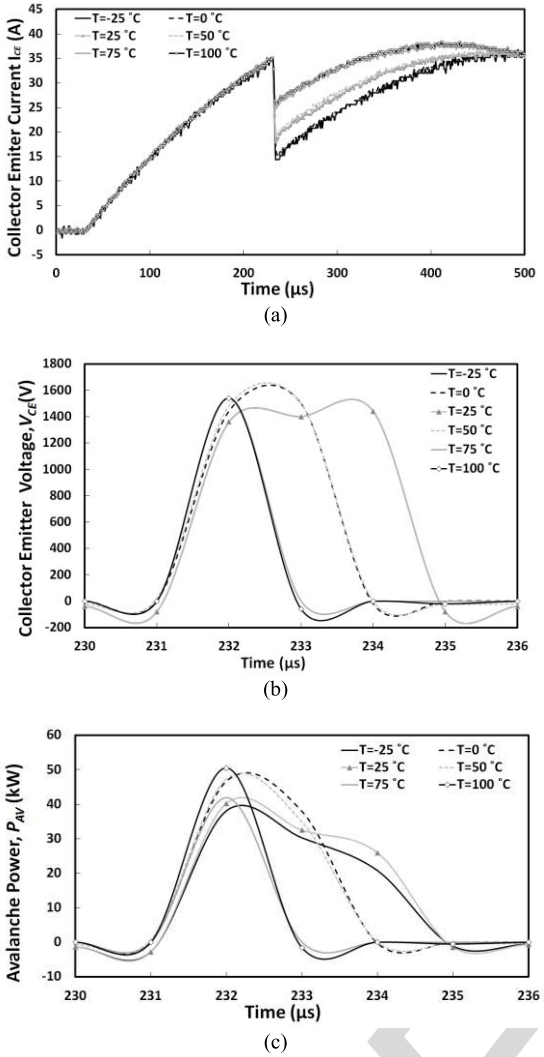


Fig. 8. (a) Collector–emitter current for the silicon IGBT under UIS at different temperatures. (b) Collector–emitter voltage for the silicon IGBT under UIS at different temperatures. (c) Avalanche power dissipated in the silicon IGBT. Test current $I_{\mathrm{L}} = 35$ A.

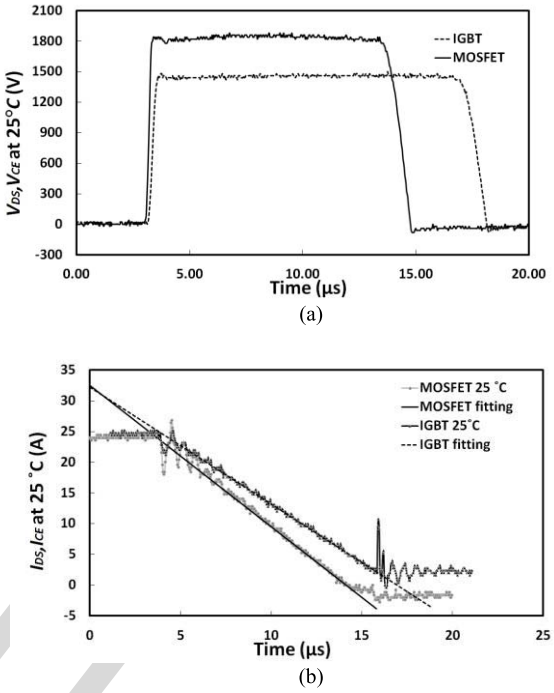


Fig. 9. (a) V_{DS} and V_{CE} for the IGBT and the MOSFET during avalanche mode conduction. (b) I_{DS} and I_{CE} for the IGBT and the MOSFET during avalanche mode conduction. Test current $I_{\mathrm{L}} = 35$ A.

temperature excursions within the device, and hence, when the device starts at a lower ambient temperature, there is more headroom to dissipate power before bipolar latchup. Fig. 7 is thus the experimental validation of Fig. 3 and the model developed for BJT latchup in Section II.

Fig. 8(a) shows the collector–emitter current of the silicon IGBT under UIS conditions with 35-A maximum avalanche current. It can be seen that unlike the SiC MOSFET, the silicon IGBT does not withstand the test at any temperature. A trend can also be noticed from the IGBT current. The latchup current (i.e., the current flowing through the device at the point when latchup occurs) increases with increasing temperature. Fig. 8(b) shows the collector–emitter voltage of the IGBT under UIS conditions at all the temperatures. Similar to the MOSFETs, the voltage across the device collapses to zero once the device latches. Fig. 8(c) shows the avalanche power dissipated before the onset of thermal runaway. The amount of avalanche power dissipated before the parasitic BJT latchup decreases with increasing temperature.

Fig. 9(a) shows the V_{CE} and V_{DS} characteristics of the IGBT and the MOSFET, respectively, during avalanche. It can be seen that the MOSFET has a higher breakdown voltage than the IGBT even though both devices are rated at 1.2 kV. Fig. 9(b) shows that the gradient of the avalanche current is higher for the IGBT. This happens because of the higher breakdown voltage of the MOSFET since $t = \mathrm{LI_{AV}}/(B_{\mathrm{VDSS}} - V_{\mathrm{DS}})$, where B_{VDSS} is the breakdown voltage, I_{AV} is the avalanche current, and t is the time. Hence, Fig. 9(b) shows that the avalanche current decreases as the avalanche duration increases.

B. Maximum Avalanche Current Determination

In this section of the experimental measurements, the goal is to determine the maximum avalanche current at a fixed temperature and fixed inductor (avalanche duration). This is done by increasing the pulse duration of the gate until device failure is initiated since the width of the gate pulse determines the peak avalanche current. The results of the measurements therefore show the peak avalanche current sustainable by the device. This test is conducted for both the SiC MOSFET and the silicon IGBT at different temperatures. Fig. 10 shows the experimental measurements of different peak avalanche currents for the SiC MOSFET at room temperature. The measurements show that extending the gate pulse gradually will eventually cause device failure when the peak avalanche current is reached at that specific temperature.

Fig. 11(a) shows the peak avalance current when the Si IGBT fails at different temperatures. Fig. 11(b) shows the equivalent results for the SiC MOSFET. It can be seen from both plots that the maximum avalanche current reduces with

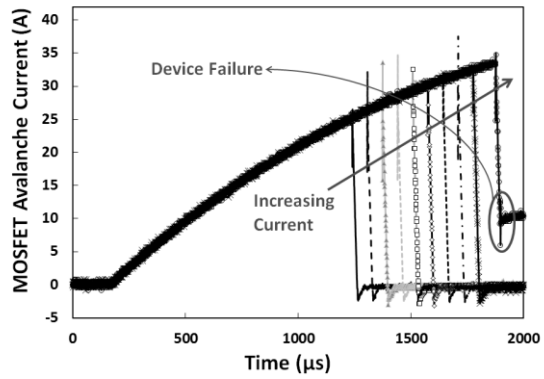


Fig. 10. Avalanche current as a function of time for different gate pulses showing the maximum avalanche current for SiC MOSFET.

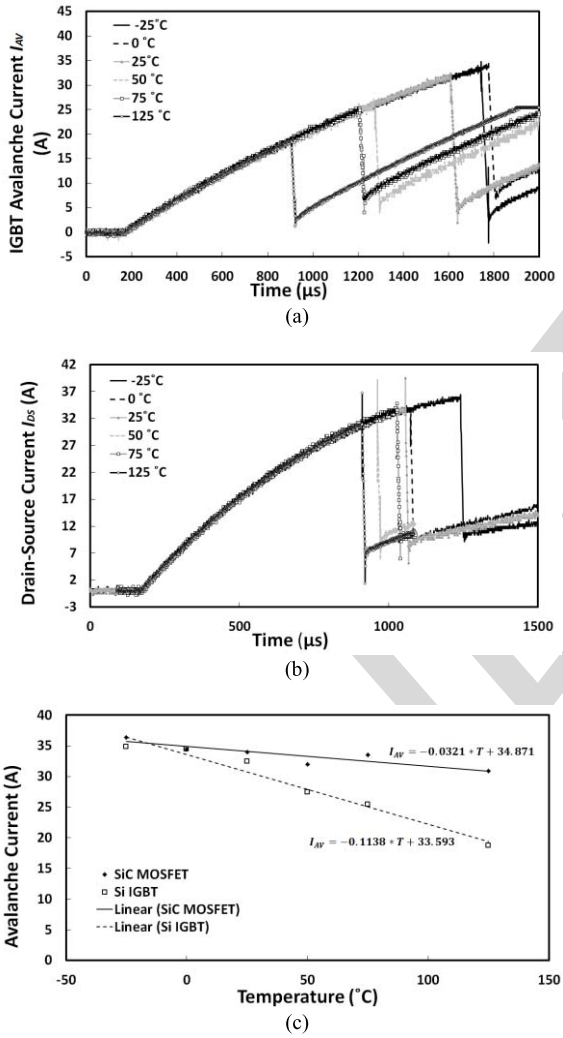


Fig. 11. (a) IGBT peak avalanche current as a function of time for different temperatures. (b) MOSFET peak avalanche current as a function of time for different temperatures. (c) Peak avalanche current as a function of temperature for the MOSFET and the IGBT.

increasing temperature for reasons explained earlier. The total charging time of the MOSFET is smaller than that of the IGBT as a result of the smaller ON-state resistance. Hence, less time is required for the device to reach a defined avalanche current. Fig. 11(c) shows the peak avalanche current sustained by the device before latchup as a function of temperature for both the silicon IGBT and the SiC MOSFET.

It can be observed that the absolute value of the slope of the maximum I_{AV} versus temperature is higher for the silicon IGBT, thereby indicating a less reliable device at elevated temperatures, i.e., there is greater temperature dependency of electothermal ruggedness in the IGBT than the MOSFET. The slope in Fig. 11(c) is -0.114 A/ °C for the silicon IGBT and -0.031 A/ °C for the SiC MOSFET. The x-axis intercept of Fig. 11(c) is an indication of the maximum operating temperature of the device. At this point, the elevated temperature causes enough thermal generation of carriers (through bandgap narrowing) that the carrier population is now equal to the background doping of the device, i.e., the device ceases to be a semiconductor. The extrapolated maximum operating temperature (x-axis intercept) for the silicon IGBT and the SiC MOSFET is 295 °C (568 K) and 1086 °C (1360 K), respectively. However, in reality, the device will fail long before the theoretical point as a result of process imperfections leading to current crowding and heat nonuniformity. This means that some parts of the MOSFET die will be at much higher temperatures compared with others. Furthermore, packaging constraints will further limit the maximum junction temperature to a value significantly lower than what the semiconductor device is capable of. It can be observed from Fig. 11(c) that the SiC device has a much higher maximum operating temperature by virtue of wider bandgap. The intrinsic carrier concentration can be calculated for silicon and SiC from the following [12]:

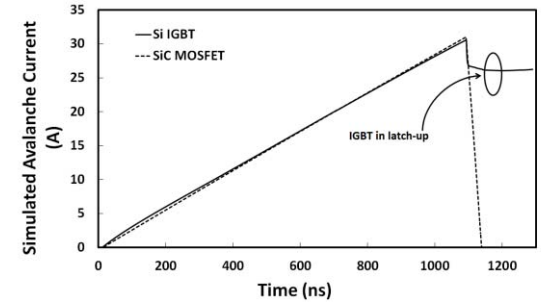
$$n_{\mathrm{i}} = 3.87 \times 10^{16}\ T^{3/2} \exp\left(-\frac{7.02 \times 10^3}{T}\right) \quad (7)$$

$$n_{\mathrm{i}} = 1.7 \times 10^{16}\ T^{3/2} \exp\left(-\frac{2.08 \times 10^4}{T}\right). \quad (8)$$

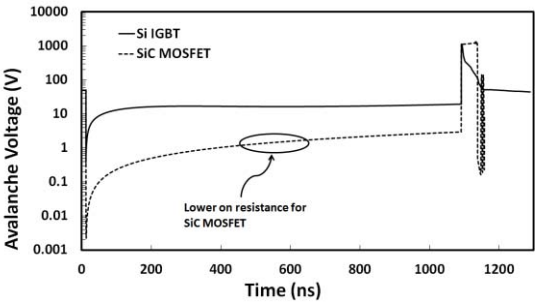
At 295 °C, the calculated intrinsic carrier concentration for silicon is 2.25×10^{15} cm^{-3}, whereas at 1086 °C, the calculated intrinsic carrier concentration for SiC is 1.92×10^{14} cm^{-3}. Hence, it is clear that the widebandgap of SiC enables better electrothermal ruggedness since the thermally generated carrier concentration for SiC is less than that of silicon even when the ambient temperature is 3.5 times higher [17].

IV. Finite-Element Models

Finite-element models have been developed to describe SiC MOSFET and silicon IGBT behavior under avalanche mode conditions. ATLAS from SILVACO was used to investigate the electrothermal behavior of the MOSFET during avalanche. The SiC device in the simulation was optimized to yield a breakdown voltage of 1200 V using an 8-μm depletion layer with a doping of 2×10^{16} cm^{-3}. The p-body doping and n-source was 1×10^{17} and 2×10^{19} cm^{-3}, respectively. The silicon IGBT is simulated with a drift layer doping of 1.1×10^{14} cm^{-3}, a p-body doping of 2.3×10^{17} cm^{-3}, and a voltage blocking drift layer thickness of 100 μm. The circuit in the simulator was identical to the one used in the experiment. The results of the simulations are shown in Fig. 12(a)–(c) for both the MOSFET and the IGBT.



(a)



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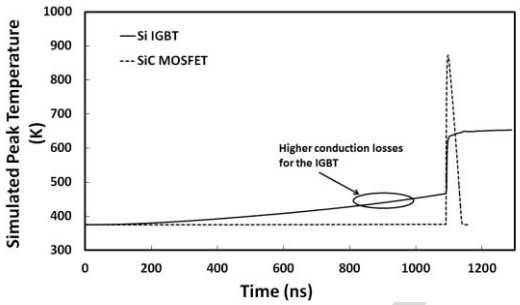
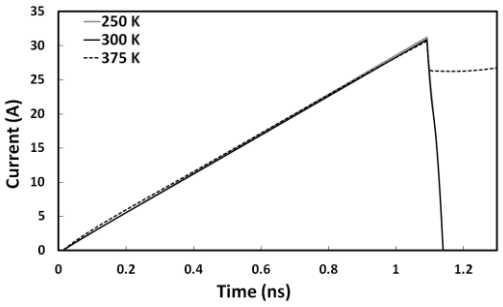


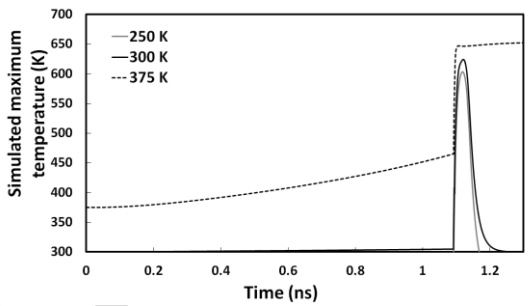
(c)

Fig. 12. (a) Simulated avalanche current as a function of time for the SiC MOSFET and the silicon IGBT. (b) Simulated avalanche voltage as a function of time for the SiC MOSFET and the silicon IGBT. (c) Simulated maximum temperature as a function of time for the SiC MOSFET and the silicon IGBT.

Fig. 12(a) shows the avalanche current as a function of time for the MOSFET and the IGBT. The ambient temperature of the simulation is 473 K, and the avalanche current is 35 A. It can be observed from Fig. 12(a) that the IGBT goes into latchup, whereas the MOSFET does not. Fig. 12(b) shows the voltage across the device as a function of time for both the SiC MOSFET and the silicon IGBT. It can be observed that the IGBT has a higher voltage during the inductor charging period than the MOSFET. This is due to the higher ON-state resistance of the IGBT as a result of the thicker drift layer compared with the SiC MOSFET, where the widebandgap and high critical field mean that a thinner voltage blocking epitaxial layer is needed. The modeled characteristics of the voltage of the device during avalanche is identical to what is observed experimentally, i.e., once the device goes into avalanche mode conduction, the voltage across the device rises to the breakdown voltage, and if the device latches, the voltage across the device falls to zero as the current rises. Fig. 12(c) shows the simulated maximum temperature of the device as a function of time during the inductor charging and the avalanche period.



(a)

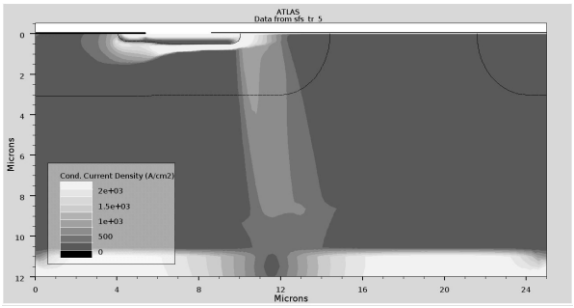


(b)

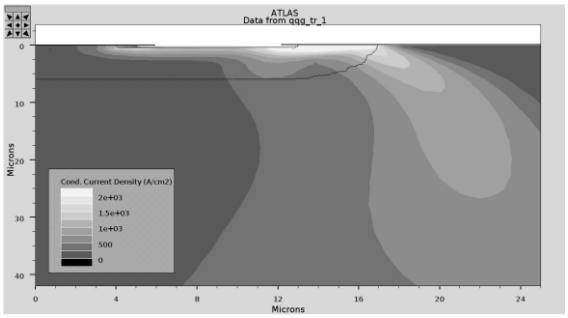
Fig. 13. (a) Simulated IGBT current during inductor charging and avalanche at different ambient temperatures. (b) Simulated IGBT current during inductor charging and avalanche at different ambient temperatures.

The IGBT shows a higher temperature rise during the inductor charging period as a result of the higher conduction losses compared with the SiC MOSFET. The rise of the SiC MOSFET temperature during avalanche is faster and the peak temperature is higher because of the smaller thermal time constant. The simulated SiC MOSFET will have a smaller thermal resistance (R_{TH}) because of the thinner epitaxial drift layer (thermal resistance increases with length in the direction of heat flow). SiC also has a thermal conductivity that is three times larger than silicon, and hence, the thermal resistance would reduce even further. The SiC MOSFET will also have a smaller heat capacitance (C_{TH}) as a result of the smaller die mass. Therefore, the smaller thermal time constant ($R_{\mathrm{TH}} \cdot C_{\mathrm{TH}}$) means that the rate of change of temperature with time will be higher, and hence, the faster heating and cooling shown in Fig. 12(c). It can also be seen in Fig. 12(c) that the IGBT never cools down unlike the SiC MOSFET. Fig. 13 shows more finite-element simulations for the silicon IGBT during inductor charging and avalanche mode conduction at different ambient temperatures. It can be observed from Fig. 13 that, similar to the case of the experimental measurements, higher temperatures induce latchup. Furthermore, in the finite-element analysis, the latchup occurs approximately at 650 K that is higher than what was extracted experimentally (568 K) by extrapolating the plots in Fig. 11(c). This is expected since the simulation does not take into consideration process imperfections and packaging constraints.

2-D current density contour plots of the SiC MOSFET and silicon IGBT were also extracted from the finite-element simulator. The results are shown in Fig. 14(a) for the MOSFET and Fig. 14(b) for the IGBT. In the case of the MOSFET, the current flow is concentrated, whereas in the IGBT, the current flow is dispersed. This is likely due to the fact that the voltage



(a)



(b)

Fig. 14. 2-D current density plots for the (a) SiC MOSFET and (b) silicon IGBT.

blocking drift layer of the SiC MOSFET is much thinner than that of the IGBT as a result of the higher critical electric field in SiC. The lower value of the thermal time constant of SiC means that heat is dissipated faster than that of silicon; hence, the temperature surge does not initiate bipolar latchup as is the case with the IGBT.

V. Conclusion

In this paper, the mechanism of parasitic bipolar latchup during avalanche mode conduction has been investigated for 1.2-kV/25-A SiC MOSFETs and 1.2-kV/30-A silicon IGBTs. It has been shown that the SiC MOSFET is more electrothermally rugged and can withstand higher temperature surges in spite of the fact that it has a lower current rating. The SiC device can withstand avalanche current 40% greater than the rated current at lower temperatures but not at higher temperatures. The IGBT is unable to withstand avalanche currents 16% beyond its rating. The SiC MOSFET can also withstand avalanche currents at the rated value at 125 °C. An electrothermal model was developed that explained why elevated temperatures accelerate the latching of the parasitic BJT, and the results are confirmed by finite-element modeling. The experimentally extracted maximum operation temperatures (extracted from avalanche current versus temperature plots) were compared with theoretical calculations using the temperature dependence of the intrinsic carrier concentration. The results showed a difference probably due to packaging constraints and process imperfections and that the SiC device is capable of withstanding approximately three times the temperature of Si. This was also supported by the finite-element models.

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Authors' photographs and biographies not available at the time of publication. AQ:7