Modeling of Temperature Dependent Parasitic Gate Turn-On in Silicon IGBTs

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***Abstract*—Parasitic turn-on can cause unintentional triggering of the IGBTs since the discharge current of the Miller capacitance coupled with high *dV/dt* can activate a device that should be off. The short circuit current resulting from parasitic turn-on coupled with the high voltage causes significant power dissipation which can be a reliability issue. This issue is exacerbated by higher ambient temperatures since the negative temperature coefficient of the IGBT's threshold voltage as well as the positive temperature coefficient of the minority carrier lifetime will increase the peak and duration of the short circuit current. Accurate modeling of the shoot-through power and its temperature dependency is important for circuit designers when designing mitigation techniques like multiple resistive paths and bipolar gate drivers. The physics-based model proposed in this paper can produce accurate results with good matching over temperature. The model improves on compact circuit models based on lumped parameters.**

***Index Terms*-- IGBT Parasitic Turn-On Modeling, Temperature Dependent, Shoot-through Current, Voltage Source Converter.**

NOMENCLATURE

C_{FB1}	Top IGBT feedback capacitance (F)
C_{FB2}	Bottom IGBT feedback capacitance (F)
I_{C1}	Top collector current (A)
I_{C2}	Bottom IGBT collector current (A)
I'_{C1}	Top IGBT observed current (A)
I'_{C2}	Bottom IGBT observed current (A)
I_{G1}	Top IGBT gate current (A)
I_{G2}	Bottom IGBT gate current (A)
I'_{G1}	Top IGBT internal gate current (A)
I'_{G2}	Bottom IGBT internal gate current (A)
I_{RL}	Load current (A)
K_p	MOSFET device transconductance (AV^{-2})
K_{p0}	MOSFET device transconductance at room temperature (AV^{-2})
L_{e1}	Top IGBT Kelvin emitter inductance (H)
L_{e2}	Bottom IGBT Kelvin emitter inductance (H)
L_{G1}	Top IGBT gate stray inductance (H)
L_{G2}	Bottom IGBT gate stray inductance (H)
L_{s1}	Top IGBT stray inductance (H)
L_{s2}	Bottom IGBT stray inductance (H)
R_{FB1}	Top IGBT feedback resistance (Ω)
R_{FB2}	Bottom IGBT feedback resistance (Ω)
R_{G1}	Top IGBT gate resistance (Ω)
R_{G2}	Bottom IGBT gate resistance (Ω)
R_L	Load resistance (Ω)
T	Temperature (K)
T_0	Room temperature (K)
V_{CE1}	Top IGBT collector-emitter voltage (V)
V'_{CE1}	Top IGBT observed collector voltage (V)
V_{CE2}	Bottom IGBT collector-emitter voltage (V)
V'_{CE2}	Bottom IGBT observed collector voltage (V)
V_{DC}	DC link or supply voltage (V)
V_{GE1}	Top IGBT gate-emitter voltage (V)
V_{GE2}	Bottom IGBT gate-emitter voltage (V)
V'_{GE1}	Top IGBT observed gate voltage (V)
V'_{GE2}	Bottom IGBT observed gate voltage (V)
V_{gg1}	Top IGBT gate drive voltage (V)
V_{gg2}	Bottom IGBT gate drive voltage (V)
$V_{L_{s1}}$	Top IGBT stray inductance voltage (V)
$V_{L_{s2}}$	Bottom IGBT stray inductance voltage (V)
V_{RL}	Load voltage (V)
V_{th}	Threshold voltage (V)
V_{th0}	Threshold voltage at room temperature (V)
μ_n	Electron mobility ($cm^2V^{-1}s^{-1}$)
μ_{n0}	Low-field (maximum) electron mobility ($cm^2V^{-1}s^{-1}$)
μ_p	Hole mobility ($cm^2V^{-1}s^{-1}$)
μ_{p0}	Low-field (maximum) hole mobility ($cm^2V^{-1}s^{-1}$)
τ_{HL}	High-level carrier lifetime (s)
τ_{HL0}	High-level carrier lifetime at room temperature (s)
τ_{lim}	Differentiator limiting time constant (s)

This work was supported by EPSRC Case Award funding in collaboration with Jaguar Land Rover Automotive PLC, UK, as well as EPSRC funding through the underpinning power electronics device theme research project (EP/L007010/1) and the component theme research project (EP/K034804/1).

I. INTRODUCTION

The unintentional turn-on of a power switching device in voltage source converters, which is influenced by the high switching frequency of the complementing device in the same phase leg is known as cross-talk or parasitic turn-on. The demand for higher switching frequency causes higher *dV/dt* and *dI/dt* which consequently coupled with the Miller capacitance of the device, induces a voltage greater than the threshold voltage of the device across the gate-emitter. Hence, a short circuit occurs across the leg of the inverter since both devices are simultaneously conducting [1].

In the half-bridge topology, which is the main block in the full-bridge and three-phase inverters, the power devices should not be switched simultaneously. However, due to parasitic turn-on, a high surge of current capable of destroying the devices can pass through the devices. The severity of this problem increases with the switching

frequency since the parasitic gate current is proportional to the turn-off *dV/dt*. In advanced new generation energy efficient power devices optimized for low conduction and switching losses, the die area, hence, the Miller capacitance is reduced. This will reduce the severity of the cross-talk problem, however, since these devices may be driven at higher *dV/dt*, the overall impact on cross-talk remains uncertain. Cross-talk reduces the reliability of the device since the instantaneous power dissipation is very high as the devices are driven into linear mode i.e. simultaneously high current through and high voltage across the device. As the devices are heated, the threshold voltage reduces as a result of higher thermal carrier generation in the MOS channel due to band-gap narrowing. This results in an even higher shoot-through current which increases the junction temperature more and possibly causes device degradation and destruction.

A well-known solution to suppress or even eliminate the self-turn-on in the gate of IGBTs in half-bridge topology is to use a negative offset in the gate-emitter of the IGBT. This creates a larger margin from the off-state to the threshold value. However this may not be effective if the switching *dV/dt* and *dI/dt* are high enough i.e. the negative voltage might not be able to fully eliminate the gate parasitic turn-on [2]. Hence, accurate modeling of the shoot-through power and its temperature dependency is very important for diagnosing and predicting the temperature surge due to shoot-through currents.

An increase in the ambient temperature of the device reduces the threshold voltage thereby reducing the margin for the off-state voltage. This also increases the short circuit duration since the device switches on sooner and the turn-off is delayed. Moreover, by increasing the temperature, the carrier mobility and carrier lifetime in the drift region of the IGBT decrease and increase respectively thereby causing an even higher surge current to flow through the device as the device heats up. Consequently, it is important for the power electronics engineers to be able to predict the shoot through current as a function of switching rate and temperature. This will help is determining the magnitude of negative bias offset.

Compact circuit simulators such as SPICE or PLECS are based on lumped parameters and cannot accurately predict the voltage and current waveforms to the degree needed for reliability prognosis. During the parasitic turn-on, the Miller capacitance is varied based on the voltage across the depletion width of the device. This nonlinear behavior of the Miller capacitance is important in determining the shape of the voltage and current waveform. The Miller capacitance is formed from two capacitors; an oxide capacitance (fixed value) and a depletion capacitance (voltage dependent). The coupling between the output waveforms and gate waveforms through the Miller capacitance is also critical. Moreover, the behavior of the drift region, which can be explained by the ambipolar diffusion equation, affects the voltage and current waveforms due to the charge stored in the drift region of the bipolar device. This charge brings about aspects of device characteristics like IGBT tail current and PiN diode reverse recovery. These are not accurately modeled in simulators based on lumped parameter models. Hence, a fast and accurate way of modeling the physics behind cross-talk in IGBTs is essential for good power electronics design.

The model proposed in this paper is based on the physics of the devices and can accurately take an account of the minority carrier distribution profile in the drift region of the bipolar devices by reconstructing the ambipolar diffusion equation. The Miller capacitances are calculated using fundamental device physics equations. Section II explains the model development and the experimental setup used to test the self-turn-on. Section III shows the results obtained from the experiment and compares them with the simulation while the last section concludes the paper.

II. Model Development and Experimental Setup

The use of the Fourier series to reconstruct the ambipolar diffusion equation in the drift region of a bipolar device has been detailed in multiple publications [3-17]. Using the drift and diffusion current equations, the behavior of the charge storage region is explained in the model which also takes the displacement current resulting from voltage dependent depletion widths into account. Moreover, the equations used in the model takes account of the Schockley-Read-Hall recombination, the Auger recombination, carrier-carrier scattering, depletion layers behavior depending on the minority carrier profile, the depletion widths and local carrier lifetime. Hence, it provides more details about the dynamic transient of the device. Moreover, as explained earlier, the Miller capacitance in the model depends on the depletion width and is voltage dependent. The model is computationally efficient and can accurately predict the switching behavior of IGBTs by reconstructing the ambiopolar diffusion equation. The behavior of the device can also be simulated using finite element device simulators such as Silvaco, however, this method is the most computationally inexpensive way of solving ADE without too much loss of accuracy. The model is developed in MATLAB/Simulink and the physical parameters of the device are used as input to the system. The parameters are extracted from the datasheet of the IGBTs and by comparing the simulation waveforms with the experimental switching waveforms obtained from the device using clamped inductive switching test rig.

Fig. 1 (a) shows the schematic of the half-bridge used in the experiments to investigate the parasitic turn-on. This circuit is used in the test rig to capture the shoot-through current and voltage waveforms. As can be seen, the model includes the parasitic inductances at the gate, emitter and collector of the device and it takes account of the parasitic capacitors within the device. Fig. 1 (b) is the actual experimental setup. During the experiment, a pulse is applied to the gate of the bottom switch and gate of the top switch is kept at the off-state voltage.

In order to change the temperature of the device, the DUTs (devices under test) were mounted on a hot plate and the temperature of the hot plate was controlled. The

cross-talk effect can be increased by using a larger gate resistance at the gate of the bottom IGBT which is not switching. In this study, the top gate resistance is kept at 10 Ω while the bottom gate drive is set to be 100 Ω. Using Kirchhoff's circuit laws on this circuit, equations (1-16) are obtained.

$$I_{G1} = I'_{G1} + (V_{CE1} - V_{GE1})(\frac{sC_{FB1}R_{FB1}}{1+sC_{FB1}R_{FB1}})(\frac{1}{1+s\tau_{lim}}) \quad (1)$$

$$I_{G2} = I'_{G2} + (V_{CE2} - V_{GE2})(\frac{sC_{FB2}R_{FB2}}{1+sC_{FB2}R_{FB2}})(\frac{1}{1+s\tau_{lim}}) \quad (2)$$

$$I'_{G1} = \frac{1}{L_{G1}}\int (V_{gg1} - I'_{G1}R_{G1} - V'_{GE1})\, dt \quad (3)$$

$$I'_{G2} = \frac{1}{L_{G2}}\int (V_{gg2} - I'_{G2}R_{G2} - V'_{GE2})\, dt \quad (4)$$

$$I_{C1} = I'_{C1} - (V_{CE1} - V_{GE1})(\frac{sC_{FB1}R_{FB1}}{1+sC_{FB1}R_{FB1}})(\frac{1}{1+s\tau_{lim}}) \quad (5)$$

$$I_{C2} = I'_{C2} - (V_{CE2} - V_{GE2})(\frac{sC_{FB2}R_{FB2}}{1+sC_{FB2}R_{FB2}})(\frac{1}{1+s\tau_{lim}}) \quad (6)$$

$$V_{L_{s2}} = V_{RL} - V'_{CE2} \quad (7)$$

$$I'_{C2} = \frac{1}{L_{s2}}\int V_{L_{s2}} dt = \frac{1}{L_{s2}}\int (V_{RL} - V'_{CE2}) dt \quad (8)$$

$$V_{L_{s1}} = V_{DC} - V'_{CE1} - V_{RL} \quad (9)$$

$$I'_{C1} = \frac{1}{L_{s1}}\int V_{L_{s1}} dt = \frac{1}{L_{s1}}\int (V_{DC} - V'_{CE1} - V_{RL}) dt \quad (10)$$

$$I_{RL} = I_{C1} + I_{G1} - I'_{C2} \quad (11)$$

$$V_{RL} = I_{RL}.R_L \quad (12)$$

In equations (13) to (16), the differentials of the currents I_{C1}, I_{C2}, I_{G1}, and I_{G2} are used that are taken from the inputs to the integrators used to calculate I_{C1}, I_{C2}, I_{G1}, and I_{G2}. The differential limiting time constant τ_{lim} is set to 10^{-12}s.

$$V'_{CE2} = V_{CE2} + L_{e2}(I_{C2} + I_{G2})(\frac{1}{1+s\tau_{lim}}) \quad (13)$$

$$V'_{CE2} = V_{CE2} + L_{e2}(I_{C2} + I_{G2})(\frac{1}{1+s\tau_{lim}}) \quad (14)$$

$$V'_{GE2} = V_{GE2} + L_{e2}(I_{C2} + I_{G2})(\frac{1}{1+s\tau_{lim}}) \quad (15)$$

$$V'_{GE1} = V_{GE1} + L_{e1}(I_{C1} + I_{G1})(\frac{1}{1+s\tau_{lim}}) \quad (16)$$

The temperature dependent parameters for the IGBT are described in equations (17-20) below [16, 17]. In equations below, T is the quasi static temperature of the device, T_0 is the room temperature V_{th0}, K_{p0}, τ_{HL0}, $\mu_{n0,p0}$ are the threshold voltage, MOS transconductance, high level lifetime, electrons and holes mobility of the device at the room temperature respectively.

$$V_{th} = V_{th0} - 9 \times 10^{-3}(T - T_0) \quad (17)$$

$$K_p = K_{p0}\left(\frac{T_0}{T}\right)^{0.8} \quad (18)$$

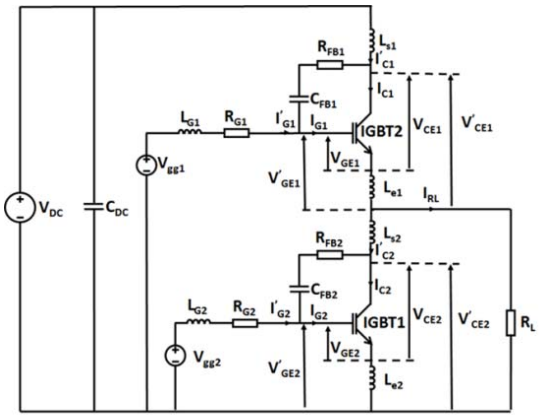
$$\tau_{HL} = \tau_{HL0}\left(\frac{T}{T_0}\right)^{1.5} \quad (19)$$

$$\mu_{n,p} = \mu_{n0,p0}\left(\frac{T_0}{T}\right)^{2.5} \quad (20)$$

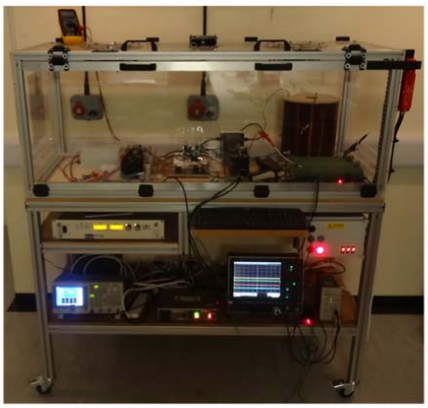
III. Results and Discussion

The experimental results showing the parasitic turn-on current waveform is shown in Fig. 2 (a) while Fig. 2 (b) shows the simulation results under the same conditions. As can be seen, the model closely matches the experimental results. By increasing the temperature, the shoot-through current increases and this is due to the reduction in the threshold voltage and increase of the minority carrier lifetime in the drift region of the device. As the temperature increases, the threshold voltage of the device reduces based on equation (17). This consequently causes the device to switch on earlier and also delays the switch-off of the device. Consequently, the period of time in which the shoot-through current passes through the device increases. Moreover, as the minority carriers increase with the rise in temperature, the peak of the shoot-through current increases which can be seen in both experimental results and the simulation in Fig. 2.

Fig. 3 (a) shows the collector-emitter voltage experimental waveform. As can be seen, the voltage waveform starts with a sharp slope and then it changes to a less steep slope i.e the collector-emitter voltage transient of the IGBT exhibits 2 distinct *dV/dts*. These two slopes are as a result of the Miller capacitance which consists of two capacitors; a fixed gate oxide capacitor and a voltage dependent depletion capacitor. The first high *dV/dt* is due to the gate oxide capacitance which is a constant value that depends on the oxide thickness and gate-source overlap area. The second smaller *dV/dt* is due to the depletion capacitance which is voltage dependent and changes with V_{CE}. As V_{CE} increases, the collector-body depletion width increases thereby decreasing the depletion capacitance. The overshoot in the voltage is due to the stray inductance in the collector of the IGBT. As the depletion width in the body of the IGBT extends through the drift region, punch-through occurs (the body of the device becomes fully depleted of minority carriers), thereby causing a rapid removal of minority carriers from the charge storage region. When the depletion layer punches through, the voltage waveform enters goes into saturation. At this point there is not enough displacement current due to the depletion formation that can supply the stray inductance with a current. Consequently, the change in the current causes a sudden voltage drop in the collector-emitter of the device. This brings about the second oscillations in the gate-emitter voltage waveform since the rapid *dV/dt* in the V_{CE} characteristics is fed-back to the gate characteristics through the Miller capacitance. Next, the voltage drops until it reaches the steady state point. Fig. 3 (b) shows the collector-emitter voltage obtained from the model. The



(a)



(b)

Fig. 1. (a) Schematic of the half bridge used in the experimental setup. (b) Experimental setup used for parasitic turn-on.

results show that the model can accurately predict the voltage behavior during the parasitic turn-on. As will be shown in subsequent figures, predicting the shape of this V_{CE} waveform is critical in accurately determining the power dissipation. The model and experimental results of Fig. 3 show that there is a rightward shift in the characteristics with increasing ambient temperature. The shift in the collector-emitter voltage characteristics is due to the increase of the carrier lifetime with temperature which means that more time is required for the carriers to be extracted from the device before the device switches off.

Fig. 4 (a) shows the gate-emitter voltage during the parasitic turn-on. The parasitic gate waveform is characterized by two peaks. The first peak is transition between the fixed oxide capacitance and the voltage dependent depletion capacitance. The time occurrence of this peak coincides with the inflexion point between the *dV/dts* in the V_{CE} characteristic of the IGBT turn-off transient. The second peak is due to the high negative collector-emitter voltage caused by the punch-through of the depletion capacitor. As explained earlier, when the charge storage region of the IGBT is fully depleted, no more current can pass through the device and this causes a large *dI/dt* on the parasitic stray inductance of the device. Consequently, due to the presence of the stray inductance, this sudden current change causes a sudden drop in the collector-emitter voltage of the device. This sudden *dV/dt* coupled with the Miller capacitance of the device induces a peak in the gate-emitter voltage of the device. Consequently, a second peak in the gate voltage can be observed. It can be seen in Fig. 4 that the time occurrence of the second peak in the parasitic V_{GE} characteristics coincides with the rapid negative *dV/dt* of the IGBTs V_{CE} transient. Fig. 4 (b) shows the model predicting this behavior during the punch-through.

Fig. 5 shows the power dissipated in the device due to the short-circuit happening during the cross-talk. As can be seen, the power losses peaks at approximately 86 kW in the short period of the parasitic turn-on for a single switching event. By continuous switching the device this large power dissipation is capable of quickly increasing the junction temperature of the device and this can be a reliability hazard for the operation of a voltage source inverter. It can be seen that increasing the ambient temperature in Fig. 5 from 25°C to 120°C increases the peak shoot-through power by 50.28% (from 56.26 kW to 84.55 kW) for the experimental measurements and 50.56% (from 86.98 kW to 57.77 kW) for the simulations. Hence, Fig. 5 shows that the simulations are able to very accurately predict the rate of change of shoot-through power with temperature.

One way to mitigate this phenomenon is to apply a negative gate voltage as the off-state voltage level. The model is capable of predicting the behavior of the inverter when a negative voltage is applied as an off-state voltage for the IGBTs using a bipolar gate drive. The peak of the shoot-through current can be reduced significantly by using this mitigation method. Fig. 6 shows the simulation results using the negative gate voltage. In this study, the off-state of the gate driver is set to be -5 V and the on state remains as 18 V. As can be seen, the peak of the shoot-through approximately reduced 10 times in comparison to the time when 0 V were used as the off-state voltage (unipolar gate drive). This is due to the fact that the negative gate voltage increases the margin between the off-state and the threshold voltage of the IGBT. Fig. 6 (a) shows the shoot-through current under the above condition. The duration of the short-circuit is reduced using this mitigation method and the peak of the current is reduced to approximately 8A at room temperature in comparison to Fig. 3 which is about 80A at the same temperature. The power dissipated in the device parasitically turned on using the bipolar gate drive reduced to approximately 5 kW at room temperature in comparison to Fig. 5 which peaks at almost 10 times larger value. As can be seen in Fig. 6, by increasing the temperature of the device, the shoot-through current increases and consequently the switching power loss due to the parasitic turn-on increases. Although the power losses in this case are significantly smaller, however it is still capable of increasing the junction temperature of the device. Hence, it is important to be able to predict the power losses due to cross-talk.

The simulation results shown in Fig. 6 can be validated using the experimental results shown in Fig. 7. Fig. 7 compares the shoot-through current of the device at room

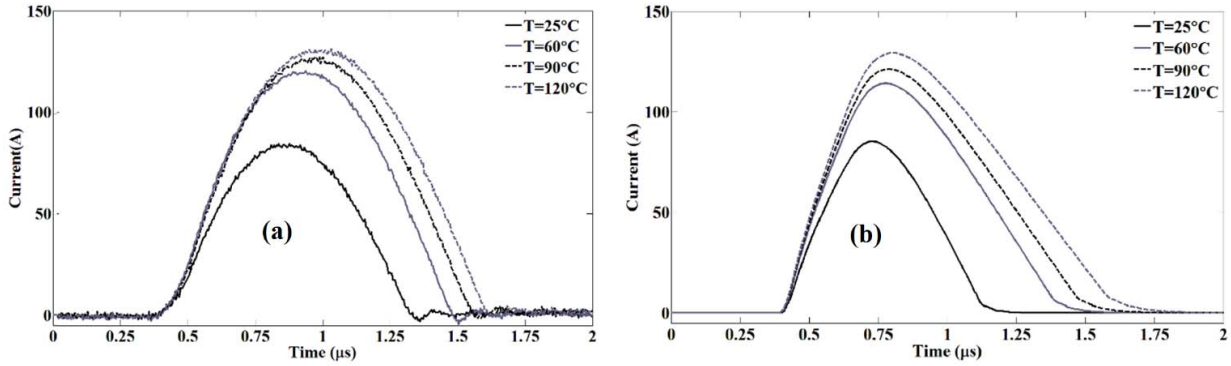


Fig. 2: (a) Experimental result showing parasitic turn-on current waveform for different temperatures. (b) the simulation results under the same conditions.

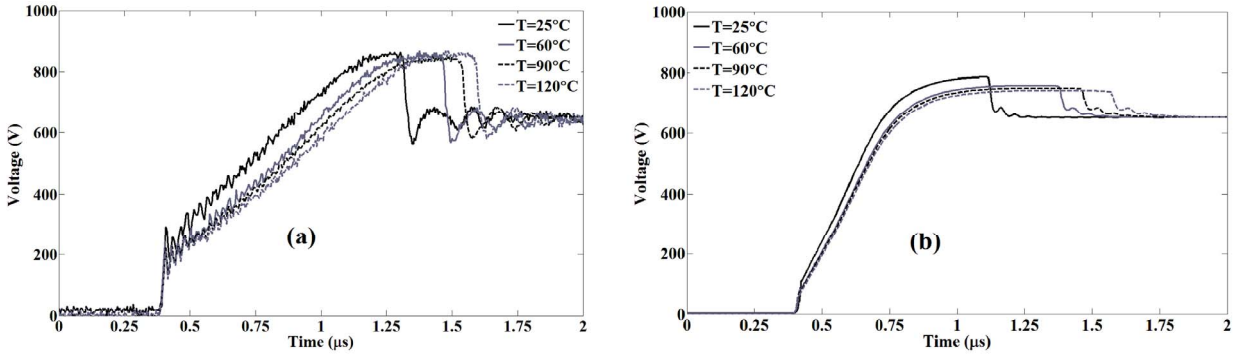


Fig. 3: (a) Experimental result showing parasitic turn-on collector-emitter voltage waveform for different temperatures. (b) the simulation results under the same conditions.

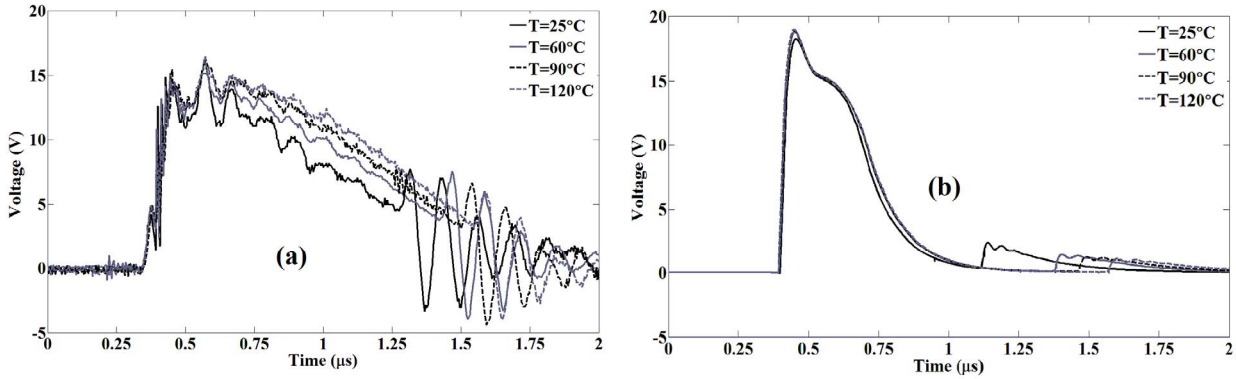


Fig. 4: (a) Experimental result showing parasitic turn-on gate-emitter voltage waveform for different temperatures. (b) Simulation results under the same conditions.

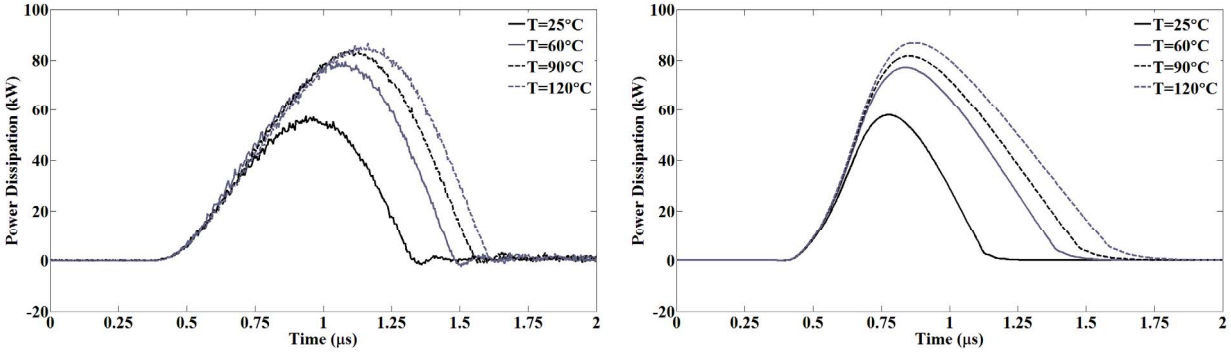


Fig. 5: (a) Experimental result showing power losses due to cross-talk for a single switching event for different temperatures. (b) Simulation results under the same conditions.

temperature using the same gate resistors as in the simulation. As can be seen, the bipolar gate drive reduces the shoot-through current by the factor of 10 at the room temperature. Fig. 8 shows the calculated peak power dissipated due to cross-talk as a function of the negative gate bias. This plot is important in determining the magnitude of the negative bias required to completely eliminate cross-talk in the converter. It is important to minimize the magnitude of the negative bias on the IGBT gate in the off-state because negative bias is stressful to oxide integrity. Negative bias causes positive fixed oxide charge trapping which can cause threshold voltage drift and other long term reliability issues regarding gate dielectric integrity. Although good IGBTs are now designed with negative gate voltage capability, the model presented in this paper is capable of optimizing the magnitude of negative bias given the switching rates and ambient temperatures.

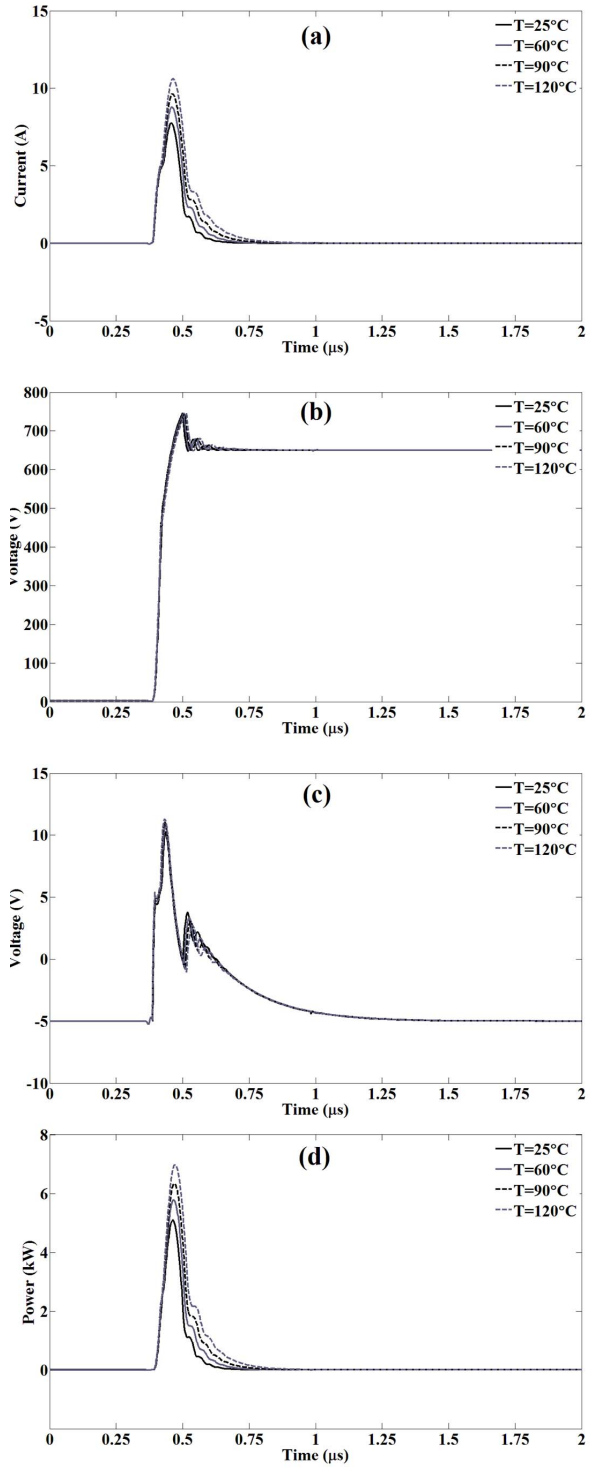


Fig. 6: Simulation result showing (a) shoot through current (b) collector-emitter voltage (c) gate-emitter voltage (d) power losses due to cross-talk for a single switching event for different temperatures.

IV. Conclusions

A physics based model for accurately predicting parasitic turn-on of an IGBT has been presented together with experimental measurements. The model takes account of the temperature dependent parameters such as the threshold voltage and the minority carrier lifetime. Hence, it can accurately show that the modelled shoot-through current, collector-emitter voltage and gate-emitter voltage transients replicate the experimental measurements with good precision at different temperatures. The results indicate that the shoot through current increases with the temperature due to the reduction of the threshold voltage. The collector-emitter voltage is shifted and becomes longer due to the increase in the carrier lifetime with temperature. Also, the *dV/dt* reduces with the temperature which is the case for the IGBT. The Miller capacitance in the proposed model consists of an oxide capacitor and a depletion capacitor which varies with voltage. This physics-based model can

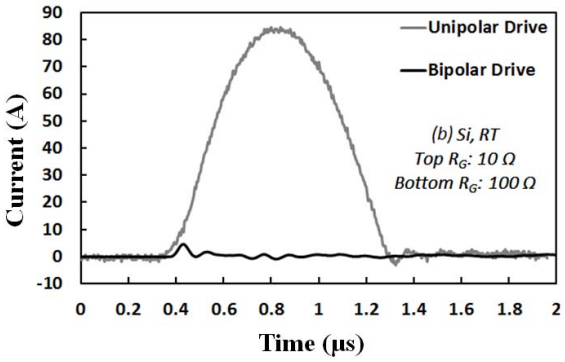


Fig. 7 Experimental result showing the comparison between the shoot-through current using unipolar gate drive and bipolar gate drive.

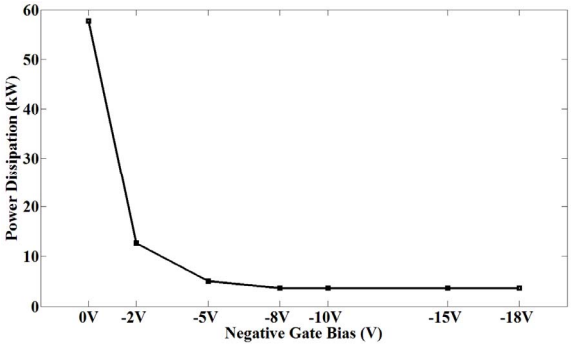


Fig. 8 Simulation result showing the peak power dissipation as a function of negative gate voltage at room temperature for 10Ω gate resistance at the top switch and 100Ω gate resistance at the bottom switch.

accurately predict current and voltage transients as opposed to compact models that use lumped parameters. Using Kirchhoff's current and voltage laws, the circuit models were developed and the device models were developed using a Fourier series based solution to the ambipolar diffusion equation to reconstruct the carrier density profile in the drift region of the bipolar device. It was demonstrated that the power losses due to the parasitic turn-on of IGBTs in a voltage source inverter is capable of increasing the junction temperature of the device significantly. Hence, the model is very useful in predicting the behavior of the device at different conditions such as temperature, gate resistance or physical device parameters such as gate oxide thickness, ratio of intercell area to active die area etc. Moreover, it was discussed that this effect can be reduced by applying negative gate voltage which can increase the margin between the off-state and the threshold voltage of the transistor. However, this method is less effective at higher temperatures where *dV/dt* across the device is high enough to trigger the gate-emitter of the device. The same method and technique can be used in case of a voltage source inverter based on SiC power MOSFETs. In the case of SiC MOSFETs, the threshold voltage of the device is significantly smaller than that of Si IGBTs. Moreover, the gate of these devices cannot withstand large negative voltage in comparison with the Si IGBTs. Consequently, it is even more important for power electronics engineers to be able to predict the shoot-through current as a function of switching rate and temperature.

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