Simulation of a new hybrid Si/SiC power device for harsh environment applications

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Abstract.

A new power device structure is proposed, conceived to operate in a high temperature, harsh environment, for example within a motor drive application down hole, as an inverter in the engine bay of an electric car, or as a solar inverter in space. The lateral silicon power device resembles a laterally diffused MOSFET (LDMOS), such as those implemented within silicon on insulator (SOI) substrates. However, unlike SOI, the Si thin film has been transferred directly onto a semi-insulating 6H silicon carbide (6H-SiC) substrate via a wafer bonding process. Thermal simulations of the hybrid Si/SiC substrate have shown that the high thermal conductivity of the SiC will have a junction-to-case temperature approximately 4 times less that an equivalent SOI device, reducing the effects of self-heating. Electrical simulations of a 600 V power device, implemented entirely with the silicon thin film, suggest that it will retain the ability of SOI to minimise leakage at high temperature, but does so with 50% less conduction losses.

1. Introduction

Harsh environment electronics is a technology area that is at the forefront of 21st century applications. Space, oil and gas exploration, aerospace, electric vehicles, mass transport and renewables are all linked by the need for electronic solutions that can operate efficiently and reliably in extreme surroundings including the very hot, the very cold, in applications with great vibration or shock, or where radiation, humidity or electromagnetic interference are an issue. Power electronic devices play a key role within numerous harsh environment applications, and improving their performance at higher maximum temperatures will have significant impact. For example, the potential reduction or even elimination of cooling systems in a planetary mission such as ESA's BepiColumbo or Venus Express would lengthen mission duration [2], while the mounting of electronics directly on the car engine frees up precious space and weight in the car engine bay [3]. In the downhole environment (as in Space), system reliability is paramount [4], and motor drives applications must continue to operate efficiently at temperatures above 150°C.

In this paper, we introduce a new silicon-on-silicon carbide (Si/SiC) semiconductor substrate in which Silicon power electronic devices, rated from 50 to 600 V are simulated. As devices implemented in bulk SiC are unable to operate in this voltage range, the hybrid Si/SiC substrates offer a solutions that is better able to handle the negative effects of temperature than bulk silicon (Si) or silicon-on-insulator (SOI) technologies. We will first introduce the problems that current Si and SOI solutions face when operating at temperatures of up to 300°C, before introducing the Si/SiC concept, using thermal simulations to show the SiC-like performance that can be attained. We then detail the electrical performance of lateral power devices simulated in the Si layer, and compare them to the equivalent state of the art in Si and SOI.

2. The problems of high temperature and self-heating in Power Electronics.

In general, the performance of any semiconductor device degrades the greater the temperature it is operating in [5], leading to greater losses and reduced efficiency. Power MOSFETs, which are most commonly limited by conduction losses, suffer major increases in on-resistance as temperature increases. At approximately 110°C the resistance of a typical Si power MOSFET [6] doubles from its room temperature value, the same occurs at around 150°C for a SiC MOSFET [7]. In contrast, the resistance of some IGBTs have a negative temperature coefficient, preventing them from being easily paralleled with uneven current sharing leading to thermal runaway until it is overloaded. However, for a single IGBT, it is the switching losses that become unmanageable at high temperature, with turn-off losses doubling with just a 50°C rise in temperature [8]. Leakage currents affect both devices, rising exponentially with temperature to compromise the off-state. The maximum temperature a device can theoretically operate

at is dictated by the number of intrinsic carriers that are thermally excited across the bandgap at the given temperature. When this reaches a level equivalent to the intentional doping, p-n junctions are compromised. In narrow bandgap materials, such as Ge and Si, this will occur at 150°C and 320°C respectively, while for the very wide bandgap materials, SiC and GaN, this limit is significantly higher, well beyond the capabilities of any realisable packaging solution.

The negative effects of temperature are made worse in power devices by self-heating, which can be viewed as the (in)ability of a material to remove any heat generated whilst it is operating. Materials with a high thermal conductivity (SiC, even diamond) will effectively remove this heat away from the active area, through the packaging to the heat sink, and any active cooling. Materials with a lower thermal conductivity (Si, GaN, Ge) will suffer from trapped heat, raising the temperature of the electrically active region to a temperature above the ambient. At the extreme, thermal runaway can occur, whereby the trapped heat locally increases the resistance of the semiconductor, which in turn increases the power loss, further heating up the semiconductor, increasing resistance, and so on. This limits the maximum power that the device can handle. This is illustrated in Figure 1 where the simulated DC characteristics of a diode implemented in silicon-on-insulator material are shown alongside the local temperature. In this example, at 3 V the temperature is shown to be nearly 200°C greater than the ambient, and no increase in voltage will permit any more current throughput.
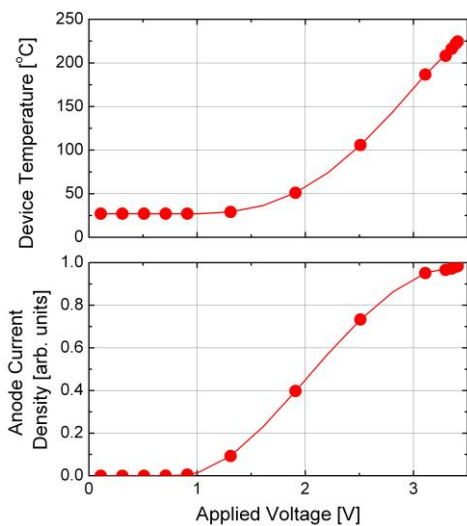
Figure 1: Self heating, as modelled within the DC characteristics of a SOI diode.
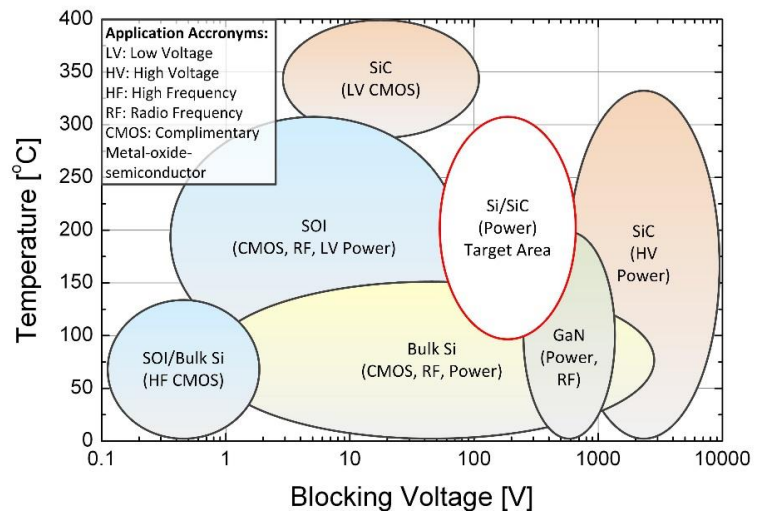
Figure 2: The technologies discussed in this paper, including the Si/SiC transistors, mapped in terms of blocking voltage capability and temperature. The 50-600V rating is typical of power applications such as downhole motor drives and automotive and solar inverters.
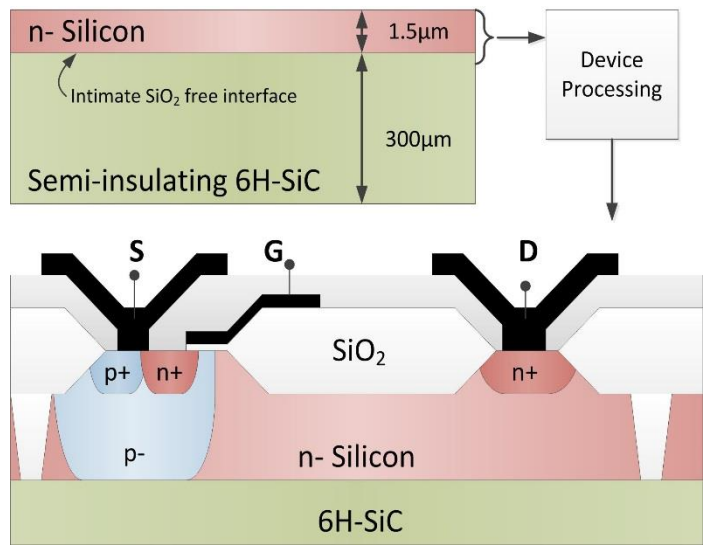
A selection of existing semiconductor device technologies are mapped out in Figure 2 in terms of their potential voltage rating and temperature. A common material for dealing with raised temperature is silicon-on-insulator (SOI) [3, 5, 9], which has been widely adopted in low voltage (LV) applications operating above 150°C ambient. The trick of SOI is to minimise the negative effects of temperature by surrounding active junctions on all sides by an insulating oxide, SiO_2. Compared to bulk Si devices, this reduces the p-n junction area by approximately 10 times, reducing leakage currents at any operating temperature, by approximately 100 times [5]. However, just as SiO_2 is a good electrical insulator, it also a good thermal insulator, which means that the problem of self-heating is many times worse in SOI than it is in bulk material.

The potential application space for silicon carbide power devices are mapped out in Figure 2. The material's wide bandgap means it has a very high maximum operating temperature, whilst a thermal conductivity three times that of Si minimises self-heating effects. To this end, research activity into high temperature SiC CMOS logic is underway, with full logic having already been implemented beyond 400°C [10]. However, a poor channel mobility at the SiO_2/SiC interface leads to very high channel resistances, such that below 300°C, silicon is still preferable for low to medium voltage applications (<600 V) [5]. SiC is,

however, a natural candidate to supersede Si in high power devices due to its high breakdown field, which is ten times that of Si [11].

3. Silicon-on-Silicon Carbide (Si/SiC) Power Electronics

A new materials system has been proposed [1] that is able to combine the benefits of SOI technology (device confinement, low resistance channel) with that of SiC (high thermal conductivity, strength, radiation hardness). The Si-on-SiC (Si/SiC) device structure is shown in Figure 3, a laterally diffused power MOSFET (LDMOS) rated up to 600 V, implemented within a thin Si film less than 1.5 μm thick. The thin film is transferred via a wafer bonding technique directly onto the surface of a high resistivity, semi-insulating 6H-SiC substrate without an interfacial oxide. 6H is the SiC polytype with the highest thermal conductivity, so efficiently sinking the heat generated by the device. Retaining the SOI-like Si layer means that, compared to SiC bulk devices, the Si/SiC transistor will have minimal channel resistance, allowing the device to operate at voltages below 600 V unlike SiC. Combining the

Figure 3: Top, the Si/SiC material system that has been developed. Bottom, the proposed Si/SiC LD-MOS transistor.

channel resistance, allowing the device to operate at voltages below 600 V unlike SiC. Combining the benefits of both materials means that the proposed Si/SiC devices have the potential to deliver efficient device performance in the application space indicated in Figure 2 – 50 to 600V and 100 to 300°C. Several harsh environment applications, such as downhole motor drives and automotive or solar inverters stand to benefit from devices operating in this range.

Previous studies on Si/SiC electronics have concentrated on demonstrating MOSFET behaviour [12, 13] and the implementation of RF devices [14, 15]. Both showed that the effects of self-heating on the forward characteristics can be suppressed, unlike equivalent SOI devices power devices. These studies have shown experimentally [13] that the channel mobility of a Si/SiC MOSFET at 300°C and hence its channel resistance was just 10% worse than it was at room temperature, compared to an 83% reduction for an equivalent Si bulk device. Experimental results from RF devices implemented in a complicated Si/poly-Si/poly-SiC substrate [15], show that the negative-resistance effect of self-heating (whereby device resistance increases with voltage due to a rise in internal temperature) is minimised in the Si/SiC device, unlike an equivalent SOI device. However, breakdown voltage, leakage current and maximum oscillation frequency were all shown to worsen. Other groups have considered SOI where the BOX and Si top layer is transferred onto a SiC substrate [16, 17]. However, this is a methodology that our own modelling [1] proves to only fractionally reduce the self-heating problems of conventional SOI.

3.1 Thermal Simulations of Si/SiC

Thermal simulations [1] of Si-on-SiC substrates were performed and compared to Si, SiC and SOI substrates using finite element modelling package Silvaco. In each layer, a generic power device is represented as a heat source with a given power density, located at the top and centre of each substrate. The maximum steady state temperature in each substrate is modelled given the materials properties of each material stack. Figure 4 shows the results and unsurprisingly, SiC with its high thermal conductivity, is best able to dissipate generated heat. The Si/SiC stack is very
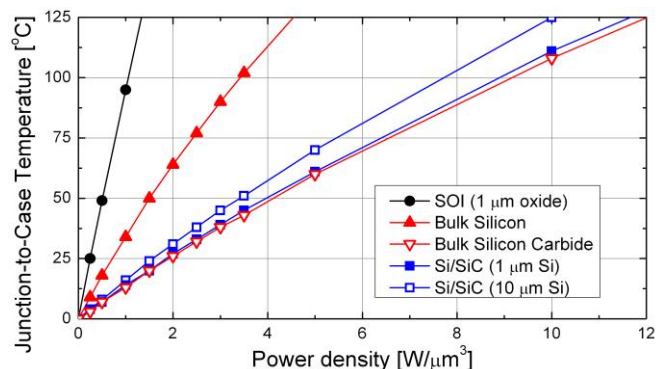
Figure 4: Thermal simulations using finite element modelling [1] showing the self-heating credentials of the proposed Si/SiC devices compared to SOI, Si and SiC

close to this performance however, with a silicon layer 1 μm thick able to dissipate 97% of the power that SiC can for the same temperature rise. These substrates dissipate around 4 times the power density than SOI for a given temperature rise, while for the same power throughput, the temperature rise in the Si/SiC is approximately seven times less than in an SOI substrate and 2.5 times less than bulk Si. This gives a generic Si/SiC device three alternative benefits, when compared to the equivalent in Si or SOI, where it can operate either:

- in exactly the same ambient temperature, dissipating the same power, but with improved performance due to a reduction in the effects of self-heating;
- at a much higher ambient temperature for the same performance;
- or at the same ambient temperature but at much higher power for the same performance.

3.2 Electrical Simulations of Si/SiC MOSFETs

High voltage devices implemented in a Si/SiC layer benefit from many of the same advantages as SOI. Compared to vertical bulk MOSFET or IGBT designs, these advantages include [18] the suppression of off-state leakage current at high temperature due to the confinement offered by the buried oxide (BOX). The BOX allows the isolation of multiple power devices, or of a power device from CMOS, making possible the integration of half bridges or fast body diodes in a single chip without the risk of latch up. Furthermore, the lateral implementation offers low switching losses compared to bulk devices.

The lateral power MOSFET design of Figure 3, was originally based upon on a Philips 600 V SOI device [19] with low on-state resistance, though significant optimisation was required for the Si/SiC device to block the same voltage in the most efficient manner. We therefore use a model of this LD-MOS SOI device simulated in Silvaco as the benchmark to compare the electrical performance of the Si/SiC device to, and from the information given in [19], the characteristic device performance was reproduced, with the DC characteristics shown in Figure 5.
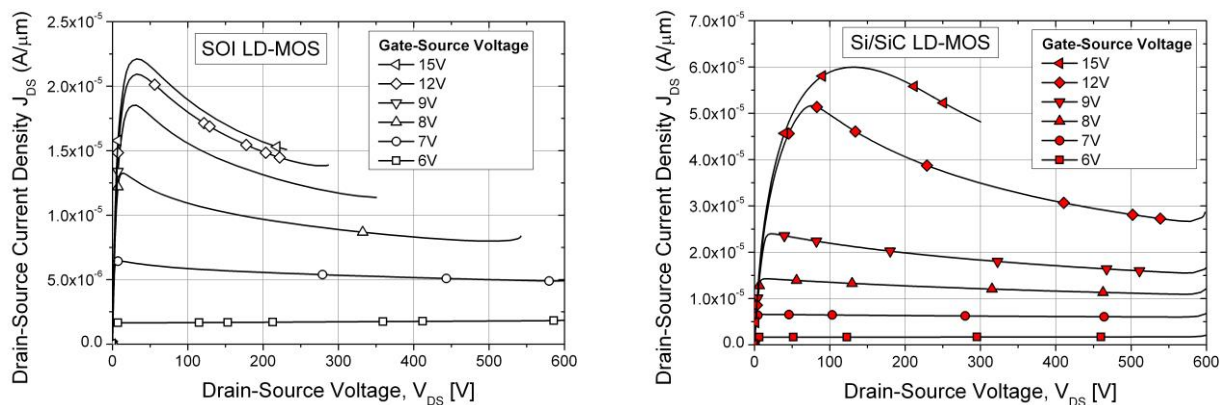

Figure 5: Simulated on-state characteristics of a SOI and Si/SiC LD-MOS operated at room temperature.

Simulation results showed little difference in the off-state characteristics (not shown) of the two devices, with low leakage values for both prior to 600 V breakdown. Leakage currents of ~1 pA/μm at room temperature and 100 nA/μm at 300°C were recorded prior to breakdown for both devices. Figure 5 shows similar on-state characteristics in each device. Both display evidence of self-heating effects, with the saturation regions showing 'negative resistance', where the decreases with voltage due to internal heating. To directly compare the effects of self-heating, in Figure 6 the data at V_{GS}=9 V has been normalised (using isothermal data) and the local temperature monitored (in the non-isothermal simulation). This shows that the SOI transistor wastes twice the amount of power than the Si/SiC device due to a three times rise in the internal temperature. At 200 V the SOI device wastes 20% of the total power resulting in an internal temperature rise of over 100°C. The Si/SiC wastes 10% resulting in a 30°C temperature rise.

These same devices were used in the extraction of dynamic, switching characteristics. These are shown in Figure 7, where they were used to drive a 50 Ω resistive load, switching just 50 V at 10 kHz. While negligible difference was observed in the rise and fall times, the Figure shows that even at such a low power, the conduction losses in the SOI transistor were substantial delivering around 90% of the current delivered by the Si/SiC device and resulting in a 30°C temperature rise (compared to 5°C).

3. Summary

A new generation of lateral power devices are introduced, implemented on a novel Si-on-SiC substrate. Thermal simulation results suggest that the thermal performance of the substrates are almost the equivalent of bulk SiC, allowing power devices to be implemented that have a higher power density and/or a higher operating temperature than conventional bulk Si or SOI devices. The Si/SiC technology brings the high temperature performance of SiC to low voltage devices, the very low resistance Si channel allowing power device implementation ion the region of 50 to 600 V. Simulation of LD-MOS transistors show that the new proposed Si/SiC device can better handle self-heating, wasting significantly less power than SOI devices in every indicator. It retains the ability of SOI to minimise leakage at high temperature, but does so wasting 50% less power.
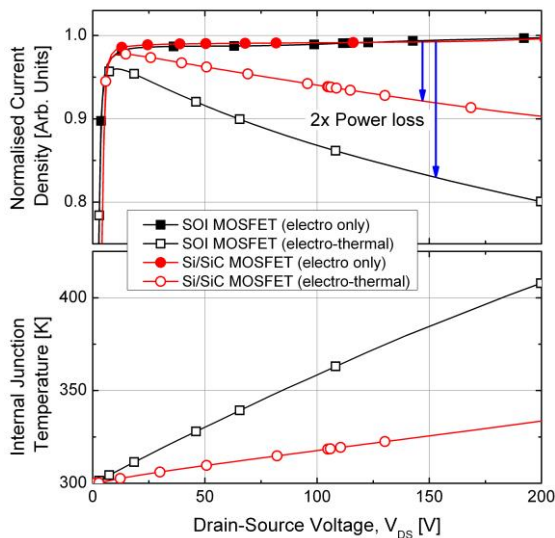
Figure 6: [Top] A comparison of the SOI and Si/SiC responses in which isothermal responses have been normalised (solid shapes). The non-isothermal model shows that the losses in the Si/SiC device are just 10% at 200 V compared to 20% in the SOI device. [Bottom] The internal junction temperature at the same voltage.
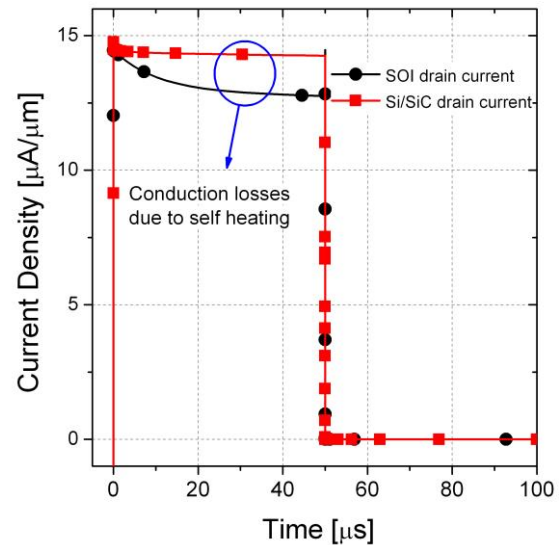
Figure 7: The dynamic response of a SOI and Si/SiC device to a resistive load. A marked difference in conduction losses can be noted reducing delivered power and increasing internal temperature.

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