Dislocation loops as a mechanism for thermoelectric power factor enhancement in silicon nano-layers

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A more than 70% enhancement in the thermoelectric power factor of single-crystal silicon is demonstrated in silicon nano-films, a consequence of the introduction of networks of dislocation loops and extended crystallographic defects. Despite these defects causing reductions in electrical conductivity, carrier concentration, and carrier mobility, large corresponding increases in the Seebeck coefficient and reductions in thermal conductivity lead to a significant net enhancement in thermoelectric performance. Crystal damage is deliberately introduced in a sub-surface nano-layer within a silicon substrate, demonstrating the possibility to tune the thermoelectric properties at the nano-scale within such wafers in a repeatable, large-scale, and cost-effective way. *Published by AIP Publishing.*
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The recent global drive to be more efficient in the way we use energy, particularly to reduce the amount of energy that goes to waste, has led to renewed interest in thermoelectrics (TE) for waste heat harvesting. In particular demand are materials that use elements that are less costly, less toxic, and more Earth-abundant than the popular TE material bismuth telluride (Bi_2Te_3). Despite requiring the scarce element tellurium, Bi_2Te_3 has significantly better thermoelectric performance than more abundant elemental semiconductors, such as silicon (Si). Three material properties determine this performance—thermal conductivity (κ), Seebeck coefficient (S), and electrical conductivity (σ). These interlinked properties are commonly combined to describe performance in terms of the thermoelectric figure-of-merit (Z), where $Z = S^2\sigma/\kappa$. Bi_2Te_3 has approximately 100-fold better Z than bulk Si,[1] but is approximately 30-times more expensive.[2] Therefore, developing methods that provide significant gains in the Z of Si offers a potential route to more cost-effective and environmentally friendly thermoelectric devices.

Since highly doped Si (doping $\sim 10^{19}\,cm^{-3}$) possesses S and σ competitive with other TE materials, much recent focus has been on reducing its thermal conductivity, which is too high for most practical applications. It has been demonstrated possible via nano-structuring, to vastly reduce κ with little or no degradation of other parameters in structures such as Si nanowires, nanofilms or films containing porosity, periodic voids or vacancies.[3–13] This allows for higher Z and makes nano-structured Si an attractive TE material. Such findings, with variations, have been corroborated by numerous groups worldwide, through both theoretical and experimental studies.[3–13]

Due to this drastic reduction in κ, which is quickly reaching the amorphous limit, further improvements might come from the thermoelectric power factor ($PF = S^2\sigma$), for which to date limited progress has been made. However, a small set of recent studies have demonstrated that a significant improvement in the PF of Si is sometimes possible for polycrystalline Si[14–16] where built-in potential barriers are created by nano-scale grain boundaries or voids,[17] combined with high levels of doping. These potential barriers increase energy filtering and as a consequence, the Si Seebeck coefficient. Our previous work demonstrated that a Seebeck coefficient improvement is also realizable in single-crystal Si nanowires by the introduction of dislocation loops, which also create potential barriers and produce a similar effect.[18] This was so far only demonstrated in n-type material and for relatively lowly-doped Si, where the PF is far too low for practical applications.

In this article, we report that a significant enhancement in the power factor is also possible for p-type bulk material, and more importantly, with high doping concentrations. Improvements in the PF by $\sim$70% compared to control samples (bulk Si) are realized, giving $PF = 6.6\,mW\,m^{-1}\,K^{-2}$ at 300 K—significantly higher than that of traditional Bi_2Te_3 materials used in current commercial devices.

Four different sample types were fashioned from prime $\langle 100 \rangle$ single-crystal Si wafers (n-type, 5–10 Ω cm). Ion-implantation of ^{28}Si ions was carried out on a Varian VIISta ion implanter at beam energy 2 MeV. Two wafers received a fluence of $2 \times 10^{15}\,ions\,cm^{-2}$ and two others received $6 \times 10^{15}\,ions\,cm^{-2}$. Wafers received thermal annealing in nitrogen in a furnace at 900 °C for a time of either 20 or 60 min, before being diced into squares. Along with a non-implanted control wafer, samples were then thinned by etching in 25% KOH solution at 60 °C, to precisely remove the top 1.5 μm of the wafer. Spin-on dopant (boron) was deposited on each sample before heating for 10 min at 900 °C in nitrogen to drive-in the dopant, creating a p-type region with a p/n junction immediately beneath it, isolating the p-type defect-rich nano-layer from the n-type substrate. A dip in HF

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was applied to remove surface boron-silicate glass. The B doping profile was confirmed as being the same in all samples by differential Hall profiling,[19] with a relatively flat doping peak. This confirmed the junction depth as being ~800 nm, to coincide with the bottom of the defective layer and that the thickness of pristine Si remaining at the top of the film was only ~30 to 45 nm. Fig. 1 provides a schematic illustration of the steps used for sample fabrication.

Each sample underwent characterization. The presence and nature of defects in the nano-layers were characterized by cross-sectional transmission electron microscopy (XTEM). Micrographs of each of the samples created are presented in Fig. 2. Fig. 2(a) shows the location of the buried layer relative to the original wafer surface. The remaining micrographs show the defects created with each of the four implant/annealing conditions. All micrographs show clear evidence of dislocation loops and implantation extended defects, with the higher implant dose creating a higher density of defects. Samples were sent to a commercial vendor for through-plane thermal conductivity measurements. These were extracted by a thermo-reflectance method. Electrical conductivity,

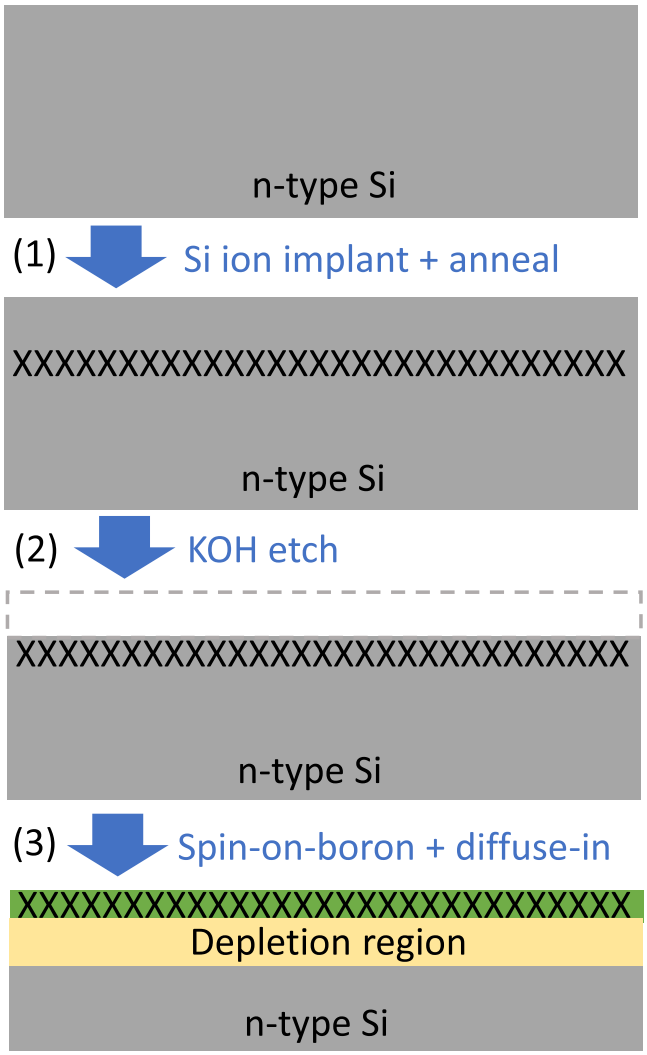

FIG. 1. Schematic diagram showing the sample fabrication steps. The Si wafers underwent Si ion-implantation and annealing to create a sub-surface nano-layer rich in defects (represented by Xs). Following removal of the wafer surface by KOH etching, the nano-layer was doped p-type, creating a p/n junction and isolating it from the n-type substrate.

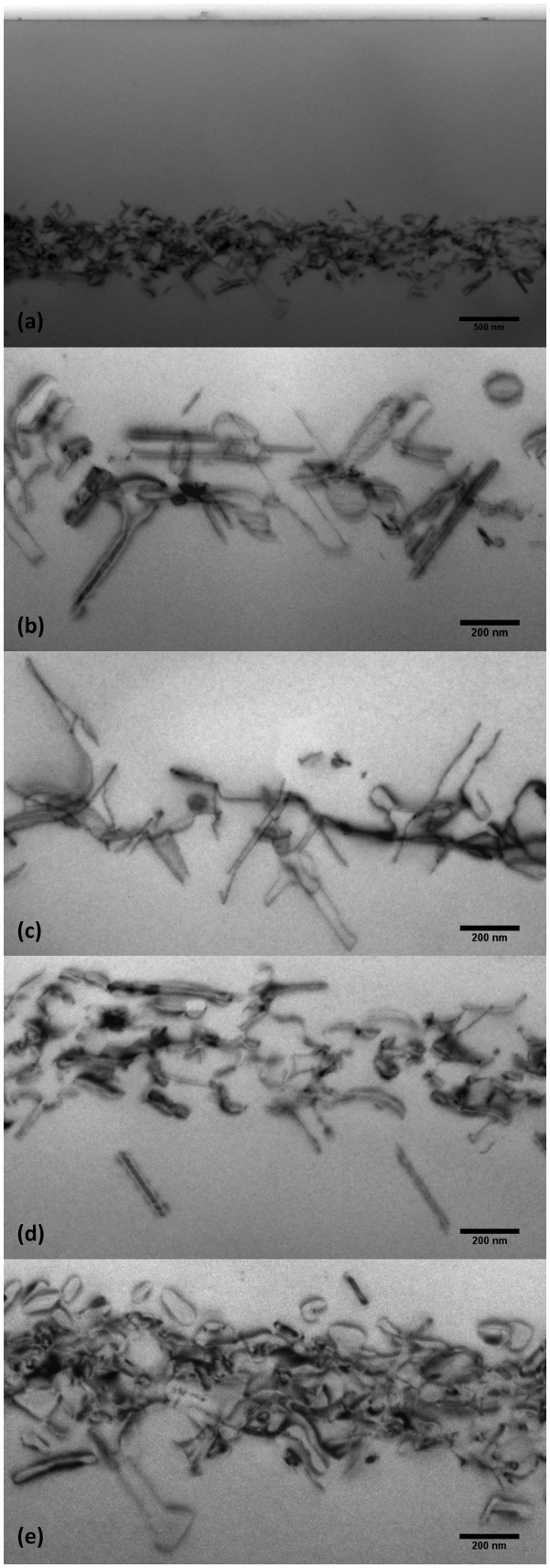

FIG. 2. Micrographs showing sub-surface defect-rich regions created in the Si wafers. (a) The layer location relative to the wafer surface (scale bar is 500 nm). (b) Defects created with 2×10^{15} cm^{-2} implant, 900 °C, 20 min annealing. (c) Defects created with 2×10^{15} cm^{-2} implant, 900 °C, 60 min annealing. (d) Defects created with 6×10^{15} cm^{-2} implant, 900 °C, 20 min annealing. (e) Defects created with 6×10^{15} cm^{-2} implant, 900 °C, 60 min annealing. (Scale bars in (b)–(e) are 200 nm).

Hall-effect, and differential Hall measurements were made in air in the van der Pauw geometry, using a Biorad HL5900 tool. Temperature-dependent electrical conductivity and Seebeck measurements were made in-plane on a Linseis LSR-3 instrument in He ambient at 10^4 Pa.

Fig. 3 shows the variation with implant/annealing conditions for through-plane thermal conductivity at 300 K. κ was 132.6 $W\,m^{-1}\,K^{-1}$ for the defect-free control sample and was found to decrease significantly as a result of the implantation-induced damage. κ fell to a value of 70.4 $W\,m^{-1}\,K^{-1}$ for the lower implantation fluence with 20 min annealing, but recovered slightly to 76.6 $W\,m^{-1}\,K^{-1}$ following annealing for 60 min. This was an expected result since it is both intuitive and well-established that the introduction of defects within a "perfect" crystal lattice reduces its thermal transport, and that with longer annealing, more damage will be removed and recovery of thermal transport will occur. For the larger fluence, κ was reduced more to 43.2 $W\,m^{-1}\,K^{-1}$ for 20 min annealing and to 48.9 $W\,m^{-1}\,K^{-1}$ with 60 min annealing.

Fig. 4 shows the change in σ in each sample as a function of the conditions used to create defects. Results are displayed for measurements made at 300, 350, and 400 K, although differences as a result of temperature were modest in these samples, with only a small conductivity decrease seen in each sample as the measurement temperature is raised. More obvious was the change in conductivity as the implant/annealing conditions were changed. Clearly, the control sample had the highest σ of 415 S cm^{-1}. For the lower of the implant fluences, conductivity was reduced relative to the control, and for the higher fluence, conductivity was reduced to less than half. For each fluence, it was the sample that received the shortest anneal that had the lowest conductivity. These trends are intuitive and it is unsurprising that trends in electrical conductivity match those in thermal conductivity (Fig. 3). These trends are similar in magnitude, i.e., as thermal conductivity is reduced

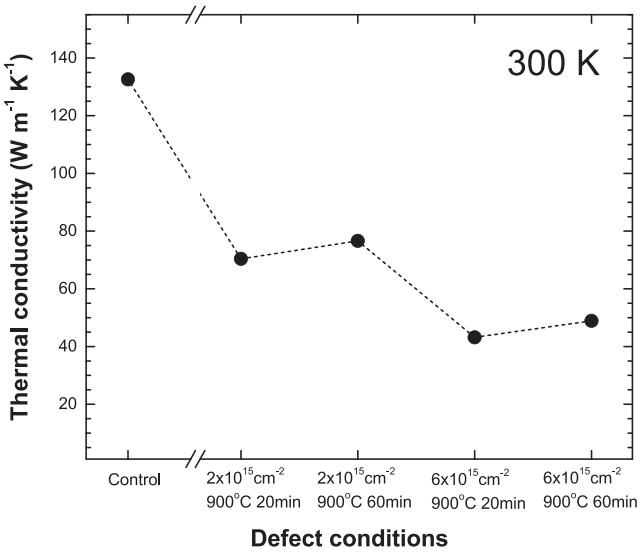

FIG. 3. Thermal conductivity (through-plane) as a function of implant/annealing conditions for a control sample relative to samples with 2 MeV Si implant with (i) 2×10^{15} cm^{-2} fluence, 900 °C, 20 min annealing, (ii) 2×10^{15} cm^{-2} fluence, 900 °C, 60 min annealing, (iii) 6×10^{15} cm^{-2} fluence, 900 °C, 20 min annealing, and (iv) 6×10^{15} cm^{-2} fluence, 900 °C, 60 min annealing. Measurements were made at 300 K.

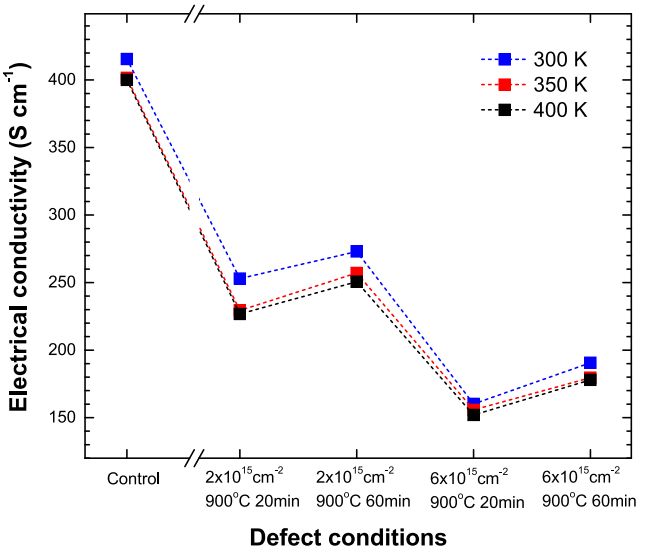

FIG. 4. Electrical conductivity (in-plane) as a function of ion-implantation condition and annealing time, for three measurement temperatures (300 K–400 K).

for a given condition, so is the electrical conductivity by a similar extent, suggesting little net gain in electrical/thermal transport behavior results from the introduction of dislocations, each quantity being reduced by a factor of ~3. It is worth mentioning that XTEM images—particularly Figs. 2(d) and 2(e)—are perhaps deceiving, as one might expect the electrical/thermal conductivity to be lower for the sample in Fig. 2(e) where defects are more apparent. This is opposite to what is measured. In reality, samples having received shorter anneals contain the most defects and lower electrical/thermal conductivity, yet these defects are in the form of smaller Si-interstitial clusters, not visible in the XTEM at its current resolution.

Fig. 5 gives further detail of the room-temperature σ by way of Hall measurement data. Carrier concentration and Hall mobility at 300 K are presented. They show that defect-mediated decreases in σ are a result of a fall in both Hall mobility and carrier concentration, though the former drop is more significant. Crystallographic defects are well known to

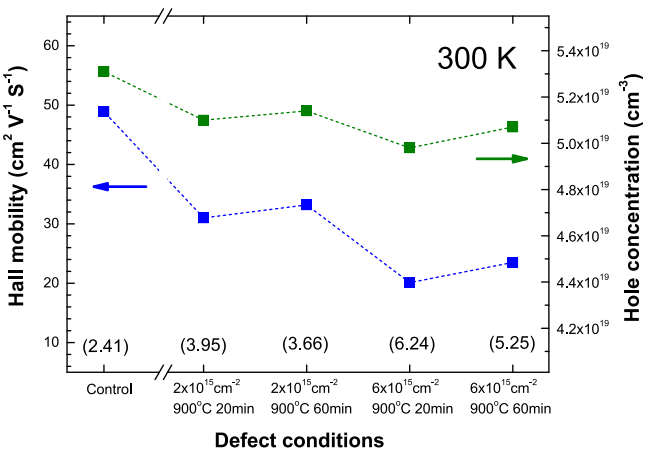

FIG. 5. Hall mobility (left axis) and hole concentration (right) as a function of defect conditions. Measurements were made at 300 K. Values in parentheses are corresponding resistivity values in mΩ cm.

degrade carrier mobility in Si and this clearly occurs in current samples. B dopant activation is highest in the control sample following drive-in, whereas defects reduce the carrier concentration by up to 10%. Since B is well-known to cluster with self-interstitials it is likely that their presence during the drive-in phase means a proportion of the dopants are trapped in inactive clusters rather than finding substitutional sites. B activation improves slightly after longer-duration annealing.

In-plane Seebeck coefficient measurements were carried out for each of the samples. Results are displayed for measurements made at 300, 350, and 400 K, although as for σ, temperature-dependent differences are modest, with only a small S increase seen in each sample as the measurement temperature is raised. In this case, S was lowest in the control sample (Fig. 6(a)), though this was expected since the sample had the highest electrical conductivity and the two parameters are interrelated, with one usually increasing at the expense of the other. Combining the two in the form of the power factor gives an indication of the net thermoelectric performance, with $PF = 3.8\,\mathrm{mW\,m^{-1}\,K^{-2}}$ at 300 K for the control sample (Fig. 6(b)). This PF value is in line with the highest value

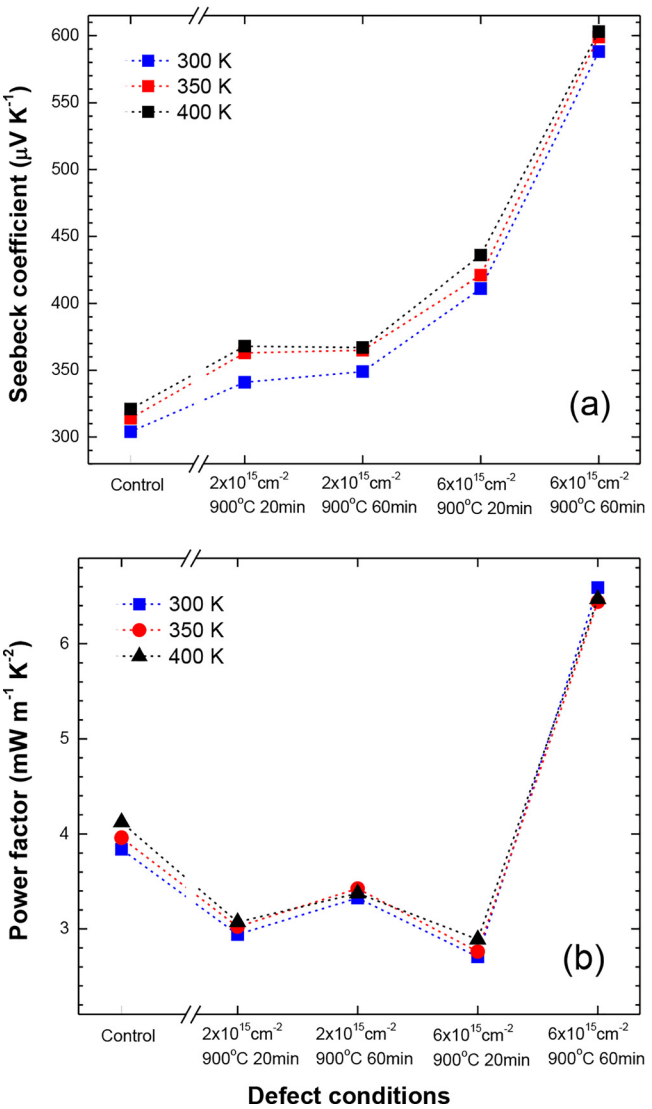

FIG. 6. (a) Seebeck coefficient (in-plane) and (b) power factor as a function of defect conditions for three measurement temperatures (300 K–400 K).

pristine Si can provide under optimal doping conditions. All other samples, with lower electrical conductivity, have a higher Seebeck coefficient. The two samples receiving the lower implant dose ($2 \times 10^{15}\,\mathrm{cm^{-2}}$) have modestly higher S that, when combined with σ, result in a significantly lower thermoelectric PF than the control sample. For the higher implant fluence ($6 \times 10^{15}\,\mathrm{cm^{-2}}$) with 20 min annealing the PF is worse still, since the relatively small rise in S is more than negated by the much larger drop in σ. An interesting result occurs, however, when the higher fluence sample is annealed for longer, resulting in the formation of a dense network of mostly dislocation-loops with diameters roughly between 100 nm and 200 nm (Fig. 2(e)). In this case, the increase in S is much greater than for all other samples and bucks the trend, since given its higher electrical conductivity than the previously mentioned sample, one would expect its Seebeck coefficient to decrease. In fact, as the reader can see, not only is the opposite true but also the increase in S is significant. This has a striking effect on the power factor, which is now on average 70% higher than that of the control sample, with $PF = 6.6\,\mathrm{mW\,m^{-1}\,K^{-2}}$ at 300 K.

The simultaneous increase in σ and S is rare, but significant, and results in improved power factors. It is similar to that observed in Ref. 14 for heavily B-doped nano-crystalline Si, again under high-temperature annealing. While the underlying reasons behind this are still under investigation, it is possible that a number of contributing factors coexist and act synergistically in order to achieve a simultaneous S and σ improvement. For the former, it is probable that potential barriers for holes are created at the dislocation sites, which improve energy filtering and consequently S. Indeed, when present within the crystal lattice, dislocation loops are known to exert a significant pressure by pushing-apart nearby Si atoms—this pressure increasing the band-gap local to the dislocation site.[20] For the first annealing condition, this local band-gap increase could be responsible for the reduction in conductivity and mobility. As well as allowing loops to form, longer annealing would heal the majority of the Si volume, and thus a slight increase in the electrical conductivity is observed, compensating for any further reduction from the increasing potential barriers. The increased pressure may also improve carrier mobility, a well-known consequence of applying stress in Si.[21] In addition, any local thermal conductivity differences between pristine Si regions and the dislocations might improve S as well. This is because the overall Seebeck coefficient is determined by the weighted average of S in the two regions, with the weighting factor being the temperature drop in each region, determined by their thermal conductivities.[14,22] Thus, as the crystal lattice is healed, especially in the last annealing step, and local thermal conductivity increases, the local Seebeck coefficient in the dislocation regions (which is expected to be high compared to bulk Si) becomes more important and could warrant the large increase in the overall S observed in Fig. 6(a). Earlier calculations on the effect of filtering by barriers in p-type Si, indicate that filtering alone could provide ~30 to 40% PF improvements,[22,23] whereas the rest of the measured improvements could originate from the various other factors identified, such as local variations in thermal conductivity and carrier mobility.

We have reported a significant enhancement in the power factor of single-crystal Si is possible for highly doped p-type material, specifically an improvement of ~70% compared to control samples (bulk Si), giving $PF = 6.6\,\mathrm{mW\,m^{-1}\,K^{-2}}$ at 300 K. This is higher than that of traditional Bi_2Te_3 materials used in commercial thermoelectric devices[24] and is a consequence of the introduction of a dense network of dislocation loops with diameter between 100 nm and 200 nm. Despite these defects causing reductions in electrical conductivity, carrier concentration, and carrier mobility, large corresponding increases in Seebeck coefficient and reductions in thermal conductivity lead to a significant net enhancement in thermoelectric performance. This finding provides a route to significant gains in the thermoelectric power factor of Si, a material that potentially offers a path to more cost-effective and environmentally friendly thermoelectric devices.

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