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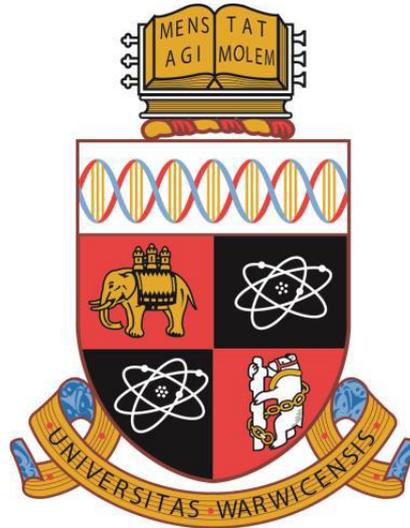
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Strain relaxation study of $\text{Si}_{1-x}\text{Ge}_x$ & Ge
buffer layers on Si(001) and InSb on
Ge/Si(001) virtual substrates

by

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Thesis

Submitted to the University of Warwick
in partial fulfilment of the requirements
for admission to the degree of
Doctor of Philosophy

Department of Physics

THE UNIVERSITY OF
WARWICK

Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. All experimental data presented was carried out by the author, or (where stated) by specialists under the author's direction.

Abstract

Due to their direct and tuneable bandgap, III-V semiconductors offer variations in electrical properties, compared to silicon. However wafers of III-V materials are more expensive to manufacture and have higher defect densities than Si(001). Epitaxially depositing high quality thin films of III-V materials onto Si(001) substrates offers a more cost effective route to manufacturing state of the art III-V electronic devices, whilst mitigating defect generation through lattice and thermal expansion coefficient mismatches.

In this study, pure Ge and $\text{Si}_{1-x}\text{Ge}_x$ layers are deposited as thin film heterostructures on on-axis and 6° off-axis Si(001) substrates using reduced pressure chemical vapour deposition to act as strain tuned “buffer layers” to integrate a particular III-V compound onto the substrate. The films are characterised using transmission electron microscopy (TEM), atomic force microscopy (AFM), high resolution X-ray diffraction (HR-XRD) and defect etching & differential interference contrast (DIC) optical microscopy.

The first key finding in this study relates to the development of an 78nm Ge buffer which is comprised of a LT seed layer followed by controlled annealing only and at a fraction of the tensile strain of state of the art thick LT/HT Ge buffer layers. The second key finding comes from the comparisons between the established linear $\text{Si}_{1-x}\text{Ge}_x$ grading (LG) process with the recently developed reverse linear $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ grading (RLG) process. Continuous tensile strain relaxation in RLG even up to $x=0.45$ yields high quality buffer layers with $\leq 3.7\text{nm}$ roughness, $\times 10^7\text{cm}^{-2}$ TDD and consistently delivering 0.2% tensile strain albeit with a rise in stacking faults past 70% Ge.

The third major discovery comes when omitting the reverse graded layer entirely in the RLG structure and depositing a constant composition $\text{Si}_{1-x}\text{Ge}_x$ step on the Ge buffer layer. High misfit dislocation densities and surface roughening is observed leading to the formation of Kirkendall voids in the Ge underlayer as a strain relieving mechanism.

The final chapter of this study investigates solid source molecular beam epitaxy growth of high quality indium antimonide which has the highest lattice mismatch of any III-V compound to Si(001) at 19.3% using the highest quality pure Ge buffer layers on 6° off-axis Si(001). HR-XRD reciprocal space maps shows identical levels of strain in Ge buffer layers grown on on-axis and 6° off-axis substrates, however an increased degree of tilt is measured in the off-axis Ge buffer layer, with reduced degree of tilt in the InSb layer.

Publications and conference presentations

Refereed Publications

- 1) V. Sivadasan, M. Myronov, S.D. Rhead, V.A. Shah, D.R. Leadley, “*Comparison of $Si_{1-x}Ge_x$ relaxed buffer layers grown on Si(001) substrate by linear grading and reverse linear grading approaches*” (in preparation for submission 2016)
- 2) V. Sivadasan, M. Myronov, S.D. Rhead, “*Ultra-thin Ge buffer layers on Si(001)*” (in preparation for submission 2016)
- 3) V. Sivadasan, M. Myronov, S.D. Rhead, “*Kirkendall void formation in reverse step graded $Si_{1-x}Ge_x/Ge$ buffer layers on Si(001)*” (in preparation for submission 2016)
- 4) V. Sivadasan, M. Myronov, S.D. Rhead, J.E. Halpin, D.R. Leadley, “*Tilt comparison in reverse terrace graded and reverse linearly graded $Si_{1-x}Ge_x/Ge/Si(001)$ virtual substrates*” (in preparation for submission 2016)
- 5) V. Sivadasan, M. Ashwin, G. Colston, S.D. Rhead, M. Myronov, “*High quality InSb epilayers grown on AlSb/Ge/Si(001) virtual substrates for photonic and electronic devices*” (in preparation for submission 2016)

Conference Presentations

V. Sivadasan, **M. Myronov (presenter)**, S.D. Rhead, V.A. Shah, D.R. Leadley, “Comparison of SiGe relaxed buffer layers grown on Si(001) substrate by forward and reverse Ge grading approaches” EMRS 2014 Spring Meeting, Lille, France, May 26-30, 2014.

V. Sivadasan (presenter), M. Myronov, S.D. Rhead, J.E. Halpin, D.R. Leadley “Reverse terrace graded $Si_{1-x}Ge_x/Ge/Si(001)$ virtual substrates grown using RP-CVD on on-axis and 6° off-axis substrates for future developments in III-V materials integration” EUROSOI-ULIS 2015, Bologna Italy, 26 -28 January 2015.

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Acknowledgments

I would like to thank my supervisor Dr Maksym Myronov for growing the wafers that I characterised for this project and his guidance. I would also to thank my second supervisor, Prof David Leadley for his support.

I would also like to thank Dr John Halpin for teaching me TEM sample preparation, Dr Vishal Shah for his advice and counsel on SiGe virtual substrates and Dr Stephen Rhead on teaching me about HR-XRD. I'd also like to say thank you to Dr Phillip Allred who was always at hand to help me when I was learning AFM and TEM techniques. Dr Alan Burton, the nano-silicon technician, who helped me with all of my physical chemistry queries. A special thank you to Gerard Colston for his assistance on the InSb study and to Dr Mark Ashwin for growing the InSb films on the Ge buffer layers. I would like to say a very big thank you to Steve York and Steve Hindemarsch, who helped me with TEM when I was having difficulty with the instruments. To Dr Richard Beanland, the greatest microscopist that I know, who has taught me so much about TEM throughout my PhD. I would also like to say a very special thank you to Ali Mostaed and Dr Alex Marsden for helping me with HR-TEM, and generally when I was stuck on something related to microscopy. I would also like to thank Dr Neil Wilson, Dawn wood and Mark Skilbeck for helping me with AFM when I was in difficulty. A special thank you to Dr David Woodward from whom I learned a great deal about X-ray diffractometry from his MPAGS course. A special thanks to Dr David Walker for giving me access to the diffractometer.

I would also like to say a big thank you to Dr Stephen Powell, Dr Gregory Jasion and Dr Trung Nam Tran for their help and support whilst I was an undergraduate engineering student at Southampton university. I would like to say a very special thank you to Dr Ahmed Al-Makky for helping me understand concepts in computational fluid dynamics as a Warwick master's student in engineering.

Finally, I dedicate this thesis to my family without whom I could not have persevered over the last four years. I would like to say a special thank you to my Valliachan who tutored me in mathematics from a young age. To my sister for her support and words of encouragement. My father, the greatest and most dedicated engineer that I know

and who has inspired me to work hard every day. Finally, to my mother whose compassion, support and understanding has taught me the importance of science and its role in the betterment of society.

1. Introduction

1.1. Silicon electronics and the semiconductor industry.

The low raw material & production costs, abundance and low impurity densities account for silicon's 70 year dominance in the electronics industry. The first point contact transistor was constructed using Germanium at Bell labs in 1947, by Brattain, Bardeen and Shockley, however manufacturing quickly transitioned over to silicon as the cheaper group IV semiconductor material of choice [1]. Through subsequent years of research and development into the fundamental properties of silicon and manufacturing processes, high purity single crystal wafers were manufactured which led to the invention of the integrated circuit, solid state memory and the microprocessor, all of which have revolutionized modern technology and created an industry worth \$336 billion in 2014 [2].

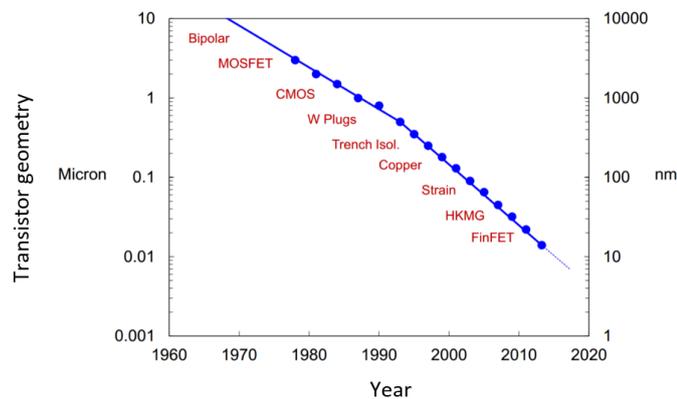


Figure 1.1 Plot showing reduction in transistor size over the last 5 decades. A slightly steeper gradient is seen beyond 1990 with processing technologies such as strain inducement and quasi planar FinFET architecture facilitating ever increasing ULSI [3]

Figure 1.1 shows Moore's law for the evolution of metal oxide semiconductor field effect transistor (MOSFET) scaling on a silicon chip over the last 50 years. Device scaling is imperative to reducing total CMOS power consumption as well as reducing the cost per transistor [4]. With control of threshold voltage (V_t) variations, fully depleted MOSFETs on ultra-thin buried oxide substrates (SOI) currently yield processing technology at 14nm, which will move onto 10nm by 2017 [5]. However due to excessive leakage currents, mobility degradation and issues with processing at such a small scale [6], processing technology at 7nm and lower requires other

materials such as silicon germanium [7]. Using III-V semiconductors such as InGaAs for channel material to take advantage of the much higher than silicon intrinsic unstrained electron and hole mobility, whilst maintaining the existing geometries, is inevitable [3].

Other than CMOS, silicon's low cost has meant it holds dominance in other sectors of the electronics industry as well, such as photovoltaics (PV). Silicon module production is at \$1.50 per peak watt [8] and the current record lab cell efficiency for monocrystalline silicon is 25.6% and 20.8% for polycrystalline silicon [9]. In 2015 Silicon wafer based PV technology accounted for 92% of total production with polycrystalline silicon holding 56%. China and Taiwan currently holding 69% of the total PV production industry due to reduced manufacturing and production costs. Silicon PV is expected to be worth \$345.59 billion by 2020.

1.2. Motivation behind developing $\text{Si}_{1-x}\text{Ge}_x$ and Ge buffer layers on Si(001)

1.2.1. III-V materials integration onto Si(001)

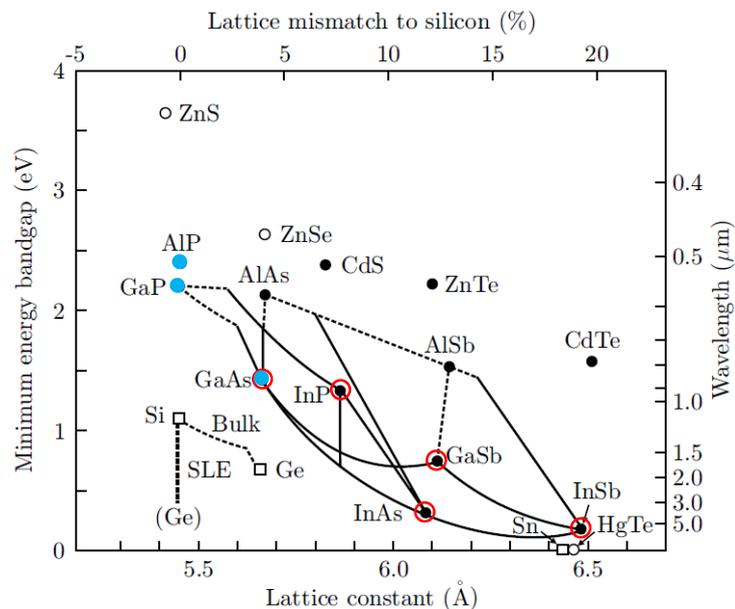


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Figure 1.2 shows lattice constants of various semiconductors against bandgaps on the left, absorption wavelength on the right and the lattice mismatch of the semiconductor to Si(001) at the top. Ternary compounds are those which have a combination of two group III elements or two group V elements such as: $Ga_{1-x}In_xAs$ and quaternary compounds have both two group III and two group V elements: $Ga_{1-x}In_xAs_{1-y}Sb_y$. Ternary and quaternary III-V semiconductors will not be discussed in this thesis, but suffice to say the aim of alloying is to change the bandstructure.

1.2.1.1. III-V photovoltaics.

The maximum efficiency of a single p-n junction cell is governed by the Shockley-Queisser limit which is approximately 33% in the laboratory [11]. The efficiency of the module is increased by connecting cells of different bandgaps in series, with each cell generating an equal current. The highest efficiency solar cells are III-V multiple junction concentrator cells, as shown in figure 1.3. Currently the highest efficiency four junction cell is at 45% [12]. Ge has a maximum absorption wavelength of $1.85\mu m$ and has consistently been used as the bottom contact cell at 41% total efficiency in both metamorphic [13], and lattice matched cell structures of $Ga_{0.35}In_{0.65}P$ (1.67 eV)/ $Ga_{0.83}In_{0.17}As$ (1.18 eV)/Ge (0.66 eV)[14]. When considering cells with 5 or even 6 junctions and efficiencies of 58%, Ge will most likely continue to serve as the bottom narrow bandgap cell [13]. Ge substrates are expensive and brittle however.

Alternatively, the narrow bandgap in InSb makes the material suitable for near field thermophotovoltaic and thermoelectric devices operating between $326^\circ C$ and $926^\circ C$ [15]

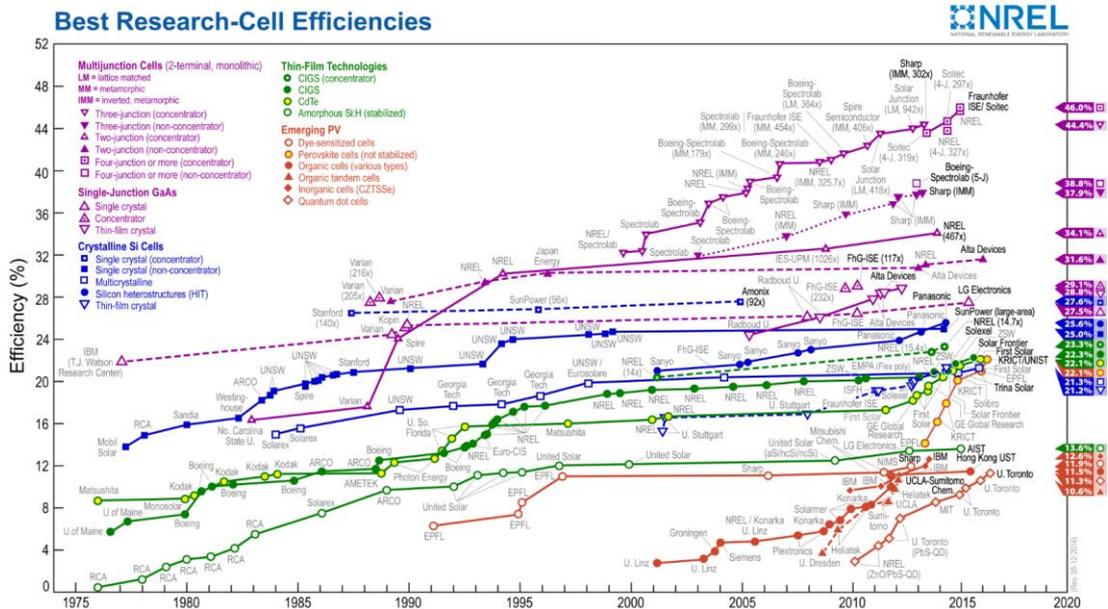


Figure 1.3: National renewable energy laboratory chart showing PV modules on time scale (x-axis) against modules efficiency (y-axis) [16].

1.2.1.2. III-V Optoelectronics and photonics.

GaAs has been used in silicon CMOS circuitry for over 30 years. In work carried out by Goosen et al in 1995 GaAs-AlGaAs multiple quantum well modulators were integrated into silicon CMOS circuitry [17]. For high speed data transmission (>100Gb/s) using a direct bandgap semiconductor, recent developments have been made in InP with increasing density photonic integrated circuits [18]. Merging such devices into the established silicon industry would reduce cost.

Despite the high electron mobility, the narrow bandgap in InSb and InAs creates a high intrinsic carrier concentration even at room temperature and typically leads to high leakage currents in field effect transistors (FETs) [19]. Alternatively, the narrow bandgap in InSb makes it an outstanding candidate for mid-infrared photodetectors, [20]. Figure 1.4 is an example of a photovoltaic sensor, fabricated on a semi-insulating GaAs substrate taken from Kuze et al. GaAs was used because it is transparent to IR.

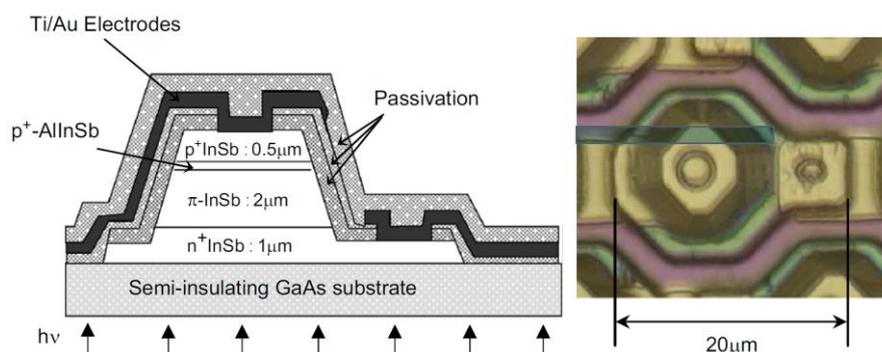


Figure 1.4: Structure of a single InSb IR photovoltaic sensor. Taken from N. Kuze et al. [21]

1.2.2. Strain engineered epilayers for CMOS and spintronic applications

SiGe is currently the preferred material in CMOS, to extend Moore's law due to: miscibility of the two elements at all concentrations, low cost and relative ease of growth on silicon substrates. Bulk Ge has higher charge carrier mobilities than bulk Si, however for both elements the hole mobility is lower than the electron mobility, as shown in table 2.2, therefore increasing mobility in p-MOS is key to improving CMOS efficiency.

Increasing carrier mobility is accomplished though reducing the carrier effective mass and/or increasing the scattering time. For example, applying compressive strain to Ge has the effect of increasing hole mobility [22]. Applying "global" strain to Ge can be carried out using relaxed $\text{Si}_{1-x}\text{Ge}_x$ buffer layers and recent developments have been made using reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers to create 20nm thick compressively strained Ge channels with hole mobility in excess of $1 \times 10^6 \text{ cm}^2/\text{Vs}$ at 12K [23] and in excess of $4 \times 10^3 \text{ cm}^2/\text{Vs}$ [24] at room temperature for spintronic applications.

1.3. Scope of work

The investigations and results of this project are divided into four chapters: 4 to 7. The purpose of chapters 4 to 6 of this project is to study the strain relaxation and defect

generation in state of the art pure Ge and three types of competitive graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers: forward linear grading, reverse linear grading and reverse step grading on on-axis and 6° off-axis Si(001) using reduced pressure chemical vapour deposition (RP-CVD), to produce high quality buffer layers that can act as a platform for future lattice matched epitaxy of III-V layers such as GaAs, AlP and GaP as well as strain engineered silicon germanium layers. A comparison is made between the suitability of forward linearly graded $\text{Si}_{1-x}\text{Ge}_x$ with the recently developed reverse linearly graded technique for such applications. Reverse grading is investigated further through reverse step grading. Chapter 7 involves the investigation of strain relaxation in InSb, the III-V with the highest lattice mismatch to Si(001) using high quality Ge buffer layers. The applications intended are listed in the motivation sub section, above.

Given that both the on-axis and 6° off-axis substrate roughness's (R_{rms}) are approximately 0.1nm and have a threading dislocation density (TDD) of $\times 10^2 \text{ cm}^{-2}$, for both application routes the buffer layer R_{rms} and TDD are targeted to be as close to substrate values as possible and promoting maximum to full strain relaxation. This is of particular importance for CMOS and spintronic applications where considerable defect density and surface roughening will degrade device performance for device geometries listed in section 1.1.

2. Theoretical Discussion.

2.1. Semiconductor crystallography.

A crystal structure is defined as a group of atoms, known as the basis, which is attached to every point in a regular periodic array known as a lattice [25]. The regular atomic ordering in a crystal is useful in explaining the macroscopic electronic, magnetic and thermal properties that it exhibits [10]. The arrangement of the basis atoms in a crystal will look identical at points r and r' given that the crystal translation vector, \underline{T} , is satisfied:

$$\underline{T} = u_1 \underline{a}_1 + u_2 \underline{a}_2 + u_3 \underline{a}_3 \quad (\text{Equation 2.1})$$

Where: \underline{a}_1 , \underline{a}_2 and \underline{a}_3 are noncoplanar vectors and u_1 , u_2 and u_3 are arbitrary integers as seen in figure 2.1 [26]. The primitive cell is defined as being the smallest volume cell and contains 1 lattice point and consequently a single basis as shown in figure 2.2.

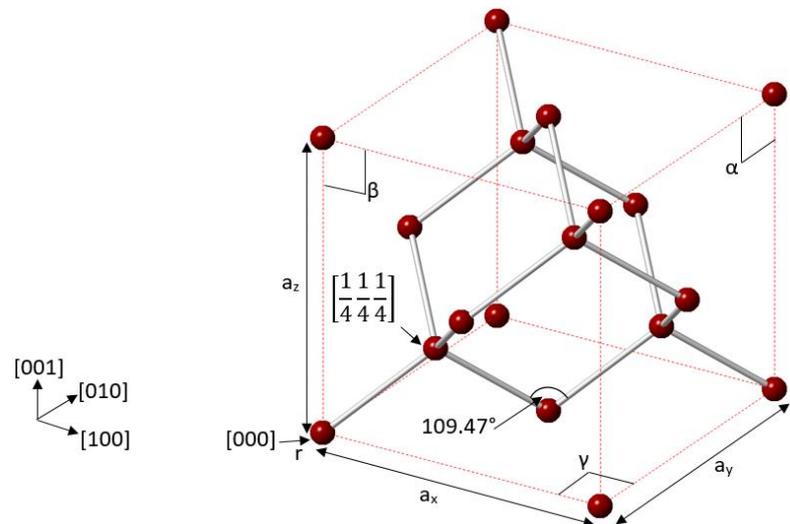


Figure 2.1: Diamond fcc lattice structure, where: $a = a_x = a_y = a_z$ & $\beta = \alpha = \gamma = 90^\circ$. The red spheres represent atoms and the silver rod are covalent bonds. The diamond basis contains 2 atoms separated by a quarter diagonal. The tetragonal bonds in a diamond structure are all 109.47° . (Adapted from Kittel) [26]

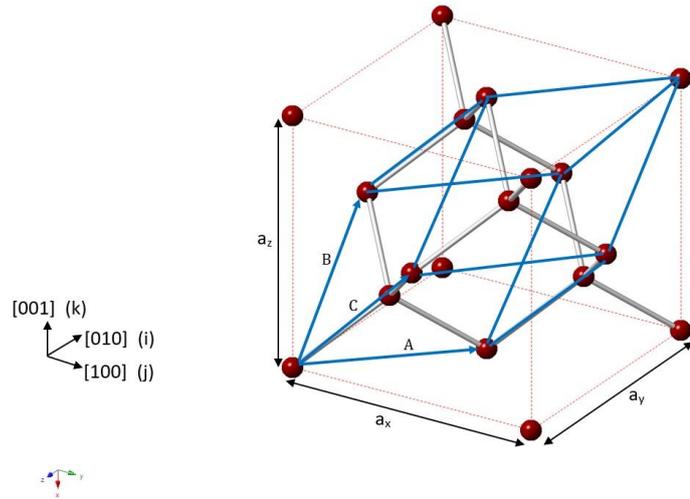


Figure 2.2: Diamond fcc lattice and primitive cell (in blue). The primitive cell vectors are: $A = \frac{a}{2}[\mathbf{i} + \mathbf{j}]$, $B = \frac{a}{2}[\mathbf{i} + \mathbf{k}]$ and $C = \frac{a}{2}[\mathbf{j} + \mathbf{k}]$. (Adapted from Kittel)[26].

There are 7 crystal systems which are sub-divided into 14 lattice types known as Bravais lattice. A space group for a particular Bravais lattice is defined by the number of symmetry operations. In a cubic lattice unit cell, the unit cell angles are all 90° and the unit cell length is identical in all directions. Within the cubic crystal system, there are 3 Bravais lattices: primitive cubic (sc or cP), body centred cubic (bcc or cI), face-centred cubic (fcc or cF). The diamond structure is a particular fcc crystal, where two fcc structures are combined into a single lattice, as seen in figure 2.1. Table 2.1 compares the simple fcc structure with the diamond fcc structure. In a diamond basis there are two identical atoms at position $[000]$ and $[\frac{1}{4}\frac{1}{4}\frac{1}{4}]$, hence there are 8 atoms per unit cell, instead of 4 as is typical in standard fcc lattices. The point group for diamond structures is O_h (Schoenflies notation) [27] and the space group is $Fd\bar{3}m$ (Hermann-Mauguin notation), where the F indicates face centered cubic, d indicates translational symmetry along the quarter face diagonal i.e.: a glide plane and $\bar{3}$ pertains to rotational symmetry along 4 diagonal 3-fold axes and m denotes 2 rotoinversion axes i.e.: a mirror plane [28]. Group IV elements such as carbon, silicon, germanium, α -Sn and group IV alloys such as SiGe have this type of covalent bonded structure.

	FCC	Diamond FCC
Conventional cell volume	a^3	a^3
Lattice points per cell	4	4

Atoms per unit cell	4	8
Primitive cell volume	$\frac{1}{4}(a^3)$	$\frac{1}{4}(a^3)$
Lattice points per unit volume	$\frac{4}{a^3}$	$\frac{4}{a^3}$
Number of nearest neighbours	12	4
Nearest-neighbour distance	$\frac{a\sqrt{2}}{2}$	$\frac{a\sqrt{3}}{4}$
Number of second neighbours	6	12
Second neighbour distance	a	$\frac{a\sqrt{2}}{2}$

Table 2.1: Comparison between fcc lattice and diamond fcc lattice [26]

The zinc blende structure is related to the diamond structure where the basis is composed of two different atoms, as is in ZnS where the Zn atoms occupy atomic sites starting at [000] and S atoms occupy sites at a quarter diagonal from the Zn. Many III-V binary compounds exist most stably as a zinc blende fcc lattice except for III-V nitrides which are most stable as a hexagonal, Wurtzite, lattice structures e.g.: boron nitride, gallium nitride and indium nitride. Due to the space group similarities between diamond and zinc blende, zinc blende semiconductors can therefore be “grown” on diamond fcc substrates such as silicon and germanium, where the grown crystal can be expected to maintain its structure and orientation in a process known as epitaxy.

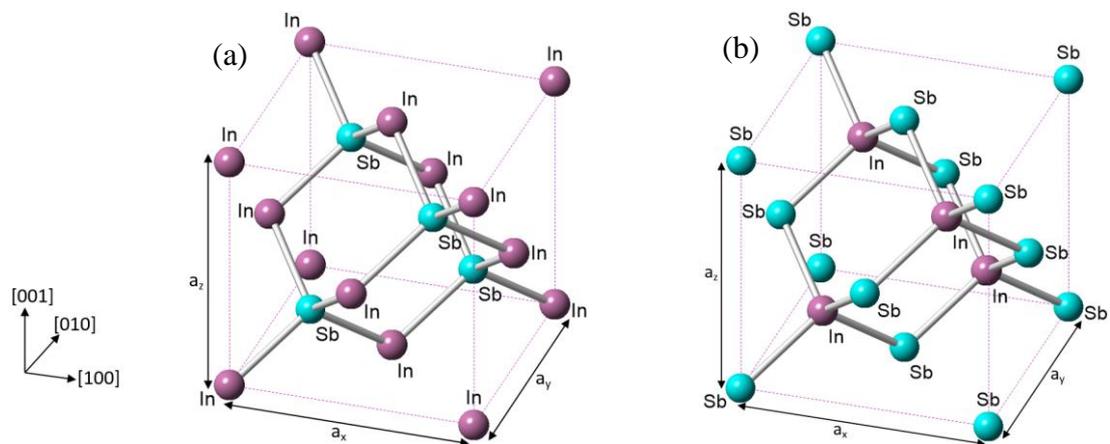


Figure 2.3: InSb unit cells showing the typical Zinc Blende structure in the diamond fcc lattice. $a_x = a_y = a_z$ is the lattice constant. In figure 2.3(a) the indium atoms (purple) occupy one fcc ‘structure’ at [000] and

the antimony atoms (blue) occupy the other fcc structure at $\left[\frac{1}{4}\frac{1}{4}\frac{1}{4}\right]$. Figure 2.3(b) is of an equivalent ‘sub-lattice’ orientation of InSb where the antimony atom occupies the [000] site and the indium atom occupies the $\left[\frac{1}{4}\frac{1}{4}\frac{1}{4}\right]$ sites, which is achieved by 90° rotation or translation from (a) to (b). (Adapted from Grundmann [29]).

Figure 2.3 (a) & (b) show unit cells of the III-V compound semiconductor InSb which has a zinc blende structure and a fcc lattice. The point group for zinc blende structures is T_d and the space group is $F\bar{4}3m$, there are 4 three-fold rotoinversion axes as is the case with all cubic space groups and the m indicates a mirror plane. There are 48 symmetry operations with diamond structure however there are only 24 with zinc blende structures [27]. Unlike diamond structure there is no quarter diagonal glide plane for translational symmetry in zinc blende structures, therefore the [110] and $[\bar{1}10]$ directions are not equivalent. Figure 2.3. (a) & (b) shows two alternative unit cells of InSb where both lattices have the same zinc blende fcc lattice space group, however the indium and antimony atoms occupy opposite locations. Figure 2.3 (a) can be converted to figure 2.3 (b) by applying any of the 24 symmetry operations present in the diamond structure but not present in zinc blende [28]. As will be discussed later on in this investigation, the simultaneous presence of the two sub lattices on a diamond cubic substrate surface leads to the generation of regions in the epitaxial crystal known as inversion domains. Inversion domains are regions with the alternate sub lattice, i.e.: regions where the polar direction changes. Due to the difference in valence electrons between the two elements in a zinc blende fcc lattice, charge neutrality is not maintained at the boundary between sub lattices leading a charged defect [29, 30]. This will be covered later in the defects section.

2.2. The Reciprocal lattice.

The crystal lattice described in section 2.1 in terms of lattice translation vectors by equation 2.1, can also be described in terms of a reciprocal translation vector, \underline{G} , in reciprocal space otherwise known as momentum space or ‘k-space’, $\left(k = \frac{2\pi}{\lambda}\right)$:

$$\underline{G} = m_1\underline{A}_1 + m_2\underline{A}_2 + m_3\underline{A}_3 \quad (\text{Equation 2.2})$$

Where: m_1, m_2 and m_3 are arbitrary integers and $\underline{A}_1, \underline{A}_2$ and \underline{A}_3 are noncoplanar reciprocal space vectors. The relationship to the real space vectors: $\underline{a}_1, \underline{a}_2$ & \underline{a}_3 is [26]:

$$\underline{A}_1 = 2\pi \frac{\underline{a}_2 \times \underline{a}_3}{\underline{a}_1 \cdot (\underline{a}_2 \times \underline{a}_3)} \quad (\text{Equation 2.3})$$

$$\underline{A}_2 = 2\pi \frac{\underline{a}_3 \times \underline{a}_1}{\underline{a}_2 \cdot (\underline{a}_3 \times \underline{a}_1)} \quad (\text{Equation 2.4})$$

$$\underline{A}_3 = 2\pi \frac{\underline{a}_1 \times \underline{a}_2}{\underline{a}_3 \cdot (\underline{a}_1 \times \underline{a}_2)} \quad (\text{Equation 2.5})$$

2.2.1. Bragg diffraction in crystals

For a wave with a wavelength, λ , that is comparable to the spacing between planes of atoms in a crystal, d , undergoing scattering the intensity of the interference is given by Bragg's law:

$$n\lambda = 2d\sin\theta \quad (\text{Equation 2.6})$$

Figure 2.4 shows this phenomenon. The path difference for two waves of wavelength, λ , that are diffracted off adjacent planes of atoms (denoted by the red spheres) in a crystal is proportional to the plane spacing, d , multiplied by the sine of the incident angle, θ . The blue lines showing the incoming and outgoing wave fronts that are in phase for this condition. Coherency of the incoming and outgoing waves will be maintained, provided that the path difference is an integer multiple of the wavelength, which results in the two outgoing waves interfering constructively. (Adapted from Kittel) [26].

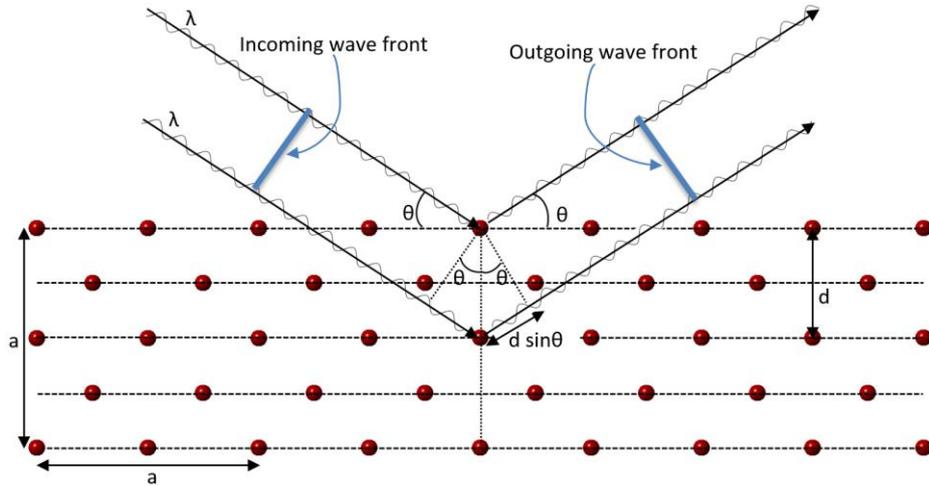


Figure 2.4: Diagram demonstrating Bragg's law in a diamond lattice.

The principle of Bragg diffraction is explained further in chapter 3 on experimental techniques as it is used in transmission electron microscopy and x-ray diffractometry to study the epitaxial layers in this investigation.

2.3. Material properties of group IV and III-V semiconductors

2.3.1. Properties of silicon, germanium and $\text{Si}_{1-x}\text{Ge}_x$ alloys.

2.3.1.1. Material properties of silicon, germanium and $\text{Si}_{1-x}\text{Ge}_x$ alloys.

Property	Silicon	Germanium	$\text{Si}_{1-x}\text{Ge}_x$
Atomic number	14	32	
Relative atomic mass	28.0855	72.630	
Electron configuration	$[\text{Ne}] 3s^2 3p^2$	$[\text{Ar}] 3d^{10} 4s^2 4p^2$	
Crystal structure	FCC Diamond	FCC Diamond	FCC Diamond
Space group	$O_h^7 - \text{Fd}\bar{3}m$	$O_h^7 - \text{Fd}\bar{3}m$	$O_h^7 - \text{Fd}\bar{3}m$ (random alloy)

Number of atom (cm ⁻³)	5.00×10^{22}	4.42×10^{22}	$(5.00 - 0.58x) \times 10^{22}$
Lattice constant (Å)	5.43102	5.6579	$a_{Si}(1-x) + a_{Ge}x - 0.02733x(1-x)$
Energy band gap (eV)	1.12	0.66	$1.12 - 0.41x + 0.008x^2$ ($x < 0.85$) $1.86 - 1.2x$ ($x > 0.85$)
Density (g/cm ³)	2.329	5.323	$2.329 + 3.493x - 0.499x^2$
Electron mobility (μ_e) (cm ² /Vs)	1450	3900	$1450 - 4325x$ ($0 \leq x < 0.3$)
Hole mobility (μ_h) (cm ² /Vs)	450	1900	$450 - 865x$ ($0 \leq x < 0.3$)
Elastic moduli:			
C ₁₁ (GPa)	165.8	128.8	$165.8 - 37.3x$
C ₁₂ (GPa)	63.9	48.3	$63.9 - 37.3x$
C ₄₄ (GPa)	79.6	66.8	$79.6 - 12.8x$
Bulk modulus, K (GPa)	98	75	$98 - 23x$
Shear modulus, G (GPa)	52	41	$52 - 11x$
Youngs modulus, Y (GPa)	[001]=130 [011]=169	[001]=103 [011]=137	[001]=130-27x [011]=169-32x
Poisson ratio, ν (σ_{100})	0.28	0.26	$0.28 - 0.02x$
Melting point (°C)	1412	937	$1412 - 738x + 263x^2$ (solidus) $1412 - 80x - 395x^2$ (liquidus)
Linear thermal expansion (°C ⁻¹)	2.61×10^{-6}	5.84×10^{-6}	$(2.6 + 2.55x) \times 10^{-6}$ ($x < 0.85$) $(7.53x - 0.89) \times 10^{-6}$ ($x > 0.85$)

Table 2.2: Table of the properties of silicon, germanium and Si_{1-x}Ge_x at 300K [31]

Si_{1-x}Ge_x is a diamond fcc lattice alloy composed of silicon and germanium atoms occupying random sites in the unit cell, as seen in figure 2.5.

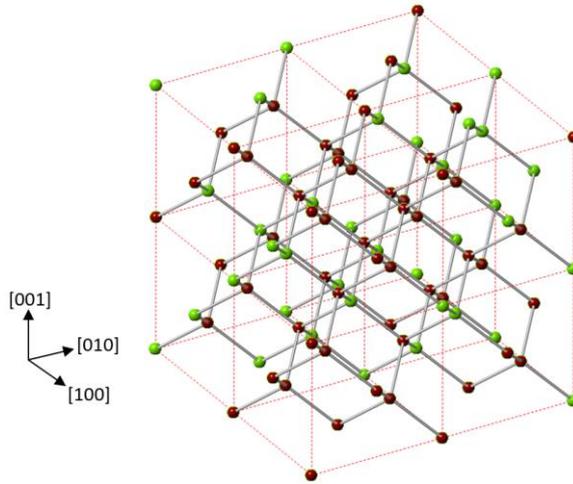


Figure 2.5: $\text{Si}_{1-x}\text{Ge}_x$ alloy diamond lattice of 8 unit cells. Germanium atoms (green) and silicon (red) occupying random sites in the lattice.

The bulk lattice constants for Si (a_{Si}) and Ge (a_{Ge}) are temperature dependent. An early x-ray camera measurement into silicon by Yim [32] concluded a quadratic approximation of the lattice constant (a_{T}) with respect to temperature, T , between 20°C and 800°C by using a least squares fit to the data. However low temperature measurements on silicon carried out such as by Batchelder and Simmons [33] (between 48.85°C and -267.15°C) and Straumanis and Shah [34] between -93.15°C and -233.15°C showed a negative thermal expansion coefficient.

The linear coefficient of thermal expansion of a material is defined as the fraction of its original length by which the material expands per degree rise in temperature. The lattice constant is related to the linear thermal expansion coefficient, (α_{T}), by the following relationship as determined by Okada [35] and Scheffler [36]:

$$\alpha_{\text{T}} = \frac{1}{a_0} \left(\frac{da_{\text{T}}}{dT} \right) = \frac{1}{a_0} \frac{(l_1 - l_2)}{(T_1 - T_2)} \quad (\text{Equation 2.7})$$

Where a_0 is the lattice constant at 0°C ; and l_1 & l_2 are the measured lattice constants at temperatures T_1 & T_2 respectively. By calculating the linear thermal expansion coefficient through changes in lattice constant at various temperature intervals, plotting it against temperature and working out the linear thermal expansion

coefficient function; the correct expression for lattice constant can be determined as follows:

$$\int da_T = a_0 \int \alpha_T dT \quad (\text{Equation 2.8})$$

First valid reports on Germanium's temperature dependent lattice parameter measurements were carried out by Singh [37] between 20°C and 812°C. However lower temperature capacitance bridge measurements carried out at between -265.15°C to 6.85°C by Carr et.al [38] also showed a negative thermal expansion. As will be covered later in the coefficient of thermal expansion sub chapter, it was determined that the negative thermal expansion at low temperatures in diamond structures is brought on by the changes in various lattice vibrational modes with respect to the crystal volume, in a parameter known as the Grüneisen parameter [39].

The equations for (a_T) for pure silicon and pure germanium below are obtained by using a nonlinear least squares fit to the data collected by Reeber and Wang from other works using various X-ray diffraction and interferometry techniques along with the semi-empirical quasi-harmonic model calculation for extrapolating lattice parameter and thermal expansion coefficient [40].

$$a_{Si}(T) = (5.428 + (2.385 \times 10^{-5})T + (1.654 \times 10^{-10})T^2 + (1.353 \times 10^{-3})e^{(0.7291 - (4.056 \times 10^{-3})T)}) \text{Å} \quad (\text{Equation 2.9})$$

$$a_{Ge}(T) = (5.656 + (3.706 \times 10^{-5})T + (3.312 \times 10^{-9})T^2 + (3.168 \times 10^{-4})e^{(0.7291 - (7.885 \times 10^{-3})T)}) \text{Å} \quad (\text{Equation 2.10})$$

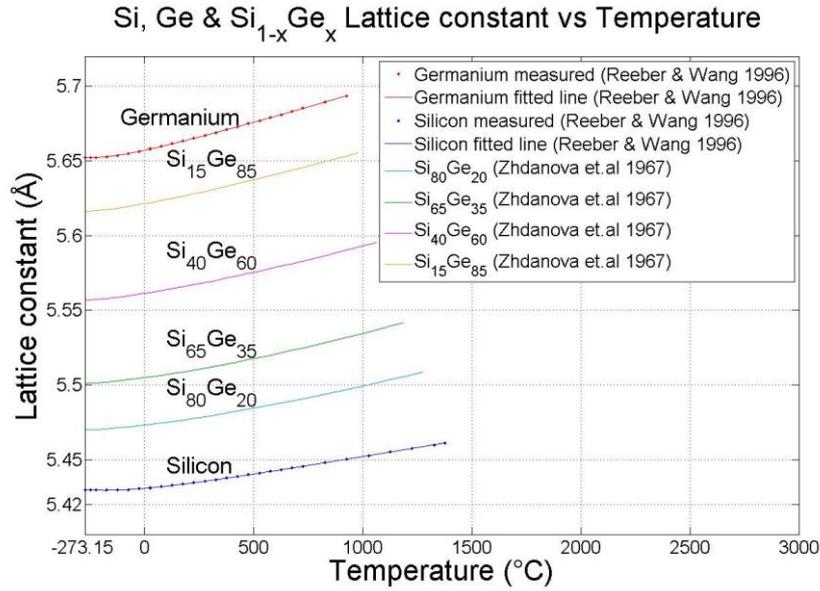


Figure 2.6: Lattice constant vs Temperature for pure silicon, pure germanium and constant composition $\text{Si}_{1-x}\text{Ge}_x$ alloys from absolute zero to the respective melting temperatures. The pure silicon and germanium plots were obtained from Reeber and Wang's data using semi-empirical quasi-harmonic models, whilst the constant composition $\text{Si}_{1-x}\text{Ge}_x$ alloy plots were extrapolated from Zhdanova et al's thermal expansion data back to absolute zero.

In figure 2.6 the fitted lines and equations for temperature dependent lattice constant for pure silicon and pure germanium were obtained by using a non-linear least squares fit to the data by Reeber and Wang 1996 (equations 2.9 and 2.10 respectively). The constant composition SiGe lattice constant plots and equations were deduced from thermal expansion coefficient data from Zhdanova 1967 and by using equation 2.8. The melting temperature for constant composition SiGe was determined from the equations in table 2.2 [31].

The bulk lattice constant of the $\text{Si}_{1-x}\text{Ge}_x$ film is determined by the Kasper corrected Vegard's law [41]:

$$a_{\text{Si}_{1-x}\text{Ge}_x} = (a_{\text{Si}}(1-x) + a_{\text{Ge}}x - \underbrace{0.02733x(1-x)}_{\text{Bowling parameter}}) \text{Å} \quad (\text{Equation 2.11})$$

Despite silicon and germanium being completely miscible over the entire composition range, growing homogenous and uniform composition single crystal ingots of $\text{Si}_{1-x}\text{Ge}_x$ is difficult due to the large difference in solidus and liquidus phase boundaries [31] as shown in figure 2.7.

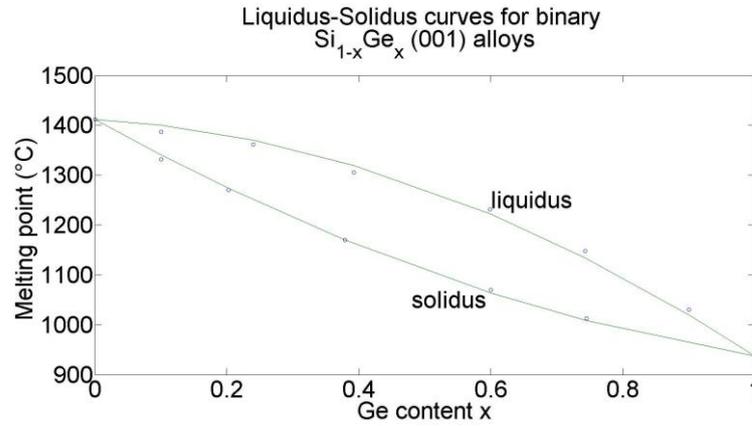


Figure 2.7: Phase curves for binary $\text{Si}_{1-x}\text{Ge}_x$ shows differences in temperatures in the solidus and liquidus phases.

With the advent of various low temperature epitaxy techniques however, the last 25 years has seen the development of high quality thin film of $\text{Si}_{1-x}\text{Ge}_x$ of $1 \geq x \geq 0$ to be used in device fabrication as well as further epitaxy and band engineering various group IV and III-V semiconductor materials on Si(001).

2.3.1.1.1. Coefficient of thermal expansion

In epitaxial growth along with lattice mismatch another competing effect is thermal expansion coefficient mismatch between epilayer materials. For silicon it is determined from equation 2.9 for the silicon lattice constant and then differentiating with respect to temperature and multiplying by $\frac{1}{a_0}$ as in equation 2.7 and is as follows:

$$\alpha_{\text{Si}}(T) = \left((4.3916 \times 10^{-6}) + (6.0912 \times 10^{-11})T - (1.0105 \times 10^{-6})e^{(0.7291 - (4.056 \times 10^{-3})T)} \right) ^\circ\text{C}^{-1} \quad (\text{Equation 2.12})$$

For germanium it is determined from equation 2.10 in the same manner and is as follows:

$$\alpha_{\text{Ge}}(T) = \left((6.5508 \times 10^{-6}) + (1.1708 \times 10^{-9})T - (4.416 \times 10^{-7})e^{(0.7291 - (7.885 \times 10^{-3})T)} \right) \text{ } ^\circ\text{C}^{-1} \quad (\text{Equation 2.13})$$

The negative thermal expansion observed below -153.15°C by refs [34] and [33] is due to a negative Grüneisen parameter which describes the shrinking of the volume of a crystal lattice due to the change in vibrational frequencies at low temperature [26].

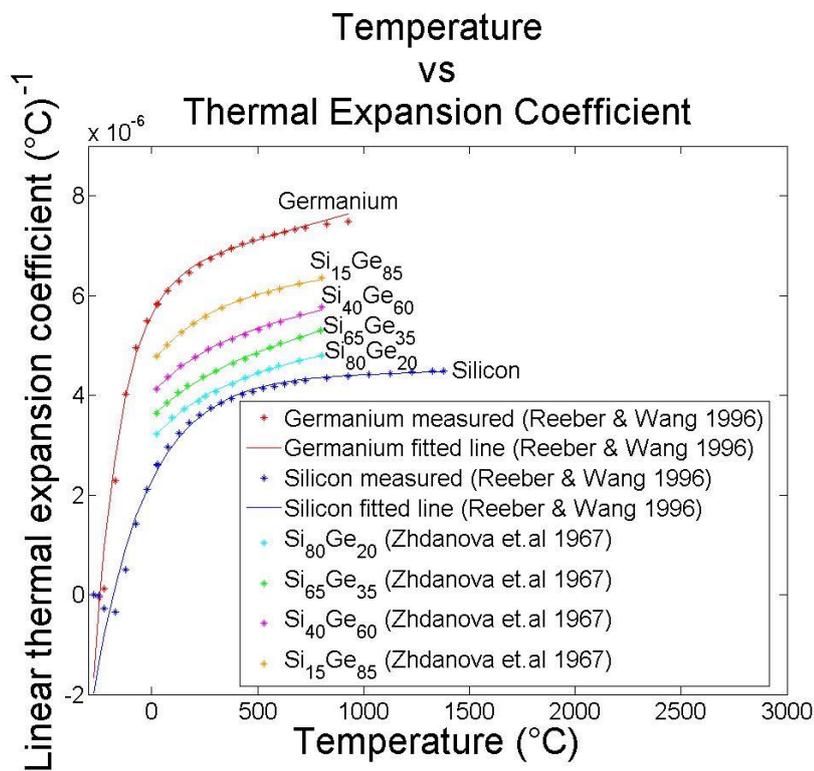


Figure 2.8: Linear thermal expansion coefficient vs Temperature plot of $\text{Si}_{1-x}\text{Ge}_x$ alloys. For silicon and germanium, the expansion coefficient was plotted from absolute zero up to the melting temperatures however for SiGe alloys the plots were made using the data from Zhdanova et al in 1967 [31].

2.3.2. Properties of III-V semiconductors.

Other than silicon and germanium other materials also display semiconducting properties. When some elements in group III of the periodic table (or group 13 under the new International Union of Pure and Applied Chemistry (IUPAC) [42]) are chemically combined with some from group V to form a compound, the compound exhibits semiconducting properties.

Property	AlP	GaP	GaAs
Crystal structure	FCC Zinc Blende	FCC Zinc Blende	FCC Zinc Blende
Space group	$T_d^2 - F\bar{4}3m$	$T_d^2 - F\bar{4}3m$	$T_d^2 - F\bar{4}3m$
Relative molecular mass	57.955299	100.696761	144.6446
Number of atoms (cm ⁻³)	4.91×10^{22}	4.94×10^{22}	4.42×10^{22}
Ionicity	$f_i = 0.307$ $f_i^P = 0.25$ $f_i^H = 0.47$	$f_i = 0.327$ $f_i^P = 0.27$ $f_i^H = 0.48$	$f_i = 0.310$ $f_i^P = 0.26$ $f_i^H = 0.47$
Lattice constant (Å)	5.4635	5.4505	5.65325
Nature of band gap	Indirect	Indirect	Direct
Energy band gap (eV)	2.45	2.26	1.42
Density (g/cm ³)	2.3604	4.1299	5.31749
Electron mobility (μ _e) (cm ² /Vs)	60	250	8500
Hole mobility (μ _h) (cm ² /Vs)	450	150	400
Elastic moduli:			
C ₁₁ (GPa)	150	141	118.8
C ₁₂ (GPa)	64.2	62.0	53.8
C ₄₄ (GPa)	61.1	70.3	59.4
Bulk modulus, K (GPa)	92.8	88.2	75.5
Shear modulus, G (GPa)	42.9	39.2	32.5
Youngs modulus, Y (GPa)	[001] = 111 [011] = 138	[001] = 103 [011] = 144	[001] = 85.3 [011] = 121.3
Poisson ratio (σ ₁₀₀)	0.3	0.306	0.312
Melting point (°C)	2530	1457	1240
Linear thermal expansion (°C ⁻¹)	4.7×10^{-6} [43]	4.65×10^{-6}	5.87×10^{-6}

Table 2.3: Table of the properties of binary III-V compounds with lattice constants in-between pure silicon and pure germanium at 300K [44] [45].

Property	GaN (β -cubic)	AlSb	InSb
Crystal structure	FCC Zinc Blende (meta stable)	FCC Zinc Blende	FCC Zinc Blende
Space group	$T_d^2 - F\bar{4}3m$	$T_d^2 - F\bar{4}3m$	$T_d^2 - F\bar{4}3m$
Relative molecular mass	83.72974	148.741538	236.578
Number of atoms (cm^{-3})	8.66×10^{22}	3.46×10^{22}	2.94×10^{22}
Ionicity	$f_i = 0.5$ $f_i^P = 0.55$ $f_i^H = 0.61$	$f_i = 0.25$ $f_i^P = 0.26$ $f_i^H = 0.56$	$f_i = 0.5$ $f_i^P = 0.55$ $f_i^H = 0.61$
Lattice constant (\AA)	4.52	6.1355	6.47937
Nature of band gap	Direct	Indirect	Direct
Energy band gap (eV)	3.25	1.615	0.17
Density (g/cm^3)	6.02	4.278	5.777
Electron mobility (μ_e) (cm^2/Vs)	1000	200	77,000
Hole mobility (μ_h) (cm^2/Vs)	200	400	850
Elastic moduli:			
C_{11} (GPa)	291	87.69	66.08
C_{12} (GPa)	148	43.41	35.31
C_{44} (GPa)	158	40.76	30.27
Bulk modulus, K (GPa)	196	58.2	45.6
Shear modulus, G (GPa)	71.5	22.1	15.1
Young's modulus, Y (GPa)	[001] = 191 [011] = 301	[001] = 58.9 [011] = 84.7	[001] = 41.5 [011] = 62.1
Poisson ratio (σ_{100})	0.337	0.331	0.348
Melting point ($^\circ\text{C}$)	2500	1060	527
Linear thermal expansion ($^\circ\text{C}^{-1}$)	3.17×10^{-6}	4.2×10^{-6}	5.37×10^{-6}

Table 2.4: Table of the properties of binary III-V compounds with lattice constants outside of pure silicon and pure germanium at 300K [44] [45].

2.4. Epitaxy.

The term Epitaxy was first coined by Louis Royer in 1928 from the Greek words “epi” which means above and “taxis” which means in an ordered manner [46]. It is the process whereby a crystal of material is grown on a bulk crystal surface, known as a substrate, where the grown material or “epilayer” has the same crystal structure and orientation as the substrate material.

The substrate and epilayer materials can be identical, known as homoepitaxy, or they could be dissimilar materials, known as heteroepitaxy.

The process of epitaxy has been of great importance to the semiconductor industry since the 1960’s as it has allowed the development of highly complicated multilayer structures for device applications. Current epitaxy techniques have exceeded the thermodynamic equilibrium in such a way as to create layers that are merely a few nm thick with atomically sharp interfaces or even single layers of atoms. This has given rise to semiconductor device structures with quantum wells and super lattices which exhibit quantum confinement of carriers [46].

In industry the epitaxy techniques are predominantly vapour phase based. This means that the precursors are vaporised at high temperature and brought into a gaseous phase first before deposition. The two types of vapour phase epitaxy are physical vapour deposition (PVD) where the precursors are solid materials which are then vaporised at high temperature and chemical vapour deposition (CVD) where the source materials are chemical precursors. The most prominent PVD technique is solid source molecular beam epitaxy (MBE) where beams of adatom species are generated through heating of the solid precursors in effusion cells until vaporisation.

2.4.1. Reduced Pressure Chemical Vapour Deposition (RP-CVD).

CVD is the most frequently used technique for semiconductor device fabrication. Its uses are not restricted to semiconductors but also include oxides, metals and organic materials in spin off techniques. Plasma enhanced CVD (PECVD) involves vaporising and ionising the precursors into plasma, which allows for epitaxy at low temperatures. Metal organic CVD (MOCVD) is where the precursors are metalorganic and is used in the deposition of III-V semiconductors. Unlike MBE, parameters such as growth rate, temperature and pressure are not independent variables with CVD.

The pressures used in CVD techniques range from ultra-high vacuum (UHV) at approximately 7.5×10^{-10} Torr to atmospheric pressure (760 Torr). The reduction in pressure from atmospheric pressure allows for a reduction of precursor gas diffusion. With CVD techniques, there are two velocities to be concerned with. The first is the mass transport velocity and the second is the surface reaction velocity. The mass transport velocity is proportional to the concentration and diffusion of the reactants as well the boundary layer thickness forming on the substrate. Thus the mass transport velocity will also decrease as the pressure is reduced, due to Bernoulli's equation. The end effect for a reduced mass transport velocity is that the deposited film grows more homogeneously and uniformly with fewer defects [47]. The obvious disadvantage to ever reducing the pressure from atmospheric pressure is that the deposition rate is slowed down and hence from an industrial point of view, the epiwafer production rate is reduced.

In this investigation reduced pressure chemical vapour deposition is used to grow $\text{Si}_{1-x}\text{Ge}_x$ and Ge buffer layers. Figure 2.19 (b) is a cross-sectional diagram for an RP-CVD growth chamber. Figure (c) is a photo of the chamber of the ASM Epsilon cold wall RP-CVD reactor used in this investigation. The operating pressure is 100 Torr. The substrates are brought onto the susceptor and baked at 1000°C under hydrogen gas to remove the native oxide; baking at a higher temperature could cause slip dislocations in the substrate as well as single atomic step surface reconstruction [48], [49]. The precursor gases (and dopant gases) are brought into the chamber on the left of the diagram at precise mass flow rates so as to control the growth rate of the epilayer.

The infra-red lamps heat the substrate whilst the gases flow over the surface and temperature is monitored using thermocouples. The substrates are rotated on the susceptor to ensure uniform exposure of precursors over the surface. The final stage involves venting the gases from the chamber to chemical scrubbers for purification of toxic gases before being vented to the external atmosphere.

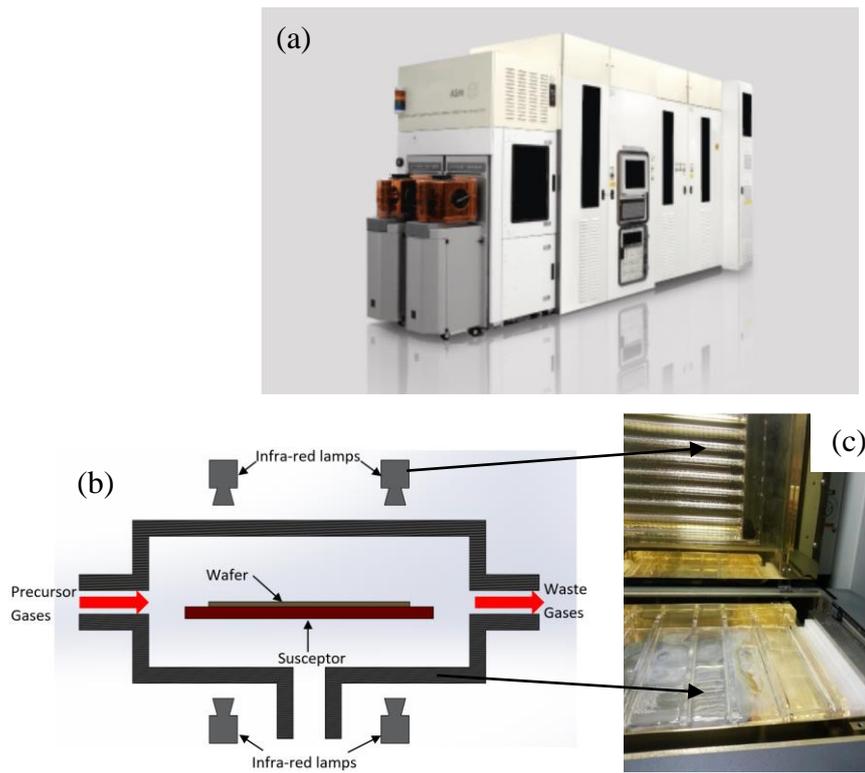


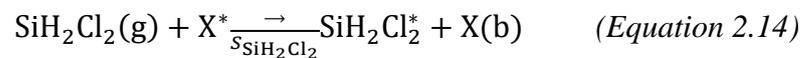
Figure 2.9: Figure (a) is an image of the ASM Epsilon 2000 RP-CVD reactor used in this project to grow $\text{Si}_{1-x}\text{Ge}_x$ and Ge buffer layers. Figure (b) is a cross sectional schematic of standard CVD chamber. Figure (c) is an image taken of the ASM Epsilon 2000 RP-CVD reactor chamber.

2.4.1.1. Si, Ge and SiGe reaction kinetics using RP-CVD

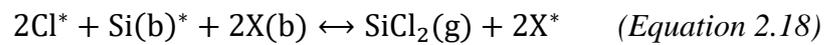
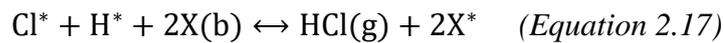
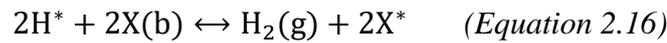
The precursors used are dichlorosilane (SiCl_2H_2) for silicon species. Germanium tetrahydride (Germane, GeH_4) is used for the germanium species. Hydrogen is used as the carrier gas. Dichlorosilane was chosen over other silicon precursors such as silicon tetrahydride (SiH_4) because during growth, deposition also occurs on the quartz chamber surface. This has the negative effect of blocking infra-red radiation to the wafer surface thereby destabilising epilayer growth conditions. In spite of the slower growth rate on silicon surfaces with chlorosilanes, the HCl gas generated by the reaction of the H_2 carrier gas with chlorine atoms allows the etching of the quartz chamber surface [50].

In this investigation, apart from one or two wafers grown in the reverse terrace graded $\text{Si}_{1-x}\text{Ge}_x$ study, HCl gas was not introduced along with the precursors and the hydrogen carrier gas. After an epilayer has been deposited on a wafer, the wafer is taken out and HCl gas is introduced into the chamber to etch it and remove any deposition from the chamber walls.

The decomposition of dichlorosilane to deposit silicon on the substrate includes both gas-phase and surface reactions. Surface reactions involve gas-phase molecules colliding with the substrate surface in which one of two events can occur depending on the energy of the precursor molecule and surface structure. Either the molecule reflects back to the gas phase or it adsorbs to the surface and decomposes there [51]. The parameter that determines this is known as the sticking coefficient and describes the probability of a dichlorosilane molecule hitting an atom, X, that is bonded to a surface site on the substrate described by (equation 2.14). X could be a silicon atom as part of the substrate or a germanium atom epitaxially deposited on the substrate and hence the sticking coefficient, $S_{\text{SiH}_2\text{Cl}_2}$, varies depending on the species of X. In the equations below ‘*’ denotes a surface free site, ‘b’ denotes the bonded lattice atom and ‘g’ denotes the gaseous species.



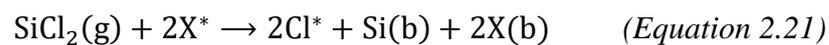
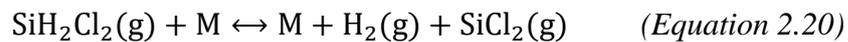
The surface reaction takes place at all temperatures up to the silicon melting point. As described by Hierlemann et al [51], the chemical equations describing the surface reaction are as follows:



The importance of the carrier gas is in diluting the precursor concentration in the growth chamber and ensuring that the wafer surface is evenly exposed to equal concentrations of precursors. Unlike argon or nitrogen, which are inert to the deposition reactions; the presence of hydrogen leads to an additional reaction taking place:

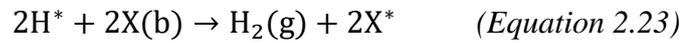


The surface reactions dominate silicon deposition until 800°C (the critical decomposition temperature for dichlorosilane) after which gas phase reactions which are thermally driven, also occur as a secondary reaction pathway. The chemical reaction is known as pyrolysis and is defined as a chemical decomposition of an organic compound in the absence of oxygen. The term, M, is a ‘third body’ term that promotes Pyrolysis in a low pressure. The gas phase reactions are as follows [51]:



The reactions of germane also follow a similar process in that there are two reaction pathways: 1) gas-phase pyrolysis of GeH₄ to GeH₂ and H₂, followed by surface reactions and 2) direct surface interaction of GeH₄. The germane direct surface

reactions are as follows (where M is again a ‘third body’ term that promotes Pyrolysis in a low pressure) [52]:



The gas phase pyrolysis of germane reaction occurs at a much lower temperature, at approximately 400°C [53], followed by subsequent surface reaction. The reactions are as follows [52]:

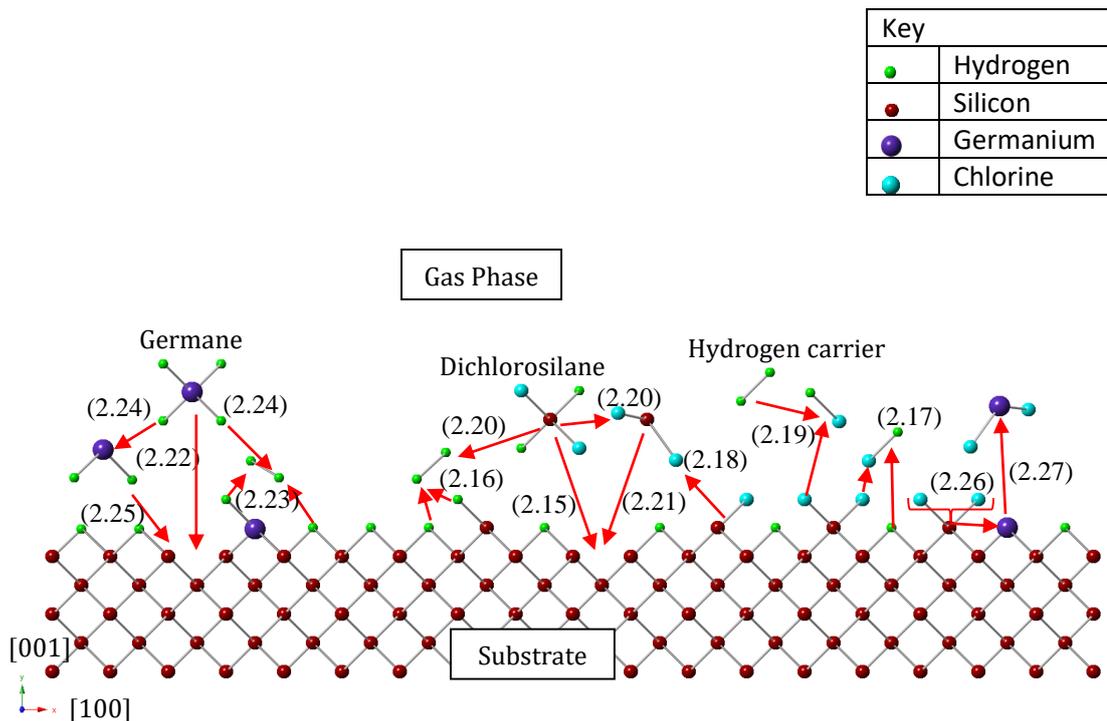
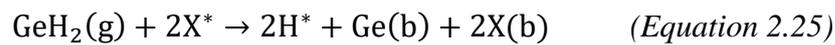
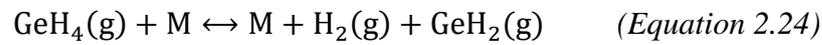
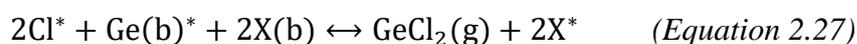
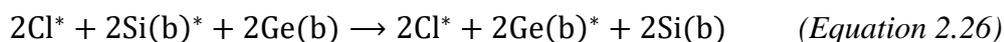


Figure 2.10: Diagram showing the surface reactions of dichlorosilane and germane on a Si(001) substrate which is initially hydrogen terminated on the surface, as a $\text{Si}_{1-x}\text{Ge}_x$ film is deposited. Adapted from Hierlemann [54]. The numbers listed in brackets in the diagram pertain to equations 2.15 to 2.27.

Figure 2.10 shows the reactions that take place on a hydrogen terminated Si(001) substrate. The reality of the deposition process is far more complicated for growth of

SiGe epilayers, since as the layer grows the surface sites become either germanium rich or silicon rich depending upon which precursors are used and what sort of layer is being deposited. This ultimately has an effect on the desorption of H and Cl adatoms since both species desorb faster from Ge sites than from Si sites [54] which leads to the generation of more free sites for the adsorption of precursor molecules and a faster growth rate. For example the activation barriers for H₂ desorption from Si (Si-H bond activation barrier of 47kcal/mol)[55] is greater than from Ge (Ge-H bond activation barrier of 37kcal/mol) [56].

Previous studies have also shown that the increased growth rate brought on by increased Ge sites on the surface is due to H and Cl species diffusing from Si sites and moving to Ge sites (unless they are already bonded to the Ge sites) and then desorbing from these more energetically favourable sites [54]. Figure 2.10 also shows the chlorine species bonded to Si free sites diffusing to a Ge free site (*equation 2.26*) and then desorbing from the surface as GeCl₂ (*equation 2.27*):



It should be noted that several decomposition pathways exist during the gas phase pyrolysis reactions for both germane and dichlorosilane. For example, GeH₄ could decompose to GeH₃ + H· or even form Ge₂H₄ through the combination of GeH₂ with GeH₄ to form Ge₂H₆ and then the subsequent reduction of H₂ from the molecule. The activation energy barrier in the formation of GeH₃ + H· is approximately 85.1 kcal/mol and the activation barrier to form GeH₂ + H₂ is 53.1 kcal/mol [57]. Similar reactions take place with dichlorosilane perhaps forming SiHCl₂ + H· but the activation energy barrier is again much higher than with the formation of H₂ + SiCl₂ as shown by the computational study of Swihart and Carr [58]. Therefore, previous computational and experimental chemistry studies have shown that the most probable reaction pathways are those listed in the (*equations 2.15 to 2.27*).

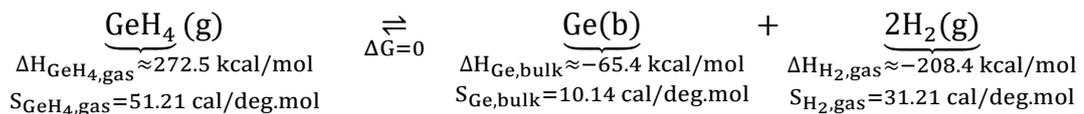
2.4.1.1.1. Growth conditions for Si_{1-x}Ge_x epilayers

The reactions for the deposition of silicon, germanium and SiGe are dependent upon the Gibbs free energy, ΔG , of the reaction. The Gibbs free energy for any thermodynamic system is given by the following equation:

$$\Delta G = \underbrace{(\Delta U + pV)}_{\Delta H} - \Delta T \cdot S \quad (\text{Equation 2.28})$$

Where: ΔU is the internal energy of the system, p is pressure, V is the volume, ΔH is the change in enthalpy of formation, ΔT is the change in temperature and S is the entropy of the system (with higher entropy in the gas phase). The equilibrium of the system will push towards the reaction stage as the Gibbs free energy reduces. For a fixed pressure and volume in the CVD chamber, this means that temperature is what drives ΔG .

Taking Germane as an example, with estimated Ge-H bond disassociation values taken from Hierlemann et al [54], and entropy values taken from the chemistry and physics handbook [59], the decomposition of germane to germanium and hydrogen is as follows:



(Equation 2.29)

$\Delta H_{\text{net,GeH}_4} \approx +1.47 \text{ kcal/mol}$, which means that the deposition process is endothermic, and $S \approx +21.4 \text{ cal/deg. mol}$. When the Gibbs free energy is at 0 the rate of the forward reaction is equal to the rate of the backward reaction. Therefore, by using equation 2.28 and equating ΔG to 0, ΔT_{GeH_4} is calculated to be approximately 69°C. When carrying out a similar calculation for dichlorosilane, it is discovered that $\Delta T_{\text{SiCl}_2\text{H}_2}$ is approximately 1016°C for $\Delta G = 0$. This is because the Si-Cl bond is much stronger than the Si-Cl or Ge-H bond. These calculated temperature values are heavily dependent on the bond disassociation energies and the entropy of the various materials,

which have been cited, and therefore there is some degree of error to these values. Ultimately this means that when using dichlorosilane and germane as the precursors and using much lower growth temperatures, the reaction tends to lean more towards the gas phase as opposed to the reaction phase and hence large quantities of the precursors are not used in the deposition process and are lost.

Figure 2.11 are examples of two separate studies where dichlorosilane was used a precursor to deposit silicon films on Si(001). Both studies show an Arrhenius relationship between the reciprocal of the absolute deposition temperature and growth rate at a fixed pressure and fixed mass flow ratios of dichlorosilane to hydrogen carrier gas. In both cases when the deposition temperature is low, i.e. the right hand side of the x-axis, the reaction is said to be temperature limited and the growth rate is reduced. This is due, in part, to the lack of the pyrolysis reaction in the gas phase and also insufficient enthalpy to overcome the binding energies of chlorine and hydrogen to silicon and germanium species from the surface this leads to a much higher activation energy, E_a . As the temperature is elevated, E_a reduces and the Gibbs free energy reduces thus pushing more towards the bulk phase of the system, therefore the system only becomes limited by the concentration of the precursors. Additional work by Everstey et al shows this same relationship between growth rate and the mass flow rate of the precursor [60].

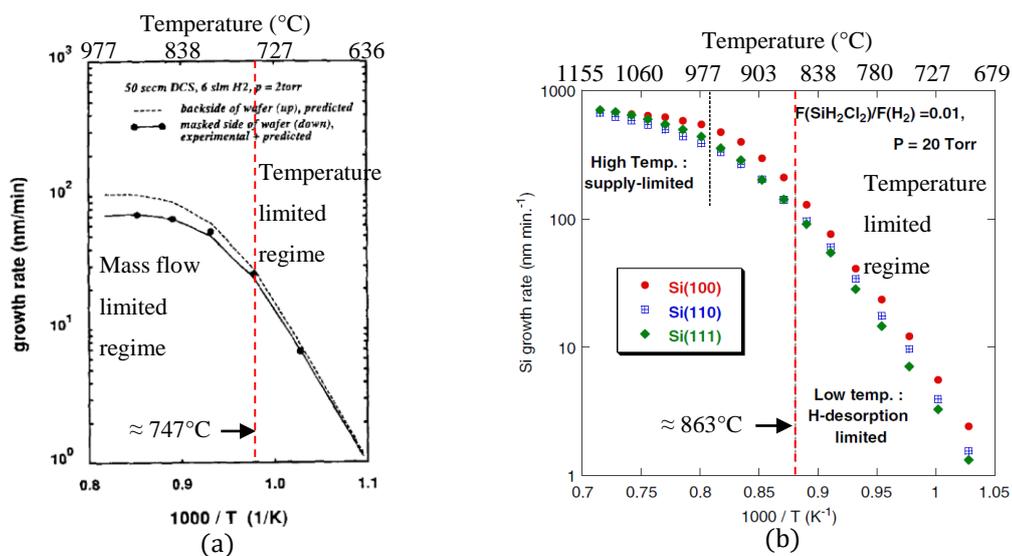


Figure 2.11: Figure (a) and (b) showing the Arrhenius function relationship between growth rate of silicon and the reciprocal of the growth temperature when using dichlorosilane as the precursor. Figure (a) adapted from Hierlemann et al [51] is of silicon deposition in a rapid thermal chemical vapour deposition reactor at

2 torr pressure and a SiH_2Cl_2 to H_2 flow rate ratio $\left(\frac{F(\text{SiH}_2\text{Cl}_2)}{F(\text{H}_2)}\right)$ of 0.025. Figure (b) adapted from Hartmann et al [61] is of deposition in an RP-CVD reactor where $\left(\frac{F(\text{SiH}_2\text{Cl}_2)}{F(\text{H}_2)}\right)$ is 0.01.

Figure 2.11 shows the effect of increasing the total pressure by 10 times and reducing $\text{SiH}_2\text{Cl}_2/\text{H}_2$ mass flow rate ratios by 2.5 times leads to the mass flow rate/temperature constrained growth transition point shifting to a higher temperature. The figure indicates how pressure and mass flow rate are inseparably linked to the transition temperature in CVD growth.

A similar situation occurs with the decomposition of Germane as seen in figure 2.12 (a) where an Arrhenius function relationship exists between germanium growth rate and deposition temperature. The transition temperature is lower than with dichlorosilane and it should be noted that UHV conditions were used in deposition.

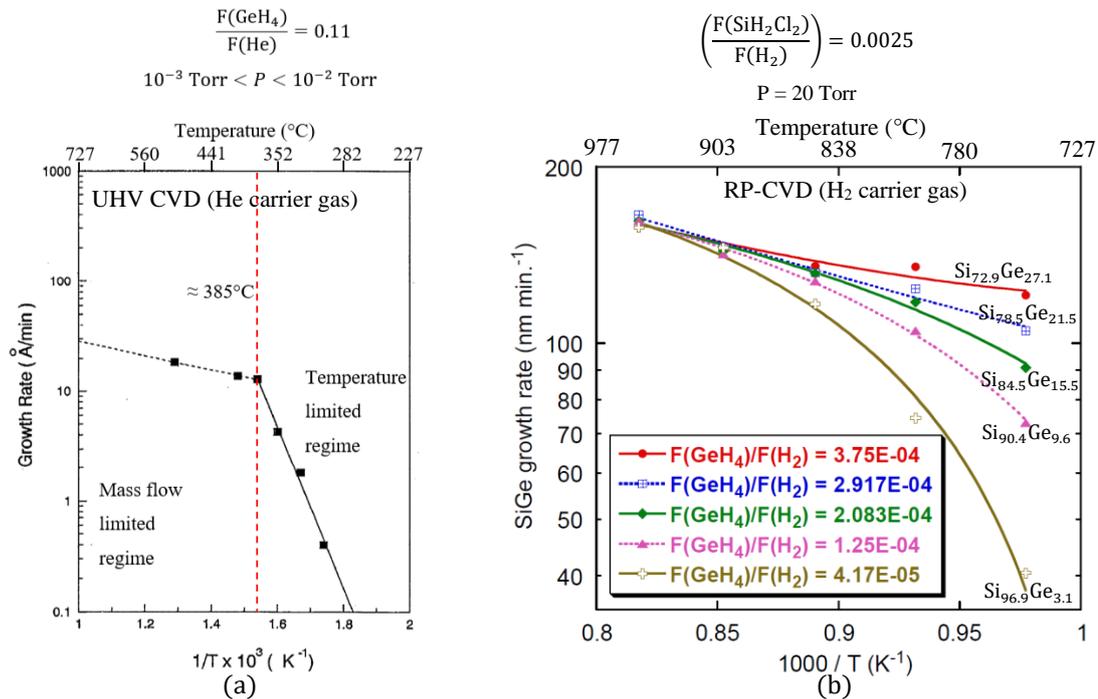


Figure 2.12: (a) Adapted from Cunningham et al [53] shows the Arrhenius function relationship between growth rate of germanium and the reciprocal of the growth temperature when using germane as the precursor. (b) Adapted from Bogumilowicz et al [62] shows the RP-CVD growth of $\text{Si}_{1-x}\text{Ge}_x$ layers with various Ge contents.

For the alloy growth of $\text{Si}_{1-x}\text{Ge}_x$ using dichlorosilane & germane as the precursors, hydrogen carrier gas and a deposition temperature of $600^\circ\text{C} < T < 900^\circ\text{C}$, the

required concentration of germanium in the alloy, x , is determined by the following relationship set by Suh and Lee [63]:

$$\frac{x^2}{1-x} = n \left(\frac{F(\text{GeH}_4)}{F(\text{SiH}_2\text{Cl}_2)} \right) \quad (\text{Equation 2.30})$$

Where, n , is a proportionality constant and is dependent on the pressure and temperature of growth. Unlike when using SiH_4 as the precursor, which has linear relationship between Ge content in the layer and the precursor flow rate ratio, the presence of Cl species causes etching of Ge from the surface as shown in figure 2.10 and equations 2.26 and 2.27 within the $600^\circ\text{C} < T < 900^\circ\text{C}$ growth temperature range. Subsequently this relationship was corroborated by Hartmann et al [61] when using RP-CVD and at 700°C growth temperature with fixed $\text{SiH}_2\text{Cl}_2/\text{H}_2$ mass flow rate ratio of 0.01 the value of n is 0.66 for Si(001) substrate and 2.24 if HCl gas is used along with H_2 carrier gas [64].

The growth rate of the $\text{Si}_{1-x}\text{Ge}_x$ epilayer is also dependent upon the GeH_4/H_2 mass flow ratio provided that the $\text{SiH}_2\text{Cl}_2/\text{H}_2$ flow rate is kept constant, as shown by figure 2.12 (b). For a $\text{Si}_{1-x}\text{Ge}_x$ layer with a fixed amount of germanium, the increase of layer growth rate with increasing GeH_4 flow rate is due to minimised hydrogen surface coverage. When Ge free sites on the surface are reduced H and Cl species on the surface cannot diffuse towards and desorb off the surface from Ge diffusion centres, which have a lower activation energy barrier than with Si surface species. Hartmann et al discovered this in two separate studies with and without additional HCl gas [64], [61].

Figures 2.11 (a) & (b) and 2.12 (a) & (b) show that the growth rate of Si and Ge films using CVD techniques are of the order of 10's if not 100's of nm/min, depending on the growth temperature and pressure. In this investigation the growth rates of the layers, particularly $\text{Si}_{1-x}\text{Ge}_x$ layers are calibrated for particular temperatures before the actual heterostructures are grown.

2.4.2. Solid Source Molecular Beam Epitaxy (SS-MBE).

Solid source molecular beam is the other epitaxy technique used in this project. This technique was used for the deposition of AlSb and InSb onto RP-CVD grown Ge buffer layers on Si(001) in chapter 7 of this project. Unlike RP-CVD, SS-MBE growth takes place in UHV conditions at approximately 10^{-9} torr. The solid materials, e.g. Aluminium, Antimony and Indium are brought into Knudsen effusion cells and then vaporised at high temperature. Since the chamber is evacuated and there is no carrier gas, the elements in their gaseous form will have a high mean free path, λ . The gaseous elements are then transported over the substrate which is heated locally from the underside, where the depositing material reacts and condenses on the substrate to form an epitaxial film. The relationship between λ , the temperature, T, diameter of molecules and atoms, D, pressure, P, and Boltzmann constant, k_B is [65]:

$$\lambda = \frac{k_B T}{\frac{1}{22\pi P D^2}} \quad (\text{Equation 2.31})$$

The SS-MBE tool used in this project is a Gen II SS-MBE and a schematic of the system is shown in figure 2.13. As mentioned in the RP-CVD section, the mass transport velocity is directly proportional to the total pressure in the chamber, therefore the advantage of using MBE is that the layer grows more homogeneously on the surface but the disadvantage is that the growth rate is dramatically reduced. For UHV conditions, the growth rate is dependent on the substrate material, epilayer material and growth temperature. For example, if growing GaAs on a GaAs substrate at a temperature of between 500-600°C then the typical growth rate is approximately 16nm/min.

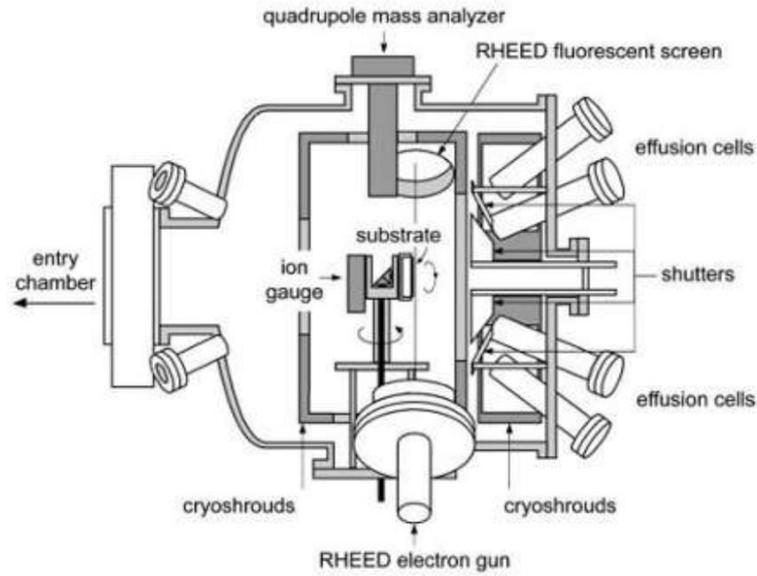


Figure 2.13: Cross sectional schematic of the Gen II SS-MBE system used to grow AlSb and InSb epilayers [66].

When carrying out epitaxy of III-V materials, such as GaAs, using MBE previous studies have shown that opening the shutters to allow a particular source to be exposed to the substrate needs to be carried out in a particular order to ensure uniform growth. Previous studies in Arsenic growth on Si(001) has shown that it forms a 2×1 reconstruction on the surface of the substrate by the formation of chemically stable As-As dimers [67]. In another example when depositing a bilayer of GaAs on Si(111), if As is deposited first it substitutes the top most layer of silicon and forms a bulk termination configuration. Whereas if Ga is deposited first a $\sqrt{3} \times \sqrt{3}$ surface reconstruction takes place. If Ga is deposited after As, full Gallium monolayer coverage occurs [68].

2.4.3. Adatom transport on the substrate surface and dimer bond energies

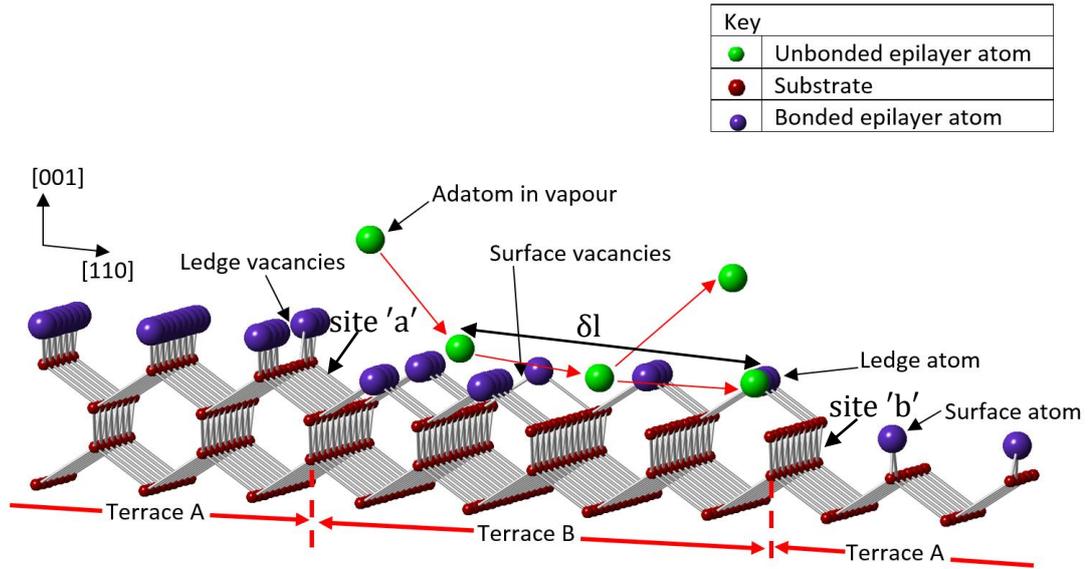


Figure 2.14: Diagram showing adatom (purple) transport and growth on substrate surface (red). (Adapted from Hudson) [69].

With desorption of hydrogen from the surface, the top silicon atoms covalently bond with an adjacent surface atom to form 2x1 pairs known as dimers. Figure 2.14 shows adatom transport on the surface of a substrate with steps and terraces on an unreconstructed surface (1x1). The distance from terrace A to terrace B can be an arbitrary value and can be dependent on temperature altered surface re-construction or intentional wafer offcut. Site 'a' is the step between terrace A and terrace B where the dimer bonds between substrate species are parallel to the terrace surface and site 'b' are where the dimer bonds between substrate species are perpendicular to the terrace surface. As the adatom species in vapour form moves along the substrate surface with kinetic energy provided by the elevated temperature, it can either be absorbed onto the substrate through a vacancy or re-enter the vapour. The parameter that determines this is known as the migration length, δl and it is governed by a number factors including growth temperature, adatom species and planar dangling bond density to name a few. When δl is greater than the terrace width, 2 dimensional planar growth occurs via an extension of these terraces. Various types of substrate vacancies exist for the adatoms to bond to such as: (and listed in order from most preferential to least) bulk vacancies, surface vacancies and ledge vacancies.

In figure 2.14, the step free energy can be taken as the difference between the surface free energy, with and without a step. Xie et al concluded that there is an energy

variation between the bonds on terrace A and terrace B [70]. Xie discovered from simulations and experimental growth of pseudomorphic SiGe (of varying Ge content) that the step energy for bonds on terrace A were approximately 44meV per ledge atom, whilst those on terrace B have an energy of <5meV per ledge atom. Therefore, it is energies associated with bonding on terrace A that is the limiting factor in determining the surface free energies of an epilayer. Xie also determined that for a strain magnitude of 2%, the energy of terrace A is $\approx 100\text{meV}$ per ledge atom if the layer is under tensile strain and $\approx -150\text{meV}$ per ledge atom if the layer is under compressive strain. Compressive strain lowers the surface free energy and as will be explained in section 2.4.4, can cause undulations to increase the surface free energy.

2.4.3.1. Growth on offcut substrates

Generally, in the electronics industry, devices are manufactured on silicon wafers that have been cut from a Czochralski ingot at 0° axis (on axis) from the centre. This is so as to ensure that minimal terraces and steps are present. From figure 2.14, it has been shown that the presence of single atomic steps allows two different dimer orientations to be present in the substrate. In which case, site 'a' can be considered as the (111) plane and site 'b' can be considered as the (110) plane. For an on axis wafer, steps and terraces can occur in any direction, meaning that different additional crystallographic planes can emerge. Carrier mobility has been observed to be heavily dependent on crystallographic orientation, as shown by Takagi et al [71] who found orientation dependent surface roughness induced scattering of electrons in Si MOSEFT'S and Fischetti et al [72] who found a higher hole mobility in Si channels along the [110] direction. This is of particular importance in the CMOS industry, which is currently at 10nm processing technology, and so ensuring uniformity in conduction properties from device to device on a single wafer is paramount. However, for other sectors of the electronics industry, such as the photovoltaics industry the presence of terraces and steps is not such a large concern.

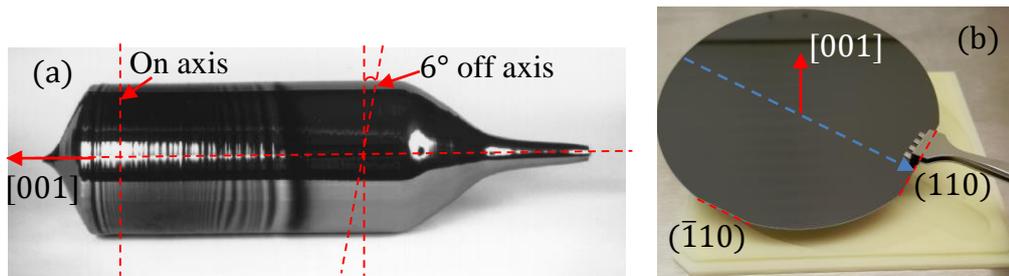


Figure 2.15: (a) Czochralski silicon (001) single crystal ingot with dashed lines showing on axis wafers to be and 6° off axis (not an accurate angle on the image) wafers to be cut from the ingot [73]. Figure (b) shows a 100mm diameter 6° off axis Si(001) wafer, with the marked flats indicating the (110) and $(\bar{1}10)$ planes. The blue arrow indicates the direction along which surface steps lie due to cutting the wafer at an angle from the ingot. All of the Si(001) substrates used in this project, both on and 6° off-axis were 100mm diameter and 525 μ m thick.

The process of cutting a wafer from an ingot at any angle other than 0° creates steps and terraces on the surface with a greater propensity and step height than on 0° axis wafers (figure 2.15). Figure 2.16 shows a diagram of an on axis Si(001) wafer with an offcut tolerance of $\pm 0.5^\circ$. Single atomic steps creating double domains, are seen in the figure as indicated by the two terraces and the green and blue coloured atoms at the edge. The diagram is an exaggeration in that the length between terraces would be of the order of at least several microns, if not more [49], however for the purposes of showing how double domains exist on an on axis wafer, the terraces have been drawn much closer together.

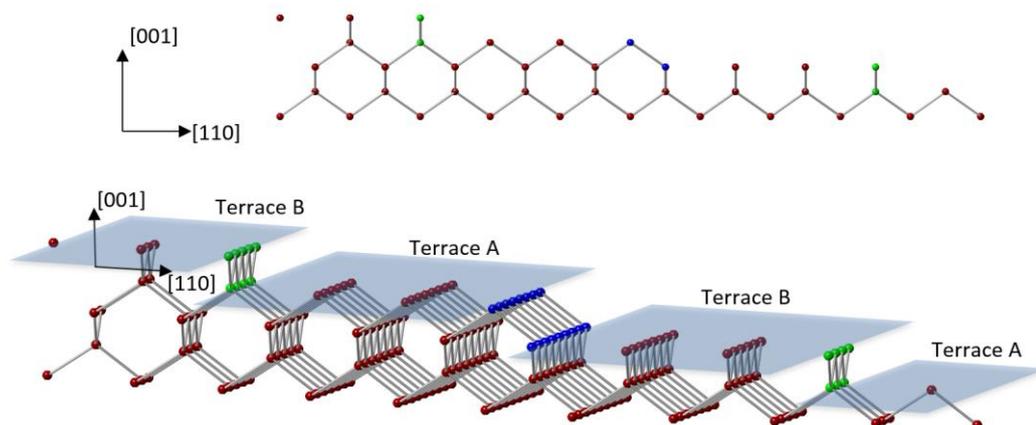


Figure 2.16: Double domain of an on axis Si(001) substrate, created by single atomic steps indicated by terrace A and terrace B, where the dimer orientation changes from being parallel to the step edge (green atoms) to perpendicular to the step edge (blue atoms).

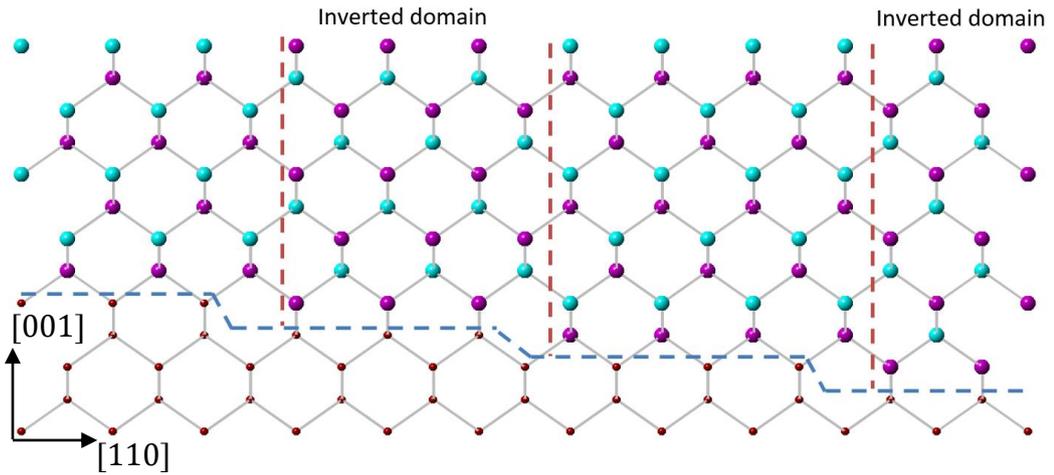


Figure 2.17: example of III-V (pink and blue atoms) material grown on on-axis Si(001) (red atoms). The pink atoms are the group V anions and the blue atoms are the group III cations. The presence of the double domain means zinc blende crystals growing on adjacent terraces would have to rotate by 90° to ensure correct bond angles are maintained in the grown fcc lattice.

Figure 2.17 shows an example of a zinc blende crystal grown on an on axis Si(001) substrate with double domains created by single atomic steps. The process of ensuring that the correct bond angles are maintained in the layer between terraces is through an inversion symmetry operation i.e. the III and V atoms swap positions in the unit cells. This means that the sub lattice shown in figure 2.3 (a) grown on terrace A would have to become the sub lattice in figure 2.3(b) when growing on terrace B. Charge neutrality is not maintained at the boundaries of the opposing domains since a cation from a group III atom would ordinarily have neutralised the charge from the anion from a group V atom in a single domain layer. Figure 2.18 are TEM image examples of inversion domains in GaP on $\text{Si}_{0.85}\text{Ge}_{0.15}/\text{Si}(001)$ virtual substrates. Inversion domains have historically been incorrectly referred to as anti-phase domains [74], however anti-phase domains are comprised of planes of incorrect nearest neighbour bonds whereas inversion domains suggest that the entire lattice has undergone an inversion symmetry operation. Inversion domain boundaries can affect the optical and electronic properties of the III-V layer, such as localising the valance band maximum on [110] inversion domain planes in GaP and trapping charge carriers [75].

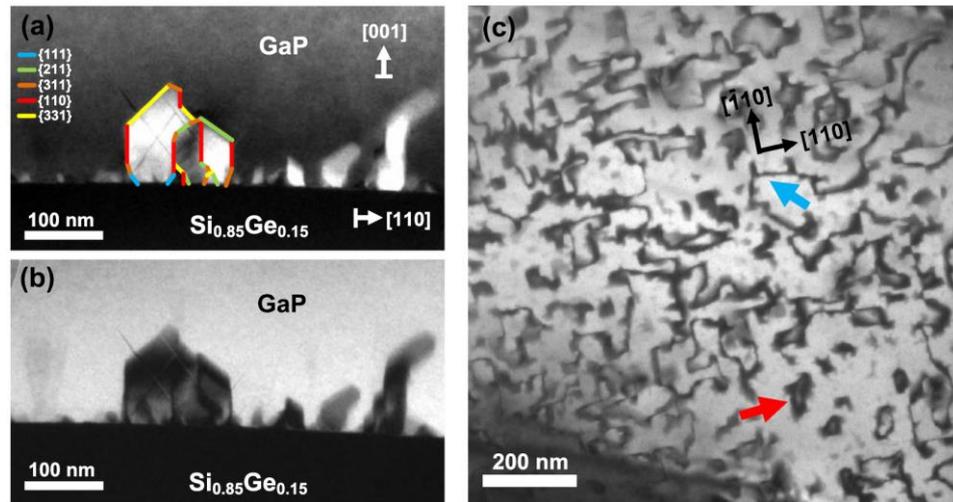


Figure 2.18: adapted from Skibitzki et al. [76] Cross sectional TEM images of 270nm GaP grown on $\text{Si}_{0.85}\text{Ge}_{0.15}/\text{Si}(001)$. Figure (a) is a $00\bar{2}$ dark field HR-XTEM, figure (b) is $00\bar{2}$ dark field and (c) $00\bar{2}$ dark field plan view image. The figures show the presence of inversion domains generated in the GaP layer as shown by the blue and red arrows in figure (c).

From the work carried out by Herbert Kroemer it was shown that by using an offcut (001) substrate and pre-annealing of the substrate for the intention of growing GaAs, has the effect of minimising inversion domains in the GaAs layer [77]. This was later corroborated by Ting and Fitzgerald with the high quality growth of GaAs on linearly graded $\text{Ge}/\text{Si}_{1-x}\text{Ge}_x/6^\circ$ off axis $\text{Si}(001)$ virtual substrates [74].

The goal behind off cutting a wafer from an ingot along the [110] direction and pre-annealing it is to create a (001) surface with double atomic steps as shown in figure 2.19. By doing so, a single domain is created on the substrate, which has even been shown to be effective when using $\text{Ge}(001)$ substrates for growth of GaAs. [78]. Additional pre annealing of the substrate causes step bunching to occur i.e. the terrace lengths become shorter, this has the effect of minimising inversion domains because shorter diffusion lengths of the adatoms enhances inversion domain annihilation mechanisms, but also because step bunching has the effect of further creating double atomic steps [79].

Figure 2.20 shows a III-V epilayer grown on a substrate with double atomic steps. As mentioned earlier in the MBE section the propensity is for group V atoms to be adsorbed on to the $\text{Si}(001)$ surface to form a stable group V-group V dimer, hence in both figures 2.17 and 2.20 the group V atoms are deposited first onto the $\text{Si}(001)$

substrate. As mentioned before Arsenic will blanket cover the (001) surface in a 2x1 orientation but each As atom has a lone pair of electrons instead of a dangling bond as in Si. This means that the As layer (or P or Sb) layer on the substrate will decrease the net surface energy therefore allowing Volmer-Weber growth of the subsequent III-V layer, as will be explained later in this work [74].

It is almost impossible to say if all inversion domains are eliminated in a III-V epilayer grown on Si(001) since there is no control over the density of double atomic steps created. The offcut angle is also disputable and it is currently not clear if the density of double atomic steps is greater in 6° offcut Si(001) than in 4° offcut Si(001) even after an annealing step. Though it is clear with Si(001) that too high an annealing temperature and duration e.g. 1100°C for 10mins causes surface reconstruction and single atomic steps [48]. Some investigations have used 4° offcut Si(001) wafers to grow III-V nitride epilayers [80] and InP epilayers [81]. Other investigations have used 6° offcut Si(001) substrates such as Grassman et al [82] where a 760°C anneal in UHV of the substrate was carried out followed by homoepitaxial growth of 20nm Si to bury any surface contamination before MBE growth of GaP. Another investigation carried out by Leitz et al on linearly graded Si_{1-x}Ge_x/6° off axis Si(001) virtual substrates showed temperature dependence in threading dislocation density glide in graded layer and saturation in threading dislocation reductions at higher growth temperatures [83].

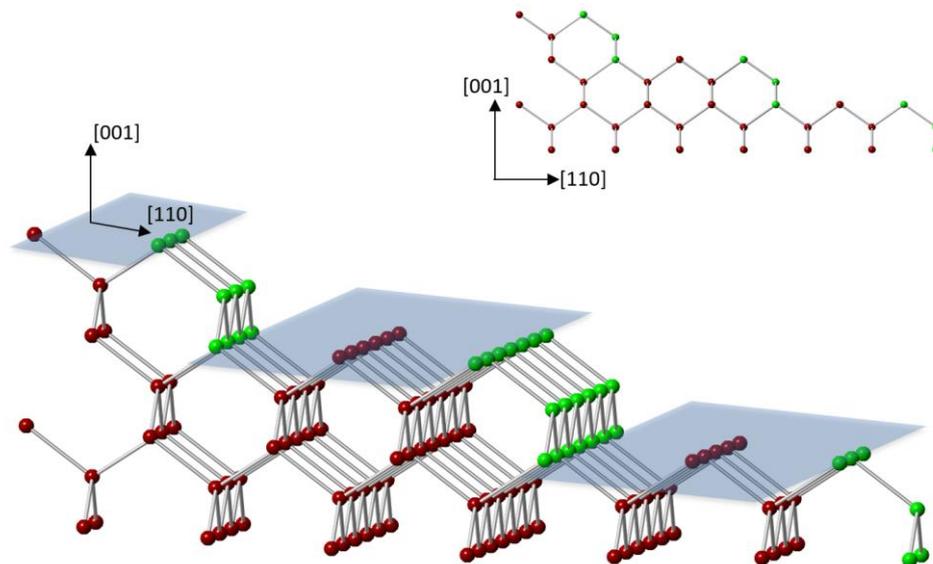


Figure 2.19: Single domain surface of an off-axis Si(001) substrate as shown by the green silicon atoms and terrace steps (in blue). The double monolayer steps allows the dimer bonds to maintain their orientation. This means that for zinc-blende structure grown on this particular substrate only one sub lattice can form.

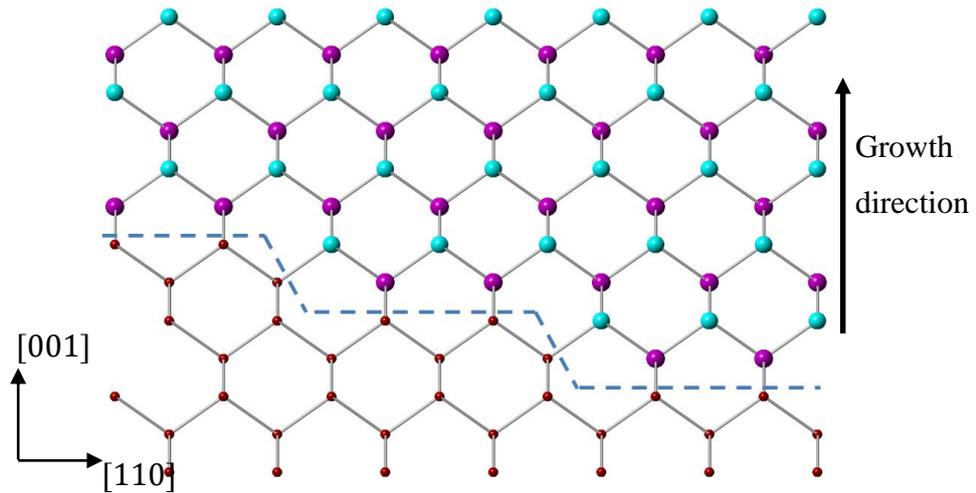


Figure 2.20: Example of III-V (pink and blue atoms) material grown on off-axis Si(001) (red atoms). The double monolayer steps allows the dimer bonds to maintain their orientation. This means that for zinc-blende structure grown on this particular substrate only one sub lattice can form. Here again the group V anions are in pink and the group III cations are in blue.

For an on-axis substrate with $\pm 0.5^\circ$ tolerance, the average terrace width is assumed to be of the order of several microns. Figure 2.21 (a) is a HR-XTEM image taken in this study at lattice resolution of a typical 6° off-axis Si(001) substrate. Figure 2.21 (b) is of the same image but compressed laterally where the pairs of silicon atoms are seen as horizontal streaked lines and the substrate surface has a slope indicating steps.

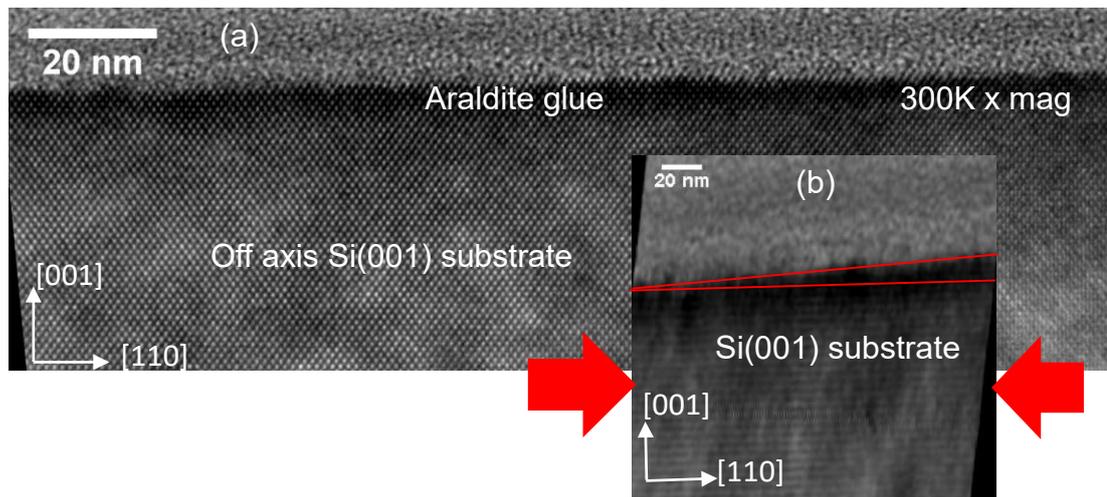


Figure 2.21: High resolution cross sectional TEM image of a Si(001) substrate offcut toward the [110] direction at a 6° angle.

The AFM tips used in this investigation are of the order of $\geq 10\text{nm}$ in width and silicon oxidises rapidly in air. Therefore, it was not possible to resolve terrace widths on the

offcut substrate surface using AFM in this study and it is assumed that for a 6° offcut substrate the terrace widths are $\leq 1\text{nm}$.

Figure 2.22 shows the different dangling bond densities for various silicon planes. From figures 2.19 and 2.20 it is clear that for an offcut wafer, with a single domain the [110] and [111] planes are partially made available for growth however it is reasonable to assume that the process of off cutting and high temperature surface treatment may also make additional planes available on the surface other than the (110) and (111) planes as seen in figure 2.23(a).

Plane	(001)	(119)	(113)	(111)	(110)
Dangling bonds surface density	$\frac{4}{a_{\text{Si}}^2} = A$	$\frac{8}{9}A$	$\frac{4}{3\sqrt{3}}A$	$\frac{1}{\sqrt{3}}A$	$\frac{1}{\sqrt{2}}A$
Normalised density of dangling bonds	1	0.89	0.77	0.58	0.71
r_{hkl} (Si 850°C)	1	0.67	0.41	0.28	0.28
r_{hkl} (Si 650°C)	1	0.84	0.73	0.62	0.70
r_{hkl} (Si 600°C)	1	0.89	0.82	0.70	0.78

Figure 2.22: Table showing dangling bond densities for various planes of silicon, normalised to Si(001) and the growth rate anisotropy, r_{hkl} , of silicon deposited at 850°C, 650°C and 600°C. Adapted from Pribat et al [84].

The growth rate anisotropy, r_{hkl} , is given as a growth rate ratio of the considered plane, GR_{hkl} , to the growth rate of the (001) plane, GR_{001} , via the following relationship: $r_{\text{hkl}} = \frac{\text{GR}_{\text{hkl}}}{\text{GR}_{001}}$. From the work carried out by Pribat et al [84] where pure silicon and constant composition $\text{Si}_{1-x}\text{Ge}_x$ films were grown on etched Si(001) substrates it was seen that $\text{GR}_{111} < \text{GR}_{113} < \text{GR}_{001}$. Moreover, it was determined that the Ge content, x , on tilted planes was lower than on the (001) surface. Figure 2.23(b) shows how the thickness of a constant composition $\text{Si}_{1-x}\text{Ge}_x$ film varies across the non-uniform surface.

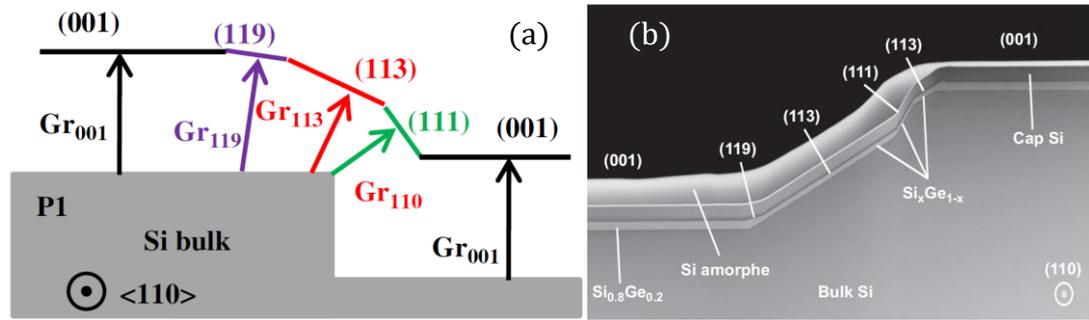


Figure 2.23: Adapted from Pribat et al [84]. Figure (a) shows a Si(001) substrate with terraces & steps and the positions of various planes. Figure (b) is a STEM image taken by Pribat et al and shows how the thickness of a $\text{Si}_{0.8}\text{Ge}_{0.2}$ + Si cap + amorphous Si film grown over a pattern etched substrate varies with respect to the (001) surface plane.

The adatom adsorption process and subsequent growth rate in hetero-epitaxy is heavily dependent on the anisotropic density of dangling bonds on the substrate surface since the sticking coefficient of adatoms will vary for different planes with different dangling bond densities. As another example, a study carried out by Hartmann et al in 2006 of RP-CVD grown Ge and $\text{Si}_{1-x}\text{Ge}_x$ on Si(001), Si(110) and Si(111) showed that the growth rate on Si(001) is the fastest amongst all three planes at the same growth temperature [61]. It was deduced that the activation energy in both the mass flow limited and temperature limited growth regimes, was lower for Si(001) than for the other two planes. With $\text{Si}_{1-x}\text{Ge}_x$ growth, it was discovered that for a constant mass flow rate ratio of the precursors, the Ge content in the layer (determined by equation 2.30) was found to be lower for the (110) and (111) planes.

2.4.4. Epitaxial growth modes

If growth is not kinetically inhibited, growth modes are determined by thermodynamics. The thermodynamic definition of free energy is the capacity for a system to do work. The control of interface and surface free energies allows the layer to be grown in a thermodynamically stable manner whilst mitigating strain caused by

lattice mismatch [85] and this is what determines how the epitaxial layer forms on the substrate.

The substrate free energy per unit area is defined as γ_s , the epilayer free energy per unit area is defined as γ_l , the epilayer/substrate interface free energy per unit area is defined as γ_i and finally the epilayer strain energy per unit volume is defined as σ_l . For an epilayer surface area, A_l , substrate surface area, A_s , and epilayer thickness, h , the free energy inequalities are:

$$\gamma_s A_s > (\gamma_l A_l) + (\gamma_i A_s) + \sigma_l A_l h \quad (\text{equation 2.32})$$

$$\gamma_s A_s < (\gamma_l A_l) + (\gamma_i A_s) + \sigma_l A_l h \quad (\text{equation 2.33})$$

For an unstrained layer, e.g. homoepitaxy, $\sigma_l = 0$. If equation 2.32 is satisfied then the epilayer grows in a two-dimensional manner known as Frank Van-der Merwe mode (figure 2.24 [86]) and $A_l = A_s$. Alternatively if equation 2.33 is satisfied, then the unstrained epilayer grows by 3-D island formation, (figure 2.25), known as Volmer-Weber growth [87] and $A_l > A_s$.

If there is lattice mismatch strain between the bulk epilayer and substrate (e.g. heteroepitaxy), then $\sigma_l \neq 0$ and the layer will either grow via the Volmer-Weber mode from the start or initially grow via the Frank Van-der Merwe mode and then transition to 3-D mode at some critical thickness depending on the lattice mismatch strain, in a mode known as Stranski-Krastanov (figure 2.26) [88].

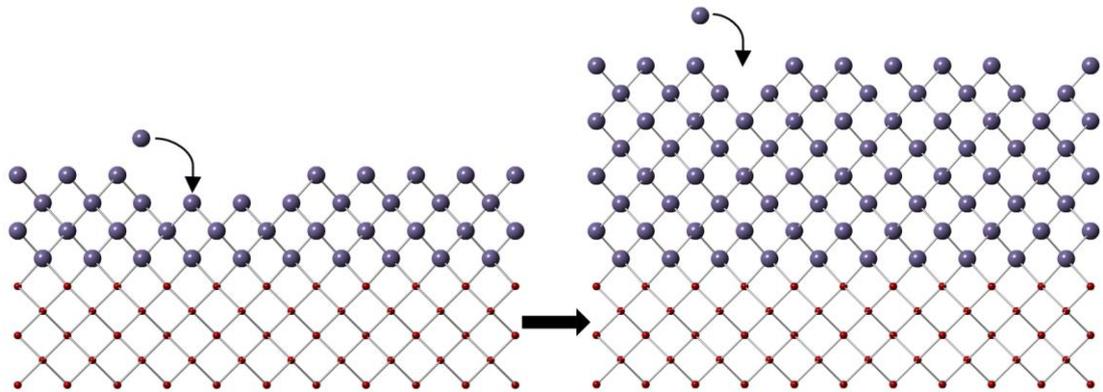


Figure 2.24: Frank-van der Merwe growth mode of epitaxial adatoms onto a substrate.

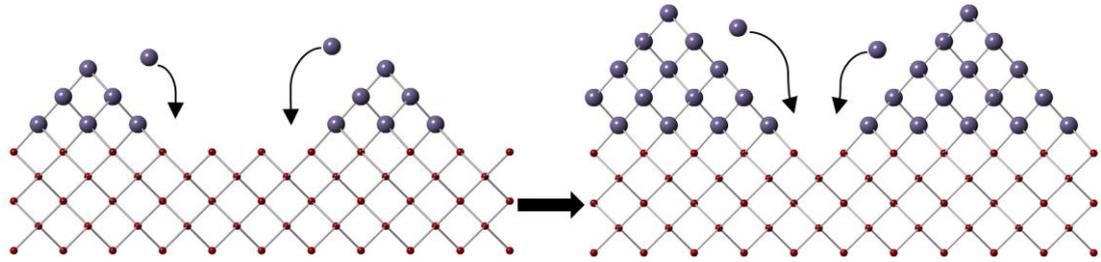


Figure 2.25: Volmer-Weber growth mode of epitaxial adatoms onto a substrate.

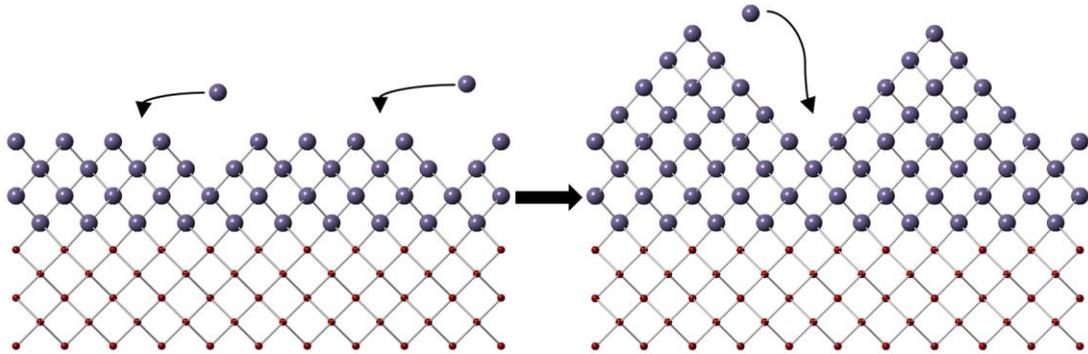


Figure 2.26: Stranski-Krastanov growth mode of epitaxial adatoms onto a substrate.

2.5. Strain relaxation and the formation of defects in FCC diamond and zinc blende epilayers.

2.5.1. Definitions of Strain and relaxation

In hetero-epitaxy since the substrate and epilayer are of two different materials, with different bulk crystal lattice constants, there may be some degree of lattice constant

mismatch between the substrate epilayer materials. The lattice mismatch, f , is defined as follows:

$$f = \frac{a_{\text{bulk epilayer}} - a_{\text{substrate}}}{a_{\text{substrate}}} \quad (\text{Equation 2.34})$$

Where: $a_{\text{bulk epilayer}}$ is the bulk unstrained lattice constant of the epilayer crystal as it would exist naturally and $a_{\text{substrate}}$ is the bulk unstrained lattice constant of the substrate crystal. With Si(001) and Ge, there exists a 4.18% lattice mismatch between the two bulk crystals with respect to the Si(001) substrate. For AlSb and Si(001) there exists a 12.97% lattice mismatch and InSb and Si(001) there exists a 19.30% lattice mismatch with respect to the Si(001) substrate.

A lattice parameter difference between epilayer and substrate creates strain in the epilayer if it becomes tetragonally distorted to match its in-plane lattice parameter, a_x , to the substrate lattice parameter, as shown in figure 2.27. With SiGe alloys, since the occupation of silicon and germanium atoms in the lattice is random, the strain is biaxial. This means that equal amounts of distortion occur along [100] and [010] directions and hence transforming the a_x and a_y lattice parameters (in-plane) equally. With binary III-V compounds such as InSb, AlSb and GaAs, since there are 4 atoms of each element per unit cell, again the strain is biaxial along lattice parameters, a_x and a_y .

For an epitaxial layer under strain, to calculate the lattice parameter perpendicular to the [100] and [010] directions i.e.: the out of plane lattice parameter, $a_z(a_{\perp})$, along the [001] direction, the following equation is used (where C_{11} and C_{12} are the elastic moduli of the material):

$$a_z = a_{\text{bulk epilayer}} + \frac{2C_{11}}{C_{12}} (a_{\text{bulk epilayer}} - a_x) \quad (\text{Equation 2.35})$$

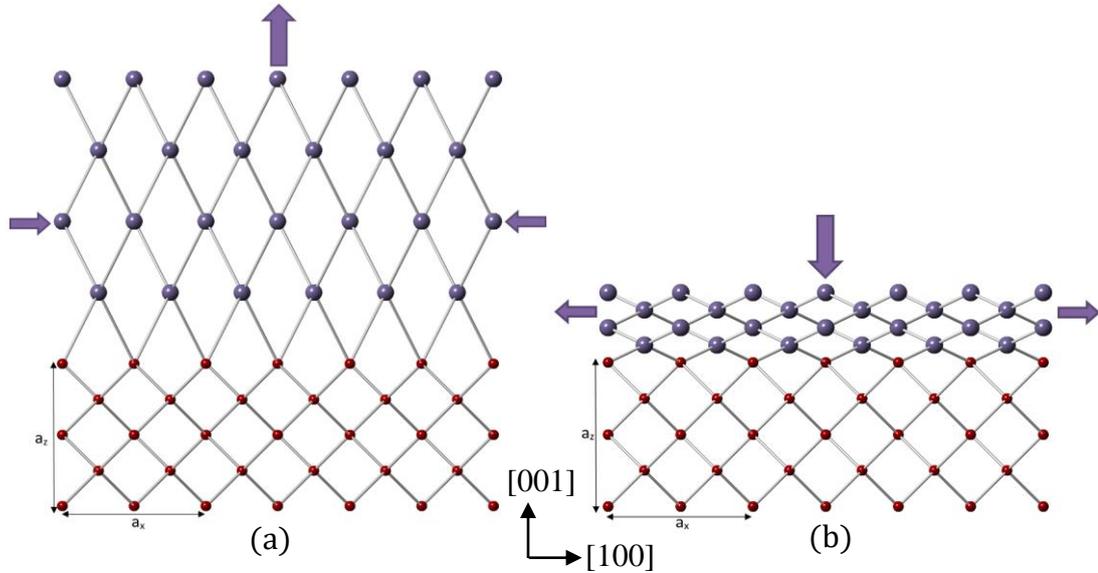


Figure 2.27: Diagrams showing epitaxial layer atoms (in purple) under compressive strain (a) and under tensile strain (b), with respect to the substrate (in red).

As the thickness of the lattice mismatched epilayer increases, the strain energy in the epilayer increases also, until strain relaxation occurs through the formation of defects in the crystal and surface roughening. The strain is defined in its classical sense as the extension of the material divided by natural length hence:

$$\varepsilon = \frac{a_{\parallel} - a_{\text{bulk epilayer}}}{a_{\text{bulk epilayer}}} \quad (\text{Equation 2.36})$$

Where a_{\parallel} is the in-plane lattice parameter of the epilayer and therefore for diamond and zinc blende crystals, $a_{\parallel} = a_x = a_y$. If $a_{\parallel} < a_{\text{bulk epilayer}}$ then ε is negative and therefore the layer is under compressive strain as shown in figure 2.27(a). If $a_{\parallel} > a_{\text{bulk epilayer}}$ then ε is positive and therefore the layer is under tensile strain as shown in figure 2.27(b). The relaxation in the layer is defined as the deviation of a_{\parallel} from the substrate lattice parameter with respect to the deviation of $a_{\text{bulk epilayer}}$ from the substrate lattice parameter, given by the following equation:

$$R = \left(\frac{a_{\text{substrate}} - a_{\parallel}}{a_{\text{substrate}} - a_{\text{bulk epilayer}}} \right) \times 100 \quad (\text{Equation 2.37})$$

For $a_{\text{substrate}} < a_{\text{bulk epilayer}}$, if the relaxation is greater than 100% then the layer is under tensile strain. If the relaxation is less than 100% then the layer is under compressive strain.

2.5.2. Surface roughening

For a strained epilayer, relaxation can occur via the surface roughening (based on Stranski-Krastanov growth, described in section 2.4.4) or the formation of dislocations [89]. Depending on the degree of misfit strain; islands and grooves on the epilayer surface can occur as a means of elastic strain relaxation by increasing the surface area, A_1 to reduce the bulk strain energy per unit volume σ_1 in equation 2.33 [90]. This can be mathematically explained via the relationship between the roughening force and proportionate displacement given by a Green's function that is used to explain the strain energy reduction caused by elastic strain relaxation.

Previous studies have shown that for epilayers of low misfit to the substrate the dominant strain relaxation mechanism is homogenous dislocation nucleation however at high misfit, surface roughening is dominant. Surface roughening has the effect of increasing the localised lattice constant at the top of the island and increasing the stress in the grooves where the energy barrier for the nucleation of dislocations is lower [91]. Once strain has been relieved by dislocations the surface will return to being smooth, as the layer thickness increases, to reduce the surface free energy term, $(\gamma_1 A_1)$.

σ_1 is described on a relative energy scale. For an epilayer under compressive strain the sign of σ_1 is negative. Considering equation 2.32, for a layer under compressive strain that has reached the critical thickness, h , for elastic strain relaxation, a decrease in $\sigma_1 h$ occurs which accompanies an increase in $\gamma_1 A_1$. Depending upon the reduction of σ_1 and the accompanying increase in A_1 , equation 2.32 will transition to equation 2.33, causing the surface to roughen. For a layer under tensile strain, the sign of σ_1 is positive and therefore $\gamma_1 A_1$ cannot increase to minimise the total free energy in the system.

Finally, roughening is temperature dependent. Previous studies have found that at low temperature equilibrium the epilayer is faceted. Higher temperatures reduce the

anisotropy of surface free energy [92] and eliminate faceting. This means that at higher growth temperatures low misfit strain causes greater surface roughness. Strain also affects the stability of different facets, and makes the minimum energy shape, size dependent.

2.5.3. Defects.

When an epilayer undergoes plastic strain relaxation from lattice parameter mismatch to the substrate, it does so by forming defects in the crystal. These defects can be zero, one, two or three dimensional. A zero dimensional defect is either a vacancy (missing atom) or an interstitial (additional atom) in the epilayer. A three dimensional defect occurs when volumes of the epilayer separate into individual crystal grains and precipitates. For diamond fcc and zinc blende crystals, the more common strain relieving defects are one dimensional defects, i.e. dislocations, and two dimensional defects, i.e.: stacking faults, or microtwins.

2.5.4. Dislocations

A dislocation is defined as being a one dimensional line defect in a crystal that separates planes of atoms, the movement of which causes plastic deformation. The Burgers vector describes the magnitude and direction along which slip occurs between planes of atoms in the crystal. The Burgers vector is determined by creating a closed vector circuit in an atom to atom path around a dislocation free region of the crystal and then constructing an identical closed vector circuit around a region where a dislocation exists. The additional vector required to complete the circuit is known as the Burger's vector, \underline{b} and when it is equal to a lattice translation vector, it is known as a perfect dislocation.

There are two main types of dislocations: an edge dislocation and screw dislocation. In an edge dislocation, the Burgers vector is perpendicular to the dislocation line, \underline{u} , which is the line along which the chemical bonds have been broken as shown in figure 2.28. As is seen in figure 2.28 (a) an edge dislocation can be treated as when an extra half plane of atoms is inserted into the lattice therefore the deflection and distortion of

the crystal is localised around the dislocation line and its effects on the crystal reduces with increasing distance from it.

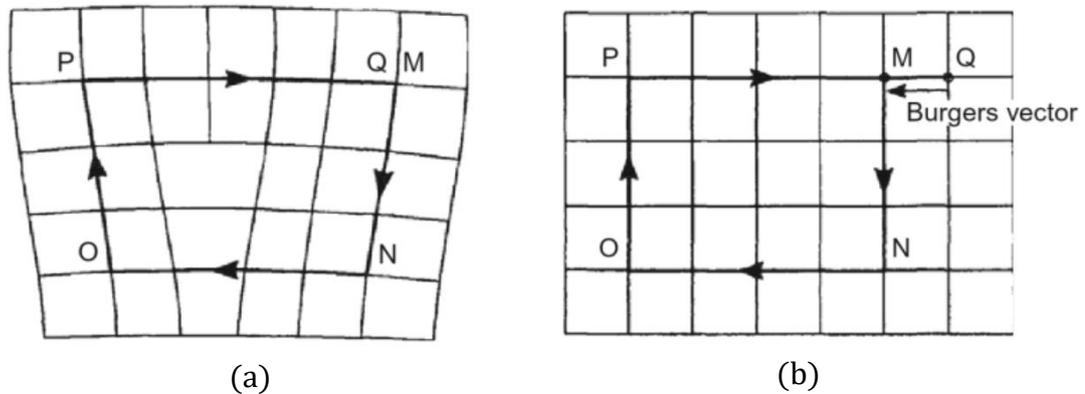


Figure 2.28: (a) Burgers circuit around an edge dislocation: [MNO PQ] and (b) equivalent burgers circuit in a dislocation free crystal [MNO P]. The outstanding vector required to close the circuit in figure (b), [MQ], is known as the burgers vector. Taken from Hull and Bacon[30].

A screw dislocation is one where the dislocation line is parallel to the Burgers vector and can be treated as a crystal being displaced either side of a line sense, helicoidally like in a spiral staircase as shown in figure 2.29.

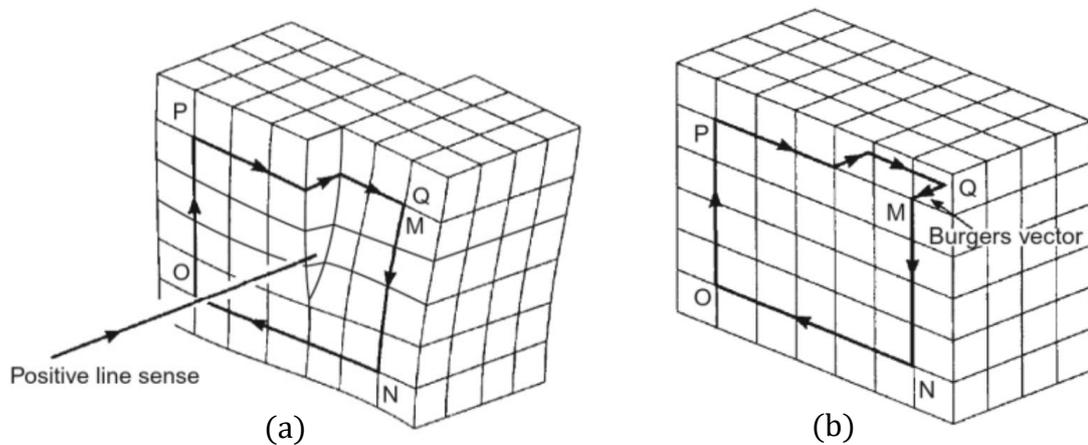


Figure 2.29: (a) Burgers circuit around a left-hand screw dislocation with a positive line sense: [MNO PQ] and (b) equivalent burgers circuit in a dislocation free crystal [MNO P] with the burgers vector shown as [MQ]. Taken from Hull and Bacon [30].

The most common misfit dislocation in SiGe layers are 60° misfit dislocations, which have a Burgers vector, $\underline{b}_{60} = \frac{a}{2} \langle 011 \rangle$. This type of dislocation forms an angle of 60° to the misfit dislocation line direction, \underline{u} . \underline{u} lies along the $\langle 011 \rangle$ directions in (001) layers because the $\langle 011 \rangle$ directions have the closest packed atoms in FCC diamond

and zinc blende crystals. Slip involves a row of atoms moving past one another and occurs on the planes which have the lowest Peierls energy barrier [93]. These are the $\{111\}$ planes because they have the highest atomic packing density. Figure 2.30 shows a $[110]$ misfit dislocation line and the 60° misfit dislocation Burgers vector is $\frac{a}{2}[011]$.

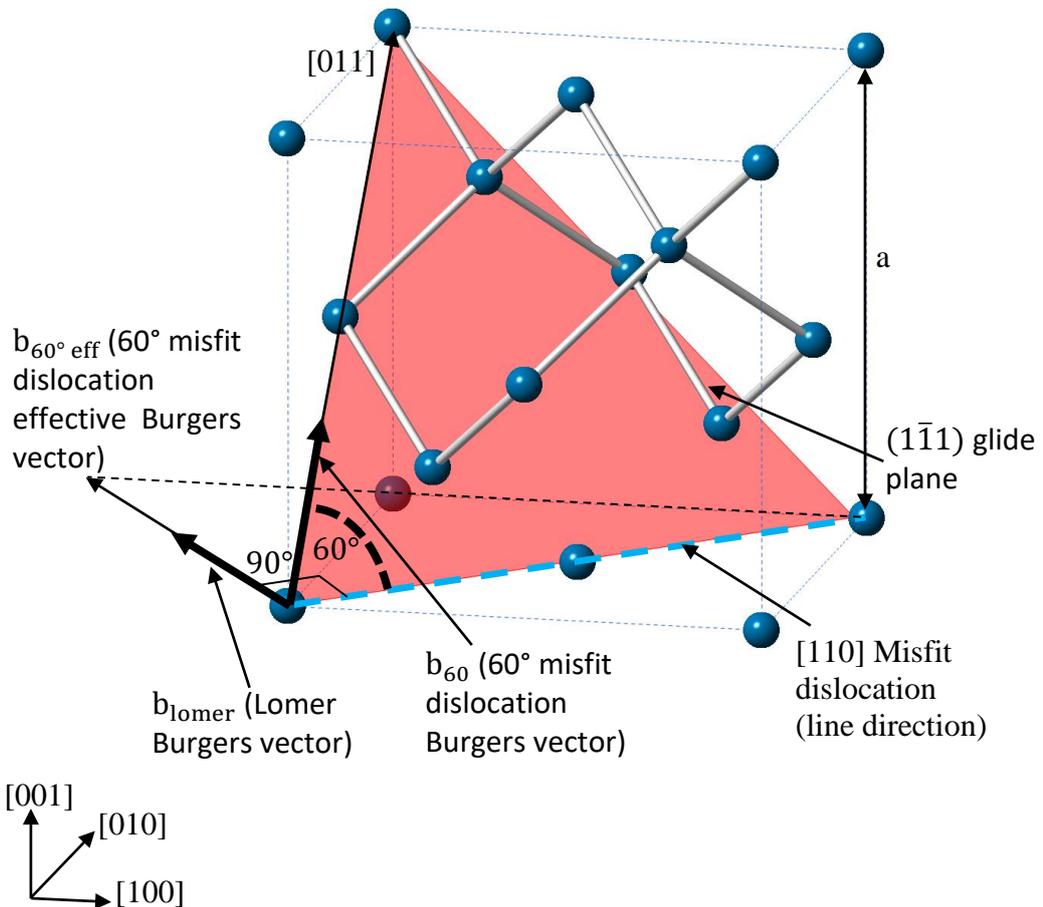


Figure 2.30: Vector diagram showing: Burgers vector and line direction for a 60° misfit dislocation and 90° Lomer dislocation in a FCC diamond (or zinc blende) crystal. The $(\bar{1}\bar{1}\bar{1})$ glide plane is the same as the $(\bar{1}\bar{1}\bar{1})$ glide plane except the normal vector is pointing down instead of up.

Another type of dislocation that can occur, is a pure edge dislocation at 90° to the $\langle 011 \rangle$ planes, known as a Lomer dislocation. Lomer dislocations occur when there is high mismatch, thick layers and also annealed layers [94]. They can also occur due to the blocking of 60° misfit dislocation glide. They have a Burgers vector, $\underline{b}_{\text{Lomer}} = \frac{a}{2} \langle 110 \rangle$ [30]. Lomer dislocations lie on the (001) plane, i.e. for a $[110]$ dislocation line as shown in figure 2.30, the Lomer dislocation would have a Burgers vector of $\underline{b}_{\text{Lomer}} = \frac{a}{2} [\bar{1}10]$ and have the (001) plane as its glide plane.

Each dislocation that forms at the mismatched interface partially relieves strain through the deformation that it induces. The component of the Burgers vector on the (001) plane and perpendicular to the dislocation line direction contributes to strain relaxation in the epilayer. This component is known as the effective Burgers vector ($\underline{b}_{\text{eff}}$) and is calculated as following:

$$\underline{b}_{\text{eff}} = \frac{\underline{b} \cdot \underline{n}_{\text{dir}}}{\|\underline{n}_{\text{dir}}\|} = b \cdot \cos \iota \quad (\text{Equation 2.38})$$

Where: $\underline{n}_{\text{dir}}$ is the direction that is normal to the dislocation line in the interface and ι is the angle between the Burgers vector and the dislocation line normal vector in the interface. For example, for a dislocation line running along [110] and a $b_{60} = \frac{a}{2}[011]$ as shown in figure 2.30, $\underline{n}_{\text{dir}} = [\bar{1}10]$ and the 60° misfit dislocation $\underline{b}_{\text{eff}} = \frac{a}{2\sqrt{2}}$. Therefore, for an epilayer of known mismatch, f , to the substrate the relaxation in the (001) plane caused by dislocations along $\langle 110 \rangle$ directions, $R_{\langle 110 \rangle}$, is given by the following equation:

$$R_{\langle 110 \rangle} = \frac{\rho_{\langle 110 \rangle} \underline{b}_{\text{eff}}}{f} \quad (\text{Equation 2.39})$$

Where: $\rho_{\langle 110 \rangle}$ is the line density of dislocations running in the $\langle 110 \rangle$ direction per unit area of the (001) plane. Lomer dislocations are far more efficient at relieving strain than 60° misfits and hence are more energetically favourable to form because their Burgers vector is the same as their effective Burgers vector.

Finally, the force keeping a single dislocation from extending is known as a line tension force, F_1 , the derivation of which is in E.A. Fitzgerald [95]:

$$F_1 = \left[\frac{Gb^2(1-\nu \cos^2 \alpha)}{4\pi(1-\nu)} \right] \left[\ln \left(\frac{h}{b} \right) + 1 \right] \quad (\text{Equation 2.40})$$

Where: α is the angle between the Burgers vector and the dislocation line, ν is the Poisson ratio and h is the layer thickness. This force multiplied by the distance moved by the dislocation is known as the ‘self-energy’ of the dislocation.

2.5.5. Threading dislocations

The only way to terminate dislocations is through a closed loop or if they propagate to the surface. Figure 2.31 shows a misfit dislocation arm lying in the (111) plane to the surface of the epilayer. This is known as a threading dislocation, and it does not contribute much to layer strain relaxation. There exists a vector component to the threading dislocation line direction along the [001] direction. During epitaxial growth threading dislocations are present on the growth surface and preserved through the continuous deposition of adatoms around the dislocation thereby extending them to the growth surface.

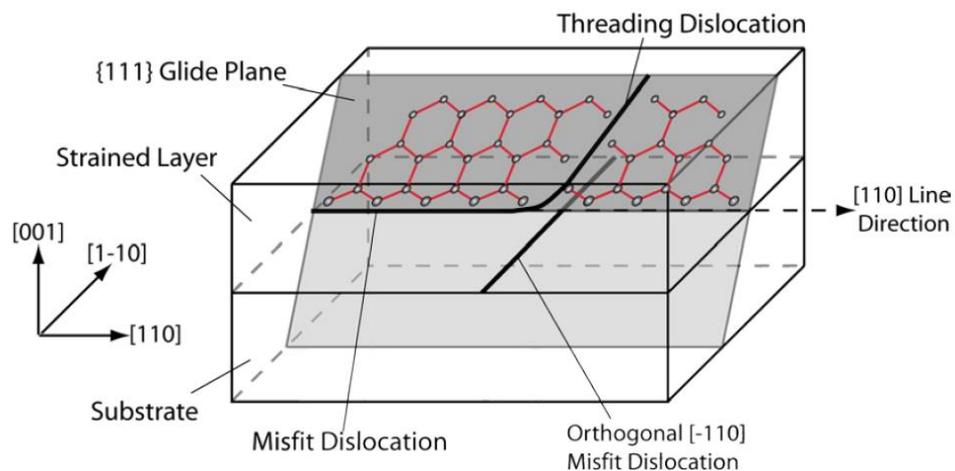


Figure 2.31: Diagram showing a [110] misfit dislocation along glide plane in an FCC diamond or zinc blende crystal, “threading” through the broken bonds. Taken from Shah [96].

Previous studies have shown that threading dislocations do act to hinder the electronic [31], [97] and photonic properties of semiconductor epitaxial layers [98]. The density of threading dislocations (TDD) in an epilayer gives a qualitative understanding of the layer and is given in units of cm^{-2} .

2.5.6. Dislocation Mechanics

The terms ‘climb’ and ‘glide’ were mentioned earlier, as methods by which dislocations propagate. Gliding of dislocations requires strain and thermal energy. In the process of dislocation glide, energy is provided to the broken bonds along any of the slip planes, and in doing so the bonds attach to the next neighbouring column of atoms; as shown in figure 2.32 for a 60° misfit dislocation. This allows for the extension of the dislocation and results in further relaxation of the epilayer. Climb is a higher energy process and involves the continuous addition and subtraction of atoms around the dislocation, thereby allowing a dislocation to move out of its slip plane and onto a parallel plane.

For FCC diamond and zinc blende crystals, the {111} slip planes for 60° misfit dislocations are also their glide planes. Lomer dislocations do not have a vector component that lies on a {111} slip plane and therefore cannot glide through the layer; they can only climb through the layer or glide along the (001) interface. Their glide force is greatest in 3-D islands due to the presence of non-uniform radial stress.

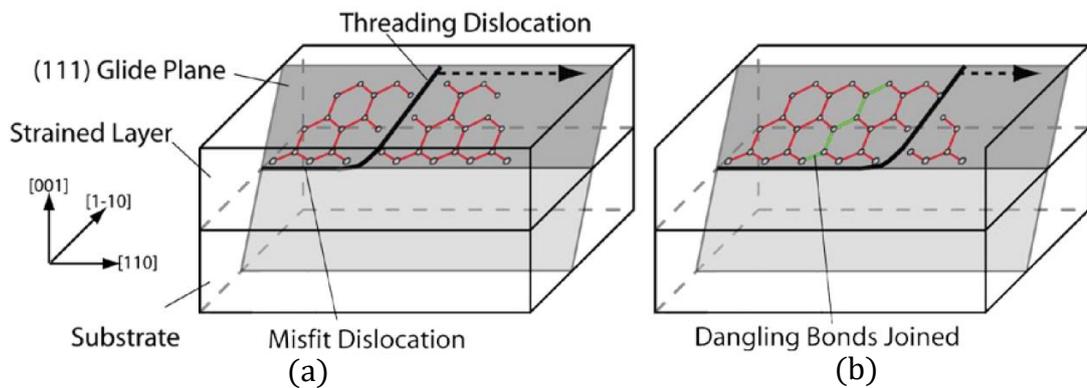


Figure 2.32: Diagram showing the glide of a [110] 60° misfit dislocation extending and gliding along the (111) glide plane in an FCC diamond or zinc blende crystal. Adapted from Shah [96].

The glide velocity, v_{glide} , of both 60° and Lomer dislocations in FCC Diamond and zinc blende crystals is given by the following relationship [31]:

$$v_{\text{glide}} = B\epsilon e^{-\frac{E_{\text{glide}}}{kT}} \quad (\text{Equation 2.41})$$

Where: B is the constant related to the initial velocity, ϵ is the amount of strain in the layer, T is the temperature applied, E_{glide} is the glide activation energy and k is the Boltzmann constant. For SiGe alloy layers, E_{glide} is as following [31]:

$$E_{\text{glide}} = (2.16 - 0.7x) \text{ eV} \quad (\text{Equation 2.42})$$

2.5.7. Nucleation and multiplication of dislocations.

As a strained layer is grown on a substrate, it will undergo relaxation and form dislocations upon reaching a critical level of strain. The nucleation of dislocations can be heterogeneous, homogenous or through some multiplication mechanism.

Homogeneous nucleation occurs as half loop from a point source on the surface, and requires high stresses which are obtained through high thermal budget (growth and annealing temperatures) or through high lattice mismatches $f > 2\%$ [30].

Heterogeneous nucleation occurs when a dislocation is already present in the epilayer. The existing dislocation can be treated as a free surface on which further dislocations can be nucleated. The existence of voids, precipitates, contaminants in the layer (including dopants) and excessive surface roughness during growth can cause the heterogeneous nucleation of dislocation [99].

Multiplication of dislocations arise due to the interaction of existing dislocations with each other. On the whole, higher levels of strain energy are required in the layer to induce dislocation multiplication than for the dislocation to glide. Examples of multiplication types include Frank-Read multiplication and the other is multiple cross glide.

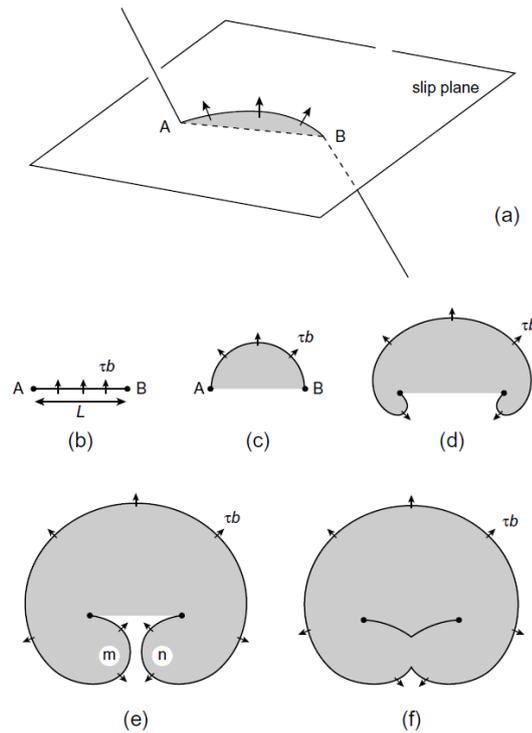


Figure 2.33: Diagram showing the progression of the Frank-Read dislocation multiplication process. Taken from Hull and Bacon [30].

With the Frank-Read process a dislocation line of length, L , can be held down on both sides by interactions with other dislocations, in a process known as dislocation pinning, as seen in figure 2.33 (a) and (b). The Burgers vector of the dislocation lies in the slip plane. The force of pinning the dislocation on either side generates a shear stress, τ , with a force of, τb , per unit length of the pinned dislocation. This makes the dislocation bow, and the radius of curvature of the bow is inversely proportional to the shear stress. As the shear stress increases the bow radius decreases (c). The dislocation continues to extend at this stress, and so the bowing radius increases causing the shear stress to reduce which causes the formation of a ‘kidney-shaped’ loop (d). The radius will continue to increase and segments ‘m’ and ‘n’ will ultimately collide and annihilate because they have the same but opposite Burger’s vector. This causes the formation of a large expanding outer loop, whilst the initial dislocation line is regenerated for the process to repeat itself.

A modified version of the Frank-Read multiplication process involving graded SiGe on Si(001) and GaInAs on GaAs was investigated by Legoues et al [100] and showed two misfit dislocations running orthogonally along $\{110\}$ planes, intersecting at the

substrate/epilayer interface and forming Frank-Read type loops which expanded along glide planes until it reached the epilayer surface where segments of the loop along the (001) plane terminate. The Frank-Read multiplication process allows for fast relaxation of the epilayer and requires a lower activation energy than homogenous nucleation. As a consequence of the loop segments terminating on the (001) planes, the TDD values have a propensity to be high under such a multiplication process. In linearly graded $\text{Si}_{1-x}\text{Ge}_x$ layers on Si(001) where 60° misfit dislocation networks are dense at the interface, pile-up of threading dislocations can occur at strain field intersection points caused by Frank-Read multiplication.

2.5.8. Critical thickness of layer relaxation

2.5.8.1. Matthews-Blakeslee model

For an elastically strained, constant composition epilayer grown on a relaxed substrate, the relationship between layer thickness, and energy per unit area, E_h is given by the following equation:

$$E_h = 2G \left(\frac{1+\nu}{1-\nu} \right) h \epsilon^2 \quad (\text{Equation 2.43})$$

Where threading dislocations already exist in the substrate, the critical thickness at the point where misfits are generated at the interface is determined through balancing the driving force of the threading dislocation, F_h , to extend and form a misfit dislocation against line tension force F_l in equation 2.40 as shown in figure 2.34 [30].

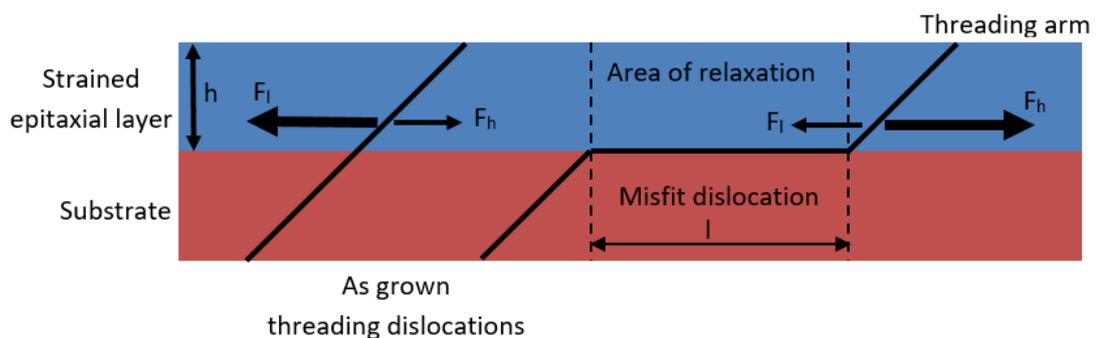


Figure 2.34: Diagram showing the Matthews-Blakeslee model for misfit dislocation propagation in a situation where the epilayer is compressively strained to the substrate. Adapted from Halpin [101].

F_h is determined from the component of the stress in the strained epilayer that acts in the direction of dislocation slip, through a term known as the Schmid factor ($\cos\lambda \cdot \cos\phi$) [95]. The equation for the driving force is given as:

$$F_h = 2G \left(\frac{1+\nu}{1-\nu} \right) bh\varepsilon(\cos\lambda) \quad (\text{Equation 2.44})$$

Where λ is the angle between the Burgers vector and a line perpendicular to the intersection of the glide plane and the interfacial plane and has been found to be 60° for $\langle 110 \rangle$, $\{111\}$ slip systems from the work by Matthews [102]. Φ is the angle between the interfacial plane and the normal to the slip plane. When $F_1 = F_h$ the layer thickness is at a critical point and the threading dislocation is able to glide and form a misfit dislocation, and therefore by equating equation 2.44 to equation 2.40 the critical thickness, h_c , is derived by Matthews and Blakeslee as [103]:

$$h_c \approx \frac{b(1-\nu \cos^2 \alpha)}{8\pi(1+\nu)\varepsilon(\cos\lambda)} \left[\ln \left(\frac{h_c}{b} \right) + 1 \right] \quad (\text{Equation 2.45})$$

The above equation does not hold true for Lomer dislocations since $\lambda = 90^\circ$.

2.5.8.2. Nucleation of dislocations in a defect free substrate

In the case of spontaneous dislocation nucleation, a half-loop can be generated on the epilayer surface with radius R . The total energy, E , remaining in the epilayer after forming a half loop is the sum of the strain energy released by forming the loop and the energy difference in forming a surface step, minus the energy cost to the substrate/epilayer system in forming the dislocation loop. This is given as [102]:

$$E = \left[\frac{GbR}{8(1-\nu)} \right] \left[\left(b(2-\nu) \cdot \ln \left(\frac{8\eta R}{e^2 b} \right) \right) - \left(8\pi R\varepsilon(1+\nu) \cdot \underbrace{\cos\lambda \cdot \cos\phi}_{\text{Schmid factor}} \right) - 2b \cdot (1-\nu) \cdot \sin\alpha \right] \quad (\text{Equation 2.46})$$

Where η is a constant. $\eta=4$ for diamond structures [104]. If E exceeds a critical activation energy value, E^* when R reaches a critical radius R^* , the half-loop will grow to form a misfit dislocation at the interface and two threading arms, as seen in figure 2.35.

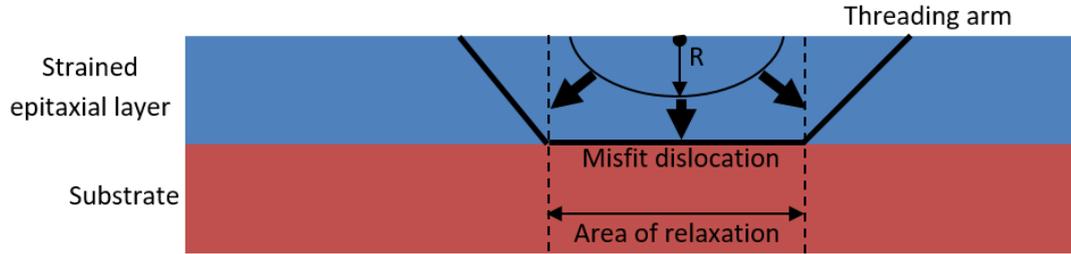


Figure 2.35: Diagram showing the nucleation of a half loop on a strained epilayer surface, expanding radially until a misfit dislocation is formed at the interface.

Temperature is known to cause the loop to enlarge and subsequently increase the dislocation nucleation rate. The nucleation rate follows an Arrhenius relationship with E^* . It is also a function of atom density and the frequency at which critical half loops become super critical. This means that the onset of strain relaxation in an epilayer can be inhibited if the growth and/or annealing temperatures are low enough, however due to the complicated non-equilibrium conditions in epitaxial growth it is very difficult to predict the frequency where half loops become supercritical.

2.5.8.3. Kinetic effects and interaction between dislocations

In epitaxial growth, the non-equilibrium conditions mean that the Matthews-Blakeslee model is not entirely accurate and previous experimental results show that a critical thickness for a strained epilayer beyond that which can be obtained from equation 2.45 is possible. The balance of the line tension stress and driving stress from the strained layer, on a threading dislocation, gives the effective stress, τ_{eff} , defined as [105]:

$$\tau_{\text{eff}} = \left[\frac{2G(1+\nu)}{(1-\nu)} \right] (\delta_{\infty} - \delta) \quad (\text{Equation 2.47})$$

Where: δ is the amount of strain relieved and δ_{∞} is the amount of strain relieved by misfit dislocations at equilibrium. The equation from Houghton for τ_{eff} [106], takes into account the increase in misfit dislocation line tension caused by dislocation-

dislocation interaction. These interactions result in an additional frictional force term that limit dislocation velocities (equation 2.41), which impede layer relaxation. The Matthews kinetic modification defines δ_∞ for lattice mismatch, f , as:

$$\delta_\infty = f - \frac{b(1-\nu \cos^2 \alpha)}{8\pi h(1+\nu)(\cos \lambda)} \left[\ln \left(\frac{h}{b} \right) + 1 \right] \quad (\text{Equation 2.48})$$

A given amount of relaxation, δ , can be achieved by a lot of low velocity threading dislocations or by a few high velocity threading dislocations and for a constant v_{glide} the relaxation time is longer in an epilayer with fewer mobile threading dislocations. A study by Ward et al estimates that $\text{TDD} \propto \frac{1}{h^2}$ [107] for (001) FCC diamond structures and shows that regardless of the starting TDD and the percentage of which are mobile, a kinetic limit will always be present. Finally, multiplication of dislocations is also important to consider as the generation of mobile dislocations contributes to calculating the strain relaxation rate.

2.5.8.4. Dislocation pile-up and annihilation.

A strain field is created when either a dislocation induces local distortion of atomic bonds along its length or from surface undulations of a strained layer undergoing elastic strain relaxation. Gliding threading dislocations can be blocked by orthogonal misfit dislocations within the strain field itself or due to a 3-D island and have a reduced glide channel height, h^* [108] (figure 2.36). As will be seen in chapter 5, this is commonly seen in linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers on Si(001) where compressive strain relaxation causes surface undulations to return the surface energy to a positive value. The high heterogeneous nucleation rate of misfit dislocations creates large radii strain fields. The strain fields effect the isotropy of adatom deposition which leads to a “cross hatch” pattern on the (001) plane [108]. If the cross hatch undulations are severe enough, it may reduce h^* to zero thereby pinning the threading dislocation. Additionally, the nucleation barrier is reduced at the cusps of the cross hatch undulations therefore at high growth temperatures dislocations can also nucleate and multiply via the Frank-Read mechanism also. The pinned threading segments affect the adatom deposition, and enhance the roughening of the surface in a

vicious cycle. When the threading segments are on the same glide plane and have the same Burgers vector, this phenomenon is known as pile up [109], [110].

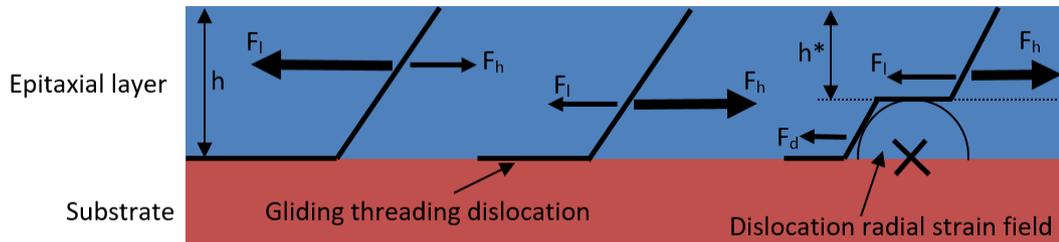


Figure 2.36: Interaction of a gliding threading dislocation with a strain field created by an orthogonal misfit dislocation. The threading dislocation has been forced into a reduced glide channel h^* by the retarding force of the strain field F_d . Adapted from Freund [111].

For threading dislocations that meet, several events can occur, depending on their Burgers vector. They can meet and generate a third dislocation or if they have opposite Burgers vectors and are on the same glide plane, they can annihilate. The annihilation of the threading arms, connects the misfit dislocations that they were attached to, leaving behind a region of perfect crystal in the epilayer and a perfect 60° misfit dislocation at the interface. For epilayers with $TDD \geq 10^8 \text{ cm}^{-2}$, this is the primary mechanism for TDD reduction. When TDD is below this level the main reduction mechanism is glide until they reach a free surface. A third event can occur where the two meeting dislocations produce two dislocations at the output with a change in type, resulting in no reduction in TDD. For more information on threading dislocation interaction see Ward et al [107].

2.5.9. Stacking faults.

The perfect 60° misfit dislocation is comprised of two Shockley partial dislocations; a 30° partial and a 90° partial [30] as seen in figure 2.37. Equation 2.49 shows the Burgers vector relationship between the 60° dislocation and its two corresponding Shockley partials. Equation 2.50 gives the vector addition of the two Shockley partials to give the perfect dislocation.

$$\underline{b}_{60^\circ} = \underline{b}_{30^\circ} + \underline{b}_{90^\circ} \quad (\text{Equation 2.49})$$

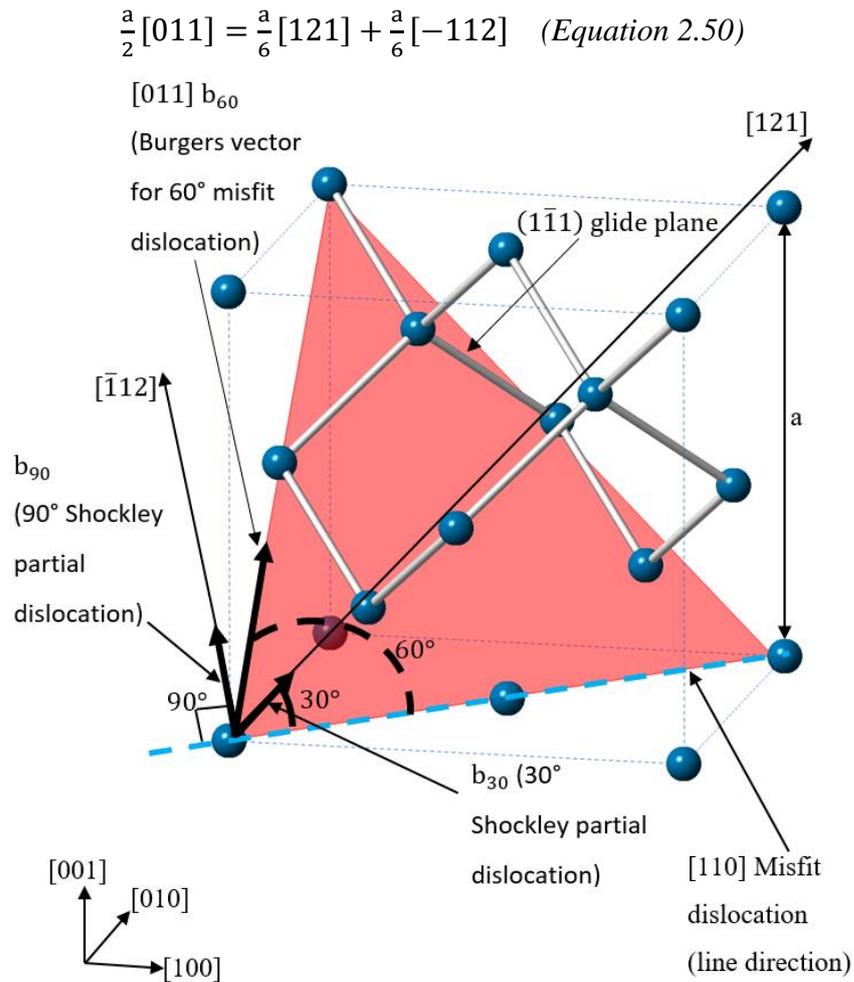


Figure 2.37: Vector diagram showing a 60° misfit dislocation in a FCC diamond (zinc blende) crystal, and the Shockley partial dislocations at 90° with a Burgers vector of $\underline{b}_{90} = \frac{a}{6}[\bar{1}12]$ and 30° with a Burgers vector of $\underline{b}_{30} = \frac{a}{6}[121]$.

Both partial dislocations have a vector component that lies in the (111) plane, meaning that the (111) plane is also a slip plane for the partial dislocations. The glide of the 60° dislocation is a two stage process, i.e. of two Shockley partials which have even shorter lattice translation vectors than the 60° misfit dislocation. The process by which 60° misfit glides via its vector components can be explained by a Thompson tetrahedron. Figure 2.38 shows a perfect 60° dislocation, that has disassociated into two partials. The force required to create a stacking fault is $F_{SF} = \gamma_{SF} \cdot d$, where γ_{SF} is the energy density for stacking fault formation and was determined to be between $55\text{-}75\text{mJm}^{-2}$ [30] and d is the separation distance between the partials and is found to be approximately 3 to 5\AA in linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers [112]. In figure 2.38, F_{SF} exerted by the partials on each other are equal and opposite.

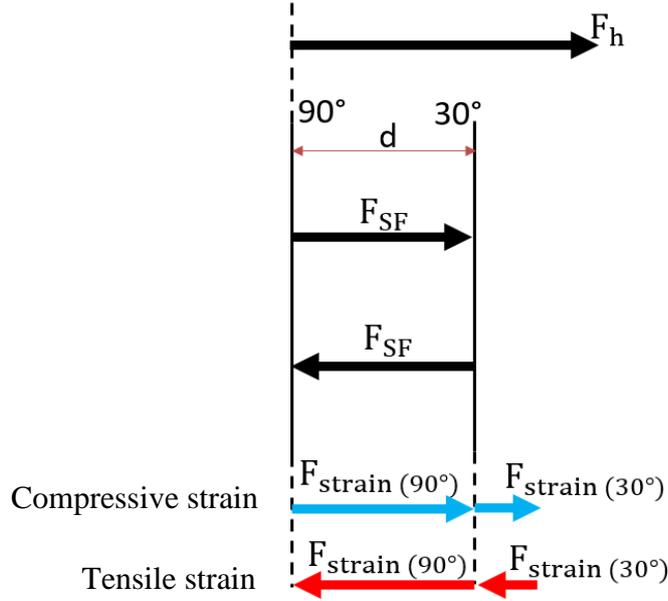


Figure 2.38: Force balance diagram of a disassociated 60° misfit dislocation and its two Shockley partial dislocations under strain on a (001) substrate.

For the \underline{b}_{60° given in equations 2.49 and 2.50, the glide plane is $(\bar{1}1\bar{1})$ and the direction vector, $\underline{\hat{m}} = \frac{1}{\sqrt{3}}(\bar{1}1\bar{1})$. The strain force (F_{strain}) on each Shockley partial generated by F_h is derived from the stress tensor, $\underline{\underline{\sigma}}$, as follows:

$$F_{strain} = \underline{\underline{\sigma}} \cdot \underline{\hat{m}} \cdot \underline{b} = \frac{2G(1+\nu)}{(1-\nu)} \cdot \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \underline{\hat{m}} \cdot \underline{b} \quad (\text{Equation 2.51})$$

Shockley partial =	30°	90°
$F_{strain} =$	$\frac{G(1+\nu)}{3\sqrt{3}(1-\nu)}$	$\frac{2G(1+\nu)}{3\sqrt{3}(1-\nu)}$

Table 2.5: F_{strain} for the two Shockley partial dislocations.

From table 2.5 it is seen that $F_{strain}(90^\circ)$ is twice as large as $F_{strain}(30^\circ)$. For a stacking fault to form, two conditions must be met. Firstly, a 60° misfit dislocation is only preserved when [30]:

$$b_{60}^2 > b_{90}^2 + b_{30}^2 \quad (\text{Equation 2.52})$$

Secondly, $F_{\text{strain}}(90^\circ)$ must be greater than F_{SF} , so that the 90° partial can separate from the 30° partial. Figure 2.38 shows that in a layer relaxing under compressive strain the 30° partial leads the 90° partial and vice versa for a layer relaxing under tensile strain. This means when the two conditions are met it is more likely that a stacking fault would form in a layer relaxing under tensile strain because the 90° partial is not hindered by the strain force of the 30° partial.

2.5.10. Crystallographic tilt

Crystallographic tilt is the misorientation of the epilayer lattice planes with respect to the substrate. Tilt has been most commonly observed in epilayers grown on offcut substrates. This can happen not only because of substrate offcut, but also due to lattice mismatch, layer thickness and growth conditions [113].

For a pseudomorphic layer on nominal substrate, the respective $\{001\}$ planes on the substrate and epilayer are parallel however other planes are tilted due to the Poisson's ratio effect and there is no overall tilt in the layer. For an offcut (001) substrate, composed of terrace steps of height, m , and length, L , the relationship to the offcut angle, Φ (in radians), is: $\tan \phi = m/L$. For a pseudomorphic strained epilayer with unit cell lattice constants, $a_{\text{substrate}} \times a_{\text{substrate}} \times c$, the (001) plane tilt caused by the Poisson effect, $\Delta\phi$, is given as:

$$\Delta\phi = \tan^{-1} \left(\left(\frac{a_{\text{substrate}} - c}{a_{\text{substrate}}} \right) \tan \phi \right) \quad (\text{Equation 2.53})$$

This is shown in figure 2.39. If $c > a_s$ the tilt will be away from the surface normal and if $c < a_s$ then the tilt will be toward the surface normal. Geometrically it is seen that $\Delta\phi$ increases with increasing offcut angle. The limitation of the model by Nagai is that once misfit dislocations appear at the interface, the terrace and step coherency is no longer maintained.

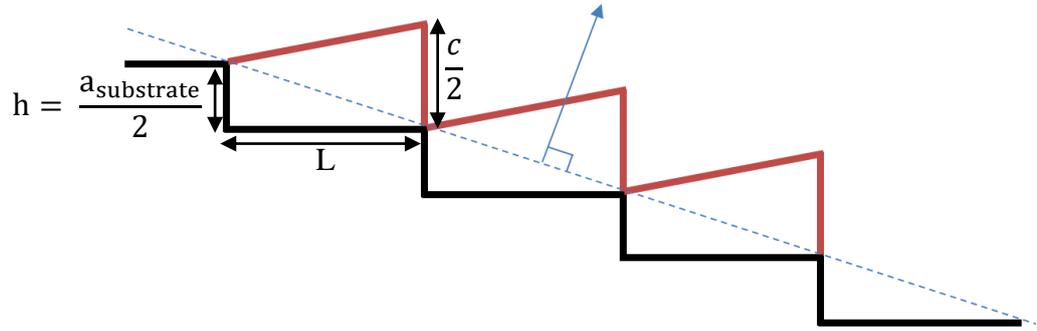


Figure 2.39: Creation of tilt in pseudomorphic epitaxial layer (red) due to the Poisson effect on a vicinal (offcut) substrate (black). The blue dashed line is the growth surface. Adapted from Nagai [114].

The second explanation for tilt involves the inclination of misfit dislocation Burgers vector to the growth plane, proposed by Olsen and Smith [115]. For a 60° misfit dislocation the vertical component of b_{60} to the (001) plane, b_1 , is responsible for tilt and is related to $\underline{b}_{\text{eff}}$ as:

$$\Delta\phi = \varepsilon_{\parallel} \left(\frac{b_1}{\underline{b}_{\text{eff}}} \right) = \varepsilon_{\parallel} \left(\frac{b_{60} \cdot (\sin 60^\circ)}{\underline{b}_{\text{eff}}} \right) \quad (\text{Equation 2.54})$$

This value of $\Delta\phi$ is the maximum tilt that can be generated for a given misfit strain however, 60° misfit networks form in orthogonal arrays therefore making complete cancellation of the tilt components possible and also making it difficult to predict tilt direction. On offcut substrates the $\{111\}$ glide planes are stressed unequally and this causes incomplete cancellation of the tilt component and resulting in asymmetrical strain relaxation and layer tilt.

Finally, on offcut substrates Lomer dislocations will have also a very small vertical Burgers vector component at the steps, meaning that Lomer dislocations can also contribute to tilt on such substrates.

2.6. Cracks

Cracks can form in epitaxial layers, as a tensile strain relaxation mechanism, if the epilayer is beyond a critical thickness. These features are much larger in size than dislocations or even stacking faults and nullify any devices constructed on the epilayer surface.

With $\text{Si}_{1-x}\text{Ge}_x$ and pure Ge epilayers, cracking has been previously reported by Curie et al in linearly graded buffer layers up to pure Ge [116]. Cracks were only observed in linearly graded $\text{Si}_{1-x}\text{Ge}_x$ layers when graded up to pure Ge where the thermal expansion coefficient differences between Ge and Si causes the Ge to relax under tensile strain at a higher growth and annealing temperature. The crack density, (ρ_{CD}), on the Ge epilayer (001) surface was measured in number of cracks per cm and in that investigation $\rho = 47\text{cm}^{-1}$.

More recently, a much more extensive investigation was carried out by Shah et al on reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers up to $x=0.75$ [117]. With the reverse grading process on partially tensile strained $1\mu\text{m}$ LT/HT Ge buffer layers on Si(001), $\text{Si}_{1-x}\text{Ge}_x$ layer also relaxes under tensile strain and was found to assist crack generation during growth. It was found that provided the total buffer layer thickness was kept below $2.7\mu\text{m}$ and $x \geq 0.75$, cracking of the epilayer was suppressed during growth. A maximum crack density of 77.7 cm^{-1} for a buffer layer total thickness of $\approx 6.7\mu\text{m}$ was obtained.

Cracking has also been investigated in III-V materials such as binary GaAs and InP and even quaternary III-V compounds such as InGaAlAs by Murray et al [118]. The process of cleaving the wafer introduces more stress, and if a critical level of stress has already been introduced to the wafer through growth, cleaving the wafer could push the stress beyond that threshold and cause fractures. The equation given in Murray et al to determine critical thickness at which cracks start to appear, for layer bulk lattice constant, a , is:

$$h_c = \frac{a(1-\nu)}{\pi^2 \epsilon^2} \quad (\text{Equation 2.55})$$

Figure 2.40 is taken from Murray et al, and shows the formation of a v-shaped crack in an epilayer. The dimensions are given and the relationship between strain relaxation, α , caused by the crack and the various parameters in the film is given as:

$$\alpha = \frac{\rho_{CD}w}{f} \left(\frac{h}{d} \right) - \frac{2\rho_{CD}w}{f} - \frac{\rho_{CD}^2 w^2}{3f^2} \left(\frac{d}{h} \right) \quad (\text{Equation 2.56})$$

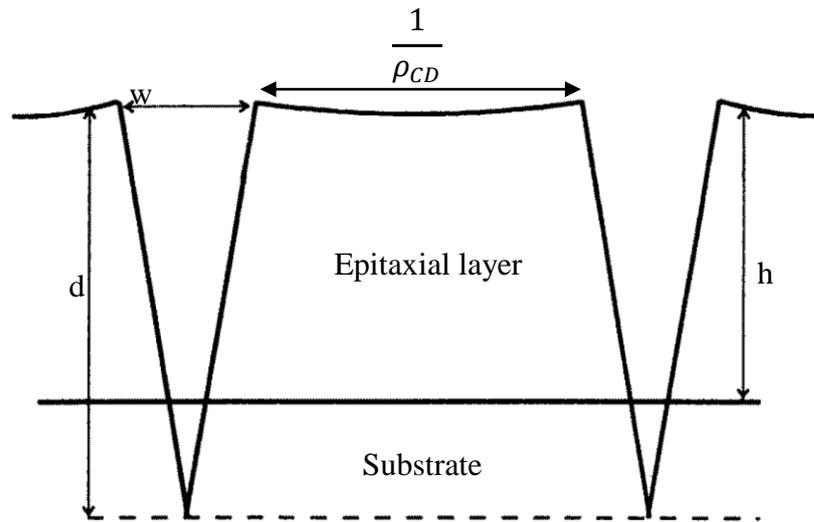


Figure 2.40: Diagram showing of how a 'V' shaped crack penetrates to a depth, d , through the epitaxial layer of thickness, h , during strain relaxation on the substrate. Taken from Murray et al [118].

3. Experimental Techniques.

3.1. Transmission Electron Microscopy (TEM).

Transmission electron microscopy was used to examine the RP-CVD grown $\text{Si}_{1-x}\text{Ge}_x$ & Ge buffer layers and SS-MBE grown InSb & InSb/AlSb heterostructures on the Ge/Si(001) virtual substrates, in order to examine crystalline quality, measure layer thicknesses and gain counts of threading dislocation densities.

The samples were cleaved from the wafer and prepared in two methods: 1) as cross-sections along the [110] and $[\bar{1}\bar{1}0]$ edges and 2) as plan view samples on the (001) plane so that the epilayer surface could be seen and analysed to get defect counts. The textbook, *Transmission Electron Microscopy a Textbook for Materials science* by Williams and Carter [119] was used as the main guide for electron microscopy throughout this study.

3.1.1. Fundamentals of TEM.

Transmission electron microscopy works under the principle that electrons behave as waves as well as particles, where the electron de Broglie wavelength, λ is:

$$\lambda = \frac{h}{\left[2m_0eV\left(1+\frac{eV}{2m_0c^2}\right)\right]^{0.5}} \quad (\text{Equation 3.1})$$

In the equation above: h is Planck's constant, c is the speed of light, V is the accelerating voltage, m_0 is the rest mass of the electron and e is the electronic charge. The resolving power any microscope is dependent on the wavelength, λ , of the imaging radiation. For optical microscopes, the maximum resolution, R, with a numerical aperture, NA, is determined by the Rayleigh criterion:

$$R = \frac{0.61\lambda}{NA} \quad (\text{Equation 3.2})$$

Optical microscopes use transparent lenses to refract light waves that have been reflected off of a sample to a singular point through an aperture [120]. Electron microscopes operate in a similar manner; however, the lenses are electrical coils that generate magnetic fields (through Ampere's law). The magnetic field deflects the

beam of incoming electrons, through various lenses and the sample until it strikes a phosphorous screen where the sample image is displayed. For an electron microscope the maximum resolution, δ , is determined by the wavelength of the electrons as well as the coefficient of spherical aberration, C_s , of the instrument by the following relationship:

$$\delta = 0.66 \times C_s^{\frac{1}{4}} \lambda^{\frac{3}{4}} \quad (\text{Equation 3.3})$$

Spherical aberration C_s is a phenomenon caused by imperfections in the lens that results in an altered magnetic field that effects off axis beams of electrons to behave differently and thus not converging at a singular point. In HR-TEM systems, so called aberration correctors are used to locally correct the imperfection in the lens magnetic field in order to achieve atomic resolution of the sample.

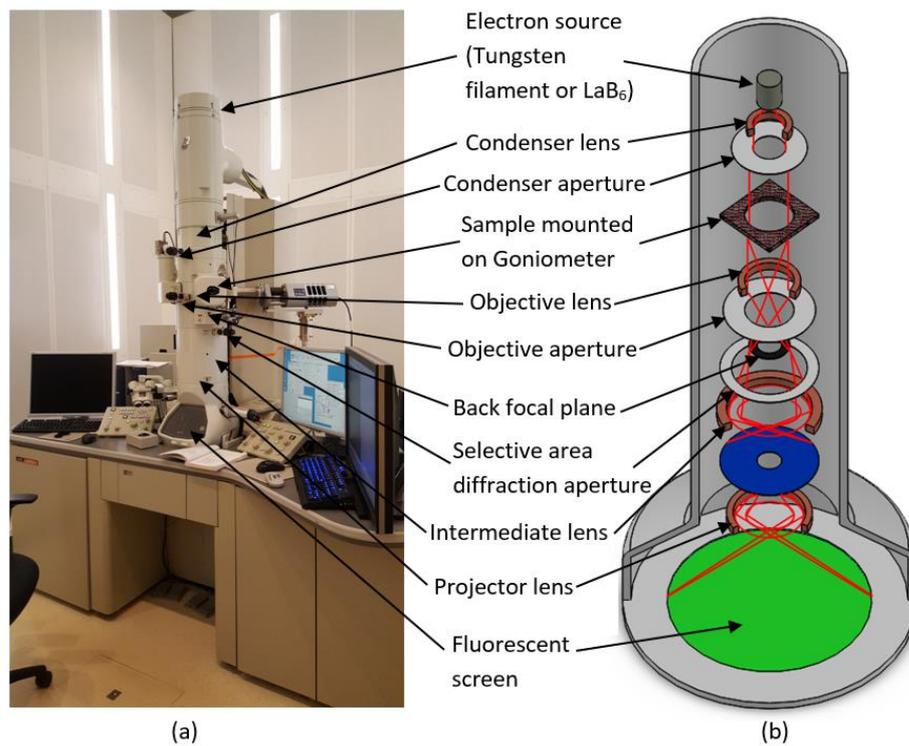


Figure 3.1: JEOL 2100 TEM (a) and cutaway schematic diagram of TEM (b). The arrows in figure (a) point to the location of the various parts inside the instrument. Figure (b) shows the instrument in normal imaging mode, as indicated by the electron beam (in red).

Figure 3.1(a) is an image of the JEOL 2100 electron microscope that was used in this investigation to carry out high resolution imaging. This particular microscope uses a LaB₆ crystal to thermionically generate an electron beam. The other microscope used

in this investigation was the JEOL 2000 microscope to carry out low magnification imaging. This microscope uses a tungsten filament to thermionically emit an electron beam. There are advantages and disadvantages to both types of sources. Some of the benefits of using LaB_6 crystal over tungsten filament are: that the operating temperatures are lower with LaB_6 (1700K) than with tungsten (2700K), a higher current density is obtained and the energy spread is lower and a longer lifetime of the LaB_6 source of about 500 hrs whereas the lifetime for tungsten filament sources is of the order of ≤ 100 hrs. The disadvantages include the need for a greater vacuum in the column.

Figure 3.1(b) shows the electron beam pathway in a transmission electron microscope for normal imaging of a sample. Initially the beam, coming from the source, is reduced in width and intensity through a condenser lens, and transmitted through the sample (which has to be of the order of $< 100\text{nm}$ thick to be electron transparent). Initially when aligning the beam, which is done at $\times 15,000$ magnification for the JEOL 2000 and at $\times 40,000$ magnification for the JEOL 2100 to ensure all the objective lenses are activated, the condenser aperture is adjusted so that as the beam spot diameter is reduced and enlarged both clockwise and in the anti-clockwise direction, it does so on a single point (see TEM microscope alignment steps written by R. Beanland for detailed instructions on alignment for the JEOL 2000 and 2100 instruments [121]). The electron beams reaching the back focal plane are those that have been diffracted through the various planes in the sample crystal but as those diffracted beams reach the intermediate lens, all diffracted beams are superimposed on top of each other and therefore a complete image of the sample is constructed, as shown in figure 3.1(b).

Before a focused image can be taken of the sample using a CCD camera beneath the phosphorous screen, objective astigmatism has to be corrected. Objective-lens astigmatism occurs if the objective aperture is misaligned or if there is residual contamination. For cross-sectional samples astigmatism is corrected by selecting an amorphous region of the sample (the araldite glue used to glue the samples together) and then taking an FFT of the area under high magnification. For a crystalline material an electron wave diffracting through the crystal will create Bragg peaks depending on the crystal plane. In reciprocal space the peak will be positioned by their reciprocal

space vectors, for an amorphous material a singular peak will not be produced since there is no crystallinity. Instead a ‘smearing’ of peaks will appear as a series of rings. Correction of objective astigmatism involves adjusting the focus on the objective lens and the beam deflections until the rings are as bright and as circular as possible respectively.

3.1.2. Sample preparation.

Sample preparation is paramount to obtaining superb TEM images. Approximately 1.5cm by 0.5cm pieces were cleaved from an epiwafer (epilayers grown on the substrate) and glued together using araldite. The processes involved in cross-sectional TEM (X-TEM) sample preparation are shown in figure 3.3. Ideally the electron transparent region should be of the order of $\leq 100\text{nm}$ thick. This is accomplished by mechanically grinding the sample down to about $10\mu\text{m}$ thickness and then using ionised argon beams in a precision ion polishing system (PIPS) to create a crater in the sample where anywhere between 1 to $10\mu\text{m}$ away from the crater edge is thinned to less than 100nm thick. The milling energy used was 6keV , however once the crater was created, the beam energies were dropped to 2keV for polishing the sample.

Cleaving pieces from off axis epiwafers (epilayers grown on off-axis substrates) proved to be more difficult, because with off-axis (001) wafers the presence of [110] direction steps meant the surface was ‘jagged’ and when pressure is applied at an indentation unequal amounts of force are distributed through the wafer surface, causing it to cleave in unintentional directions. Figure 3.2 shows the process for cleaving off-axis wafers.

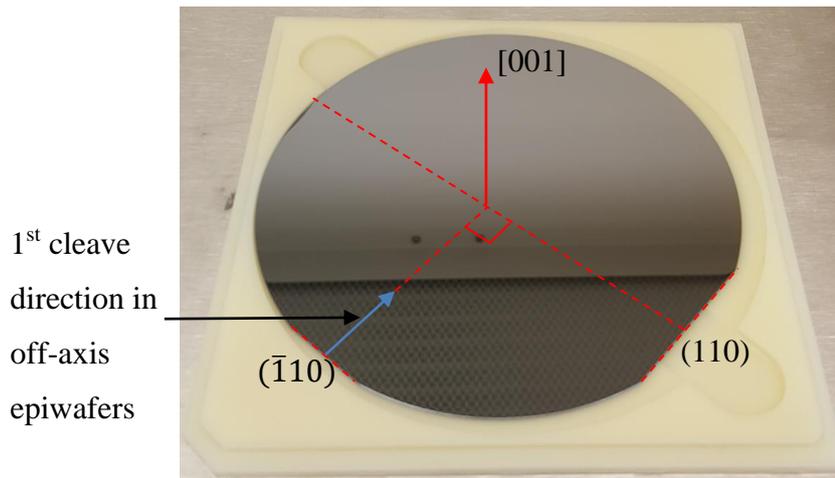


Figure 3.2: Cleave lines on an (001) orientation 100mm diameter epiwafer. For off axis substrates, where the offcut steps lie towards the [110] direction the cleaving process requires cleaving parallel to a step first i.e. perpendicular to the $(\bar{1}10)$ plane, to ensure more evenly shaped wafer pieces.

For the samples with InSb epitaxial layers, which has a low melting temperature, and for ultra-thin Ge buffer layers ($\leq 10\text{nm}$ thickness), ion beam milling was carried out under liquid nitrogen cooling to ensure that the heat generated from milling didn't turn the layer amorphous or simply destroy it. The cryo-milling process involved adding liquid nitrogen to the PIPS dewar until the chamber temperature reached about -150°C before inserting the sample, evacuating the chamber and aligning the beams. Finally, it was important to wait approximately 15 mins after venting but before extracting the sample from the PIPS to allow time for the sample to reach room temperature or else the thermal shock could cause the epilayer to crack.

In the X-TEM sample preparation process (figure 3.3), with ion beaming to perforate the sample and create a crater at the interface (step (f), single modulation and double sided orientation was used with the ion guns at 6keV energy. Single modulation meant that the steeper angled beam (used for milling), alternated from top to bottom every 360° in tandem with the shallower angle beam used for polishing. This ensured thinning only occurred from one side of the sample interface and resulted in more thin area which was electron transparent.

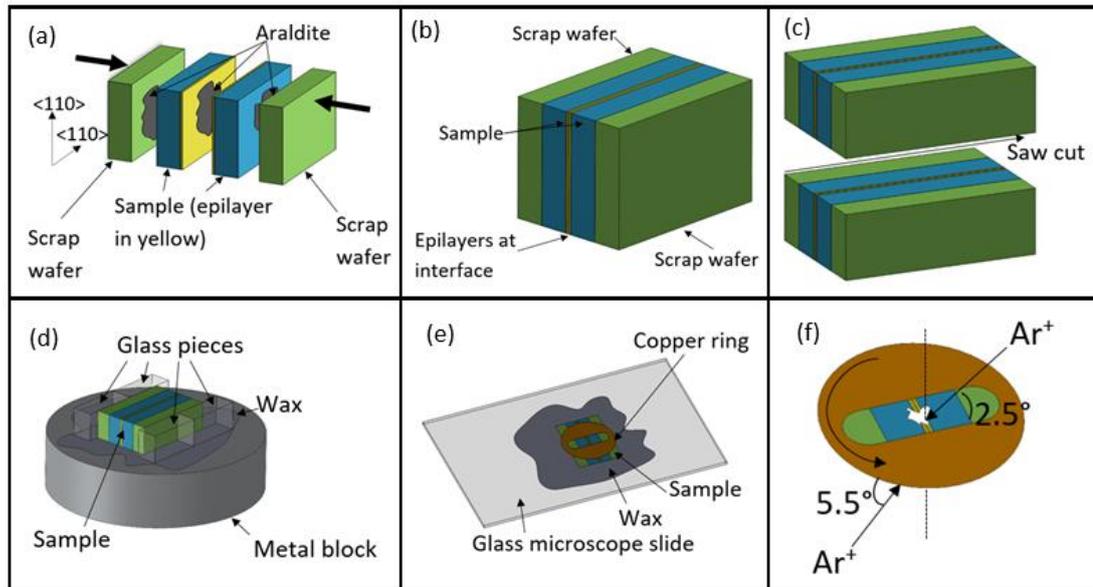


Figure 3.3: cross sectional TEM sample preparation process.

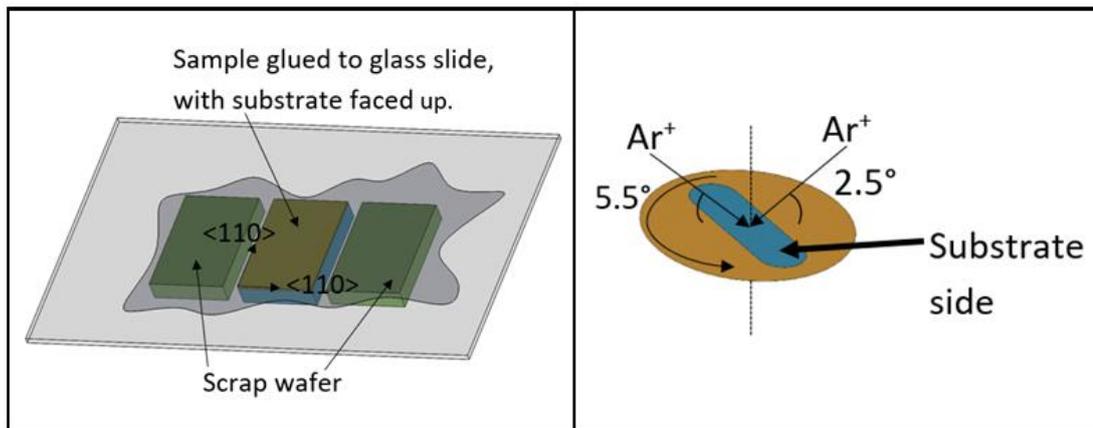


Figure 3.4: Plan view sectional TEM sample preparation process.

With plan view TEM sample preparation, the sample is stuck directly onto a glass slide with wax (figure 3.4). The epilayer is facing down and support pieces of scrap wafer are used to ensure surface is ground smooth. The grid is placed on the substrate side. Ion milling and polishing has to be carried out from the substrate side so as to prevent damage to epilayer. For particularly thin epilayers such as Ge buffer layers less than 100nm thick, due to closeness of the substrate and epilayer diffraction vectors, g_1 and g_2 , the total amount thin area made available from the edge of the crater is

reduced due to Moiré fringing effects and so unavoidably less thin area becomes available to clearly image and obtain TDD counts. The process of milling deposits sputtered material back onto the epilayer surface. To avoid this, it was found that by covering the sample in sodium chloride solution prior to ion milling and then immersing the sample into de-ionised water afterwards had the effect of removing the sputtered material and therefore gave more thin area to be defect analysed.

With Plan View TEM imaging approximately 20 to 30 images were taken under the 220 diffraction condition. The dislocations were counted per image using Imagej software and an average was taken over all of the images to give an average TDD count for the sample.

3.1.3. Diffraction contrast TEM.

In diffraction contrast TEM, the diffracted electron beams reaching the back focal plane is allowed to be passed straight to the phosphorous screen by adjusting the current and magnetic field strength of the projector lens as seen in figure 3.5(a). The resulting diffraction pattern seen on the phosphorous screen is of the straight through electron 000 beam, Bragg peaks and Kikuchi lines. Kikuchi lines are created by incoherent scattering of electrons from thicker regions of the sample, however if the sample is too thick inelastic scattering will dominate and no discernible Bragg diffraction can be detected [119]. The intersection points of Kikuchi lines form zones as seen in figure 3.5(b).

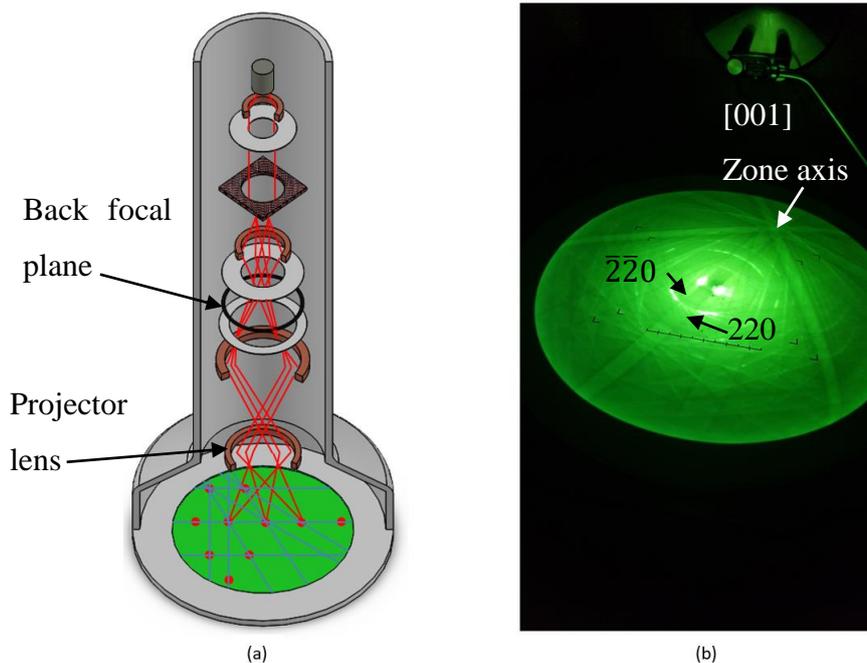


Figure 3.5: Diffraction mode on the TEM. Figure (a) shows the TEM in diffraction mode. This is achieved by adjusting the magnetic field strength of the projector lens which in turn allows the image from the back focal plane to be displayed on the fluorescent screen. Figure (b) is an image taken of the TEM phosphorous screen in diffraction mode whilst setting up a two beam condition showing the Kikuchi lines on the [001] zone axis, and the straight through beam on the $\bar{2}20$ Kikuchi line and the Bragg peak on the 220 Kikuchi line.

The diffraction vector is known as \underline{g} and each pair of Kikuchi lines represent \underline{g} and $\bar{\underline{g}}$. the distance between Kikuchi line pairs is $|\underline{g}|$. As the sample is tilted using the goniometer in two axes of movement, the straight through beam is found to remain stationary but the Kikuchi lines start to move. It is clear that the sample orientation affects the Kikuchi lines made visible, and that they are in effect fixed to the crystal and connected via different zone axes. For an X-TEM sample that has along the $\langle 110 \rangle$ cross sections, the closest zone axis seen is the [110] and for a plan view sample the closest zone axis is the [001]. Kikuchi lines are used as guides to find and identify specific planes on which to set up two beam diffraction conditions. For lattice resolving an image at high resolution, as well as correcting for objective astigmatism at high resolution and ensuring that the voltage centre is corrected, the straight through beam must be placed through the zone axis centre.

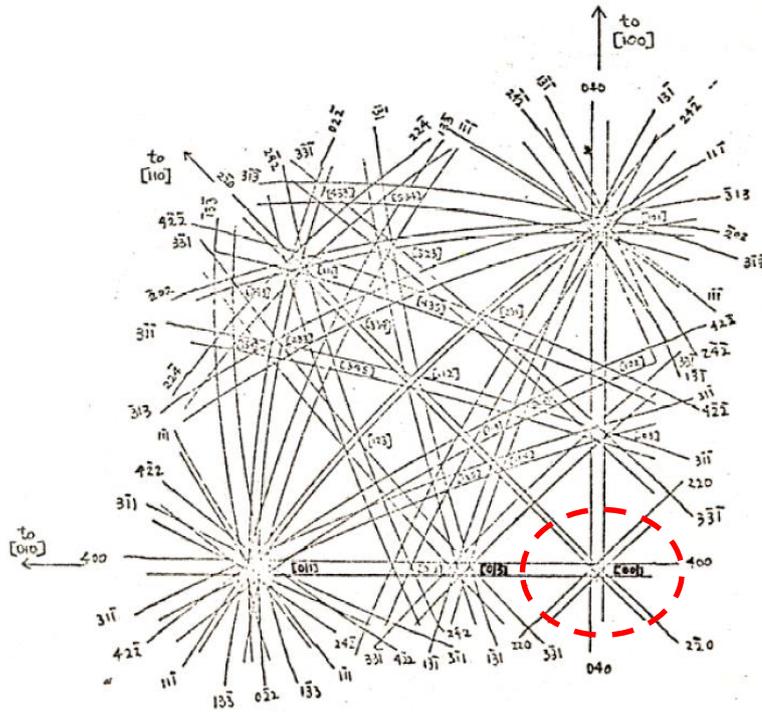


Figure 3.6: Stereographic [001] Kikuchi line map for FCC diamond and zinc blende crystals [122]. The [001] zone axes is indicated by the red dashed circle.

3.1.3.1. Two beam diffraction condition

The dark field condition is where only the electrons scattered by the sample and collected by the objective lens are used in imaging, as opposed to bright field where both scattered and unscattered electrons are used to create an image of the sample. A two beam condition can be created when the straight through beam in bright field is isolated along with the diffracted beam from a desired plane in dark field. The technique involves tilting the sample until the straight through beam is brought over the Kikuchi line of a desired plane with a diffraction vector \underline{g} in bright field. Then in dark field condition, the straight through beam is brought over to the Kikuchi line and Bragg peak of \underline{g} . The objective aperture is placed over the straight through beam in bright field, thereby isolating it, blocking scattered electrons from the other spot, and providing contrast between bright field and dark field images.

Thickness measurements of the layer were carried out using the two beam diffraction condition in 004 because in FCC diamond and zinc blende structures the (004) structure factor gives the strongest intensity symmetrical Bragg peak along the crystal growth direction.

For clearly seeing defects in (001) zinc blende and FCC diamond crystals the 220 diffraction condition is used because this diffracted beam has the shortest extinction distance; the distance travelled before the beam is diffracted again. A shorter extinction distance leads to minimal broadening of the Bragg angle around the dislocation strain field, thus providing greater contrast between perfect crystal and the dislocation. A dislocation will only show residual contrast when $\underline{g} \cdot \underline{b} = 0$ as shown in figure 3.6. It will be completely invisible when $\underline{g} \cdot (\underline{b} \times \underline{u}) = 0$ as well. This is known as the invisibility criterion.

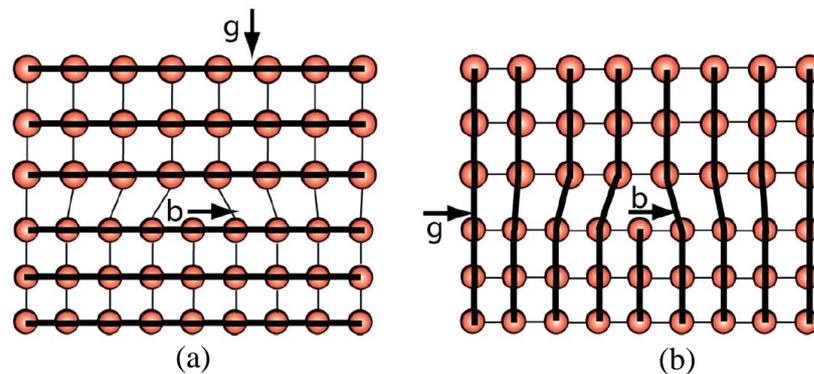


Figure 3.7: (a) represents the condition when $\underline{g} \cdot \underline{b} = 0$, i.e. the diffraction vector and Burgers vector are orthogonal to each other and only residual contrast is seen. Figure (b) shows the condition where \underline{g} and \underline{b} are parallel, therefore the distortion caused by the dislocation is visible. Taken from Shah [96].

It is not often that both conditions are met simultaneously, hence calculations show that 60° misfit will appear in any combination of $\underline{b} = \frac{a}{2} \langle 110 \rangle$ and \underline{g} and $\bar{\underline{g}}$ are either Kikuchi pairs 220 and $\bar{2}\bar{2}0$ or $\bar{2}20$ and $2\bar{2}0$. Stacking faults will be invisible when $\underline{g} \cdot \underline{R}$ is an integer, where \underline{R} is the stacking fault vector and is the Burgers vector of either of the two partial dislocations.

Finally, the weak beam diffraction condition involves moving the straight through beam not over to the Kikuchi line and Bragg peak of $\bar{\underline{g}}$ in dark field, but onto the Bragg

peak and Kikuchi line of weakly scattered electrons in the opposite direction with a diffraction vector $-\underline{\bar{g}}$. For 220 diffraction condition, this shortens the extinction distance even more and gives much stronger diffraction contrast which is particularly useful in the 220 diffraction condition to clearly see dislocations.

3.2. High Resolution X-Ray Diffraction (HR-XRD).

3.2.1. Fundamentals of high resolution X-ray diffractometry

X-rays have a wavelength, λ , that is comparable to the lattice spacing in crystals and can be used to diffract through the crystal via Bragg's law (figure 2.4) as explained in chapter 2.2.1 and equation 2.6. However, X-rays do not interfere as strongly with matter as electrons do. High resolution X-ray diffraction was used in this study to analyse lattice constants, strain, tilt and composition in the RP-CVD grown $\text{Si}_{1-x}\text{Ge}_x$ and Ge epitaxial layers and then the SS-MBE grown InSb/AlSb layer grown on the Ge/Si(001) virtual substrate. The textbook, '*x-ray scattering from semiconductors*' by Paul F. Fewster was used as the main guide to HR-XRD in this study [123].

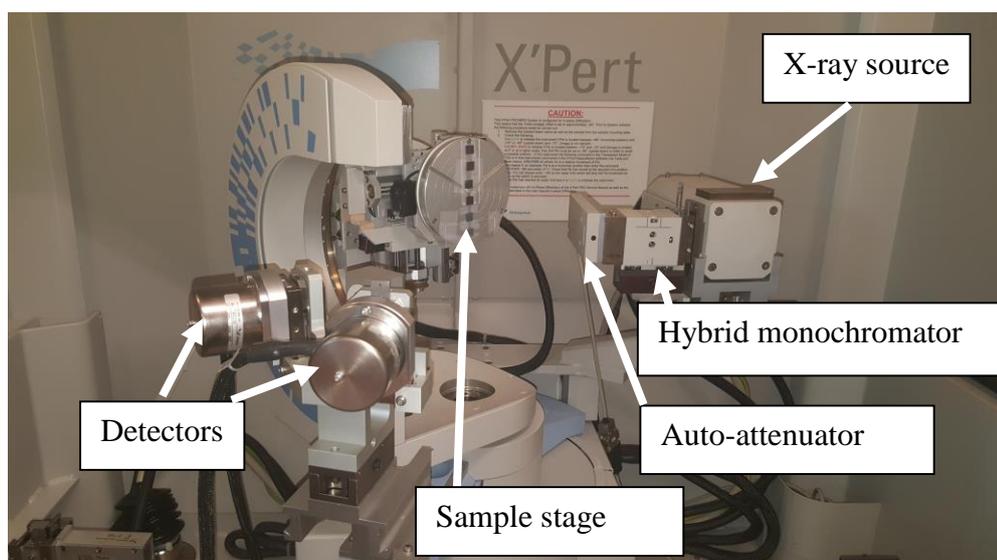


Figure 3.9: Image of the Panalytical X'pert Pro X-ray diffractometer used in this study.

Figure 3.9 is an image of the diffractometer used in this study. The X-ray source is generated from Copper ($\text{CuK}\alpha_1$) at an operating voltage of 45kV, a current of 40mA and generating a wavelength of 1.5406\AA . Once the X-ray beam is generated, it is passed through a hybrid monochromator and attenuator. The attenuator acts to reduce the intensity of the x-ray beam should the count rate reach 500,000 cps, which may

damage the detector i.e. attenuation is primarily used during the alignment stage to the Si(001) substrate which should be almost perfect crystalline quality. A triple axis Ge crystal detector was used with a collimating slit to collect only the diffracted x-rays from the sample.

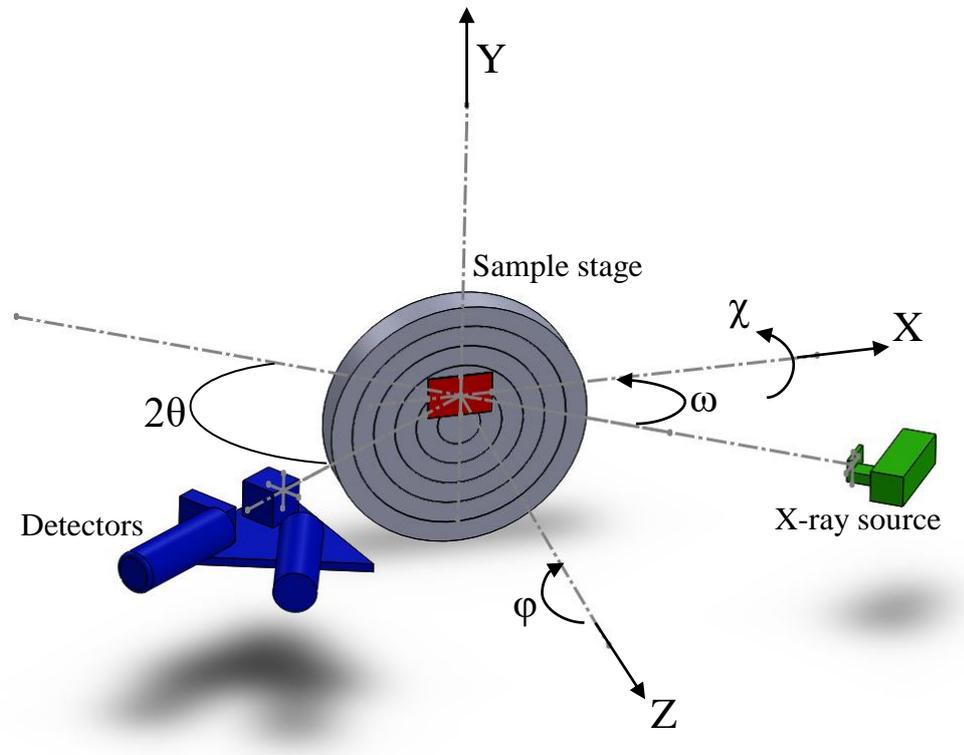


Figure 3.10: ω - 2θ coupled scan set up. The sample (in red) is taped to the stage. The angle χ has been referred to as ψ in some references however, the term χ has been adopted as it is the standard Synchrotron notation.

Figure 3.10 shows the set up for the diffractometer. The stage has three axes of free translational motion: X, Y and Z, and 2 axes free rotational motion χ and ϕ . ω (sometimes referred to as θ) is the angle between the incidence beam and the sample and 2θ is the angle between the incidence beam and the diffracted beam from the sample.

Fine calibration offset scans are carried out initially to zero the set-up and once done, the sample should be in the ‘half cut’ position, i.e.: where the incident beam is cut in half by the sample. For detailed instructions on calibration, aligning onto a sample and carrying out an RSM measurement please refer to Capewell, Palmer and Shah [124].

3.2.2. Reciprocal space and the Ewald's sphere

In Chapter 2.1, the lattice translation vector, T , was explained for FCC diamond and zinc blende crystals as equation 2.1. In Chapter 2.2, the reciprocal lattice was explained with the equivalent reciprocal lattice translation vector in reciprocal space, G , given by equation 2.2 with the noncoplanar vectors: A_1 , A_2 and A_3 given by equations 2.3, 2.4 and 2.5 respectively.

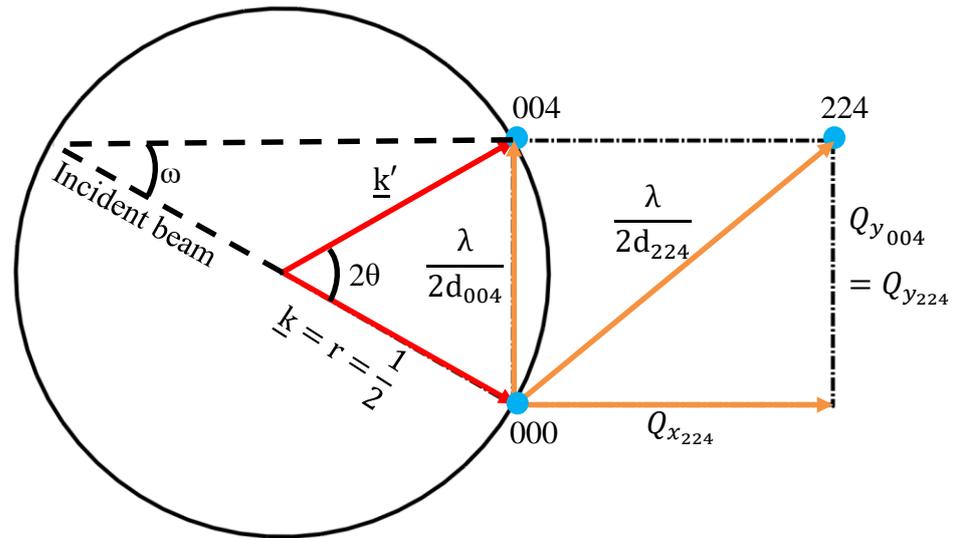


Figure 3.11: Diagram of the Ewald sphere intersecting the 004 Bragg peak showing the satisfaction of Bragg's law for the (004) plane. \underline{k} is the incident wavevector and \underline{k}' is the diffracted wavevector. The origin of reciprocal space is shown as 000. The radius of the Ewald sphere is $r = \frac{1}{2}$ and the reciprocal lattice units are $\frac{\lambda}{2d_{hkl}}$. The distances of the 004 and 224 Bragg peaks are shown with respect to the origin as reciprocal lattice units.

If the incident x-ray beam wavevector, \underline{k} , is plotted in reciprocal space, the locus of all possible scattered wavevectors will describe a sphere known as the Ewald sphere as shown in figure 3.11. When the Ewald sphere intersects with a Bragg peak in reciprocal space then Bragg's law is satisfied and diffraction occurs along those sets of planes.

3.2.3. Structure factor and conditions to meet Bragg's law

When selecting planes to carry out XRD on crystals, an important parameter to consider is the structure factor, F_{hkl} . This parameter determines the intensity of the diffracted X-ray signal which is obtained by summing all the waves with wavevector, \underline{k} , scattered from each atom whilst taking into account the scattering factor and phase of the wave over the unit cell [125]. For a crystal with planes, hkl , the structure factor is given by the following relationship:

$$F_{hkl} = \sum_i f_i (e^{-2\pi i(hx_n + ky_n + lz_n)}) \quad (\text{Equation 3.7})$$

Where: f_i is the atomic form factor of the n^{th} unit cell and x , y and z are vectors for the position of each atom in the unit cell. For Si and Ge, atoms are located at $[0,0,0]$, $[\frac{1}{2}, 0, \frac{1}{2}]$, $[\frac{1}{2}, \frac{1}{2}, 0]$ and $[0, \frac{1}{2}, \frac{1}{2}]$ in the unit cell (figure 2.1). By solving the equation above with these points, a non-zero structure factor (and visible Bragg peak) is obtained when h , k and l are all odd or all even. However, as the Basis also contains atoms at $[0,0,0]$ and $[\frac{1}{4}, \frac{1}{4}, \frac{1}{4}]$ as well, therefore solving equation 3.7 with these points gives a second condition for Bragg peak visibility; $h+k+l$ must not be an odd multiple of two. The square of the structure factor gives the intensity of the diffracted signal and it has been found that for a symmetrical scan the (004) plane and for an asymmetrical scan the (224) plane gives a some of the strongest signals. With zinc blende crystals such as InSb and AlSb due to the reduced number of symmetry operations compared to FCC diamond, the structure factor calculations show that the 002 reflection is also accessible [126]. The 002 would be weaker than the 004 peak for zinc blende materials, however in this investigation both $\text{Si}_{1-x}\text{Ge}_x$ epilayers and consequent AlSb/InSb layers, the 004 reflection was used for simplicity of alignment. Figure 3.12 shows the orientation of the (004) and (224) planes for FCC diamond crystals.

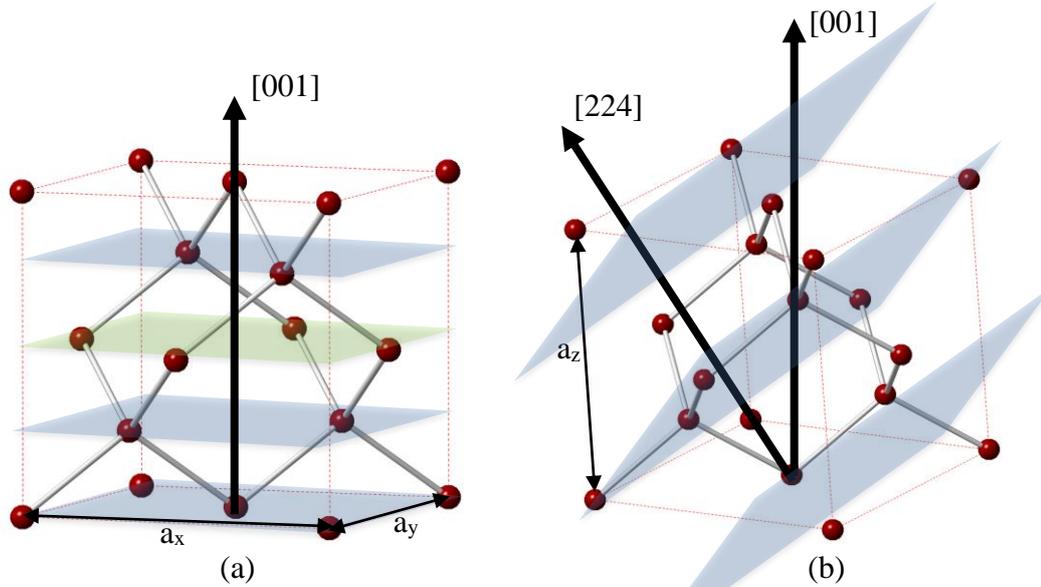


Figure 3.12: (004) crystal planes (a) and (224) (intercepts at $[\frac{1}{4}, \frac{1}{4}, \frac{1}{2}]$) planes (b) for FCC diamond crystals. The arrows shown are the surface normal vectors. The green plane in figure (a) shows the (002) plane that obeys the structure factor equation for zinc blende crystals and therefore is allowable.

Additionally, due to the limited movement of the X-ray source and detector angles, certain reflections maybe difficult to physically measure. For cubic materials with a lattice constant, a , the value for, d , in Bragg's law in equation 2.6 and shown in figure 2.4 is given by:

$$d_{hkl} = \frac{a}{\sqrt{h^2+k^2+l^2}} \quad (\text{Equation 3.8})$$

For a desired reflection, d_{hkl} can be calculated and thus θ_{hkl} can be determined from equation 2.6. For the 004 reflection since the surface plane is parallel to the (001) plane a correction to the [001] normal is not required, however for the (224) plane only a component of the vector lies parallel to the (001) plane therefore a correction is required given by the following equation:

$$\theta_{\text{correction}} = \left[\frac{(h_{\text{normal}} \times h) + (k_{\text{normal}} \times k) + (l_{\text{normal}} \times l)}{\sqrt{((h_{\text{normal}}^2 + k_{\text{normal}}^2 + l_{\text{normal}}^2) \times (h^2 + k^2 + l^2))}} \right] \quad (\text{Equation 3.9})$$

For the (224) plane the tilt corrected angle along the [001] direction is 35.36°. This value is subtracted from the calculated Bragg angle for 224 scans.

Relaxed layer	θ_{hkl} (°)		
Si ₀₀₄	34.5645		
Ge ₀₀₄	32.9962		
AlSb ₀₀₄	30.1451		
InSb ₀₀₄	28.3963		

Relaxed layer	θ_{hkl} (°)	Tilt corrected angle from (001) normal θ_{hkl} (°)
Si ₂₂₄	44.0144	8.7544
Ge ₂₂₄	41.8341	6.5741
AlSb ₂₂₄	37.9561	2.6961
InSb ₂₂₄	35.6400	0.3800

Table 3.1: Bragg angles for Si, Ge, AlSb and InSb for the 004 and 224 reflections including the tilt corrected angles for the 224 reflections. The tilt corrected angle for InSb₂₂₄ is very small however it is still obtained and so a different asymmetric reflection was not chosen for the InSb layer.

The 004 scan is used to measure layer tilt. The asymmetric 224 scan is used to give in-plane (a_{\parallel}) and out of plane (a_{\perp}) lattice constants, that are corrected for tilt.

3.2.4. ω - 2θ coupled scans and reciprocal spacing mapping

A rocking curve is a particular type of XRD scan where ω is kept fixed to the Bragg angle of substrate crystal and the detector angle, 2θ , is rotated so that a plot of intensity vs ω can be generated (since $\omega = \frac{1}{2}(2\theta)$). A coupled scan is a collection of individual rocking curves, i.e. ω is rotated as well within a range, and therefore $\omega = \frac{1}{2}(2\theta) + \text{offset}$. The benefit of carrying out coupled scans is that the true Bragg angle for a epilayer will be uncovered with little to no uncertainty. For example, high defects in the layer can cause mosaicity brought about through misaligned nucleation [125]. From the ω , 2θ and intensity values obtained from coupled scans, the Bragg peaks for the various epilayers can be plotted on a map in reciprocal space as shown in figure 3.13. If the incident angle is rotated through 180° around the sample i.e. from one edge of the sample to the other, a region of reciprocal space is mapped out. However not all regions are uncovered as some regions are deemed forbidden as shown by the blue

in Chapter 9: Appendices of this thesis in equations 9.1 to 9.31. The steps are shown, taking a Ge epilayer as an example however the equations can be used to calculate lattice constants for $\text{Si}_{1-x}\text{Ge}_x$ layers then subsequently using equations 9.32 to 9.36 to calculate Ge composition and then using equation 2.11 to calculate the bulk lattice constant of the alloy.

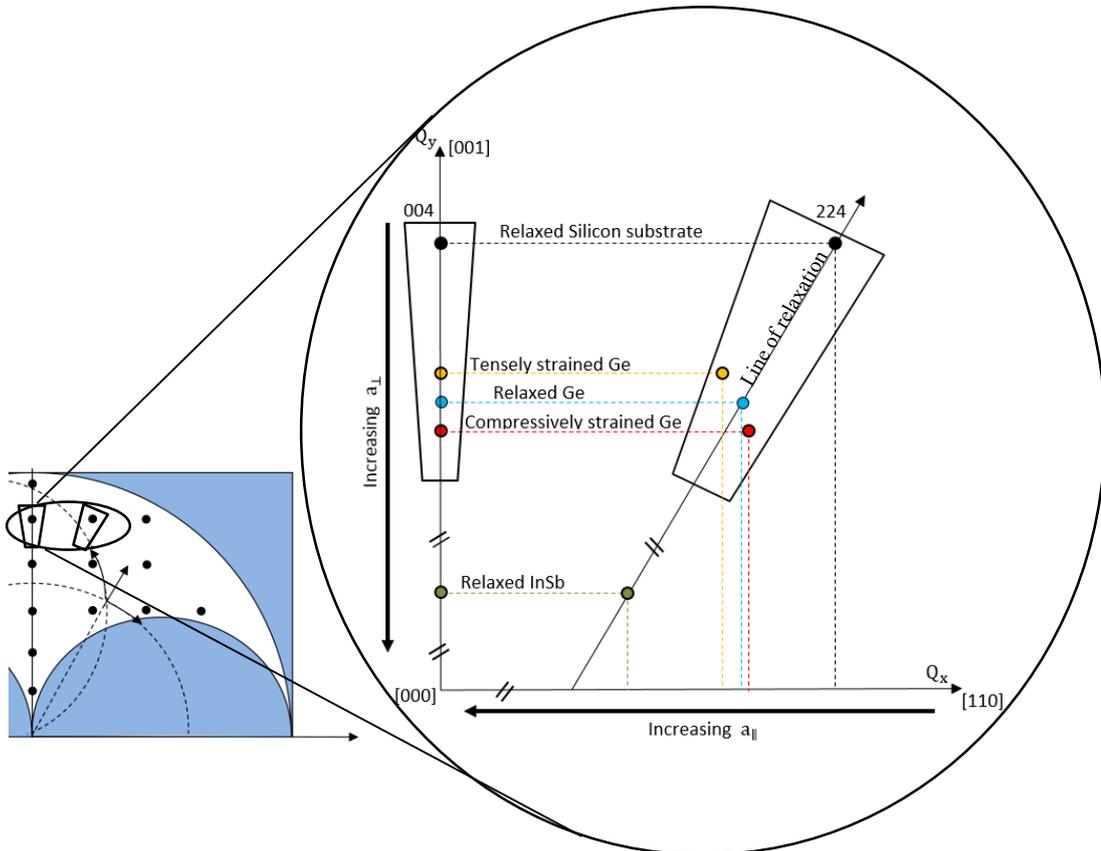


Figure 3.14: Analysis of 004 and 224 RSMs. The InSb layer is included to show peak positioning based on lattice constant of the crystal. The larger the lattice constant in bulk form, the closer the peak sits towards the origin [000].

Figure 3.14 shows an example RSM of multiple epilayers grown on a Si(001) substrate in 004 and 224 reflection. Silicon has the smallest lattice constant so in both the 004 and 224 scans it sits furthest away from the origin, whilst the InSb layer has the largest lattice constant and so sits closest to the origin. The Ge epilayer can be fully relaxed (blue), tensely strained (yellow) or compressively strained (partially or fully) to the substrate. The 004 reflection cannot be used to give out of plane or in-plane lattice parameters, it is used to determine and correct tilt with respect to the silicon substrate. However, any change in strain in the layer will be observed as a peak shift along Q_y

in 004. Any tilt observed in 004 could be due to defects in the layer, strain or intentional off-cut. The substrate peak is expected to be sharp and small (limited only by instrument broadening), since it is assumed to be a perfect crystal wafer with $< 10^{-2} \text{cm}^{-2}$ TDD. As the peaks in the epilayers broadens along Q_x , this indicates mosaicity of the epilayer which causes the rise of a periodic strain fields from small blocks single crystalline regions due to misfit dislocation interactions. Surface and interface roughness also contributes to the spreading of peaks, particularly in multi-epilayer structures.

In the 224 reflection, any level of insufficient strain relaxation in the epilayer, will be witnessed as additional tilt. If the epilayer is un-tilted in 004 and fully relaxed, then it should lie along the “line of relaxation” which lies from the substrate peak to the origin. The Q_y coordinate are the same for 224 and 004 relaxed peaks.

3.2.5. RSM measurements on off-axis substrates.

Finally, when carrying XRD experiments on samples grown on offcut substrates, the sample mounting orientation needs to be considered. Because of the heavy step and terrace surface on off-axis wafers the Bragg angle for 004 and 224 scans will not be at the positions in table 3.1. Depending on whether the sample is mounted with the offcut direction perpendicular or parallel to the X axis on the stage, either a wide ω scan or a wide χ scan is required to find the silicon peak and align onto the substrate.

As shown in figure 3.14, the incident beam will have to move to a position where the surface normal vector is along the [001] direction. If the sample is orientated as is shown in figure 3.14, a wide ω scan is required, this means that the ω scanning angle should be $\theta_{\text{Si}_{\text{hkl}}} \pm 10^\circ$ as opposed to $\pm 1^\circ$ for on-axis substrates in order to detect the required Bragg angle. A $\pm 10^\circ$ wide scan with large intervals is carried out because the off-axis wafers have an off-cut of 6° and such a wide scan guarantees that the substrate peak will be picked up. Depending on whether the (110) plane of the sample was on the left or right hand side, the off axis ω angle was either $\theta_{\text{Si}_{\text{hkl}}} + 6^\circ$ or

$\theta_{Si_{hkl}} = 6^\circ$. Once the off-axis substrate had been aligned, the setup is then zeroed with the offset recorded.

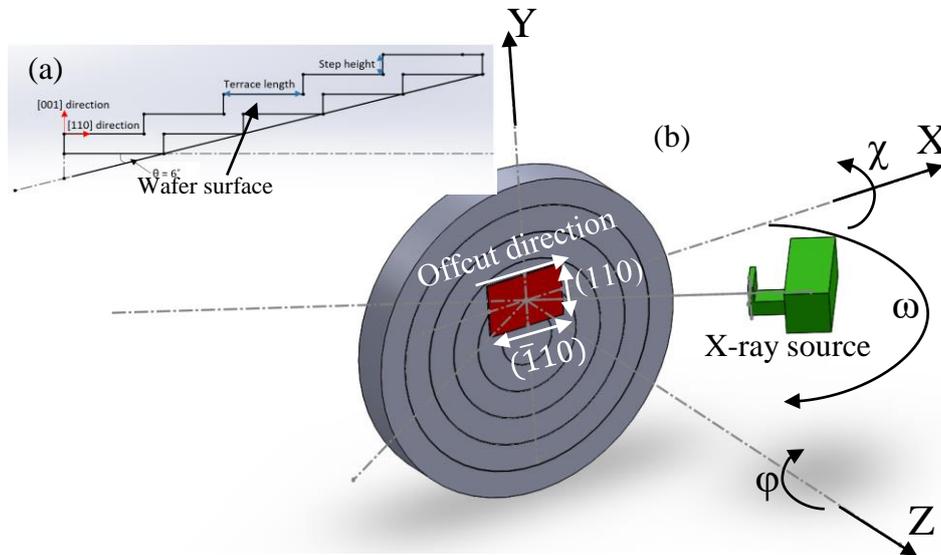


Figure 3.15: Figure (a) shows the step and terrace surface of an off-axis substrate. Figure (b) shows the importance of sample orientation of the off-axis grown sample with (110) plane perpendicular to the incident beam in order to initially align to the substrate. If the sample was mounted with the (110) plane horizontally and the $(\bar{1}10)$ vertically then a wide χ scan wide be required to pick up the substrate peak.

3.3. Atomic Force Microscopy (AFM).

3.3.1. Principles of AFM

The Veeco Multimode AFM with the Nanonis SPM controller in both contact and tapping modes were used. Figure 3.16 (a) is an image of the instrument, figure (b) is an example SEM image of the SiN cantilever tip used.

The principle behind atomic force microscopy is to measure the force exerted on a sample surface by a cantilever tip as a function of distance as the tip is tracked along the sample surface resulting in a topographical representation of the surface. The cantilever is made from silicon nitride and the tip has a width of 8 to 10nm. This means that the tip is unable to resolve features that are less than 10nm apart. In this study a minimum scan size of 50nm x 50nm scans were obtained in tapping mode by adjusting the gains.

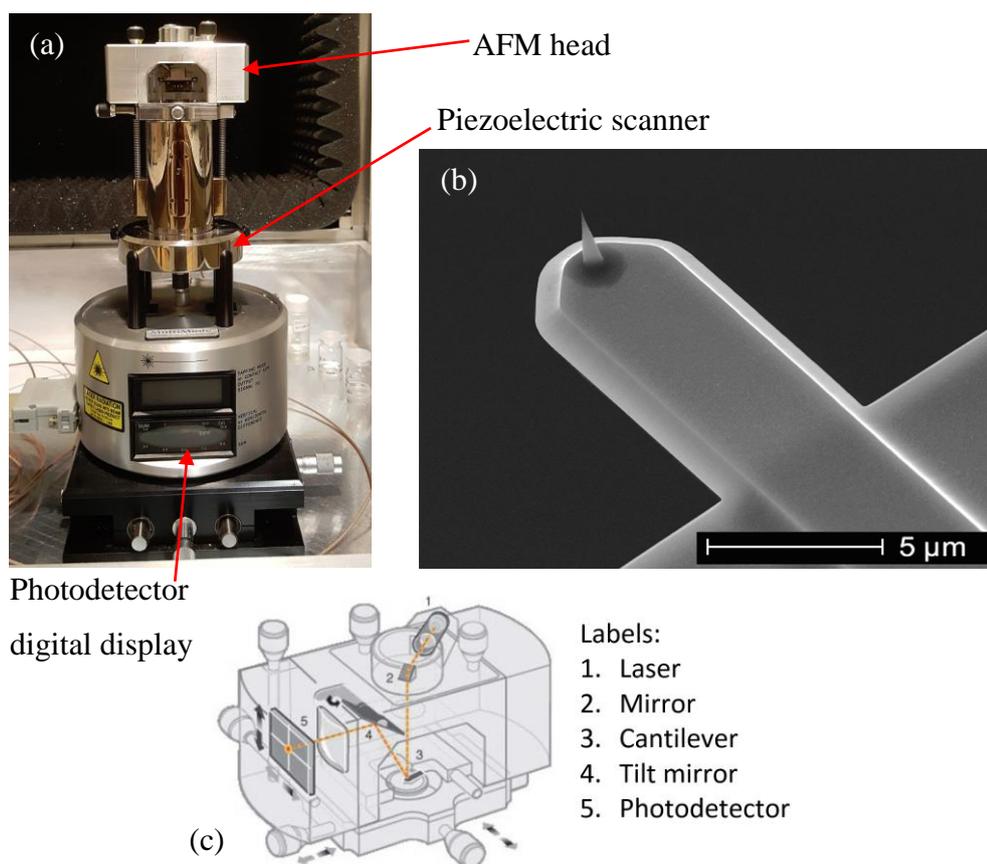


Figure 3.16: (a) Veeco Multimode AFM, (b) SiN AFM cantilever and tip [127] and (c) AFM head with labelled parts [128].

Figure 3.17 shows the tip-sample interaction forces using the tip-sample Lennard-Jones potential, $U_{ts}(z)$ (equation 3.12). This equation describes the interaction between two neutral atoms (one on the cantilever tip and another on the sample surface) and consists of two parts: 1) a term describing the van der Waals attractive forces and 2) the repulsive forces [129]:

$$U_{ts}(z) = 4U_0 \left[\underbrace{\left(\frac{z_a}{z}\right)^{12}}_{\substack{\text{repulsion} \\ \text{(short range)}}} - \underbrace{\left(\frac{z_a}{z}\right)^6}_{\substack{\text{attraction} \\ \text{(long range)}}} \right] \quad (\text{Equation 3.12})$$

Where: Z_a is the tip-sample distance at which $U_{ts}(z) = 0$, U_0 is the depth of the potential well and, z , is the radius between atoms. Differentiating the Lennard Jones potential with respect to, z , gives the corresponding force between tip and sample, F_{ts} . Figure 3.16 shows a plot of F_{ts} vs $\frac{z}{z_a}$ (in red). The vertical black dashed line represents the boundary where the forces transition from repulsive forces between atoms to Van der Waals attractive forces.

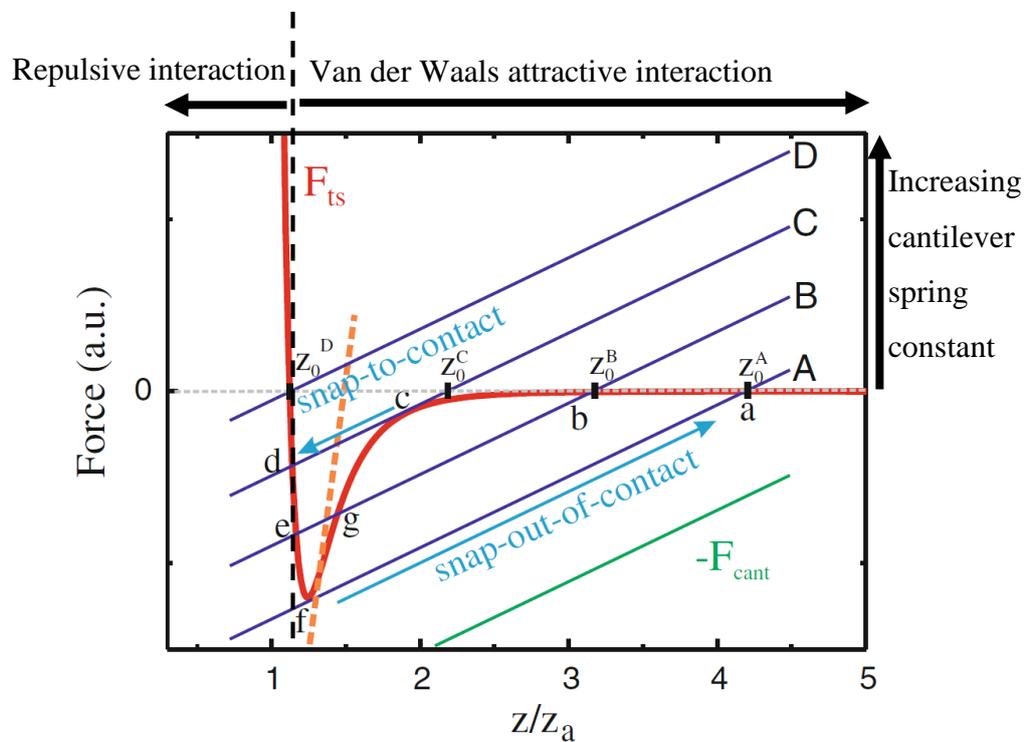


Figure 3.17: Lennard-Jones force between sample and tip, F_{ts} (red), plotted with cantilever spring constant forces (in blue) the gradient of which is k . Taken from Voigtlander [129].

The cantilever can be treated like a spring and so obeys Hooke's law for different vertical deflections along, z , where z_0 is the zero-point deflection and k is the spring constant:

$$F_{\text{cant}}(z, z_0) = k(z - z_0) \quad (\text{Equation 3.13})$$

Equation 3.13 can be integrated with respect to z to give the cantilever spring potential, U_{cant} . If the cantilever is far from the sample surface, i.e.: a large z_0 , a stable spring potential minimum is obtained at $z \approx z_0$. As the tip is brought closer to the sample surface, the potential minimum close to z_0 vanishes due to stronger attractive forces and a new stable potential minimum will be found that is closer to the sample surface. This is explained in figure 3.17. Points 'a' to 'c' show the cantilever approaching the sample surface, where $\frac{\delta F_{\text{ts}}}{\delta z} < k$ holds. Points 'b' and 'e' correspond to two minimum potentials and point 'g' corresponds to a potential maximum in between. When the tip reaches Z_0^c , $\frac{\delta F_{\text{ts}}}{\delta z} > k$ and the tip jumps from an unstable point 'c' to the stable potential minimum point 'd'. This is known as snapping to contact. At point 'f' snap out of contact takes place because $\frac{\delta F_{\text{ts}}}{\delta z}$ again becomes larger than the spring constant, k as z/Z_a increases (i.e.: when the tip retracts from the surface).

3.3.2. Scanning modes:

3.3.2.1. Contact mode

In contact mode the tip makes full contact with the sample surface. The sample is first mounted on a stage. A laser beam is fired at the cantilever top surface, and the reflected beam is adjusted to strike at the centre of a photodetector as shown in figure 3.15 (c). A triple axis piezoelectric scanner is positioned underneath the sample, where the z direction is perpendicular to the sample surface (001).

As the sample is moved under a stationary tip over a cross sectional area, feedback is provided from the photodiode to maintain a constant laser deflection by adjusting the sample in the z direction using the piezoelectric scanner. The Nanonis software records

the z position at each x and y position of the scan and hence a topographical image of the sample can be gathered.

3.3.2.2. Tapping mode

In tapping mode, the cantilever is oscillating. Snap to contact would stop the oscillation due to the very narrow potential minimum close to the surface and so it must be prevented. This is achieved by using cantilevers with a larger spring constant, k . If the gradient of F_{cant} line is greater than the F_{ts} curve, then snap to contact never occurs as shown by the orange dashed line figure 3.16.

Another method to prevent snap to contact is by using large oscillation amplitudes which results in $F_{\text{cant}} > F_{\text{ts}}$. This can be achieved by ‘tuning’ the cantilever to its resonant frequency thus achieving maximum amplitude.

The benefit of carrying out contact mode AFM is that large scan sizes can be obtained. In this investigation up to $100\mu\text{m} \times 100\mu\text{m}$ scans were carried out. If the sample is relatively sturdy, then contact mode should be the preferred choice to scanning a sample as it gives a complete topographical representation of the surface without missing any features. However, if the sample is relatively fragile such as suspended membranes then tapping mode serves as the better scanning method since snap to contact could destroy the membrane [130].

Additionally, tapping mode allows for higher resolution scans since constant contact isn’t made to the sample surface the sample z height is constantly adjusted to maintain a fixed oscillation amplitude which allows for higher resolution of the scan in the z direction. The scan resolution is limited by the width of the tip and so in this investigation the highest resolution scan that was able to gather any data was at $100\text{nm} \times 100\text{nm}$.

3.3.3. Image analysis

In both contact and tapping mode, the proportionality and time constants can be adjusted in the software as can the scanning speed. Generally, a scanning speed of 0.5sec/line was used for most samples, however for dense features, such as the facets in low temperature Ge buffer layers (chapter 4) a much slower scan speed of 4 sec/line was used to resolve the shape of the features. Image analysis of the scans was carried out using Gwyddion SPM software. In unprocessed AFM images surface artefacts caused by tip shape, scanner hysteresis and dirt on the sample have to be removed before extracting data such as rms roughness (R_{rms}) and z-height.

The first step of image processing involves calculating and subtracting a plane from all the image data points. The second is to remove noise using an n^{th} order polynomial function from the data in both the x and y directions. Selecting a value of value of n where no further increase in n causes considerable to change to R_{rms} . The third step is to use a height median tool to remove any horizontal lines (artefacts caused by rastering the tip across the sample) that were created when scanning the sample. If additional scarring is seen on the scan in limited region due to dirt, a mask can be applied and subtracted from the main scan.

Whether doing contact or tapping mode, to ascertain the true roughness of the surface of the sample the sample should be scanned across a range of scan sizes. With contact mode the scan size ranges from $1\mu\text{m} \times 1\mu\text{m}$ to $100\mu\text{m} \times 100\mu\text{m}$. Whilst with tapping mode the scan sizes range from $100\text{nm} \times 100\text{nm}$ to $50\mu\text{m} \times 50\mu\text{m}$. If y_i is the horizontal deflection from that of the ideal surface, then the rms roughness (R_{rms}) is given as:

$$R_{rms} = \sqrt{\frac{1}{n} \sum_{i=1}^n y_i^2} \quad (\text{Equation 3.14})$$

The R_{rms} is determined when the scan size is large enough to maximise the mean number of deflections from the ideal surface.

3.4. Differential Interference Contrast (DIC) Optical Microscopy

Based on the Rayleigh criterion (equation 3.2), standard optical microscopes have a limit to resolution. DIC optical microscopy (also referred to as Normaski microscopy) allows small surface features to be seen through optical interference contrast in a non-quantitative manner.

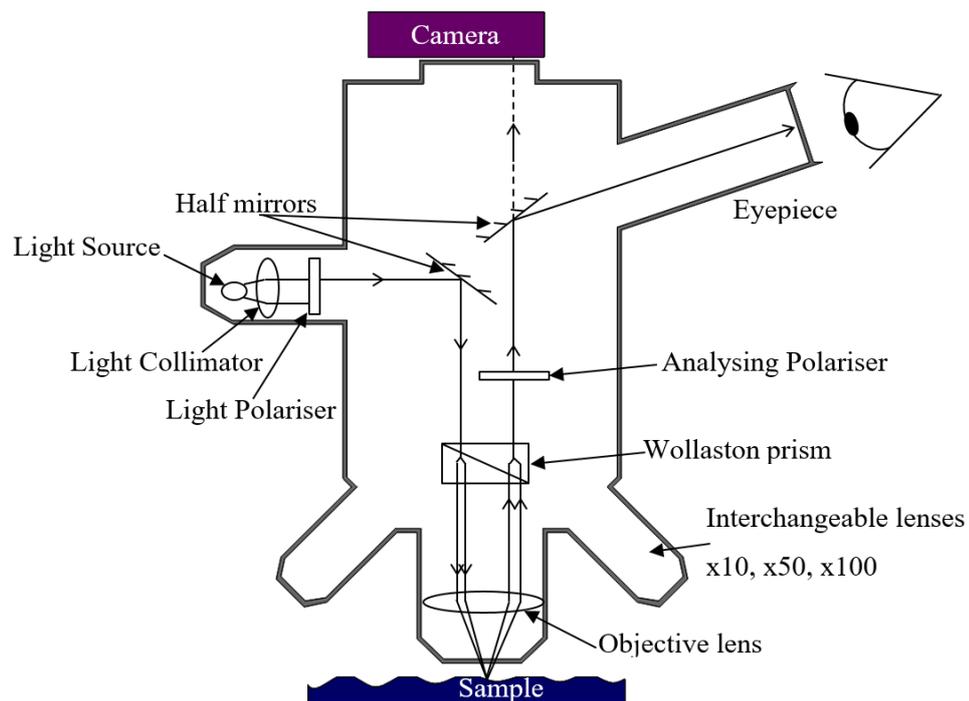


Figure 3.18: Diagram of a DIC (Normaski) optical microscope. Adapted from Nash [131].

The technique involves first collimating and polarising light from a source, which is then brought into the microscope. The light is reflected by a half mirror to a Wollaston Prism which splits the beam into two perpendicular beams. The Wollaston prism aids in further polarisation and prevents further interference between the beams. The two beams are then focused on the sample and then reflected back through the prism where they are recombined. The beam is then passed through an analysing polariser that is perpendicular to the light polariser at the source. The polarisation difference causes depth interference contrast, which allows features on the surface of

the order of nm's to be seen. The image is then seen through the eyepiece or captured using a CCD camera for analysis.

DIC optical microscopy was used to image etched samples and obtain counts of TDD. The optical microscope used was a Zeiss Axioimager with attached CCD camera.

3.5. Selective Defect Etching.

As mentioned in section 2.5, threading dislocations do not contribute to strain relaxation much and have a line vector component along the [001] direction which means that they appear on the epilayer surface and disrupt any devices made on the epilayer or serve as nucleation points in further epitaxy on the surface.

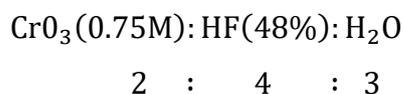
The lowest magnification on the JEOL 2000 TEM is x1000. At this magnification if the TDD density is $\leq 1 \times 10^7 \text{ cm}^{-2}$ then the threading dislocation (TD) coverage is not ubiquitous enough to obtain images of the sample that have roughly the same number of TDs from image to image and hence a low enough standard deviation between images to get an accurate count of TDD. Therefore, other techniques have to be employed to measure TDD.

Along with plan view TEM and AFM, wet chemical defect etching was used to analyse samples for TDD depending on the density. As a general rule if the TDD density was less than $1 \times 10^8 \text{ cm}^{-2}$, then defect etching was an acceptable method to determine dislocation densities because at this amount anisotropic etching would not cause adjacent dislocations to coalesce and contribute to errors in the measurements. If the sample TDD was in between $1 \times 10^8 \text{ cm}^{-2}$ and $1 \times 10^9 \text{ cm}^{-2}$ then AFM was used to make the measurement. Finally, if the sample had a TDD greater than $1 \times 10^9 \text{ cm}^{-2}$ then plan view TEM was used as the TDD measurement method. Using wet etching methods, the TDD count was obtained through DIC optical microscopy, where 10 to 15 random images of the etched sample were taken, the etch pit density counted per image and then averaged to give a TDD for the sample.

In this investigation, the etching experiments were limited to the linearly graded and reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers in chapter 5 and the reverse terrace graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers in chapter 6. The principle behind etching is a continuous oxidation of the sample and removal of the oxide with a reducing agent.

3.5.1. Dilute Schimmel etchant.

The composition of the dilute Schimmel etchant is as follows:



The ratios given are as volume parts and the calculations are given in the appendices: section 9.2. The oxidising agent is the CrO_3 and the reducing agent is the HF. In a standard Schimmel etchant solution, only 150ml of de-ionised H_2O is required [132]. In this study however, 250ml of de-ionised water is used to slow down the etch rate. The reason why this was done was because in select samples of linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers, unintentional in-situ HCl etching during growth in the RP-CVD chamber of the layer was observed, as will be explained in chapter 5. The tell-tale sign of these pits is the inverted pyramids as seen by Hartmann et al when intentionally introducing HCl gas into the chamber between 772° for $\text{Si}_{0.8}\text{Ge}_{0.2}$ and 700°C for $\text{Si}_{0.5}\text{Ge}_{0.5}$ [133], [134]. In order to see how the HCl pits change in dimension around the threading dislocations during the Schimmel etch process, the etch rate was slowed down.

The Schimmel etchant has been shown to be effective for low Ge content layers due to its anisotropic behaviour i.e.: it etches the $\langle 001 \rangle$ planes faster than any of the other planes [135]. This is a particularly useful phenomenon as the threading dislocations lie on $\langle 111 \rangle$ glide planes, and so this etchant etches the material on the $\langle 001 \rangle$ planes more quickly therefore enlarging the threading dislocations into larger pits that are visible under an optical microscope or scanning electron microscope which can then be counted to give a value of threading dislocation density.

Previous studies on Schimmel etch rate vs Ge composition have yielded the following results:

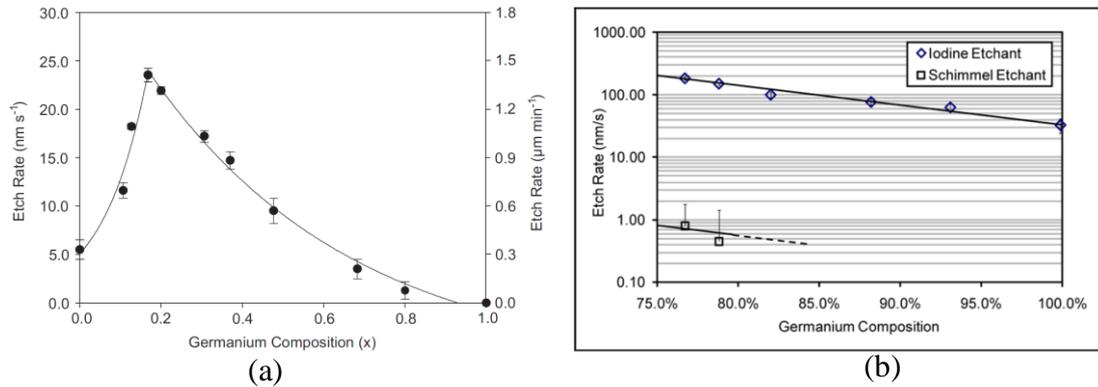


Figure 3.19: (a) Ge composition in $\text{Si}_{1-x}\text{Ge}_x$ vs Schimmel etch rate investigation carried out by J.Parsons in 2007 [136] and (b) Ge composition in reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers vs Schimmel and Iodine etch rate carried out by Shah in 2009 [96].

Figure 3.19 (a) shows how the Schimmel etch rate reaches a maximum when the Ge content in the layer is approximately 0.2 however after $x=0.2$ the etch rate drops until it reaches 0 when $x=0.92$. Figure 3.19 (b) is a etch rate comparison plot created in the work carried out by Shah in 2009 [96], where Iodine etchant was predominantly used as the Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ buffer layer samples was $1 \geq x \geq 0.75$ and so Schimmel etchant was not very effective.

In chapter 5 of this study linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer samples lay within the region $0.636 \geq x \geq 0.09$ and reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ samples lay within $0.708 \geq x \geq 0.45$ region and so the Schimmel etchant was predominantly used in this investigation.

3.5.1.1. Etch rate comparison technique

With this further diluted Schimmel etchant, the etch rate for linearly graded and reverse linearly graded samples was measured and plotted as is explained in Chapter 5.

The process involves applying a protective Apiezon W black wax to a section of the sample with is etch resistant. The sample is then etched for a measured amount of time and then rinsed in de-ionised water. The sample is then taken and immersed in toluene (C_7H_8), which dissolves the wax. The sample thus has a region which was protected from etching and a profilometer is used to measure the step height difference between

the etched and un-etched regions of the sample. The etch rate is then calculated as step height difference divided by etching time.

4. Low temperature (LT) epitaxy of ultra-thin pure Ge buffer layers on Si(001) using RP-CVD.

4.1. Background on pure Ge buffer layers.

4.1.1. Development of the LT/HT Ge buffer layer

Over the last thirty years various epitaxy techniques have been used to create high quality germanium buffer layers on Si(001) for various applications (see chapter 1). The quality of pure germanium buffer layers deposited straight onto Si(001) varies depending on the technique used. The key issues being to mitigate the 4.2% lattice mismatch and the thermal expansion coefficient mismatch between Si and Ge.

Since 1998 ultra-high vacuum CVD was first used by Colace et al [137] as an alternative to MBE to quickly deposit Ge thin films onto Si(001) substrates for photodetector applications using a two temperature approach and GeH_4 as the precursor. The base pressure was 1×10^{-9} Torr. The low temperature (LT) layer is thin and is approximately 30 to 60nm thick and grown between 330°C and 350°C. The surfactant properties of hydrogen at low temperatures allows the suppression of Volmer-Weber island growth and instead 2D Frank-Van de Merwe growth takes place through the heavy formation of dislocations to promote strain relaxation. The surface is consequently very rough and a high density of the dislocations propagate to the surface. Once planar growth has been established, a thicker high temperature (HT) layer between 200nm to 4 μm thick (depending on the final application) is grown at 600°C. Additionally, 10 cycles of thermal annealing was employed at temperatures between 780°C and 900°C to improve the film quality and reduce threading dislocations even further. This had the effect of giving threading dislocations enough energy to glide & annihilate and create a smoother surface with a roughness of $\leq 1\text{nm}$ and TDD of $2.3 \times 10^7 \text{ cm}^{-2}$.

A similar two step UHV-CVD process was taken by Luan et al in 1999 [138] at identical growth temperatures, pressures and to identical LT/HT thicknesses. With this

particular study, two temperature germanium was grown on patterned wafers as well as a means of using the technique of aspect ratio trapping to further reduce threading dislocation densities.

Alternatively pure germanium buffer layers were achieved through linearly grading SiGe layers, starting from pure silicon at the substrate to pure germanium at the top of the epilayer as carried out by Currie et al in 1998 [116]. However, the grading rate of the $\text{Si}_{1-x}\text{Ge}_x$ layer had to be kept low at 10% Ge/ μm in order to prevent high surface roughening. This meant that the layers were over 12 μm thick and due to the thick graded layers there was a propensity for the films to crack under strain. Compressive strain relaxation, the low grading rate and thick graded layers also meant that large arrays of misfit dislocation networks were created which produces dense crosshatch features from strain fields. Threading dislocation “pile-up” is also a problem as explained in section 2.5.8.4. To counter the emergence of high surface roughness and the dislocation pile-up, the wafers are polished using chemical and mechanical methods upon linearly grading to 50% Ge. This had the effect of reducing the TDD count in the Ge epilayer on the surface by 10 times to $2 \times 10^6 \text{cm}^{-2}$ and halving the rms roughness to 24nm, which was still very high.

Early work by Hartmann in 2004 [139] had investigated Ge grown on Si(001) using RP-CVD at 400°C to deposit a seed layer which was roughly 25nm thick followed by high temperature growth (between 400°C to 750°C) upto a thickness of 1660nm. 10 cycles of annealing at 750°C for 10 mins followed by at 850°C for another 10 mins showed that the tensile strain relaxation in the layer jumps from 103% to 109% and the rms roughness increases from 0.6nm to 2nm. The TDD level was $< 2 \times 10^8 \text{cm}^{-2}$. However chemical and mechanical polishing steps were used along with a 700°C H_2 bake in this investigation to bring the roughness down to 0.5nm.

More recently in 2011 Shah et al created high quality Ge epilayers using the two temperature method where the LT layers were grown at 400° and were between 30 to 150nm thick. The high temperature layer was grown at 670°C and the total buffer layer is between 760nm and 1.2 μm thick [140]. The relaxation of a 400°C Ge layer was found to increase with thickness and for a 150nm thick low temperature layer a

relaxation of 95.8% was measured, which means some compressive strain remains in the layer, and a TDD of $6.1 \times 10^{10} \text{cm}^{-2}$. The thicker HT Ge layers show a drop in TDD drop from 2×10^8 to $4.6 \times 10^7 \text{cm}^{-2}$. This is due to a higher thermal budget being supplied to the layer to allow faster glide velocities and leading to annihilation. A single H₂ annealing stage at 830°C has also been shown to reduce TDD from 1×10^8 to $1 \times 10^7 \text{cm}^{-2}$ for the thickest layers but at the cost of imparting tensile strain to the layer and leaving the total Ge layer 104.4% relaxed.

Recent investigations into temperature ramping in between the 400° and 600° layers has also shown to be effective in producing high quality Ge buffer layers with TDD of $3 \times 10^6 \text{cm}^{-2}$ and R_{rms} of 0.621nm [141]. The explanation to this is given that the low temperature growth rate provides sufficient time for thermal exposure, hence preventing a “thermal shock” due to a change from LT to HT growth and hence does not allow strong Stranski-Krastanov growth.

4.1.2. Additional techniques in obtaining relaxed Ge buffer layers with low defect densities.

In the quest for creating high quality Ge buffer layers for the integration of III-V compounds, other techniques have also been employed such as: magnetron sputtering and cyclic thermal annealing, as a lower cost and safer alternative to CVD deposition [142].

Selective epitaxy on patterned Si(001) substrates using SiO₂ features has also been used to grow LT(400°C)/HT(600°C) Ge buffer layers. In the work carried out by Park et al in 2007 [143], defect free Ge was created using the aspect ratio trapping methods where the aspect ratio, $AR = \frac{\text{trench height}}{\text{trench width}}$. For trench heights of 490nm, when $AR > 1$ most of the dislocations are trapped at the side walls of the SiO₂ features.

Other developments in selective epitaxy of pure Ge include those by Miglio et al [144] into deep patterning of Si(001) substrates using standard photolithography and deep

reactive ion etching to create 8 μm high Si(001) pillars using low energy plasma enhanced CVD. This technique has yielded unusually high quality 70 μm high Ge pillar crystals. The nature of the enormous 3D crystals is such that threading dislocations on the {111} glide planes are able to terminate on the sidewalls however vertical threading dislocations along the [001] direction, are only terminated on the surface facets of the Ge crystal. The facets on the surface ((001), {111}, {113} and {15 3 23}) of the Ge crystal is dependent on the growth temperature. 3D crystals of GaAs were subsequently grown on 2 μm high Ge pillars created on 6° offcut patterned substrates very recently using MOVPE [105]. The GaAs crystal apex is formed by {137} lateral facets symmetrically arranged around the [110] crystal direction and two main top surfaces: one parallel to (001) plane and another corresponding to the real GaAs (001) plane due to anisotropic growth causing tilt in the layer. Patterning has shown to reduce TDD through aspect ratio trapping means, however blanket coverage of the wafer is preferable over selective epitaxy especially if the III-V material that is grown is to be used for CMOS applications and large areas are required to manufacture more devices on an un-faceted planar surface.

4.2. This study on ultra-thin LT Ge buffer layers on Si(001) using RP-CVD.

The aim of this experiment is to improve upon existing state of the art “blanket” Ge buffer layers on un-patterned Si(001) on-axis substrates. In the background section of this chapter the LT/HT method has been discussed as being the best available compromise between thickness, roughness, TDD and strain relaxation.

This investigation aims to make contributions to the Ge buffer layer technology through two routes. Firstly, to see how the: strain, surface roughness and TDD varies

for thin Ge epilayers whilst growing in between $300^{\circ}\text{C} \leq T \leq 400^{\circ}\text{C}$ using RP-CVD. The thickness of the layer's ranges from 2nm up to 351nm.

The second part is a study into omitting the HT layer completely, by growing the LT layer only and then annealing this layer at 650°C for different lengths of time to promote TD glide. The reasons for wanting to keep the Ge buffer layer as thin as possible will be explained in chapter 5 on reverse linearly graded and reverse step graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers which are susceptible to cracking under tensile strain. By omitting the HT layer completely, firstly a reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layer can be made thinner. When considering devices on the Ge buffer layer or on the $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layer, thinner layers are preferable to allow heat energy to be transmitted into the substrate and dissipated, because Si(001) has a much higher thermal conductivity than Ge.

4.2.1. Thin LT Ge Buffer design

LT-Ge	$300^{\circ}\text{C} < T < 400^{\circ}\text{C}$	$2\text{nm} < t < 351\text{nm}$
p ⁻ Si(001)		

(a)

Anneal	$T = 650^{\circ}\text{C}$	1 min/5min
LT-Ge	$300^{\circ}\text{C} < T < 400^{\circ}\text{C}$	$20\text{nm} < t < 78\text{nm}$
p ⁻ Si(001)		

(b)

Figure 4.1: (a) LT Ge/Si(001) buffer structure. The Ge buffer layers in this low temperature study were grown between $T = 300^{\circ}\text{C}$ and 400°C . The thicknesses ranged from $(t) = 2\text{nm}$ to 351nm . (b) In the annealing study, the Ge buffer layers were grown between 20nm and 78nm thickness and then annealed for either 1min or 5mins.

The 100mm Si(001) substrates used in this chapter were on axis with a tolerance of $\pm 0.5^{\circ}$. The thickness of the substrates was $525\mu\text{m}$ and have a surface roughness of 0.1nm . An initial bake was used at 1000°C to remove the native oxide on the surface before depositing the Germanium. The growth pressure was 100 Torr and the GeH_4

flow rate was 150 sccm (standard cubic centimetres per minute) under 20,000 sccm of H₂.

4.2.2. List of samples:

400°C growth	
Sample number:	Ge buffer layer max thickness (nm) (+/- 5%)
15-42	8.3
15-41	12
14-295	24
15-40	50
14-296	72
15-39	94
14-297	122
14-298	175
14-299	267
15-38	351

Table 4.1: 400°C Ge growth temperature buffer samples

350°C growth	
Sample number:	Ge buffer layer max thickness (nm) (+/- 5%)
15-46	6.4
15-45	12.6
14-44	25
14-300	42

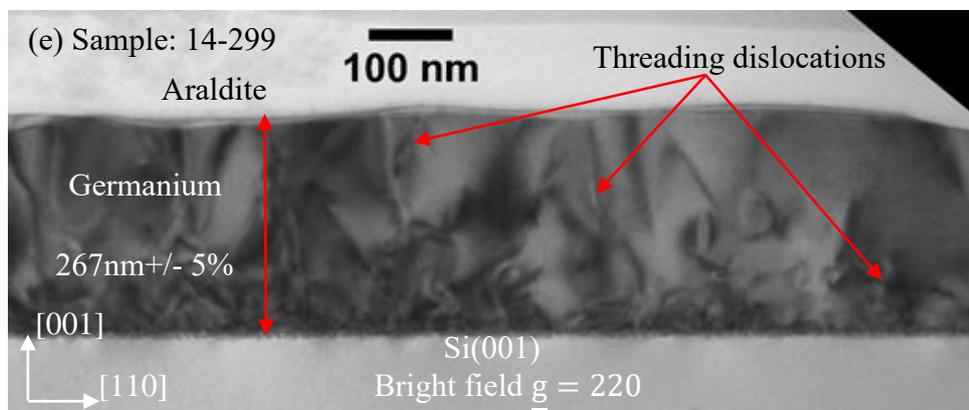
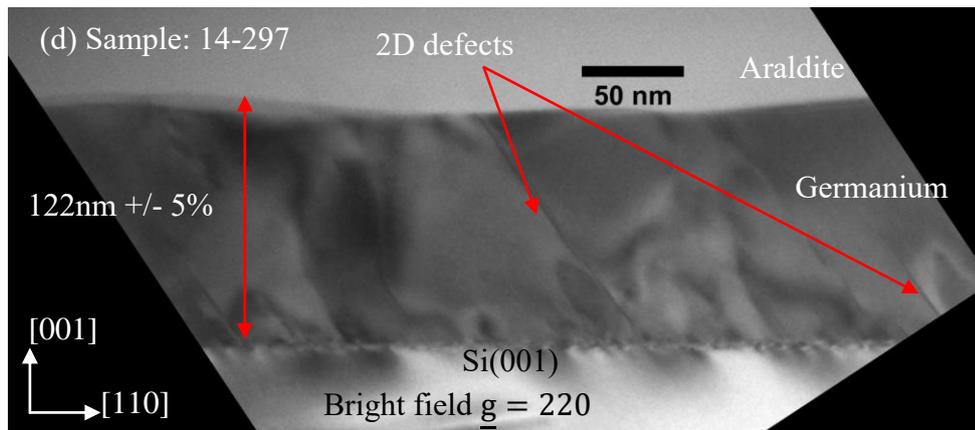
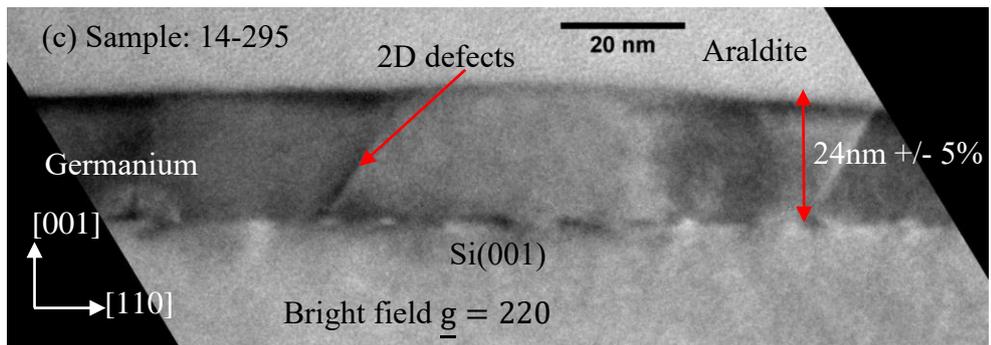
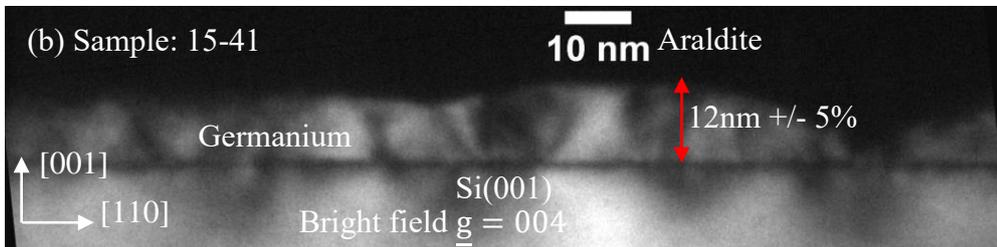
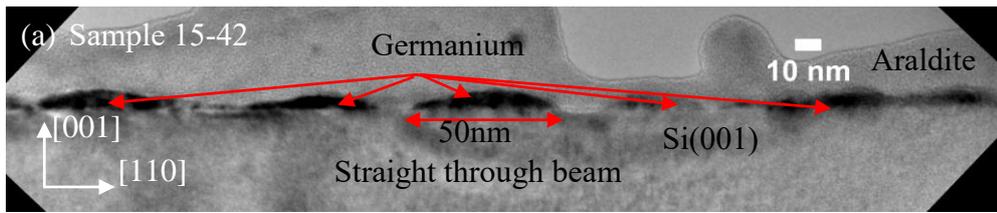
14-301	75
15-51	84
14-302	95
15-53	155
15-43	174

Table 4.2: 350°C Ge buffer growth temperature buffer samples

300°C growth	
Sample number:	Ge buffer layer max thickness (nm) (+/- 5%)
15-50	2
15-49	5
15-48	13
14-303	15
14-304	24
15-47	78.9

Table 4.3: 300°C Ge buffer growth temperature buffer samples

4.2.3. X-TEM comparisons of Ge buffer films grown at 400°C, 350°C and 300°C.



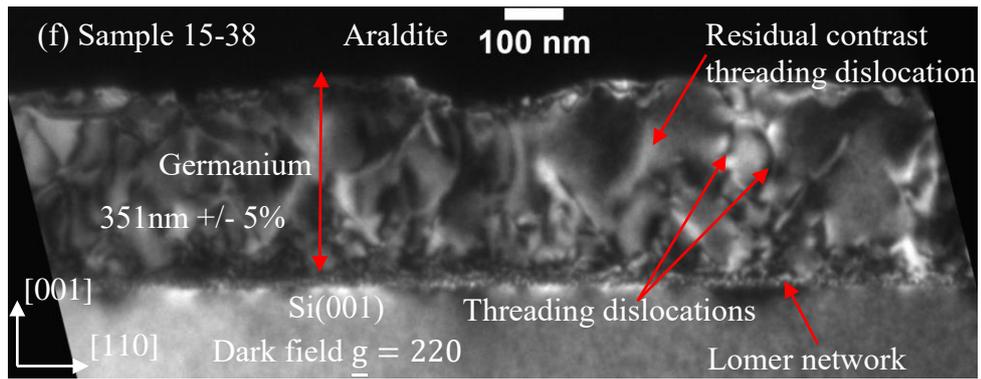
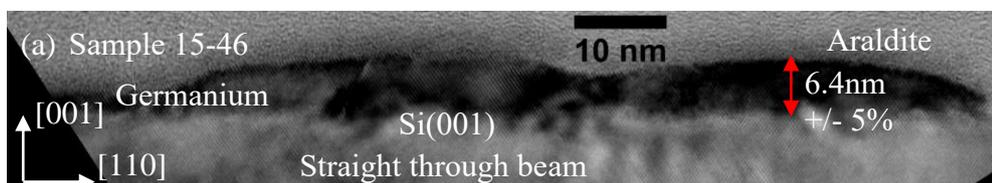


Figure 4.2: X-TEM of samples grown at 400°C. Samples: 15-42 (a), 15-41 (b), 14-295 (c), 14-297 (d), 14-299 (e) and 15-38 (f). Diffraction contrast TEM allows the thickness to be ascertained using the 004 diffraction condition.

Figure 4.2 shows how the Ge layer changes in film morphology with respect to increasing thickness when grown at 400°C and 100Torr pressure from the RP-CVD. From figure 4.2 (a) at 8.3nm thickness, the film has already transitioned from a wetting layer to 3D islands. The higher growth temperature means that adatoms have greater energy and longer diffusion lengths and 2D growth does not take place at all. From the cross sectional images, it can be seen that the surface roughness increases with thickness and so it can be surmised that at this growth temperature, lattice mismatch dominates over thermal mismatch hence the layer relaxes under compressive strain. The 4.2% mismatch creates a Lomer network at the interface to the substrate which appears to be present at all thicknesses. Visible threading dislocations are seen, particularly in thicker layers and are most likely caused by 60° misfit dislocations. Some threading dislocations show $\underline{g} \cdot \underline{b}$ residual contrast (figures 4.2 (e) and (f)), which suggest that they are most likely caused by Lomer climb.



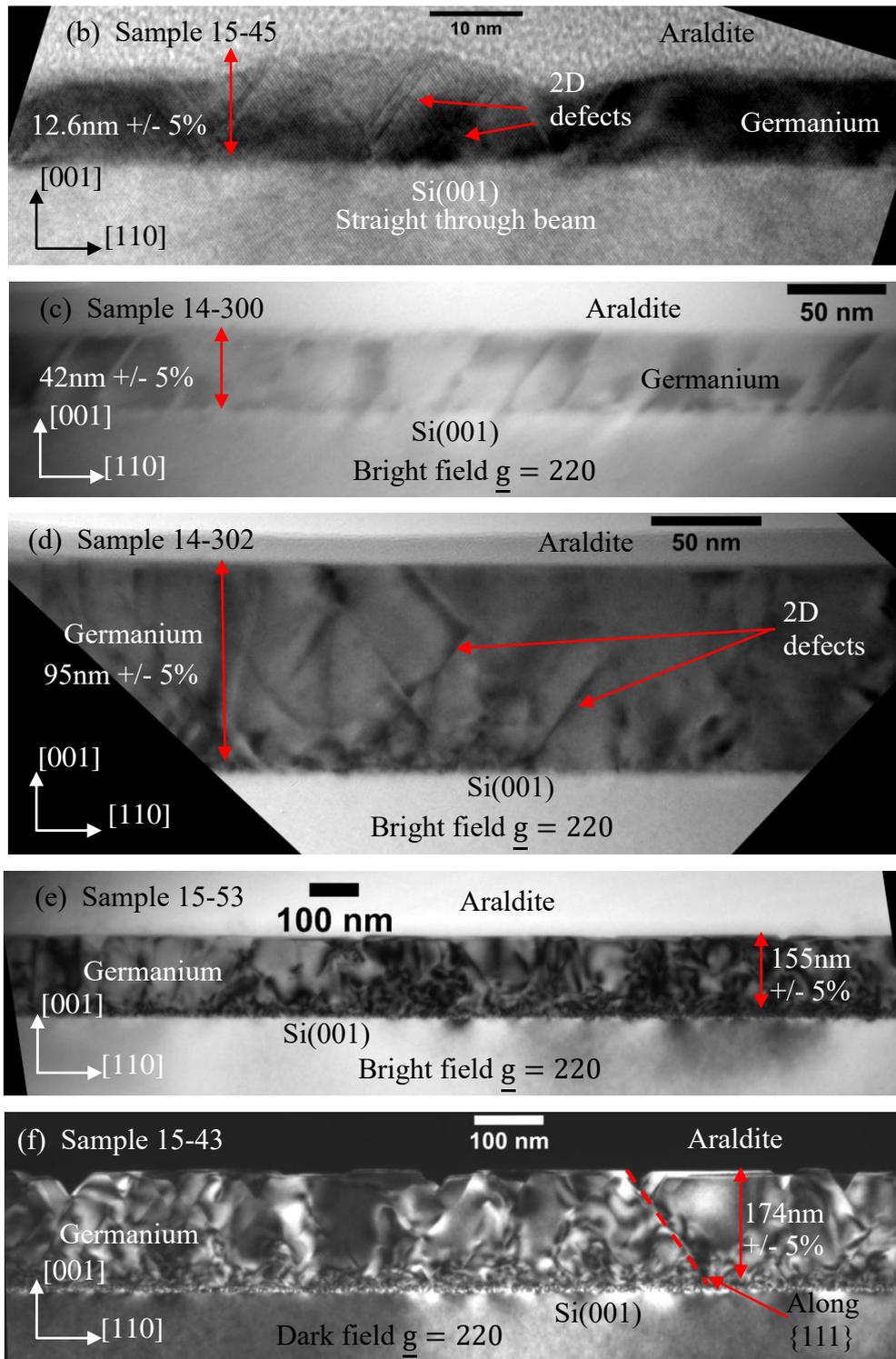


Figure 4.3: X-TEM of samples grown at 350°C. Samples: 15-46 (a), 15-45 (b), 14-300 (c), 14-302 (d), 15-53 (e) and 15-43 (f): Ge buffer layer grown at 350°C with increasing thickness from (a) to (f). The thickness measurements were ascertained from the 004 diffraction condition. Notice that the layer is relatively smooth and planar until approximately at 95nm thickness, after which faceting takes place.

For a buffer layer grown at 350°C up to 6.4nm thickness, the Frank Van der Merwe 3D islands appear to be not as distinct as when grown at 400°C (figure 4.3 (a)). This

suggests that the bulk strain energy per unit volume (σ_1) value from equations 2.32 and 2.33 in section 2.4.4 is not as large at this growth temperature and therefore the epilayer surface area (A_1) does not increase as much to compensate. As the layer thickness is increased to 12.6nm, the islands coalesce sooner and 2D growth proceeds until reaching a thickness of 95nm. X-TEM images show a greater number of 2D defects in the layer which arise from $\{111\}$ facets on the islands during the initial growth stages. It cannot be said with certainty whether these are stacking faults or micro twins without obtaining lattice resolved images. As the layer thickness increases and thus σ_1 increases, islanded growth takes place along these defects, where the $\{111\}$ planes are the island boundaries (figure 4.3(f)).

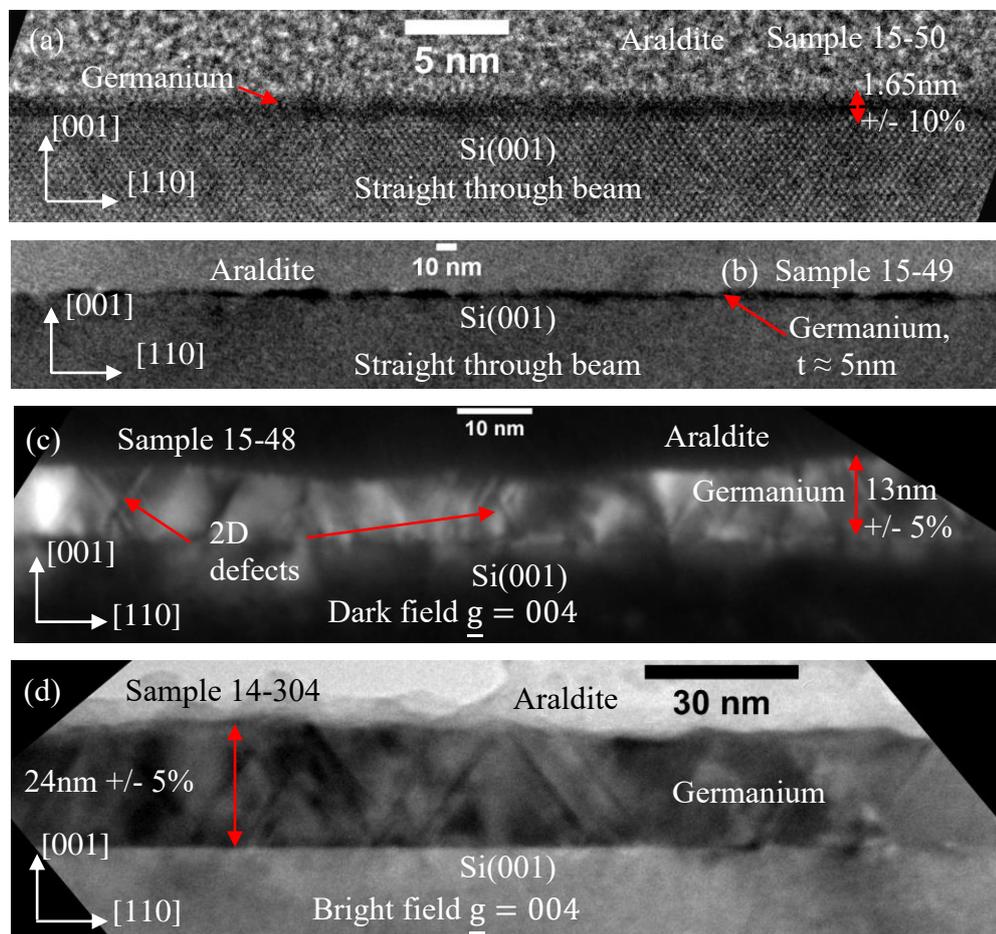


Figure 4.4: X-TEM of samples grown at 300°C. Samples: 15-50 (a), 15-49 (b), 15-48 (c) and 14-304 (d).

With the thinnest sample, 15-50 (figure 4.4 (a)), the error in the measurement is increased to +/- 10% as the nominal thickness is 2nm and it is assumed that several monolayers of the Ge surface have been oxidised. When the temperature is dropped to

300°C the bulk strain energy per unit volume is lower still than at 350°C, and so island formation is inhibited further. By comparing X-TEM images of samples of similar thicknesses grown at 400°C, 350°C and 300°C in figures 4.2 (b), 4.3(b) and 4.4(c) respectively, it appears that the 2D defect density is even greater at 300°C growth temperature.

When comparing the thickest grown 300°C layer ($\approx 78.9\text{nm}$) in this investigation with equivalent layers grown at 350°C ($\approx 75\text{nm}$) and 400°C ($\approx 72\text{nm}$) in figure 4.5, it is clearly seen that faceting is triggered at a much lower thickness when grown at 300°C.

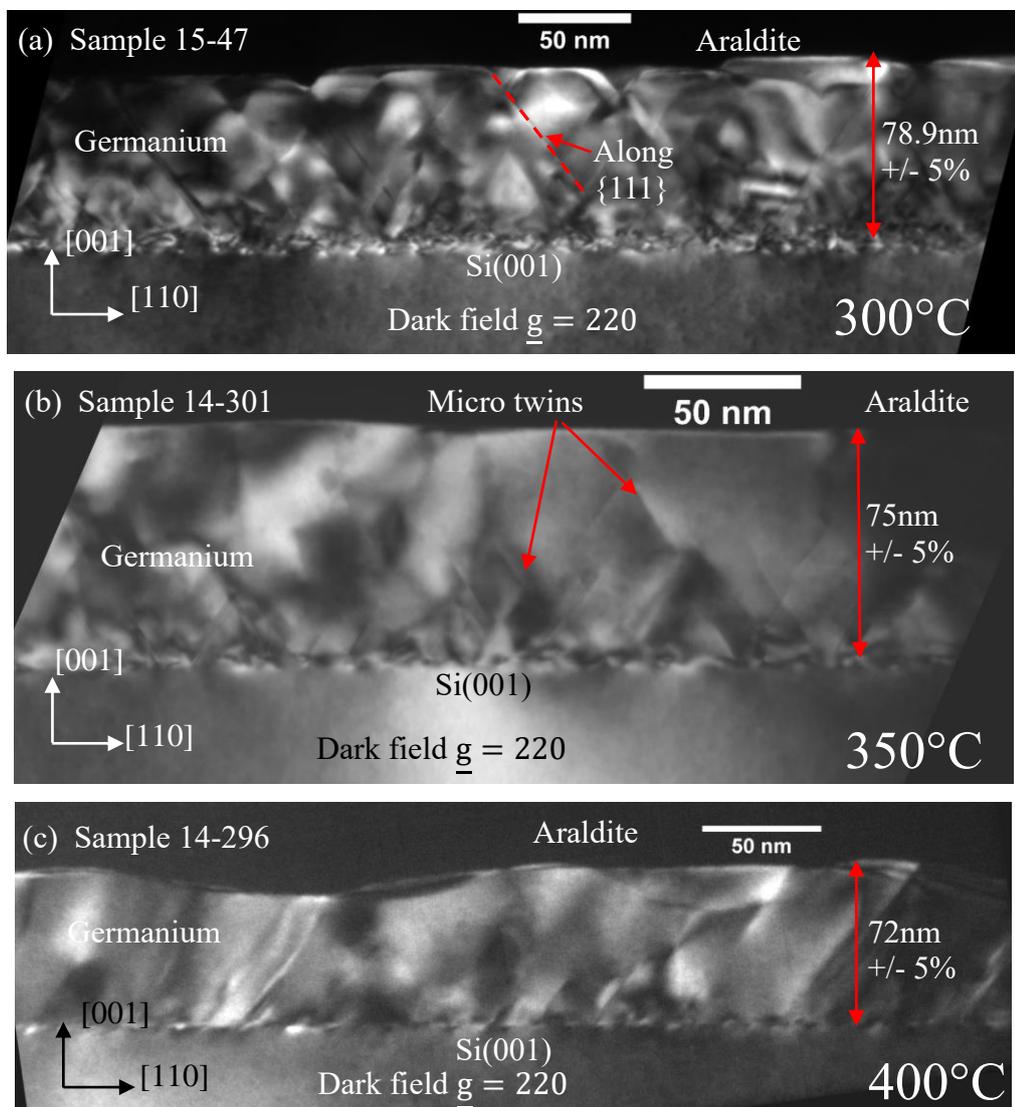


Figure 4.5: Comparison of Ge buffer layers grown at 300°C, 350°C and 400°C to roughly similar thicknesses. Figure (a) X-TEM of sample 15-47; Ge grown at 300°C to 78.9nm thickness. Figure (b) X-TEM of sample 14-301; Ge buffer layer grown at 350°C and figure (c) X-TEM of sample 14-296; Ge buffer layer grown at 400°C.

4.2.3.1. Growth rate and stagnation time

The stagnation time is defined as the time taken from the moment at which the precursor and carrier gases are introduced over the wafer until growth starts to occur. The stagnation time is obtained by plotting the growth times (on the x-axis) against layer thicknesses (on the y-axis) and determining the time at which the thickness is equal to zero. The stagnation time for samples grown at 400°C is 61 secs and for those grown at 350°C is 298 secs.

The growth rates were determined by differentiating these plots. The growth rate at 400°C is approximately 0.41nm/s \pm 0.004nm/s, at 350°C the growth rate is approximately 0.064nm/s \pm 0.001nm/s. This is expected because the temperature supplied during growth gives adatoms kinetic energy to find free sites during transport, and so the greater the temperature the more kinetic energy adatoms have to drift along the substrate surface until it encounters a vacancy.

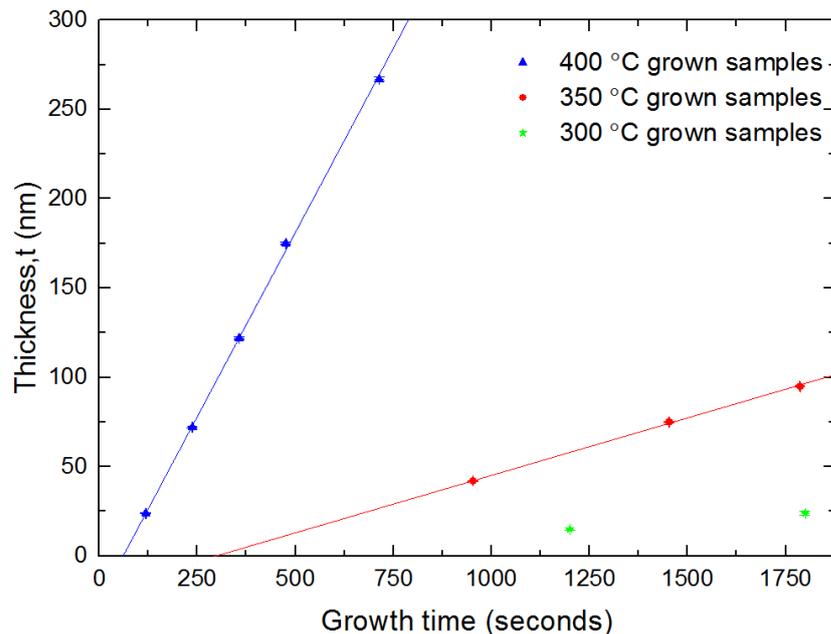


Figure 4.6: Growth time vs thickness plots for Ge grown at various temperatures. Due to insufficient samples and higher error in thickness measurements for samples grown at 300°C the stagnation time and growth rate could not accurately be calculated but given the location of the points, it would seem that the stagnation time is longer and the growth rate lower for 300°C grown Ge buffer layers.

4.2.4. Annealing effects on thin Ge buffer layers.

Sample number:	Growth temperature (°C)	Intended growth thickness prior to annealing (nm)	Anneal time (Minutes)	Ge buffer maximum measured thickness (nm) (+/- 0.5%)
15-56	300	20	1	66
15-57	300	20	5	70
15-58	400	20	1	65
15-59	400	20	5	67
15-60	400	100	1	78
15-61	400	100	5	78

Table 4.4: Annealing study on LT thin Ge buffer layers.

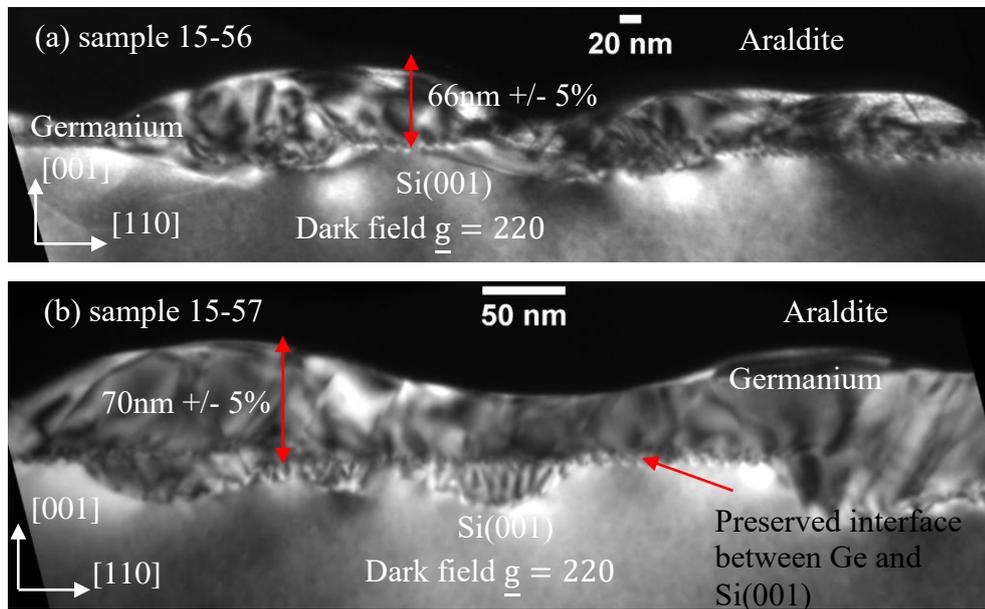


Figure 4.7: (a) 220 dark field X-TEM image of sample 15-56; 20nm Ge buffer layer grown at 300°C and then annealed at 650°C for 1 minute and (b) 220 dark field X-TEM image of sample 15-57; 20nm Ge buffer layer grown at 300°C and then annealed at 650°C for 5 minutes.

Figure 4.7 shows a 20nm thick Ge buffer layer that has been annealed at 650°C for 1 min: figure (a) and for 5 mins: figure (b). Annealing a layer as thin as 20nm for 1

minute has already destroyed uniformity and the maximum measured thickness from misfit interface to the peak of the epilayer is 66nm. When the layer is annealed for 5 mins in total the maximum height measured in three locations on the sample averaged 70nm +/- 2nm.

Figure 4.8 shows a similar effect occurring when the LT Ge epilayer is grown at 400°C to 20nm thickness and then annealed for at 650°C for 1 min and 5mins. The maximum measured thickness (from 3 locations of the epilayer) from misfit dislocation interface to the peak of the epilayer is 70nm for the sample annealed for 1min. The maximum thickness for the 20nm layer grown at 400°C and annealed for 5 mins is also 70nm +/- 5nm.

As can be seen in both figures 4.7 and 4.8 the act of annealing a 20nm Ge buffer layer regardless of growth temperature has the effect of destroying the interface between the substrate and the Ge buffer. Regions do still exist where misfit dislocations can be seen and the interface has been preserved. This disruption is presumed to be due to the differences in diffusion coefficients between silicon and germanium. The diffusion coefficient of solids follows an Arrhenius relationship [145]:

$$D = D_0 e^{-\left(\frac{E_A}{kT}\right)} \quad (\text{Equation 4.1})$$

Where: D_0 is the maximum diffusion coefficient at infinite temperature. It was determined empirically that at 650°C the diffusion of silicon into germanium has the following value; $6.9 \times 10^{-17} \text{ cm}^2/\text{s}$ [146] and germanium has into silicon at 650°C is $1.395 \times 10^{-24} \text{ cm}^2/\text{s}$ [145]. Therefore, presumably below a critical thickness of the Ge epilayer, subjecting the layer to a temperature of 650°C has caused silicon to diffuse into the germanium epilayer because it has a faster diffusion rate.

HR-XRD was not carried out for these layers since the thickness and layer non-uniformity was too low to be able to detect a coherent signal from either of the two annealed samples. And from the cross-sectional images it can be seen that the dislocation densities for both the 300°C grown + annealed samples and the 400°C

grown + annealed samples have a TDD $> 1 \times 10^{11} \text{ cm}^{-2}$. A study based on Fick's law has not been carried out in this project, however it is recommended as future work to further optimise the thin Ge buffer layer.

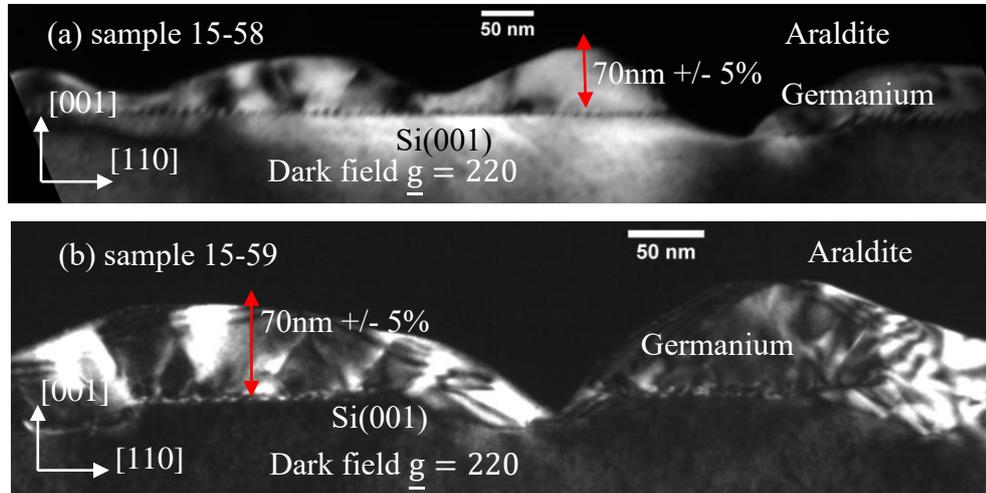


Figure 4.8: (a) 220 dark field X-TEM image of sample 15-58; 20nm Ge buffer layer grown at 400°C and then annealed at 650°C for 1 minute and (b) 220 dark field X-TEM image of sample 15-59; 20nm Ge buffer layer grown at 400°C and then annealed at 650°C for 5 minutes. Thickness were measured from the 004 diffraction condition.

When annealing a 78nm Ge buffer layer grown at 400nm for 1 min at 650°C, this has not destroyed layer uniformity as can be seen in figure 4.9 (a). If figure 4.9 (a) is compared to figure 4.5 (c) which is of a Ge buffer layer grown at 400°C but has not been annealed, a change in surface quality can be seen. Whilst undulations can be seen in figure 4.5 (c), the layer appears relatively smooth in figure 4.9 (a). Secondly by comparing the two figures, it is clearly seen that the Lomer dislocation network at the interface in the annealed sample has become re-ordered and uniformly spaced, with noticeable improvement in the crystalline quality and fewer threading dislocations. If the 78nm buffer layer is annealed for 5 mins, as seen in figure 4.9 (b) then uniformity is still maintained in the layer. This would suggest that annealing for 5 mins at 650°C is acceptable for 78nm thick layers. It maybe that some critical thickness lies in between 20nm and 78nm thickness at which the layer can be annealed without disrupting the uniformity in the layer. Annealing the 78nm layer for longer than 5 mins may disrupt the buffer uniformity however this cannot be said conclusively because the maximum annealing time for the wafer in this study was 5mins.

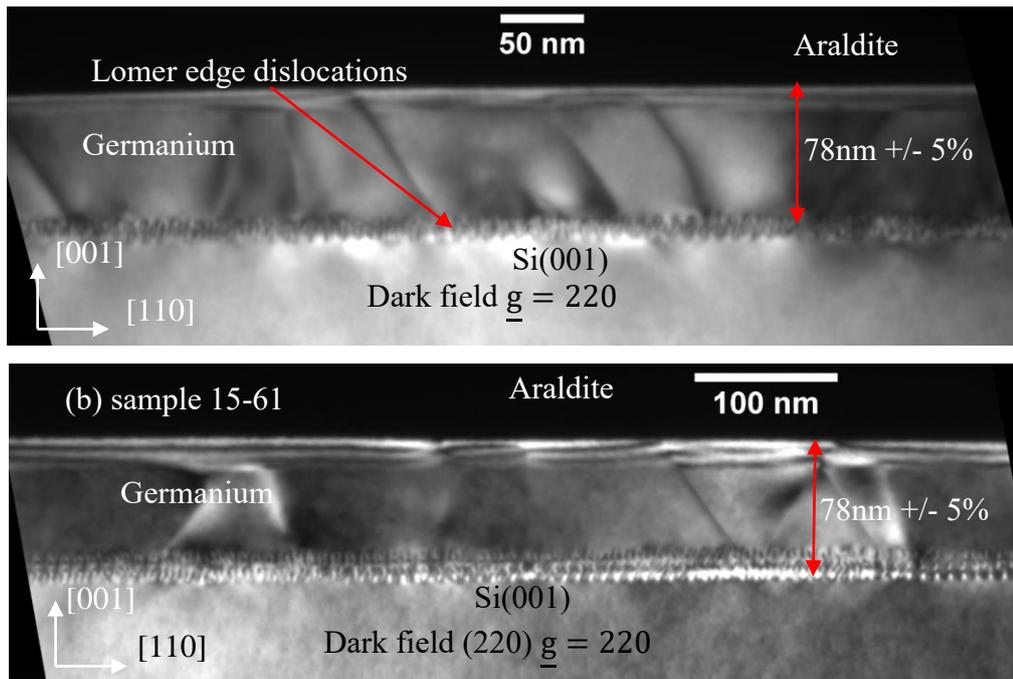


Figure 4.9: (a) 220 dark field X-TEM image of sample 15-60; 78nm Ge buffer layer grown at 400°C and then annealed at 650°C for 1 minute and (b) 220 dark field X-TEM image of sample 15-61; 78nm Ge buffer layer grown at 400°C and then annealed at 650°C for 5 minutes. Thicknesses were measured from the 004 diffraction condition.

4.2.5. Surface roughness of LT-Ge buffer layers

4.2.5.1. Surface roughness variation as a function of growth temperature: 300°C, 350°C, 400°C.

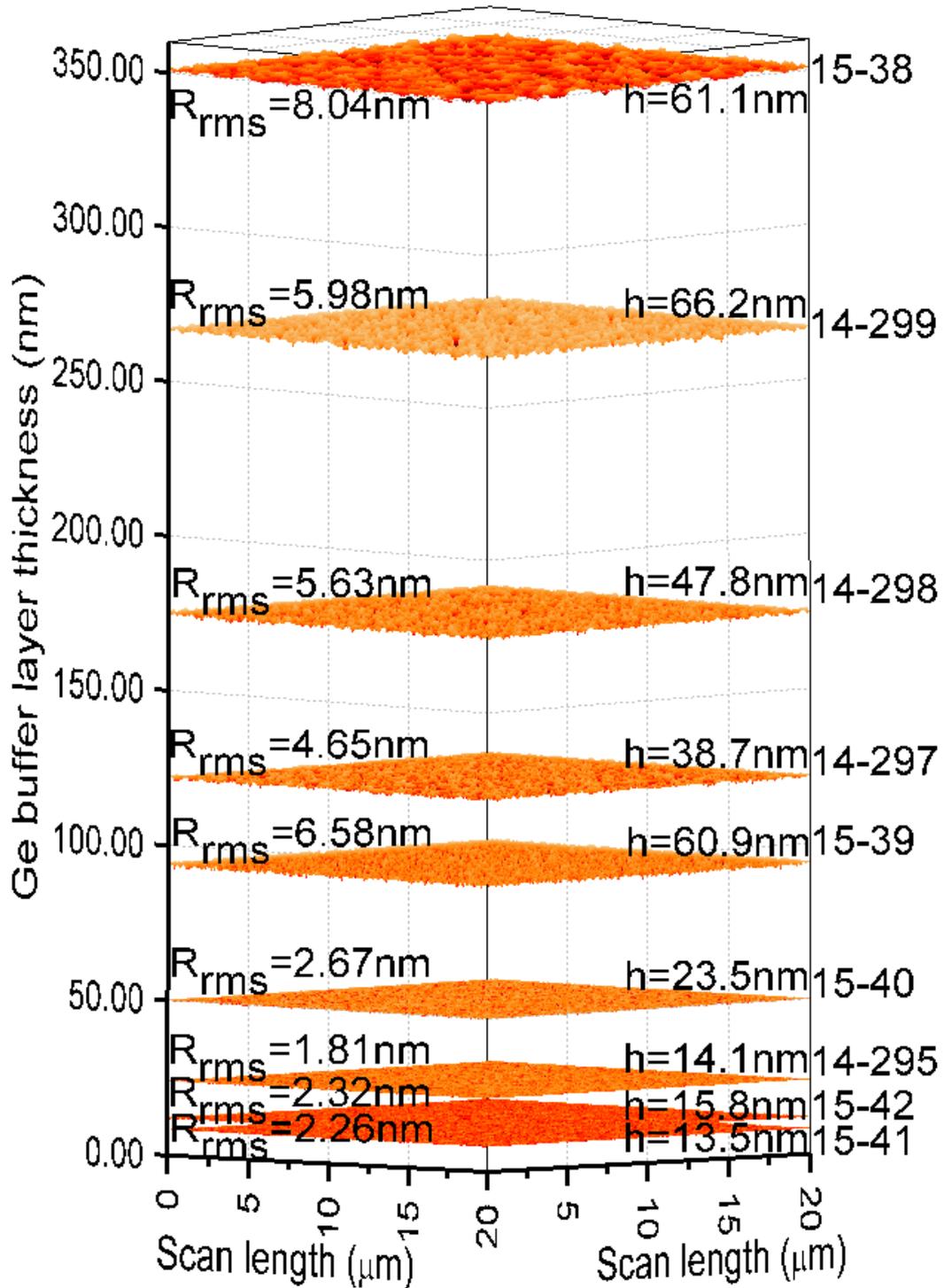


Figure 4.10: 3D 20μm x 20μm AFM micrographs of Ge buffer layers grown at 400°C, plotted in increasing thickness. The sample numbers are labelled to the right of each micrograph. The rms roughness (R_{rms}) and maximum to minimum heights (h) are listed as well.

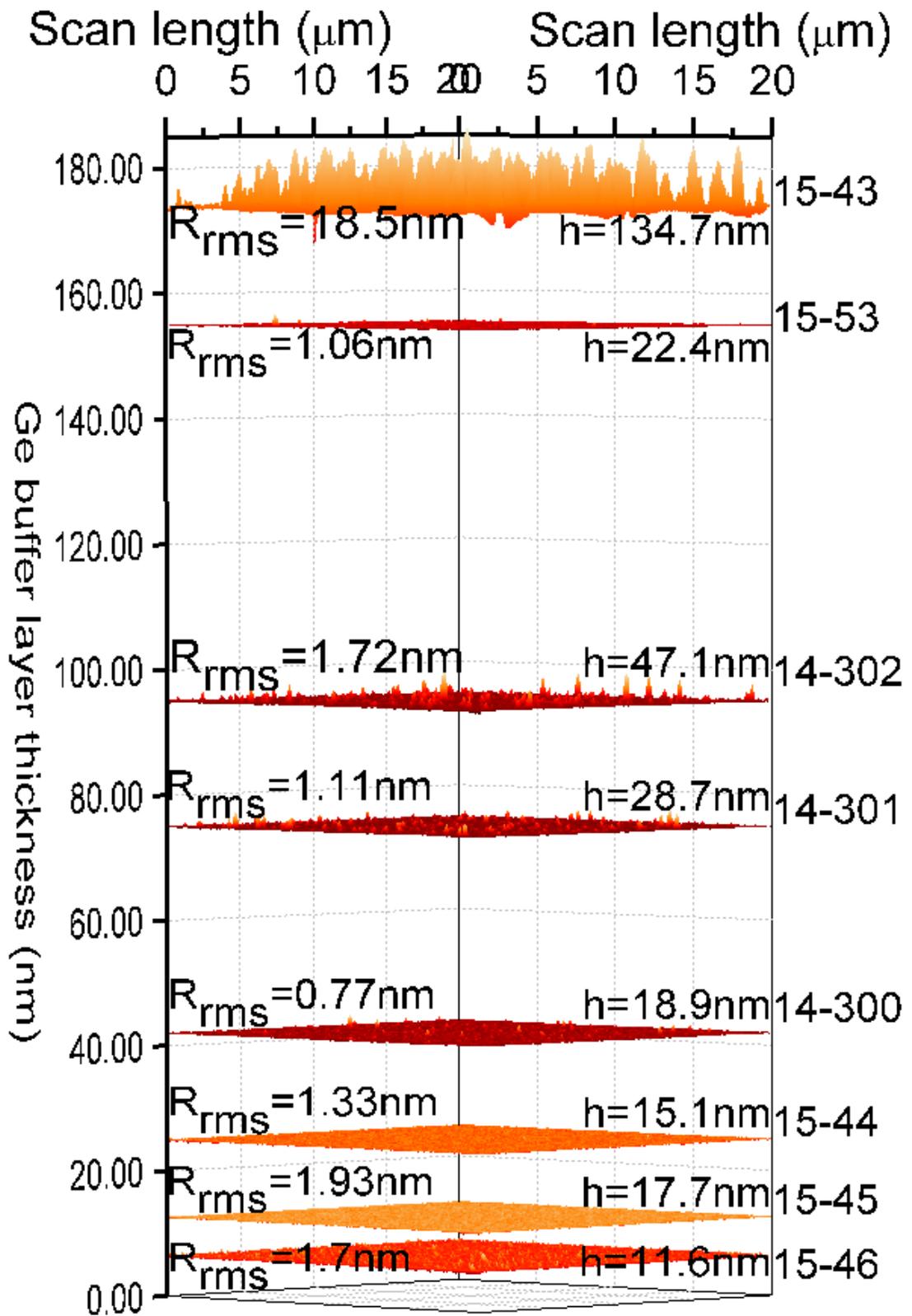


Figure 4.11: 3D 20 μ m x 20 μ m AFM micrographs of Ge buffer layers grown at 350°C, plotted in increasing thickness. The sample numbers are labelled to the right of each micrograph. The rms roughness (R_{rms}) and maximum to minimum heights (h) are listed as well.

From figure 4.2 it is seen that when a 400°C Ge buffer layer is grown to 351nm thickness, the surface becomes very rough due to continuing compressive strain relaxation. Figure 4.10 shows that at this thickness the R_{rms} is 8.04 nm. It was previously speculated that roughness would reach a maximum at 150nm thickness in Ge grown at 400°C, explained as a maximisation of surface feature density by Shah et al [140]. The plots in Chapter 4.2.5.3 will describe why this may not be the case.

The micrographs in figure 4.11 show that faceting features are subdued under a buffer layer thickness of approximately 42nm. The diagram also shows that as the layer is grown thicker, the facet islands grow stronger in density and height. This suggests that as soon as a deviation in planar growth occurs along {111} planes then growth will continue in this manner until possibly reaching an apex of some sort. Sample 15-53 is possibly a measurement error because based on predictions, faceting should be much stronger for the layer grown to 155nm. At 174nm thickness, AFM measurements show that facets have heights of 134.7nm on average.

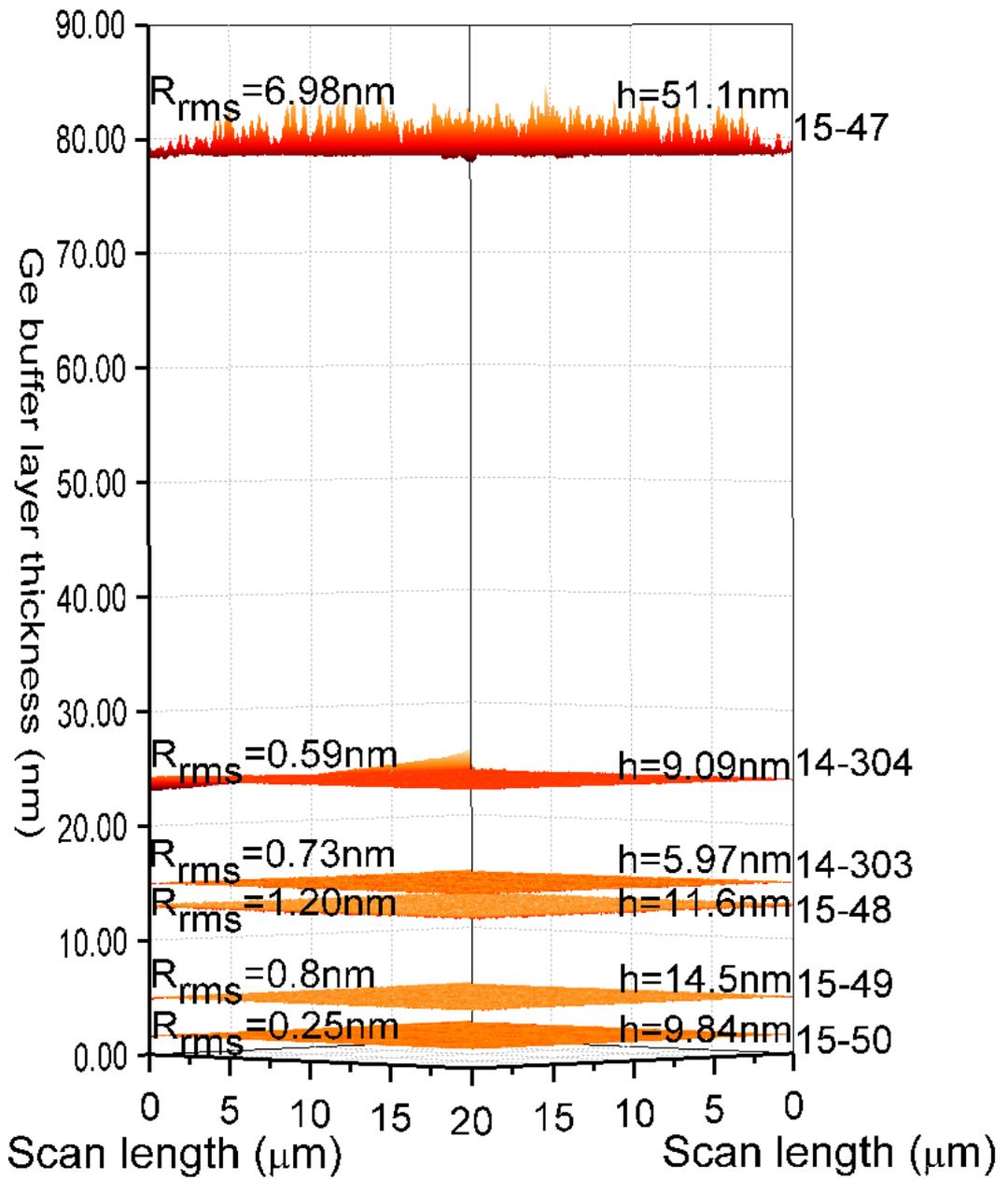


Figure 4.12: 3D 20 μm x 20 μm AFM micrographs of Ge buffer layers grown at 300 $^{\circ}\text{C}$ as shown in table 4.3. The sample numbers are labelled to the right of each micrograph and are listed in order of thickness on the z-axis. The rms roughness (R_{rms}) and maximum to minimum heights (h) are listed as well.

4.2.5.2. Annealing effects on LT-Ge buffer layer surface morphology

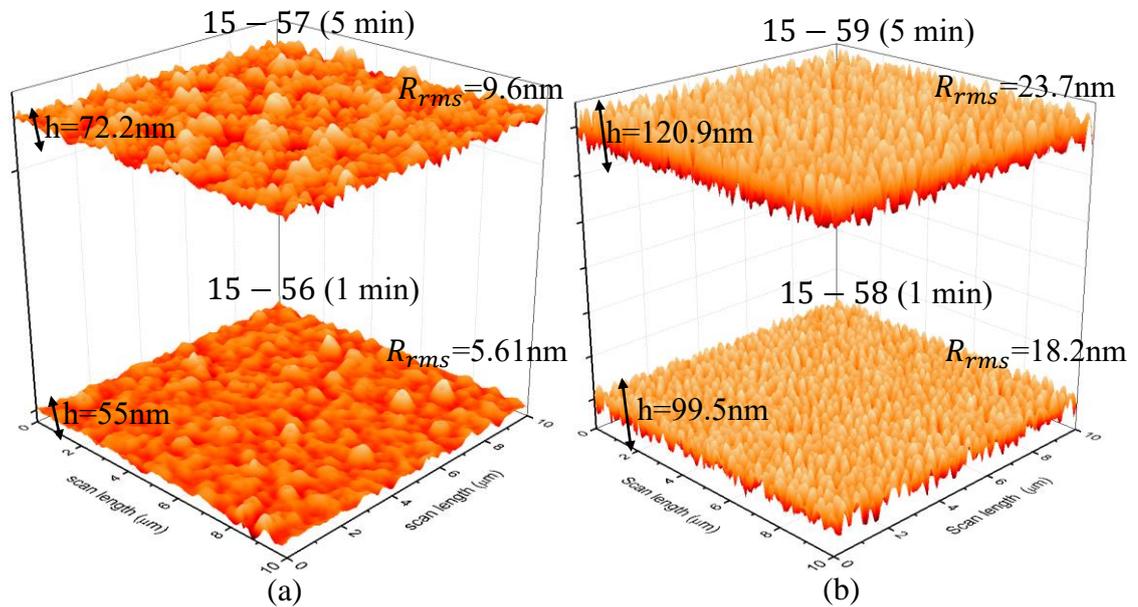


Figure 4.13: Contact mode AFM micrographs of Ge buffer layers grown to 20nm thickness and annealed at 650° as per table 4.4. Figure (a) is of Ge layers grown at 300°C, (b) is of Ge layers grown at 400°C.

For the annealed samples in section 4.2.4, it has been seen from X-TEM images that 650°C annealing of a 20nm thick Ge buffer layer causes disruption to layer uniformity regardless of the growth temperature. Contact mode AFM shows that the severity in layer disruption is least for 20nm Ge layer grown at 300°C and annealed for 1 minute (sample 15-56 at 5.61nm roughness) and the most amount of disruption to a 20nm layer that is grown at 400°C and annealed for 5 mins (sample 15-59 at 23.7nm roughness). It is speculated that higher growth temperatures increase the heat energy supplied per unit time (thermal budget) to allow silicon atoms to have enough kinetic energy to diffuse through from the substrate into the epilayer. Increasing the annealing time has the effect of increasing sample roughness and promoting faster diffusion between substrate and epilayer.

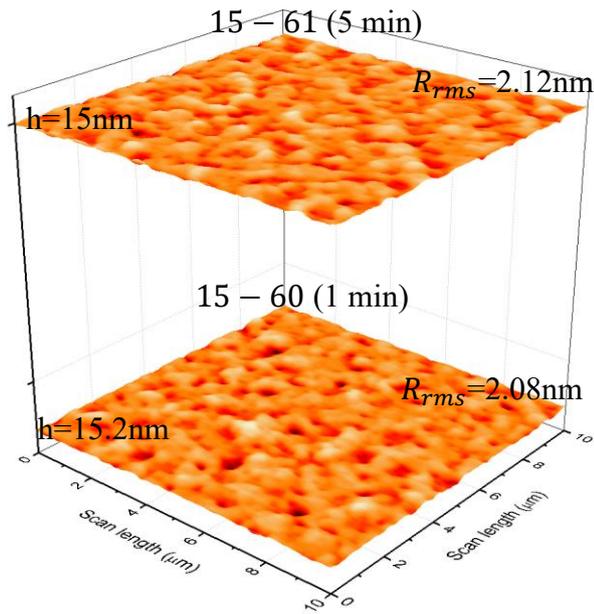


Figure 4.14: Contact mode AFM micrographs of Ge buffer layers grown to 78nm thickness and annealed at 650° for 1min and 5 mins. Annealing a 400°C 78nm layer for 4 more mins doesn't affect the roughness.

With 78nm thick buffer layers the roughness obtained using contact mode AFM shows that annealing at 650°C for 1 min and 5 mins gives a value of approximately 2.1nm +/- 0.02nm. This means that no significant change in surface morphology occurs when annealing for an extra 4 mins. However, when considering a similar Ge buffer layer grown at 400°C and is un-annealed; sample 14-296 ($R_{rms} = 3.83\text{nm} \pm 0.02\text{nm}$) which was grown to 72nm thickness, there is a significant difference in surface morphology which lies outside of the error margins. This means that 650°C annealing categorically improves surface quality for 78nm Ge layers as shown in figure 4.14.

4.2.5.3. LT-Ge Surface morphology summary plots

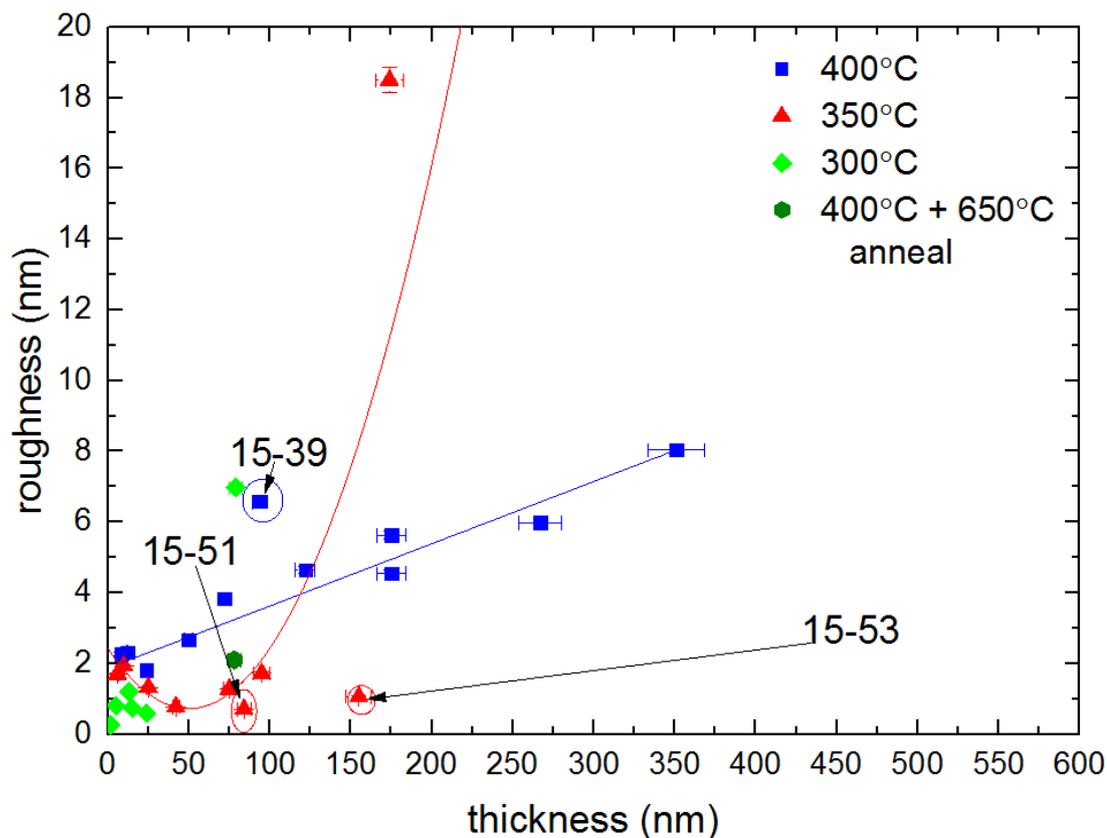


Figure 4.15: Roughness (rms) vs thickness plot for the Ge buffer layers grown at various temperatures.

In figures 4.15 and 4.16 a linear trend between thickness vs roughness and thickness vs height, is seen respectively for layers grown at 400°C, with all vacancy sites being used during growth. It is therefore hypothesised from the findings of this investigation that if the layer was to be grown thicker still at this temperature, then it would become rougher with greater amplitude in surface undulations based on the linear line of best fit (blue) drawn against the data points in figures 4.15 and 4.16.

As mentioned earlier, it appears that faceting takes place sooner for layers grown at 300°C as seen in figure 4.12. AFM measurements indicate faceting occurs at 24nm thickness as shown in figures 4.15 and 4.16. This is corroborated by the height difference in features being 51.1nm in a 78.9nm thick layer. The roughness of the layer is only significantly affected once the layer thickness has reached a point in between 24nm and 78.9nm as shown in figure 4.15. For a 1.65nm Ge buffer layer planar growth

seems to occur as the roughness is 0.25nm which is within the roughness error of the substrate.

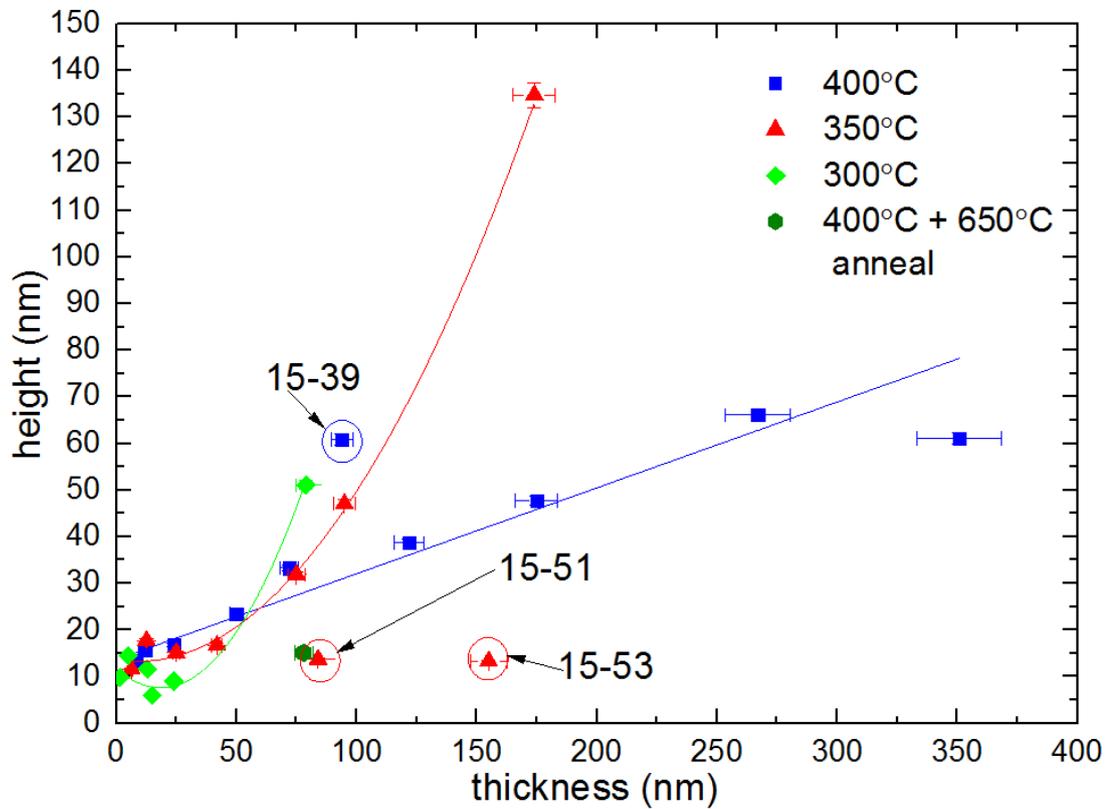


Figure 4.16: AFM scan height difference vs thickness plot for the Ge buffer layers grown at various temperatures.

Smooth surface buffer layers can be grown at 350° to 95nm, despite the facets as made evident in figure 4.16 however, the stagnation time and growth rate are hindered. This means that there is a trade-off between smooth surfaces for further epitaxy or faster throughput for epiwafers if thinking as an industrial process.

4.2.6. Temperature dependent strain variation in the buffer layers.

Due to the limitations of the triple axis detector, epitaxial layers with a thickness less than 78nm could not be detected in a 004 symmetrical scan, regardless of the amount of strain.

The in-plane strain in the Ge epilayer due to thermal expansion coefficient mismatch ($\epsilon_{\parallel-\text{Ge}T_H}$) is calculated by treating the substrate/epilayer as a bending moment problem, where the shear force of the substrate on the epilayer and vice versa multiplied by the respective thicknesses (t_{Ge} and t_{Si}) equals the bending moments [147]. An assumption is taken that all compressive strain due to the 4.2% lattice mismatch has been relieved. The higher thermal expansion coefficient of Ge means that when the wafer is cooled down to room temperature ($T_L \approx 26.85^\circ\text{C}$) from being subjected to a higher temperature (T_H), the Ge epilayer shrinks even more than the Si(001) substrate. Given that the Ge is covalently bonded to the Si(001), this results in the entire wafer ‘bowing’ upwards. The radius of curvature of the bowed wafer, r , is given by equation 4.2, where the (001) Young’s modulus of Si and Ge are given as Y_{Si} and Y_{Ge} respectively. The $\epsilon_{\parallel-\text{Ge}T_H}$ is then calculated from equation 4.3 for the wafer at various values of T_H as seen in figure 4.17. The figure shows that the standard deviation in strain values is 0.000071% from the thinnest (78nm) to the thickest epilayer (351nm).

$$\left(\frac{1}{r}\right) = \frac{6Y_{\text{Ge}}Y_{\text{Si}}t_{\text{Ge}}t_{\text{Si}}(t_{\text{Ge}}+t_{\text{Si}}) \int_{T_H}^{T_L} [\alpha_{\text{Si}}(T) - \alpha_{\text{Ge}}(T)] dT}{3Y_{\text{Ge}}Y_{\text{Si}}t_{\text{Ge}}t_{\text{Si}}(t_{\text{Ge}}+t_{\text{Si}})^2 + (Y_{\text{Ge}}t_{\text{Ge}} + Y_{\text{Si}}t_{\text{Si}})(Y_{\text{Ge}}t_{\text{Ge}}^3 + Y_{\text{Si}}t_{\text{Si}}^3)} \quad (\text{Equation 4.2})$$

$$\epsilon_{\parallel-\text{Ge}T_H} = \left(\frac{1}{r}\right) \frac{Y_{\text{Ge}}t_{\text{Ge}}^3 + Y_{\text{Si}}t_{\text{Si}}^3}{6Y_{\text{Ge}}t_{\text{Ge}}(t_{\text{Ge}}+t_{\text{Si}})} \quad (\text{Equation 4.3})$$

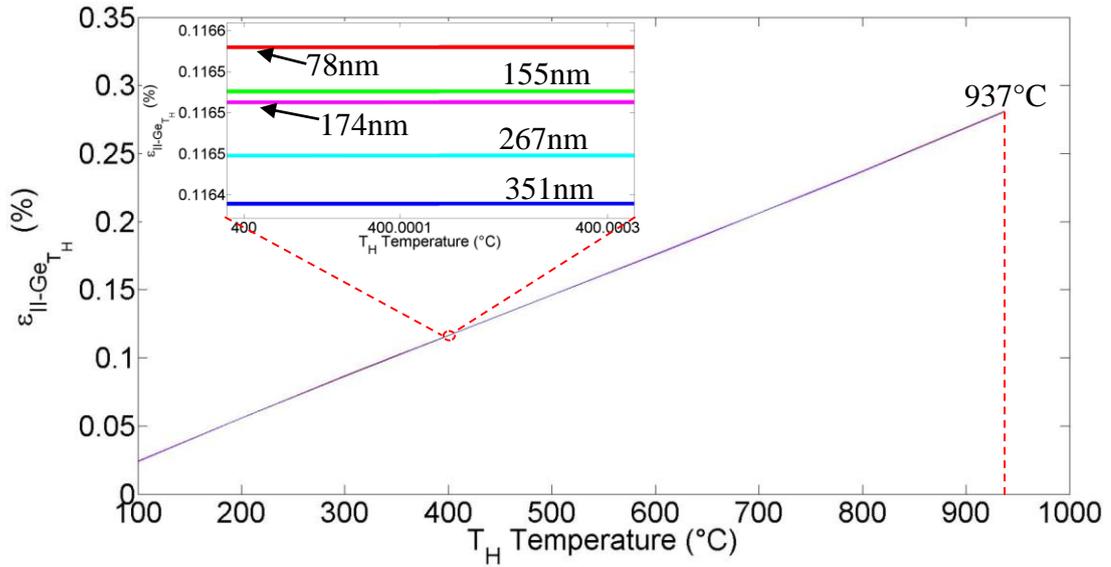


Figure 4.17: Starting temperature T_H vs thermal expansion coefficient mismatch strain between Ge epilayer and $525\mu\text{m}$ Si(001) substrate ($\epsilon_{||-Ge_{T_H}}$) when cooled down to 26.85°C for various thickness of Ge film (t_{Ge}) listed in different colours. Inset, magnified section of the plot lines.

The complicated nature of strain relaxation makes it very difficult to determine the exact thermal energy needed to produce Ge layers with zero strain. According to figure 4.17, Ge layers grown below 400°C should be under tensile strain of less than 0.12%. However, HR-XRD RSMs of the thickest LT-Ge layers were carried out and showed that layers grown at 300°C , 350°C and 400°C are under relaxed with respect to the substrate i.e.: have some residual compressive strain as indicated in figures 4.18 (b), 4.19 (b) and 4.20 (b) respectively with the Ge peak lying on the right hand side of the relaxation line in the 224 scans. This means that below 351nm film thickness and below 400°C growth temperature, strain relaxation due to lattice mismatch through the formation of misfit dislocations has not been completed. From figure 4.18 it seems that for a 78.9 nm thick/ 300°C growth temperature Ge layer, the compressive strain is at its highest at -0.45% which is evident from the 224 scan however the difficulty in finding the peak in the 004 scan of this sample means that there is greater degree of error on this measurement as shown in figure 4.22.

For a Ge layer grown at 350°C to 174nm thickness the compressive strain reduces to 0.18% +/-0.03% and for a 400°C layer grown to 351nm thickness, the compressive strain reduces still to 0.11% +/- 0.01%. Figure 4.22 shows that a possible strain asymptote is reached with the thickest 400°C grown Ge sample. A possible

explanation to this is that at this amount of thermal budget, 60° misfit dislocations are kinetically limited to glide which leads to incomplete strain relaxation. Insufficient radial stresses mean that Lomer dislocations are also blocked from gliding along the (001) plane.

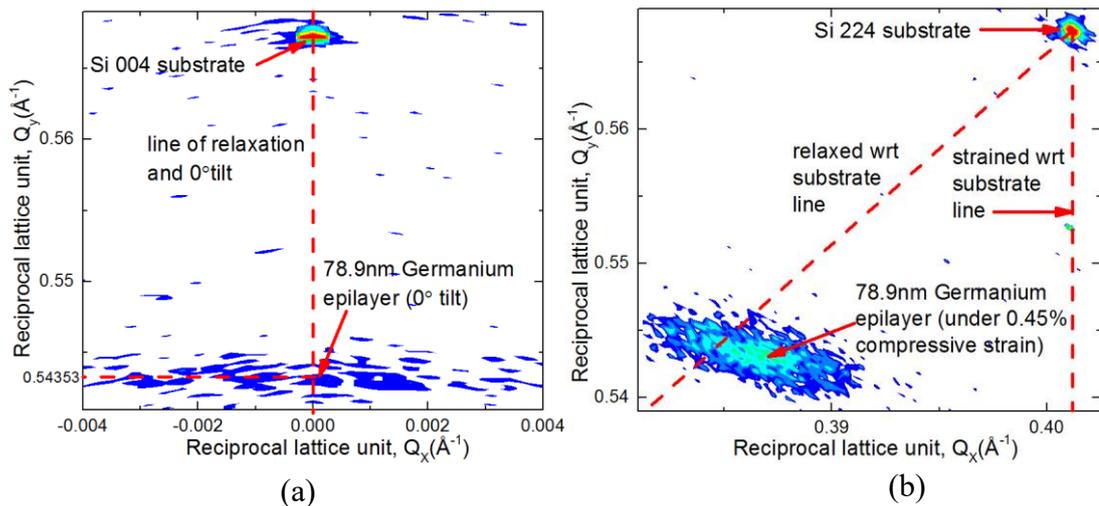


Figure 4.18: HR-XRD 004 (a) and 224 (b) RSM of sample 15-47: Ge buffer layer grown to 78.9nm thickness at 300°C .

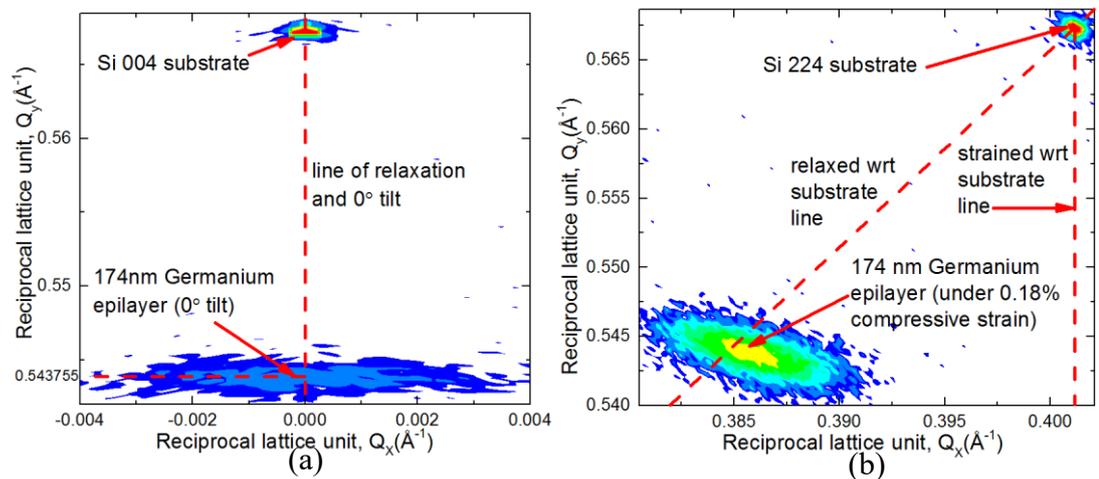


Figure 4.19: HR-XRD 004 (a) and 224 (b) RSM of sample 15-43: Ge buffer layer grown to 174nm thickness at 350°C .

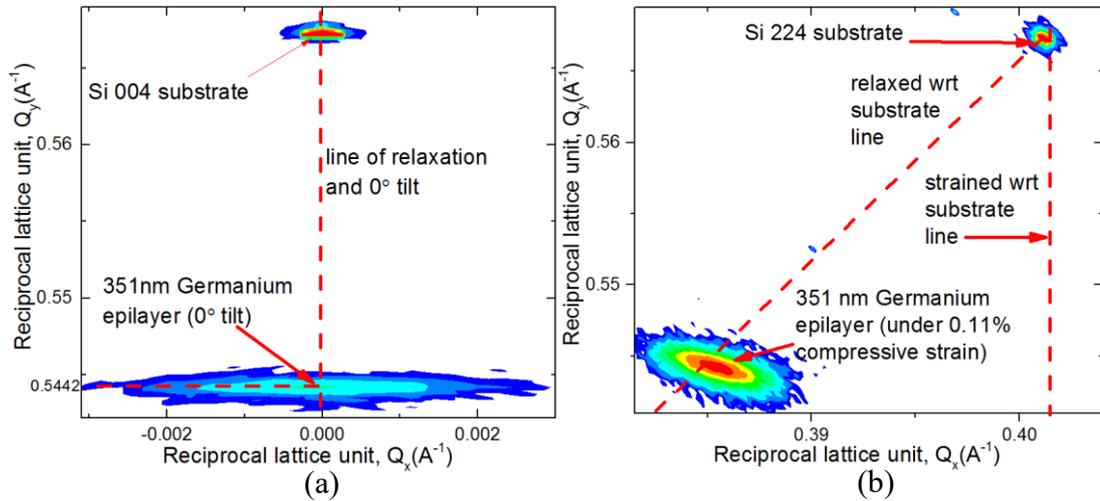


Figure 4.20: HR-XRD 004 (a) and 224 (b) RSM of sample 15-38: Ge buffer layer grown to 351nm thickness at 400°C.

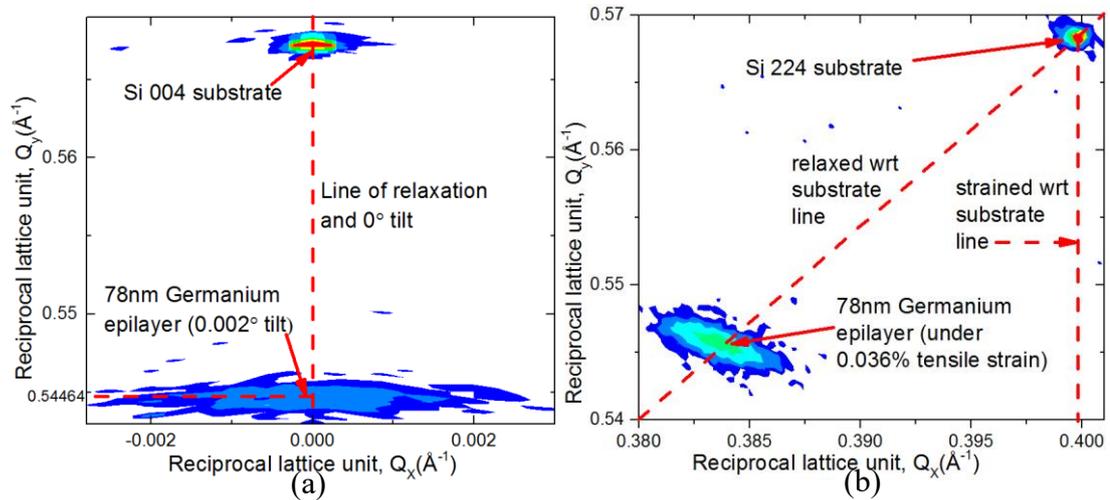


Figure 4.21: HR-XRD 004 (a) and 224 (b) RSM of sample 15-61 grown at 400°C and annealed at 650°C for 5mins.

When the 78nm thick/ 400°C growth temperature layer is subjected to annealing under hydrogen for 1 min at 650°C the strain in the layer has reduced to $\approx -0.037\%$, as shown in figure 4.22. When the same layer is annealed for additional 4 mins (5mins in total) at 650°C, the strain in the layer has now transitioned to become marginally tensile $\approx 0.036\%$ as seen in figure 4.21, where the Ge peak is lying on the left hand side of the substrate relaxation line. This means that growing Ge at 400°C and subsequently annealing at 650°C for 5 mins has supplied sufficient thermal budget to shrink the Ge epilayer upon cooling to room temperature to overcome the residual compressive strain due to lattice mismatch. From figure 4.22, it is hypothesised that annealing a

400°C grown layer at 78nm thickness for 3 mins should provide sufficient thermal budget to cause the Ge layer to become completely strain neutralised.

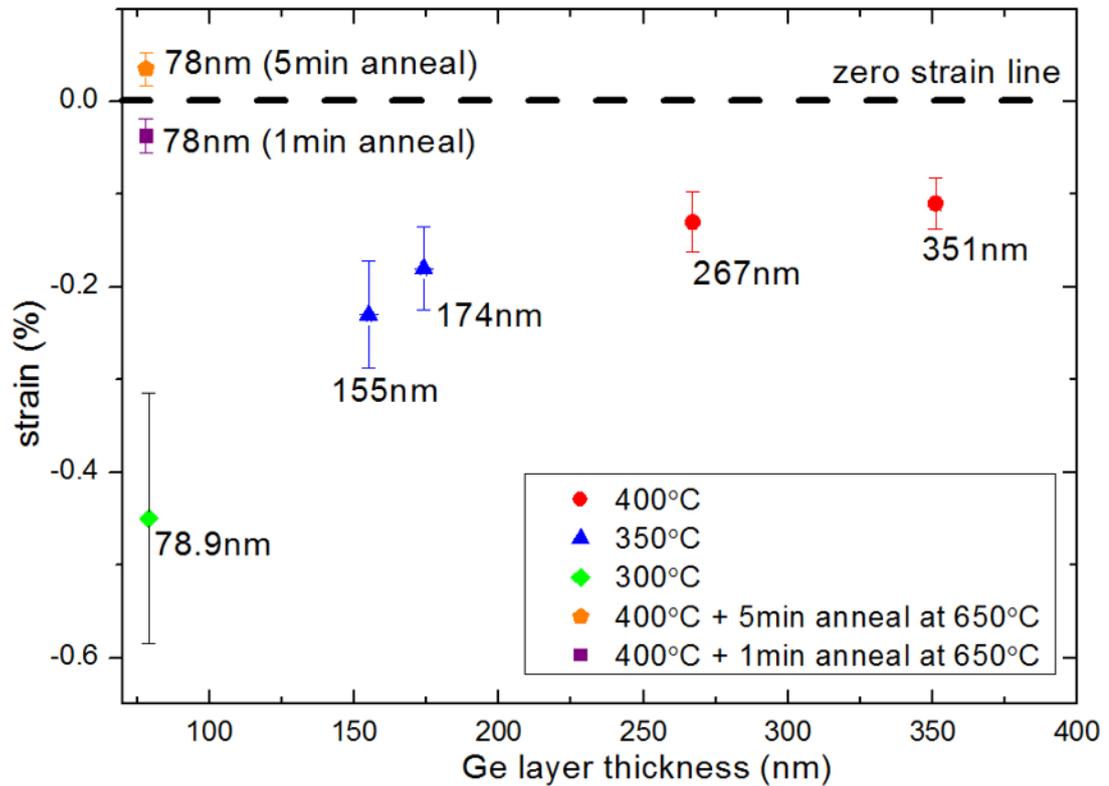


Figure 4.22: Strain in the LT Ge buffer layer measured using HR-XRD, grown at various temperatures and plotted against thickness. The error in the TEM thickness measurements is +/-0.5%.

4.2.7. Defect analysis

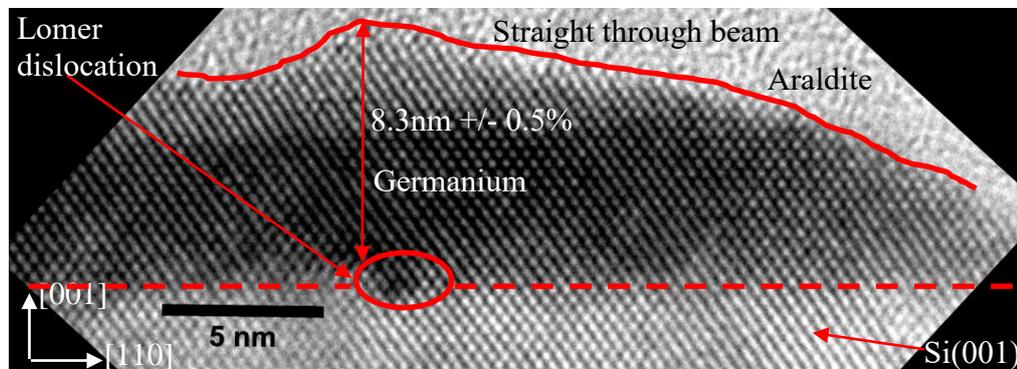


Figure 4.23: HR-XTEM of sample 15-42; Ge buffer layer grown at 400°C. The average measured thickness of the islands 8.3nm.

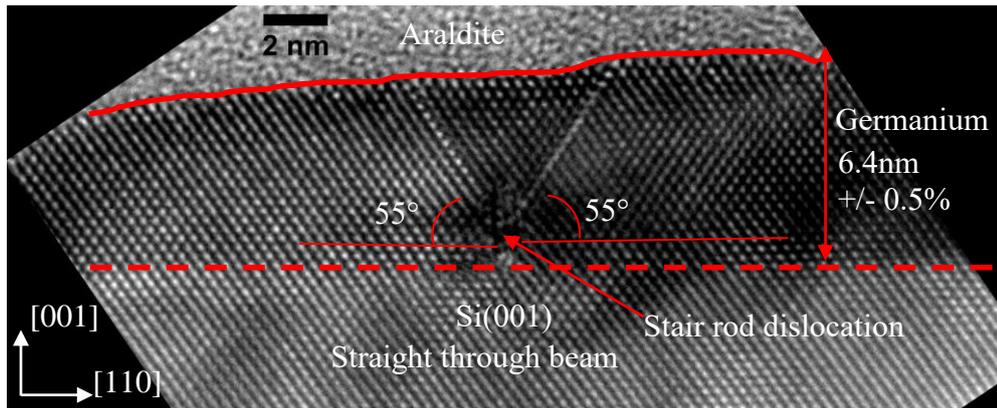


Figure 4.24: HR-XTEM of sample 15-46. Stacking faults propagating from a single stair-rod dislocation, can be seen. The measured angle from either stacked section of the layer is 55° along $[110]$ direction.

Figure 4.23 is a lattice resolved image taken of a single Ge island grown at 400°C to 8.3nm thickness. A Lomer dislocation is seen at the interface between the substrate and epilayer. 2D defects are predominantly seen for the Ge buffer layers grown at 350°C and 300°C . Figure 4.24 is a lattice resolved image of 6.4 nm Ge buffer layer showing opposing stacking faults that emanate from a stair rod dislocation. Stair rod dislocations can occur in islands where the shear stress is particularly high at the edges. Figure 4.26 is a plan view TEM image taken at the edge of a milled hole of a 350°C layer grown to 42nm thickness. 2D defects are seen, possibly emanating from stair rod dislocations and the measured angle is 125° on the (001) plane. If these are caused by stair rod dislocations, then the correct angle is 135° however since the sample is bent around the edges of the milled hole there is possibly a 10° discrepancy. When the layer is grown thicker, to 174nm thickness as seen in figure 4.27, plan view images show that the 2D defects have vanished which is expected because the facet islands form with the $\{111\}$ planes as boundaries.

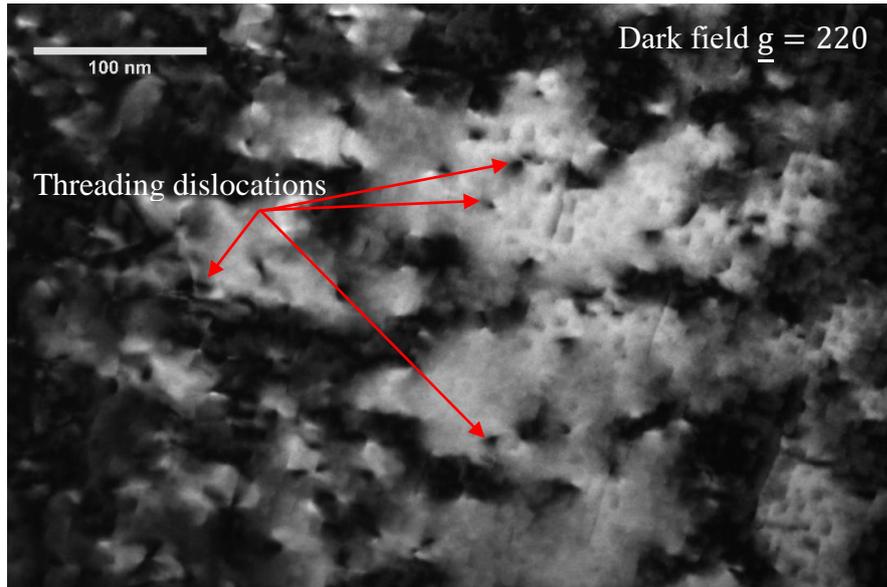


Figure 4.25: Plan view TEM of sample 15-47 (300°C growth 78.9nm thickness) showing threading dislocations. TDD for this image is $1.05 \times 10^{11} \text{ cm}^{-2}$. Average TDD for this sample is $9.86 \times 10^{10} \text{ cm}^{-2}$.

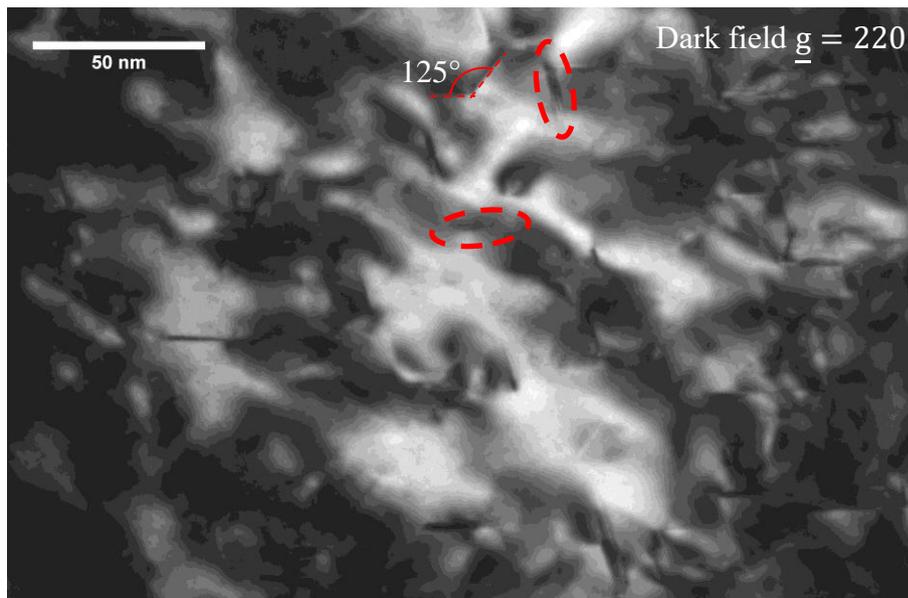


Figure 4.26: Plan view TEM of sample 14-300 (350°C growth, 42nm thickness) showing 2D defects as indicated by the red dashed circles, possibly emanating from the stair rod dislocations. The angle measured between 2D defects is 125°.

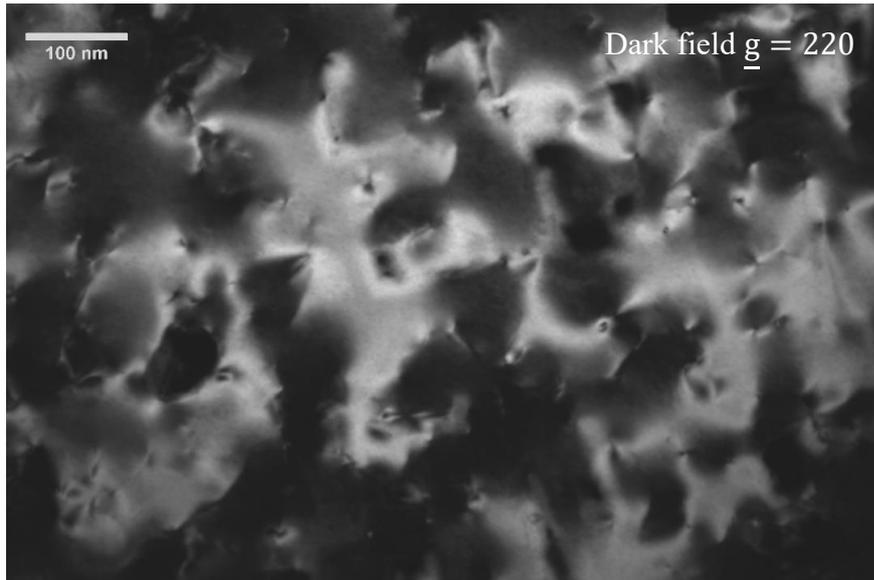


Figure 4.27: Plan view TEM of sample 15-43 (350°C growth 174nm thickness). TDD for this image is $2.32 \times 10^{10} \text{ cm}^{-2}$. Average TDD for this sample is $2.30 \times 10^{10} \text{ cm}^{-2}$

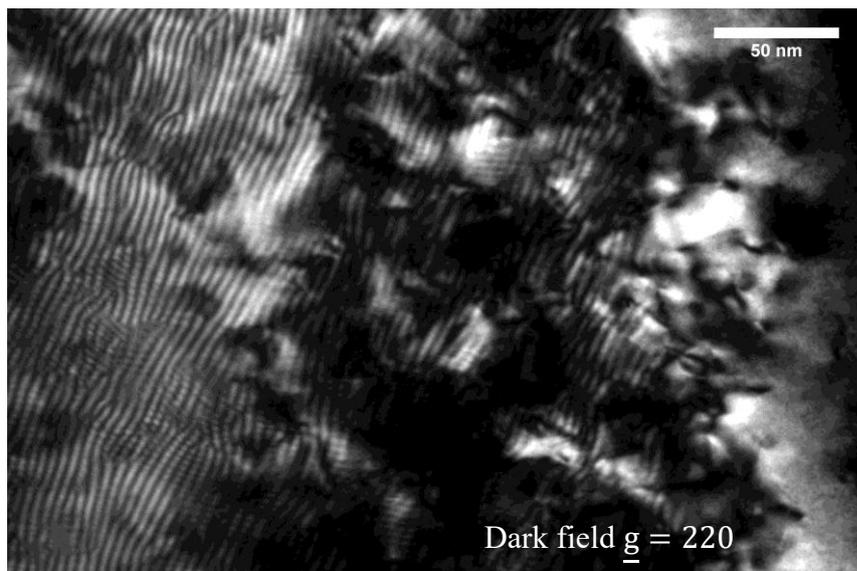


Figure 4.28: Plan view TEM of sample 14-302 (350°C growth and 95nm thickness) showing Moiré fringes on the left and side of the image caused by the interference between the substrate diffraction vector and the thin partially relaxed epilayer diffraction vector. Average TDD for this sample is $6.15 \times 10^{10} \text{ cm}^{-2}$.

The amount of thin area available for imaging becomes drastically reduced for thin samples and where Moiré fringes occur. This effect occurs when there is a change in diffraction vector $|\underline{\Delta g}|$ between the partially relaxed epilayer and substrate and is more pronounced in particularly thin layers. The thinnest sample imaged in this investigation was sample 14-300 (350°C growth and 42nm thickness). Their presence makes it

difficult to clearly see the threading dislocations. Only the thickest (78.9 nm) 300°C grown sample was imaged as shown in figure 4.25.

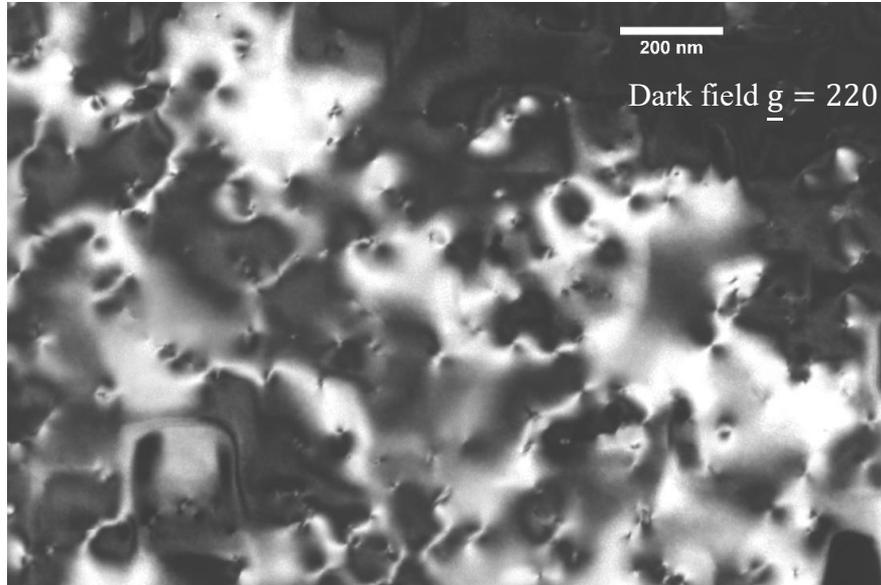


Figure 4.29: Plan view TEM of sample 15-38 (400°C growth, 351nm thickness). TDD for this image is $9.13 \times 10^9 \text{ cm}^{-2}$. Average TDD for this sample is $8.61 \times 10^9 \text{ cm}^{-2}$.

Different materials have been known to have different relationships between thickness and TDD [107]. From figure 4.31 it is seen that as the layer thickness, h , increases for all growth temperatures, the TDD value decreases. Several power law functions were used to fit the thickness vs TDD data, however the function that gave the closest to a linear fit when taking \log_{10} on both axes (figure 4.32) was the following relationship:

$$\text{TDD} = \frac{530}{h} - 0.5$$

This relationship can be explained by the annihilation mechanism of $> 10^8 \text{ cm}^{-2}$ TDD, where closed loop meeting of anti-parallel Burgers vector is preferred with misfit-misfit dislocation interaction creating a kinetic limit. So far, annealing of 78nm thick 400°C layers at 650°C has shown the creation of uniform buffer layers, with a more ordered Lomer network at the substrate interface, as well as 2.1nm roughness and a transition to 0.036% tensile strain as opposed to 0.2% compressive strain. 1min annealing reduces the threading dislocation density by approximately x 6 of an

equivalent un-annealed sample. Annealing for a further 4 mins (5 mins total) at 650°C reduces the TDD but only by a further x1.1 (figure 4.30). This can be explained by the increased glide velocities made available through annealing for 60° misfits along {111} planes and Lomers along (001), however again a kinetic limit is present with annealing. Higher annealing temperatures could be investigated as well as longer anneal times at 650°C in future works but at the risk of de-stabilising the layer.

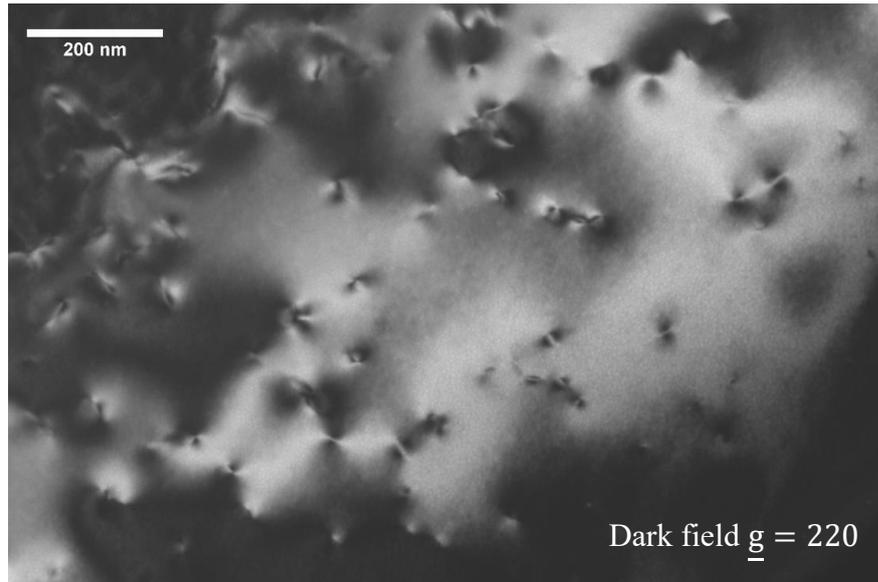


Figure 4.30: Plan view TEM of sample 15-61 (400°C growth + 650°C for 5 mins 78nm thickness). TDD for this image is $6.18 \times 10^9 \text{ cm}^{-2}$. Average TDD for this sample is $7.57 \times 10^9 \text{ cm}^{-2}$.

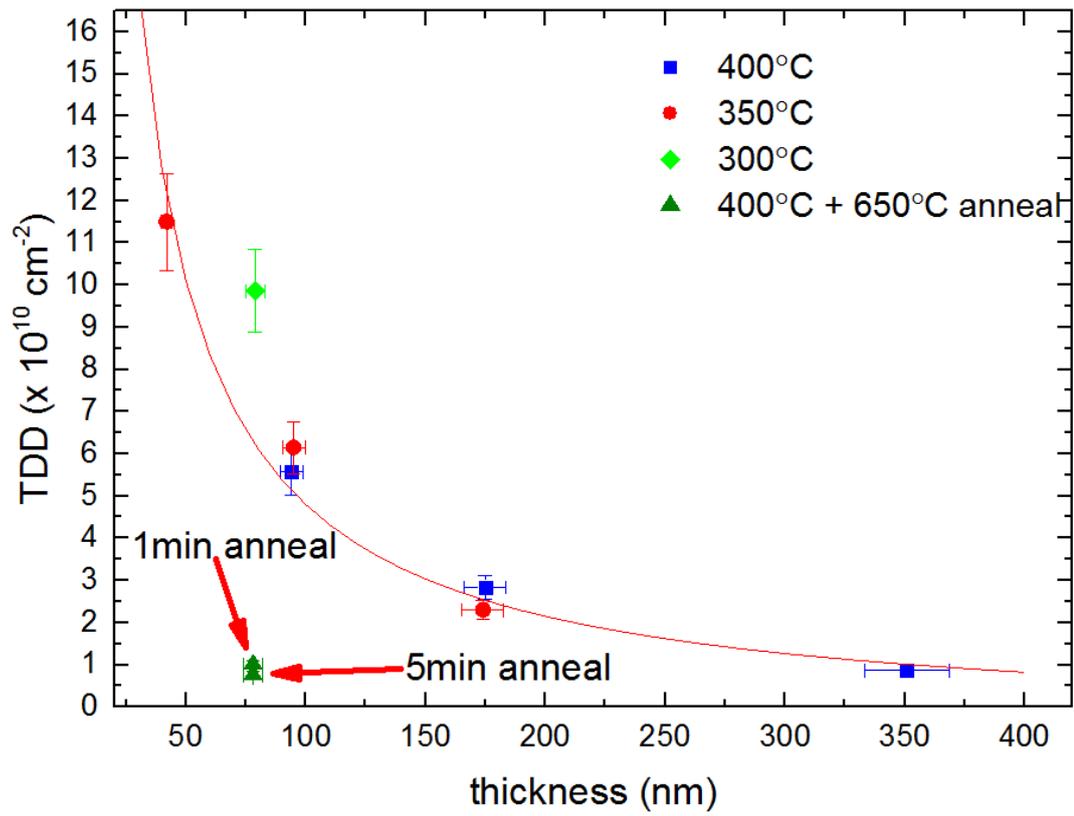


Figure 4.31: Threading dislocation density vs thickness for LT-Ge buffer layers

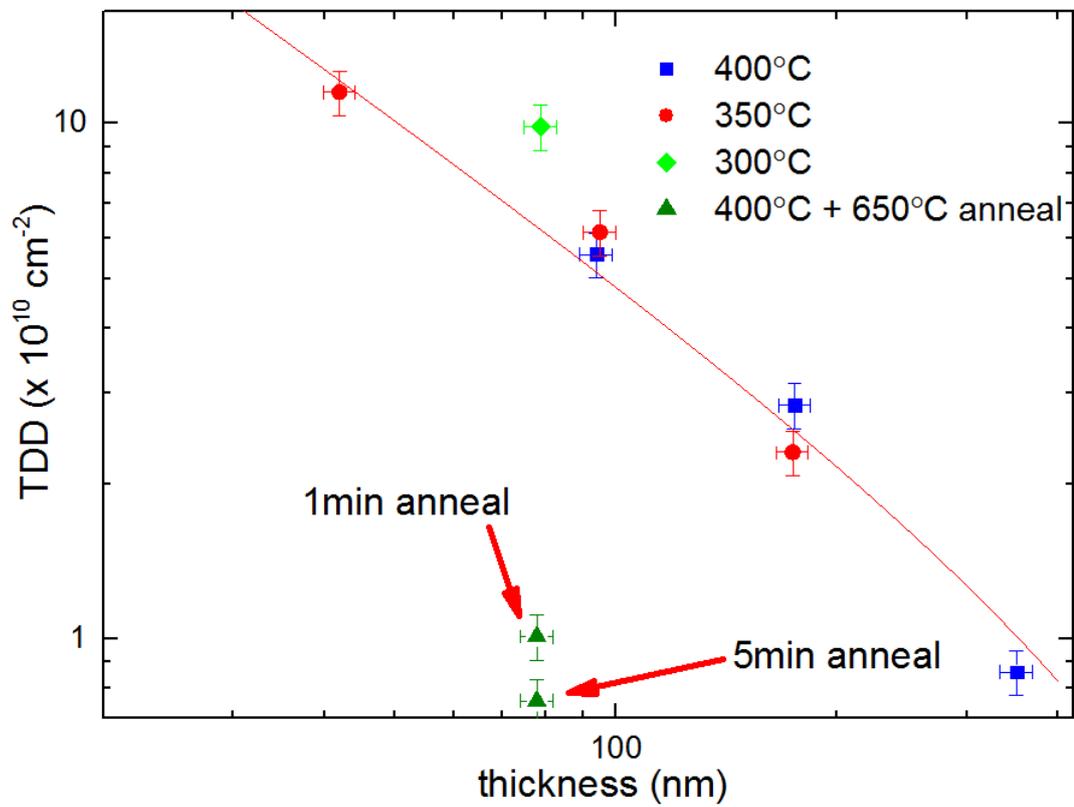


Figure 4.32: TDD vs thickness for LT-Ge buffer layers plotted on log scales

4.3. Chapter 4: Summary

In this work, LT-Ge buffer layers on Si(001) were produced via RP-CVD and investigated for material quality. Faceted islands form when the growth temperature is $\leq 350^\circ\text{C}$ and has been shown to emerge from 2D defects generated during initial growth stages along $\{111\}$ planes. The faceted features themselves may prove to be useful as a somewhat “patterned” surface for the subsequent growth of $\text{Si}_{1-x}\text{Ge}_x$ or III-V material such as InSb, for the purposes of aspect ratio trapping.

The second part of this investigation showed that the traditional HT Ge layer could be omitted entirely by adjusting the annealing time and temperature of the LT Ge layer and potentially neutralising the strain completely. As will be explained in Chapter 5, cracking of the reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layer is a major problem. One solution is to make the heterostructure thinner and minimise the total amount of tensile strain by having a thin strain neutralised Ge underlayer. Current state of the art LT/HT Ge buffer layers are 760nm to $1.2\mu\text{m}$ thick, are 1nm rough, have a TDD of $2 \times 10^7\text{cm}^{-2}$ but are 0.2% tensile strained. However, in this investigation an alternative almost fully relaxed Ge buffer layer is produced consisting of LT-Ge + between 1 to 5min anneal to produce layers that are 78nm thick, 2nm rough, and between -0.037% and 0.036% strained but a TDD of between 10.1 and $7.57 \times 10^9\text{cm}^{-2}$ respectively.

Neutralising strain in the Ge buffer layer is important in perfectly lattice matching GaAs to Si(001), where thermal expansion in state of the art LT/HT Ge buffer layers increases the lattice mismatch from -0.08% to -0.3% even when grown on 6° off-axis substrates [148]. This higher mismatch percentage will reduce the GaAs critical thickness, at which 60° misfit dislocations are generated.

Both the thickness of the LT-Ge layer, anneal temperature and annealing time are crucial parameters that need to be investigated further from a nano-scale diffusion perspective to prevent the substrate from diffusing into the epilayer if even thinner, fully strain neutralised Ge buffer layers are to be produced with even lower TDD.

The types of misfit dislocations at the interface between Ge epilayer and substrate are observed to be a combination of Lomer and 60° misfit dislocations when growing at

400°C or less. When annealing for 1 min at 650°C the strain has transitioned from compressive to tensile and the Lomer network has become more uniformly distributed through (001) glide and the TDD has dropped by a factor of $\approx \times 6$ through the {111} plane glide of 60° misfits.

It is hypothesised that by annealing the 351nm layer (sample 15-38) at 650°C for 5 mins will drop the TDD count from $9.13 \times 10^{-9} \text{cm}^{-2}$, transition the layer from 0.2% compressive strain to marginally tensile strain and reduce the roughness without causing significant inter-diffusion. Thus making a buffer layer at half the thickness of the current state of the art LT/HT layers.

5. Graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers on Si(001).

5.1. Background to $\text{Si}_{1-x}\text{Ge}_x$ buffer layers on Si(001)

Unlike growing pure Ge buffer layers on Si(001), growing $\text{Si}_{1-x}\text{Ge}_x$ is more complicated because it is a random alloy of silicon and germanium with varying material properties depending on the composition of the alloy. For example, surface segregation is more likely to occur with $\text{Si}_{1-x}\text{Ge}_x$ growth on Si(001) than on Ge(001) substrates because Ge adatoms have higher surface mobility than Si adatoms and this surface mobility is heavily dependent on whether the strain is compressive or tensile [149]. The importance of having strain relaxed $\text{Si}_{1-x}\text{Ge}_x$ buffer layers lie in the tunability of the in-plane lattice constant to a particular III-V compound listed in table 2.3 thereby allowing lattice matched integration onto Si(001) substrates.

There are a number of grading techniques used to create strain relaxed buffers such as ion implantation, which involves ion bombardment of the substrate followed by high temperature anneal [150], and Ge condensation which involves depositing SiGe on a SOI substrate and then selective oxidation of the Si on the surface of the SiGe thereby increasing the Ge composition of the layer [151]. However, for the purposes of this chapter the four most relevant grading techniques will be discussed.

5.1.1. Constant composition $\text{Si}_{1-x}\text{Ge}_x$

The first method to depositing $\text{Si}_{1-x}\text{Ge}_x$ on Si(001) would be to grow a constant composition layer directly onto the substrate, of desired Ge% just as is done with pure Ge buffer layers. The layer would be thick enough, so that it has undergone strain relaxation. It has been seen in recent studies that if the growth temperature is too high then strong Stranski-Krastanov growth takes place [152]. Thick (1 μm) high Ge content ($x=0.75$) constant composition $\text{Si}_{1-x}\text{Ge}_x$ buffer layers using LEPECVD at 475°C growth temperature have shown TDD greater than $1 \times 10^9 \text{cm}^{-2}$ with the generation of both 60° dislocations and vertical dislocations along [001] direction. The misfit dislocations are generated at the interface only and so cross hatching on the surface is not seen and so the layers do not have very high roughness [153]. Incomplete relaxation is observed in constant composition layers, especially for low Ge content layers since there is a higher propensity of 60° misfits to be generated as strain relieving mechanism which can cause dislocation blocking.

5.1.2. Step graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}_{1-y}\text{Ge}_y$

In this technique the desired constant composition layer is obtained by growing a thick step $\text{Si}_{1-y}\text{Ge}_y$ layer with a Ge content of $x \leq y \leq 0$ on Si(001) substrate first. The $\text{Si}_{1-x}\text{Ge}_x$ layer is then grown on top [154]. The purpose of doing this to prevent excess misfit dislocations from being generated and reduce mutual threading dislocation blocking by splitting the mismatch between the two interfaces: substrate/ $\text{Si}_{1-y}\text{Ge}_y$ and $\text{Si}_{1-y}\text{Ge}_y/\text{Si}_{1-x}\text{Ge}_x$. Recently Chrastina et al grew a 500nm $\text{Si}_{0.6}\text{Ge}_{0.4}$ step on the substrate then grew a 500nm $\text{Si}_{0.25}\text{Ge}_{0.75}$ layer at 475°C [153]. The TDD was found

to have been reduced to $7.8 \times 10^7 \text{ cm}^{-2}$ compared to an equivalent $\text{Si}_{0.25}\text{Ge}_{0.75}$ layer deposited on the substrate.

5.1.3. Linearly graded $\text{Si}_{1-x}\text{Ge}_x$

The most extensively researched grading technique is the linear grading process. The linear grading technique can be traced back to work carried out by Fitzgerald et al in 1991 [155]. The technique involves growing a graded $\text{Si}_{1-x}\text{Ge}_x$ layer on the substrate first where the Ge content is increased linearly at a constant Ge% per micron to a value x . Then a constant composition $\text{Si}_{1-x}\text{Ge}_x$ layer is deposited of the x value as at the end of the graded layer. This is carried out by adjusting the mass flow rate ratios of dichlorosilane and germane, set by equation 2.45. The linear grading rate (R_{grlinear}) as a %Ge/ μm is given by the following equation:

$$R_{\text{grlinear}} = \frac{\text{final composition}}{\text{graded layer thickness}} \times 100 \quad (\text{Equation 5.1})$$

The problem with linear grading is compressive strain relaxation which readily leads to surface roughening and dislocation pile-up (see chapter 2.5). As the in-plane, out-of plane and bulk lattice constants are changing across the graded layer, nucleation and glide of dislocations will be spread out across the graded region, which means that the probability of dislocations being annihilated in closed loops is reduced in the graded region.

The work carried out by Fitzgerald et al showed that to create relaxed linearly graded buffer layers the grading rate must be kept low enough to give sufficient time for threading dislocations to glide and prevent surface roughening, especially if the mismatch between the desired composition and the substrate is greater than 2% [109]. Typically, the grading rate should be kept at 10%Ge/ μm . Orthogonal strain fields in linearly graded buffer layers created by $\langle 110 \rangle$ misfit dislocations, create cross hatch patterns on the surface which increase in density as the graded region is linearly graded to higher percentages of Ge leading to rougher surfaces. Fitzgerald et al determined

the following Arrhenius relationship for TDD against growth rate, (R_g), Burger's vector (b), Y is the Young's modulus, ϵ_{eff} is effective strain, B is constant related to the initial glide velocity (as given in equation 2.55) and m is an exponent between 1 and 2 [156]:

$$\text{TDD} = \frac{2R_g R_{gr} e^{\frac{E_{\text{glide}}}{kT}}}{bBY^m \epsilon_{\text{eff}}^m} \quad (\text{Equation 5.2})$$

For linearly graded layers the TDD of the constant composition layer is Ge content dependent. For example: a linearly graded layer to $\text{Si}_{0.7}\text{Ge}_{0.3}$ could have a TDD of $7.5 \pm 2.5 \times 10^5 \text{ cm}^{-2}$ with 97% relaxation [157]. Whilst layers that are linearly graded to pure Ge at 9%Ge/ μm have a TDD $> \times 10^7 \text{ cm}^{-2}$ [109]. When linearly grading to high Ge content the continuous blocking of threading dislocation leads to massive pile-ups and this will distort the surface. Therefore, chemical and mechanical polishing is required when $x=0.5$ in the $\text{Si}_{1-x}\text{Ge}_x$ layer which if grading to pure Ge would bring the TDD in the final Ge layer to $2.1 \times 10^6 \text{ cm}^{-2}$ [116].

5.1.4. Reverse graded $\text{Si}_{1-x}\text{Ge}_x$

The definition of reverse grading is somewhat ambiguous. Fundamentally, reverse grading of $\text{Si}_{1-x}\text{Ge}_x$ involves reducing the Ge content of the layer as it is grown however some works have done so directly onto the silicon substrate, whilst others have deposited a relaxed Ge layer first onto the substrate and then deposited a graded $\text{Si}_{1-x}\text{Ge}_x$ layer where the Ge content reduces as the layer is grown.

For example, Wong et al investigated the deposition of a reverse graded layer straight onto Si(001) [158]. The layer started at the substrate as $\text{Si}_{0.65}\text{Ge}_{0.35}$ and was reverse linearly graded to $\text{Si}_{0.86}\text{Ge}_{0.14}$. This means that there is a decreasing lattice mismatch in the graded layer with increasing distance from the substrate. The graded layer was followed by a constant composition layer of $\text{Si}_{0.75}\text{Ge}_{0.25}$ (65% wrt the substrate) and a 20nm strained Si layer. The TDD of the $\text{Si}_{0.75}\text{Ge}_{0.25}$ was $< 1 \times 10^5 \text{ cm}^{-2}$. A similar

investigation by Liu et al was carried out where $\text{Si}_{0.68}\text{Ge}_{0.32}$ on the $\text{Si}_{0.86}\text{Ge}_{0.14}$ layer and the relaxation wrt the substrate was measured as 85% [159].

Reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$

The reverse graded buffer layer that is more pertinent to this investigation is the reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layer, that was developed recently by Shah et al in 2009 [117]. In this technique, a relaxed LT/HT Ge buffer layer is deposited first on the substrate (between 600nm and 1 μm thickness) and then a reverse graded $\text{Si}_{1-x}\text{Ge}_x$ layer is grown at 850°C where the Ge content is reduced linearly at a constant Ge% per micron to a value x. A constant composition $\text{Si}_{1-x}\text{Ge}_x$ layer is deposited of the same x value as is at the end of the graded layer. The thickness of the LT/HT Ge underlayer was between 760nm and 1.2 μm . In the study carried out by Shah the Ge content in the layer ranged between $0.75 \leq x \leq 1$. The grading rate was defined as:

$$R_{\text{grreverse}} = \frac{(1-\text{final composition})}{\text{graded layer thickness}} \times 100 \quad (\text{Equation 5.3})$$

In terms of dislocation mechanics reverse graded buffers were found not show the emergence pile-up or large surface roughness. The explanation for this was given in that the $\text{Si}_{1-x}\text{Ge}_x$ layers relax under tensile strain on Ge buffer layers. The surface free energy, as mentioned in chapter 2.4.4 determines the growth mode of the epilayer. In figure 2.14 in chapter 2.4.3, the process of adatom transport and adsorption on a surface is explained with the bonding on terrace A being responsible for surface free energy. The experiments by Xie et al showed that undulations do not form in SiGe layers undergoing tensile strain relaxation, regardless of the level of strain, as the formation of undulations does not minimise the total free energy of the system (see chapter 2.5.2.)

Shah et al determined that for a reverse grading rate of between 10% Ge/ μm and 100% Ge/ μm , TDD values of $\times 10^6 \text{cm}^{-2}$ were obtained for a Ge underlayer of 1 μm thick and a TDD of $2 \times 10^7 \text{cm}^{-2}$. The existing threading dislocations in the Ge underlayer will be nucleation centres for the glide of misfit dislocations, as shown in the Matthew Blakeslee model (figure 2.34) which is more energetically favourable than

heterogeneous half loop generation. The glide regime critical grading rate for reverse graded $\text{Si}_{1-x}\text{Ge}_x$ was determined to be $124\% \text{Ge}/\mu\text{m}$. Below a grading a rate of $61.3\% \text{Ge}/\mu\text{m}$ the $\text{Si}_{1-x}\text{Ge}_x$ layer was found to grow in Frank van der Merwe mode which is much higher than the $10\% \text{Ge}/\mu\text{m}$ grading rate limit for linearly graded buffers. The reason for this was determined to be the higher glide velocities associated with high Ge content layers. It was explained that the reason for the layer becoming rough beyond $124\% \text{Ge}/\mu\text{m}$ grading rate is due to relatively high growth temperatures, growth rates and strain at the various interfaces.

The biggest problem with reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers is that it is prone to cracking under tensile strain. The cracks have been observed to form after stress-based cleaving of the wafer. It was noted that for a $\text{Si}_{0.25}\text{Ge}_{0.75}/\text{Ge}$ buffer layer, a total heterostructure thickness below $2.7\mu\text{m}$ leads to no cracks being formed.

5.2. This study on $\text{Si}_{1-x}\text{Ge}_x$ graded buffer layers using RP-CVD

The first part of this investigation involves growing $\text{Si}_{1-x}\text{Ge}_x$ buffer layers at 850°C on Si(001) on axis substrates using the well-established linear grading (LG) technique between $0.089 \leq x \leq 0.636$.

The second part of this investigation involves growing $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers on Si(001) using the reverse linear grading (RLG) technique. Previous works have reverse graded up down $x = 0.75$ from $x=1$ [96]. In this chapter the buffer will be reverse graded lower to $x=0.45$ and compared to the linear graded buffers. The LT/HT temperature Ge buffer layer was used (as opposed to the LT + 650°C anneal from chapter 4) because it has a known low TDD of approximately $1(+/-0.1) \times 10^8 \text{cm}^{-2}$ which is much lower than $6.2 \times 10^9 \text{cm}^{-2}$ of the LT + 650°C anneal Ge buffer layer and is a good compromise in thickness to TDD ratio and an attempt to keep the total thickness low and prevent the formation of cracks in the heterostructure. The low temperature region is 95nm and the high temperature layer is 460nm making a total thickness of approximately $555\text{nm} +/- 30\text{nm}$. Two samples were grown on 6° off-axis substrates and

the results are given in this chapter, however the off-axis samples will be discussed in chapter 6. The reverse linearly graded samples will then be compared to the linearly graded samples and conclusions drawn.

The final part of this investigation involves the growth of a new type of reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer: the reverse step graded buffer layer. With this type of buffer layer, instead of reverse linearly grading to desired Ge composition by gradually adjust the dichlorosilane to germane ratio, a constant composition layer $\text{Si}_{1-x}\text{Ge}_x$ buffer layer is deposited on the LT/HT Ge underlayer on an on axis Si(001) substrate, with an instantaneous increase in dichlorosilane. The purpose of this type of structure is to avoid creating thick reverse graded layers when trying to access low Ge content $\text{Si}_{1-x}\text{Ge}_x$ buffer layers which can cause cracks, whilst taking advantage of tensile strain relaxation for surface smoothing and dislocation glide. The $\text{Si}_{1-x}\text{Ge}_x$ composition range in the step graded buffer is $0.9 \leq x \leq 0.47$.

The substrates used in this chapter are 525 μm thick, 100mm Si(001) 0° on-axis with a tolerance of $\pm 0.5^\circ$ and 6° off-axis towards the [110] direction with a tolerance of $\pm 0.5^\circ$ in both cases. The thickness of the substrates is 525 μm . Before deposition a 1000 $^\circ\text{C}$ bake was carried out to remove the native oxide.

5.3. Linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer design.

$\text{Si}_{1-x}\text{Ge}_x$	00:05:00
Linearly graded $\text{Si}_{1-x}\text{Ge}_x$	00:10:00
p ⁻ Si(001)	

Figure 5.1: Schematic of the linearly graded buffer structure. The graded layer was created by adjusting $\text{F}(\text{GeH}_4)$ whilst keeping the flowrate of DCS constant. The growth temperature was kept fixed at 850 $^\circ\text{C}$.

The pressure used in the growth of $\text{Si}_{1-x}\text{Ge}_x$ layers was reduced to 20 Torr and the H_2 carrier flow rate was kept at a constant 20,000 sccm. The GeH_4 flow rate was kept

constant throughout and the SiCl_2H_2 flow rate was ramped down to reach the desired Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ layer, by solving equation 2.30. All Si substrates used in the linearly graded batch are nominal (001).

The growth time for both the graded layer and the constant composition layers are kept constant for all of the samples. This means that within a fixed amount of time the flow rate ratios of GeH_4 and SiH_2Cl_2 are adjusted to give a value for x in equation 2.30. As a consequence, the samples will all have different grading rates. Annealing was not carried out after the buffer layer is grown, as the growth temperature is already quite close to the melting temperature of Ge, and had to be fairly high so that growth is taking place in the mass limited regime at 100 Torr pressure.

The graded region was estimated by measuring the distances between the start of the misfit network at the substrate interface to where it finishes in the buffer layer in (004) diffraction condition, even though the dislocation network finishes before the end of the graded layer [111]. A compositional tool such as secondary ion mass spectroscopy was not used in this study and therefore a slightly larger error is placed on the measured thickness of the graded region. For the sake of analysis, samples with similar grading rates ($\pm 2.5\% \text{Ge}/\mu\text{m}$ from the mean) were taken and grouped together collectively.

Sample number	Ge composition (+/- 0.5%)	Grading rate (%Ge/ μm) ($\pm 5\%$)	Total buffer thickness (μm) ($\pm 2\%$)	In-plane lattice constant (\AA)
13-217	0.113	13.400	1.860	5.45042
13-101	0.146	13.640	2.020	5.45341
13-219	0.098	15.600	1.850	5.44866
13-218	0.137	19.800	1.493	5.45370
13-117	0.119	19.900	1.221	5.45067
13-100	0.089	20.370	1.709	5.44471
13-102	0.209	20.900	1.997	5.47106
13-221	0.188	27.000	1.170	5.46262
13-118	0.168	35.000	1.160	5.45876
13-220	0.245	37.300	1.040	5.47493
13-095	0.229	39.500	1.080	5.46133
13-119	0.335	56.000	1.093	5.49764
13-096	0.431	98.000	1.050	5.51082

13-120	0.565	103.000	1.085	5.54688
13-099	0.608	130.500	1.140	5.52942
13-121	0.636	135.900	1.092	5.56909

Figure 5.2: Linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer samples grown on on-axis $\text{Si}(001)$. Listed in order of increasing grading rate

5.3.1. Buffer quality, surface morphology, strain and defect comparison at different grading rates and Ge%

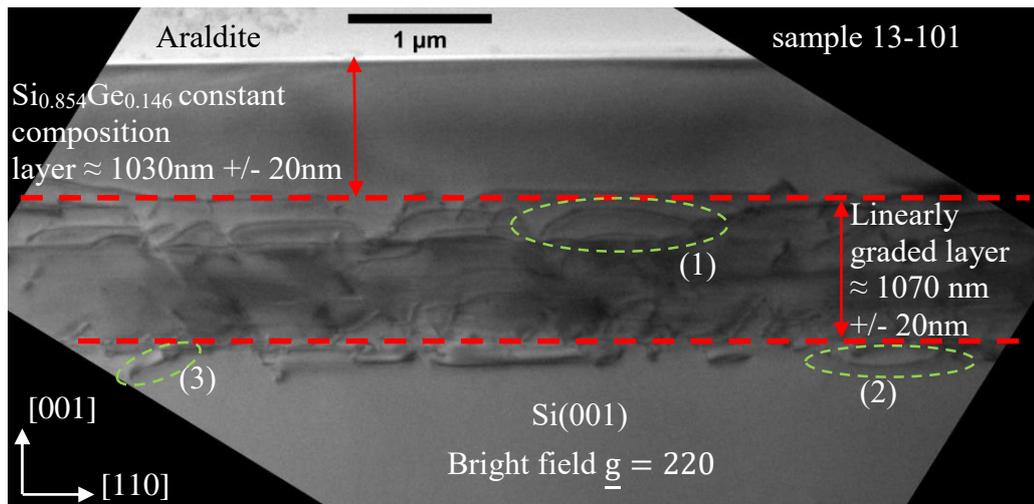


Figure 5.3: X-TEM image of sample 13-101 linearly graded to $\text{Si}_{0.854}\text{Ge}_{0.146}$ buffer layer total thickness is $2020\text{nm} \pm 10\text{nm}$ with a grading rate of $13.64\% \text{Ge}/\mu\text{m} \pm 5\%$. $R_{\text{rms}} = 1.27\text{nm}$. The green dashed circles indicate Frank-Read loops.

With linear grading, the grading rate is crucial in determining the surface quality of the layer as well as promoting glide of existing dislocations and preventing nucleation of new dislocations. At a low grading rate ($\approx 13.64\% \text{Ge}/\mu\text{m}$) in the grading layer, the constant composition layer follows a Frank Van der Merwe growth mode as seen in figure 5.3.

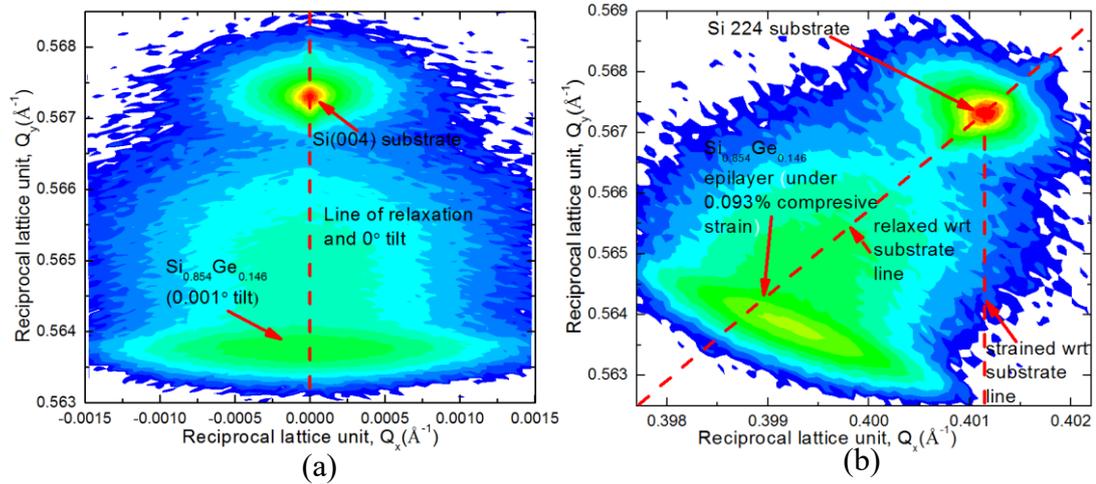


Figure 5.4: 004 and 224 HR-XRD RSM of sample 13-101, linearly graded to $\text{Si}_{0.854}\text{Ge}_{0.146}$. Total buffer layer thickness is 2020nm \pm 10nm with a grading rate of 13.4%Ge/ μm \pm 5%.

In the HR-XRD RSM of sample 13-101 (figure 5.4), it is seen that the $\text{Si}_{0.854}\text{Ge}_{0.146}$ is under 0.093% compressive strain and has a bulk lattice constant of 5.46079\AA , suggesting a lattice mismatch of 0.548% to the substrate. This lattice mismatch is ideal for 60° misfit dislocations to be generated which would undoubtedly cause dislocation pinning and bowing. Frank-Read dislocation loops readily form in the graded layer and at the 850°C growth temperature, they also penetrate into the substrate as seen by loops (2) and (3) in figure 5.3. The compressive 0.093% strain means less energy is available to allow threading dislocations to glide. Figure 5.5(a) shows an AFM micrograph of sample 13-101, which shows etch pits on the surface. HCl was not introduced during growth, however if temperature and surface chemistry permits, the surface could be in the etching regime as chlorine ions desorb from the (001) surface and take Si and Ge atoms with it; as shown in figure 2.10 in chapter 2.4.1.1 and equations 2.18 and 2.27. Figure 5.5 (b) is a plan view TEM image of the sample in 220 diffraction condition on a single etch pit.

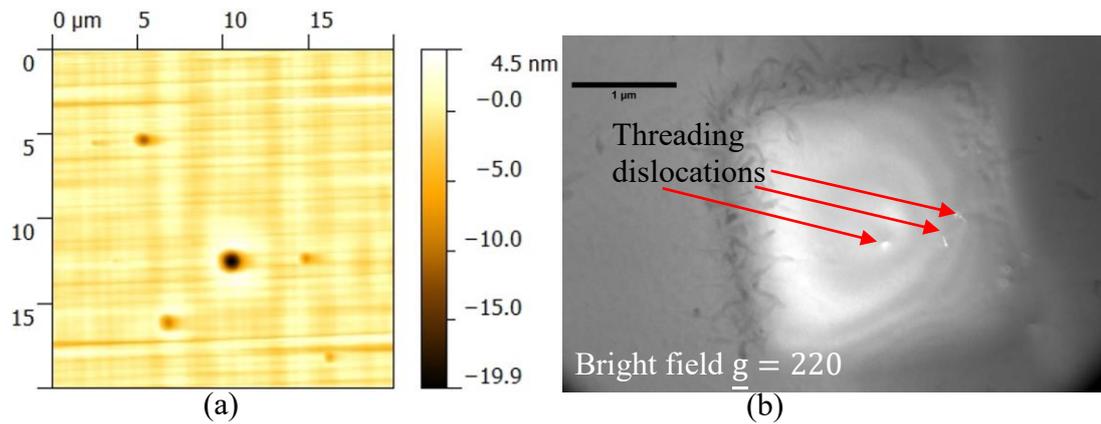


Figure 5.5: (a) 20µm x 20µm Contact mode AFM of 13-101, linearly graded to $\text{Si}_{0.854}\text{Ge}_{0.146}$. $R_{\text{rms}} = 1.27\text{nm} \pm 0.2\text{nm}$. Total buffer layer thickness is 2020nm $\pm 10\text{nm}$ with a grading rate of 13.4%Ge/µm $\pm 5\%$. Figure (b) is a plan view TEM image of an etch pit showing a threading dislocation at the centre of the pit.

The HCl etch pits were only observed in samples with a grading rate of below 20%Ge/µm. A possible explanation for this is that low grading rates equate to a reduced change in lattice constants between atomic layers meaning that strain in the graded layer is kept low and thus threading dislocations can be blocked by orthogonal strain fields. Once they are blocked and given the 850°C growth temperature, etching around the dislocation on the {111} planes can happen readily by the chlorine species leading to inverted pit pyramid features. Figure 5.6 shows a series of DIC optical images taken of sample 13-101, where the sample was etched with Schimmel for short periods of time to see how the surface changes. The chlorine in-situ etching seems to have a lower selectivity than Schimmel, meaning that it reveals fewer threading dislocations. The greatest chlorine etch pit densities were seen in the samples with the lowest grading rates: sample 13-217 and sample 13-219

As the sample is continuously etched anisotropically, the surface begins to show how the linearly graded region effects epitaxy by creating orthogonal strain fields and thus the cross hatching effect becomes stronger as the graded region is approached. The strain fields also block threading dislocations creating pile-up as seen in figure 5.6 (f). The total threading dislocation density counted was the sum of pile-up and field as the two could not be readily distinguished.

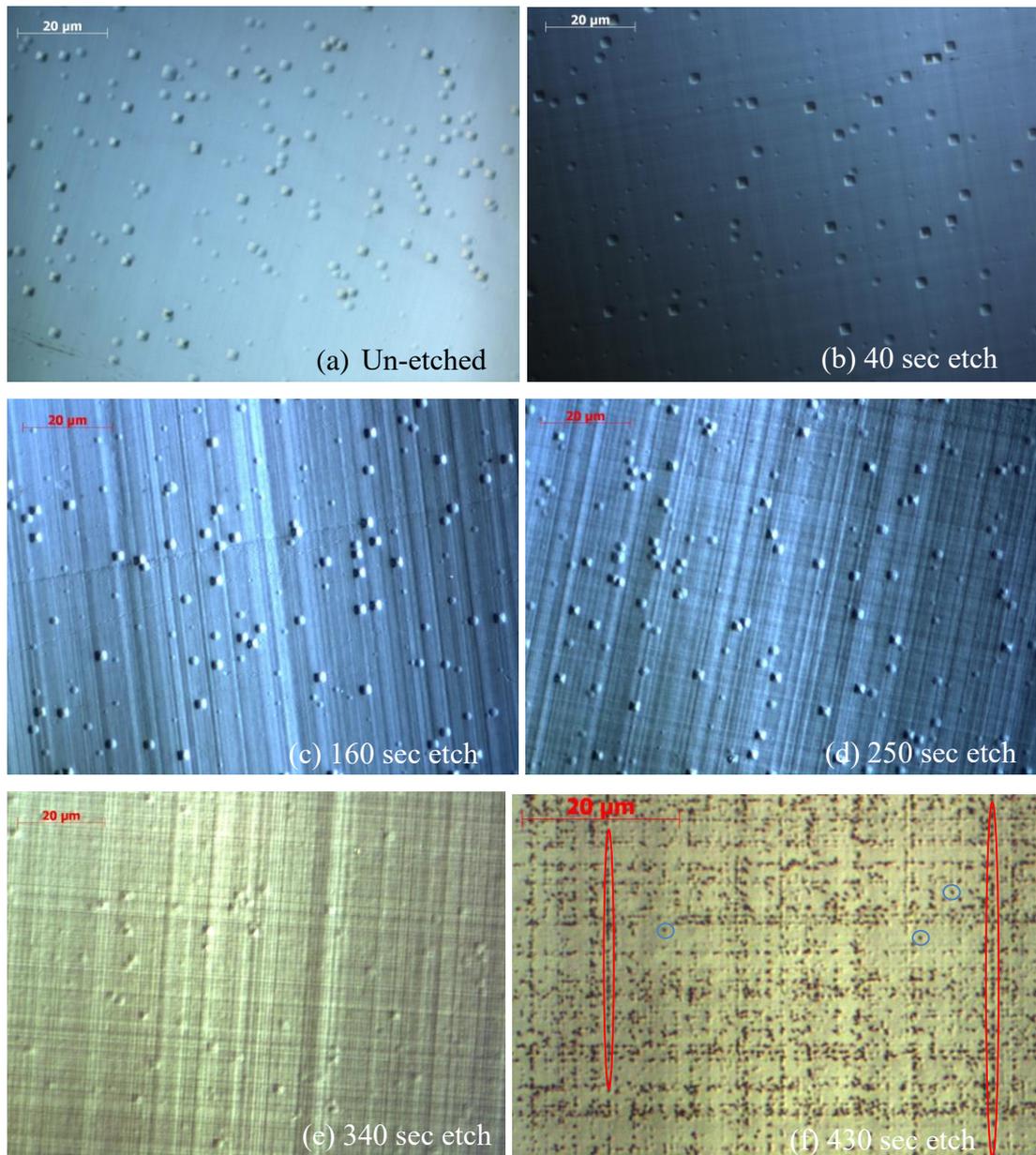


Figure 5.6: DIC optical microscope images of sample 13-101 $\text{Si}_{0.854}\text{Ge}_{0.146}$ after Schimmel etching for different periods of time (a) - (f), revealing threading dislocations. Total buffer layer thickness is $2020\text{nm} \pm 10\text{nm}$ with a grading rate of $13.4\% \text{Ge}/\mu\text{m} \pm 1\%$. Average TDD (pile up + field) taken from images etched for 430 secs = $9.10 \times 10^7 \text{cm}^{-2}$. The two red orthogonal ellipses in the diagram indicate pile up of threading dislocations and the blue circles shows field threading dislocations.

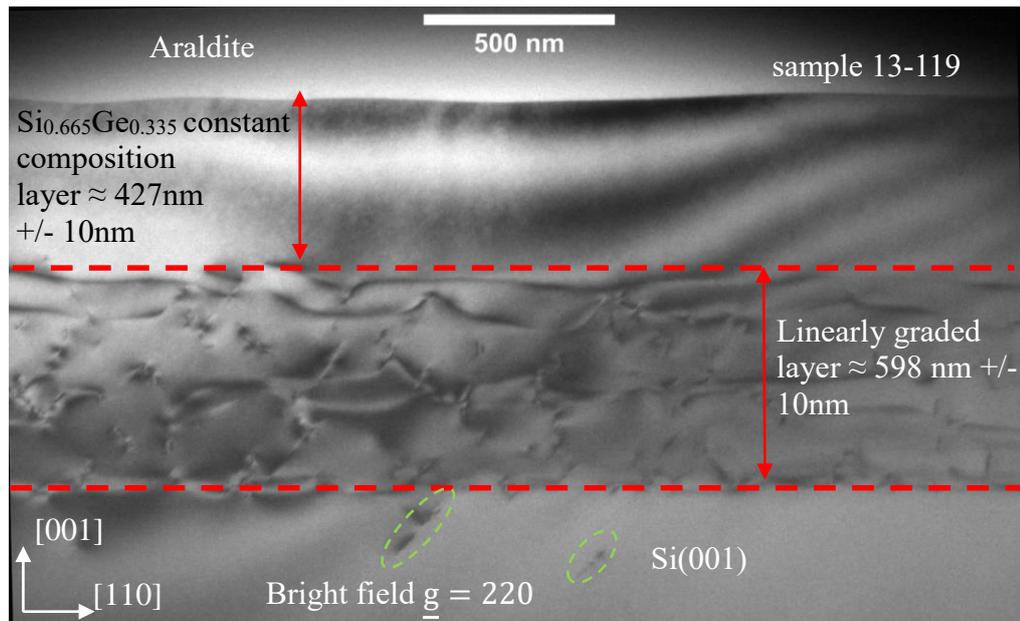


Figure 5.7: X-TEM image of sample 13-119 linearly graded to $\text{Si}_{0.665}\text{Ge}_{0.335}$ buffer layer total thickness is $1093\text{nm} \pm 5.5\text{nm}$ with a grading rate of $56\% \text{Ge}/\mu\text{m} \pm 1\%$. $R_{\text{rms}} = 4.73\text{nm}$.

When the grading rate is increased to $56\% \text{Ge}/\mu\text{m}$, figure 5.7 shows a sample that has been linearly graded to 33.5% Ge and from the outset it is seen that the surface has undulations. Dislocations are seen in the substrate as shown by the green dashed circles. The graded regions are taken at the points where the 60° misfit segment starts and ends as shown by the red dashed lines.

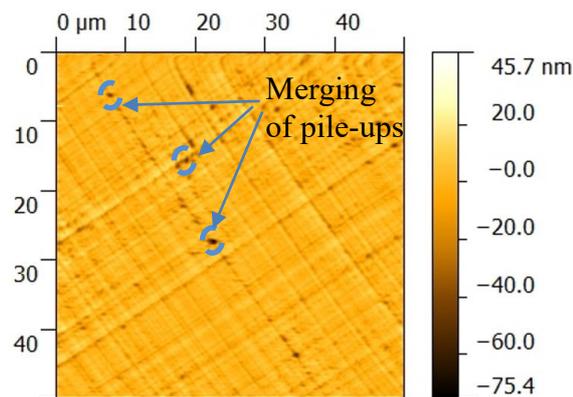


Figure 5.8: $50\mu\text{m} \times 50\mu\text{m}$ contact mode AFM of sample 13-119 linearly graded to $\text{Si}_{0.665}\text{Ge}_{0.335}$ buffer layer total thickness is $1093\text{nm} \pm 10\text{nm}$ with a grading rate of $56\% \text{Ge}/\mu\text{m} \pm 1\%$. $R_{\text{rms}} = 4.73\text{nm}$. Strong cross hatching is seen as well as large pits along cross hatch lines indicating merging of pile-up TDs into large pits.

In the XRD RSMs of sample 13-119 (figure 5.9), the $\text{Si}_{0.665}\text{Ge}_{0.335}$ peak is heavily tilted to 0.559° as seen in the 004 reflection. This is probably caused by differences in

the Schmidt factor on different glide systems, favouring particular Burgers vector for the Frank-Read mechanism relaxing the layer, which leads to bowing of the misfit dislocation and the formation of loops. The action of 60° misfit dislocations of like sign is to tilt the lattice of the epitaxial layer (see chapter 2.5.10). Sample 13-119 has the highest measured compressive strain in the constant composition layer of all of the linearly graded samples.

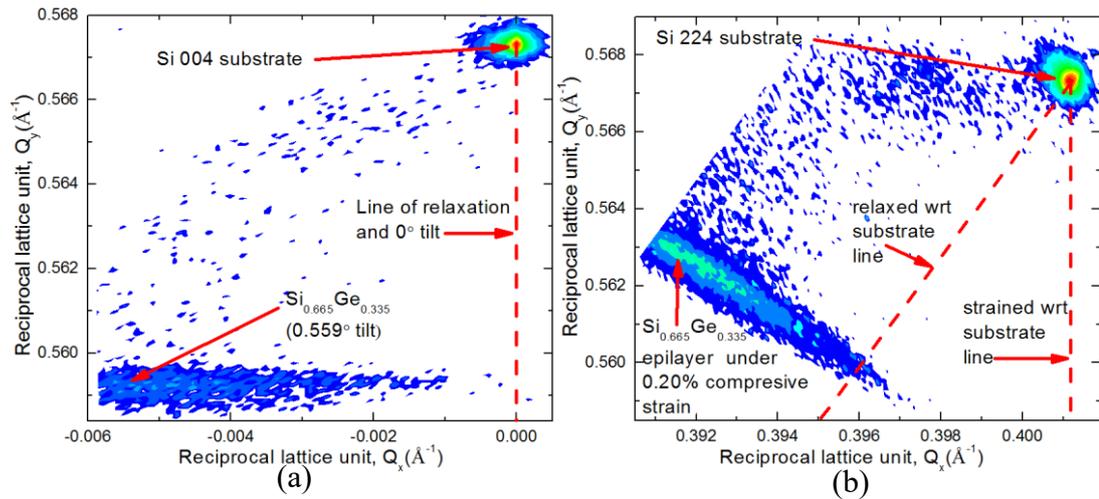


Figure 5.9: HR-XRD of sample 13-119, linearly graded to $\text{Si}_{0.665}\text{Ge}_{0.335}$. Buffer layer total thickness is 1093nm \pm 10nm with a grading rate of 56%Ge/ μm \pm 1%. Notice the large tilt in SiGe epilayer possibly due to strain relaxation via the modified Frank-Read mechanism.

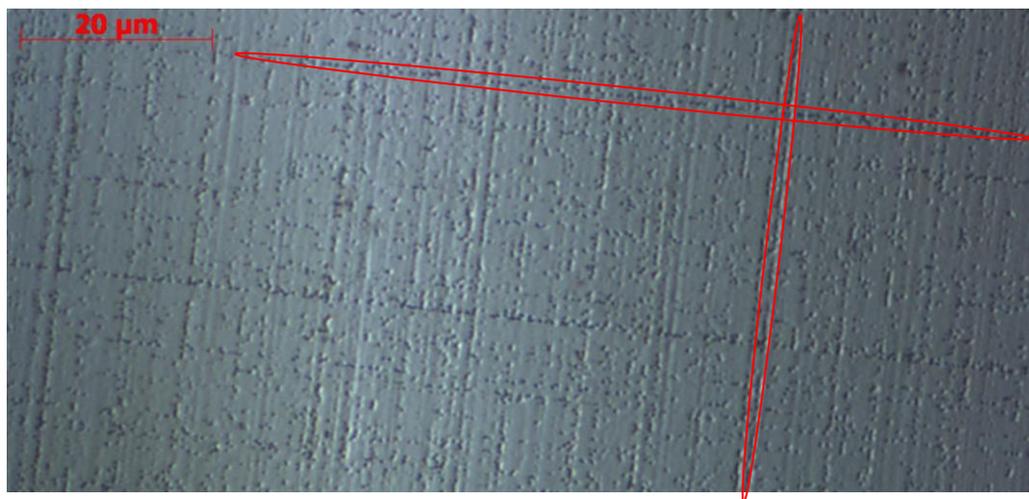


Figure 5.10: DIC optical microscope image of sample 13-119 linearly graded to $\text{Si}_{0.665}\text{Ge}_{0.335}$ buffer layer total thickness is 1093nm \pm 10nm with a grading rate of 56%Ge/ μm \pm 1%. The sample has been Schimmel etched for 190 secs. Average TDD (pile up + field) = $5.26 \times 10^7 \text{ cm}^{-2}$. The two red orthogonal ellipses in the diagram indicate pile up of threading dislocations.

A grading rate of 56%Ge/ μm , is approximately the optimum grading rate which creates enough strain in the graded region to promote glide. As a consequence, the TDD of the layer is slightly lower as shown in figure 5.10. The merging of pile-ups in to large pits effects the surface undulation formation even more which leads to higher surface roughness in the layer as shown in figure 5.8.

When linearly grading to a 63.6% Ge and at a grading rate of 135.9%Ge/ μm (sample 13-121) a high degree of dislocations and 2D defects can be seen (5.13). It cannot be said for certain if these 2D defects are micro twins or stacking faults without obtaining high resolution images.

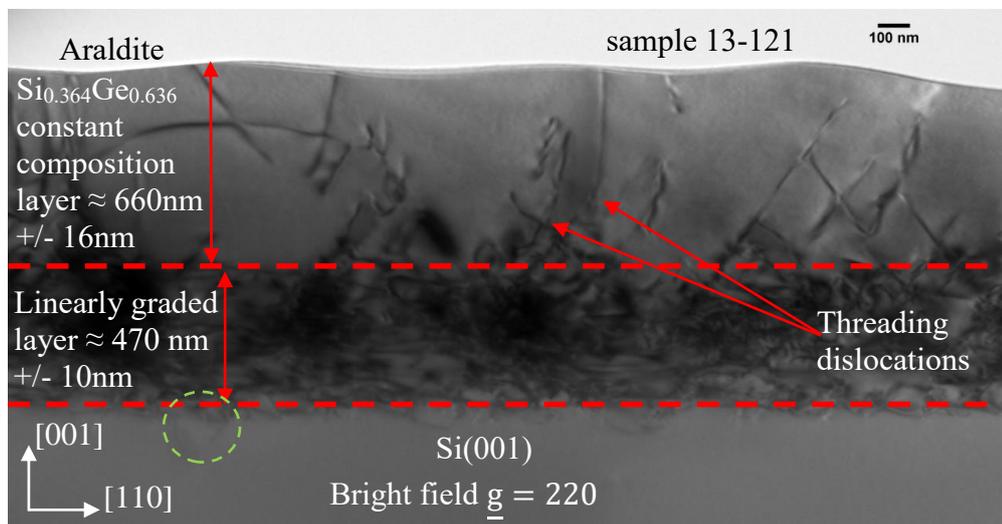


Figure 5.11: X-TEM image of sample 13-121 linearly graded to $\text{Si}_{0.364}\text{Ge}_{0.636}$ buffer layer total thickness is 1092nm \pm 10nm with a grading rate of 135.9%Ge/ μm \pm 1%. $R_{\text{rms}} = 26.43\text{nm}$. The green dashed circle is of a dislocation loop that has penetrated into the substrate.

The HR-XRD of sample 13-21 (figure 5.12) shows a layer tilt of 0.24° . As a consequence of having such a fast grading rate, the HR-XRD RSM's show a split in the SiGe Bragg peak. This is assumed to be caused by a rigid rotation of the crystal lattice through particular angles as a consequence of forming microtwins from the high layer stress that causes plastic deformation [160]. The micro twins are generated from successive glides of 90° Shockley partial dislocations on {111} planes [161]. One layer is $\text{Si}_{0.365}\text{Ge}_{0.635}$ and is under 0.006% tensile strain whilst the other is $\text{Si}_{0.364}\text{Ge}_{0.636}$ and under 0.038% compressive strain and so is possibly at the bottom. The two layers cannot be distinguished from the X-TEM image (figure 5.10).

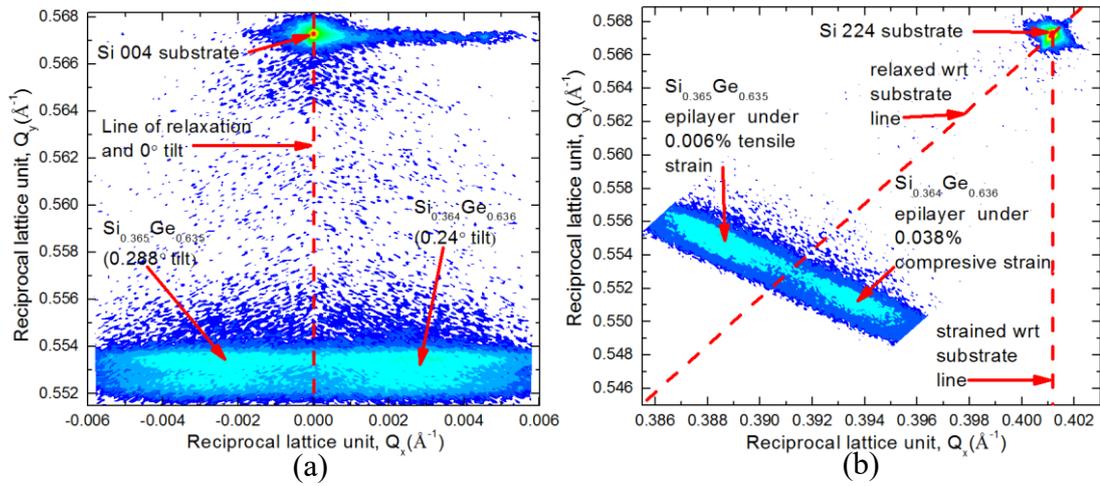


Figure 5.12: HR-XRD of sample 13-121, linearly graded to $\text{Si}_{0.364}\text{Ge}_{0.636}$. Total buffer layer thickness is $1092\text{nm} \pm 10\text{nm}$ with a grading rate of $135.9\% \text{Ge}/\mu\text{m} \pm 1\%$.



Figure 5.13: Plan view TEM of sample 13-121: linearly graded to $\text{Si}_{0.364}\text{Ge}_{0.636}$. Total buffer layer thickness is $1092\text{nm} \pm 10\text{nm}$ with a grading rate of $135.9\% \text{Ge}/\mu\text{m} \pm 1\%$. Average TDD (pile up + field) = $1.58 \times 10^9 \text{cm}^{-2}$. The red circles highlight 2D defects (possibly micro twins) and the arrows point to threading dislocations.

5.4. Reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer design.

$\text{Si}_{1-x}\text{Ge}_x$		00:10:00
Reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x$		00:09:08
LT/HT Ge	555nm	
$p^- \text{Si}(001)$		

Figure 5.14: Schematic of the reverse linearly graded buffer structure. The LT Ge was grown at 350°C and the HT Ge was grown at 550°C using GeH_4 . The graded layer was created by adjusting $F(\text{SiCl}_2\text{H}_2)$ whilst keeping the flowrate of GeH_4 constant. The growth temperature of the $\text{Si}_{1-x}\text{Ge}_x$ was kept fixed at 850°C.

A pure Ge buffer layer is deposited first on the substrate using GeH_4 precursor and H_2 carrier gas. The LT layer is grown at 350°C to 95nm thickness. Then a 550°C high temperature layer is grown to 460nm. The $\text{Si}_{1-x}\text{Ge}_x$ layer is grown at 850°C. Firstly a constant composition $\text{Si}_{0.05}\text{Ge}_{0.95}$ layer was grown on the Ge buffer layer to about 365nm +/- 38nm thickness.

The reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x$ layer was then grown from $x = 0.95$ to a value between $0.717 \geq x \geq 0.45$ over a fixed amount of time. This was carried out by keeping the GeH_4 flow rate constant throughout growth and then gradually increasing the SiH_2Cl_2 flow rate after the Ge underlayer had been grown, in a manner to solve equation 2.45 for x . This also meant that the samples had various grading rates and as with the linearly grade samples however the compositional change over the linear graded samples is over 54.7% Ge whilst the compositional change for the reverse linearly graded samples is 26.7% Ge. Therefore, there was not as much discrepancy in grading rate amongst samples in the reverse linearly graded batch. A final constant composition layer was grown on top of the graded layer with the same value x , as was grown at the end of the graded layer. Annealing was not carried out with the reverse graded buffer samples because the growth temperature is already very close to the melting temperature of Ge. Two reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers were grown on 6° off-axis $\text{Si}(001)$ substrates.

As with the linearly graded samples, the graded region was only estimated through measuring the distance between where the misfit network started (where the constant composition $\text{Si}_{0.05}\text{Ge}_{0.95}$ layer was assumed to have ended) to where the misfit network ended in the 004 diffraction condition.

Sample number	Ge composition ($\pm 0.5\%$)	Thickness of $\text{Si}_{0.05}\text{Ge}_{0.95}$ (nm) ($\pm 10\%$)	Total grading rate (% Ge/ μm) ($\pm 5\%$ Ge/ μm)	Total thickness of buffer layer (nm) ($\pm 30\text{nm}$)	In-plane lattice constant (\AA)
13-132	0.667	401.00	10.58	5782	5.58798
13-131	0.675	370.00	12.42	5583	5.58865
13-165	0.717	401.00	12.77	5535	5.59843
13-166	0.658	371.00	14.30	5800	5.58357
13-116	0.605	362.00	17.34	6040	5.57233
13-133	0.552	414.00	18.12	6561	5.55938
13-114	0.611	284.00	19.19	5409	5.57393
13-115	0.620	401.00	21.68	5725	5.57554
13-134	0.450	381.00	22.85	7584	5.53814
13-130	0.673	336.00	23.04	5408	5.58923
13-113	0.576	303.00	29.68	5041	5.56733
13-163	0.659	374.00	16.48	5597	5.59817
13-162	0.708	353.00	17.34	5172	5.58648

Figure 5.15: List of reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer samples. The samples are listed in order of increasing grading rate, except the bottom two rows, in pink, which were grown on off-axis Si(001)

When growing the heterostructure on 6° off-axis substrates, it was discovered that the thickness of the two buffer layers grown on off-axis substrates were marginally thinner (by approximately 4%) than structures grown on on-axis substrates. This is seen when comparing sample 13-162 (70.8% Ge) with sample 13-165 (71.7% Ge) and when comparing sample 13-163 (95.9% Ge) with sample 13-166 (65.8% Ge) in figure 5.15.

5.4.1. Low temperature/ High temperature Ge underlayer.

The low temperature Ge seed layer was grown at 350°C to 95nm. As seen in figure 4.3(d) (sample 14-302). This gave a starting threading dislocation density of $6.15 \times 10^{10} \text{ cm}^{-2}$ and an R_{rms} of 1.72nm. the Ge buffer layer growth pressure was 100 Torr and the flow rate of GeH_4 is 150 sccm. The temperature is brought up in the CVD chamber to 550°C whilst keeping the GeH_4 to H_2 flow rate constant and so a layer of germanium is deposited at a higher temperature. Annealing was not carried out to minimise the thermal budget applied to Ge underlayer and therefore minimise the strain in order to suppress cracks. The deposition time is varied and hence the layer thickness is also varied.

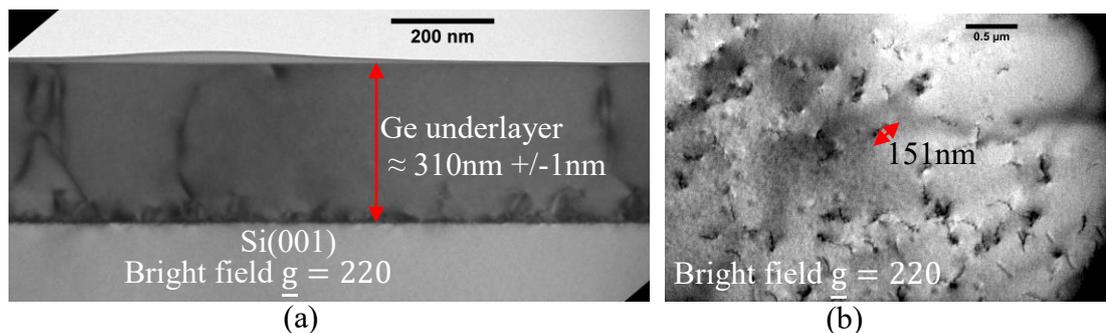


Figure 5.16: (a) X-TEM of 310nm LT/HT Ge buffer layer. (b) 220 plan view TEM image, Average TDD = $1.01 \times 10^9 \text{ cm}^{-2} \pm 10\%$. $R_{\text{rms}} = 2.25\text{nm}$. Typical length of threading dislocation is 151nm.

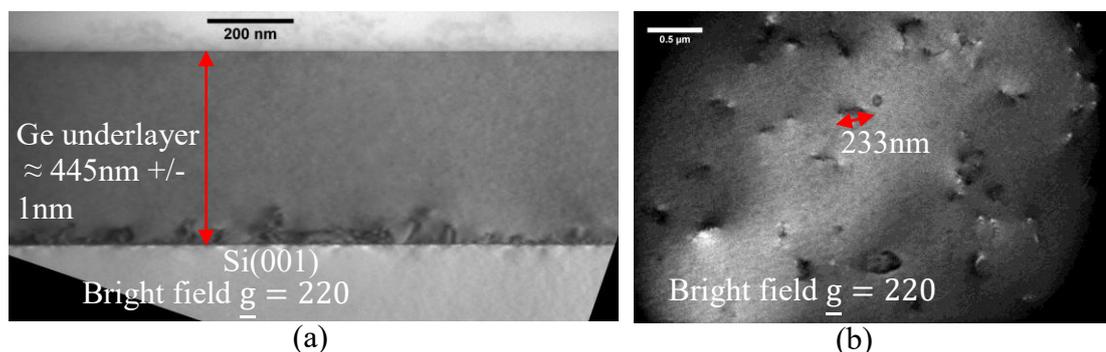


Figure 5.17: X-TEM of 445nm LT/HT Ge buffer layer Average TDD = $3 \times 10^8 \text{ cm}^{-2} \pm 10\%$. $R_{\text{rms}} = 1.46\text{nm}$.

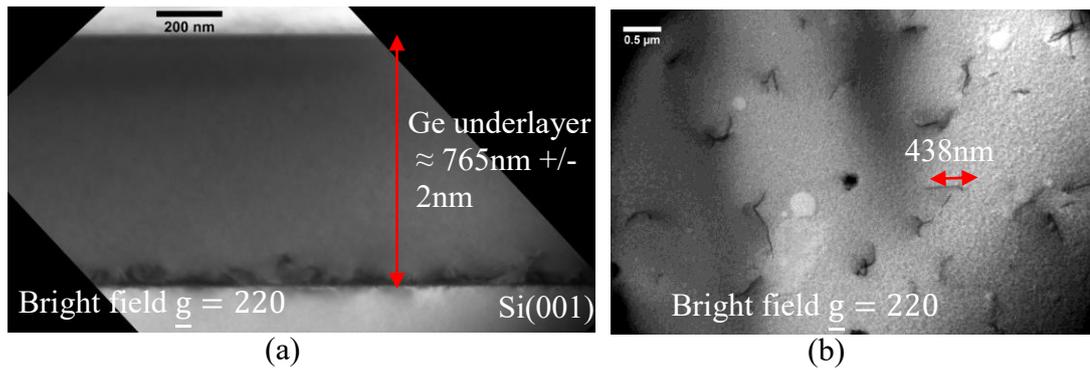


Figure 5.18: X-TEM of 765nm LT/HT Ge buffer layer Average TDD = $1 \times 10^8 \text{cm}^{-2} \pm 10\%$. $R_{\text{rms}} = 0.76 \text{nm}$.

Figures 5.16, 5.17, and 5.18 show how the LT/HT Ge buffer improves in quality and surface roughness, as the thickness of the HT layer is increased. It was determined that a high temperature layer thickness of 460nm (555nm +/- 30nm total Ge underlayer thickness) was a good compromise in terms of TDD, surface roughness ($\approx 1 \text{nm} \pm 0.1 \text{nm}$) and thickness.

5.4.2. Reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers.

The pressure used in the growth of $\text{Si}_{1-x}\text{Ge}_x$ layers was again reduced to 20 Torr and the H_2 carrier flow rate was kept at a constant 20,000 sccm. The GeH_4 flow rate was kept constant throughout however for reverse grading the SiCl_2H_2 flow rate was ramped up to reach the desired Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ layer, by solving equation 2.45.

The grading rates, in this reverse graded buffer investigation, remained under $60\% \text{Ge}/\mu\text{m}$. Shah et al, concluded that provided the grading rate remain under $61.3\% \text{Ge}/\mu\text{m}$, Frank van der Merwe growth takes place [117]. Despite the large error in the grading rate, the grading rate for all of the samples in this batch remained under $61.3\% \text{Ge}/\mu\text{m}$ and so it was observed that they all grew via Frank van der Merwe growth mode even when reverse grading to 45% Ge from pure Ge. This is an astonishing discovery, because this is unlike the linear grading process where even

with a grading rate of 10%Ge/ μm requires CMP when reaching $\text{Si}_{0.5}\text{Ge}_{0.5}$ due to high surface roughening and pile-up due to compressive strain relaxation.

Figure 5.19 is a 004 diffraction condition X-TEM image of sample 13-134 which was reverse graded to $\text{Si}_{0.55}\text{Ge}_{0.45}$. The estimated thickness of the $\text{Si}_{0.05}\text{Ge}_{0.95}$ layer is approximately 381nm \pm 40nm. This measurement was estimated by determining the misfit interfaces between the Ge underlayer and the $\text{Si}_{0.05}\text{Ge}_{0.95}$ layer and determining the interface location of the $\text{Si}_{0.05}\text{Ge}_{0.95}$ layer and the graded region. The graded region measured in (004) bright field is measured as 2197nm and the entire heterostructure is measured to be 7584nm \pm 30nm in (004) dark field. The reverse graded region grading rate is 21.4%Ge/ μm \pm 10%. As is seen in the figure, the surface looks planar and there are no discernible undulations.

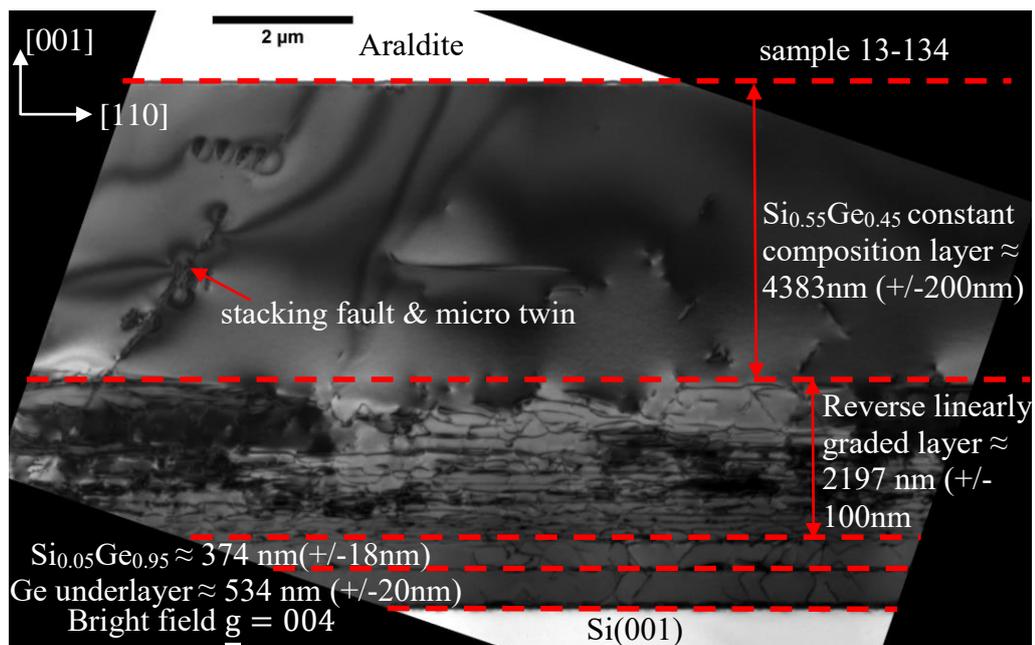


Figure 5.19: X-TEM of sample 13-134, reverse linearly graded to $\text{Si}_{0.55}\text{Ge}_{0.45}$. Buffer layer total thickness is 7584nm \pm 20nm with a total grading rate of 21.4%Ge/ μm \pm 10%. The surface appears to be free of severe undulation formation due to tensile strain relaxation.

From both figures 5.19 and 5.20, it is seen that the constant composition $\text{Si}_{0.55}\text{Ge}_{0.45}$ region is of reasonable crystalline quality. However micro twins (90° and 30° Shockley partial dislocations) and stacking faults are observed in the constant composition layer. When looking at the 220 diffraction condition, orthogonal stacking faults can be seen.

The stacking faults seem to be emerging from the graded region of the buffer layer despite. From defect etching and DIC imaging of the samples, it is seen that the line density of stacking faults increases after the reverse graded region is $\geq 70\%$ Ge. Tensile strain relaxation, the thickness and the Ge content in the reverse graded $\text{Si}_{1-x}\text{Ge}_x$ layer has reached a critical point where the 90° Shockley partial dislocation has disassociated and separated from the 30° Shockley partial dislocation, to form a stacking fault (see chapter 2.5.9).

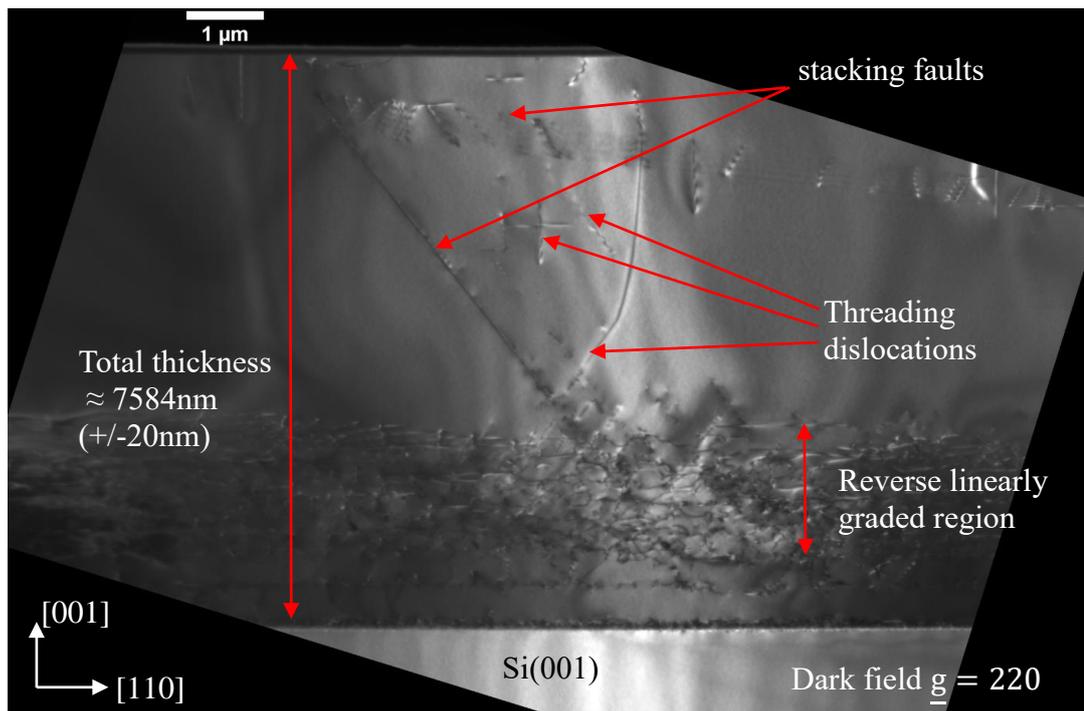


Figure 5.20: X-TEM of sample 13-134, reverse linearly graded to $\text{Si}_{0.55}\text{Ge}_{0.45}$. Buffer layer total thickness is 7584nm ± 10 nm with a grading rate of 21.4%Ge/ μm $\pm 1\%$.

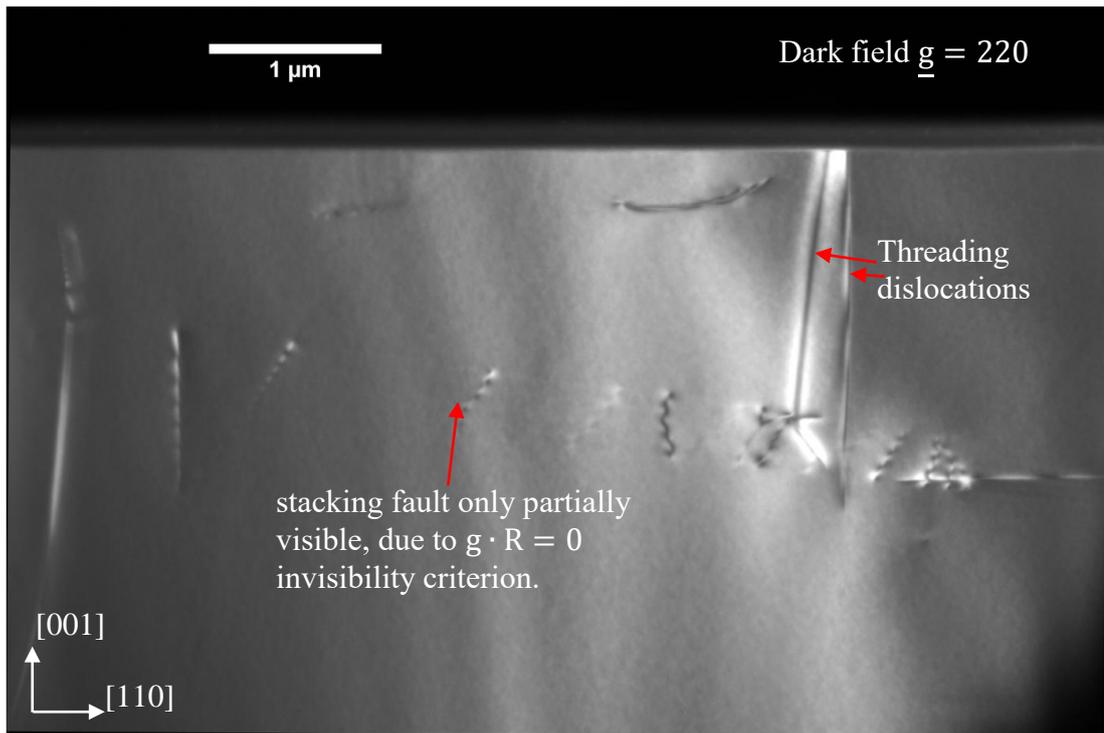


Figure 5.21: X-TEM of sample 13-134, reverse linearly graded to $Si_{0.55}Ge_{0.45}/Ge$ magnified at the top of the constant composition region. A partially visible stacking fault is seen by the position of its partial dislocations.

At the interface between the Ge underlayer and the silicon substrate, Lomer dislocations are seen (figure 5.22), with an average spacing between dislocations of about 10.4nm.

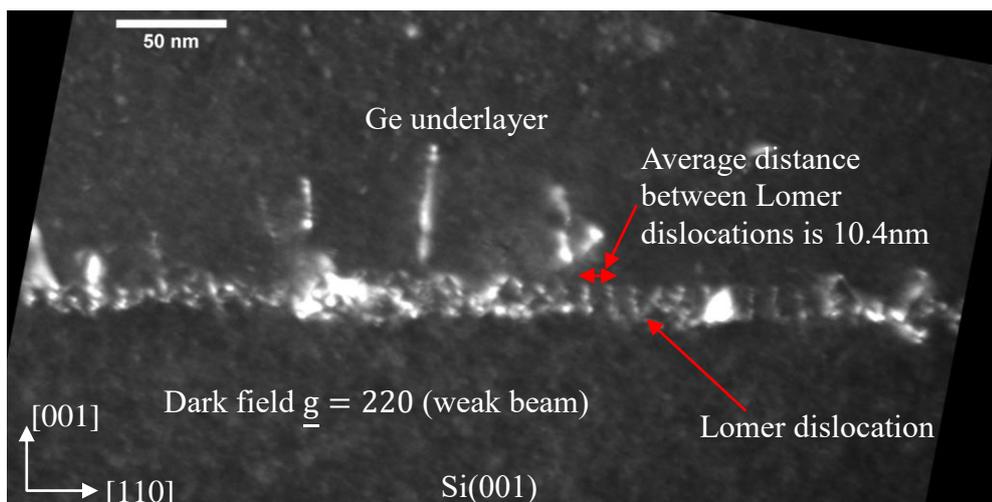


Figure 5.22: X-TEM of sample 13-134, reverse linearly graded to $Si_{0.55}Ge_{0.45}$. at the interface between the Si(001) substrate and the Ge underlayer showing Lomer dislocations.

5.4.2.1. Morphology

In the work by Shah, smooth reverse graded $\text{Si}_{0.25}\text{Ge}_{0.75}/\text{Ge}$ buffer layers with a roughness of $< 4\text{nm}$ [117] were produced. Figure 5.23 is a $20\mu\text{m} \times 20\mu\text{m}$ contact mode scan of sample 13-165, reverse graded $\text{Si}_{0.283}\text{Ge}_{0.717}/\text{Ge}$ sample. The roughness for the sample is measured to be 2.42nm . Figure 5.24 is a contact mode AFM micrograph of sample 13-134. Stacking faults can be in the scan and the R_{rms} for the sample is approximately 3.7nm when measured at $100\mu\text{m} \times 100\mu\text{m}$ in contact mode. The slightly larger roughness in sample 13-134 is attributed to the density of stacking faults whilst the region in between the stacking faults is planar and reasonably smooth.

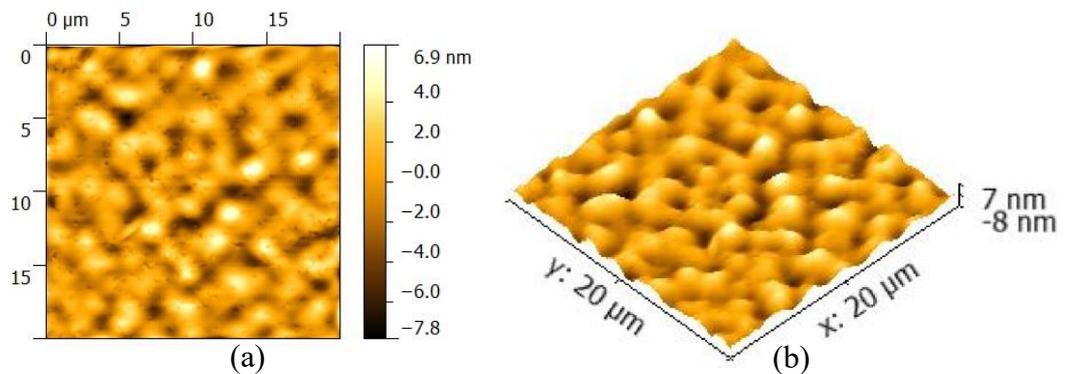


Figure 5.23: $20\mu\text{m} \times 20\mu\text{m}$ contact mode AFM micrograph of sample 13-165, reverse linearly graded to $\text{Si}_{0.283}\text{Ge}_{0.717}/\text{Ge}$. Threading dislocations can be seen from the scan. The estimated TDD from the AFM scan $\approx 2 \times 10^7 \text{cm}^{-2}$ which is lower than the value measured through Schimmel etching of the sample. $R_{\text{rms}}=2.42\text{nm}$

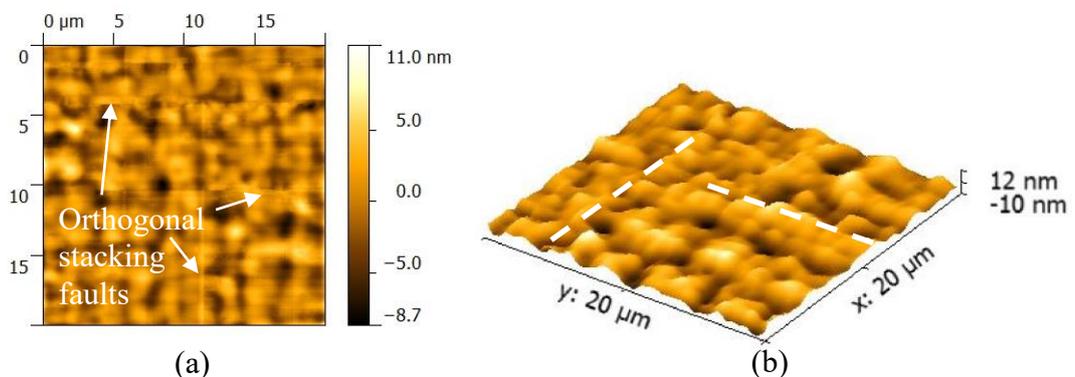


Figure 5.24: $20\mu\text{m} \times 20\mu\text{m}$ contact mode AFM micrograph of sample 13-134, reverse linearly graded to $\text{Si}_{0.55}\text{Ge}_{0.45}/\text{Ge}$. Stacking faults can be seen on the surface, indicated by the dashed white line in figure (b). $R_{\text{rms}}=3.7\text{nm}$.

5.4.2.2. Tilt and strain in $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers

When reverse grading between 71.7% Ge and 45% Ge on on-axis substrates, it is seen that the average tilt in Ge underlayer, $\text{Si}_{0.05}\text{Ge}_{0.95}$ layer and reverse graded $\text{Si}_{1-x}\text{Ge}_x$ layer are 0.006° , 0.002° and 0.005° respectively. This is within the margin of error for an on-axis substrate with a tolerance of $\pm 0.5^\circ$ hence it is concluded that negligible tilt is generated in each of the epilayers in a reverse graded heterostructure when reverse grading to between $x=0.717$ and $x=0.45$, as seen in figures 5.25 and 5.26, respectively. The $\text{Si}_{1-x}\text{Ge}_x$ peak in both 004 and 224 however is much broader for when $x=0.45$ than for when $x=0.717$. The reason for peak broadening is due to the rise in stacking faults which, due to their 2D nature, damages crystal uniformity in two axes and causes mosaicity in the two directions.

The average amount of strain in the LT/HT Ge underlayer for all of the samples remains consistent at $0.212\% \pm 0.014\%$ tensile strain which is approximately 105.45% relaxed with respect to the substrate. The strain in the $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace layer is $0.221\% \pm 0.019\%$ tensile strain, which falls within the error limit of the Ge underlayer so it can be said that there is negligible difference in strain between the $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace layer and the Ge underlayer. With all of the reverse graded $\text{Si}_{1-x}\text{Ge}_x$ layers an average strain of $0.2\% \pm 0.0173\%$ tensile strain exists which is also within the error limits of the Ge underlayer and the $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace layer. Therefore, it is said categorically that no variation in strain is observed in the heterostructure starting from the Ge epilayer, right through to the $\text{Si}_{1-x}\text{Ge}_x$ buffer layer for $0.45 \leq x \leq 0.717$ when grading below $30\% \text{Ge}/\mu\text{m} \pm 10\% \text{Ge}/\mu\text{m}$.

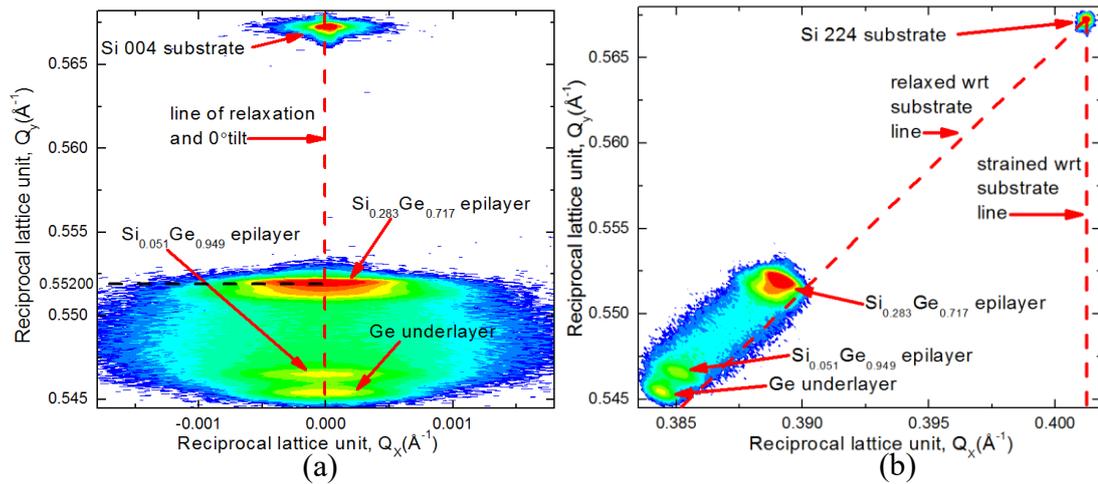


Figure 5.25: HR-XRD of sample 13-165, reverse linearly graded to $\text{Si}_{0.283}\text{Ge}_{0.717}$. Negligible tilt with respect to $\text{Si}(001)$ is observed in the epilayers. 0.006° , 0.002° and 0.005° tilt was measured in the Ge underlayer, $\text{Si}_{0.051}\text{Ge}_{0.949}$ epilayer and $\text{Si}_{0.283}\text{Ge}_{0.717}$ epilayer respectively.

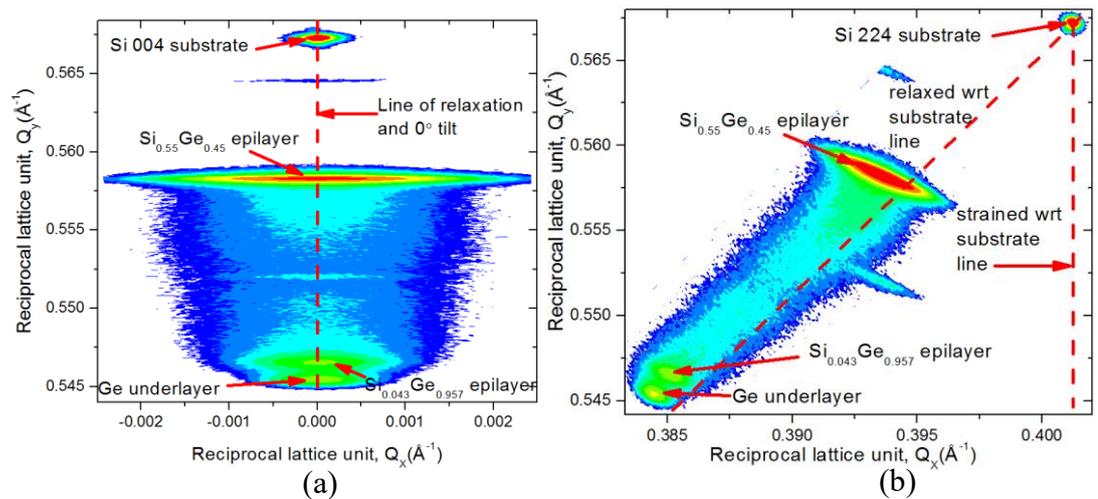


Figure 5.26: HR-XRD of sample 13-134, reverse linearly graded to $\text{Si}_{0.55}\text{Ge}_{0.45}$. 0° tilt in the Ge underlayer, $\text{Si}_{0.043}\text{Ge}_{0.957}$ and $\text{Si}_{0.55}\text{Ge}_{0.45}$ epilayers. Severe peak broadening in the $\text{Si}_{0.55}\text{Ge}_{0.45}$ layer is due to the rise in stacking faults.

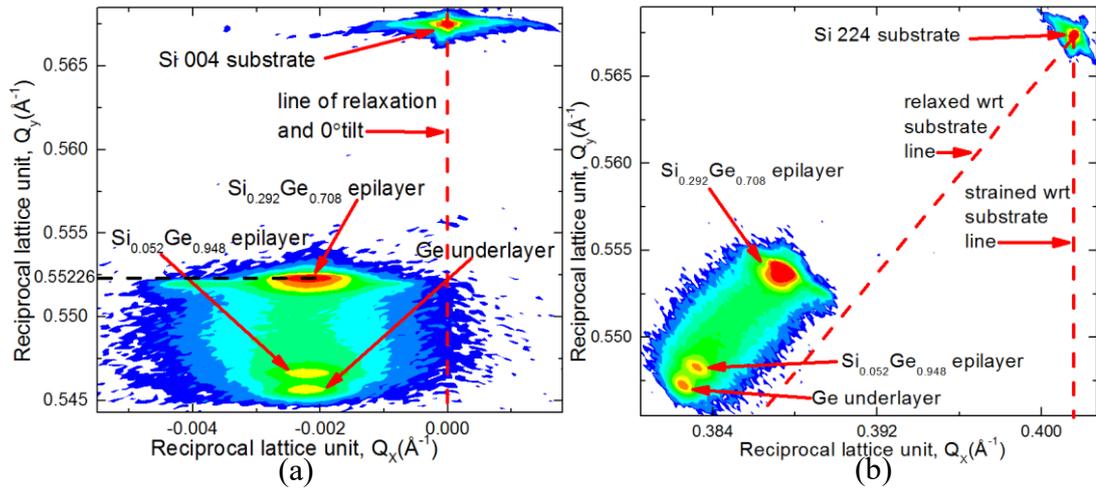


Figure 5.27: HR-XRD of sample 13-162, reverse linearly graded to $\text{Si}_{0.292}\text{Ge}_{0.708}$ on 6° off-axis Si(001). The measured tilt in the epilayers were as following: 0.231° in the Ge underlayer, 0.221° in the $\text{Si}_{0.052}\text{Ge}_{0.948}$ epilayer and 0.221° in the $\text{Si}_{0.292}\text{Ge}_{0.708}$ epilayer. Strain in the Ge underlayer was 0.24% and strain in the $\text{Si}_{0.292}\text{Ge}_{0.708}$ epilayer was 0.22%.

When growing a reverse linearly graded buffer layer on a 6° off-axis substrate the (004) reflection shows a degree of tilt in the entire heterostructure as is seen in figure 5.27. From the two samples grown on off-axis Si(001), the average tilt in the Ge underlayer is $0.226^\circ \pm 0.007^\circ$ and the average tilt in the reverse graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer is $0.231^\circ \pm 0.014^\circ$. The tilt in the off-axis grown Ge underlayer is assumed to be caused by the tilt component in the 60° and Lomer dislocations. The unequal stressing of the glide planes in off-axis substrates as described in chapter 2.5.10 means that dislocation annihilation and strain relaxation takes place asymmetrically. The uniform low grading rate and constant strain in the graded region means that only 60° misfit dislocations are generated and multiplication is not observed. It is also presumed that the vicinal steps and terraces are preserved into the entire heterostructure. These reasons provide a probable explanation as to why the $\text{Si}_{1-x}\text{Ge}_x$ layer is under the same amount of tilt as the Ge underlayer.

5.4.2.3. Defects

Tensile strain relaxation and low strain energy in the RLG buffer means that surface undulations do not have a propensity to form. Also, the 60° misfit dislocation readily dissociates in layers under tensile strain therefore cross-slip (dislocation moving from

a glide plane to another glide plane) is unlikely to occur. As a consequence, Frank-Read multiplication of dislocations that causes pile-up, is unlikely to occur in reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ layers. Figure 5.28 shows an example of the TDD distribution in a reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layer.

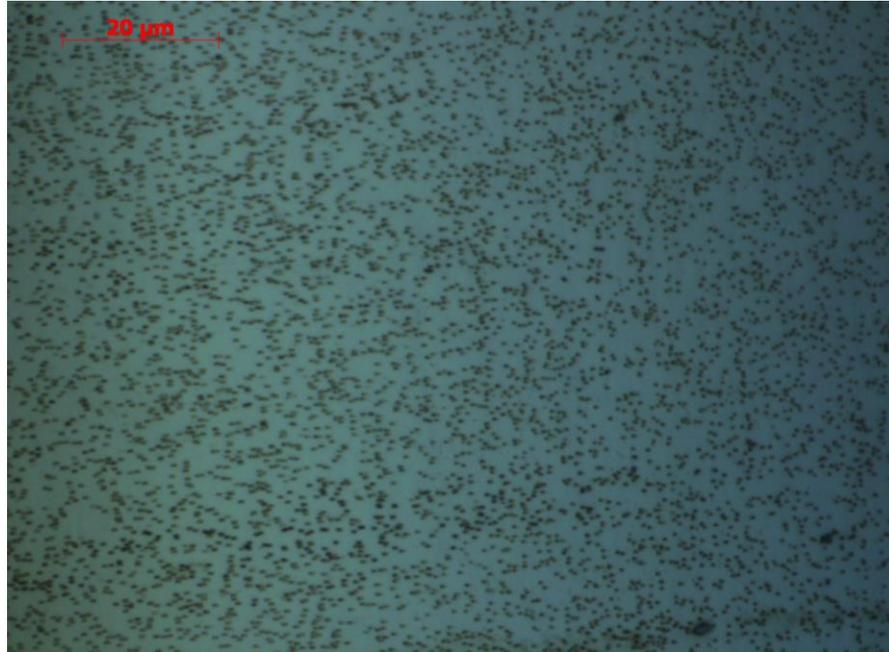


Figure 5.28: 2 min Schimmel etch and DIC optical microscopy of sample 13-165, reverse linearly graded $\text{Si}_{0.283}\text{Ge}_{0.717}/\text{Ge}$ buffer. Average TDD $\approx 5.29 (\pm 0.529) \times 10^7 \text{cm}^{-2}$. This image is an example of a reverse linearly graded buffer. As can be seen, pile-up of threading dislocations does not occur.

The 555nm thick LT/HT Ge underlayer has a TDD of approximately $2 \times 10^8 \text{cm}^{-2}$. This is the starting TDD value for the heterostructure. All of the reverse linearly graded samples have a TDD of less than $8 \times 10^7 \text{cm}^{-2}$ which means that some degree of annihilation has taken place across the $\text{Si}_{0.05}\text{Ge}_{0.95}/$ graded $\text{Si}_{1-x}\text{Ge}_x$ region. It is hypothesised that due to the low mismatch of 0.19% between the $\text{Si}_{0.05}\text{Ge}_{0.95}$ layer and the Ge underlayer 60° misfits are more likely to generated than any existing dislocations annihilated. This will undoubtedly raise the TDD. The grading rates for all of the samples are measured to be within the temperature limited glide regime [117], and so it is predicted that the graded region will provide strain assisted annihilation. This results in a lower TDD than the Ge underlayer but not one order of magnitude lower as was seen in the investigation by Shah et al [117] where the $\text{Si}_{0.25}\text{Ge}_{0.75}/\text{Ge}$ buffer layer drops in TDD to $6 \times 10^6 \text{cm}^{-2}$ from $2 \times 10^7 \text{cm}^{-2}$ i.e: in that

investigation 1 μm 400°C/650°C LT/HT Ge underlayer was used and the entire graded region was reverse linearly graded without the presence of an intermediate terrace.

As the buffer is reverse graded to a lower Ge%, the TDD density is noticed to reduce. This occurs in tandem with a rise in stacking faults, and is assumed to be generated via the dissociation of threading dislocations within the graded layer.

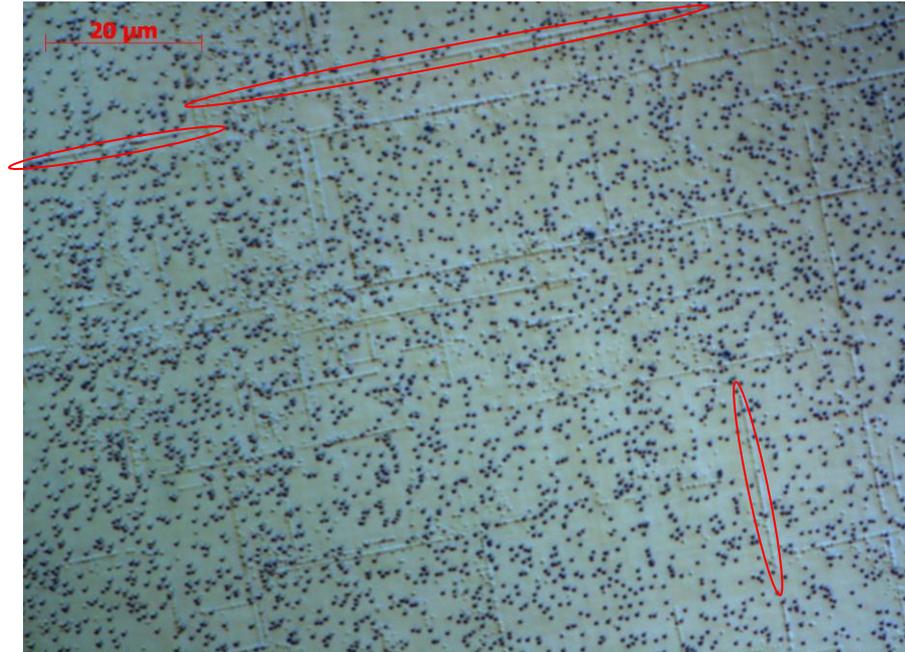


Figure 5.29: 2 min Schimmel etch and DIC optical microscope image of sample 13-134, reverse linearly graded $\text{Si}_{0.55}\text{Ge}_{0.45}/\text{Ge}$ buffer. Average TDD $\approx 3.53 (\pm 0.353) \times 10^7 \text{ cm}^{-2}$. The black dots are threading dislocations whilst the straight lines are stacking faults highlighted by the red ellipses.

As a final point it has also been observed, that reverse grading on off-axis substrates, marginally increases the TDD by $\times 1.4$. This is explained by the glide planes being stressed unequally in vicinal substrates, thus leading to reduced annihilation. Since it is presumed that the heavy step and terrace pattern is preserved in both the $\text{Si}_{0.05}\text{Ge}_{0.95}$ and $\text{Si}_{1-x}\text{Ge}_x$ layers, it is assumed that at each of the interfaces, larger networks of misfit dislocations are generated through multiplications which leads to a higher density of threading dislocations.

5.5. Comparisons between linear grading with reverse linear grading

5.5.1. Strain comparison between buffer grading techniques:

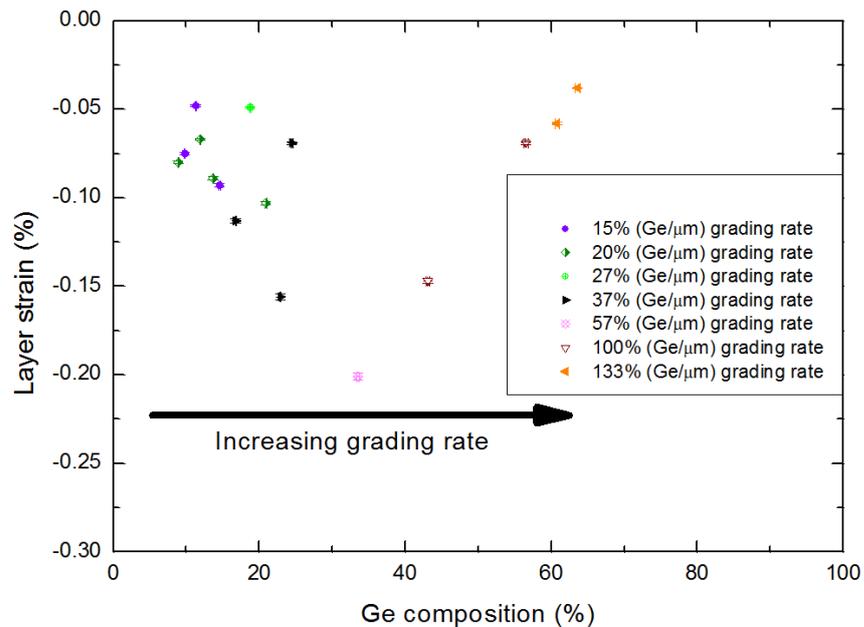


Figure 5.30: Ge composition (%) vs layer strain (%) in linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers

When examining strain variation in linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers grown at 850°C , both grading rate and Ge composition have influences. By comparing figures 5.30 and 5.31, it cannot be distinguished whether grading rate or Ge composition has the larger influence on layer strain. Increasing the grading rate between 15 to $57\% \text{ Ge}/\mu\text{m}$ has the effect of increasing the strain almost linearly to reach a maximum of 0.2% compressive strain with a $57\% \text{ Ge}/\mu\text{m}$ grading rate. This can be explained by the low lattice and thermal mismatch between low Ge composition SiGe layers with Si(001) which generates a high density of 60° misfit dislocations at the interface which leads to greater strain relaxation. By increasing the grading rate, there is a greater compositional jump between atomic layers and therefore not enough strain relaxation takes place. Increasing the grading rate beyond $60\% \text{ Ge}/\mu\text{m}$ sees the reduction of strain through the over generation of surface undulations, misfit dislocations and stacking faults.

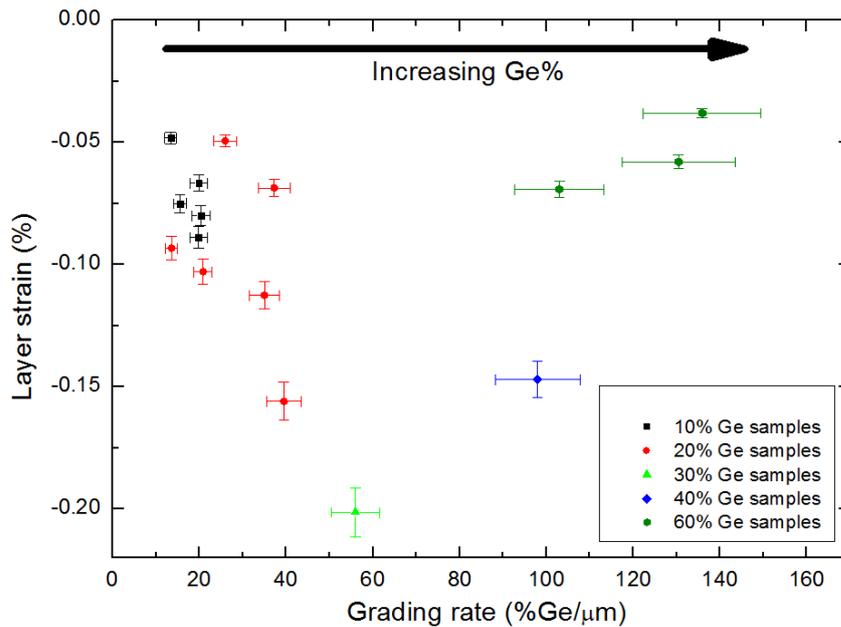


Figure 5.31: Grading rate %Ge/ μm vs layer strain (%) in linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers.

Comparatively in the reverse linear grading process, 0.2% tensile strain is maintained through each epilayer in the heterostructures even when reverse grading to 45% Ge from pure Ge, as seen in figure 5.32. This is reasoned by the fact that 0.2% tensile strain is already present in the Ge underlayer due to thermal mismatch. Therefore, the in-plane lattice constant of the Ge underlayer is slightly higher than its bulk crystal value and so for example the $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace layer is under more tensile strain than it would experience if it were grown on a relaxed Ge(001) wafer. The 0.2% tensile strain is the starting point if you will. All subsequent epilayers experience a deviation in strain from this value. If the grading rate is kept below approximately 100%Ge/ μm [117], therefore the change in lattice parameters per atomic layer is not so drastic and 2D Frank van der Merwe growth takes places, hence the 0.2% tensile strain is maintained. It cannot be said for certain how the strain will continue to progress as the layer is reverse graded all the way back to pure silicon, at less than 30%Ge/ μm growth rate and so should be a point of further investigation.

Finally, it has also been observed that whilst the LT/HT Ge underlayer is over relaxed and therefore is not lattice matched to GaAs at room temperature, the 0.2% tensile strained $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace in all of the samples however has an in-plane lattice constant that is lattice matched to GaAs, and so could be used as a better buffer layer.

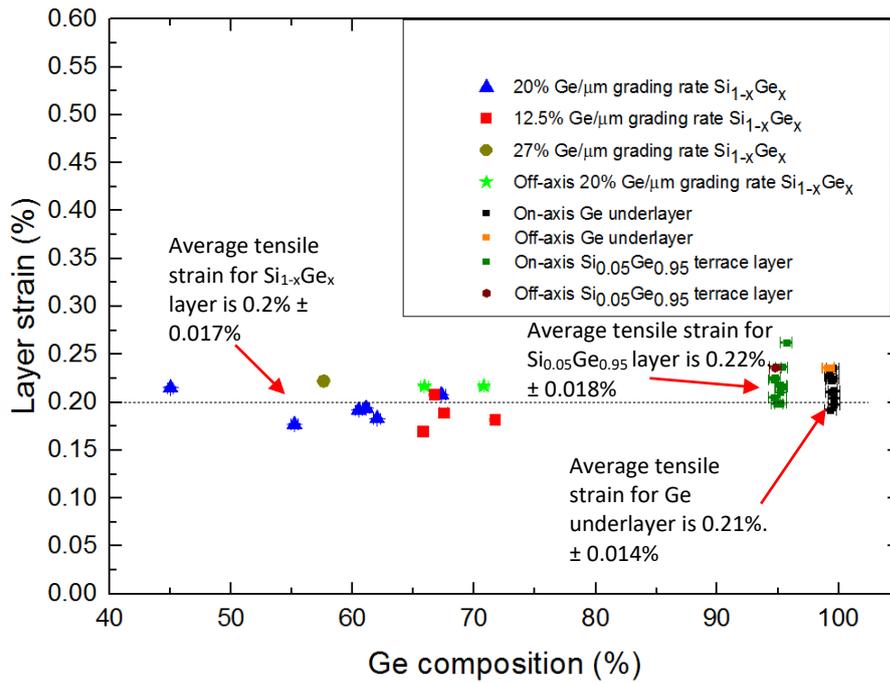


Figure 5.32: Grading rate %Ge/ μm vs layer strain (%) in reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers.

5.5.2. Surface morphology

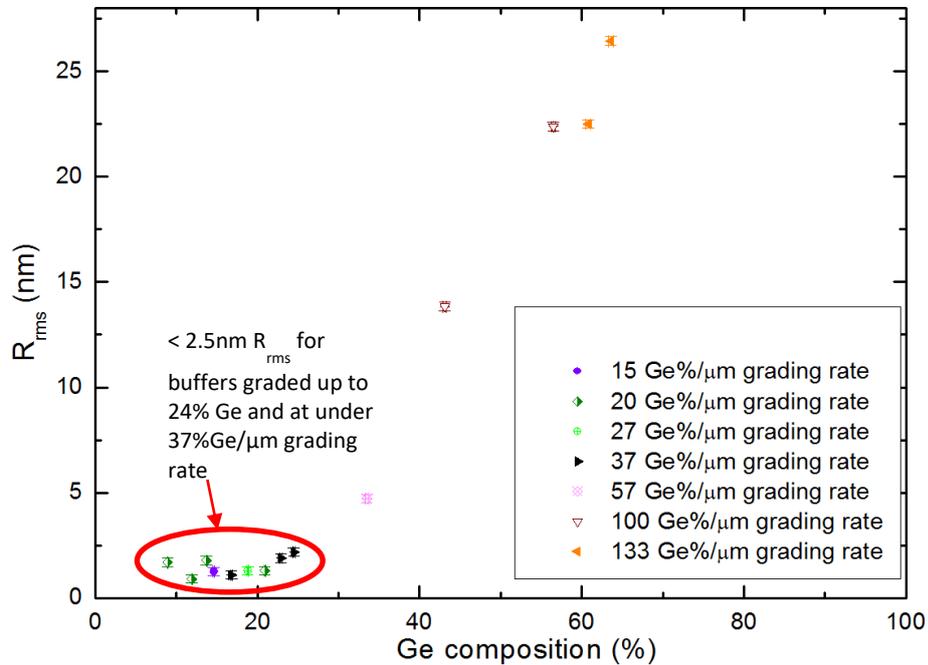


Figure 5.33: Ge composition vs R_{rms} for linearly graded $\text{Si}_{1-x}\text{Ge}_x$ at various grading rates

For linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers, the surface roughness is under 4nm when the grading rate is kept below 40% Ge/ μm as shown in figure 5.33. Previous literature

has shown that severe pile-up and cross-hatching takes places after the buffer layer has been graded to 30% even with an optimum grading rate of 10% Ge/ μm which requires the use of CMP when 50% Ge has been reached [116]. An escalation in surface roughness is seen when linearly grading at a grading rate higher than 56% Ge/ μm .

Shah et al proved that less than 3nm roughness is obtainable for reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ samples reverse graded below 61% Ge/ μm for between $0.75 \leq x \leq 1$. In this investigation it has been shown that less than 4nm roughness can be obtained through tensile strain relaxation even when reverse grading to 45% Ge at below 30% Ge/ μm grading rate. The marginally high rise in roughness to 3.7nm is attributed to the rise of stacking faults on a planar surface. It is unknown how the surface morphology will change when reverse grading to even lower contents of Ge, i.e. perhaps back to pure silicon. The buffer layer will undoubtedly be thicker if doing so, since the reverse graded region will also be thicker.

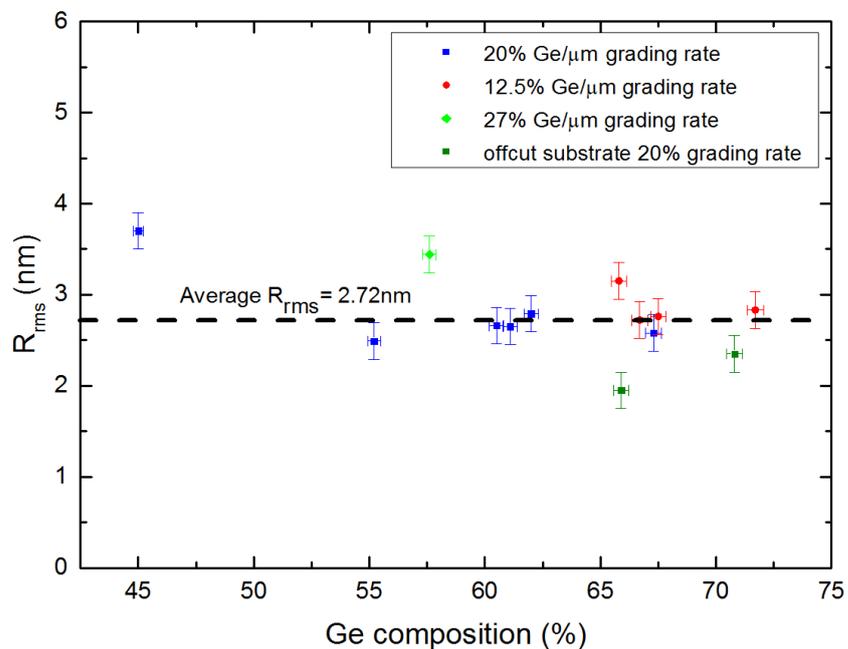


Figure 5.34: Ge composition vs R_{rms} for reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ at various grading rates

5.5.3. Defect comparison

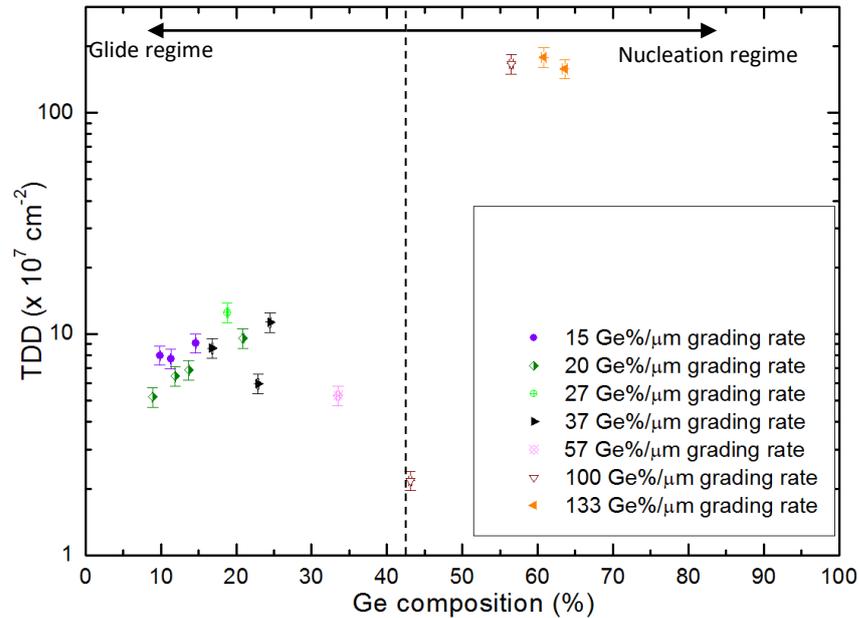


Figure 5.35: Plot showing Ge composition (%) vs TDD of linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers graded at various grading rates.

Low lattice mismatch in linear graded buffers means that 60° misfit dislocations are generated which readily glide along the $\{111\}$ planes. For samples graded below $37\% \text{Ge}/\mu\text{m}$, TDD appears to slowly rise with increasing Ge content as seen in figure 5.35. This is explained by a greater density of misfits generated in the graded region. When the grading rate is increased further to $100\% \text{Ge}/\mu\text{m}$, the TDD is shown to drop to its lowest point as seen in both figures 5.35 and 5.36. This means that at $100\% \text{Ge}/\mu\text{m}$ the graded region is at its maximum point in the glide regime but as seen in figure 5.33 the surface roughness of such a grading rate is 13.83nm which suggests that at this strain (0.15% compressive from figure 5.31) and grading rate high misfit dislocations are being created but are simultaneously being annihilated by anti-Burger's vector loops.

When compared to reverse linearly graded samples, it is seen that the TDD in the layers decays with reducing Ge content from $x=0.717$ to $x=0.45$ as seen in figure 5.37. The grading rates for all of the reverse graded samples are below $30\% \text{Ge}/\mu\text{m}$ therefore they are within the temperature limited glide regime [117]. The decay in TDD is seen with a complimentary rise in stacking fault as shown in figure 5.38.

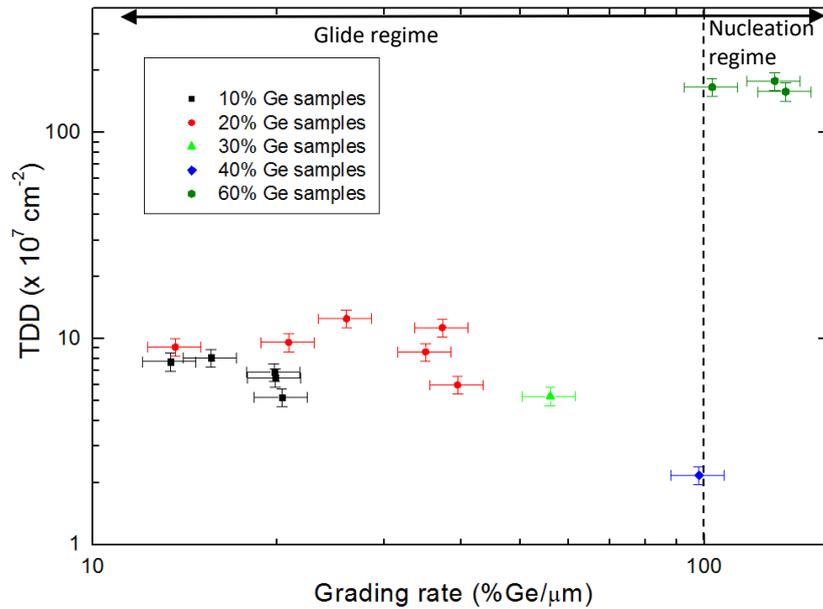


Figure 5.36: Plot showing grading rate vs TDD of linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers graded to various compositions of Ge.

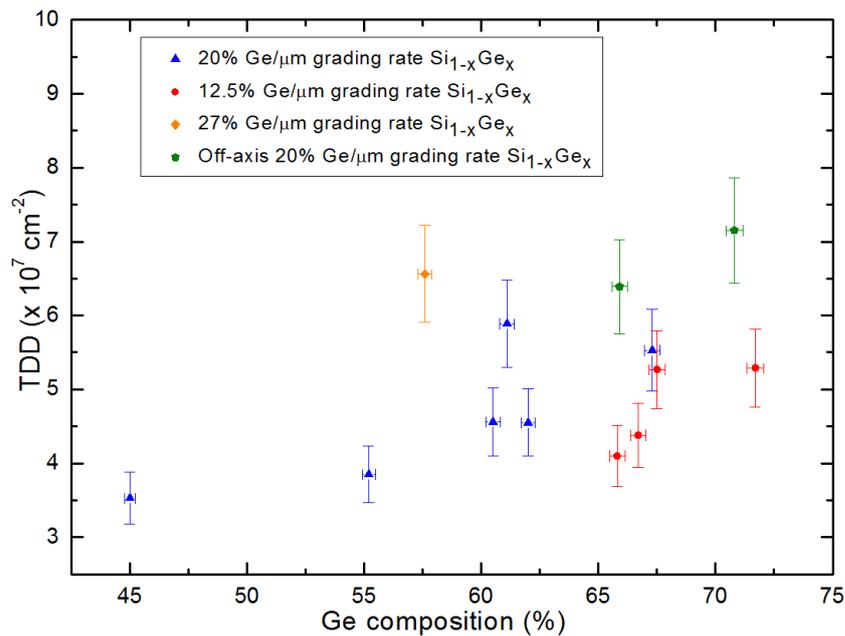


Figure 5.37: Plot showing grading rate vs TDD of reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers graded to various compositions of Ge.

The stacking fault line density is measured as number of fault lines per cm along orthogonal $\langle 110 \rangle$ directions and then averaged along the two axes. Figure 5.38 is a logarithmic plot showing the stacking fault density relationship with Ge composition.

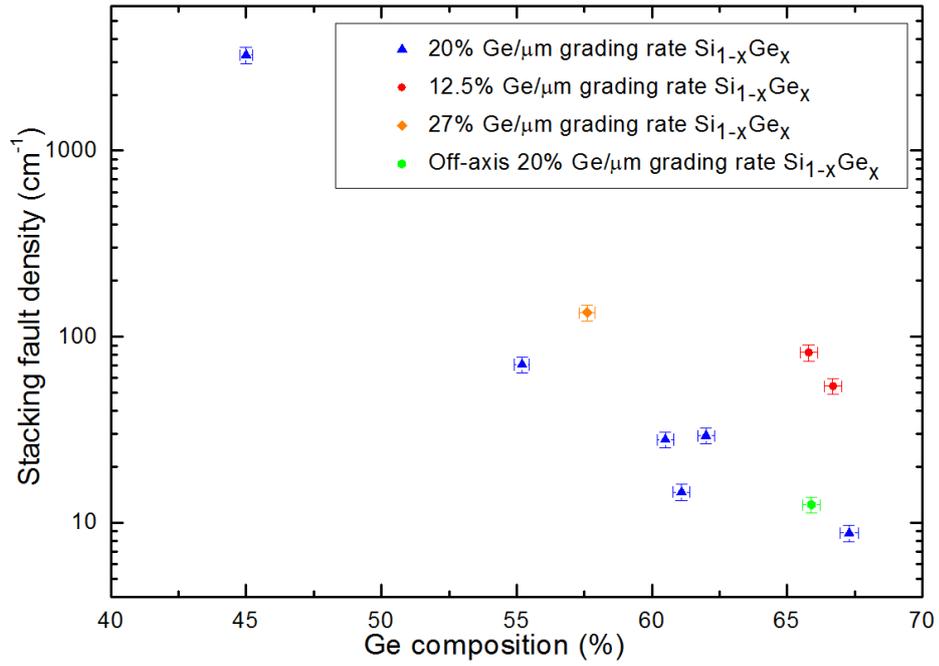


Figure 5.38: Plot showing grading rate vs stacking fault density of reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers graded to various compositions of Ge.

Equation 2.39 is used to calculate the relaxation of the layer by stacking faults. The maximum line density of stacking faults is 3272 cm^{-1} which was observed for sample 13-134 ($\text{Si}_{0.55}\text{Ge}_{0.45}$). The line density is measured over two of the $\{111\}$ planes, therefore, for the $(\bar{1}\bar{1}\bar{1})$ glide plane the total line density is 1636 cm^{-1} . As there are 4 $\{111\}$ glide planes each with 3 $\langle 110 \rangle$ slip directions. The $[110]$ direction is a screw direction, therefore the edge slip directions are: $[10\bar{1}]$ and $[011]$ with $\underline{n}_{\text{dir}}$: $[\bar{1}01]$ and $[0\bar{1}1]$ respectively and b_{eff} for a 90° partial dislocation ($b_{90^\circ} = \frac{a}{6}[-1\ 12]$): $\frac{a}{2\sqrt{2}}$ and $\frac{a}{6\sqrt{2}}$ respectively. Therefore, for the $(\bar{1}\bar{1}\bar{1})$ glide plane the relaxation is $0.20\% \pm 0.1\%$. The measured relaxation of the reverse graded $\text{Si}_{0.55}\text{Ge}_{0.45}$ epilayer is 112.45% and so 0.20% of that relaxation comes from stacking faults on the $(\bar{1}\bar{1}\bar{1})$ glide plane. The increase in relaxation is also brought about through cracks which shall be discussed later on.

5.5.4. Growth rate and etch rate variations

When plotting the growth rates of the linearly graded and reverse linearly graded constant composition regions with respect to Ge composition, it was discovered that a growth rate variation is observed as shown in figure 5.39. Reverse graded buffer layers were noticed to grow faster than linearly graded buffer layers. This is hypothesised to be due to tensile strain relaxation which creates much smoother surfaces, free of undulations. As a consequence, terraces on the growing epilayer surface in reverse graded samples are parallel to the (001) surface and so adatom drift and adsorption on the surface, as explained by Hudson in figure 2.25 [69], is easier than on a surface with a changing surface plane as is the case with linearly graded buffers which are quite rough. This is why in figure 5.19, the constant composition $\text{Si}_{0.55}\text{Ge}_{0.45}$ layer in the reverse graded structure was so unnecessarily thick; because the growth rate was expected to be similar to the growth rate for a linearly graded $\text{Si}_{0.55}\text{Ge}_{0.45}$ buffer layer.

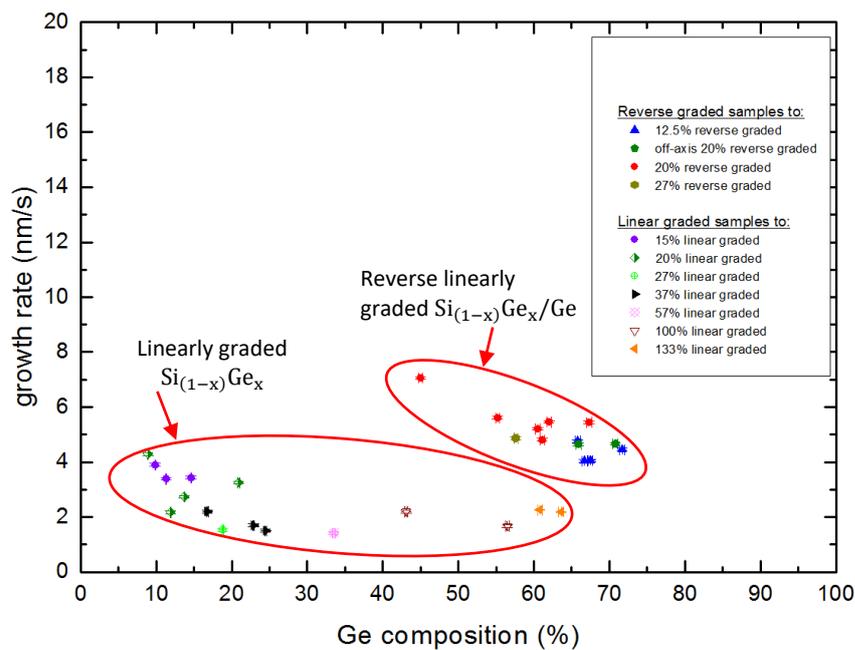


Figure 5.39: Plot showing Ge composition vs growth rate of linearly graded $\text{Si}_{1-x}\text{Ge}_x$ and reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers using RP-CVD at 850°C .

Using the wax and Schimmel etching method described in section 3.5.1.1, the etch rates of the linearly graded and reverse linearly graded samples were calculated and plotted against composition. A complete range of linearly graded $\text{Si}_{1-x}\text{Ge}_x$ and reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ samples was not available i.e.: from $x=1$ to $x=0$ for each grading technique and so a full comparison could not be made. However, when plotting the etch rates from the available samples from this study and comparing them

to figure 3.18 (a) in the work carried out by J. Parsons [136], a similar trend is seen. The etch rates from this study are slower than those reported by J. Parsons because 100ml more de-ionised water was used which slows down the etch reactivity, and so the highest etch rate in that investigation was observed for $\text{Si}_{0.82}\text{Ge}_{0.18}$ at 23.5nm/s, whereas the highest etch rate in this investigation was for $\text{Si}_{0.791}\text{Ge}_{0.209}$ at 9.18nm/s. From the plot in figure 5.40, the predicted highest etch point is at approximately $\text{Si}_{0.78}\text{Ge}_{0.22}$. What is clear from the plot is that when combining available etch rates for linearly graded and reverse linearly graded samples and fitting curves against the data points, it seems that there is no discernible difference in etch rates. The Schimmel etch rate is known to vary with temperature, strain and de-ionised water concentration [162], since the samples were not reverse graded across the whole Ge content range i.e.: back to pure silicon, it cannot be said with any certainty if tensile strain in the layers effects etch rate and therefore generates a different etch curve to compressively strained $\text{Si}_{1-x}\text{Ge}_x$. A second fitting curve, in green, is plotted for just the RLG samples in figure 5.40 which shows that tensile strain in the RLG samples has indeed effected etch rate. It is recommended that the reverse graded buffer be graded back to pure silicon (at below 30%Ge/ μm grading rate) to see how the etch truly varies with respect to Ge content.

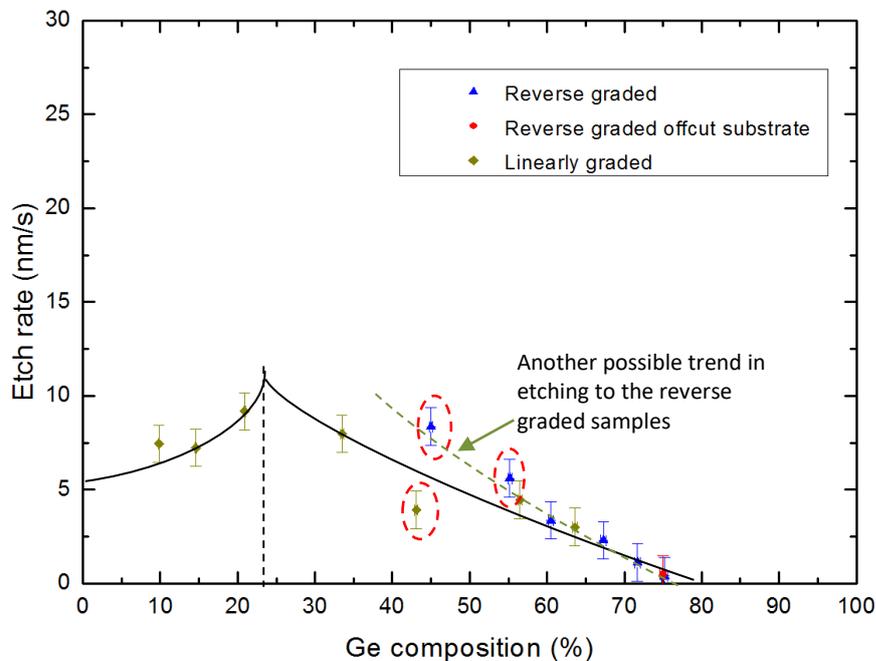


Figure 5.40: Plot showing Ge composition vs etch rate of linearly graded $\text{Si}_{1-x}\text{Ge}_x$ and reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers using Schimmel etch at 20°C in an evacuated fume cupboard. The points in red dashed circles are outside of the experimental error and so are not included in the fitting curves. A second (green) curve is plotted with against all of the reverse linear graded samples.

5.5.5. Crack generation

Cracking in reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers is a problem and the previous works have shown that cracking during the cleaving process can be limited for $\text{Si}_{0.2}\text{Ge}_{0.8}/\text{Ge}$ if the total thickness is limited to $2.7\mu\text{m}$ [117]. In this investigation, the buffer layers range in thickness from $5.172\mu\text{m}$ to $7.584\mu\text{m}$ but the Ge content is between $0.45 \leq x \leq 0.717$. The as grown crack density, prior to cleaving the wafer, was not measured and therefore it cannot be said with any degree of certainty if cracks were created through the growth of the heterostructure.

Figure 5.41 is an X-TEM image of sample 13-165. Due to the difficulty in capturing a crack in a cross-sectional image, to measure dimensions, this sample was taken as the standard to determine penetration depth to epilayer thickness ratio, d/h . The line density of cracks was taken after etching the sample in Schimmel etchant and then imaging the sample using DIC optical microscopy and counting the number of cracks. The relaxation of the reverse graded buffer layers due to cracks was then calculated using equation 2.70. Figure 5.42 is a typical DIC optical image of a reverse graded buffer than has been etched to widen the crack widths and make more visible.

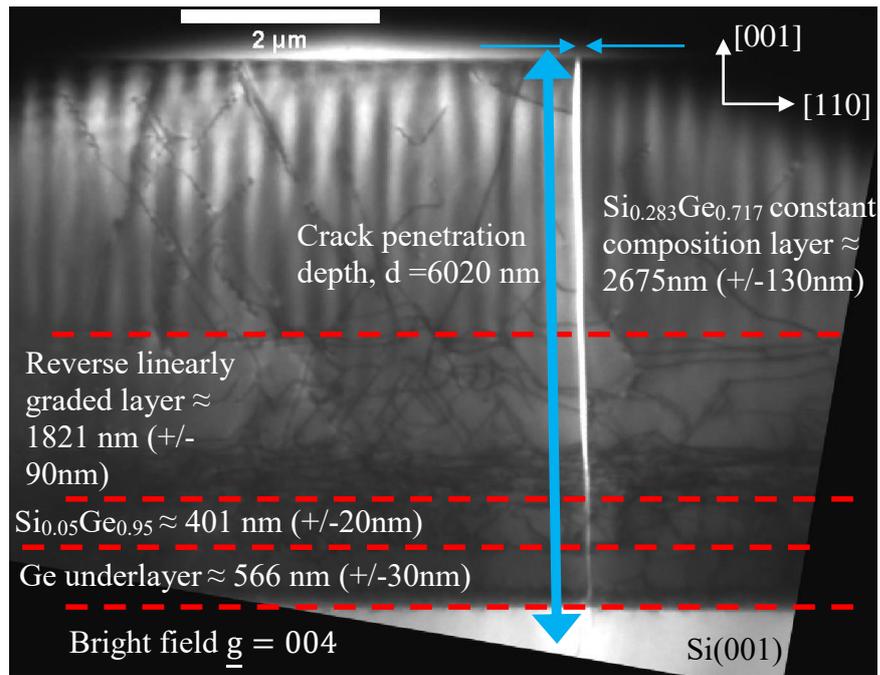


Figure 5.41: X-TEM of sample 13-165, reverse linearly graded to $\text{Si}_{0.283}\text{Ge}_{0.717}$. Buffer layer total thickness, h , is $5535\text{nm} \pm 15\text{nm}$ with a grading rate of $12.72\% \text{Ge}/\mu\text{m} \pm 10\%$. The relaxation of the Ge underlayer is 104.95% with respect to the substrate and the $\text{Si}_{0.283}\text{Ge}_{0.717}$ layer with respect to the substrate is 106.48% . The crack penetration depth, d , is measured to be $6.02\mu\text{m}$. The crack width, w , is measured to be $0.0617\mu\text{m}$.



Figure 5.42: 2 min Schimmel etch and DIC optical microscope image of sample 13-165, reverse linearly graded to $\text{Si}_{0.283}\text{Ge}_{0.717}/\text{Ge}$ showing cracks. The crack line density for this sample, $\rho_{\text{CD}} = 90.83 \text{ cm}^{-1}$. The distance between cracks varies and at the lowest possible magnification ($\times 20$) the number of cracks in two directions, perpendicular to each other, was counted over a measured distance.

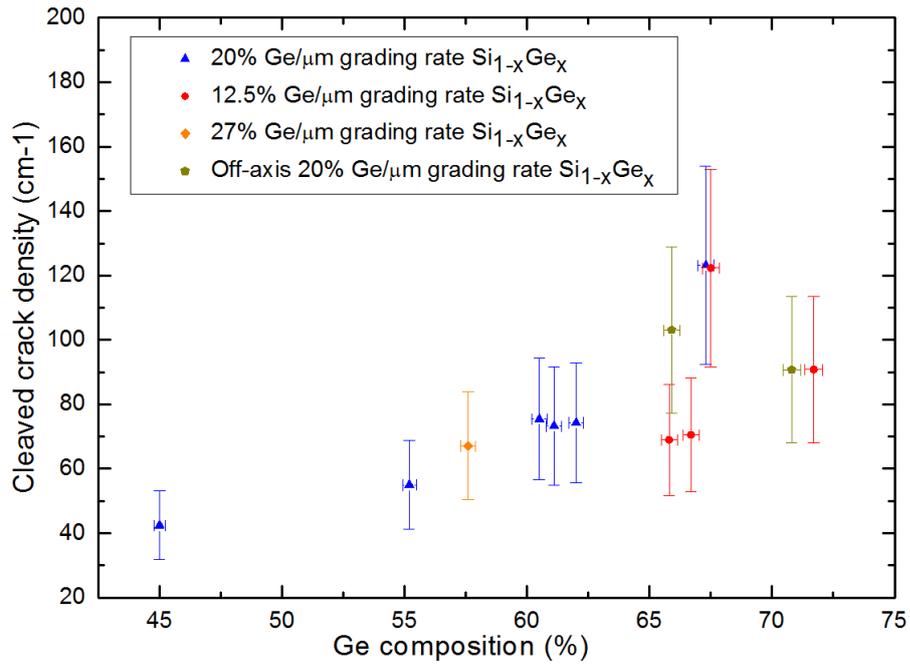


Figure 5.43: Plot of Ge composition (%) vs cleaved crack density for $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers. A trend is seen where the cleaved crack density reduces with reducing Ge content.

Figure 5.43 shows how the cleaved crack density reduces as a function of Ge content. This is suspected to be because the Young's modulus difference between the $\text{Si}_{1-x}\text{Ge}_x$ epilayer and the Si(001) substrate is reduced by having higher silicon content epilayers. The relaxation from cracks is also shown to drop as the Ge content is reduced in the layer.

5.6. Reverse step graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer design

The final investigation in the $\text{Si}_{1-x}\text{Ge}_x$ grading techniques investigation is on $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ step graded (RSG) buffer layers. This type of buffer layer is similar to the reverse linearly graded structure, however rather than gradually changing the Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ layer, a constant composition layer is deposited on the Ge buffer layer. This type of structure was investigated as a means to eliminate the reverse graded layer whilst taking advantage of the benefits of tensile strain relaxation.

$\text{Si}_{0.05}\text{Ge}_{0.95}$		00:02:00
LT/HT Ge	930nm	
p-Si(001)		

Figure 5.45: Schematic no. 1 of the reverse step graded buffer structure graded to $\text{Si}_{0.1}\text{Ge}_{0.9}$. The LT Ge was grown at 350°C and the HT Ge was grown at 550°C using GeH_4 . The step graded layer was created by adjusting $F(\text{SiCl}_2\text{H}_2)$ whilst keeping the flowrate of GeH_4 constant so as to solve equation 2.45 for $x=0.9$.

$\text{Si}_{1-x}\text{Ge}_x$		00:03:00
LT/HT Ge	930nm	
p-Si(001)		

Figure 5.46: Schematic no. 2 of the reverse step graded buffer structure. The buffer growth conditions are identical as with schematic no. 1, however the $\text{Si}_{1-x}\text{Ge}_x$ layer is grown for 3 minutes therefore based on figure 5.39, it is assumed that the step layers with lower Ge content will have a faster growth rate and therefore thicker layers. In the $\text{Si}_{1-x}\text{Ge}_x$ layer, x is calculated to be between 0.95 and 0.55 from equation 2.45.

The HT/LT Ge underlayer used in this investigation is slightly thicker at 930nm +/- 4nm as opposed to the 555nm thick underlayer used in section 5.4 on RLG buffer layers. The LT layer was grown at 350°C to 95nm and the HT layer was grown at 550°C to 835nm. This was done so as to reduce the TDD and since the reverse graded region was being omitted it was therefore deemed permissible to allow the Ge underlayer to be grown thicker. Figure 5.47 is a table of all of the samples in this investigation. As was the case with the Ge underlayer in RLG investigation, the Ge underlayer in this investigation was not annealed to prevent excessive thermal budget being supplied to the layer and causing too much tensile strain in the layer.

Sample number	Intended Ge composition ($\pm 0.5\%$)	Actual Ge composition ($\pm 0.5\%$)	Actual Ge composition ($\pm 0.5\%$)	Total thickness of buffer layer (nm)
15-72	1			930 (± 4 nm)
15-73	0.90			1108 (± 5.5 nm)
15-74	0.72	0.7	0.79	1560(max)- 1303(min)
15-75	0.55	0.47	0.79	1674(max) – 1560(min)
15-76	> 0.8	0.54	0.78	1667(max) – 1522(min)
15-77	> 0.8	0.83	0.84	1388 (max) - 1070(min)
15-78	> 0.8	0.78	0.82	1370(max) – 1291(min)

Figure 5.47: List of samples of reverse step graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers. As will be seen in the results section, reverse step grading to lower Ge content layers has the effect of creating two separate layers.

The growth temperature of the $\text{Si}_{1-x}\text{Ge}_x$ layer was kept fixed at 850°C . The flow rates and pressures that were used in the RSG buffer growth were identical to the RLG buffer layers, with the only difference being that SiCl_2H_2 flow rate in the reverse graded $\text{Si}_{1-x}\text{Ge}_x$ was not ramped but was instantaneously increased to a set flow rate to achieve the desired composition.

5.6.1. Buffer quality variation with reducing Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ step.

5.6.1.1. Sample 15-72: Ge underlayer

Figure 5.48 shows TEM images of the Ge underlayer as a cross section in (a) and in plan view in (b). 0.92nm roughness was measured using contact mode.

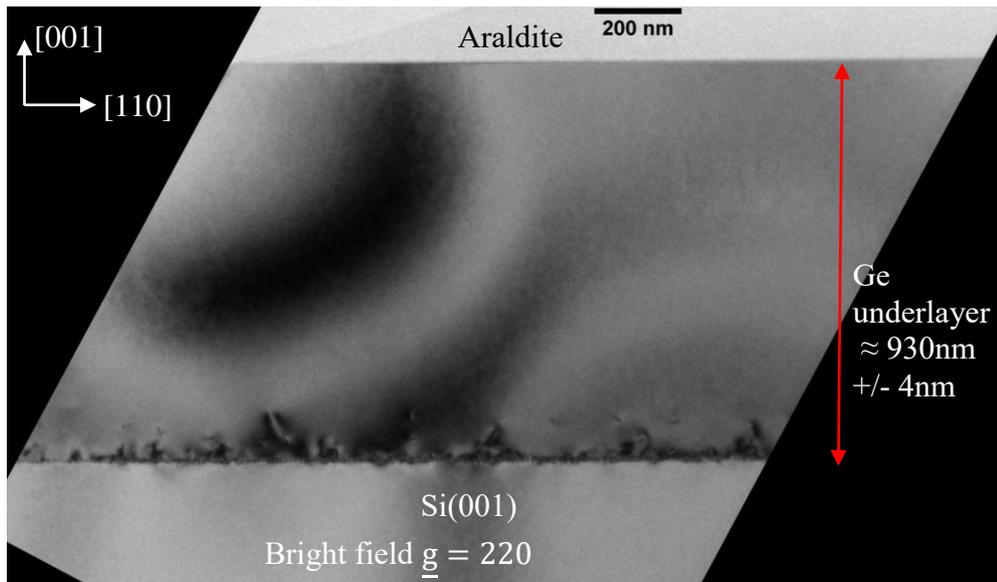


Figure 5.48: X-TEM of sample 15-72: 930nm LT/HT Ge buffer layer Average TDD = $6.19 \times 10^7 \text{ cm}^{-2} \pm 10\%$. $R_{\text{rms}} = 0.92 \text{ nm}$. The cross-sectional image shows the Ge buffer layer to be of very high crystalline quality.

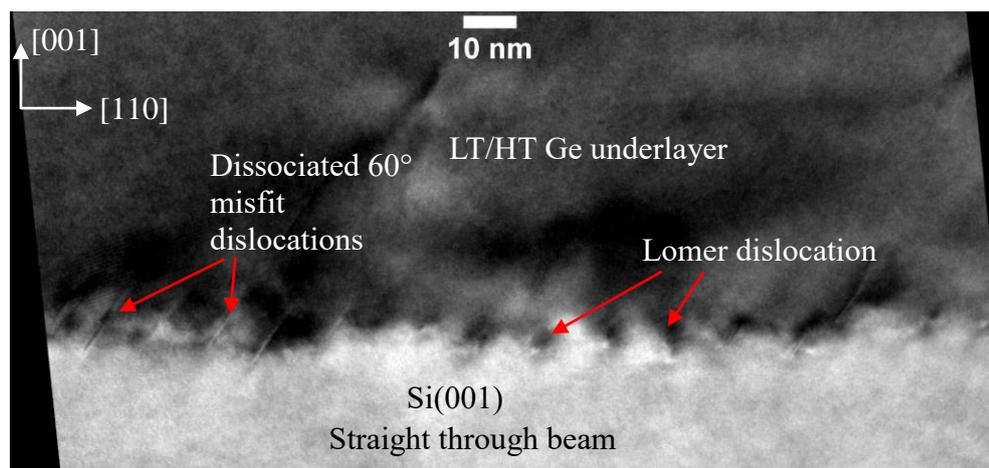


Figure 5.49: TEM of sample 15-72 at the interface between the Ge epilayer and Si(001) substrate. Stacking faults can be seen at the interface; presumably from the 350°C layer and Lomer dislocations. The interface between the 550°C and 350°C layers cannot be distinguished.

XTEM shows that dissociated 60° misfit dislocations at the interface which then recombine to form perfect Lomer misfits at the interface between the substrate and the Ge underlayer as seen in figure 5.49. The HT layer cannot be distinguished from the LT layer. Lomer dislocations with $[110]$ line direction can be seen at the interface, which are magnified in figure 5.50. The average distance between Lomer dislocations is measured to be approximately $11\text{nm} \pm 1.5\text{nm}$ which agrees with the Stillinger-Weber potential model investigation by Ichimura and Narayan on the Ge/Si(001) interface where the calculated distance achieve full strain relaxation in the Ge layer is $\frac{25a_{\text{Si}}}{\sqrt{2}} = 9.6\text{nm}$ [163].

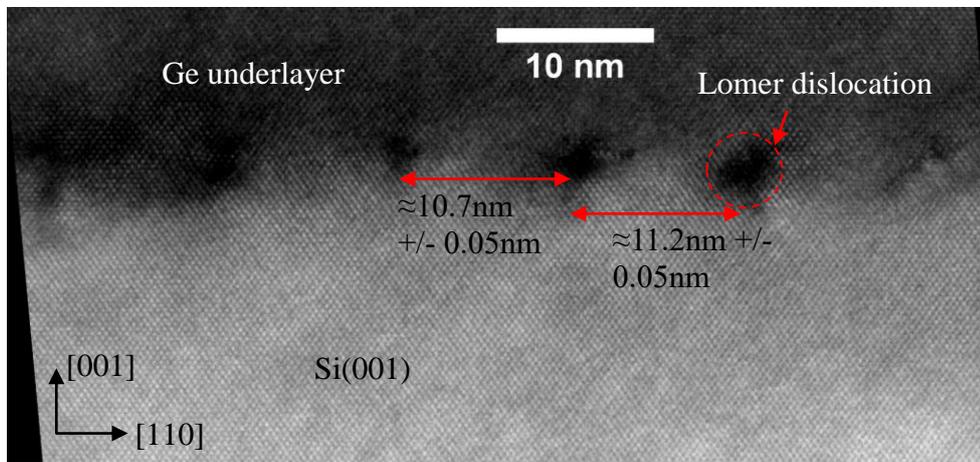


Figure 5.50: HR-XTEM of sample 15-72 at lattice resolution. The distance measured in the image between Lomer dislocations is approximately $11\text{nm} \pm 0.05\text{nm}$.

Figure 5.51 is of the 004 and 224 RSMs of the buffer layer. When compared to the RSM of sample 15-61 as shown in figure 4.20, the Ge peak in figure 5.51 is much narrower and in the 224 reflection, the peak has shifted further to the left of the relaxation line with respect to the substrate. The narrowness of the peak indicates that there are fewer defects but the shift left of the relaxation line indicates more tensile strain than with sample 15-61. Figure 5.52 is a sample plan view TEM image of the 930nm Ge underlayer. The TDD in the layer was measured as $6.19 \times 10^7 \text{cm}^{-2}$.

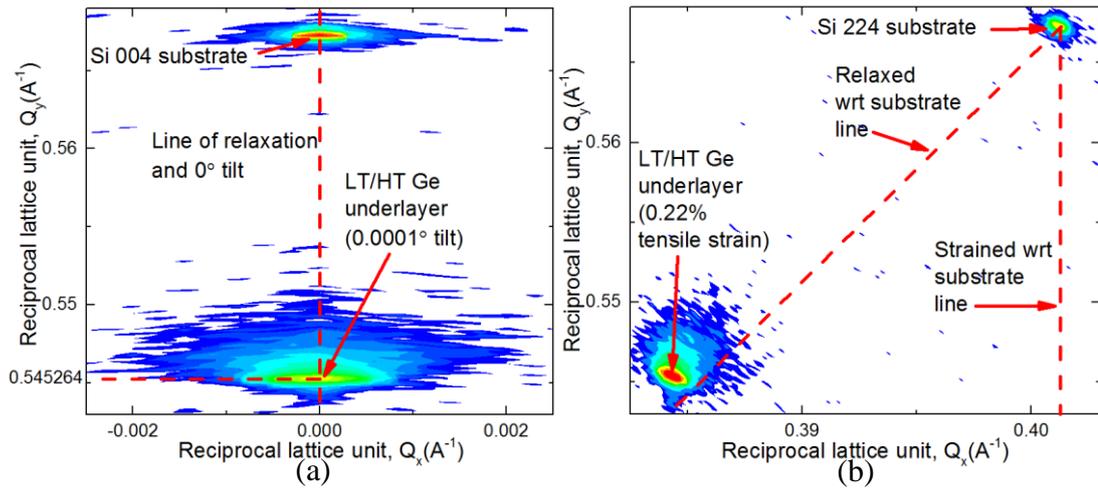


Figure 5.51: 004 and 224 HR-XRD RSM of sample 15-72: 930nm LT/HT Ge buffer layer. The strain in the layer is 0.22% tensile strain. The sharp Ge peak indicates low defect density in the layer.

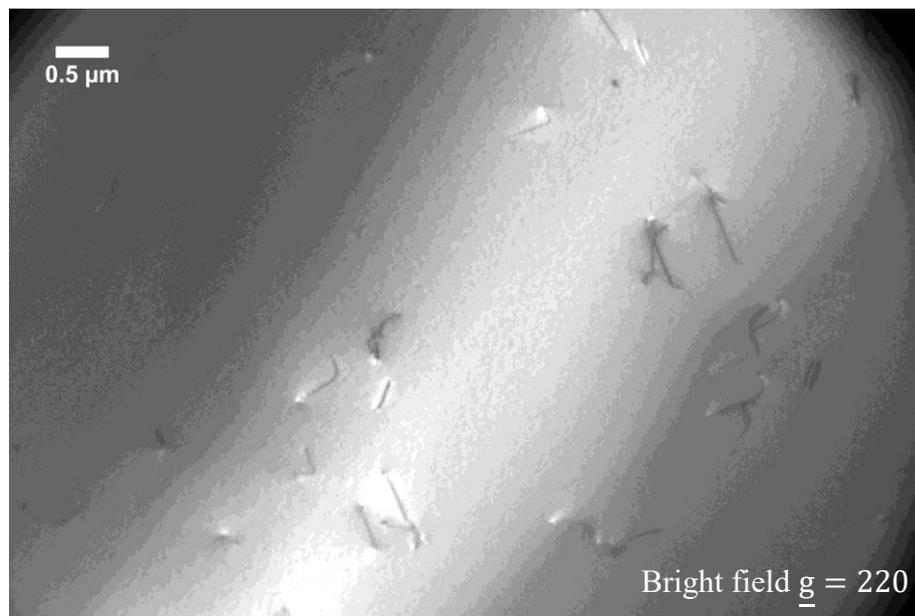


Figure 5.52: Plan view TEM of sample 15-72 930nm LT/HT Ge underlayer. A typical threading dislocation length is shown.

5.6.2. Reverse step graded (RSG) $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ structures.

5.6.2.1. Sample 15-73: RSG $\text{Si}_{0.1}\text{Ge}_{0.9}/\text{Ge}$ buffer layer

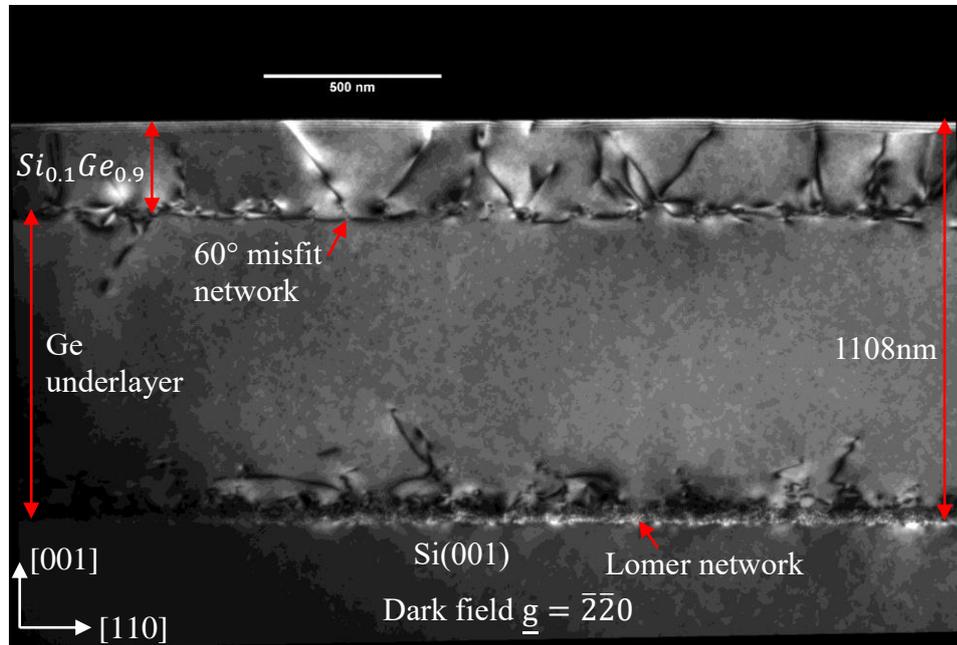


Figure 5.53: X-TEM of sample 15-73 RSG $\text{Si}_{0.1}\text{Ge}_{0.9}/\text{Ge}$ buffer layer. The total thickness of the structure = 1108nm \pm 5nm. The thickness of the $\text{Si}_{0.1}\text{Ge}_{0.9}$ buffer layer is estimated from 004 diffraction image as 228nm \pm 20nm.

The thickness of the total $\text{Si}_{0.1}\text{Ge}_{0.9}/\text{Ge}$ layer is 1108nm \pm 5nm measured in the 004 condition. The estimated thickness of the $\text{Si}_{0.1}\text{Ge}_{0.9}$ layer is approximately 228nm \pm 20nm (measured to the 60° misfit network from the 004 diffraction condition). However, given that the total structure is 1108nm \pm 5nm and the Ge underlayer is 930nm \pm 5nm, this would suggest that the $\text{Si}_{0.1}\text{Ge}_{0.9}$ should be 178nm however it is 50nm thicker than this. This possibly suggests some inter-mixing at the Ge/SiGe interface, however this has not been corroborated with SIMS.

When depositing a constant composition $\text{Si}_{0.1}\text{Ge}_{0.9}$ layer on the Ge buffer layer, 60° misfit dislocations are generated due to the -0.62% lattice mismatch between the Ge buffer layer and the $\text{Si}_{0.1}\text{Ge}_{0.9}$ step layer. Contact mode AFM shows that the surface roughness increases to 2.53nm from 0.92nm in the Ge underlayer as shown in figure 5.54, due partly to the heavy density of threading dislocations on the surface as well. The alloy composition is only 10% silicon and so its mechanical properties are going

to be based more on Ge than silicon. HR-XRD in figure 5.56 shows that the $\text{Si}_{0.1}\text{Ge}_{0.9}$ layer is under 0.19% tensile strain. This suggests that at this composition and despite the thickness of the $\text{Si}_{0.1}\text{Ge}_{0.9}$ layer which has exceeded critical lattice mismatch thickness to the Ge epilayer, thermal mismatch to the Si(001) substrate imparts some degree of tensile strain to the layer.

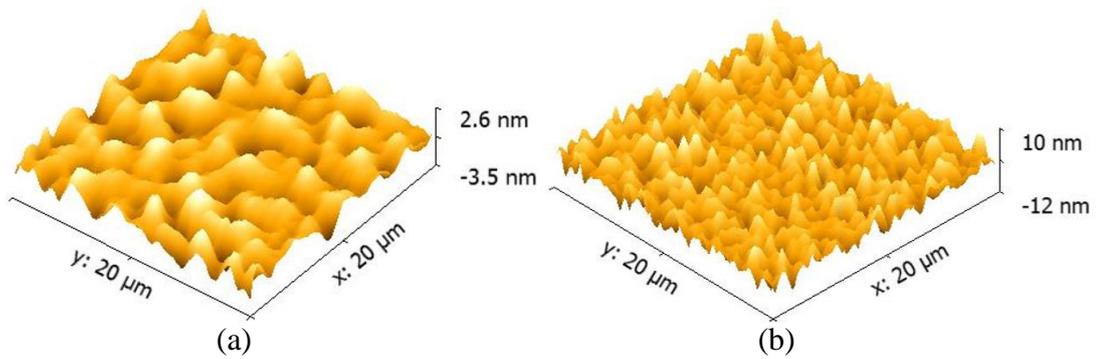


Figure 5.54: Contact mode AFM of (a) sample 15-72 930nm LT/HT Ge underlayer: $R_{\text{rms}} = 0.92\text{nm}$, height = 15.1nm (b) sample 15-73 RSG $\text{Si}_{0.1}\text{Ge}_{0.9}/\text{Ge}$ buffer layer: $R_{\text{rms}} = 2.53\text{nm}$, height = 21.2nm.

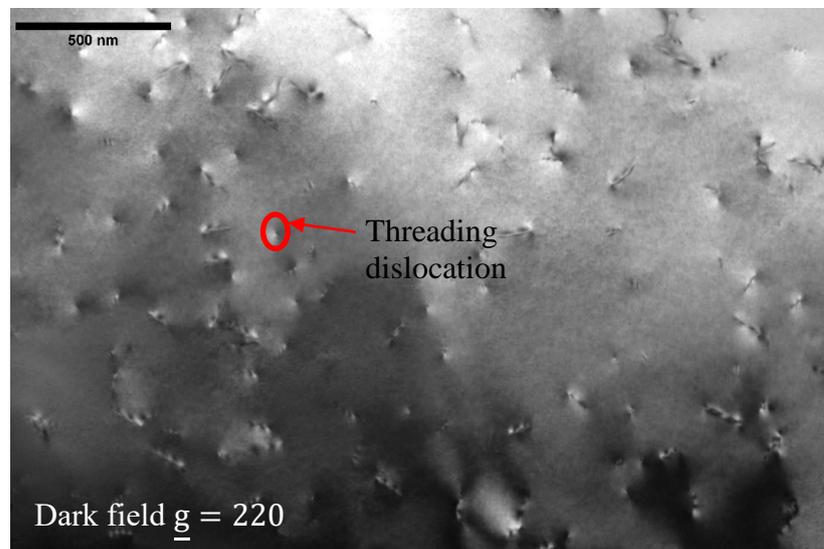


Figure 5.55: Plan view TEM of sample 15-73 RSG $\text{Si}_{0.1}\text{Ge}_{0.9}/\text{Ge}$ buffer layer. The average TDD of the sample is $2.57 \times 10^9\text{cm}^{-2}$. This is a factor of x100 more threading dislocations than in the Ge underlayer.

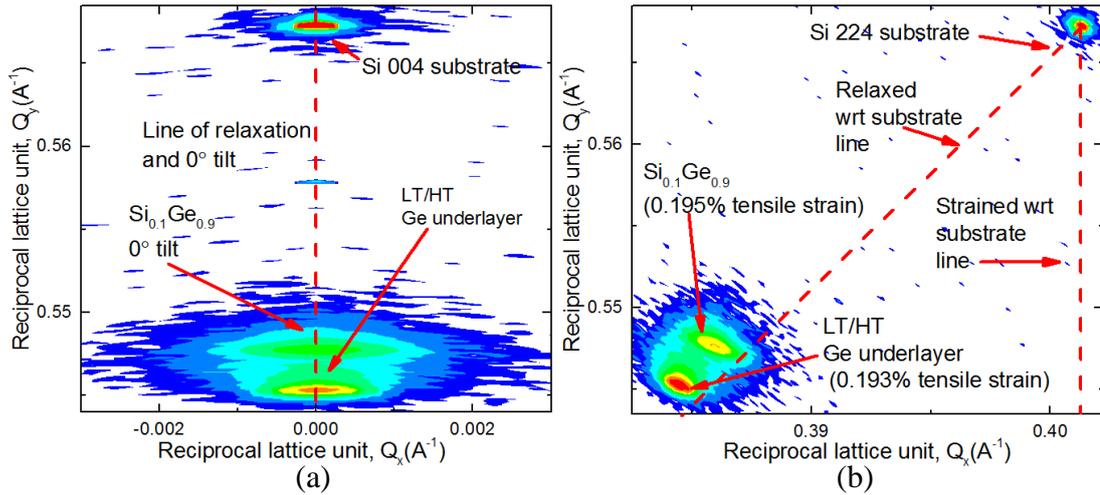


Figure 5.56: 004 and 224 HR-XRD RSM of sample 15-73: 1108nm RSG $\text{Si}_{0.1}\text{Ge}_{0.9}/\text{Ge}$ buffer layer. The broadening of the $\text{Si}_{0.1}\text{Ge}_{0.9}$ peak is due to a greater density of defects in the layer compared to the Ge underlayer.

5.6.2.2. Sample 15-77: RSG $\text{Si}_{0.16}\text{Ge}_{0.84}/\text{Ge}$ buffer layer

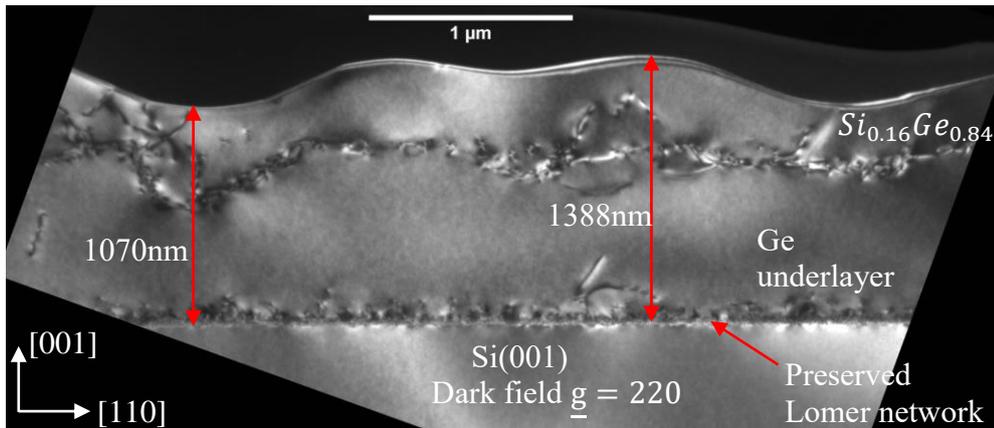


Figure 5.57: X-TEM of sample 15-77 RSG $\text{Si}_{0.16}\text{Ge}_{0.84}/\text{Ge}$ buffer layer. When depositing a $\text{Si}_{0.16}\text{Ge}_{0.84}$ layer; the interface at the Ge underlayer has been disturbed. HR-XRD shows that two compositions of $\text{Si}_{1-x}\text{Ge}_x$ are present. One layer is $\text{Si}_{0.16}\text{Ge}_{0.84}$ and the other is $\text{Si}_{0.17}\text{Ge}_{0.83}$, however it is not possible to determine where each of the layers are from the TEM image. The maximum measured thickness of the entire heterostructure in the 004 diffraction condition is 1388nm.

When reverse step grading to a $\text{Si}_{0.16}\text{Ge}_{0.84}$ layer the uniformity of the layer has been disturbed and Stranski-Krastanov growth proceeds as witnessed by the severe undulations on the surface shown in the X-TEM image in figure 5.57 and the AFM micrograph in figure 5.59. The misfit strain between the Ge underlayer and the $\text{Si}_{0.16}\text{Ge}_{0.84}$ layer is -0.919% and it is concluded that the misfit strain energy is high enough for elastic strain relaxation to take place. It is presumed that if the layer was

grown thicker, then the surface would have returned to Frank van Der Merwe growth to minimise surface free energy. The disturbance of the misfit network between the Ge underlayer and the $\text{Si}_{0.16}\text{Ge}_{0.84}$ layer is probably caused by the diffusion of silicon from the SiGe epilayer promoted by tensile strain relaxation. This diffusion effect seems to have created a separate $\text{Si}_{0.17}\text{Ge}_{0.83}$ layer, as seen in the XRD RSMs.

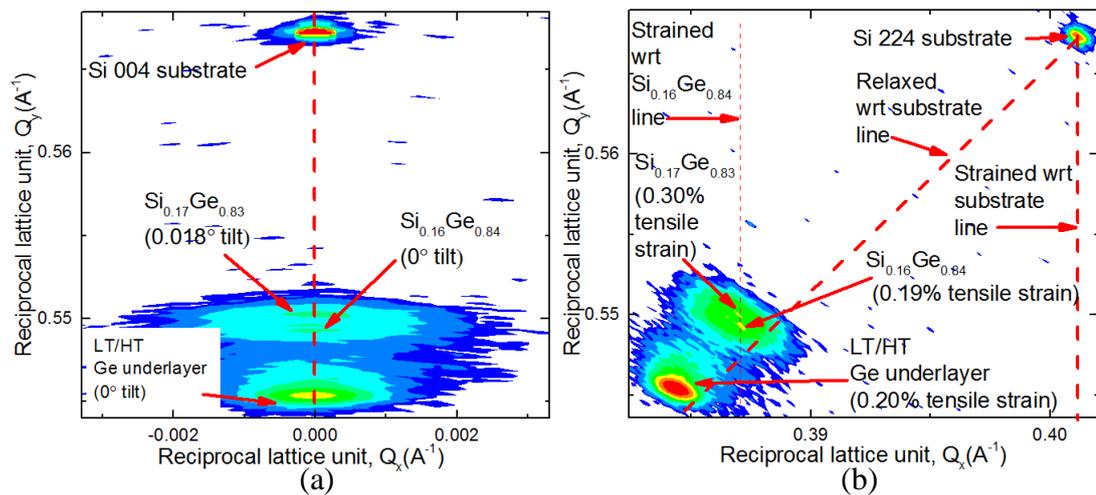


Figure 5.58: 004 and 224 HR-XRD RSM of sample 15-77: RSG $\text{Si}_{0.16}\text{Ge}_{0.84}$ /Ge buffer layer. A $\text{Si}_{0.17}\text{Ge}_{0.83}$ layer is also seen from the RSMs. The 224 RSM shows that the $\text{Si}_{0.17}\text{Ge}_{0.83}$ layer is strained with respect to the $\text{Si}_{0.16}\text{Ge}_{0.84}$ layer and is 0.018° tilted with respect to the substrate.

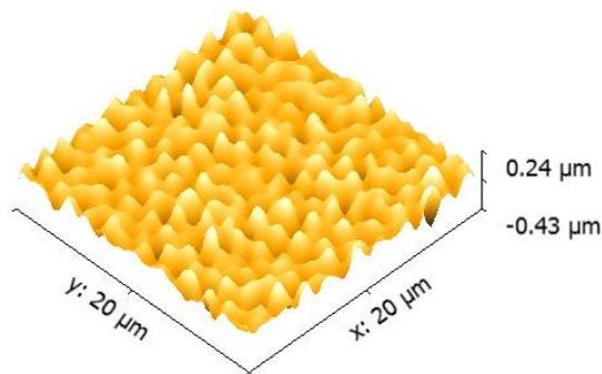


Figure 5.59: Contact mode AFM of sample 15-77. The $R_{\text{rms}} = 71.5\text{nm}$ and height is 709nm. The starting roughness in the Ge underlayer is 0.92nm. This is the maximum roughness recorded for the RSG buffer layers. This suggests that strain relief through the formation of surface undulations is at its maximum here.

Figure 5.60 is a plan view TEM image of the surface and shows threading dislocations on the surface. Due to the very rough surface it was difficult to get a 220 diffraction condition across the entire surface that was being imaged so as to clearly see the threading dislocations. The TDD of sample 15-77 is the lowest measured in this batch.

This is explained by a drop in TDD nucleation rate due to elastic strain relaxation. The cusps of the 3D islands are under higher stress and have a reduced nucleation barrier for misfit dislocations. Therefore, if the layer was grown thicker misfit dislocations would nucleate here or existing threading dislocations from the Ge underlayer would form 60° misfit dislocations at the interface and thread to the surface.

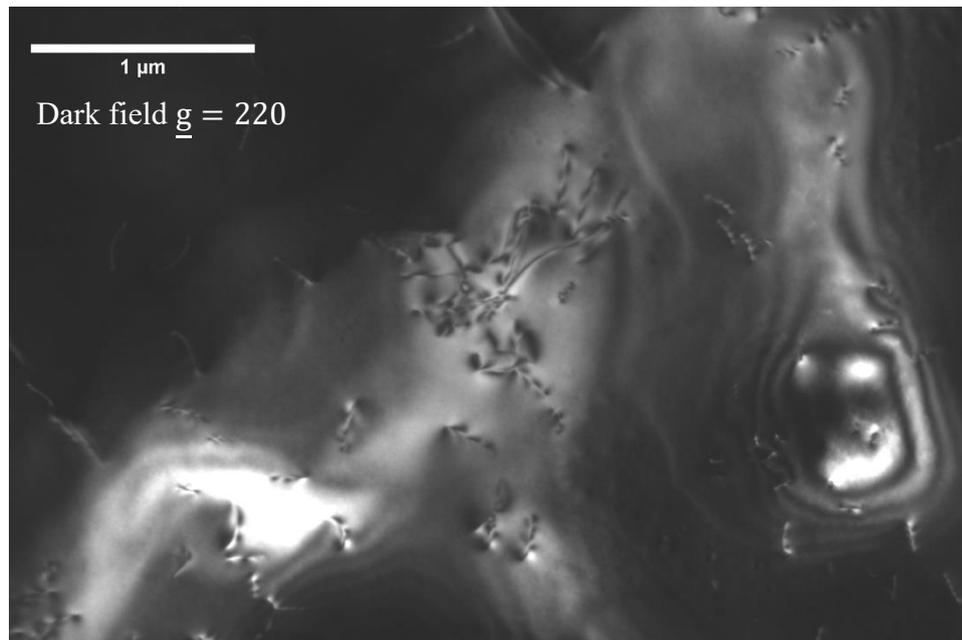


Figure 5.60: Plan view TEM of sample 15-77: RSG $\text{Si}_{0.16}\text{Ge}_{0.84}/\text{Ge}$ buffer layer. Average TDD = $5.35 (\pm 0.54) \times 10^8 \text{cm}^{-2}$.

5.6.2.3. Sample 15-74: RSG $\text{Si}_{0.28}\text{Ge}_{0.72}/\text{Ge}$ buffer layer

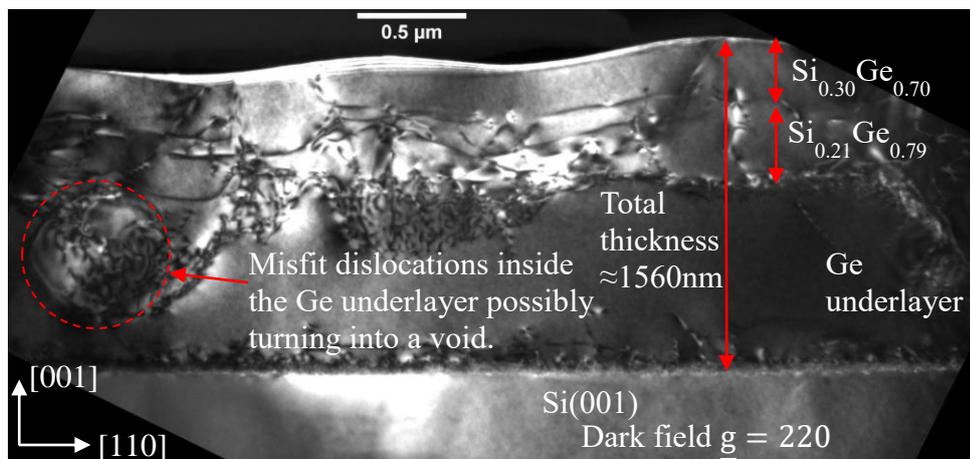


Figure 5.61: X-TEM of sample 15-74 RSG $\text{Si}_{0.28}\text{Ge}_{0.72}/\text{Ge}$ buffer layer. Total thickness = 1560nm. Reverse step grading to $\text{Si}_{0.28}\text{Ge}_{0.72}$ has caused the layer to separate into two distinct compositions, as verified

through HR-XRD, of $\text{Si}_{0.30}\text{Ge}_{0.70}$ and $\text{Si}_{0.21}\text{Ge}_{0.79}$. The positions of these two layers is estimated on the TEM image based on the locations of misfit dislocations.

The lattice mismatch between bulk $\text{Si}_{0.28}\text{Ge}_{0.72}$ and the Ge underlayer is approximately -1.44%. The lower thermal expansion coefficient function of the $\text{Si}_{0.28}\text{Ge}_{0.72}$ layer (obtained from figure 2.8 in section 2.3.1.1) compared to Ge suggests that at 850°C growth temperature the $\text{Si}_{0.28}\text{Ge}_{0.72}$ layer doesn't expand as much as the Ge underlayer, meaning that lattice mismatch dominates in the strain relaxation mechanism for the $\text{Si}_{0.28}\text{Ge}_{0.72}$ layer. The lattice mismatch is less than 2.3% and so 60° misfit dislocations have a greater propensity to form at the interface between these two layers as the layer grows thicker and becomes unstable [164].

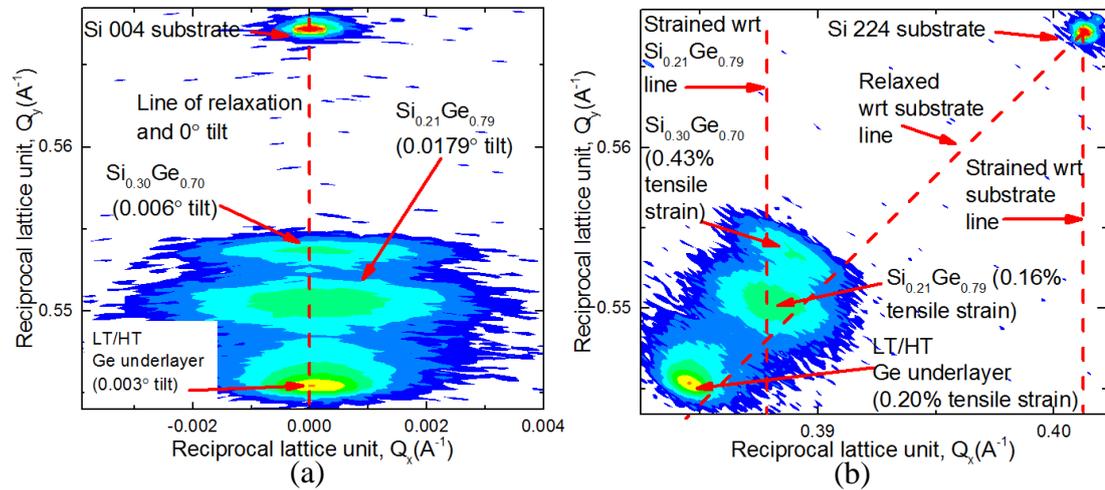


Figure 5.62: HR-XRD of sample 15-74: RSG $\text{Si}_{0.28}\text{Ge}_{0.72}$ /Ge buffer layer. Total thickness = 1560nm. Reverse step grading to $\text{Si}_{0.28}\text{Ge}_{0.72}$ has caused the layer to separate into two separate compositions of $\text{Si}_{0.30}\text{Ge}_{0.70}$ and $\text{Si}_{0.21}\text{Ge}_{0.79}$. It is assumed that the $\text{Si}_{0.30}\text{Ge}_{0.70}$ is on top and the $\text{Si}_{0.21}\text{Ge}_{0.79}$ is on the bottom. All of the epilayers are under some degree of tensile strain, with the $\text{Si}_{0.30}\text{Ge}_{0.70}$ layer being under a slightly higher tensile strain of 0.43% and the $\text{Si}_{0.21}\text{Ge}_{0.79}$ being more relaxed at 0.16% tensile strain.

At this level of misfit strain plastic deformation is preferable through the creation of misfit dislocations in the $\text{Si}_{0.28}\text{Ge}_{0.72}$ layer. However as is seen in figure 5.61, the $\text{Si}_{0.28}\text{Ge}_{0.72}$ layer has diffused even further into the Ge underlayer, more so than in sample 15-77. The interface between the $\text{Si}_{0.28}\text{Ge}_{0.72}$ layer and the Ge underlayer has been disrupted almost entirely. Misfit dislocations can be seen across the epilayer heterostructure and inside the Ge underlayer due to the presence of silicon atoms in it. The XRD RSMs in figure 5.62 show that the $\text{Si}_{0.28}\text{Ge}_{0.72}$ layer has in fact split into two distinct layers: one layer is $\text{Si}_{0.30}\text{Ge}_{0.70}$ and the other layer is $\text{Si}_{0.21}\text{Ge}_{0.79}$.

However, this time the lower Ge content layer is not so fully strained to the higher Ge content layer, most probably because it is much thicker, as indicated from the 224 reflection. Figures 5.63 and 5.64 are FIB-SEM and SEM images taken of sample 15-74. The images confirm that in some regions of the Ge underlayer, the dense misfit dislocations caused by silicon diffusion into a spherical shape has created voids. This also confirms that the voids were not created by the TEM sample preparation process and actually occurs during growth.

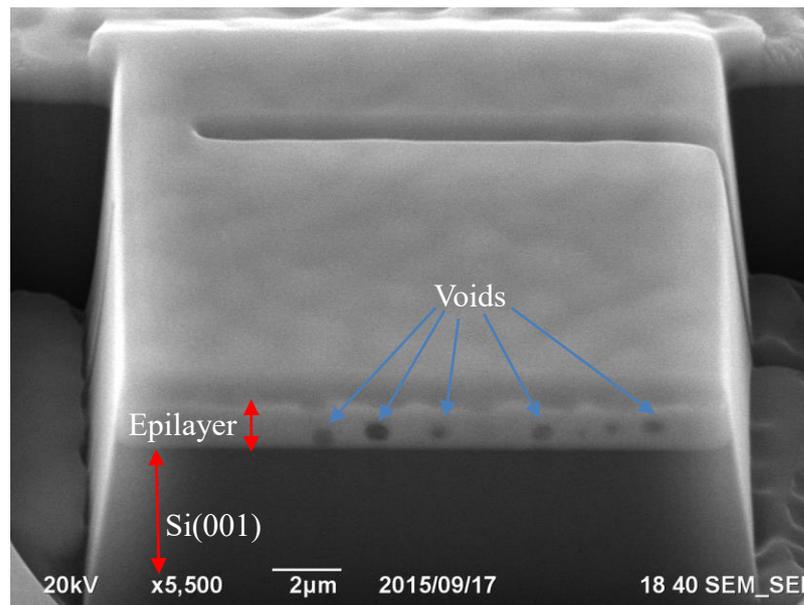


Figure 5.63: Focused ion beam-SEM image of sample 15-74 showing the presence of voids in the epilayer. The argon ion beam was used to dig a trench in the sample and then the sample was tilted to see a cross section. This was done to see a larger cross-section of the epilayer, since X-TEM only gives a limited region of thin area. As can be seen from the image, spherical voids are present in the epilayer.

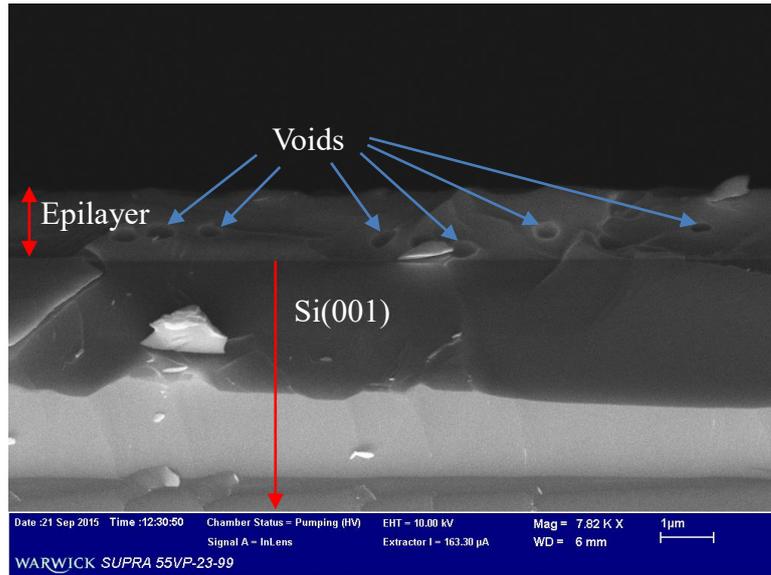


Figure 5.64: SEM image of sample 15-74, confirming the presence of voids in the epilayer. It was not possible to distinguish between the Ge underlayer and the SiGe epilayer from the SEM image. The average distance between voids is about 1.3 μm .

Figure 5.65 shows that the sample surface is still very rough, however because dislocation nucleation is energetically more favourable to island formation, a noticeable reduction in roughness is measured from sample 15-77. The diffusion of silicon from the epilayer into the Ge underlayer and the subsequent creation of a wide network of misfit dislocations and the splitting of the step layer into two separate compositions has led to this high surface roughening to relieve strain. It is presumed that these dislocations can act as sources which provide equilibration of vacancy sites for chemical diffusion due to the difference in atomic radius between silicon and germanium atoms, akin to the Kirkendall effect [165], [166].

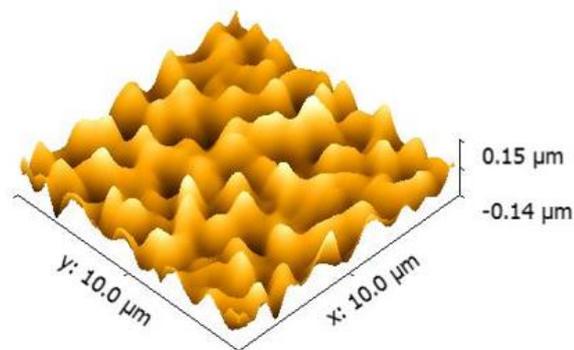


Figure 5.65: Contact mode AFM of sample 15-74: RSG $\text{Si}_{0.28}\text{Ge}_{0.72}/\text{Ge}$. $R_{\text{rms}} = 52.6\text{nm}$, height = 418nm. The real composition of the layer is: $\text{Si}_{0.30}\text{Ge}_{0.70}/\text{Si}_{0.21}\text{Ge}_{0.79}/\text{Ge}$.

Figure 5.66 is a plan view TEM image of the sample surface showing threading dislocations. Due to the surface being very undulated it was very difficult to obtain an image of the surface where the diffraction condition was met completely, everywhere.

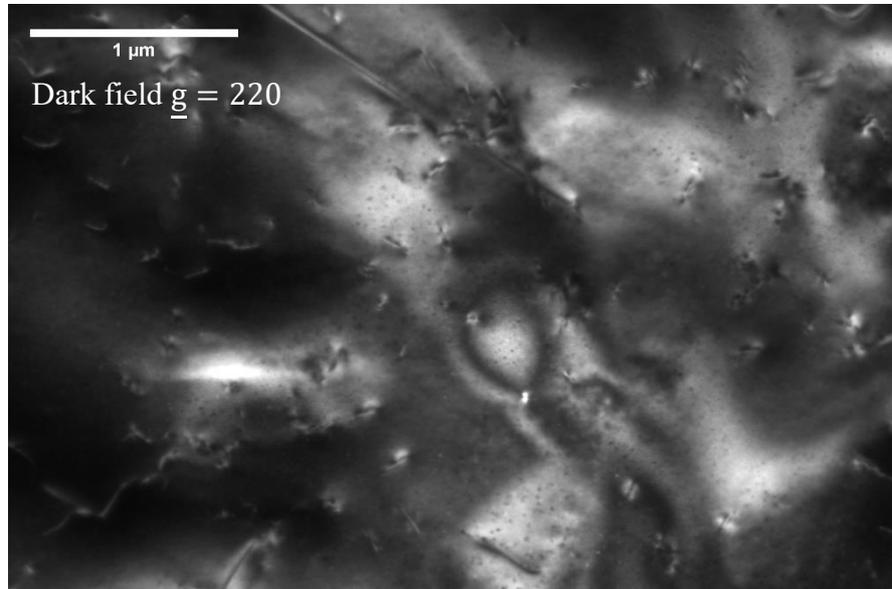


Figure 5.66: Plan view TEM of sample 15-74. Sample average TDD = $5.04 (\pm 0.5) \times 10^8 \text{cm}^{-2}$.

5.6.2.4. Sample 15-75: RSG $\text{Si}_{0.45}\text{Ge}_{0.55}$ /Ge buffer layer

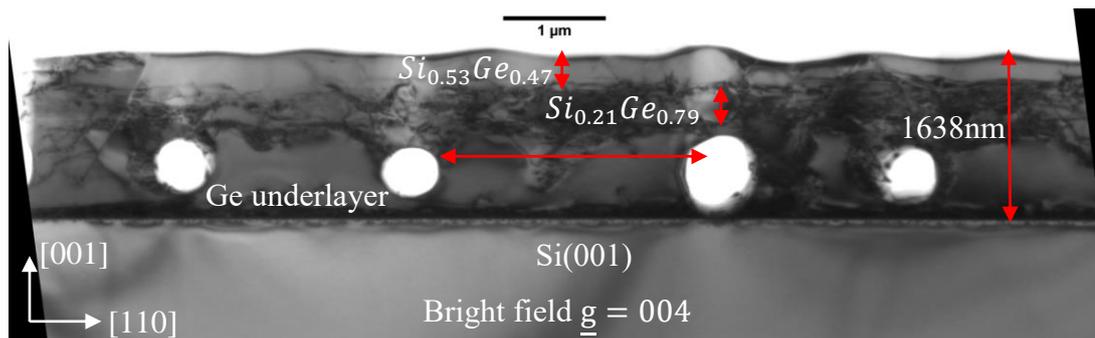


Figure 5.67: (004) diffraction condition bright field X-TEM of sample 15-75. The voids are clearly seen in the Ge underlayer. The average total thickness of the buffer layer is approximately 1638 nm. The average spacing between voids is 2.2 μm.

When reverse step grading to a $\text{Si}_{0.45}\text{Ge}_{0.55}$, X-TEM shows that there is a higher density of voids. The possible explanation to this phenomenon is that silicon has a higher diffusion constant than Ge and that at 850°C growth temperature, a layer with

higher silicon content and undergoing high tensile strain relaxation through the creation of 60° misfit dislocations has created a “pathway” for silicon atoms with smaller atomic radii to displace the Ge atoms, initially in the SiGe layer but as the misfit dislocations originate in the Ge underlayer, the silicon atoms can thus travel into the Ge underlayer firstly by intermixing into spheres and then having the spheres collapsing into voids. Figure 5.64 shows a 220 diffraction condition image of sample 15-75. Misfit dislocations are seen from the interface between the Ge underlayer and SiGe epilayer, penetrating all the way back to the Si(001)/Ge underlayer Lomer interface.

HR-XRD in figure 5.69 shows that the $\text{Si}_{0.45}\text{Ge}_{0.55}$ layer has separated into two distinct constant composition SiGe layers: $\text{Si}_{0.53}\text{Ge}_{0.47}$ and $\text{Si}_{0.21}\text{Ge}_{0.79}$. A marginally higher degree of strain is measured in the Ge underlayer as well as the bottom $\text{Si}_{0.21}\text{Ge}_{0.79}$ layer at 0.26%, but this could fall under experimental error. The two SiGe layers can be seen more distinctly in the TEM image of figure 5.68, separated by a network of 60° misfit dislocations.

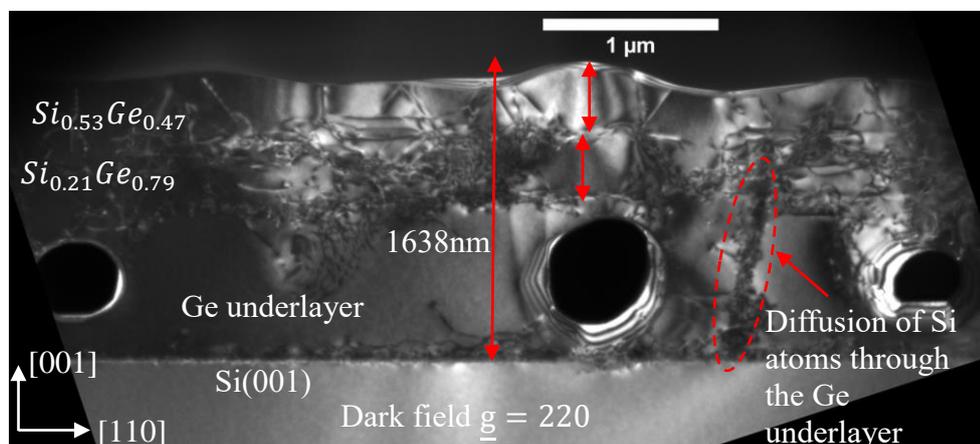


Figure 5.68: X-TEM of sample 15-75: RSG $\text{Si}_{0.45}\text{Ge}_{0.55}/\text{Ge}$. The total thickness of the layer is 1638nm (measured in the 004 diffraction condition). Silicon atoms from the SiGe epilayer can be seen diffusing through the Ge underlayer and meeting the Lomer interface between the Ge underlayer and the Si substrate. The estimated thickness of the $\text{Si}_{0.21}\text{Ge}_{0.79}$ layer is 322nm +/- 15nm and the $\text{Si}_{0.53}\text{Ge}_{0.47}$ layer is 426nm +/- 20nm.

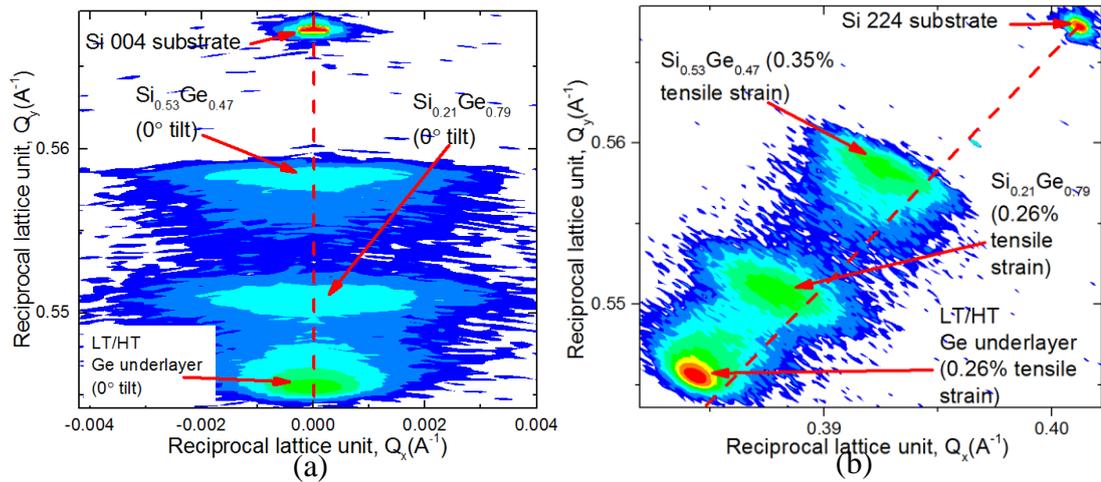


Figure 5.69: 004 and 224 HR-XRD RSMs of sample 15-75: RSG $\text{Si}_{0.45}\text{Ge}_{0.55}/\text{Ge}$. As is the case with all the other RSG samples in this batch the $\text{Si}_{0.45}\text{Ge}_{0.55}$ has separated into two layers: $\text{Si}_{0.53}\text{Ge}_{0.47}$ and $\text{Si}_{0.21}\text{Ge}_{0.79}$. The lower Ge content layer which in this case is $\text{Si}_{0.53}\text{Ge}_{0.47}$ is much more relaxed with respect to the higher Ge content SiGe layer: $\text{Si}_{0.21}\text{Ge}_{0.79}$ than was the case with sample 15-74.

The $\text{Si}_{0.53}\text{Ge}_{0.47}$ is under 0.35% tensile strain and not strained with respect to the bottom SiGe layer: $\text{Si}_{0.21}\text{Ge}_{0.79}$. It is suspected that the reason for this is probably because the $\text{Si}_{0.53}\text{Ge}_{0.47}$ layer is much thicker. As a consequence, strain relaxation takes place via generating a greater density of 60° misfit dislocations between adjacent SiGe layers, through surface roughening and also through the generation of voids in the Ge underlayer. Therefore, the surface of sample 15-75 is marginally smoother than sample 15-74 as shown in figure 5.70.

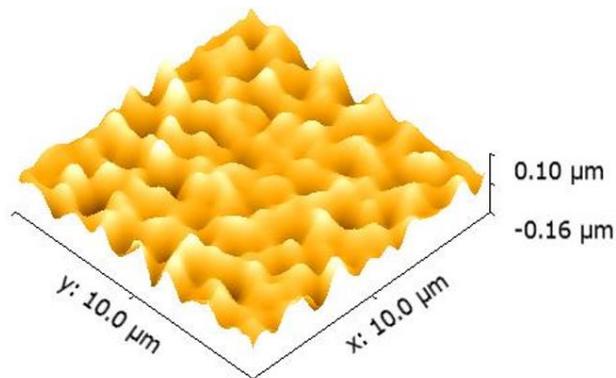


Figure 5.70: Contact mode AFM of sample 15-75. $R_{\text{rms}} = 33 \text{ nm}$, height = 273nm.

As a consequence of a greater 60° misfit dislocation network, a higher TDD count was measured for sample 15-75. Figure 5.71 is a typical plan view TEM image of the

sample. Due to the lower surface roughness, slightly better diffraction contrast TEM images could be taken of the surface.

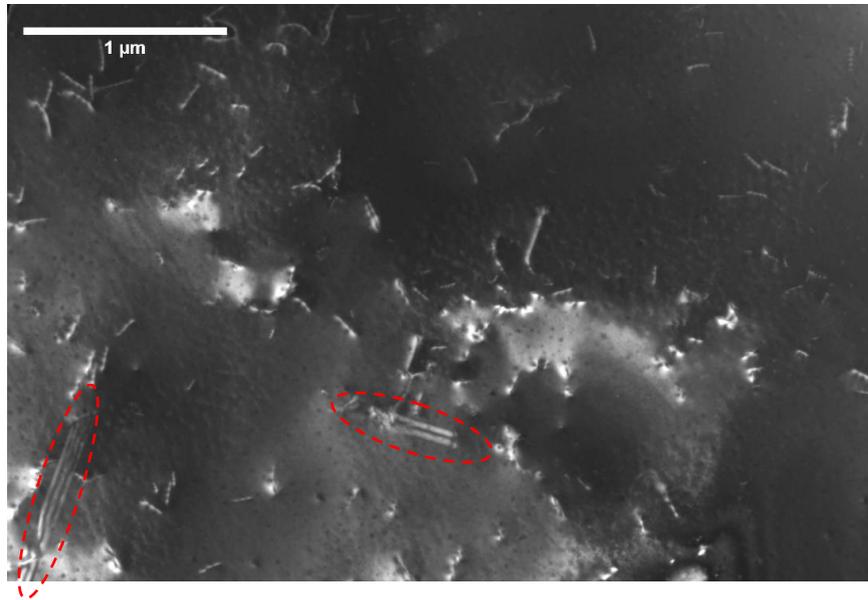


Figure 5.71: Plan view TEM of sample 15-75. Sample average TDD = $1.32 (\pm 0.13) \times 10^9 \text{ cm}^{-2}$. The red dashed ellipses highlight stacking faults.

5.6.3. Strain, surface morphology and TDD variation in RSG $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers

5.6.3.1. Strain variation

When reverse step grading, in the absence of a reverse linearly graded layer which allows the release of lattice mismatch strain slowly, it appears that the tensile strain in the top constant composition layer increases and doesn't stay at a constant 0.2% as it does with RLG layers that are graded at less than 30% Ge/ μm . For a $\text{Si}_{0.1}\text{Ge}_{0.9}$ step layer the strain is maintained at 0.2% from the Ge underlayer. However, when step grading to lower and lower compositions of Ge the strain increases and reaches an asymptote at 0.43% for the $\text{Si}_{0.3}\text{Ge}_{0.7}$ layer in sample 15-74. It is in this sample that Kirkendall voids are first witnessed which is assumed to be a tensile strain relieving mechanism. When the voids start to form in greater density, the strain in the SiGe step layer drops to 0.2% as seen in figure 5.71: i.e. as seen when a $\text{Si}_{0.46}\text{Ge}_{0.54}$ step is grown. The strain then starts to increase as a lower Ge content step layer is grown possibly due to the voids in the Ge underlayer. When reverse step grading below 70% Ge, the

separated SiGe layer at the bottom is roughly a $\text{Si}_{0.21}\text{Ge}_{0.79}$ layer. This is suspected to be because the misfit strain generated between the Ge underlayer and SiGe epilayer when the Ge content is 79%, is the maximum that can be taken whilst keeping a thermodynamically stable layer.

In figure 5.71 the green dashed circle highlights $\text{Si}_{0.21}\text{Ge}_{0.79}$ layer in the $\text{Si}_{0.53}\text{Ge}_{0.47}$ RSG buffer. This layer and the Ge underlayer beneath it with voids have marginally higher tensile strain possibly due to the radial stresses around the cavities, but this has not been confirmed.

A density of the voids in the samples where they were witnessed, was not obtained in this investigation. It is suspected that the density of voids in the Ge underlayer is correlated to the Ge content in the step layer. This hypothesis is made by observing the diffusion of silicon from the SiGe epilayer into the Ge underlayer and its increased effects as lower Ge content SiGe layers were step deposited.

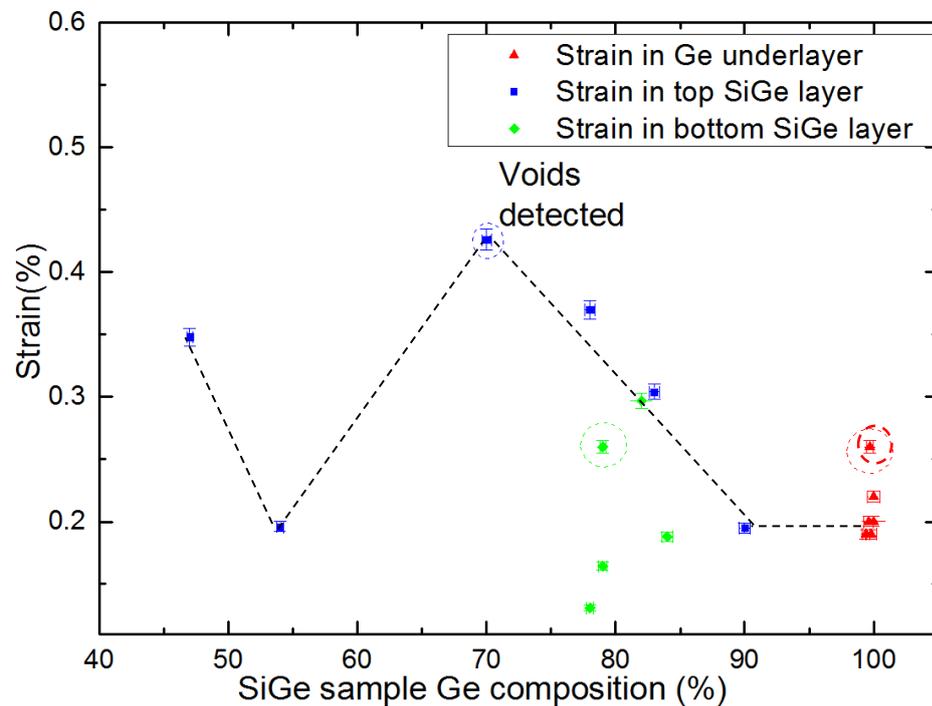


Figure 5.71: Ge composition (%) vs TDD. The dashed line is a guide for the eye only. The data point in the red dashed circle is the Ge underlayer from sample 15-74 (reverse step graded to $\text{Si}_{0.53}\text{Ge}_{0.47}$) and the point in the dashed green circle is the $\text{Si}_{0.21}\text{Ge}_{0.79}$ separated bottom layer.

5.6.3.2. Surface morphology variation

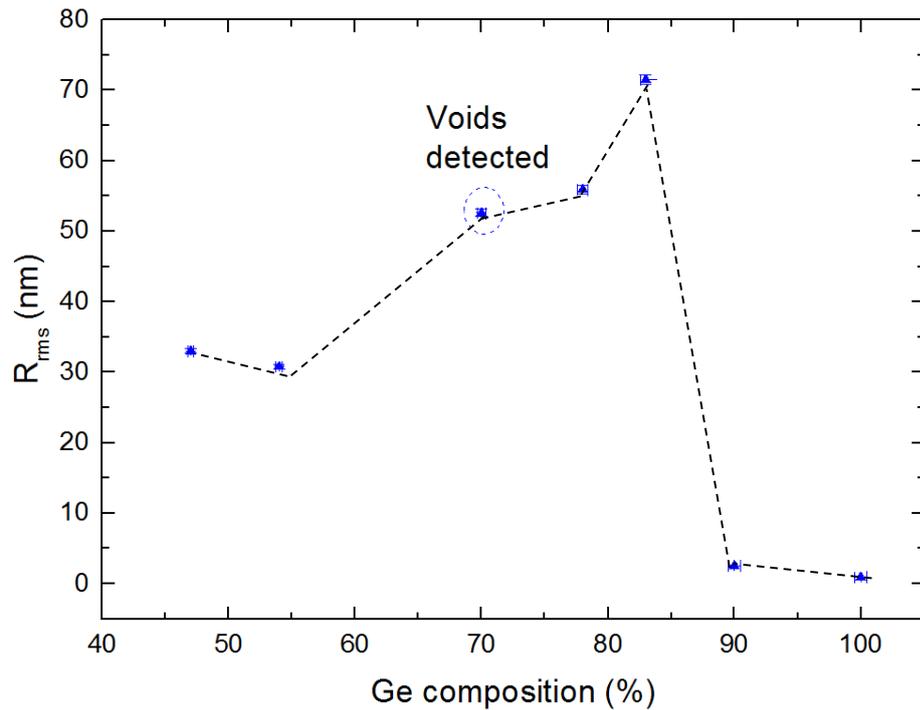


Figure 5.73: Ge composition (%) vs rms roughness. The dashed line is a guide for the eye only.

As mentioned earlier, sample 15-77 had the roughest surface, this is because at 84% Ge in the step layer, maximum strain relief is obtained through the formation of surface undulations. After 84% Ge in the step layer, the roughness reduces as higher densities of 60° misfit dislocations are generated to relieve misfit strain. After the voids start to form in the Ge underlayer a large reduction in surface roughness is observed which further supports the theory that the voids act to relieve strain.

5.6.3.3. TDD variation

The TDD is highest for sample 15-73 at $2.53 \times 10^9 cm^{-2}$. At this level the main reduction method is thought to be anti-Burger's vector annihilation as opposed to glide which requires a thicker layer for dislocations to climb. When a $Si_{0.17}Ge_{0.83}$ step layer is deposited, the TDD measured is approximately x10 lower. From 83% down to 70% step graded layers, the TDD is shown to be in annihilation regime. As the growth rate increases for lower Ge content layers in reverse graded structures, as shown in figure 5.39 in section 5.5.4, thicker layers are deposited and so adjacent SiGe layers undergo strain relaxation through 60° misfit network generation. This leads to a higher threading dislocation density, as seen in figure 5.72 after 70% Ge

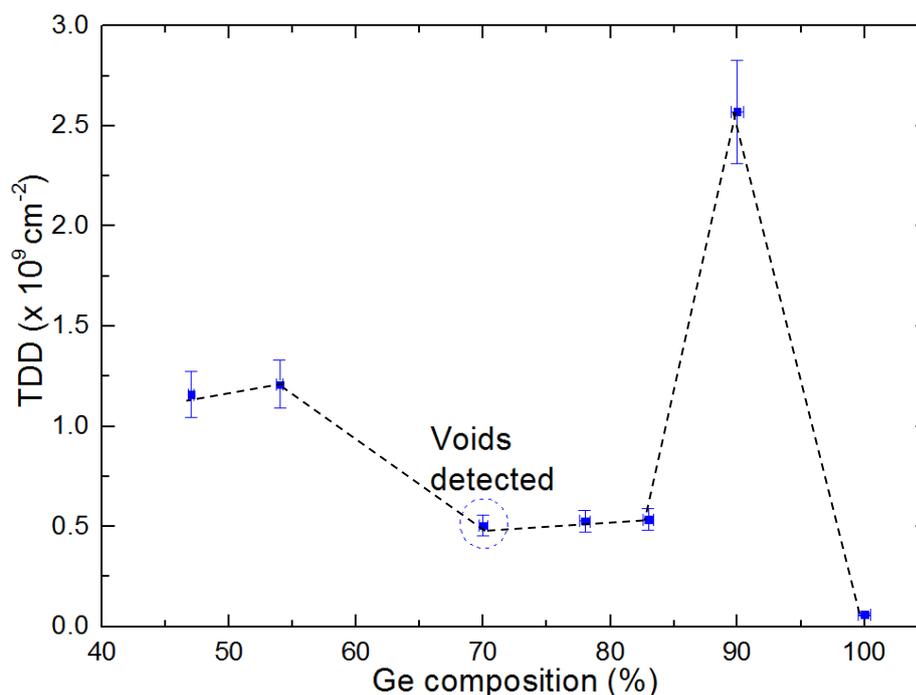


Figure 5.72: Ge composition (%) vs TDD. The dashed line is a guide for the eye only.

5.7. Chapter 5: Summary

In this chapter, three different $\text{Si}_{1-x}\text{Ge}_x$ buffer grading techniques are investigated: the established linear grading technique, the recently developed reverse linear grading technique and the reverse step grading technique, newly developed in this study.

5.7.1. Pros and cons of using linear and reverse linear graded $\text{Si}_{1-x}\text{Ge}_x$ layers for III-V integration and strained channel devices

Whilst linear grading has been investigated thoroughly over two decades, it is clear that the low mismatch between low Ge content layers and Si(001) caused 60° misfit dislocations to be generated which glide to the surface along {111} planes. The 850°C growth temperatures meant that annealing was not feasible, because this temperature

lay so close to the Ge melting temperature. As had been discovered previously, keeping a 10%Ge/ μm grading rate is essential in creating smooth surfaces, where dense cross hatching from the misfit network strain field in the linear graded region has a propensity to generate large surface undulations under compressive strain relaxation. These undulations also block and pile-up threading dislocations along orthogonal $\langle 110 \rangle$ strain fields. At low grading rates however insufficient strain is available in the graded region and therefore dislocations do not have a high enough glide velocity to be unpinned.

For buffer layers linearly graded between 9% and 20% Ge and below a grading rate of 20%Ge/ μm , the average tdd (sum of pile-up and field tdd) lies between $5 \times 10^7 \text{cm}^{-2}$ and $9 \times 10^7 \text{cm}^{-2}$. Using dichlorosilane as the silicon precursor has seen the chlorine atoms etch the surface around pinned threading dislocations at 850°C growth temperature. A trend has been observed where the samples with the lowest grading rates ($\leq 15\% \text{Ge}/\mu\text{m}$) have the highest chlorine etch pit densities. Incomplete strain relaxation has been observed in all of the linearly graded layers even at the lowest grading rates. Frank-Read loops have been observed in 220 diffraction condition X-TEM images of less than 20%Ge content layers with $\leq 15\%$ grading rates. The loops have been shown to penetrate into the substrate as well as into the constant composition layer and it is suspected that these kinetic effects are primarily the source of incomplete strain relaxation. Typical residual compressive strain ranges from 0.05% to 0.1%. At 57%Ge/ μm grading rates, the strain in the graded region reaches a maximum of 0.2% compressive strain, which gives threading dislocations a higher glide velocity and so a drop in threading dislocations is first observed at this grading rate. This drop in threading dislocations continues and reaches a maximum at 100%Ge/ μm grading rate where the drop in TDD is by x5. Above this grading rate the graded region is within the nucleation regime as piled-up threading dislocations are able to multiply into half loops caused by very dense misfit dislocation undulations in the layer.

The reverse linear grading technique offers an alternative solution. Previous studies have investigated reverse grading down to 75% Ge on a 1 μm LT/HT Ge underlayer using RP-CVD and 850°C growth temperature. That investigation yielded buffer layers of 2.7 μm thick, and the 0.2% tensile strain in the SiGe layer was found to aide

threading dislocation glide ($tdd = 4.5 \times 10^6 \text{ cm}^{-2}$) and provide a surface with a roughness of less than 3nm [117]. This investigation goes further, by reverse grading down to 45% Ge using a 555nm LT/HT Ge underlayer. A trade-off is seen between both grading techniques.

With the reverse grading technique, whilst keeping a grading rate below 30%Ge/ μm , a constant 0.2% tensile strain is observed in both the Ge underlayer and the SiGe layers even when reverse grading down 45% Ge. This high degree of strain promotes faster glide velocities for threading dislocations. Tensile strain relaxation at below 30%Ge/ μm grading rate also creates undulation free, smooth surfaces (at less than 4nm roughness) even when reverse grading down to 45% Ge. As a consequence, pile-up does not occur. The TDD for the highest Ge content reverse graded layer on on-axis Si(001) substrates is approximately $5 \times 10^7 \text{ cm}^{-2}$ and for off axis substrates it is $7 \times 10^7 \text{ cm}^{-2}$. A noticeably higher level of TDD is observed for off-axis buffer layers than on equivalent on axis buffer layers, possibly due to a Burger's vector imbalance that occurs because of the heavy step and terrace profile along the [110] direction. As the $\text{Si}_{1-x}\text{Ge}_x$ layer is reverse graded to lower Ge content, a drop in TDD is observed which coincides with a rise in stacking faults. A rise in stacking faults is seen when reverse grading below 70% Ge due to an increase in strain energy in the graded region leading to $F_{\text{strain}} (90^\circ)$ being greater than F_{SF} for dissociated 60° misfit dislocations. It is this rise in stacking faults that marginally roughens the surface with a 45% Ge buffer layer. It is recommended that in future work, reverse grading be carried out to pure silicon to investigate the behaviour of stacking faults, but for the sake of this investigation it is hypothesised that the stacking fault line density will continue rise when reverse grading to lower Ge content layers. 2D defects are far more damaging than 1D threading dislocations since they create much higher leakage currents in semiconductor devices fabricated on the layer and will undoubtedly be passed onto further epitaxial layers, i.e. when considering epitaxy of III-V materials with lattice constants that are closer to silicon such as GaP (5.4505) and AlP (5.4635) which would require buffer layers of $\text{Si}_{0.85}\text{Ge}_{0.15}$ and approximately $\text{Si}_{0.8}\text{Ge}_{0.2}$ respectively taking into account thermal expansion coefficient mismatch between GaP and AlP with Si(001). It is a conclusion from this work that reverse grading may not be the solution to lattice matched integration of III-V semiconductors such as GaP and AlP due to the

phenomenon of rising stacking faults. Up to 70% Ge reverse graded buffer are suitable and smooth enough for epitaxy and devices fabrication.

The buffer layer structure maintains a 0.2% tensile strain throughout, due to the LT/HT Ge underlayer being over relaxed. This has undoubtedly contributed to stress being built up in the heterostructure that has caused it to crack under applied stress. Experimentally, one course of investigation would be to use sample 15-61 in chapter 4 (400°C 78nm layer + 5min anneal at 650°C) as a replacement for the Ge underlayer, since the strain in this sample is 0.036% tensile which is a fifth of the LT/HT underlayer used in this chapter. It has also been noted in this investigation that crack line density has reduced with reducing Ge content in the layer and therefore the relaxation due to cracks has also reduced with lowering Ge content in the buffer layers.

From HR-XRD analysis, the strain in the Ge underlayer and the reverse graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layer grown to identical compositions of Ge are the same when grown on on or off-axis substrates. When comparing sample 13-166 which was grown on axis and reverse graded to 65.8% Ge with sample 13-163 which was grown off-axis and reverse graded to 65.9% Ge, the tensile strain that was measured agrees to 0.05% and so there is no greater distortion in-plane by growing off-axis. The only noticeable feature is that the Ge underlayer and the $\text{Si}_{1-x}\text{Ge}_x$ reverse graded buffer layer are both tilted with respect to the substrate by 0.22° when grown off-axis.

In previous works GaP has been integrated onto Si(001) using a 400nm RP-CVD grown $\text{Si}_{0.85}\text{Ge}_{0.15}$ linearly graded buffer layer [76] to overcome the small but not negligible lattice mismatch between Si and GaP of 0.36% at room temperature. Likewise, GaAs has been integrated onto Si using linearly graded buffer layers graded up to pure Ge at 10%Ge/ μm grading rate, meaning that the layers were over 10 μm thick but required CMP once 50% Ge composition was reached to prevent high surface roughening [167]. The reverse graded buffer offers an alternative to lattice matched integration of GaAs. As mentioned in the conclusions section of chapter 4, due to the over-relaxation of LT/HT Ge, the in-plane lattice constant is slightly larger than that for bulk Ge. The reverse graded $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace layer has an in-plane lattice constant matched to GaAs. Its critical thickness when relaxing on a Ge epilayer is

approximately 60nm and it is suspected that due to the low mismatch between the Ge underlayer and the $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace, 60° misfit dislocations will be generated. This will presumably lead to a much higher TDD in the $\text{Si}_{0.05}\text{Ge}_{0.95}$ terrace layer than in the Ge underlayer of $1 \times 8 \text{ cm}^{-2}$ as was evidenced in the $\text{Si}_{0.1}\text{Ge}_{0.9}$ step layer in sample 15-73.

5.7.2. Reverse step grading and the formation of Kirkendall voids

The purpose behind reverse step grading was so as to create reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ structures that omitted the reverse graded region entirely, with the aim to prevent cracks from forming. In attempting to do so, the 850°C growth temperature has allowed Si to diffuse into the Ge underlayer. From sample 15-73 ($\text{Si}_{0.1}\text{Ge}_{0.9}/\text{Ge}$), where the thickness of the Ge underlayer was measured to be thinner than in sample 15-72, it is assumed that some degree of silicon diffusion had started to take place at that point. Later as the Ge content in the SiGe layer reduces, the diffusion effects become more pronounced, as seen in sample 15-77 where the uniform misfit interface between the Ge underlayer and the SiGe epilayer has been disturbed and is no longer a straight line. Growth temperature, tensile strain relaxation and silicon content in SiGe epilayer are undoubtedly contributors to this phenomenon.

The Kirkendall phenomenon has been greatly investigated in transition metals and metal oxides, however due to the extremely low inter-diffusion rates for Si and Ge (and reported in section 4.2.4), the Kirkendall effect has only been reported in thin film [168] or nanowire structures [169].

The thickness of the Ge underlayer may also be a contributor to this phenomenon, but this is not verified in this investigation. Furthermore, a density of the voids could not be obtained in this investigation however it is suspected that void density increases with lowering the Ge content in the SiGe step layer. It is recommended as future work to investigate reducing the Ge content in the SiGe step layer further to see if more voids are generated in the underlayer and also to determine a quantitative count of the number of voids per sample.

6. Ge and Si_{1-x}Ge_x/Ge buffer layers on 6° off axis Si(001) substrates using RP-CVD.

This chapter is divided into two sub investigations. The first investigation is on Ge buffer layers grown on 6° off-axis Si(001) to use as virtual substrates to integrate InSb through SS-MBE. The second sub investigation is on reverse terrace graded (RTG) Si_{1-x}Ge_x/Ge buffer layers grown on both on-axis and off-axis Si(001) substrates for comparison to each other and also to the RLG buffer layers in chapter 5.

6.1. Background to pure Ge buffer layers on 6° off-axis Si(001) substrates.

In 2009 Hartmann et al investigated the RP-CVD growth of LT/HT Ge buffer layers on on-axis Si(001) and 6° off-axis Si(001) [170]. The low temperature layers were grown between 330°C and 450°C and the high temperature layers were grown between 600-850°C. Four cycles of thermal annealing were also carried out at temperatures between 875°C and 900°C. A growth rate reduction of 5% was observed when growing Ge on off-axis substrates; the growth rate on on-axis Si(001) was determined to be 8.6nm/min at 400°C and 100Torr pressure, whereas on 6° off-axis Si(001) at the same temperature and pressure the growth rate was 8.2nm/min. When the temperature was elevated to 750°C and the pressure dropped to 20 Torr, the HT Ge layer grew at 44nm/min on 6° off axis Si(001) and 45.5nm/min on on-axis Si(001). The reduced growth rate on off-axis substrates is due to the presence of the [110] plane in the offcut which has a lower dangling bond density as explained in section 2.4.3.1.

Hartmann et al also discovered that as well as mounds and perpendicular cross hatching; the threading dislocation {111} glide planes intersecting on a 6° offcut surface causes three sets of lines on the Ge buffer layer surface. One along the <110> direction (perpendicular to the offcut direction) and the other two roughly 9° apart on either side of the <110> direction parallel to the offcut direction.

More recent work on Ge buffer layer growth on 6° off-axis substrates includes the work by Lee et al [171]. The results in that study seems to indicate that Ge buffer layers

grown on off-axis Si(001) substrates are under 0.6% tensile strain. However, in that investigation only substrate orientated rocking curves were carried out to measure the strain of the epilayer. Without doing reciprocal space mapping to satisfy the Bragg condition for the Ge epilayer on off-axis substrates tilt in the epilayer cannot be seen and corrected therefore erroneous values for strain are presumed to be calculated, as will be seen in this study.

6.2. Background on terrace grading in $\text{Si}_{1-x}\text{Ge}_x$ buffer layers

The technique of terrace grading was first developed by Capewell in 2002 for linearly graded SiGe buffer layers and involves periodically alternating linearly graded and constant composition layers in the graded region [172]. By having high grading rates in the graded regions, more strain is available to provide threading dislocations with higher glide velocities and therefore promoting relaxation as well as dislocation annihilation. However, to prevent the onset of elastic strain relaxation, the grading rate has to be low enough to prevent strain energy from accumulating and causing Stranski-Krastanov growth. The addition of the constant composition layers intermittently permits the layer to relax and thereby allowing the surface free energy to reduce to low enough levels and promote 2D growth.

Subsequent work on linear terrace grading by Nash in 2005 [131], investigated linear terrace grading in $\text{Si}_{1-x}\text{Ge}_x$ buffer layers for $1 \geq x \geq 0$. Up to $x = 0.5$, the TDD ranged between 10^6 and 10^4 cm^{-2} and the surface roughness lay under 3nm, however the top layer remained 0.2% compressively strained as a side effect of the high grading rate in the graded regions. Beyond $x = 0.5$ and up to pure Ge, the TDD was noticed to increase to 10^7 cm^{-2} and the roughness increased to 13nm.

In 2009 Shah investigated reverse terrace grading (RTG) to $\text{Si}_{0.2}\text{Ge}_{0.8}$ [173]. This technique is similar to the linear terrace grading method however as with the reverse linear grading process (RLG) in chapter 5, a Ge buffer layer is deposited on the Si(001) substrate first and then the $\text{Si}_{1-x}\text{Ge}_x$ layer is reverse graded back to the required Ge

composition. It was discovered that RTG buffer layers offered marginally lower TDD than RLG buffer layers (x1.6 reduction) at 1.9nm roughness when reverse graded back to 77% Ge at 12%Ge/ μm grading rate. The average grading rate over the reverse terrace graded region is defined as:

$$R_{\text{gr reverse (average)}} = \frac{(1-\text{final composition})}{\text{RTG region total thickness}} \times 100 \quad (\text{Equation 6.1})$$

The effective grading rate is the grading rate in the graded regions only and is defined as:

$$R_{\text{gr reverse (effective)}} = \frac{\text{No. of graded layers and constant composition terraces}}{\text{No. of graded layers}} \times R_{\text{gr reverse (average)}} \quad (\text{Equation 6.2})$$

6.3. This study on Ge buffer layers on 6° off-axis Si(001).

The aim of this investigation is to create a high quality pure Ge buffer layer on 6° off-axis Si(001) and under 1 μm thickness to create a Ge/Si(001) virtual substrate for the SS-MBE epitaxy of an AlSb buffer layer and InSb in chapter 7. GeH₄ is used as the precursor with H₂ as the carrier gas.

A LT/HT approach was taken with the Ge buffer layer, because chapter 5 has shown that such buffer layers have under 1nm roughness and approximately $6 \times 10^7 \text{cm}^{-2}$ TDD, when grown on on-axis Si(001) up to 900nm thickness. The in-plane over-relaxation was deemed acceptable in this case. For the purpose of integrating InSb, as much tensile strain relaxation in-plane was aimed for in the Ge buffer layer so as to create a higher in-plane lattice constant and therefore minimise the lattice mismatch to the AlSb buffer layer and subsequently the InSb layer. A 10 min annealing stage was used in the structure to promote glide of threading dislocations. There was no danger in cracks appearing in the film because the thickness of the Ge buffer layer lay under 1 μm and a reverse graded SiGe layer was not going to be deposited on top of the Ge buffer layer.

6.3.1. Ge buffer layer on 6° off-axis Si(001) design.

Ge	650°C	4:41	Stage 2	Stage 3
Anneal	650°C	10:00		
HT-Ge	550°C	3:42		
LT-Ge	350°C	18:51	Stage 1	
p ⁻ Si(001) 6° off-axis				

Figure 6.1: Ge buffer layer on 6° off-axis Si(001) substrate using GeH₄ as the precursor and H₂ carrier gas. Stage 1 involved depositing a LT layer at 350°C. Stage 2 involved depositing a HT layer on top at 550°C and then annealing for 10 mins under H₂ at 650°C. Stage 3 involved depositing a final HT Ge layer at 650°C. This Ge buffer layer structure is used in chapter 7 for the SS-MBE deposition of AlSb and InSb.

Anneal	650°C	10:00
LT-Ge	350°C	18:51
p ⁻ Si(001) 6° off-axis		

Figure 6.2: Annealed LT-Ge buffer layer on 6° off-axis Si(001) substrate using GeH₄ as the precursor and H₂ carrier gas. Only one sample was manufactured to the above specification: 15-171

Sample number	stage	Total thickness (nm)
15-172	1	65
15-170	2	526
15-208	3	881

Figure 6.3: List of Ge buffer layer on 6° off-axis Si(001) samples.

The substrates used in this chapter are 100mm Si(001) 6° off-axis towards the [110] direction with a tolerance of +/-0.5°. The thickness of the substrates is 525µm. The on axis wafers were of the same diameter and thickness and had a tolerance of +/-0.5°. Before deposition a 1000°C bake was carried out to remove the native oxide. The growth pressure used was a 100 Torr. The GeH₄ flow rate is 150 sccm and the H₂ carrier gas flow rate was 20,000sccm.

6.3.2. Material quality of the layer through the stages.

6.3.2.1. Stage 1. Sample 15-172: LT-Ge buffer layer on 6° off-axis Si(001)

When compared to sample 14-301 in section 4.2.3, sample 15-172 has a similar morphology. Both Ge buffer layers are grown at 350°C and up to similar thicknesses. Whilst 14-301 was grown on on-axis Si(001) to 75nm thickness, 15-172 was grown on 6° off-axis Si(001) to 65nm thickness as seen in figure 6.4. X-TEM reveals that the sample is very defective but appears to have a reasonably smooth surface. The 2D defects at the interface are possibly twins generated during initial stages of growth and arise from the (111) facets. HR-XRD was not carried out on this sample because it was very thin but it is assumed that the layer is under 0.2% compressive strain based on 350°C growth of Ge buffer layers in chapter 4. It is also assumed that the layer is tilted due to the asymmetrical dislocation annihilation from the offcut substrate.

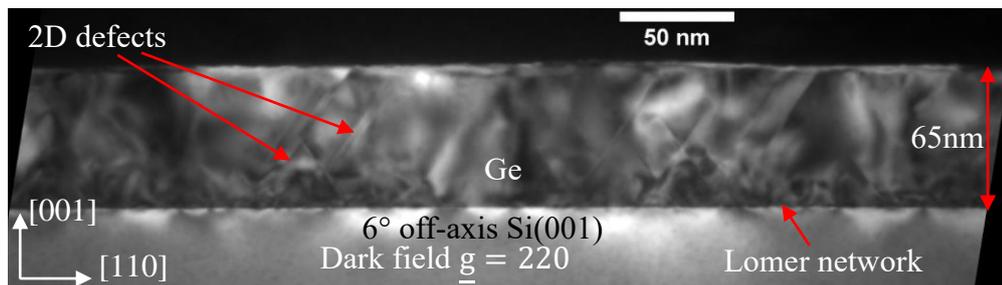


Figure 6.4: X-TEM of sample 15-172: 350°C Ge/6° off-axis Si(001). 2D defects (possibly microtwins) can be seen.

AFM measurements reveal that facets have started to form in sample 15-172 as shown in figure 6.5. In sample 14-301, facets were first noticed at 42nm thickness when Ge was grown at 350°C on on-axis Si(001). When comparing sample 14-301 with 15-172, it seems that faceting occurs in the Ge buffer layer regardless of whether the layer is grown on-axis or off-axis and that lower than 400°C growth temperature is the key triggering parameter. The surface roughness of the LT-Ge layer is approximately 1.21nm. Plan view TEM in figure 6.6 shows that the 65nm LT-Ge layer has a TDD of $6.85 \times 10^{10} \text{cm}^{-2}$.

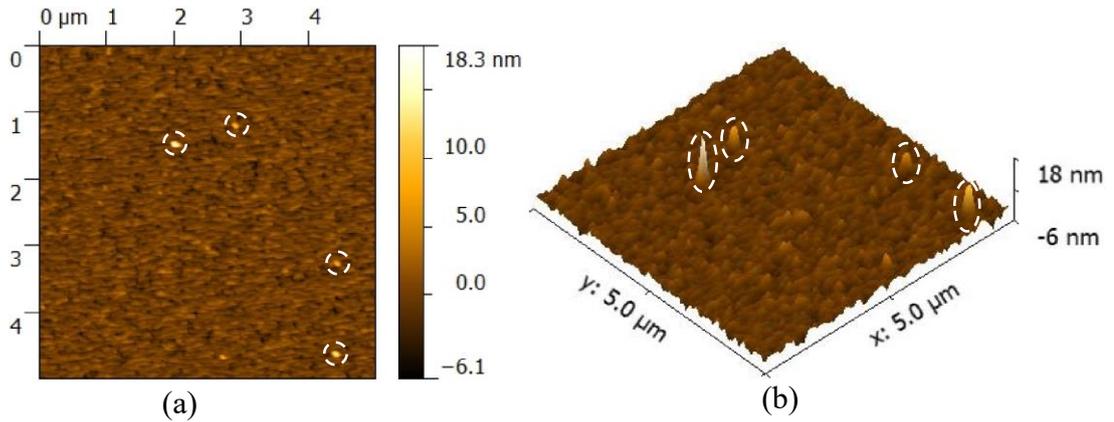


Figure 6.5: $5\mu\text{m} \times 5\mu\text{m}$ Tapping mode AFM of sample 15-172: 350°C Ge/ 6° off-axis Si(001). The white dashed circles indicate facets. The scan speed was 1s/line. Due to the relatively fast scan speed the facets appear as peaks. It is presumed that if the scan speed was slowed down further then the features would be resolved more clearly. $R_{\text{rms}} = 1.21\text{nm} \pm 0.2\text{nm}$. Height = $24\text{nm} \pm 5\text{nm}$.

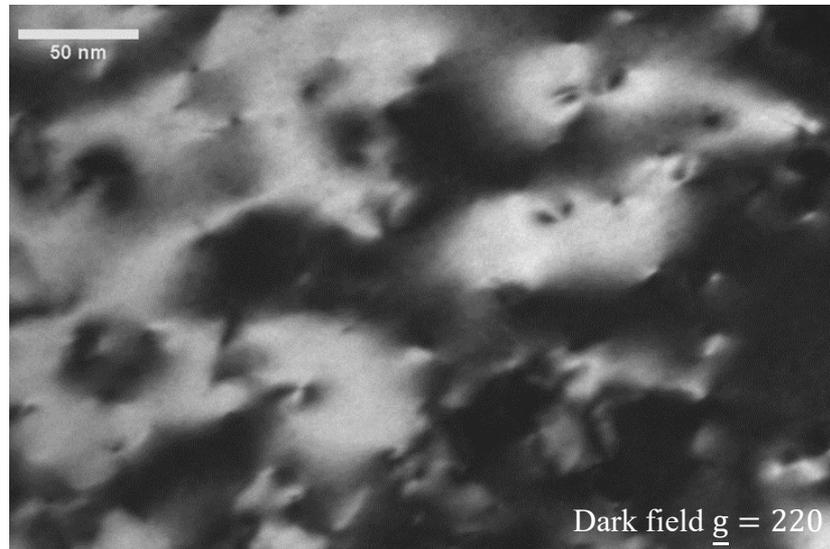


Figure 6.6: TEM image of sample 15-172: 65nm LT-Ge/ 6° Si(001). Sample average TDD = $6.85 \times 10^{10}\text{cm}^{-2}$.

6.3.2.2. Stage 2. Sample 15-170: Anneal/HT-Ge/LT-Ge buffer layer on 6° off-axis Si(001)

The HT-Ge layer is 461nm thick. When the HT-Ge layer is deposited on the LT-Ge buffer at 550°C and then annealed at 650°C for 10 mins, a dramatic increase in quality is observed from figure 6.7. At the interface between Ge epilayer and Si(001) substrate, Lomer dislocations can be seen suggesting that the layer has transitioned from compressive strain in sample 15-172 to tensile strain as seen in figure 6.8.

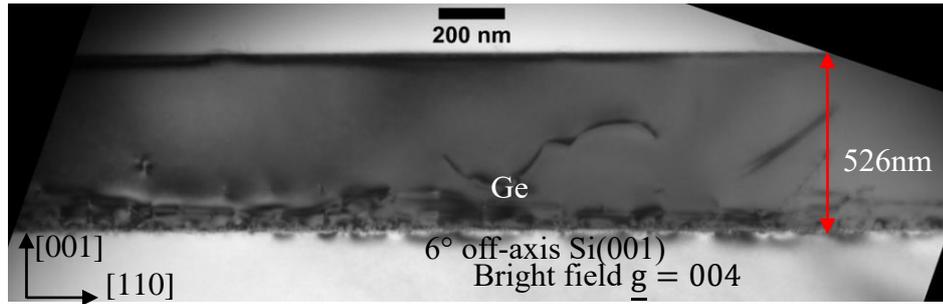


Figure 6.7: TEM image of sample 15-170: Anneal/HT-Ge/LT-Ge/6° Si(001). The HT-Ge layer is 461nm thick, calculated by subtracting the LT-Ge layer thickness from the total thickness of this sample.

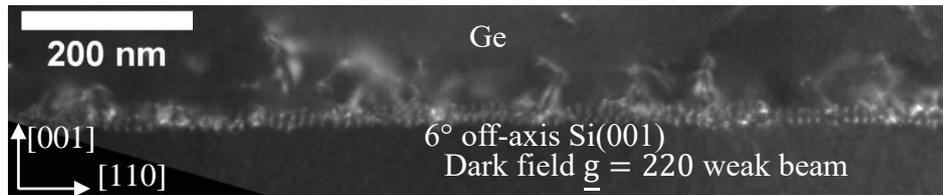


Figure 6.8: TEM image of sample 15-170: Anneal/HT-Ge/LT-Ge/6° Si(001). The presence of Lomer dislocations indicates that the layer has transitioned to tensile strain from compressive strain in the LT-Ge layer.

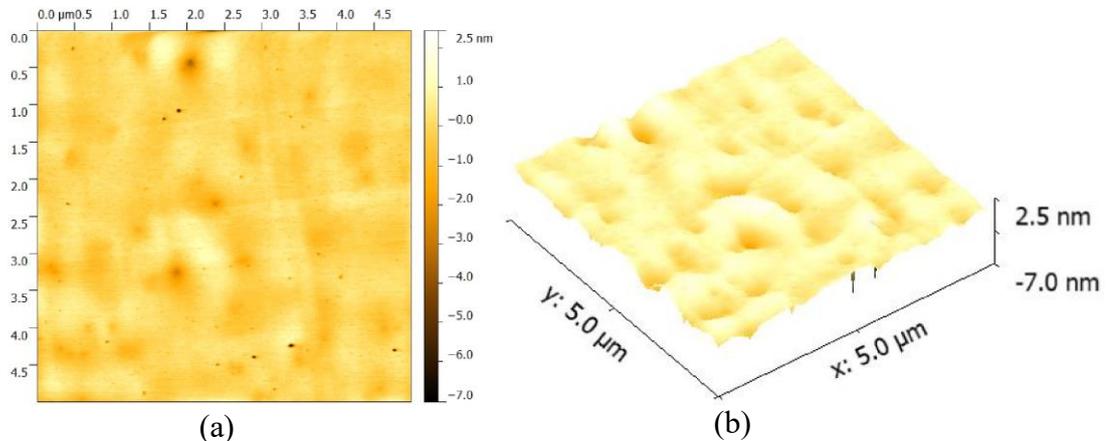


Figure 6.9: 5μm x 5μm Tapping mode AFM of sample 15-170: Anneal/HT-Ge/LT-Ge/6° Si(001). $R_{rms} = 1.91\text{nm} \pm 0.2\text{nm}$. Height = 12nm \pm 5nm.

Tapping mode AFM shows that the roughness of sample 15-170 has increased marginally to 1.91nm. The facets on the surface have disappeared and instead mild cross hatching can be seen. It is presumed that this cross hatching is because of the threading dislocations propagating on {111} planes, as witnessed by Hartman et al [170]. High temperature growth could possibly cause 60° misfit dislocations to climb and combine to form Lomer dislocations. The combination of HT growth and annealing for 10 mins has the effect of reducing the TDD by x300 from sample 15-

172 through glide and annihilation and possibly through Lomer and 60° climb as seen in figure 6.10.

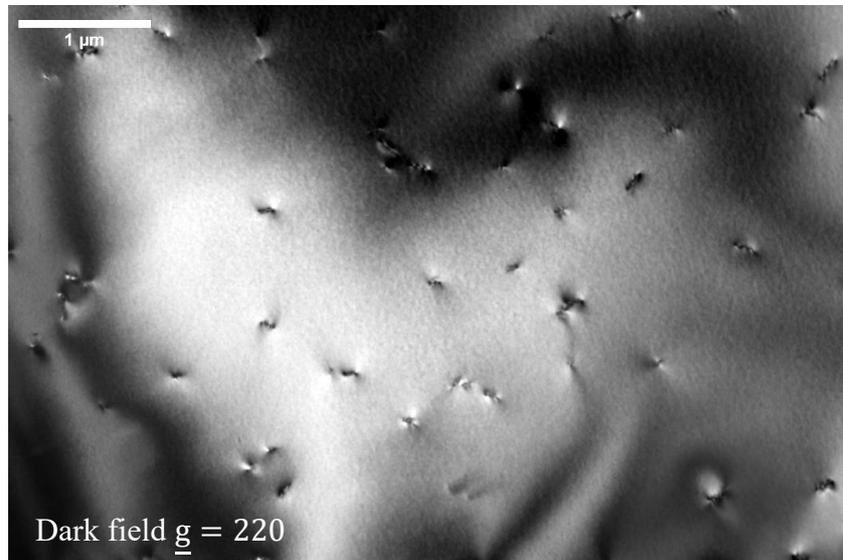


Figure 6.10: Plan view TEM image of sample 15-170: Anneal/HT-Ge/LT-Ge/ 6° Si(001). Sample average TDD = $2.32 \times 10^8 \text{cm}^{-2}$.

6.3.2.3. Stage 3. Sample 15-208: Ge/Anneal/HT-Ge/LT-Ge buffer layer on 6° off-axis Si(001)

The final stage involves depositing a 650°C layer on top of the anneal/HT-Ge/LT-Ge buffer layer to further promote glide. At the end of sample 15-170 the TDD was $2.32 \times 10^8 \text{cm}^{-2}$. The thickness of the 650°C Ge layer is approximately 355nm and the total thickness of the Ge buffer layer is 881nm as shown in figure 6.11.

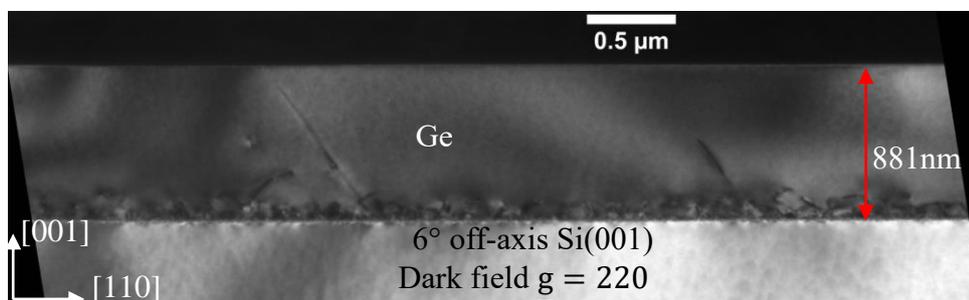


Figure 6.11: X-TEM of sample 15-208: Ge/anneal/HT-Ge/LT-Ge/ 6° Si(001). The thickness of the 650°C Ge layer was calculated by subtracting the thickness of this layer from sample 15-170 and was determined as 355nm.

Figure 6.12 is a HR-XTEM image of sample 15-208. Lomer dislocations are seen at the interface, where the distance between dislocations is measured and shown in the figure. In sample 15-72 (LT/HT Ge grown on on-axis Si(001)) the distance between Lomer dislocations was measured as approximately 11nm (section 5.6.1.1 figure 5.50) and as mentioned, the predicted distance between Lomer dislocations for strain relaxation in Ge on Si is approximately 9.6nm. It appears that the distance between Lomer dislocations on terraces is marginally longer when grown off-axis however HR-XRD shows that the strain for off and on-axis buffer layers is identical. Further investigation in HR-XTEM is needed to confirm Lomer spacing.

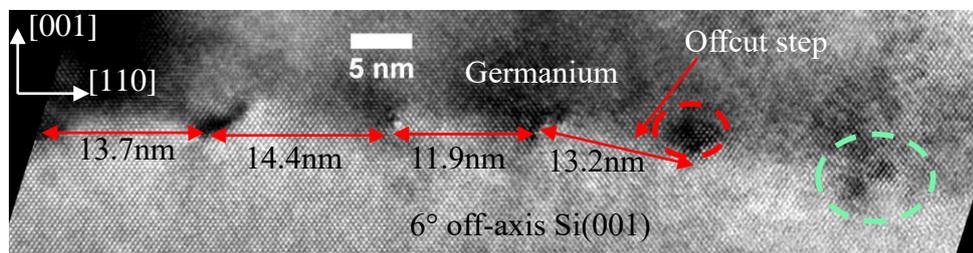


Figure 6.12: [110] zone axis HR-XTEM image of sample 15-208: Ge/anneal/HT-Ge/LT-Ge/6° off-axis Si(001). The step and terrace profile of the offcut substrate can be seen. Lomer dislocations can be seen at the interface between the off axis substrate and Ge epilayer. The Lomer dislocation in the red dashed circle appearing at the edge of a terrace is magnified in figure 6.13.

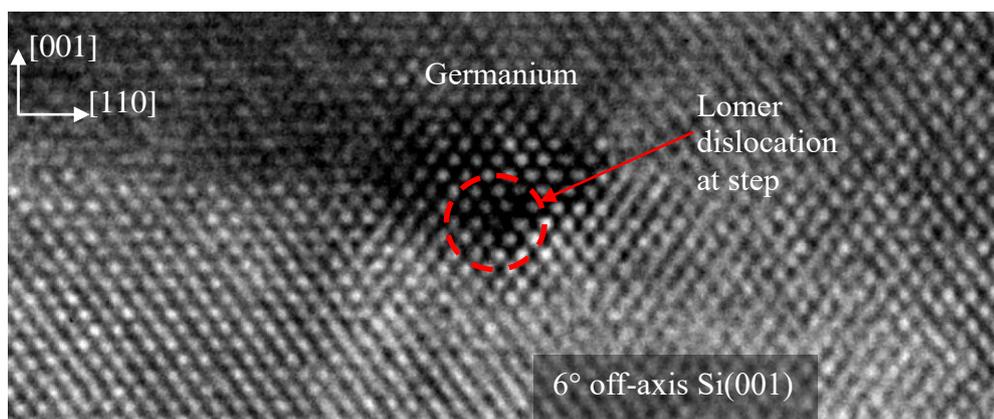


Figure 6.13: Magnified HR-XTEM image of the Lomer dislocation at the edge of a terrace in a red dashed circle from figure 6.12. The Burger's vector of the dislocation is pointing off the page

Figure 6.14 is a 50µm x 50µm tapping mode AFM micrograph of sample 15-208 and shows that the surface has a roughness of 1.64nm and height difference of 20nm. When examining all through stages, there is not much of a change in roughness. The facets

in the LT-Ge buffer did not affect the roughness significantly and the annealing only roughening the surface marginally with the presence of cross hatches. In sample 5-208, by depositing an additional HT-Ge layer at 650°C has not reduced the roughness of the surface significantly, as seen in figure 6.13.

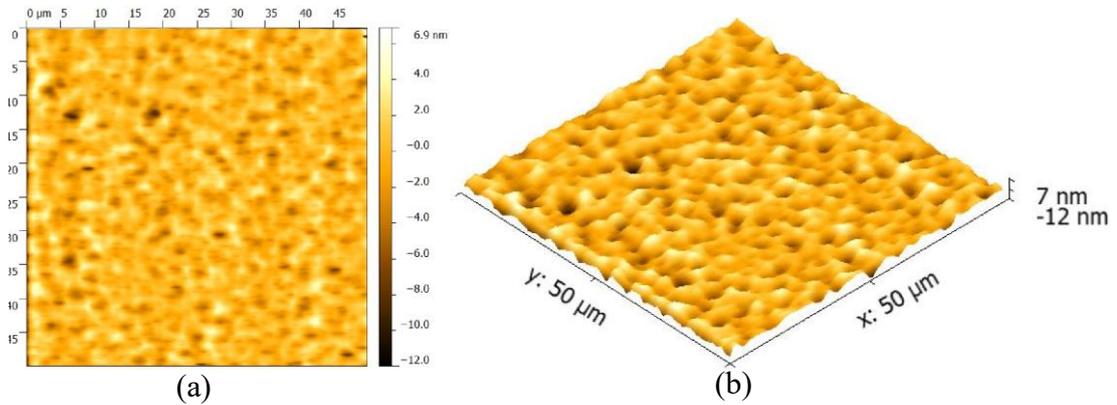


Figure 6.14: 50µm x 50µm Tapping mode AFM of sample 15-208: Anneal/HT-Ge/LT-Ge/6° Si(001). $R_{rms} = 1.64\text{nm} \pm 0.2\text{nm}$. Height = 20nm \pm 5nm.

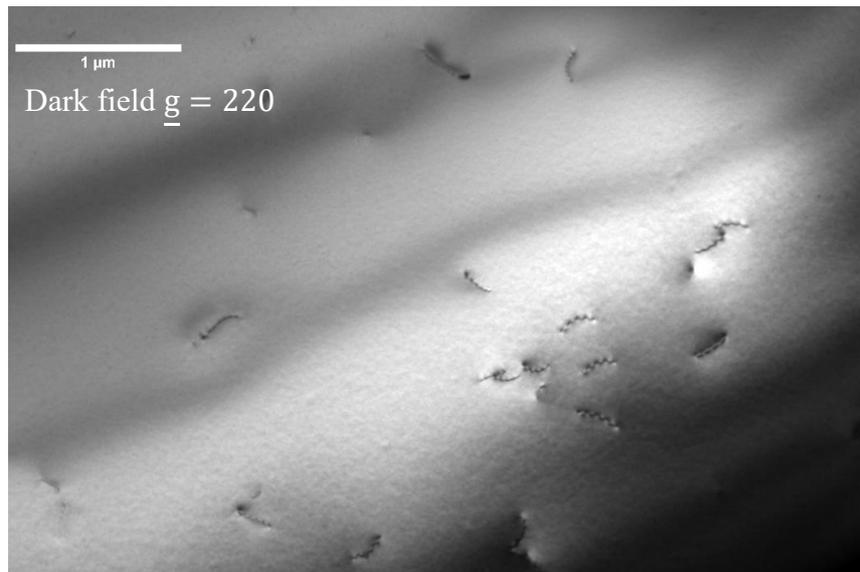


Figure 6.15: Plan view TEM image of sample 15-208: Ge/anneal/HT-Ge/LT-Ge/6° Si(001). Sample average TDD = $1.51 \times 10^8\text{cm}^{-2}$.

Plan view TEM shows that the TDD of sample 15-208 has not reduced significantly from sample 15-170, only by a factor x1.55, as seen in figure 6.15. As the HT layer is grown thicker the annihilation rate reduces, possibly following a power law function. The unequal stressing of {111} glide planes in off-axis substrate growth results in

asymmetrical dislocation annihilation hence when comparing LT/HT Ge buffer layers, sample 15-72 in chapter 5 which had a TDD of $6.19 \times 10^7 \text{ cm}^{-2}$ for a layer that is 930nm thick with sample 15-208 which is 881nm thick and has a TDD of $1.51 \times 10^8 \text{ cm}^{-2}$, it is seen that the off-axis buffer layer has x2 greater TDD.

6.3.2.3.1. HR-XRD of LT/HT Ge buffer layers on 6° off-axis Si(001)

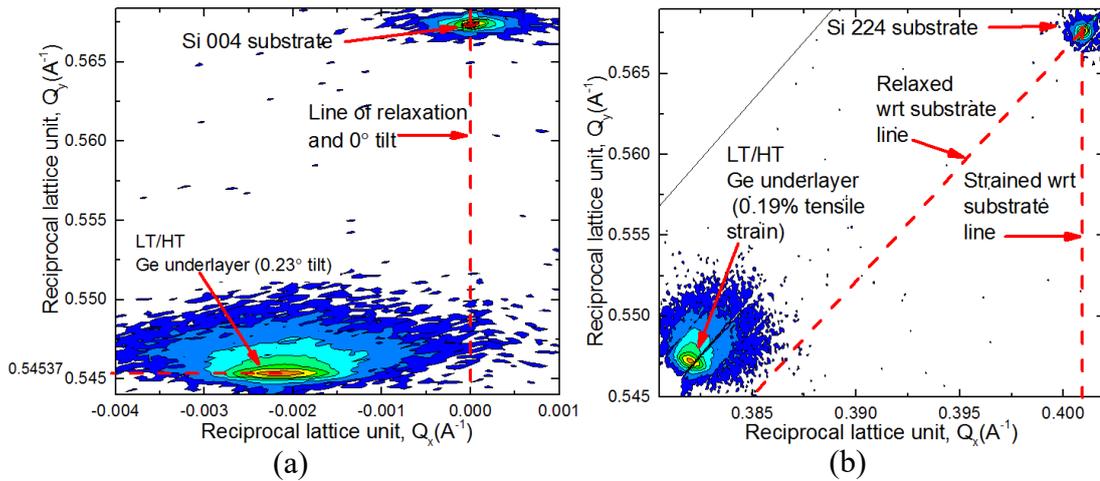


Figure 6.16: HR-XRD 004 and 224 RSMs of sample 15-208. In the (004) reflection the Q_y value of the Ge epilayer is 0.54537. The equivalent Q_y value for LT/HT Ge grown on on-axis Si(001) in figure 5.51 is 0.545264. The difference in Q_y values for the two buffer layers is 0.00011, therefore the strain in the two types of Ge buffer layers is the same within a margin of error.

For off-axis substrates the scattering plane lies along either the $[110]$ offcut direction or the $[\bar{1}10]$ direction. As mentioned in section 3.2.5, in the lab based HR-XRD RSM scans, the sample mounting orientation has to be considered in order to satisfy Bragg's law for the substrate for alignment. This means that the scattering plane projection angle, defined as being an angle between the x-ray scattering plane and the offcut direction, has to be either 0° or 90° depending on whether scattering was carried out along the $[110]$ direction or the $[\bar{1}10]$ direction respectively. For simplicity in alignment the $[110]$ direction was taken as the scattering plane in this investigation. Furthermore, depending on whether the $[110]$ direction was facing towards or away from the scanning incidence beam, the tilt of the RSM Bragg peak would be either to the right or left of the line of relaxation in both 004 and 224 reflections, thereby changing the sign of the tilt angle only and not the magnitude.

The tilt in the epilayer is 0.23° . When correcting for the tilt of the epilayer with respect to the substrate in the (004) reflection using equations 9.1 to 9.36 in the appendices, it is seen that there is no change in strain between Ge buffer layers grown on on-axis Si(001) or off-axis Si(001) In contradiction to the work carried out by Lee et al [171].

6.3.3. Annealing of LT-Ge buffer layer on 6° off-axis Si(001)

As was the case in chapter 4, successful annealing of thin LT-Ge buffer layers on on-axis Si(001) was found to be dependent on the thickness of the layer. Annealing 78nm thick layers grown at 400°C , for 1 min or 5 mins was found to have improved surface quality and lowered the TDD without causing inter-diffusion with the substrate. When annealing sample 15-172 (65nm thick and grown at 350°C on 6° off-axis Si(001)) for 10 mins at 650°C , X-TEM analysis shows that the misfit interface between the substrate and the epilayer is no longer a uniform straight line as seen in figure 6.17 and some diffusion from the substrate into the epilayer has started to take place. The 60° misfit dislocations in sample 15-172 have been converted into Lomer dislocations in sample 15-171 through annealing at 650°C , as seen in figure 6.18. HR-XRD was not carried out on the layer as it was very thin but it is reasonable to assume that some SiGe has formed in the layer and that it is not of pure Ge. In dark field X-TEM the layer is still revealed which means that it is crystalline and Lomer dislocations suggest some degree of tensile strain relaxation has taken place,

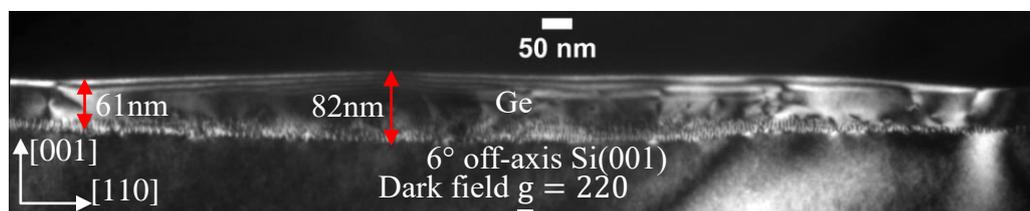


Figure 6.17: X-TEM of sample 15-171: 65nm Ge grown at 350°C on 6° off-axis Si(001) and annealed for 10 mins at 650°C . The misfit interface between the substrate and epilayer has been disturbed slightly and is no longer a uniform line. Given the faster diffusion coefficient of silicon, it appears that the substrate is starting to diffuse into the epilayer.

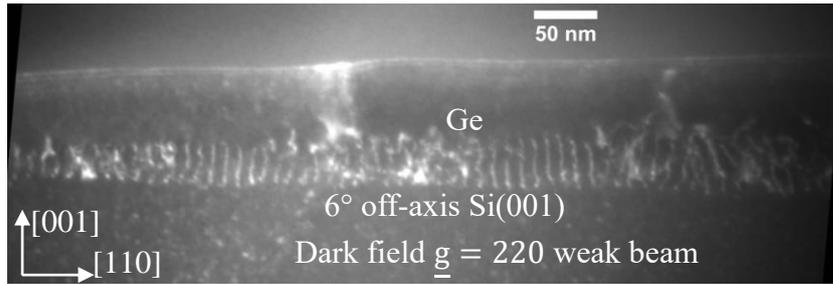


Figure 6.18: X-TEM of sample 15-171. Lomer dislocations can be seen at the interface. The maximum thickness measured in the (004) diffraction condition is 82nm and the minimum thickness is 61nm.

When the 65nm layer is annealed for 10 mins at 650°C, the R_{rms} increases to 3.89nm as shown in figure 6.19. This is also made evident in the X-TEM images in figures 6.17 and 6.18 which shows an undulated surface, due to the diffusion of the substrate into the epilayer. This suggests that annealing a 65nm layer, grown at 350°C, for 10 mins at 650°C does not improve the surface quality.

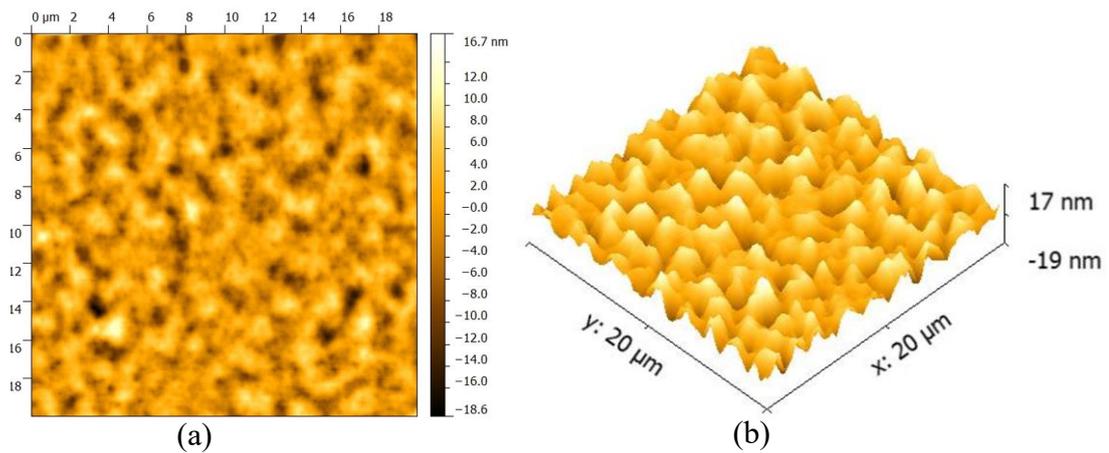


Figure 6.19: (220) 20 μ m x 20 μ m tapping mode AFM of sample 15-171. $R_{rms} = 3.89\text{nm} \pm 0.2\text{nm}$. Height = 34nm \pm 5nm.

Plan view TEM shows that the TDD has dropped. Initially sample 15-172 had an average TDD of $6.85 \times 10^{10}\text{cm}^{-2}$. Annealing at 650°C for 10 mins has dropped the TDD by x15 to $4.72 \times 10^9\text{cm}^{-2}$ whilst maintaining layer thickness to within 20nm.

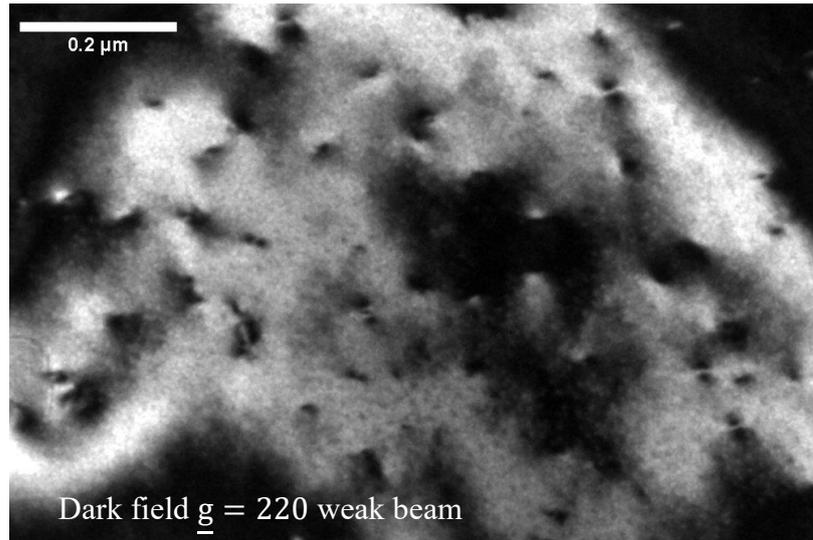


Figure 6.20: Plan view TEM of sample 15-171. Sample average TDD = $4.72(+/-0.47) \times 10^9 \text{cm}^{-2}$.

6.4. Reverse terrace graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers on on-axis and 6° off-axis Si(001)

The aim of this 2nd sub investigation into off-axis growth is to see how reverse terrace grading of $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ affects the material properties of the buffer layer when grown on an off-axis substrate. RTG buffer layer structures are also grown on on-axis Si(001) to similar Ge contents for comparison.

Additionally, reverse terrace grading will also be compared to reverse linear grading on off-axis substrates. In Chapter 5, section 5.4, wafers 13-162 and 13-163 are RLG buffers grown on 6° off-axis Si(001). The LT/HT Ge underlayer is 555nm. These samples will be used to investigate strain effects on sticking coefficient and tilt in the $\text{Si}_{1-x}\text{Ge}_x$ buffer layer when growing on off axis substrates.

The Ge buffer layer is grown using the LT(350°C)/HT(550°C) process to between 820nm and 1200nm total thickness. The $\text{Si}_{1-x}\text{Ge}_x$ layer is reverse terrace graded to between $0.764 \geq x \geq 0.723$. GeH_4 and SiCl_2H_2 are used as the precursors at 850°C growth temperature under H_2 carrier gas. 10 sccm of HCl is used as well during growth, because the buffer layers are expected to grow beyond 6μm thickness and therefore significant deposition on the chamber wall is likely to occur. Deposition on the

chamber wall will prevent infra-red radiation from the lamps reaching the wafer surface and thus affect growth conditions.

HCl gas was not included in figure 2.10, in section 2.4.1.1 on SiGe growth in RP-CVD, nor was a chemical equation written to describe the reaction taking place because it was not used in the majority of samples grown in this study. HCl gas is already generated through the desorption of chlorine species from the surface and reaction with H_2 carrier gas as well as with the hydrogen on the passivated substrate surface shown by equations 2.19 and 2.17 respectively. Introducing additional HCl gas increases its concentration in the chamber and pushes the system into the etching regime. The value of n in equation 2.30 is expected to increase with the additional HCl and this will slightly reduce the overall SiGe epilayer growth rate as well [174].

6.4.1. Reverse terrace graded $Si_{1-x}Ge_x/Ge$ buffer design

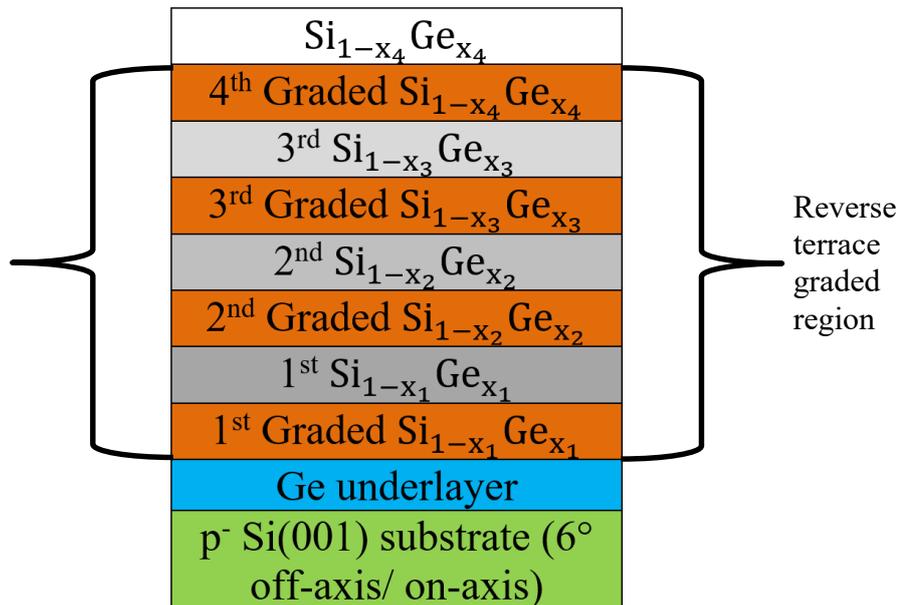


Figure 6.21: Reverse terrace graded $Si_{1-x}Ge_x/Ge$ buffer structure on either Si(001) on axis or 6° off-axis for buffer layers reverse terrace graded in the range of $0.72 \leq x \leq 0.764$ Ge \pm 0.5%. The LT/HT Ge underlayer was between 820 and 1190 nm measured through X-TEM in the (004) diffraction condition

Wafer ID	Ge composition ($\pm 0.5\%$)	Average grading rate (% Ge/ μm) ($\pm 5\%$)	Strain in Ge underlayer wrt itself (%)	Thickness in Ge underlayer nm ($\pm 50\text{nm}$)	Total thickness of buffer (nm) ($\pm 30\text{nm}$)	Cap strain (%) ($\pm 0.5\%$)
13-053	0.764	8.19	0.218	820	5920	0.194
13-054	0.752	8.10	0.174	1140	6440	0.216
13-055	0.741	8.83	0.155	1090	6540	0.203
13-085	0.756	8.39	0.187	1190	6380	0.234
13-086	0.756	8.33	0.157	1150	6840	0.199
13-087	0.750	7.59	0.189	1160	6990	0.232

Figure 6.22: List of reverse terrace graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer samples grown on 6° off-axis Si(001).

Growth of RTG layers is similar to RLG layers in terms of pressures, temperatures and flow rates as described in chapter 5. The only difference being that the flow of SiCl_2H_2 is held constant at intervals during the ramp up to create the constant composition layers. Figures 6.22 and 6.23 are tables listing all of the samples grown off-axis and on-axis respectively in this investigation. The samples highlighted in yellow and red in both tables are comparable in terms of Ge composition. Due to the difficulties in distinguishing between the constant composition and graded regions in the buffer layers in 004 TEM images, it was not possible to determine the effective grading rate from X-TEM image analysis alone and so an average grading rate was determined across the terrace graded region and then using equation 6.2 the effective grading rate calculated. The average grading rates all lay under $8.5\% \text{Ge}/\mu\text{m}$ and agreed within 2% of each other. The effective grading rate for all of the RTG buffer layers in this investigation were approximately $15\% \text{Ge}/\mu\text{m}$.

Wafer ID	Ge composition (%) ($\pm 0.5\%$)	Average grading rate (% Ge/ μm) ($\pm 5\%$)	Strain in Ge underlayer wrt itself (%)	Thickness in Ge underlayer nm ($\pm 50\text{nm}$)	Total thickness of buffer (nm) ($\pm 30\text{nm}$)	Cap strain (%) ($\pm 0.5\%$)
13-088	0.752	6.72	0.170	1160	7360	0.199
13-089	0.737	6.96	0.189	1190	7550	0.212
13-090	0.723	7.26	0.152	1160	7630	0.194

Figure 6.23: List of reverse terrace graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer samples grown on on-axis Si(001).

6.4.2. Thickness comparison between on and off-axis buffer layers.

X-TEM thickness measurements indicate that Ge/Si_{1-x}Ge_x buffer layers grown on off-axis silicon are approximately 15% thinner than those grown on on-axis silicon. Figure 6.24 is an image of an off-axis buffer layer (sample 13-054) and figure 6.25 is an image of an on-axis buffer layer (sample 13-088), both are reverse graded to 75.2% Ge. A total buffer layer thickness difference can be seen in the two samples, of 920nm +/-50nm. Sample 13-088 has a thicker graded region than sample 13-054 by about 630nm +/-50nm.

In section 2.4.3.1, growth on offcut substrates was discussed and figure 2.23 shows how the dangling bond density varies for different planes on Si and how the subsequent growth rate also varies. The (001) plane was shown to have the fastest growth rate and all other planes have a growth rate which is a fraction of this value. The (110) plane has a dangling bond density of $\frac{1}{\sqrt{2}}$ times less than Si(001). The sticking coefficient on each plane is also dependent on other parameters such as an inverse relationship with temperature, the rate of desorption of H₂ which is lower on the (110) and (111) planes [175] and also the Ge content of the layer [176].

It is suspected that the thinner layers grown on off-axis substrates is caused by the anisotropic dangling bond density. The sticking coefficient is changing throughout the heterostructure, particularly in the terrace graded region and so it was not possible to determine quantitatively the expected growth rates in the different sections of the RTG buffer in this investigation. Undoubtedly, tensile strain relaxation in the reverse graded structure provides a faster growth rate due to smoother layers, as seen in chapter 5.

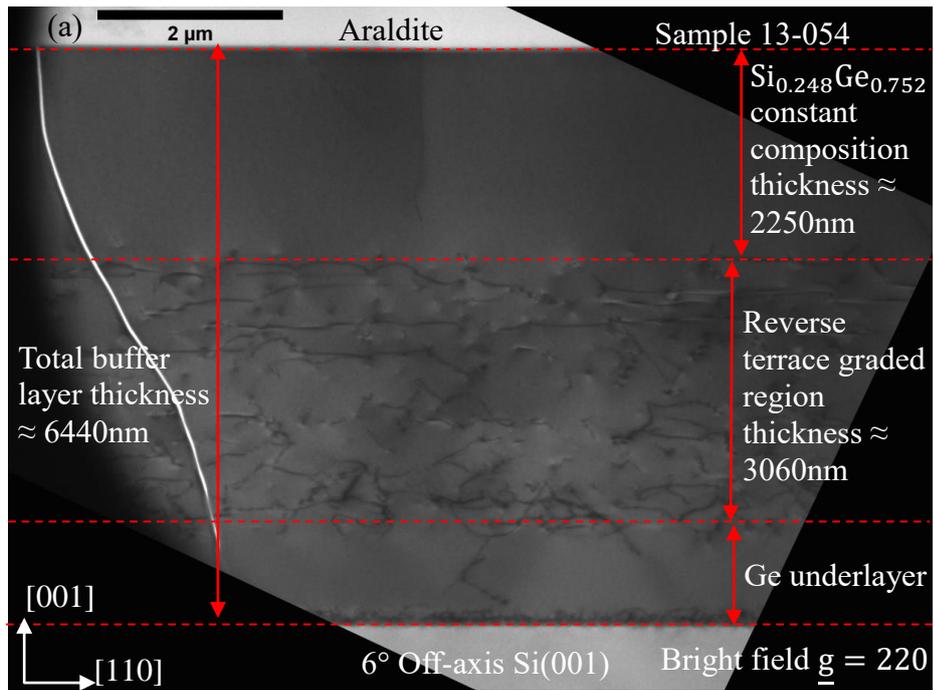


Figure 6.24: X-TEM of sample 13-054: $\text{Si}_{0.248}\text{Ge}_{0.752}/\text{Ge}$ RTG buffer layers on off-axis Si(001). On the whole off-axis RTG buffer layers were 14% thinner than on-axis buffer layers. Cracks were observed in both types of RTG buffer layer however a crack investigation was not carried out in this chapter.

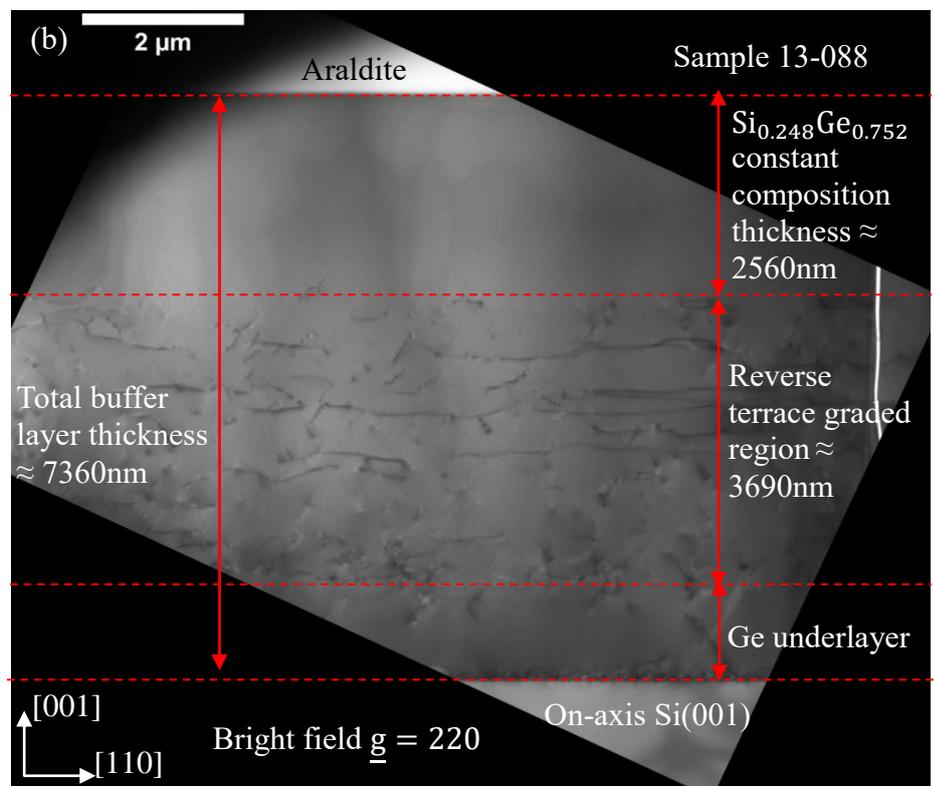


Figure 6.25: X-TEM of sample 13-088: $\text{Si}_{0.248}\text{Ge}_{0.752}/\text{Ge}$ RTG buffer layers on-axis Si(001). The terrace graded region was estimated from the misfit network. A smooth surface can be seen in the buffer layer due to tensile strain relaxation.

6.4.3. Threading dislocation density comparison.

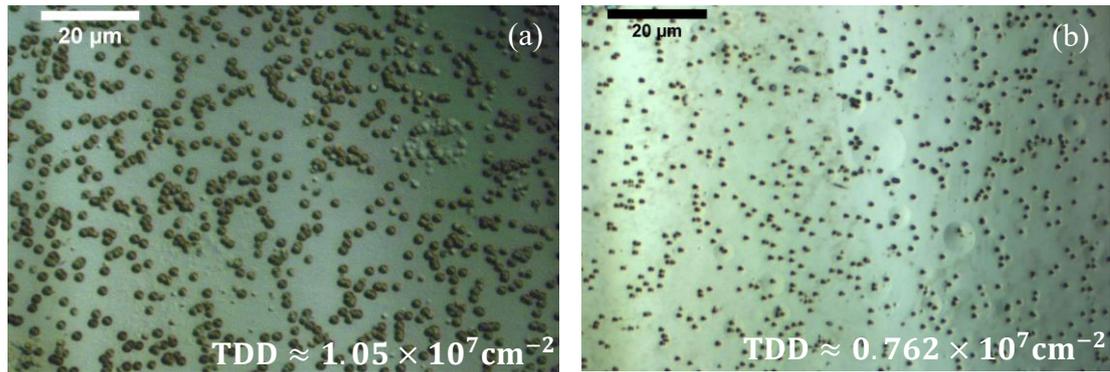


Figure 6.26: (a) 2min 30sec Schimmel etch and DIC optical microscopy image of sample 13-054: $\text{Si}_{0.248}\text{Ge}_{0.752}/\text{Ge}$ RTG buffer layer on off-axis Si(001) and (b) 2min Schimmel etch and DIC optical microscopy image of sample 13-088: $\text{Si}_{0.248}\text{Ge}_{0.752}/\text{Ge}$ RTG buffer layer grown on on-axis Si(001).

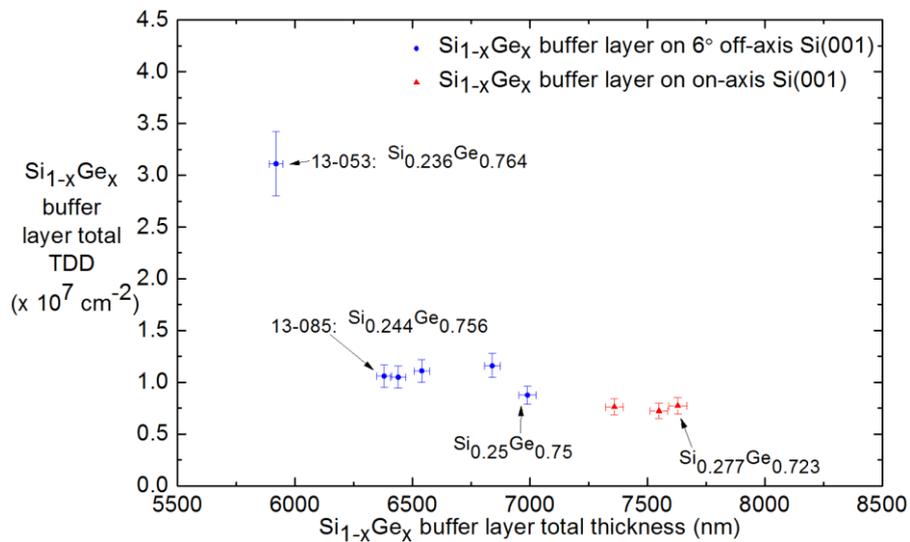


Figure 6.27: TDD as a function of $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$. The Ge content for all buffers is in the range: $0.72 < x < 0.764$.

Ge grown on off-axis substrates had a noticeably higher TDD than equivalent samples grown on-axis, explained earlier by the unequal stressing of the $\{111\}$ glide planes on offcut substrates. Figure 6.27 shows how TDD varies with total RTG buffer layer thickness. A noticeable drop in TDD is seen from sample 13-053 to sample 13-085 by approximately a factor of x3. The HT/LT Ge underlayer measured in sample 13-053 was 820nm +/- 50nm and the thickness of the HT layer has been estimated to have a reciprocal relationship with TDD, possibly following a power law function. It is

therefore surmised that the starting TDD in the Ge underlayer in sample 13-053 is the highest in all of the off-axis RTG buffer layers.

The on-axis buffer layers had an average Ge underlayer thickness of 1175 nm +/- 50nm. If a starting TDD in the underlayer is assumed to be approximately $6 \times 10^7 \text{cm}^{-2}$ (based on sample 15-72 in chapter 5: 930nm HT/LT Ge on on-axis Si(001)) then the RTG layer has reduced the TDD in the constant composition SiGe layer by approximately x10. Similarly, with Ge buffer layers on off-axis substrates if the starting TDD is assumed to be approximately $2 \times 10^8 \text{cm}^{-2}$ (based on sample 15-208 earlier in this chapter) then a reduction by a factor of x10 has also been observed in the SiGe layer in the off-axis RTG buffer layers. Therefore it is concluded that the RTG buffer layer in both off and on axis Si(001) has the same effect in reducing TDD. This effect is presumed to be multiplication and annihilation of threading dislocations through glide from the additional strain. The low average and effective grading rates, probably create insufficient strain in the RTG graded layer to annihilate TDD further than x10 but the constant composition layers in the terraced region and in the top constant composition layer aides in dislocation glide. From figure 6.27, it is presumed that a kinetic limit is present to annihilation. From figure 6.27 it is also seen that on-axis buffer layers have a slightly lower TDD, most likely because they are thicker overall.

6.4.4. Strain comparisons between on-axis and off-axis $\text{Si}_{1-x}\text{Ge}_x$ buffer layers.

Earlier in this chapter it was shown that for LT/HT Ge buffer layers grown on off-axis Si(001) at similar temperature conditions to on-axis grown LT/HT Ge buffer layers, the strain is identical at 0.2% +/-0.03%. However due to the asymmetrical stressing of the {111} glide planes the tilt component of 60° misfit dislocations is not nullified and also a small tilt component exists for Lomer dislocations. Therefore, the Ge film grown off-axis is tilted by about $0.23^\circ \pm 0.05^\circ$.

When reverse terrace grading $\text{Si}_{1-x}\text{Ge}_x$ on top of the Ge buffer layer off-axis, it is seen that there is an increase in tilt. In fact, as can be seen in figure 6.28 the tilt increases per constant composition terrace. The maximum tilt is obtained in the top constant composition $\text{Si}_{1-x}\text{Ge}_x$ layer and from all of the off-axis samples, the average maximum tilt in the constant composition $\text{Si}_{1-x}\text{Ge}_x$ terrace is measured to be $0.43^\circ \pm 0.05^\circ$ as seen in the plot of figure 6.30.

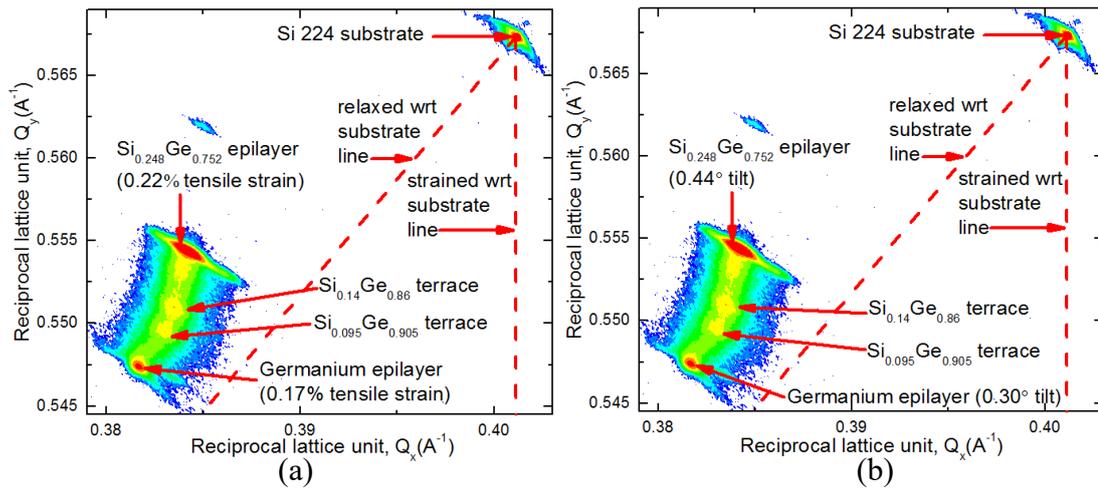


Figure 6.28: (a) 004 and (b) 224 HR-XRD RSMs of sample 13-054: $\text{Si}_{0.248}\text{Ge}_{0.752}/\text{Ge}$ RTG buffer layer.

When compared to equivalent RTG structures on on-axis $\text{Si}(001)$ the average tilt in the Ge underlayer is negligible at $0.003^\circ \pm 0.004^\circ$ and so is the average tilt in the top constant composition $\text{Si}_{1-x}\text{Ge}_x$ layer at $0.005^\circ \pm 0.005^\circ$. The 224 RSM alone in figure 6.28 would indicate that an increase in strain should appear in the RTG SiGe layers since the peaks are moving away from the substrate relaxation line. However, this is false. After correcting for tilt using the (004) reflection and calculating the true in-plane and out-of-plane lattice constants using equations 9.1 to 9.36. (in chapter 9 the appendices) it is seen that for samples reverse terrace graded to identical compositions of Ge on off-axis substrates, the strain in the $\text{Si}_{1-x}\text{Ge}_x$ layer is identical to those grown on-axis, at $0.2\% \pm 0.03\%$. This is seen when comparing the RSMs of sample 15-054 in figure 6.28 with sample 15-088 in figure 6.29, where both samples have been reverse terrace graded to $\text{Si}_{0.248}\text{Ge}_{0.752}$.

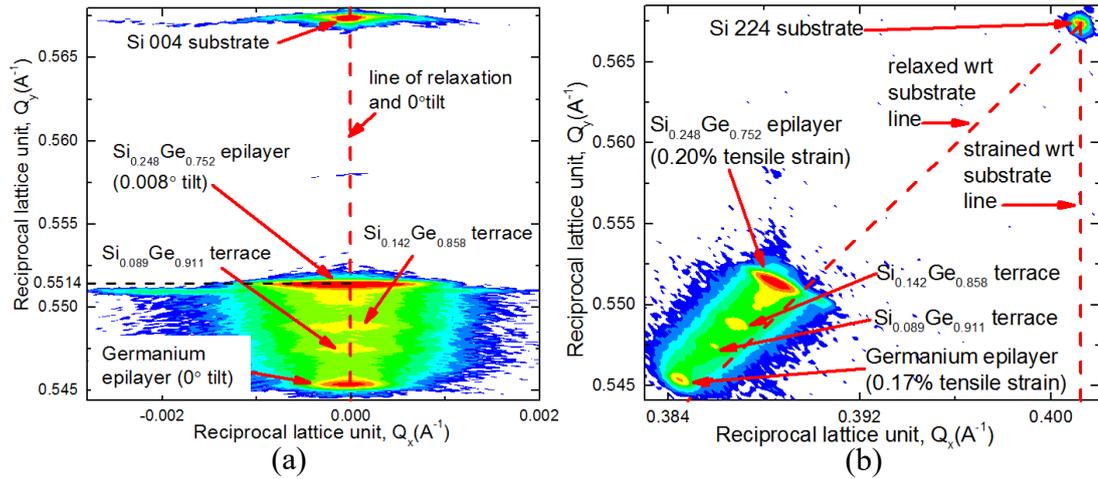


Figure 6.29: (a) (004) and (b) (224) HR-XRD RSMs of sample 13-088: $\text{Si}_{0.248}\text{Ge}_{0.752}/\text{Ge}$ RTG buffer layer.

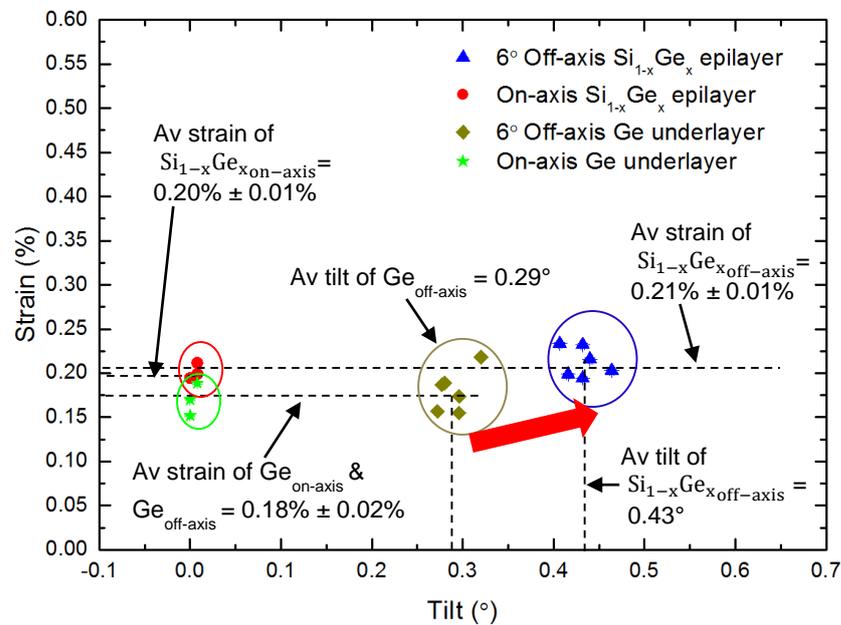


Figure 6.30: Tilt vs strain in Ge underlayer and $\text{Si}_{1-x}\text{Ge}_x$ buffer layers grown on 6° off-axis and on-axis $\text{Si}(001)$ substrates.

In chapter 5, section 4 two RLG samples (13-162 and 13-163) were grown on 6° off-axis $\text{Si}(001)$. However, unlike the RTG process, with the RLG process it is noticed that the top constant composition $\text{Si}_{1-x}\text{Ge}_x$ layer has the same degree of tilt as the Ge underlayer. Figure 5.27 shows the RSMs of sample 13-162, which was reverse linearly graded to $\text{Si}_{0.292}\text{Ge}_{0.708}$ from a 555nm HT/LT Ge underlayer. The strain in the $\text{Si}_{0.292}\text{Ge}_{0.708}$ layer is 0.22% and the tilt is also $0.221^\circ \pm 0.05^\circ$. The increase in tilt from Ge buffer layer to $\text{Si}_{1-x}\text{Ge}_x$ layer in RTG buffer layers is explained by dislocation multiplication taking place in the graded regions. The high grading rate in

the RTG graded regions cause multiplication of 60° misfit dislocations via the Frank-Read process, this leads to a greater overall tilt component and causes greater asymmetrical strain relaxation. Further investigations are required to confirm this. The increased degree in tilt in RTG buffer layers does not seem to affect the in-plane lattice constant of the SiGe since the strain is still 0.2% hence the same degree of tetragonal distortion takes place in the layer.

6.4.5. Surface morphology in RTG $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers.

Tensile strain relaxation provides smooth surfaces in reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers, provided that the grading rate is below $61\% \text{Ge}/\mu\text{m}$ [96], as was seen in chapter 5. The RTG buffer layers grown on off-axis Si(001) in this investigation showed smooth surfaces, with R_{rms} of under $2.2\text{nm} \pm 0.2\text{nm}$. This is comparable to RTG buffer layers grown on on-axis Si(001) to at $2\text{nm} \pm 0.2\text{nm}$ and comparable to work carried out by Shah et al on reverse terrace grading down to 75% Ge [173]. Figure 6.31 is a contact mode AFM micrograph of sample 13-054. The cross hatching effects can be seen on the surface due the $\langle 110 \rangle$ direction misfit dislocations in the terrace graded region.

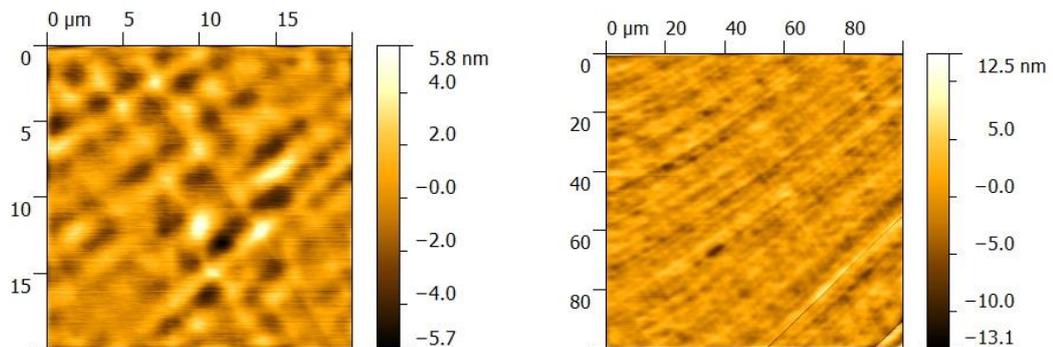


Figure 6.31: (a) $20\mu\text{m} \times 20\mu\text{m}$ and (b) $100\mu\text{m} \times 100\mu\text{m}$ contact mode AFM micrograph of sample 13-054: RTG buffer layer on off-axis Si(001). $R_{\text{rms}} \approx 1.64\text{nm}$.

6.5. Chapter 6: Summary

In this chapter pure Ge buffer layers and reverse terrace graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers have been grown on 6° off-axis Si(001) substrates to be used as virtual substrates for the epitaxy of III-V materials.

In the first part of this investigation a high quality Ge buffer layer was created on Si(001) using the LT/HT approach. HR-XRD (004) RSM shows that the buffer layer is tilted with respect to the substrate by $0.23^\circ \pm 0.05^\circ$ and (224) asymmetric scans show that upon correction for tilt, the in and out-of-plane lattice constants are identical to an equivalent LT/HT Ge buffer layer grown on on-axis Si(001). Current state of the art the Ge buffer layers using the two temperature approach use 400°C for the LT ‘seed’ layer up to 100nm thick followed by a 600°C to 670°C HT layer and annealing between 800°C and 830°C . In chapter 4, 350°C growth on on-axis Si(001) had shown to provide smooth epilayers, with majority 60° misfit dislocations at the interface, until severe faceting takes place at some point between 95nm and 174nm thick layers. Therefore, in this study 350°C was used as the growth temperature for the seed layer up to 65nm thick on 6° off-axis substrates. The epilayer surface showed a similar R_{rms} to an on-axis Ge buffer layer grown at the same temperature to a similar thickness; 1.21nm and a TDD of $6.85 \times 10^{10}\text{cm}^{-2}$. It was discovered that annealing the 65nm thick LT layer for 10 mins caused the beginning of substrate diffusion into the epilayer as witnessed in chapter 4. Annealing the LT layer reduced the TDD by a factor of x14 however the diffusion process had disrupted the misfit interface and undoubtedly caused the creation of SiGe in the epilayer but since the epilayer was so thin this could not be confirmed through HR-XRD. Therefore, the solution was to grow a HT layer at 550°C up to a thickness of 461nm and then anneal at 650°C for 10mins. This had the effect of improving crystalline quality, promoting glide of Lomer dislocations along (001) and dropping the TDD by a factor of x300 by promoting glide of 60° misfit dislocations. A further 355nm HT layer was deposited at 650°C to promote more glide and further reduce the TDD to final value of $1.51 \times 10^8\text{cm}^{-2}$. The unequal stressing of {111} glide planes sees TDD increase marginally in off-axis buffer layers compared to equivalent layers grown on axis, therefore compared to the latest thick state of the art LT/HT Ge buffer layers grown on axis the TDD is marginally higher [141] but within the expected TDD for state of the art layers grown off-axis [170].

The over relaxation means that the in-plane lattice constant of the buffer layer is the same as bulk Ge crystals and as explained earlier, the Ge epilayer is not lattice matched to GaAs. The over relaxation, however will serve to reduce the lattice mismatch between Ge and other III-V materials such as AlSb and InSb for lattice mismatched epitaxy. Ge serves as a good buffer layer for InSb because of the similarity in thermal expansion coefficient between the two materials, as will be detailed in the next chapter.

The second investigation involved the development of reverse terrace graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers on 6° off axis Si(001) substrates. Previously in chapter 5 two forms of reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers were investigated. The RLG technique yielded smooth surfaces even when reverse grading down to 45% Ge however, threading dislocation densities remained at between 4 and $7 \times 10^7 \text{ cm}^{-2}$. Previous studies have shown that reverse terrace grading in both linearly graded and reverse linearly graded buffer layers have reduced TDD densities whilst providing smooth surfaces. Reverse terrace grading was investigated as a means to reduce TDD whilst keeping smooth surface brought on by tensile strain relaxation.

In this study it was discovered that when reverse terrace grading on either on-axis or 6° off-axis substrates at identical growth conditions and low grading rates, both the Ge and $\text{Si}_{1-x}\text{Ge}_x$ epilayers are under the same amount of strain (0.2% tensile strain), however layers grown off-axis are tilted with respect to the substrate. The epilayer heterostructures grown off-axis were found to be 15% thinner than those grown on-axis. The reduced buffer layer thicknesses are caused by additional planes being made available on the offcut substrate, such as the (110) plane. The different planes have different dangling bond densities with varying growth rates. This creates growth anisotropy where growth occurs fastest on the (001) plane compared to the others.

A thicker LT/HT Ge layer helped to reduce the starting TDD however it was determined that RTG regions for both off-axis and on-axis samples were equally as effective in reducing the TDD in the SiGe constant composition layer by a factor of $\times 10$. When comparing RLG buffer layers with RTG buffer layers, it was found that reverse terrace grading increased the tilt in the top $\text{Si}_{1-x}\text{Ge}_x$ layer to $0.43^\circ \pm 0.05^\circ$

whilst RLG buffers layers maintained the same 0.23° degree tilt from the Ge underlayer. The reason for this is presumed to be Frank-Read multiplication in the graded sections of the RTG region, where the high grading rate causes 60° dislocations to multiply thereby increasing the vertical component. It is presumed that this multiplication process is responsible for producing a higher TDD in off-axis samples as the $\{111\}$ planes are stressed unequally. The increased degree of tilt in the SiGe buffer layer did not affect the in-plane lattice constant and so the findings in this investigation will pave the way to reverse terrace grading on off-axis Si(001) to lower Ge content layers for lattice matched integration of GaP and AlP or even strained GaAs integration for high electron mobility transistors.

7. SS-MBE deposition of InSb on Ge/Si(001) virtual substrate

7.1. Background to InSb epitaxy on Si(001)

InSb has the highest high electron mobility of any of the III-V compound semiconductors at $77,000 \text{ cm}^2/\text{Vs}$. This makes this material very useful in manufacturing high electron mobility transistors, operating at 100's of GHz and low operating voltage for CMOS circuits [177]. InSb has a direct bandgap which is also the narrowest of all of the III-V materials; at 0.17eV. This also makes this material particularly attractive for mid to near IR and magnetic sensors and thermophotovoltaics [21], but should preferably be grown on IR transparent substrates for best efficiency.

Figure 1.2 is a graph that shows lattice constant plotted against bandgap and wavelength for a number of semiconductors, including III-V materials. InSb has the highest lattice mismatch to Si in that plot of approximately 19.3% at room temperature. The lattice mismatch for InSb to Ge is slightly lower at 14.5%. This means that InSb cannot be 'lattice matched' grown on a Si(001) wafer using any composition of $\text{Si}_{1-x}\text{Ge}_x$ buffer layer. InSb also has a thermal expansion coefficient (CTE) mismatch to silicon with the $\text{CTE}_{\text{Si}} = 2.61 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$ and $\text{CTE}_{\text{InSb}} = 5.37 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$, meaning that high temperature growth will cause expansion of the layer and transition the layer from marginally compressive to tensile strain (as was seen in the Ge buffer layers in chapter 4), however since the InSb melting temperature is much lower than Ge at 527°C, it is difficult to supply enough thermal budget to the layer to achieve this without the layer melting.

The earliest cited work carried out into InSb epitaxy on Si(001) is in 1986 by Yata [178], where MBE was used to deposit several monolayers of InSb at a temperature range of 366.85°C and 546.85°C on Si(001) 2x1 dimer surfaces. The substrate temperature affected the deposition process and it was discovered that below 366.85°C nucleation and growth of antimony occurs. It was discovered for antimony growth to take place above 426.85°C, In atoms have to be present on the surface and that the Sb_4 ceramic molecules have to dissociate to form Sb_2 to react with In to form InSb clusters.

Between 176.85°C and 426.85°C growth temperatures Sb_4 molecules bond to the surface without the presence of In.

GaAs has been investigated as an alternative buffer layer to Ge because it has a similar lattice constant to bulk Ge and a similar thermal expansion coefficient to both Ge and InSb as listed in table 2.3 in section 2.3.2. The polar nature of GaAs is also noted to be useful in minimising inversion domain boundaries in InSb layer. Work carried out by Rao et al in 1988 investigated the heteroepitaxy of InSb using metalorganic magnetron sputtering on MBE grown GaAs/Si(001) virtual substrates and found lower defect densities in the InSb layer than if it were grown by MBE [179].

GaAs (001) substrates have alternatively been used by several groups, including very recently by Jia et al [180] to grown 730nm thick InSb layer that 100% strain relaxed and with a R_{rms} of 1.1nm, but the room temperature electron mobility has been measured to have dropped to 33,840 cm^2/Vs most likely due to the high density of defects in the epilayer. Lomer edge dislocations were observed at the InSb/GaAs interface due to high strain relaxation. Another study by D'Costa et al in 2015 investigated the optical properties of InSb grown on GaAs(001) substrates using SS-MBE [181] and through spectroscopic ellipsometry experiments was found to have similar quality to bulk InSb.

In a study carried out by Tran et al in 2008 on growth of InSb on Si(001), a GaSb/AlSb super lattice was deposited first on a 4° off-axis p- Si(001) substrate [182]. Initially the substrate was heated to 820°C to remove the native oxide, but shows a 2x4 surface reconstruction. After increasing the baking temperature to 1015°C, a 2x1 reconstruction appeared which suggested that double atomic, single domain steps appeared. The 30 period 1nm GaSb/ 1nm AlSb super lattice was grown at between 300°C and 420°C. The In/Sb flux ratio was set at 5 and after the growth of the 2 μm InSb layer the temperature was brought down to 200°C under a constant Sb flux. HR-XRD rocking curves shows that the InSb 004 peak is narrowest and has FWHM of 951 arcseconds when the growth temperature was set to 420°C. This indicates lower defect densities in the InSb layer at this temperature. XRD also showed that the InSb had an in-plane lattice constant of 6.48Å indicating very slight over relaxation. The surface roughness

was measured to be lower than 16nm for samples grown within the temperature range. Further to this study Dobbert et al showed that without the presence of the GaSb/AlSb super lattice, stacking faults and microtwins are generated at the interface in high density [183] and Hall effect measurements showed that the room Temperature electron mobility of the 2 μ m thick layer is 26,000 cm²/Vs.

Ge has been used in previous studies as a buffer layer for the growth of InSb on on-axis Si(001) because the CTE mismatch between InSb and Ge is much lower with $CTE_{Ge} = 5.84 \times 10^{-6} \text{ } ^\circ\text{C}^{-1}$. In 1997 Mori et al first proposed and used Ge buffer layers on Si(001) for InSb growth [184]. MBE was used for both Ge buffer and InSb growth at 5×10^{-9} Torr. The substrates were baked at 950 $^\circ\text{C}$ for 30 mins to remove the native oxide. The Ge buffer layer was grown at 400 $^\circ\text{C}$ up to 400nm thick and then annealed at 800 $^\circ\text{C}$ for 10 mins. The InSb was then deposited between 250 $^\circ\text{C}$ and 370 $^\circ\text{C}$, at an Sb/In flux ratio of between 1 to 6. The temperature of the In source was kept at 800 $^\circ\text{C}$ and the Sb source was kept at 360 $^\circ\text{C}$. The thickness of the InSb layer ranged from 800nm to 1200nm, and it was found that the quality of the InSb is heavily dependent upon the thickness of the Ge underlayer as well as an optimum flux ratio of 4.5 and 300 $^\circ\text{C}$ growth temperature.

Finally, AlSb has also been used as buffer layer on Si(001) for InSb epitaxy. AlSb has a 13% lattice mismatch to Si(001) and has a 5.6% lattice mismatch to InSb. It is however not a direct band gap semiconductor. It has band gap of 1.615eV and also reasonably low electron and hole mobilities at room temperature as shown in table 2.4 in section 2.3.2. The thermal expansion coefficient of AlSb is $4.2 \times 10^{-6} \text{ } ^\circ\text{C}^{-1}$ which is $1.609 \times CTE_{Si}$ and not as large as the CTE mismatch between Si and Ge. In 2003 Mori et al also investigated InSb films grown on AlSb/Si(001) via MBE [185]. The same substrate preparation conditions were used as with Ge buffer film deposition in the previous paragraph, however the AlSb was deposited to 300nm thickness at 520 $^\circ\text{C}$ with an Sb/Al flux ratio of about 3.0. The R_{rms} of the surface of the AlSb/Si(001) virtual substrate was 1.7nm. The InSb was grown at between 180 $^\circ\text{C}$ and 430 $^\circ\text{C}$ with a fixed Sb/In flux ratio of 4.7. HR-XRD 004 rocking curves showed that the InSb peak is strongest at 330 $^\circ\text{C}$ growth temperature, indicating strong monocrystalline crystalline growth. When compared to InSb growth on Ge buffer layers, the results implied that

AlSb has a much wider growth temperature window. Due to the thermal mismatch between AlSb and InSb, cracks were detected using AFM on InSb surface, when the InSb growth temperature was above 400°C. In 2007 Mori continued this investigation of AlSb buffer layer thickness and its effect on the InSb epilayer [186]. The MBE grown AlSb thickness varied between 8nm to 250nm at 520°C growth temperature. The Sb/In flux ratio used was 3.0 at 400°C growth temperature. 900nm of InSb was grown. AFM showed that as the thickness of the AlSb buffer layer increased the density and diameter of InSb Stranski-Krastanov islands increased as well. HR-XRD 002 scans showed that preferential growth of InSb occurred on {001} planes and that a strong InSb signal was achieved at 40nm AlSb thickness. It was discovered that at 8nm of AlSb buffer layer, heteroepitaxial growth of InSb can be achieved but the InSb is polycrystalline. 40nm of AlSb buffer layer, better quality, crack-free InSb can be grown. Hall effect measurements showed that the room temperature electron mobility of the InSb layer grown on 40nm AlSb/Si(001) is 6000 cm²/Vs and the room temperature electron mobility of the InSb layer grown on 250nm AlSb/Si(001) is 8000 cm²/Vs.

7.2. This study on SS-MBE InSb deposition on RPCVD Ge/Si(001) virtual substrate.

Material heterostructure (substrate/epilayer)	Mismatch (%)
Si(001)/Ge	4.2
Si(001)/AlSb	12.97
Si(001)/InSb	19.3
Bulk Ge/InSb	14.52
Tensile strained Ge/InSb	14.33
Bulk Ge/AlSb	8.44
Tensile strained Ge/AlSb	8.26
AlSb/InSb	5.6

Figure 7.1: Table listing lattice mismatch of Si, Ge, AlSb and InSb heterostructure arrangements. The arrows indicate the gradual reduction in lattice mismatch from Si(001) to InSb.

Figure 7.1 is a summary table of the lattice mismatch between Si, Ge, AlSb and InSb heterostructure combinations. With 0.2% tensile strained LT/HT Ge buffer layers, the in-plane lattice constant is marginally higher hence its lattice mismatch to AlSb and InSb is marginally smaller. By using both a Ge buffer layer and an AlSb buffer, the strain due to the 19.3% lattice mismatch between InSb and Si(001) can be released gradually.

The aim in this chapter is to use the high quality RP-CVD grown 6° off-axis Ge/Si(001) virtual substrate (sample 15-208 in chapter 6) to obtain as high a quality InSb epilayer as possible using SS-MBE. AlSb will be used as a secondary buffer layer on the Ge to reduce the lattice mismatch further. A Veeco Gen II MBE system was used. High purity Aluminium, Indium and Antimony were used as source materials. The substrate holder only accepts 500mm diameter wafer therefore the Ge/Si(001) virtual substrates had to be cleaved into quarters, as described in section 3.1.2 on TEM sample preparation, where the wafer is cleaved parallel to the (110) face first in order to cut parallel to the steps and get more symmetrical sample edges. The cleaved quarters were then placed in molybdenum holders, ready for MBE deposition. Thermocouples located at the back of the substrate were used to measure the substrate temperature. The growth temperature for the AlSb buffer layer was fixed at 550° and for the InSb epilayer at 450°C for all of the samples. Three samples were grown in total with varying thicknesses of AlSb.

Sample:	TMW09014	TMW09017	TMW09021
Ge buffer thickness (nm) ($\pm 0.5\%$)	881	881	881
AlSb buffer thickness (nm) ($\pm 2\%$)	0	20	16
InSb thickness (nm) (max/min) ($\pm 0.5\%$)	1747/304	1002	984
Total thickness (nm)	2629 (max)	1909	1861

Figure 7.2: List of InSb and InSb/AlSb samples grown in this chapter.

InSb	450°C		- SS-MBE grown InSb
Ge	650°C	4:41	881nm RP-CVD grown Ge/6° off-axis Si(001) virtual substrate (sample 15-208)
Anneal	650°C	10:00	
HT-Ge	550°C	3:42	
LT-Ge	350°C	18:51	
p ⁻ Si(001) 6° off-axis			

Figure 7.3: Schematic 1 of InSb/Ge/6° off-axis Si(001). Sample 15-208 from chapter 6 is used as the high quality RP-CVD Ge/Si(001) virtual substrate. Only one sample was grown to this specification: Sample TMW09014.

InSb	450°C		- SS-MBE grown InSb
AlSb	550°C		- SS-MBE grown AlSb buffer
Ge	650°C	4:41	881nm RP-CVD grown Ge/6° off-axis Si(001) virtual substrate (sample 15-208)
Anneal	650°C	10:00	
HT-Ge	550°C	3:42	
LT-Ge	350°C	18:51	
p ⁻ Si(001) 6° off-axis			

Figure 7.4: Schematic 2 of InSb/AlSb/Ge/6° off-axis Si(001). Sample 15-208 from chapter 6 is used as the high quality RP-CVD Ge/Si(001) virtual substrate. Two samples were grown to this specification: Sample TMW09017 and TMW09021.

7.2.1. InSb on Ge/Si(001) 6° off axis virtual substrate.

7.2.1.1. Analysis of sample TMW09014

The lattice mismatch between the tensile strained Ge buffer layer and the InSb epilayer is 14.33%. When growing InSb directly on to the Ge buffer layer at 450°C, the strain energy per unit volume is clearly too high for Stranski-Krastanov growth to take place and so Volmer-Weber growth takes place immediately as seen by the appearance of voids in the InSb crystal shown in figure 7.5 of sample TMW09014.

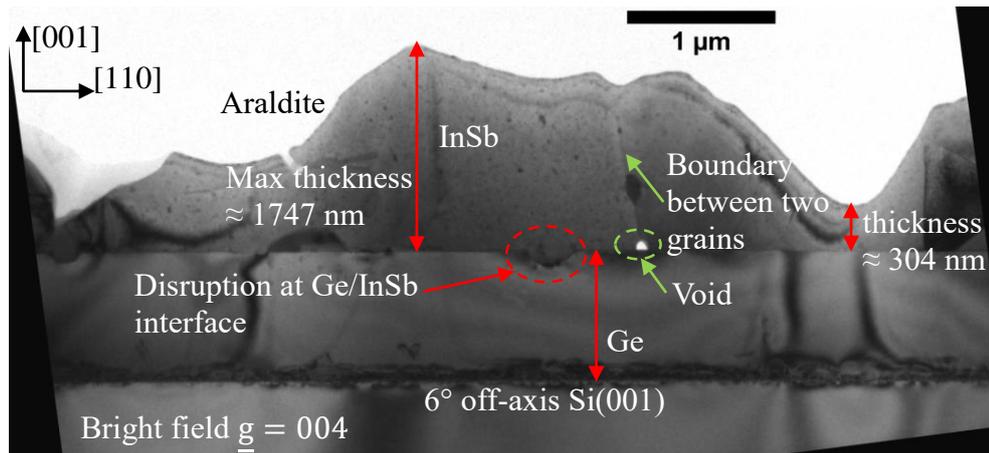


Figure 7.5: X-TEM of sample TMW09014. The InSb epilayer has not formed as a uniform film via Frank van der Merwe growth or even Stranski-Krastanov islands but as a Volmer Weber islands which grow independently. A grain boundary can be seen between two crystals grains with a 73nm diameter void at the interface between the Ge buffer layer and the InSb epilayer.

It can also be seen in figure 7.5 that the Ge/InSb interface has been disrupted and that the InSb has started to diffuse into the Ge buffer layer. This cannot be explained further as there is no literature available on the diffusion coefficients of Ge into InSb and vice versa at 450°C growth. Due to the strong 3D growth of the InSb layer, there is a large difference in measured height of the epilayer of 1.5μm. Contact mode AFM measurements indicate that the maximum height difference is 2505nm as shown in figure 7.7.

Figure 7.6 is a (220) dark field diffraction condition image of the sample and clearly shows that the Lomer dislocation network between the Si(001) substrate and the Ge buffer layer, but no such dislocation network is seen between the InSb and the Ge buffer layer. In dark field parts of the InSb appear black and invisible suggesting that the layer has become polycrystalline. HR-XRD was thus not carried out on the sample.

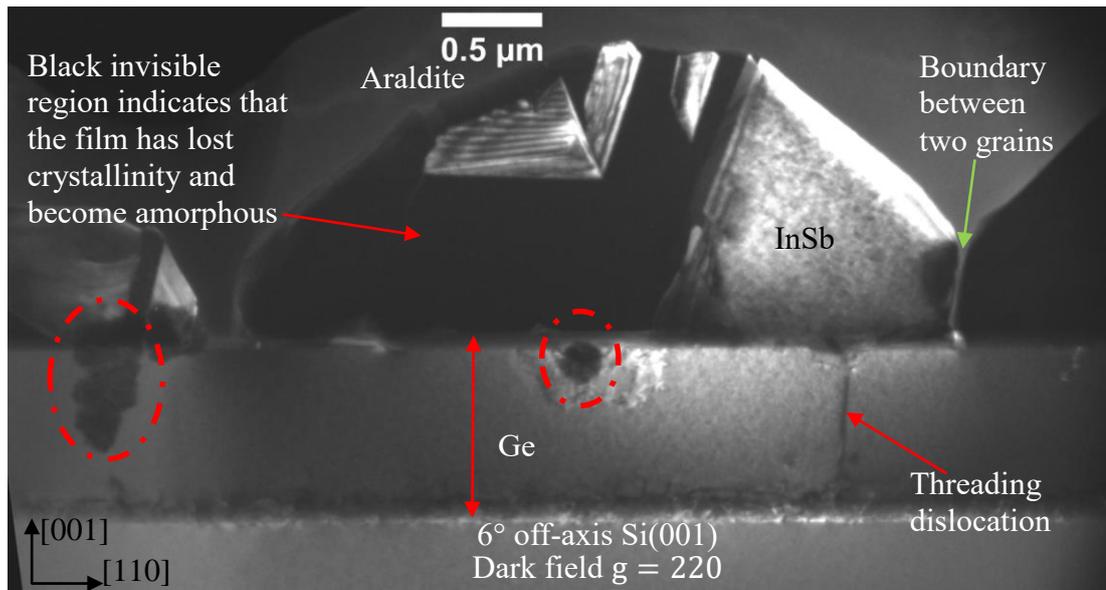


Figure 7.6: X-TEM of sample TMW09014. It's clear the film is not a single crystal but polycrystalline islands. The fact that certain regions of the film are black suggests that the film has become polycrystalline. Disruption at the Ge/InSb epilayer interface is seen shown in red dashed circles.

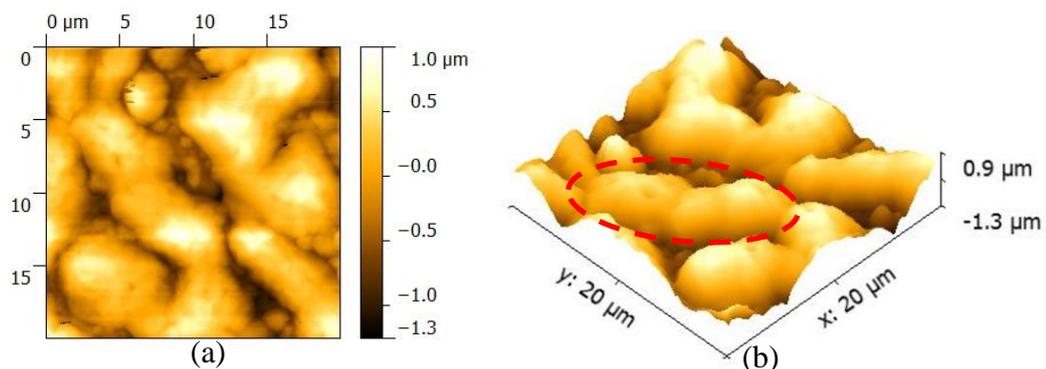


Figure 7.7: Contact mode AFM of sample TMW09014: InSb/Ge/6° off-axis Si(001). $R_{rms} = 395\text{nm}$ and height = 2505nm. The islanded feature are seen on the AFM micrograph as indicated by the red dashed circle.

7.2.2. InSb on AlSb/Ge/Si(001) 6° off axis virtual substrate

7.2.2.1. Analysis of sample TMW09017

7.2.2.1.1. X-TEM analysis of sample TMW09017

When 20nm of AlSb buffer is deposited on the Ge buffer layer, the ensuing InSb films shows much better crystalline quality. Figure 7.8 is a 004 dark field X-TEM image of

sample TMW09017. The surface of the layer appears much smoother from a cross-sectional view and 2D Frank Van der Merwe growth seems to have taken place. At high resolution of the InSb epilayer, the layer is shown to be crystalline (figure 7.9). At low magnification and in the 004 diffraction condition it is not possible to differentiate the AlSb from the InSb, particularly because of the high density of defects at the interface due to strain relaxation at the Ge/AlSb interface. The thickness of the AlSb layer was confirmed through HR-XTEM.

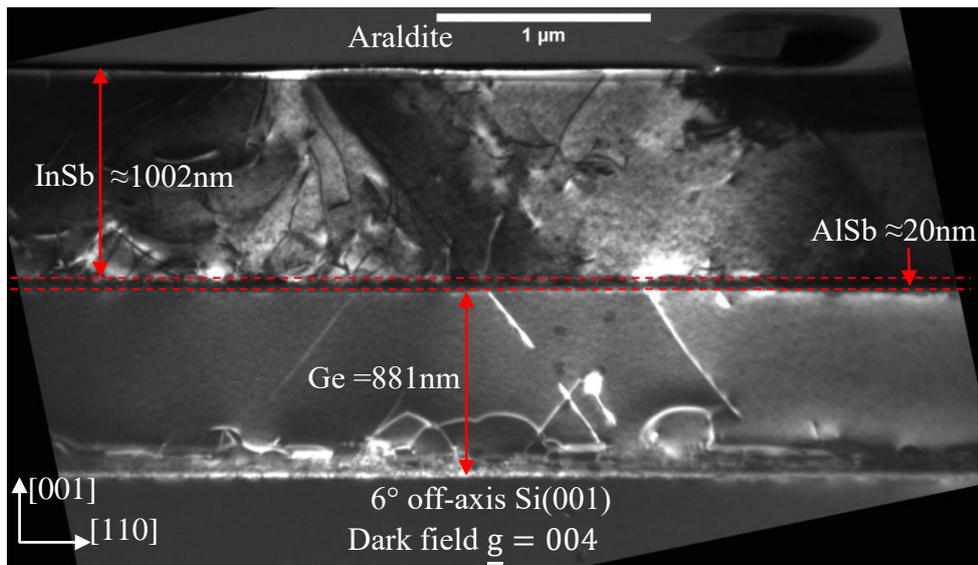


Figure 7.8: 004 dark field X-TEM of sample TMW09017. The 002 diffraction condition would have given better diffraction contrast between the InSb and the AlSb layer.

The 002 diffraction condition would have given better diffraction contrast between the InSb/AlSb layers and the Ge buffer layer. The 002 diffraction condition would also have categorically confirmed the existence of inversion domains in either the AlSb and InSb layers. From 004 and 220 conditions however inversion domains have not been seen in the sample X-TEM images. It is assumed that the 6° offcut and high temperature surface treatment of the Si(001) substrate has successfully created a higher density of single domains in the Ge buffer layer along [110] direction which has minimised inversion domains in the AlSb and InSb layers. Figure 7.10 shows sample TMW09017 in 220 dark field condition. From the cross section, it is seen that the InSb film is more defective than the Ge buffer layer.

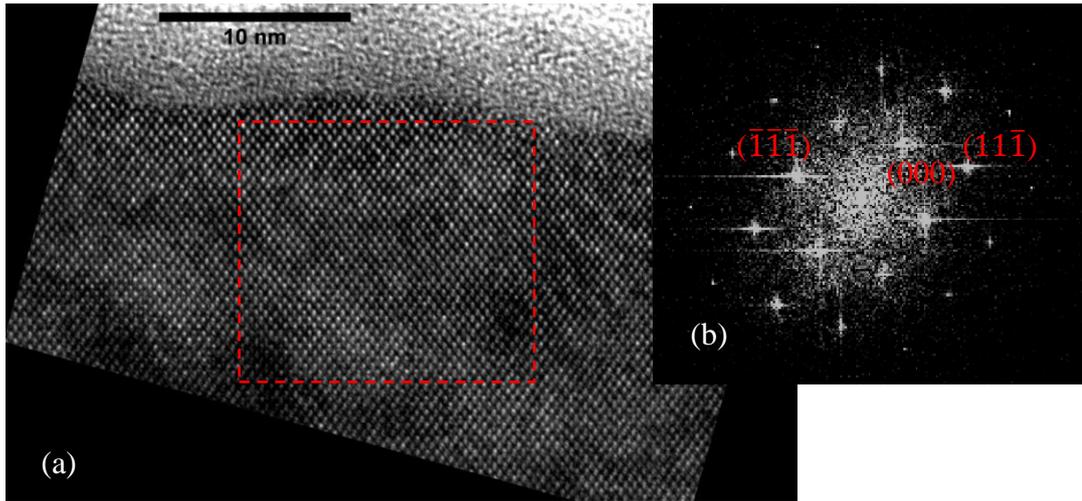


Figure 7.9: (a) HR-XTEM of sample TMW09017 at the top of the InSb layer taken at the [110] zone axis. An undulated surface can be seen brought about through compressive strain relaxation. (b) When taking the FFT of the top of the InSb epilayer, strong Bragg peaks are seen, indicating good crystalline quality.

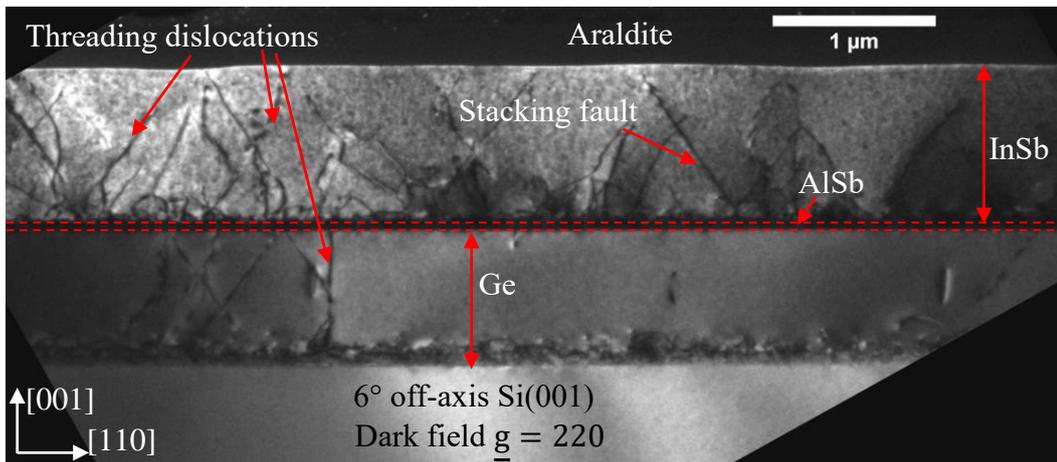


Figure 7.10: X-TEM of sample TMW09017. Threading dislocations and stacking faults from the Ge underlayer are shown to be nucleation points at the Ge/AlSb interface.

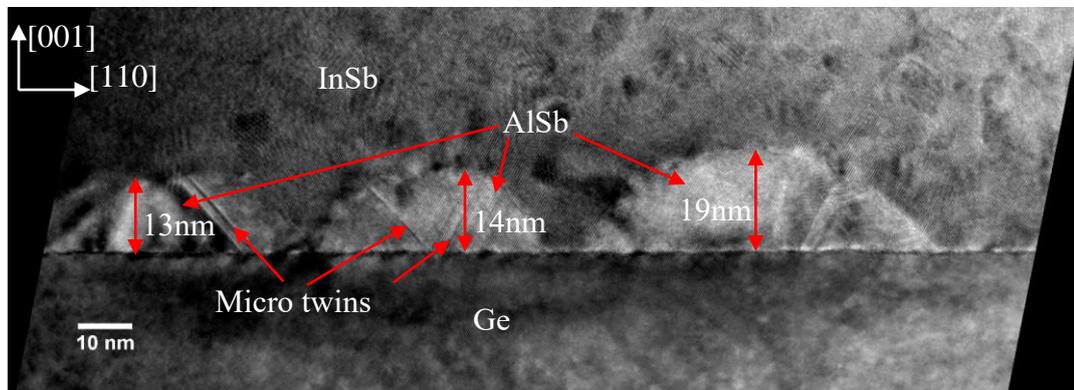


Figure 7.11: HR-XTEM of sample TMW09017 at the top interface between the Ge buffer layer and the AlSb layer. The AlSb has not formed a continuous layer. A wetting layer can be seen at the Ge/AlSb interface, suggesting that this is Stranski-Krastanov growth.

HR-XTEM at the Ge/AlSb interface indicates that the AlSb is not a continuous film, and is in fact composed of a wetting layer and islands as seen in figure 7.11. The 8.26% lattice mismatch between AlSb and the tensile strained Ge buffer at this growth temperature with a constant strain energy per unit volume causes Stranski-Krastanov growth with thicker islands than was seen in chapter 4 with 400°C Ge grown on Si(001). In chapter 4, at 400°C Ge islands appear to 8.4nm thick but by 10nm the islands have coalesced to form a blanket film but the lattice mismatch is only 4.2%. The formation of AlSb islands up to 20nm thick may also have to do with reduced mass transport velocities in MBE due to UHV pressure but this has not been verified.

Given a longer growth time at 550°C, it is assumed that the AlSb islands would have grown to a particular thickness, whereby the islands would start to merge and form a blanket layer. Figure 7.11 shows that the AlSb islands vary height from a maximum recorded value of 19nm to a smallest value of 13nm. AFM measurements were not able to be carried out on just the AlSb buffer layer so it is not possible to determine the maximum height of the islands. Micro twins are seen within the AlSb island due to growth on {111} planes during the initial stages of deposition.

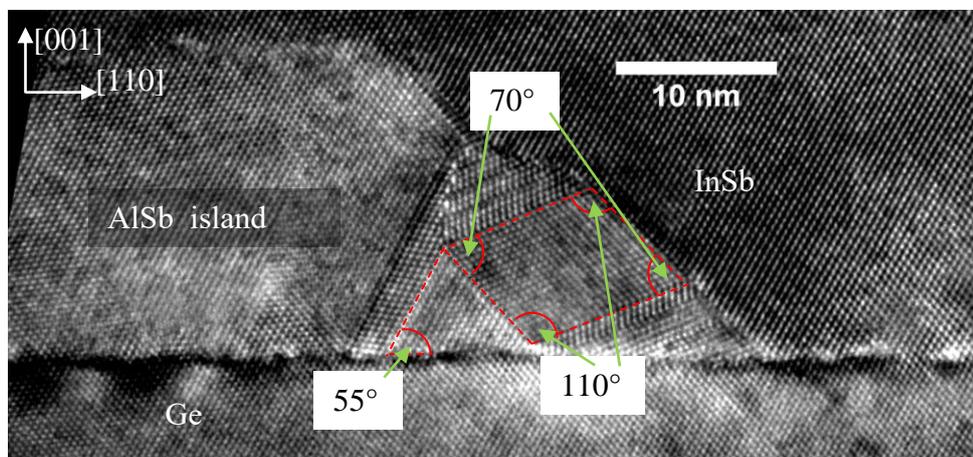


Figure 7.12: [110] zone axis HR-XTEM of sample TMW09017 at the interface between the Ge buffer layer and the AlSb layer. A single AlSb island is lattice resolved and double twinning can be seen within the island where twins interact with each other to form another twin.

The angle measured between the Ge surface and the micro twin in the island is 55°. This angle is the angle between the {111} glide plane and the (001) surface when looking along the [110] direction. Both of the Shockley partial dislocations of the

stacking fault lies on two sets of $\{111\}$ glide planes. This is typical for zinc blende/diamond structures as was seen in chapter 4 on LT-Ge buffer growth.

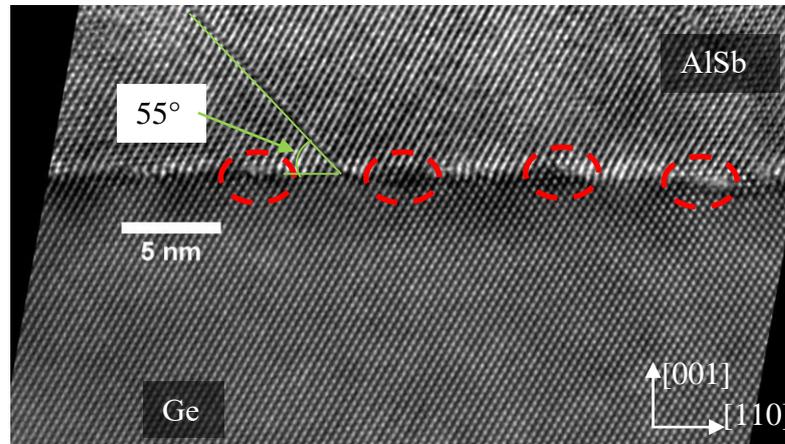


Figure 7.13: $[110]$ zone axis HR-XTEM of sample TMW09017 at the top interface between the Ge buffer layer and the AlSb layer showing the step and terrace features from the offset preserved into the Ge buffer layer as indicated by the red dashed circles. The stacking fault angle was measured to be 50° .

7.2.2.1.2. Surface morphology and defect analysis of sample TMW09017

Tapping mode AFM shows that the roughness of the InSb/AlSb/Ge/Si(001) surface has increased to 4.75nm from 1.64nm on the Ge buffer layer. This is a huge improvement in surface roughness compared to sample TMW09014 where the InSb epilayer was deposited directly onto the Ge buffer layer and generated a surface roughness of 395nm due to large amorphous/polycrystalline islands. Even when scanning up to $40\mu\text{m} \times 40\mu\text{m}$, cracks were not detected on the surface, which has been reported in previous literature to be a danger due to the thermal mismatch between AlSb and InSb.

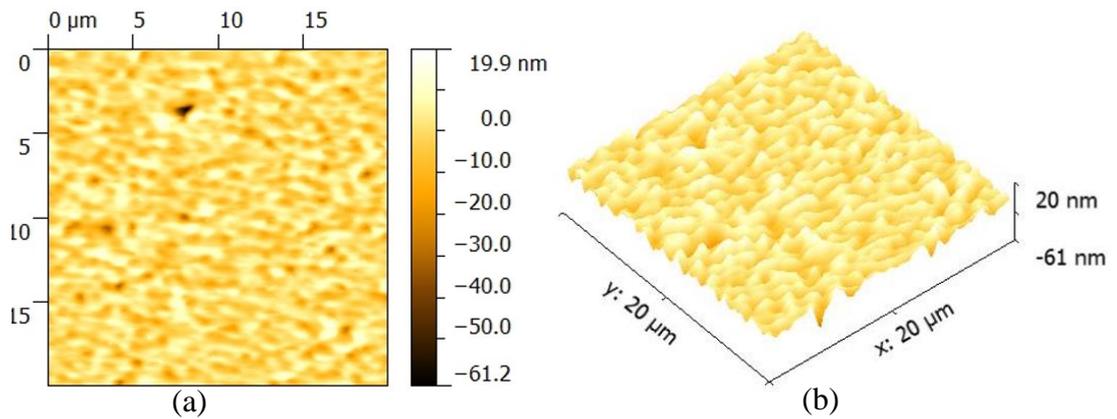


Figure 7.14: 20 μm \times 20 μm tapping mode AFM of sample TMW09017. $R_{\text{rms}} = 4.75\text{nm}$. Height = 74.7nm.

Plan view TEM showed the InSb epilayer had a TDD $1.13 \times 10^9 \text{ cm}^{-2}$ (figure 7.15). This is only $\times 10$ higher than the TDD in the Ge buffer layer on 6° off-axis Si(001). There is not much literature available on TDD in InSb epilayers on Ge/Si(001) virtual substrates to compare this value to, however given the large lattice mismatch between Si(001) and InSb, a $\times 10^9 \text{ cm}^{-2}$ defect density is a superb starting accomplishment.

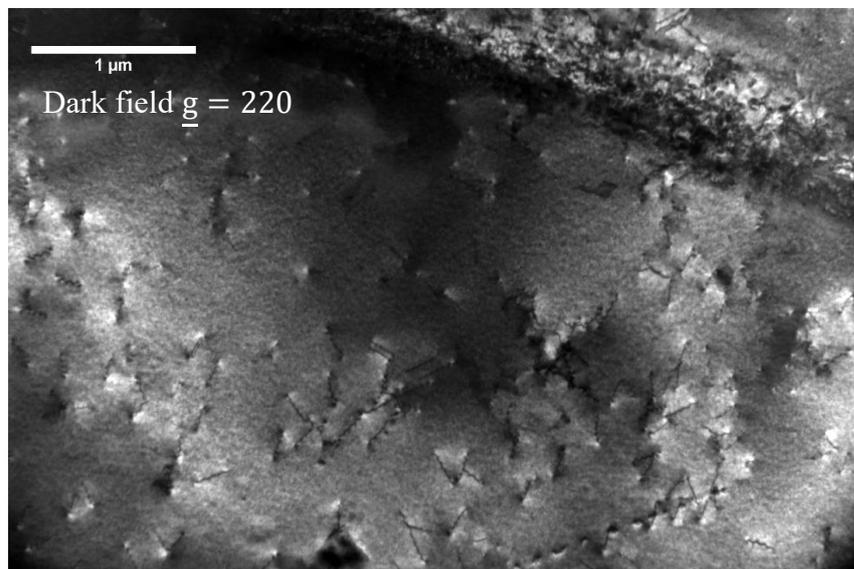


Figure 7.15: Plan view TEM of sample TMW09017. TDD = $1.13 \times 10^9 \text{ cm}^{-2}$.

7.2.2.1.3. HR-XRD of sample TMW09017

When carrying HR-XRD RSMs of sample TMW09017, The AlSb peak is not detected. In the 004 scan given that AlSb has a lattice constant in between Ge and InSb, it should

have been detected at a point in reciprocal space between the Ge and InSb peaks. The reason why it was not detected was because it was not a continuous layer, therefore a coherent X-ray signal could not be generated from this material.

Due to the large difference in lattice constant for between Ge and InSb instead of scanning for both the Ge and InSb peaks in one scan for 004 and 224, which have wasted time by covering empty space in reciprocal space, the scans were divided into two: one for off axis Si(001) & the Ge buffer layer and secondly around the supposed InSb Bragg angle in 004 and 224. The 002 reflection would have also been acceptable as a symmetrical scan for InSb since it is a zinc blende material and so 002 is not forbidden.

After obtaining Q_x and Q_y position values for the InSb layer and then correcting for tilt wrt the Si(001) substrate in the (004) scan, the in-plane and out-of-plane lattice constants were calculated using the same equations: 9.1 to 9.31. The strain was calculated by assuming that the InSb layer was a 50% In/50% Sb compound given its ionicity and therefore the bulk lattice constant of InSb was taken.

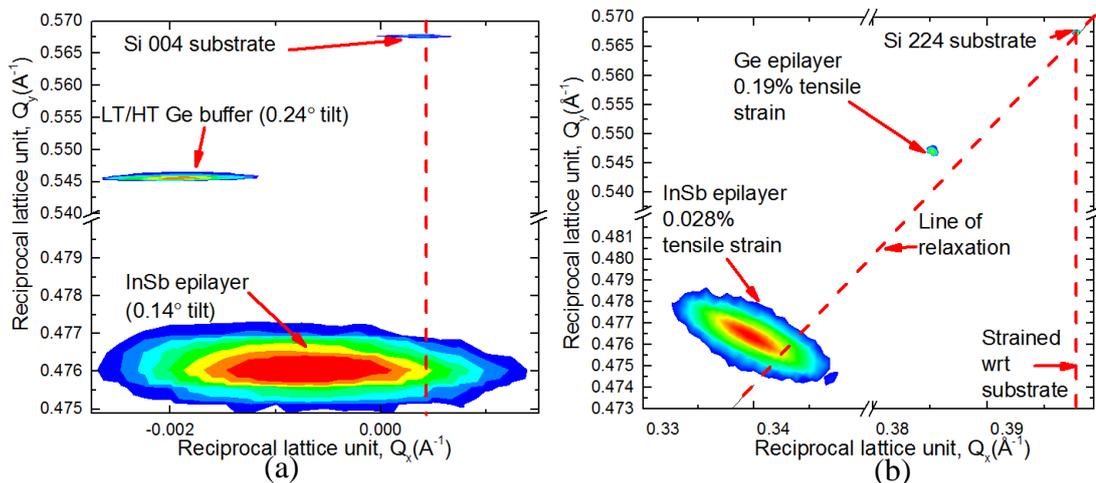


Figure 7.16: 004 and 224 RSMs of sample TMW09017. The in-plane and out-of-plane lattice constants in the InSb layer were determined in the same manner as for the SiGe and Ge epilayers.

The Ge buffer was under 0.19% tensile strain and was tilted by 0.24° ; both of which were expected. The InSb epilayer however was under 0.028% tensile strain and was

tilted by 0.14° wrt Si(001). The over relaxation of the InSb layer is possibly due to the thermal mismatch to AlSb.

The reduced tilt is hypothesised to be caused by a lack of multiplication of 60° misfit dislocation at the AlSb/InSb interface and also because of the presence of the islands which reduce the disparity in stressing along the $\{111\}$ planes in the InSb layer thereby promoting more symmetrical strain relaxation. The InSb peak is much broader than the Ge buffer layer peak and the Si(001) peak. This mosaic spread of the peak in the Q_x direction is caused by defects in the layer, as was seen in the plan view image showing a high density of threading dislocations. Due to the low density of stacking faults, a line density of stacking faults in the InSb layer could not be obtained and so it is currently not known how much layer relaxation is attributed to stacking fault formation.

7.2.2.2. Analysis of sample TMW09021

In the final InSb sample, the deposition time for the AlSb buffer layer was reduced so to produce a thinner AlSb layer. In sample TMW09017 it was seen that the AlSb was not a continuous layer but rather composed of islands. By reducing the deposition time, it is expected to reduce the island density and/or height and negatively affect the quality of the InSb epilayer.

7.2.2.2.1. X-TEM analysis of sample TMW09021

When reducing the deposition time for the AlSb buffer layer, the ensuing InSb layer is still a continuous film. A higher density of defects is seen in the InSb epilayer than in the Ge buffer layer as was the case with sample TMW09017. Figure 7.17 shows micro twins present in the InSb epilayer that are only partially visible due to the invisibility criterion. Figure 7.18 shows a (220) diffraction condition image of the same sample. A possible Frank-Read loop is seen in figure 7.18. As with sample TMW09017, inversion domains were not seen in the InSb film indicating the offcut and surface treatment in the substrate was preserved in the Ge buffer layer and successfully created a single domain.

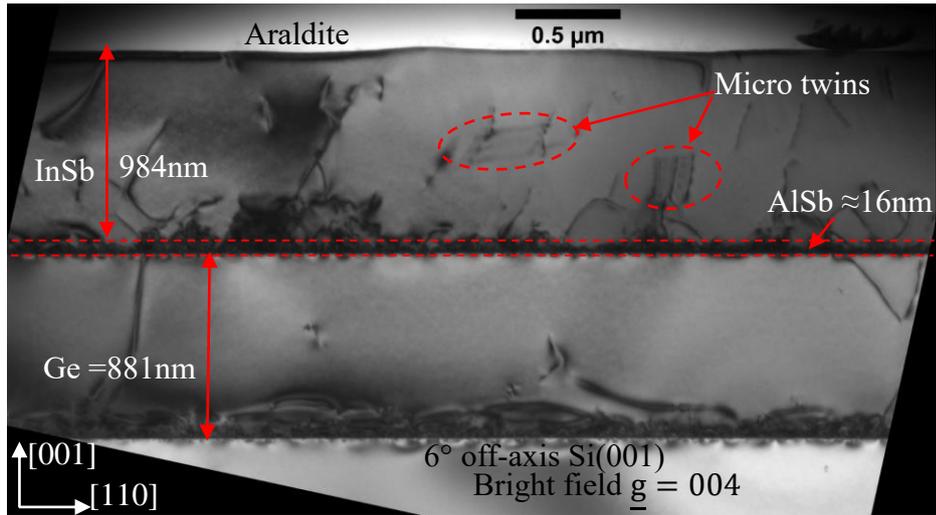


Figure 7.17: X-TEM of sample TMW09021. The AISb buffer layer could not be distinguished from the InSb layer due to the high misfit dislocation network at the interface between Ge and AISb. The thickness of the AISb layer was verified through HR-XTEM. All thicknesses are measured in the (004) diffraction condition.

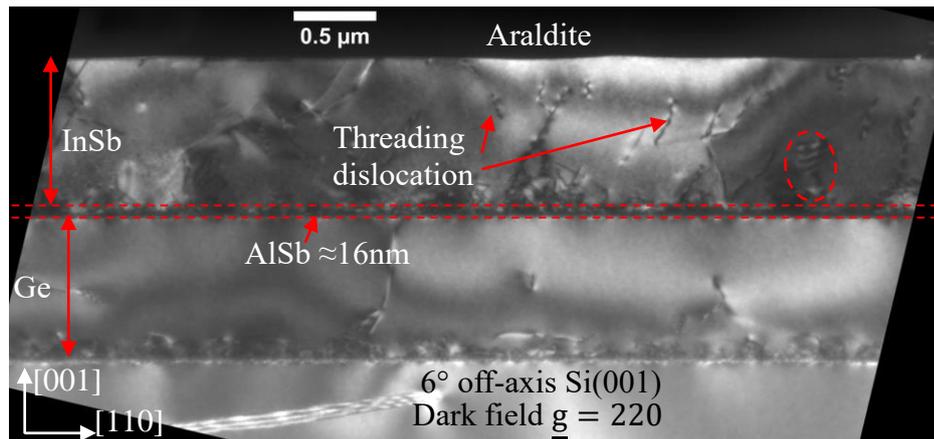


Figure 7.18: X-TEM of sample TMW09021. The red dashed circle indicates an observed dislocation multiplication, possibly Frank-Read. The InSb epilayer still appears to have a higher defect density than the Ge buffer layer.

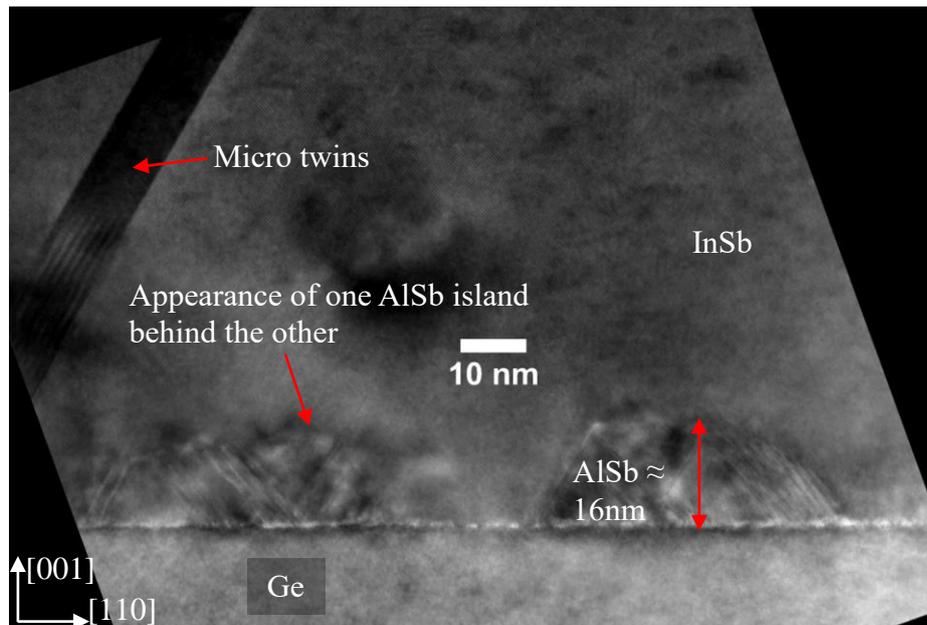


Figure 7.19: (110) zone axis HR-XTEM image of sample TMW09021. In this image, it seems as though the islands are not as pronounced as sample TMW09017, suggesting that there are not as many. A higher number of growth micro twins are seen, due to growth on {111} planes

Upon closer examination of the Ge/AlSb interface at high resolution, it is seen that there are not as many AlSb islands present. The reduced deposition time has led to a lower coverage of the Ge buffer layer surface with AlSb islands. (110) zone axis HR-XTEM shows that the islands are not as pronounced as in sample TMW09017. The average height of the islands is 16nm. A 0.8nm +/- 0.2nm wetting layer of AlSb has been measured in some regions. The reduced density of AlSb islands means that as well as being deposited on the AlSb islands, InSb is also being directly deposited on the AlSb wetting layer and directly on the Ge buffer layer in between the islands. A density of islands could not be obtained from (110) zone axis imaging. If the sample was tilted in order to have the straight through beam go through the (113) zone axis, then perhaps the sample could have been imaged to see the islands better. ref [119].

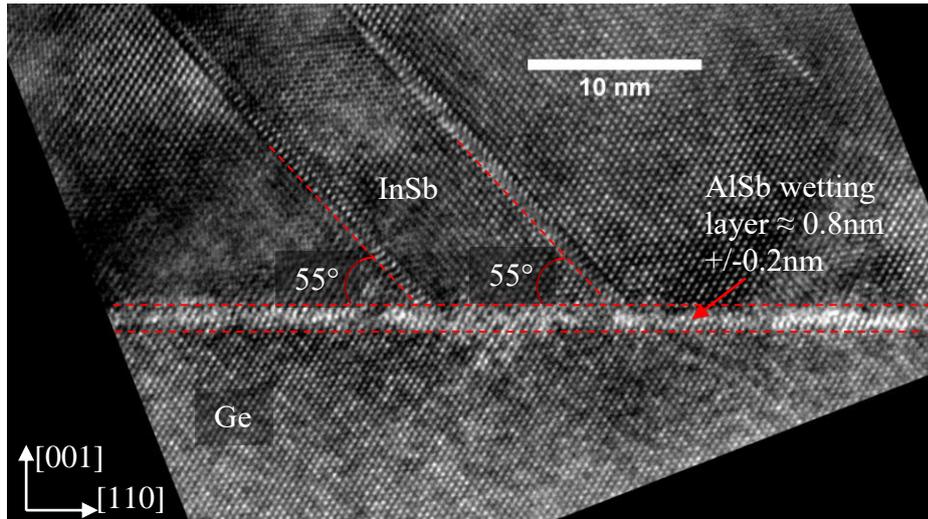


Figure 7.20: (110) zone axis straight through HR-XTEM image of sample TMW09021. Micro twins are seen to have formed in the InSb layer at the Ge/AlSb surface. A possible AlSb wetting layer may exist between the Ge and InSb, but this has not been confirmed.

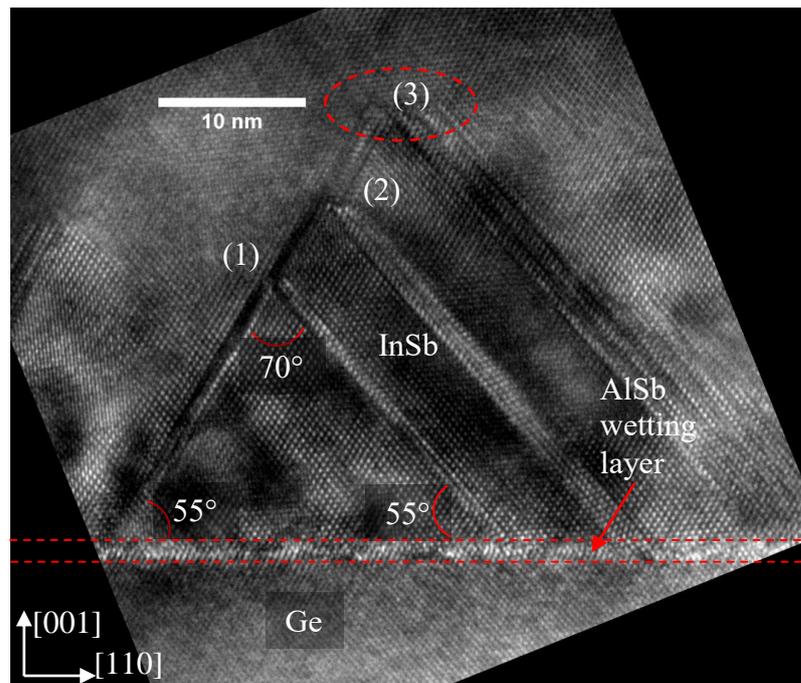


Figure 7.21: (110) zone axis straight through HR-XTEM image of sample TMW09021. Micro twins on opposing {111} glide planes are seen in the InSb layer to meet and annihilate leaving behind defect free InSb crystal. The red dashed circle indicates where the twins have been fully annihilated. At points, (1) and (2) multiplication has occurred. However, at point (3) full annihilation occurs.

Finally, it is seen that the micro twins terminate within the InSb layer itself (figure 7.21) through opposing {111} glide planes. In figure 7.21, it is seen that as the micro twins from opposing {111} glide planes meet, depending on the density on each {111} glide plane, they either multiply or annihilate. Point (1) shows how two twins meet to

create a wider fault which continues up to point (2). Full annihilation occurs at point (3)

7.2.2.3. Surface morphology and defect analysis

Tapping mode AFM analysis shows that the sample has a roughness of 16nm and height difference of 121nm. The reduced thickness and density of AlSb islands has meant that the InSb layer undergoes strain relaxation on a thin strained AlSb wetting layer, or perhaps the Ge buffer layer itself. The roughness is 4 times higher than in sample TMW09017. Due to the thin wetting layer and low density of AlSb island coverage it is hypothesised that a great deal of InSb strain relaxation takes places on the Ge buffer itself. This means that InSb relaxes under compressive strain and so the formation of surface undulations is seen.

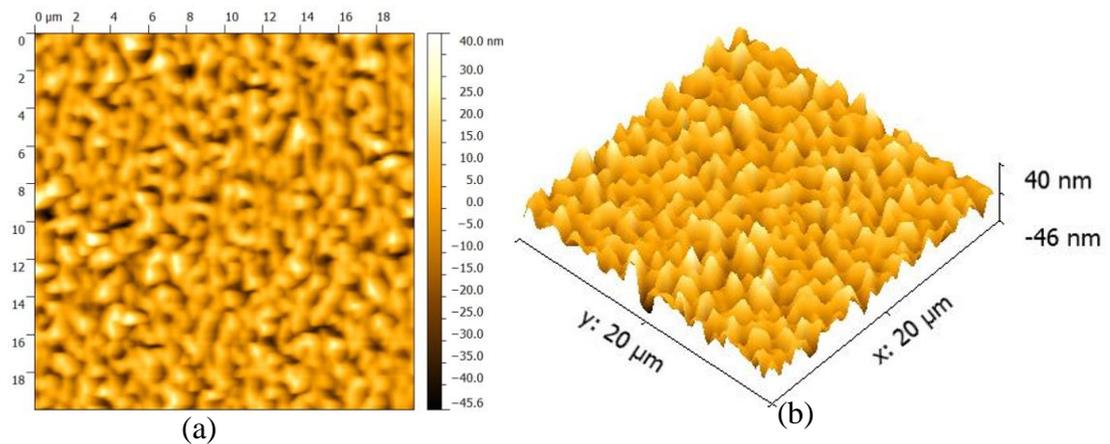


Figure 7.22: $20\mu\text{m} \times 20\mu\text{m}$ tapping mode AFM of sample TMW09021. $R_{\text{rms}} = 16 \text{ nm}$. Height = 121nm

Plan view TEM measurements show that the TDD in the InSb epilayer is $1.37 \times 10^9 \text{ cm}^{-2}$ as seen in figure 7.23.

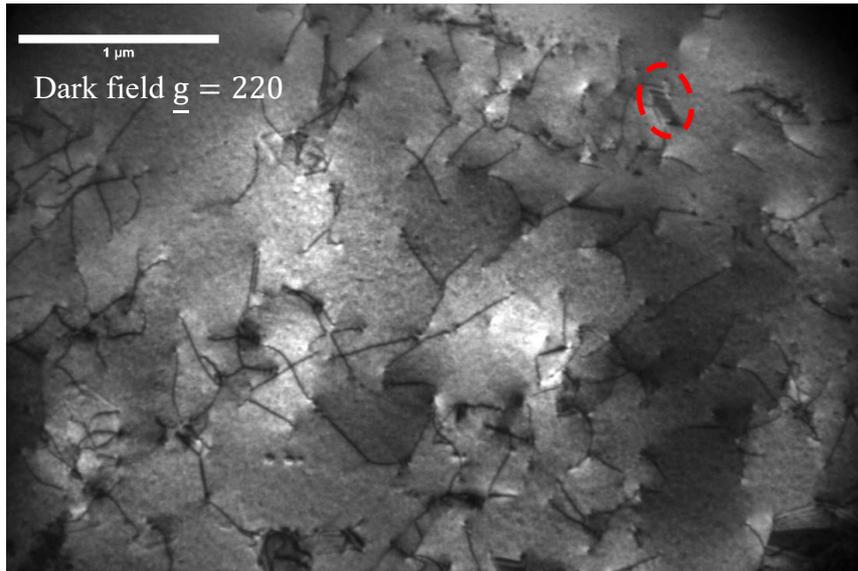


Figure 7.23: Plan view TEM of sample TMW09021. TDD = $1.37 \times 10^9 \text{cm}^{-2}$. The dashed red circle indicates a stacking fault

7.2.2.3.1. HR-XRD of sample TMW09021

XRD RSMs indicate that the InSb layer is under 0.6% compressive strain as shown by figure 7.24. This is explained by the thinner and lower island density AlSb layer and exposed Ge buffer layer. It is more likely that since the thermal expansion coefficients between Ge and InSb are very similar, lattice mismatch is the prominent method by which the InSb undergoes strain relaxation. Unlike sample TMW09017, where the thicker and dense island populated AlSb layer allows the InSb to relax on it as a full buffer layer. The end result is that InSb relaxes under tensile strain in sample TMW09017 due to thermal mismatch to the AlSb whilst it relaxes under more compressive strain due to the exposed Ge buffer. The degree of tilt in the layer is 0.12° which is similar to the tilt in sample TMW09017.

The InSb peak itself has the same distance of mosaic spread across the Q_x axis and this means that the layers have similar defect densities, which was corroborated by plan view TEM.

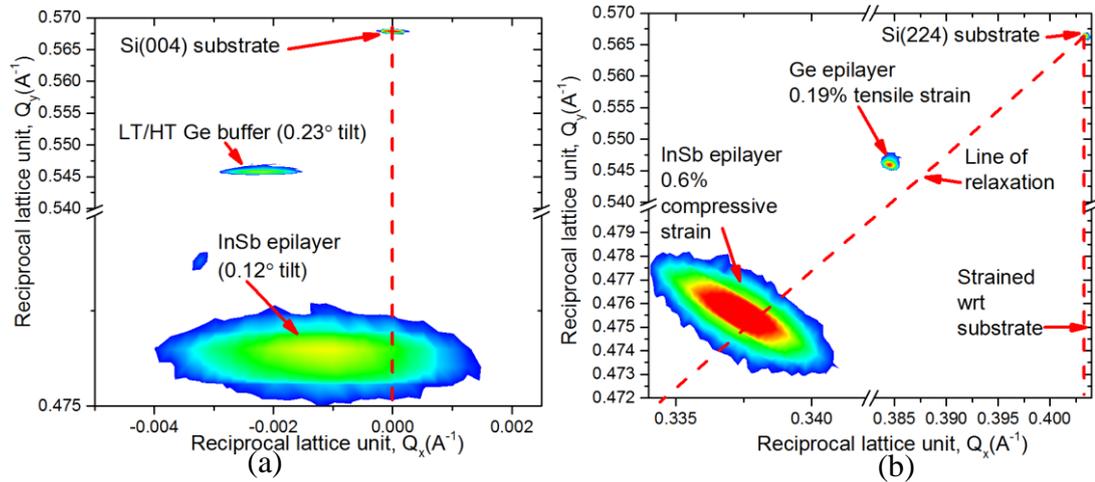


Figure 7.24: 004 and 224 RSMs of sample TMW09021.

7.3. Chapter 7: Summary

In summary, in this chapter sample 15-208 from chapter 6: high quality Ge/Si(001) 6° off-axis virtual substrates are used for the SS-MBE growth of InSb; a semiconductor with $77,000 \text{ cm}^2/\text{Vs}$ room temperature electron mobility and 0.17eV bandgap but with 19.3% lattice mismatch to Si(001). Ge has a similar thermal expansion coefficient to InSb and so is considered a suitable candidate for the epitaxy of InSb. The tensile strained Ge buffer layer acts to reduce the lattice mismatch to 14.33% however growth of an InSb film at 450°C shows that the layer is polycrystalline and partially amorphous. Disruption of the Ge buffer layer/InSb interface was observed when depositing the InSb. Diffusion of InSb was seen into the Ge buffer layer. The surface roughness was measured as 395nm via contact mode AFM and shows the presence of $2.5\mu\text{m}$ high grain boundaries.

SS-MBE grown AlSb was used as a secondary buffer layer on top of the tensile strained Ge to reduce the lattice mismatch to InSb from 14.33% to 5.6% . However due to the 8.26% lattice mismatch between AlSb and tensile strained Ge, Stranski-Krastanov growth of the AlSb islands is observed up to a height of 20nm . The density and height of the AlSb islands was found to be proportional the deposition time. AFM measurements were not carried out on the AlSb buffer layer, but should be done in a

future investigation to determine the diameter of the islands and the thickness at which they coalesce into a continuous film.

Micro twins were found to have been generated in the AlSb islands which were annihilated in closed loops inside individual islands. The quality in the subsequent growth of InSb was dependent on the density and height of these AlSb islands. The best quality 1 μ m thick InSb layer had a surface roughness of 4.75nm, TDD = $1.13 \times 10^9 \text{cm}^{-2}$ and was under 0.028% tensile strain. The tensile strain in the InSb film was attributed to the thermal expansion coefficient mismatch between InSb and AlSb.

For AlSb with shorter deposition times, it was discovered that the density of islands and ubiquity of the wetting layer was reduced. Therefore, it is suspected that a greater surface area of the Ge buffer layer underneath was exposed to the InSb for growth. The subsequent InSb film grown was under 0.6% compressive strain, had a TDD = $1.37 \times 10^9 \text{cm}^{-2}$ and a surface roughness of 16nm.

Additionally, it was discovered that the degree of tilt in the InSb epilayer is lower than in the Ge buffer layer, which has an average tilt of 0.24° . The tilt in the InSb layer with 0.028% tensile strain 0.14° whilst the tilt in the InSb layer under 0.6% compressive strain was 0.12° . This reduction in tilt is explained by the presence of the AlSb islands which negates the effects of the offcut step and terraces and as a consequence the {111} planes are stressed more equally, thus allowing more symmetrical glide of 60° misfit dislocations and more symmetrical strain relaxation.

8. Conclusions and further work

8.1. Conclusions

RP-CVD grown pure Ge and $\text{Si}_{1-x}\text{Ge}_x$ buffer layers on Si(001) were investigated as potential pathways to integrate III-V materials for state of the art optical and electronic devices.

The first investigation involved growth of Ge buffer layers in between 300°C and 400°C and in between 1.65nm to 351nm thickness. It was observed that smooth Ge buffer layers could be obtained below 95nm thickness and 350°C growth temperature after which severe faceting caused by growth anisotropy creates a rise in surface roughness. Faceting is a temperature phenomenon and was triggered in thinner layers at lower temperatures. It was also discovered that the current state of the 1nm rough, 1 μm thick LT/HT Ge buffer layer could be replaced with a 78nm LT + annealed buffer layer that had a tenth of the tensile strain of the LT/HT layers but was 2nm rough but had x100 more TD's. This was achieved by controlling the thermal budget applied to the layer. It was discovered that annealing 20nm layers for more than 1 min at 650°C caused the substrate to diffuse into the Ge epilayer and ruin the crystal quality.

The second investigation involved comparison between the established linearly graded technique (LG) with the recently discovered reverse linearly graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer technique (RLG). In both case the $\text{Si}_{1-x}\text{Ge}_x$ buffer layer was grown at 850°C using dichlorosilane and germane as the Si and Ge precursors respectively. For the reverse graded process a LT(350°)/HT(550°) Ge buffer layer was used. It was discovered that by reverse grading down to 45% Ge below 30%Ge/ μm grading rate, the surface roughness continued to remain under 3.7nm. The strain in the Ge under layer was 0.2(\pm 0.05) % tensile, and this level of strain remained in the reverse graded $\text{Si}_{1-x}\text{Ge}_x$ layer even when reverse grading down to 45% Ge. The maintenance of 0.2% tensile strain in the reverse graded $\text{Si}_{1-x}\text{Ge}_x$ buffer is explained by the already present 0.2% strain in the Ge underlayer as a starting point and given the low grading rate, no further excess strain is generated in the layer. The TDD started at $7 \times 10^7 \text{cm}^{-2}$ for 71% Ge layers but dropped to $4 \times 10^7 \text{cm}^{-2}$ when reverse graded to 45%Ge. This occurred in tandem with a rise in stacking faults, caused by the

dissociation of 60° misfit dislocations given the tensile strain relaxation process. This rise in stacking faults is responsible for marginally disrupting the roughness on what is otherwise a planar surface. Cracking of the $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layer was also investigated and it was found that that cleaved crack density reduced as the buffer was reverse graded to lower percentages of Ge. This was explained to be because the difference in Young's modulus between the $\text{Si}_{1-x}\text{Ge}_x$ buffer layer and the Si(001) substrate, reduces as the buffer is reverse graded to lower Ge content layers.

Alternatively, the linear grading process showed the formation of Frank-Read dislocation loops, high surface roughness and pile-up due to compressive strain relaxation. This was prevalent in low Ge content layers, linearly graded at less than $15\% \text{Ge}/\mu\text{m}$. Modified Frank-Read multiplication of 60° misfit dislocations led to dislocation interaction and kinetic effects that resulted in incomplete strain relaxation. Low grading rates in linearly graded buffer layers provided limited glide velocities. High surface roughness and large radii orthogonal strain fields led to reduced glide channels and dislocation pinning. For samples linearly graded at less than $15\% \text{Ge}/\mu\text{m}$ chlorine etching was observed in the layers.

When comparing the linear graded and reverse linear graded techniques it was observed that reverse graded layers had faster growth rates than the linear graded process. This was explained as being due to tensile strain relaxation providing smooth surfaces for adatom adsorption whereas compressive strain relaxation in the linear grading process creates dense cross hatching features that cause surface undulations and uneven growth surfaces. Linear grading also has to be carried out at under $10\% \text{Ge}/\mu\text{m}$ in order to promote Frank van der Merwe growth, whereas reverse grading at $30\% \text{Ge}/\mu\text{m}$ still generated smooth surfaces. Finally, when comparing the Schimmel etch rate between linearly graded and reverse linearly graded layers it was observed that reverse graded layers followed a similar etch trends as had been seen in the literature, however without reverse grading back to pure Si a full plot could not be made.

An additional investigation in the 2nd chapter involved reverse step graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ (RSG). This technique is a new grading technique developed in this

study and involves reverse grading without a grading layer. An astonishing discovery was made, when reverse step grading below 70% Ge. Tensile strain build up in the $\text{Si}_{1-x}\text{Ge}_x$ layer, the 850°C growth temperature, thin layers in the heterostructure and the faster diffusion coefficient of silicon into germanium vs germanium into silicon, had caused the Si to diffuse into the Ge underlayer and form Kirkendall voids in the underlayer as a strain relieving mechanism. This phenomenon has rarely been observed in Si and Ge because the diffusion coefficients of the two elements are very low. Additionally, the strain caused by the lattice mismatch between the Ge underlayer and the $\text{Si}_{1-x}\text{Ge}_x$ layer resulted in the $\text{Si}_{1-x}\text{Ge}_x$ layer separating into two separate compositions. RSG were only investigated down to 47% Ge.

The third investigation involved investigation into pure Ge and reverse terrace graded (RTG) $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ layer buffer layers on 6° off-axis Si(001) for $0.72 \leq x \leq 0.764$. It was discovered that 10min, 650°C annealing of a 65nm thick 350°C Ge buffer grown on off-axis Si(001) had started to allow the substrate to diffuse into the Ge epilayer, as had been observed in the LT-Ge on on-axis Si(001) study. A high quality 1.6nm rough, 881nm thick LT/HT Ge/6° off-axis Si(001) virtual substrate with a TDD of $1.51 \times 10^8 \text{cm}^{-2}$ and under 0.2% tensile strain was created for the purpose of lattice mismatched heteroepitaxy to InSb. Strain in Ge buffer layers grown in the same conditions on or off axis Si(001) are identical. Off-axis Ge buffer layers are shown to be tilted wrt to the substrate by an average of $0.24^\circ \pm 0.05^\circ$ due to unequal stressing of the {111} glide planes on offcut substrates, therefore leading to incomplete cancellation of the tilt component and reduced annihilation of threading dislocations.

Reverse terrace grading has been shown to be effective in reducing TDD from the Ge underlayer to the $\text{Si}_{1-x}\text{Ge}_x$ whilst keeping smooth surfaces whether on on-axis or 6° off-axis Si(001). $\text{Si}_{1-x}\text{Ge}_x$ buffer layers grown on and off-axis have identical levels of strain of 0.2% given the under 10%Ge/ μm average grading rate. Due to the additional planes made available on off-axis substrates, a reduced dangling bond density results in slower growth and thinner layers in off-axis samples. An increase in tilt is observed along the RTG structure. The average tilt in the $\text{Si}_{1-x}\text{Ge}_x$ layer $0.44^\circ \pm 0.05^\circ$. RLG buffer layers grown to similar percentages of Ge did not exhibit an increase in tilt in the $\text{Si}_{1-x}\text{Ge}_x$ layer. Modified Frank Read multiplication of 60° misfits is presumed to

occur in the graded regions of the RTG layers due to the high grading rates on both on-axis and off-axis samples. The unequal stressing of the {111} glide planes due to the offcut causes incomplete cancellation of the vertical tilt component of 60° misfit dislocations and thereby increasing the layer tilt from the Ge to the Si_{1-x}Ge_x layer and also incomplete annihilation of threading dislocations resulting in higher TDD in offcut samples.

The fourth and final investigation in this project involved SS-MBE growth of InSb on the high quality Ge/6° off-axis Si(001) virtual substrate from chapter 6. Direct growth of InSb at 450°C on the virtual substrate produced a polycrystalline/amorphous InSb film due to the 14.33% lattice mismatch between tensile strained Ge and InSb. Using a secondary buffer layer of SS-MBE grown AlSb at 550°C, had the effect of mitigating the large lattice mismatch jump into two smaller jumps of 8.26% for tensile strained Ge/AlSb and 5.6% for AlSb/InSb. AlSb Stranski-Krastanov islands were seen on the Ge buffer surface. The quality of the InSb epilayer was found to be dependent the density of the AlSb islands. 0.028% tensile strain in the InSb epilayer was observed in the sample with the greatest density of AlSb islands, whilst 0.6% compressive strain in the InSb layer was observed in the sample with the lowest density of AlSb. This is explained via the thermal expansion coefficient mismatch between AlSb and InSb causing tensile strain relaxation whereas with the sample with the fewest AlSb islands, the Ge buffer layer underneath was exposed and available for growth, therefore leading to compressive strain relaxation in the InSb layer.

8.2. Future works

8.2.1. Ultra-thin strain neutralised Ge buffer layers

Strain neutralised thin Ge buffer layers are important for a number of reasons. For GaAs (Å=5.65325) growth because the lattice constant for bulk Ge is very similar to GaAs, and so is the thermal expansion coefficient. A LT-Ge + annealed buffer offers a much better defect free solution for GaAs based LED devices on Si(001) [187].

For future development of high quality reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ buffer layers, it is predicted that a strain neutralised Ge underlayer would minimise or even eliminate the 0.2% tensile strain seen in the $\text{Si}_{1-x}\text{Ge}_x$ buffer layer, provided that the grading rate was kept below 30%Ge/ μm . The 0.2% tensile strain in the Ge underlayer and its thickness contributes to the overall stress in the heterostructure which causes the film to crack. Recent works into FEA modelling of SiGe heterostructures have given predictions on $\text{Si}_{1-x}\text{Ge}_x$ channel stressors [188]. FEA should be used to model critical thickness and Ge content in reverse graded $\text{Si}_{1-x}\text{Ge}_x/\text{Ge}$ heterostructures to determine when fractures occur so as to optimise the buffer.

The Kirkendall effect seen in RSG buffer layers is assumed to be dependent on the growth temperature as well as the thickness of the constituent layers. It would be interesting to see how the void formation propagates when reverse step grading below 70% but on a 78nm thick Ge buffer layer as opposed to a 930nm LT/HT Ge buffer.

Finally the 78nm strain neutralised Ge buffer layer should be grown on 6° off-axis Si(001) for the purpose of being a virtual substrate for AlSb/InSb. It is predicted that the strain will be exactly same in the thin Ge buffer layer grown 6° off-axis Si(001), however the TDD might slightly higher due to unequal stressing of {111} glide planes. Si(001) has a much higher thermal conductivity than either Ge or InSb, therefore having as thin a Ge buffer layer as possible is crucial in conducting the heat away from a proposed InSb device layer and into the substrate.

8.2.2. Investigation of increased annealing time on TDD of 80nm thick Ge buffer layer.

From chapter 4 it was clearly seen that 650°C annealing of a 20nm Ge buffer layer (regardless of growth temperature) for 1 min causes substrate diffusion into the epilayer. In chapter 6 annealing a 65nm off-axis grown Ge buffer layer for 10 mins causes the same effect but is not as pronounced. The process of annealing thin layers has shown a reduction of threading dislocations by glide of 60° misfits on the {111} plane as well as (001) glide of Lomer dislocations. An in-depth investigation should be carried out on various Ge buffer layers grown below 78nm thick and annealed at a range of temperatures for a range of times to determine how the annealing affects

change on a thickness profile so that a strain relaxed buffer can be created as thin as possible with as few TD's as possible. It may be the case that annealing sample 15-61 (78nm Ge buffer) for any longer than 10 mins could start to cause substrate out diffusion but this has not been determined in this project.

8.2.3. Investigation of faceting effects on TDD in $\text{Si}_{1-x}\text{Ge}_x$ buffer layers grown subsequently.

The phenomenon of faceting in LT-Ge buffer layers could have useful applications in providing a “patterned” buffer layer on which to deposit graded or constant composition $\text{Si}_{1-x}\text{Ge}_x$. The facet walls could serve to annihilate threading dislocations in the same manner that oxide walls in intentionally patterned wafers annihilate TDs through the process of aspect ratio trapping. The growth temperature of the SiGe layer has to be carefully controlled so as to not collapse the facets, since beyond 400°C growth facets are not seen in the Ge buffer layer.

8.2.4. RLG and RSG to pure silicon

In chapter 5, section 5.4 it was seen that reverse linearly grading to low Ge content $\text{Si}_{1-x}\text{Ge}_x$ layers has the effect of causing a rise in stacking faults due to 60° misfit dissociation. In this investigation reverse grading was only carried out up to 45% Ge. To get a full understanding of how the buffer responds, it would be important to reverse grade back to pure silicon. It is hypothesised that the rise in stacking faults on a planar surface will continue. It is currently unknown as to how to combat this. In linearly graded $\text{Si}_{1-x}\text{Ge}_x$ buffer layers grading beyond 30% Ge at 10%Ge/ μm causes large surface roughness and pile-up, requiring the need to carry out chemical and mechanical polishing once 50% Ge has been reached. The rise in stacking faults in reverse graded buffers appears to be a trade-off in the alternative buffer structure. Stacking faults have also been seen in RSG buffer layers, but a line density could not be gathered from plan view TEM images.

8.2.5. Further development with InSb epilayer

A remarkable breakthrough has been achieved with the successful integration of InSb; the III-V compound which has arguably the greatest lattice mismatch to Si(001) using a high quality Ge buffer layer and AlSb secondary buffer layer. The next stage in the current samples: TMW09017 and TMW09021 is to carry out Hall effect measurements to determine the room temperature electron mobility of the InSb epilayers. Given the high TDD in both of the layers, it is expected that the electron mobility is a fraction of the bulk value. But given the complex heterostructure isolating the InSb layer may prove to be difficult. It may be interesting to suspend the InSb film. This would require applying photoresist to the InSb face, substrate face and then using lithography to create a section of the substrate to etch using tetramethyl ammonium hydroxide and then using reactive ion etching to remove a section of the Ge buffer layer and AlSb buffer layer as well. However, InSb is a very soft metal and so may not withstand the process of suspension used to fabricate Ge membranes [130].

Further to this additional investigation should be carried out into increasing the thickness of the AlSb buffer layer to create a blanket film. It is currently not known how much tensile strain will be imparted in the InSb layer due to thermal mismatch to AlSb. The offcut profile is expected to be preserved in the AlSb layer if it was to become a 2D blanket films as opposed to islands. In which case the tilt in the InSb epilayer may increase from the values measured in the samples in this investigation.

8.2.6. Integration of other III-V heterostructures

With the successful integration InSb, other lower lattice constant III-V materials can be considered for growth on the high quality Ge/6° off-axis Si(001) virtual substrate. GaSb($\text{\AA} = 6.09593$)/InAs($\text{\AA} = 6.0583$) quantum well structures have applications in spintronic devices [189]. Given that the thermal expansion coefficient for InAs being very similar to AlSb, the AlSb/ Ge/6° off-axis Si(001) virtual substrate could be used here to produce silicon electronics industry compatible state of the art III-V spin devices.

9. Appendices

9.1. XRD RSM Calculations

Strain calculations to account for layer tilt for a Ge epilayer on Si(001) as an example. The Ewald sphere radius is $\frac{1}{2}$ and the corresponding reciprocal lattice units are $\lambda/2d$, where d is the plane spacing.

$$\text{Input } Q_X = \frac{1}{2}[\cos(\omega) - \cos(2\theta - \omega)] \quad \& \quad (\text{Equation 9.1})$$

$$\text{Input } Q_Y = \frac{1}{2}[\sin(\omega) + \sin(2\theta - \omega)] \quad (\text{Equation 9.2})$$

Absolute Si(001) co-ordinates are:

$$Q_{X \text{ Absolute Si}(004)} = 0 \quad (\text{Equation 9.3})$$

$$Q_{Y \text{ Absolute Si}(004)} = \frac{\lambda}{2} \times \frac{4}{a_{\text{Si}}} \quad (\text{Equation 9.4})$$

$$Q_{X \text{ Absolute Si}(224)} = \frac{\lambda}{2} \times \frac{2\sqrt{2}}{a_{\text{Si}}} \quad (\text{Equation 9.5})$$

$$Q_{Y \text{ Absolute Si}(224)} = \frac{\lambda}{2} \times \frac{4}{a_{\text{Si}}} \quad (\text{Equation 9.6})$$

Peak shifts in Si due to alignment:

$$\Delta Q_X(004)_{\text{Si}} = Q_{X \text{ Absolute Si}(004)} - \text{Input } Q_{X, (004)\text{Si}} \quad (\text{Equation 9.7})$$

$$\Delta Q_Y(004)_{\text{Si}} = Q_{Y \text{ Absolute Si}(004)} - \text{Input } Q_{Y, (004)\text{Si}} \quad (\text{Equation 9.8})$$

$$\Delta Q_X(224)_{\text{Si}} = Q_{X \text{ Absolute Si}(224)} - \text{Input } Q_{X, (224)\text{Si}} \quad (\text{Equation 9.9})$$

$$\Delta Q_Y(224)_{\text{Si}} = Q_{Y \text{ Absolute Si}(224)} - \text{Input } Q_{Y, (224)\text{Si}} \quad (\text{Equation 9.10})$$

Corrected layer co-ordinates due to alignment for silicon:

$$Q_{X \text{ 004 corrected, Si}} = \text{Input } Q_{X, (004) \text{ Si}} + \Delta Q_X(004)_{\text{Si}} \quad (\text{Equation 9.11})$$

$$Q_{Y \text{ 004 corrected, Si}} = \text{Input } Q_{Y, (004) \text{ Si}} + \Delta Q_Y(004)_{\text{Si}} \quad (\text{Equation 9.12})$$

$$Q_{X \text{ 224 corrected, Si}} = \text{Input } Q_{X, (224) \text{ Si}} + \Delta Q_X(224)_{\text{Si}} \quad (\text{Equation 9.13})$$

$$Q_{Y \text{ 224 corrected, Si}} = \text{Input } Q_{Y, (224) \text{ Si}} + \Delta Q_Y(224)_{\text{Si}} \quad (\text{Equation 9.14})$$

Corrected layer co-ordinates due to alignment for Ge underlayer:

$$Q_{X \text{ 004 corrected, Ge}} = \text{Input } Q_{X, (004) \text{ Ge}} + \Delta Q_X(004)_{\text{Si}} \quad (\text{Equation 9.15})$$

$$Q_{Y \text{ 004 corrected, Ge}} = \text{Input } Q_{Y, (004) \text{ Ge}} + \Delta Q_Y(004)_{\text{Si}} \quad (\text{Equation 9.16})$$

$$Q_{X \text{ 224 corrected, Ge}} = \text{Input } Q_{X, (224) \text{ Ge}} + \Delta Q_X(224)_{\text{Si}} \quad (\text{Equation 9.17})$$

$$Q_{Y \text{ 224 corrected, Ge}} = \text{Input } Q_{Y, (224) \text{ Ge}} + \Delta Q_Y(224)_{\text{Si}} \quad (\text{Equation 9.18})$$

Calculation of tilt (in degrees) in Ge underlayer wrt to Si substrate:

$$\text{Tilt} \left(\frac{\text{Ge}}{\text{Si}} \right) = \tan^{-1} \left(\frac{Q_{X \text{ 004 corrected, Ge}}}{Q_{Y \text{ 004 corrected, Ge}}} \right) \quad (\text{Equation 9.19})$$

Relaxed Ge co-ordinates (corrected for tilt):

$$\alpha_{\text{Si}_{224}} = \tan^{-1} \left(\frac{Q_{Y \ 224 \ \text{corrected, Si}}}{Q_{X \ 224 \ \text{corrected, Si}}} \right) \quad (\text{Equation 9.20})$$

$$\alpha_{\text{Ge}_{224}} = \tan^{-1} \left(\frac{Q_{Y \ 224 \ \text{corrected, Ge}}}{Q_{X \ 224 \ \text{corrected, Ge}}} \right) \quad (\text{Equation 9.21})$$

$$\alpha_{1\text{Ge}} = \alpha_{\text{Si}_{224}} - \alpha_{\text{Ge}_{224}} \quad (\text{Equation 9.22})$$

$$\alpha_{2\text{Ge}} = \alpha_{1\text{Ge}} - \text{Tilt} \left(\frac{\text{Ge}}{\text{Si}} \right) \quad (\text{Equation 9.23})$$

$$R_{1\text{Ge}} = \sqrt{(Q_{X \ 224 \ \text{corrected, Ge}})^2 + (Q_{Y \ 224 \ \text{corrected, Ge}})^2} =$$

distance from origin to relaxed Ge peak before tilt. (Equation 9.24)

$$D_{1\text{Ge}} = R_{1\text{Ge}} \times (\cos(\alpha_{1\text{Ge}})) = \text{Component of } R_{1\text{Ge}} \text{ along the line from origin to Si substrate peak.}$$

$$(\text{Equation 9.25})$$

$$R_{2\text{Ge}} = \frac{D_{1\text{Ge}}}{\cos(\alpha_{2\text{Ge}})} \quad (\text{Equation 9.26})$$

Corrected positions of Ge Q_X and Q_Y are:

$$Q_{X \ 224 \ \text{Ge tilt}} = R_{2\text{Ge}} \times \cos(\alpha_{\text{Si}_{224}} - \alpha_{2\text{Ge}}) \quad (\text{Equation 9.27})$$

$$Q_{Y \ 224 \ \text{Ge tilt}} = R_{2\text{Ge}} \times \sin(\alpha_{\text{Si}_{224}} - \alpha_{2\text{Ge}}) \quad (\text{Equation 9.28})$$

Ge lattice constants are then given by:

$$\text{In-plane lattice constant, } a_{\parallel, \text{Ge}} = \frac{\lambda}{2} \times \frac{2\sqrt{2}}{Q_{X \ 224 \ \text{Ge tilt}}} \quad (\text{Equation 9.29})$$

$$\text{Out-of-plane lattice constant, } a_{\perp, \text{Ge}} = \frac{\lambda}{2} \times \frac{4}{Q_{Y \ 224 \ \text{Ge tilt}}} \quad (\text{Equation 9.30})$$

Ge% in the layer is given by:

$$f(x) = Ax^3 + Bx^2 + Cx + D = 0, \quad (\text{Equation 9.31})$$

Where:

$$A = 0.026 (c_{11\text{Ge}} - c_{11\text{Si}}) + 0.052 (c_{12\text{Ge}} - c_{12\text{Si}}) \quad (\text{Equation 9.32})$$

$$B = c_{11\text{Ge}}(a_{\text{Ge}} - a_{\text{Si}} - 0.026) + c_{11\text{Si}}(a_{\text{Si}} - a_{\text{Ge}} + 0.052) + c_{12\text{Ge}}(2a_{\text{Ge}} - 2a_{\text{Si}} - 0.052) + c_{12\text{Si}}(0.104 + 2a_{\text{Si}} - 2a_{\text{Ge}}) \quad (\text{Equation 9.33})$$

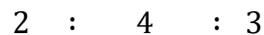
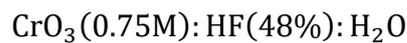
$$C = c_{11\text{Ge}}(a_{\text{Si}} - a_{\perp, \text{Ge}}) - c_{11\text{Si}}(a_{\text{Ge}} + a_{\perp, \text{Ge}} - 2a_{\text{Si}} - 0.026) + c_{12\text{Ge}}(2a_{\text{Si}} - 2a_{\parallel, \text{Ge}}) + c_{12\text{Si}}(2a_{\text{Ge}} + 2a_{\parallel, \text{Ge}} - 4a_{\text{Si}} - 0.052) \quad (\text{Equation 9.34})$$

$$D = c_{11\text{Si}}(a_{\text{Si}} - a_{\perp, \text{Ge}}) + 2c_{12\text{Si}}(a_{\text{Si}} - a_{\parallel, \text{Ge}}) \quad (\text{Equation 9.35})$$

$$c_{11\text{Si}} = 165.8 \text{ GPa}, c_{12\text{Si}} = 63.9 \text{ GPa}, c_{11\text{Ge}} = 128.8 \text{ GPa}, c_{12\text{Ge}} = 48.3 \text{ GPa} \quad (\text{Equation 9.36})$$

9.2. Selective defect etch calculations

Schimmel etchant



R.m.m of $\text{CrO}_3 = 99.9943$

R.m.m of HF = 20.0063432

R.m.m of $\text{H}_2\text{O} = 18.01528$

0.75 moles of $\text{CrO}_3 \approx 75\text{g}$

For a solution of CrO_3 made up to 1litre, the density (ρ) of the solution is 0.075g/ml

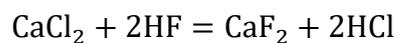
\therefore For 100ml of CrO_3 (@ 0.075g/ml)

The mass of $\text{CrO}_3 = 7.5\text{g}$

Using the above ratio, for 7.5g of CrO_3

200ml of HF(48%) and 150ml of de-ionised water is required

Calcium chloride neutralisation



1) Determining HF amount

48% by weight of HF with a density, $\rho(\text{HF}) = 1.5\text{g/ml}$.

$\therefore 1\text{ml}$ of HF = $1.5\text{g} \approx 0.075$ moles.

For 0.075 moles of HF, 0.0375 moles of CaCl_2 is required to fully neutralise it.

2) Determining amount of $\text{CaCl}_2 \cdot 2\text{H}_2\text{O}$ needed to neutralise HF.

The $\text{CaCl}_2 \cdot \text{H}_2\text{O}$ solution has a density $\rho(\text{CaCl}_2 \cdot 2\text{H}_2\text{O}) = 147.02\text{g/l}$

R.m.m. of $\text{CaCl}_2 \cdot 2\text{H}_2\text{O} = 147$

\therefore mass of $\text{CaCl}_2 \cdot 2\text{H}_2\text{O}$ in 0.0375 moles is given as: $0.0375 \times (147) = 5.5125\text{g}$

\therefore to neutralise 1ml of HF, approximately 37.5ml of $\text{CaCl}_2 \cdot 2\text{H}_2\text{O}$ is required.

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