Cryogenic Characterisation and Modelling of Commercial SiC MOSFETs

L.J. Woodend[1,a], P.M. Gammon[1,b,*], V.A. Shah[1], A. Pérez-Tomás[3],

F. Li[1], D.P. Hamilton[1], M. Myronov[2] and P.A. Mawby[1]

[1] School of Engineering / [2] Department of Physics, University of Warwick, Coventry, CV4 7AL, UK

[3] Catalan Institute of Nanoscience and Nanotechnology (ICN2), CSIC and the Barcelona Institute of Science and Technology, Campus UAB, Bellaterra, 08193 Barcelona, Spain

[a] L.Woodend@warwick.ac.uk   [b] P.M.Gammon@warwick.ac.uk

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Abstract

Two commercial 1.2 kV SiC MOSFETs have been extensively characterised from 30 to 320 K. The temperature dependence of their I/V characteristics, threshold voltage, and breakdown voltage has been examined and are presented in this paper. Overall, the measured characteristics of both devices demonstrate very similar temperature dependencies and it is shown that below ~100 K any further decrease in temperature has little effect on any of the tested characteristics. Increasing temperature beyond 100 K results in a decrease in drain current for a given drain-source and gate-source voltage, a decrease in threshold voltage, and an increase in breakdown voltage. Successful attempts have been made to model the results of these tests by applying theories found in the literature.

Introduction

SiC MOSFETs have several demonstrated advantages over comparable Si power electronics devices, particularly for use in high voltage and extreme-environment applications. Work involving commercial SiC power devices available today has so far demonstrated their high temperature characteristics, showing them to operate beyond 200 °C [1]. However despite growing commercial forces from the Space and super-cooled electronics industries just a handful of studies have investigated the behaviour of these devices in extreme-low temperatures down to 70 K [2], and even fewer have ventured below 50 K [3-4].

The aim of this work is twofold. Primarily it is to assess the suitability of commercially available SiC devices for use in applications, such as the aforementioned, that involve the exposure of power electronics circuitry to cryogenic temperature conditions. Secondly, it is to gain some insight into the device physics that occur in SiC MOSFETs that leads to the temperature dependencies observed during the course of this study.

In order to meet these objectives the threshold voltage, breakdown voltage, and I/V characteristics of two commercially available 1.2 kV n-channel SiC MOSFETs, Device A (Cree CMF20120D) and Device B (Rohm SCT2080KE), have been measured from 30 to 320 K using a Tektronix 371b Curve Tracer. Changes observed in the characteristics of each device with respect to temperature have subsequently been modelled by applying parameters and expressions found in the literature.

Experimental Set-up

The device characterisation process was carried out using a temperature-controlled 'cryogenic' vacuum chamber, in which a packaged device could be mounted and exposed to environmental temperatures between ~20 and 320 K. These temperatures were achieved using a closed cycle liquid-helium chiller, and a Lake Shore temperature controller. With connections made between the gate, source and drain of the device under test at the cold head, and the outside of the chamber, a Tektronix 371b Curve Tracer was used to carry out the electrical measurements.

Results and Discussion

I/V Characteristics: A selection of the I/V characteristics of each device measured at gate-source voltages between 10 and 20 V are shown in Figure 1. In the case of each device, a decrease in temperature gives rise to a decrease in drain current (I_{DS}) for given drain-source (V_{DS}) and gate-source (V_{GS}) voltage conditions. For example, with respect to device A at V_{GS}=10 V and V_{DS}=5 V the measured drain current was 3.5 A greater at 320 K than at 30 K. This occurs due to the temperature dependence of the threshold voltage, which we shall see in Figure 3, and hence when the device is fully turned on at V_{GS}=20 V, the temperature dependence of drain the current appears to diminish, particularly in device B which demonstrate an increase in I_{DS} of just 0.1 A from 30 to 320 K at V_{DS}=1.12 V.

Eq.1 displays the quadratic model for the output characteristics of a MOSFET [5] and was used to produce the results in Figure 2. Measured values of threshold voltage (V_{TH}), shown in Figure 3, were used while $\beta(T)$ and λ represent fitting parameters.

$$I_{DS}(T) = \beta(T)(V_{GS} - \frac{V_{DS}}{2} - V_{TH}(T))(1 + \lambda V_{DS})V_{DS} \qquad (1)$$

This model provides a reasonably close fit to empirical measurements of I_{DS} when V_{GS}=20 V and V_{GS}=10 V where the linear and saturation regions are clearly defined, but fails to reproduce the gradual saturation of drain-current as V_{DS} is increased which is prominent when V_{GS} = 15 V. This behaviour may arise as a result of electron scattering effects caused by charge trapped at the SiC/SiO$_2$ interface when the narrower width of the n-channel at lower gate-source voltages causes a greater proportion of electrons to flow closer to the interface charge traps [6].
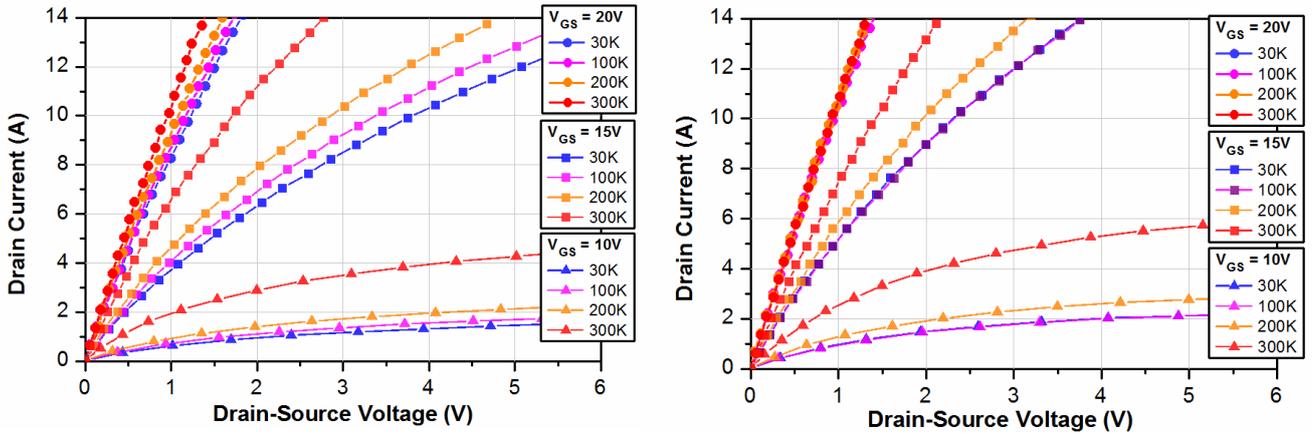

Figure 1: I/V characteristics of device A (left) and device B (right) measured with gate-source voltages of 20 V, 15 V and 10 V, at temperatures of 30 K, 100 K, 200 K, and 300 K.
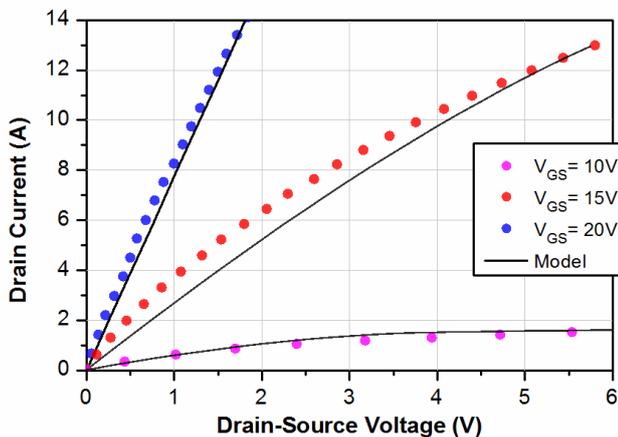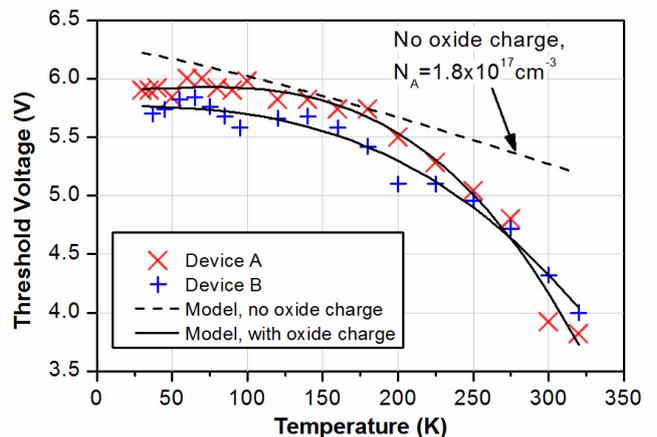

Figure 2: Measured (circles) and modelled (lines) I/V characteristics of device A at 30 K (red crosses) and Device B (blue crosses) along with data modelled using eq.2

Threshold Voltage: Threshold voltage was extracted from the transfer characteristics of each device, measured under a constant drain-source voltage of 10 V, using the constant current method presented in [7]. V_{TH} was taken to be the gate-source voltage at which $I_{DS}=2$ mA

As shown in Figure 3, the threshold voltage of each device decreases non-linearly as temperature is increased. Between 30 and 150 K the threshold voltage of both Device A and Device B remained relatively constant whilst any increase in temperature beyond 150 K yielded a decrease in threshold voltage down to minima of 3.82 V and 4.0 V in Devices A and B respectively.

Eq.2 is a an expression for threshold voltage in which Ψ_{MS} is the metal-semiconductor work function difference, Q_B is the zero-bias depletion region charge under the gate oxide, and ϕ_B is the potential barrier height under the gate oxide. Using an acceptor dopant concentration (N_A) of 1.8×10^{17} cm^{-3} and oxide capacitance (C_{OX}) of 69 nFcm^{-2} [8] while neglecting the effect fixed oxide charge (Q_F) and the temperature dependent charge contained within interface traps (Q_{IT}), the dashed line in Figure 3 was generated [9]. However, the presence of charge at the SiC/SiO$_2$ interface may offset threshold voltage and by using $[Q_F + Q_{IT}(T)]$ as a fitting parameter a close approximation to experimental data was achieved. In order to generate the solid lines in Figure 3 oxide charge densities in the range 0.16 $\times 10^{11}$ cm^{-2} at 150 K to 6.3 $\times 10^{11}$ cm^{-2} at 320 K were extracted in the case of device A.

$$V_{TH} = \psi_{MS} + \frac{Q_B}{C_{OX}} + 2\phi_B - \frac{q[Q_F + Q_{IT}(T)]}{C_{OX}} \tag{2}$$

Breakdown Voltage: Breakdown voltage was measured by applying a large drain-source voltage to a device whilst the gate and source terminals were shorted together, creating a reverse biased pn-junction. Breakdown voltage was said to be the drain-source voltage measured when $I_{DS}=1$ mA.

As shown in Figure 4, the breakdown voltage of each device increased with temperature however this relationship was more prevalent in Device B which demonstrated a maximum breakdown voltage of 1774 V at 320 K compared to 1674 V seen in device A. Both devices maintained reasonably stable breakdown voltages at around 1650 V at temperatures below 100 K. There is little data in

Figure 4: Measured and modelled breakdown voltage of Device A (blue crosses) and Device B (red crosses) against temperature.

the literature to either support or question the observed decrease in temperature dependence as temperature is reduced below 100 K. One possible explanation for this is that heating effects from the movement of carriers in the presence of a large electric field, where a decrease in carrier mobility begins to limit any increase in mean free path, gives avalanche breakdown its positive temperature coefficient, as temperature is decreased [10].

An approximation of the ionization coefficient of a p-n junction undergoing avalanche breakdown, proposed by Fulop in [11] for Si abrupt junctions can be evaluated and written as eq.3 in which W_D is the depletion layer width when breakdown occurs and N_D is the donor dopant concentration. Eq.3 gives avalanche breakdown voltage in terms of A and b which have been used in the literature as temperature dependent fitting parameters [2,12].

$$V_{BD} = \frac{1}{2} \left[\frac{b+1}{A} \right]^{\frac{2}{b+1}} \left[\frac{qN_D}{\varepsilon_{SiC}} \right]^{\frac{(1-b)}{(1+b)}} \tag{3}$$
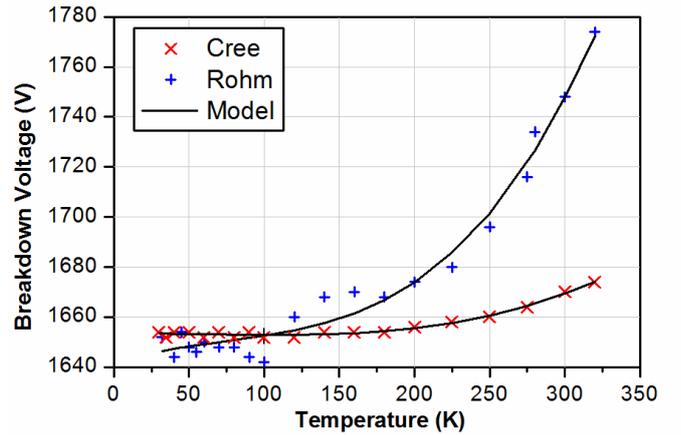
Assuming that $b = 5.8 + 1.2\frac{T}{300}$, empirical approximations found for A that give the fit shown in Figure 4 are $A_{(A)} = 10^{-31}e^{-\frac{16.2T}{300}}$ and $A_{(B)} = 10^{-31}e^{-\frac{16.5T}{300}}$ for devices A and B respectively.

Conclusions

Two commercial 1.2 kV SiC MOSFETs have been characterised from 30 to 320 K and have been shown capable of operation at cryogenic temperatures, however temperature dependencies have been observed and these should be taken into account when designing with devices similar to those used in this study. Threshold voltage has been shown to rise from its room temperature value by as much as 50 % at 30 K whilst breakdown voltage has been shown to decrease by as much as 5.5 % over the same temperature range. However, perhaps the most important changes to consider that have been demonstrated in both tested devices are the decrease seen in drain current with temperature at gate-source voltages below 20 V and the increase observed in threshold voltage. To limit the impact of these temperature dependencies on a system utilizing these or similar devices as part of a switch-mode power supply for example, the applied gate-source voltage should be sufficiently high, at least 20 V based on the results shown in Figure 1 to ensure that a consistent current is supplied.

References

[1] P. Gammon, "Silicon and the wide bandgap semiconductors, shaping the future power electronic device market", *Proc. 14th Int. Conf. Ultimate Integr. Silicon*, 2013.

[2] S. Chen et al., "Cryogenic and High Temperature Performance of 4H-SiC Power MOSFETs", *Applied Power Electronics Conference and Exposition (APEC),* 2013.

[3] H. Chen et al., "Cryogenic Characterization of Commercial SiC Power MOSFETs", *Materials Science Forum, Vols. 821-823,* pp. 777-780, 2015.

[4] P. Gammon et al., "The Cryogenic Testing and Characterisation of SiC Diodes", Vols. 778-780, *Materials Science Forum,* pp. 863-866, 2014.

[5] B. Van Zeghbroek, "MOS Field-Effect-Transistors", *Principles of Semiconductor Devices*, 2004.

[6] S. Potbhare et al., "Characterization of 4H-SiC MOSFET Interface Trap Charge Density Using a First Principles Coulomb Scattering Mobility Model and Device Simulation", *International Conference On Simulation of Semiconductor Processes and Devices*, 2005.

[7] A. Ortiz-Conde et al., "A review of recent MOSFET threshold voltage extraction methods", *Microelectronics Reliability* **42***,* pp. 583-596, 2002.

[8] T. Kimoto and J. A. Cooper, "Unipolar Power Switching Devices", *Fundamentals of silicon carbide technology*, John Wiley & Sons Singapore Pte. Ltd, 2014, pp. 327-343.

[9] S. Potbhare et al., "Numerical and experimental characterization of 4H-silicon carbide lateral metal-oxide-semiconductor field-effect transistor", *Journal of Applied Physics* **100**, **4**, 2006

[10] N. Vukmirović and Lin-Wang Wang, "Carrier Heating in Conjugated Polymers in Electric Field", *Phys. Rev. B* **81**, 2010

[11] W. Fulop, "Calculation of Avalanche Breakdown Voltages of Silicon p-n Junctions," *Solid Sate Electronics,* **10**, pp. 39-43, 1967.

[12] R. Singh and B. Baliga, "Analysis and Optimization of Power MOSFETs for Cryogenic Operation," *Solid-State Electronics* **36***,* **8***,* pp. 1203-1211, 1993.