Relaxation of strained silicon on $Si_{0.5}Ge_{0.5}$ virtual substrates

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Strain relaxation has been studied in tensile strained silicon layers grown on $Si_{0.5}Ge_{0.5}$ virtual substrates, for layers many times the critical thickness, using high resolution x-ray diffraction. Layers up to 30 nm thick were found to relax less than 2% by the glide of preexisting 60° dislocations. Relaxation is limited because many of these dislocations dissociate into extended stacking faults that impede the dislocation glide. For thicker layers, nucleated microtwins were observed, which significantly increased relaxation to 14%. All these tensile strained layers are found to be much more stable than layers with comparable compressive strain. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2975188]

Improvements in the charge carrier transport properties of metal-oxide-semiconductor field-effect transistor (MOSFET) devices have been achieved by inducing tensile strain into their active silicon channel.[1] This tensile strain can be effectively introduced by growing Si on a relaxed SiGe virtual substrate (VS) with the possibility of inducing larger degrees of strain than are currently available by processing techniques.[2] However, relaxation of the VSs requires a high density of 60° dislocation, the threading components of which are subsequently grown into the overlying strained silicon layer. These threading dislocations degrade device performance[3] and can also relax the strained silicon by gliding to form 60° misfit dislocations at the VS/strained layer interface. For strained silicon layers that already contain threading dislocations, the critical thickness is predicted by the mechanical theory of Matthews and Blakeslee[4] to be just 4 nm for growth on a relaxed $Si_{0.5}Ge_{0.5}$ VS. In the absence of such glide induced relaxation, spontaneous 60° dislocation half-loop nucleation is predicted by People and Bean[5] to occur at around 16 nm for 50% Ge composition.

Our previous work[6] showed that *tensile* strained silicon layers on 20% Ge VSs resist relaxation and remain strained up to many times the critical thickness compared to the relaxation of similarly stressed *compressively* strained $Si_{0.8}Ge_{0.2}$ layers on silicon substrates. This was confirmed in Ref. 7 for a set of tensile strained Si layers grown on smoothed $x=0.2$–0.5 VSs, with a maximum strained Si thickness of 24 nm at the highest strain level. Layers in excess of the critical thickness for dislocation nucleation[5] considered in these studies unexpectedly show few dislocation nucleation events.[6–8] Here we present an investigation of the relaxation processes of highly strained silicon on 50% VSs, which offers further potential improvements for MOSFETs especially the *p*-channel. As a wider channel reduces carrier scattering, we particularly look at thick layers (up to 70 nm) for which a different mode of relaxation is found.

As a straining platform, 50% linearly graded VSs were grown by low pressure chemical vapor deposition with a compositional grading rate of 10% μm^{-1} and capped with 2 μm of $Si_{0.5}Ge_{0.5}$. The VS was found to have a threading dislocation density (TDD)$=4(\pm 1)\times 10^5$ cm^{-2} and a linear pile-up density of $0.4(\pm 0.1)$ cm^{-1} using Schimmel etching.[9] A rms surface roughness of $9.5(\pm 0.9)$ nm was found by atomic force microscopy (AFM) over a 20×20 μm^2 area.

A set of strained silicon layers with thickness from 10 to 70 nm was epitaxially grown on top of these VSs using silane at 700 °C. The layer thicknesses were confirmed using cross-sectional transmission electron microscopy (XTEM), with most being well above the critical thickness for relaxation.

For device applications, it is important to understand the effect of thermal processing when Ge diffuses into the strained Si layer, thus reducing the effective thickness and allowing it to relax.[10] Samples with a 35 nm strained Si layer were annealed for 1 h between 750 and 950 °C in a nitrogen atmosphere. The Ge diffusion was measured by ultralow energy secondary ion mass spectroscopy (SIMS). Figure 1 shows that annealing at 750 or 850 °C had little effect on the as-grown Ge profile, where the Ge concentration drops by 1.3 nm/decade. At higher temperatures, significant Ge diffusion from the VS is evident, reaching 4 nm/decade for 950 °C, so annealing was limited to 850 °C for 1 h in our investigations of thermal stability of the tensile strained layers.

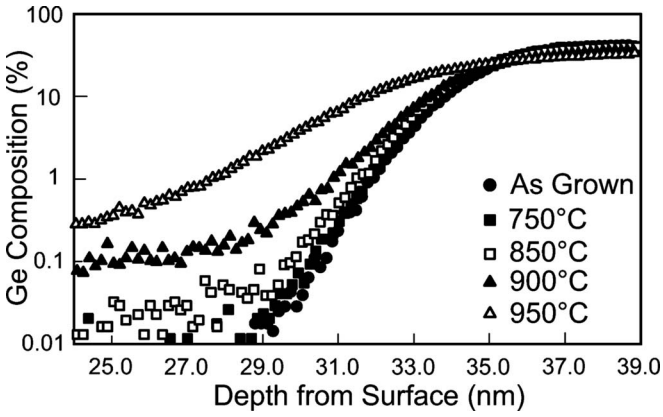

FIG. 1. SIMS depth profiles taken from a 35 nm layer in the as-grown state and after annealing at temperatures between 750 and 950 °C for 1 h.

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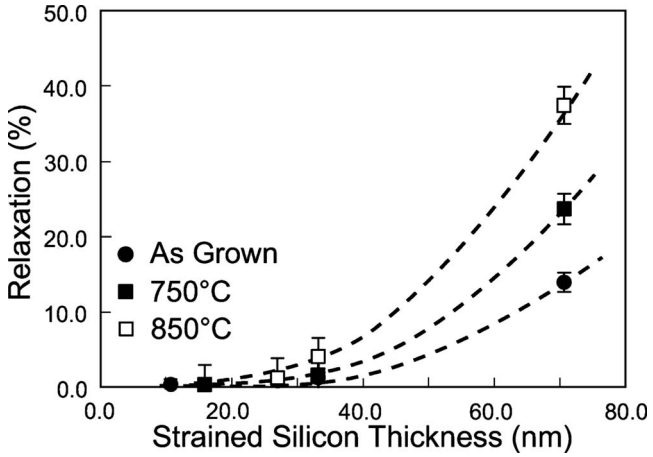

FIG. 2. Relaxation of strained silicon layers measured using HRXRD reciprocal space mapping. Scans were conducted over an 18 h period to minimize errors associated with reduced x-ray intensity diffraction from thin strained silicon layers. Lines are for guidance only.

The degree of relaxation of the strained Si layers was obtained from high resolution x-ray diffraction (HRXRD) using the relative peak positions from the constant composition layer of the VS, the strained Si layer, and the Si substrate. Reciprocal space maps were taken around the (224) and (004) reflections to eliminate layer tilting effects.[11] Figure 2 shows that the as-grown strained silicon relaxation remains at less than 2% for layers up to 35 nm thick. This remarkable stability is consistent with the conclusions of Hartmann *et al.*[8] based on Raman measurements. Furthermore, there is no further relaxation evident after annealing at 850 °C. Even for 70 nm layers, relaxation of the as-grown layer only rises to 14%, although this increases significantly with annealing to 37%. This observed level of relaxation for tensile strained silicon is much lower than that of compressively strained $Si_{0.5}Ge_{0.5}$ of comparable thickness reported elsewhere. For example, a 50 nm thick layer of $Si_{0.5}Ge_{0.5}$ grown on Si at 550 °C was measured to be 60% relaxed, which increased to 95% for a thickness of 120 nm,[12] and a 45 nm layer of $Si_{0.4}Ge_{0.6}$ was found to be 71% relaxed.[13] In both cases, relaxation was observed to occur via a combination of the modified Frank–Read (MFR) multiplication mechanism[14] and surface roughening in the form of a three-dimensional island formation.[15]

To find the origin of the much greater stability and understand the relaxation processes in these tensile strained Si layers, we have employed AFM and XTEM. In both the as-grown state and after annealing, dislocations in layers thinner than 30 nm were observed by XTEM (Fig. 3) to be either 60° dislocations or extended stacking faults, which form when a 60° dislocation dissociates into a pair of 90° and 30° Shockley partial dislocations. Under strain the force on the 90° partial dislocation is greater than that on the 30° partial dislocation[16] and, as the former leads the dissociation for tensile strain, it can glide away from the trailing 30° partial dislocation and create an extended stacking fault. Observation of extended stacking faults together with misfit dislocations suggests that relaxation in these layers, thinner than 30 nm, is *glide dominated*. The limited degree of relaxation observed can be attributed to the stacking faults pinning the strain-relieving misfit dislocation and inhibiting glide, as previously postulated as a source of stability.[17] For compressive

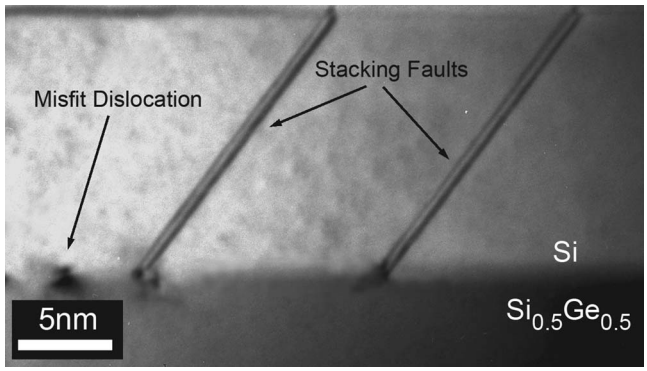

FIG. 3. XTEM image of a 15 nm strained silicon layer showing two stacking faults and a misfit dislocation.

strain the 90° partial dislocation trails but still experiences the larger force, so stacking faults cannot form and impede relaxation in compressively strained layers.

AFM observations show that all layers adopt the cross-hatching of their underlying VS and have a rms surface roughness less than 0.5 nm different from that of the VS with no evidence of three-dimensional islands. As in previous reports,[6,7] this shows that strain is not being relieved by islanding and the ultimate smoothness of the tensile strained layer is determined by the platform on which it is produced.

As stacking faults are known to affect electronic device performance,[18] the critical thickness for their formation has implications in device manufacturing. Figure 4 shows an estimate of this thickness obtained by considering the forces acting on a gliding 90° partial dislocation in a strained layer, using the equations of Matthews and Blakeslee[4] and Hull and Bean.[15] Above 20% Ge equivalent strain, the glide of 60° threading dislocations to form misfit dislocations becomes less favorable than their dissociation and the glide of 90° partial dislocations to form stacking faults. Here we observed both stacking faults and misfit dislocations in a 7 nm strained Si layer, but further work is required to see if stacking faults

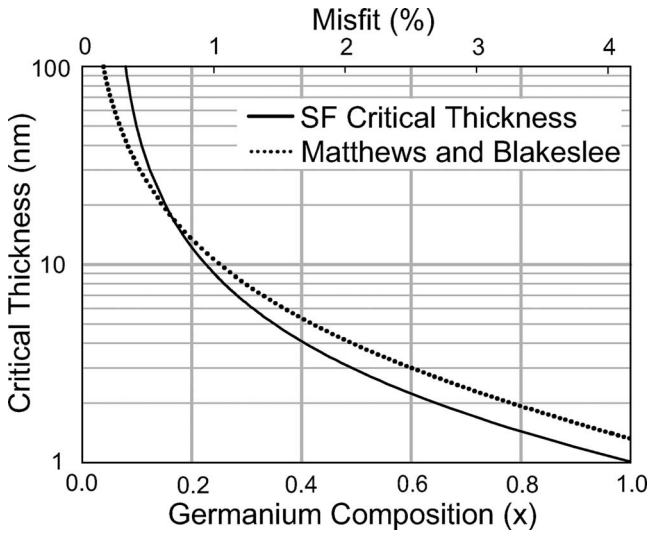

FIG. 4. Estimated critical thickness for stacking fault formation and the Matthews and Blakeslee critical thickness. The formation of stacking faults by the glide of the leading 90° partial dislocation becomes more energetically favorable than the glide of the 60° dislocation itself above a Ge composition of 20%.

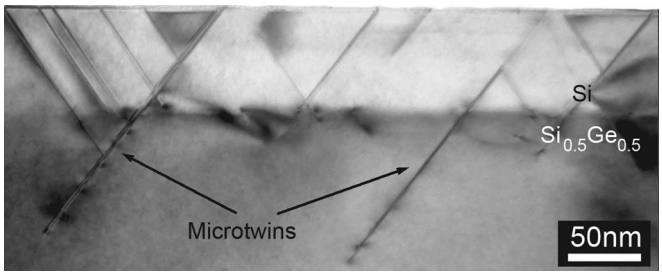

FIG. 5. XTEM image of a 70 nm strained silicon layer showing a high density of microtwins, indicating that relaxation of thicker layers are nucleation dominated.

form in thinner layers than misfit dislocations as suggested by Fig. 4.

The increase in relaxation beyond a thickness of 35 nm (in Fig. 2) coincides with the XTEM observation of nucleated microtwins, which initially form by the surface nucleation of a 90° partial dislocation half loop. This half loop creates a surface step that favors the nucleation of other 90° partial dislocation half loops on adjacent glide planes;[19] however, these mutually repel and result in a stack of 90° partial dislocations extending into the VS along the [111] direction. A significantly higher density of microtwins is observable in the 70 nm layer (Fig. 5), which we associate with the increased relaxation at 70 nm in Fig. 2 and represents a change from glide dominated to *nucleation dominated* relaxation. VS designs with a lower TDD will therefore be unable to reduce relaxation in these thicker layers. After annealing, the number of nucleated microtwins observable in the 70 nm layer does not significantly increase; however, 60° misfit dislocations are observed below the misfit interface. This could be due to the early stages of the MFR mechanism,[14] in which dislocations are injected into the substrate through multiplication events. It is suggested that this multiplication process, rather than an increase in the density of microtwins or stacking faults, is responsible for the increased relaxation at 70 nm after annealing evident in Fig. 2.

In conclusion, tensile strained silicon grown on 50% Ge content VSs to many times the equilibrium critical thickness has been shown to relax much less than equivalent compressively strained layers. Relaxation was found to be dominated by the glide of threading dislocations originating from the VS up to a layer thickness of around 35 nm. It is suggested that the presence of extended stacking faults in these layers inhibits dislocation glide and limits relaxation to less than 2%. Improvements in the VS design to reduce the density of threading dislocations would therefore reduce relaxation and the formation of extended stacking faults in these glide dominated layers. As the layer thickness exceeds 35 nm, nucleated microtwins become evident, and relaxation increases significantly to 14% at 70 nm. Annealing further increases relaxation by what appears to be the early stages of the MFR multiplication process. The predicted formation of extended stacking faults at a thickness of around 7 nm has a profound implication in obtaining defect free strained silicon layers of a useable thickness for device processing.

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