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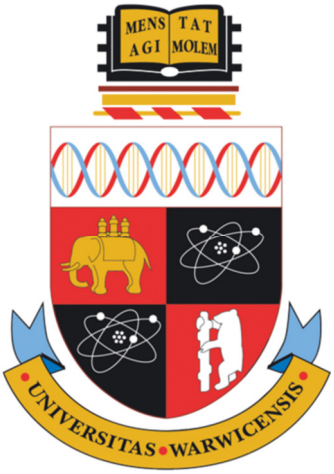

Wafer Scale Heteroepitaxy of Silicon Carbon and Silicon Carbide Thin Films and their Material Properties

by

Gerard Colston

Thesis

Submitted to the University of Warwick

for the degree of

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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has been composed by myself and has not been submitted in any previous application for any degree.

The work presented (including data generated and data analysis) was carried out by the author except in the cases outlined below:

- Material growth within the ASM Epsilon 2000 RP-CVD was carried out by Dr. Maksym Myronov
- SIMS measurements were carried out externally by Evans Analytical Group (EAG)

Parts of this thesis have been published by the author.

Publications and Presentations

The following publications, presentations and patents result directly from the investigations studied within this thesis and other investigations that I was involved in during the period of study.

Journal Publications

1. **G. Colston** and M. Myronov, *"Controlling the Optical Properties of monocrystalline 3C-SiC Heteroepitaxially Grown on Silicon at Low Temperatures"*, Semicond. Sci. Technol. (2017) (accepted).
2. L. Q. Zhou, **G. Colston**, M. J. Pearce, R. G. Prince, M. Myronov, D. R. Leadley, O. Trushkevych, and R. S. Edwards, *"Non-linear vibrational response of Ge and SiC membranes"*, Appl. Phys. Lett. **111**, 5, 011904 (2017).
3. **G. Colston**, S. D. Rhead, V. A. Shah, O. J. Newell, I. P. Dolbnya, D. R. Leadley, and M. Myronov, "Mapping the strain and tilt of a suspended 3C-SiC membrane through micro X-ray diffraction", Materials & Design **103**, 244 (2016).
4. **G. Colston**, S. D. Rhead, V. A. Shah, O. J. Newell, I. P. Dolbnya, D. R. Leadley, and M. Myronov, *"Mapping the Strain State of 3C-SiC/Si (001) Suspended Structures Using μ-XRD"*, Material Science Forum **858**, 274 (2016).
5. **G. Colston**, M. Myronov, S. Rhead, and D. Leadley, *"Analysis of surface defects in $Si_{1-y}C_y$ epilayers formed by the oversaturation of carbon"*, Semicond. Sci. Technol. **30**, 114003 (2015).
6. V. A. Shah, S. D. Rhead, J. Finch, M. Myronov, J. S. Reparaz, R. J. Morris, N. R. Wilson, V. Kachkanov, I. P. Dolbnya, J. E. Halpin, D. Patchett, P. Allred, **G. Colston**, K. J. S. Sawhney, C. M. Sotomayor Torres, and D. R. Leadley, *"Electrical properties and strain distribution of Ge suspended structures"*, Solid-State Electron. **108**, 13 (2015).

Additional publications are in preparation which cover the low temperature deposition of 3C-SiC but are delayed due to the patenting of the growth process. Publications relating to other topics that are in preparation are noted in the text.

Conference Presentations

1. *Effect of Thickness on the Optical Properties of monocrystalline 3C-SiC Epilayers grown on Silicon*, The 10th International Conference on Silicon Epitaxy and heterostructures (ICSI) 14 – 19 May 2017 University of Warwick, **G. Colston** and M. Myronov. *(Awarded Best Poster Prize)*
2. *SiC thin film anode for LIB*, The 57th Battery Symposium 29 November – 1 December Chiba, Japan, A. Nurpeissova, A. Molkenova, A. Mukanova, **G. Colston**, Z. Bakenov, M. Myronov.
3. *Wafer scale heteroepitaxy of very high crystalline quality 3C-SiC on a standard Si substrate*, E-MRS Spring Meeting 2 – 6 May 2016 Lille, M. Myronov and **G. Colston**.
4. *Mapping the strain state of 3C-SiC/Si(001) suspended structures using μ-XRD*, Size-Strain-VII 21 – 24 September 2015 Oxford, **G. Colston**, S. D. Rhead, V. A. Shah O. J. Newell, I. P. Dolbnya, D. R. Leadley and M. Myronov.
5. *Low temperature epitaxy of crystalline 3C-SiC on standard Si (001) substrates*, 16th International Conference on Silicon Carbide and Related Materials (ICSCRM) 4 – 9 October 2015 Giardini Naxos, M. Myronov, **G. Colston** and S. D. Rhead.
6. *Origin of Surface Defects in RP-CVD Grown $Si_{1-y}C_y$ Epilayers by the Oversaturation of Carbon*, Microscopy of Semiconducting Materials (MSM-XIX) 29 March – 2 April 2015 Cambridge, **G. Colston**, M. Myronov, S.D. Rhead and D.R. Leadley.
7. *RP-CVD Growth of High Carbon Content Si1-xCx Epilayers Using Disilane and Trimethylsilane Precursors,* 7th International Silicon-Germanium Technology and Device Meeting (ISTDM) 2-4 June 2014 Singapore, M. Myronov, S.D. Rhead, **G. Colston** and D.R. Leadley.
8. *Disilane and Trimethylsilane as Precursors for RP-CVD Growth of $Si_{1-y}C_y$ Epilayers on Si(001),* 15th International Conference on Ultimate Integration of Silicon (ULIS) 7-9 April 2014 Stockholm, **G. Colston**, M. Myronov, S.D. Rhead and D.R. Leadley.
9. *SiC thin film anode for LIB*, 57th Battery Symposium 29 November – 1 December 2016 Tokyo, A. Nurpeissova, A. Molkenova, A. Mukanova, **G. Colston**, Z. Bakenov and M. Myronov.

10. *Silicon carbide thin film as negative electrode for lithium ion batteries*, The 20th Topical Meeting of the International Society of Electrochemistry 19-22 March 2017 Buenos Aires, A. Mukanova, M. Myronov, **G. Colston**, D. Batyrbekuly, A. Moldabayeva, A. Molkenova, Z. Bakenov.
11. *3C-SiC thin film as negative electrode for Li-ion batteries*, European Materials Research Society (EMRS) Spring Meeting 22-26 May 2017 Strasbourg, A. Mukanova, **G. Colston**, D. Batyrbekuly, A. Molkenova, A. Nurpeissova, M. Myronov, Z.Bakenov.

Patents

1. M. Myronov, **G. Colston** and S. Rhead "Growing epitaxial 3C-SiC on single-crystal silicon" G.B. Patent Application GB1513014.9 (23 July 2015).
2. M. Myronov, **G. Colston** and S. Rhead "3C-SiC based sensor" G.B. Patent Application GB1517173.9 (29 September 2015).

Abstract

For years now, many have believed the solution to reducing the cost of the wide bandgap compound semiconductor silicon carbide (SiC) is to grow its cubic form (3C-SiC) heteroepitaxially on silicon (Si). This has the potential to reduce cost, increase wafer size and integrate SiC with Si technology. After decades of research, 3C-SiC grown on Si is still yet to penetrate the commercial market as the process is plagued with various issues such as very high growth temperatures, thermal stresses, high cost, poor epitaxial material quality and poor scalability to wafer sizes beyond 100 mm diameter.

The first section of this thesis starts with a focus on the traditional, high temperature growth of 3C-SiC carried out in the first industrial type SiC based reduced pressure chemical vapour deposition (RP-CVD) reactor installed in a UK University. After the process demonstrated little promise for mass scale implementation into the semiconductor industry, a radical change in strategy was made.

The research pivoted away from SiC and instead focussed on silicon carbon alloys ($Si_{1-y}C_y$) with carbon (C) contents in the range of 1-3%. $Si_{1-y}C_y$ has a range of applications in strain engineering and reducing contact resistance, differing from 3C-SiC quite significantly. Crystalline alloys with C contents around 1.5% were achieved using an industry standard Si based RP-CVD growth system. Analysis was carried out on the defects that form due to the saturation of C in higher content alloys. The high temperature annealing of $Si_{1-y}C_y$ resulted in out diffusion of C and traces of 3C-SiC growth which presented itself as a potential buffer layer for 3C-SiC epitaxy.

Through the careful selection of growth precursors and process optimisation, high crystalline quality 3C-SiC was grown heteroepitaxially on Si within the industry standard Si based RP-CVD and in-depth material characterisation has been carried out using a vast range of techniques. High levels of electrically active dopants were incorporated into the 3C-SiC and its electrical properties were investigated.

Various investigations were carried out on suspended 3C-SiC and $Si_{1-y}C_y$ films including strain and tilt measurements through micro X-ray diffraction and the effect of thickness and doping on their optical properties. The results led to a greater understanding of suspended films and provide a foundation for a number of applications in microelectromechanical systems (MEMS) and optical devices.

Further material growth research was carried out on $Si_{1-y}C_y$ multilayers, selective epitaxy of 3C-SiC and the growth of 3C-SiC on suspended growth platforms. Each topic presents an interesting area for further research.

The research presented demonstrates new, state of the art 3C-SiC heteroepitaxial material and its basic structural, electrical and optical properties. A new low-cost and scalable process has been developed for the heteroepitaxial growth of 3C-SiC on Si substrates up to 100 mm with a clear path to scaling the technology up to 200 mm and beyond. Not only does the developed technology have a high commercial impact, it also paves the way for many interesting future research topics, some of which have been briefly investigated as part of this work.

Abbreviations

μT – Microtwin

AC – Alternating Current

AFM – Atomic Force Microscopy

ALD – Atomic Layer Deposition

APD – Anti-Phase Domain

BF – Bright-Field

CCC – Closed Cycle Cryostat

CMOS – Complementary Metal Oxide Semiconductor

CMP – Chemical Mechanical Polishing

CVD – Chemical Vapour Deposition

DC – Direct Current

DF – Dark-Field

EDS – Energy Dispersive Spectroscopy

ELO – Epitaxial Lateral Overgrowth

FCC – Face Centred Cubic

FIB-SEM – Focussed Ion Beam-Scanning Electron Microscope

FTIR – Fourier Transform Infrared Spectroscopy

FWHM – Full Width at Half Maximum

FZ – Floating Zone

HR – High Resolution

HT – High Temperature

IDB – Inversion Domain Boundary

IGBT – Insulated Gate Bipolar Transistor

IR – Infrared

LASER – Light Amplification by Stimulated Emission of Radiation

LED – Light Emitting Diode

LO – Longitudinal Optic

LT – Low Temperature

MBE – Molecular Beam Epitaxy

MEMS – Microelectromechanical System

MMS – Monomethylsilane

MOCVD – Metal Organic Chemical Vapour Deposition

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

PECVD – Plasma Enhanced Chemical Vapour Deposition

PIPS – Precision Ion Polishing System

PVD – Physical Vapour Deposition

PV-TEM – Plan-view Transmission Electron Microscopy

QCL – Quantum Cascade Laser

RCA – Radio Corporation of America

RF – Radio Frequency

RIE – Reactive Ion Etch

RMS – Root Mean Squared

RP-CVD – Reduced Pressure Chemical Vapour Deposition

RSM – Reciprocal Space Map

SAED – Selective Area Electron Diffraction

SEM – Scanning Electron Microscope

SF – Stacking Fault

SIMS – Secondary Ion Mass Spectroscopy

SOI – Silicon on Insulator

SSP – Single Source Precursor

ST – Straight Through

TCS – Trichlorosilane

TEM – Transmission Electron Microscope

TLM – Transfer Length Method

TMS – Trimethylsilane

TO – Transverse Optic

UHV – Ultra High Vacuum

UV – Ultraviolet

XPS – X-ray Photoelectron Spectroscopy

XRD – X-Ray Diffraction

X-TEM – Cross-Sectional Transmission Electron Microscopy

Chapter 1
Introduction

1.1 The History of the Semiconductor

The first study of semiconductor behaviour can be traced back to Michael Faraday in 1833, investigating the temperature dependence on electrical conductivity of silver sulphide. In 1873, Willoughby Smith discovered photoconductivity in selenium, another interesting property of semiconductors. The first patent of a semiconductor device was filed in 1901 by Sir J C Bose, who invented a semiconductor based rectifier capable of receiving wireless signals for radio waves [1].

Although much work led to the greater understanding of semiconductors, the birth of the semiconductor industry is typically attributed to the invention of the transistor. The first transistor was demonstrated by R Hilsch and R. W. Pohl in 1938 by attaching three electrodes to a potassium bromide crystal [2]. In 1947 John Bardeen, Walter Brattain and William Shockley applied the same technology to semiconductor materials at Bell labs [3]. Due to its reduced melting point, making it easier to work with, germanium (Ge) was the semiconductor used for the first junction transistors. While certain properties of Ge make it more efficient than silicon (Si) in some aspects, the wider bandgap of Si makes it more ideal for use in transistors, as it reduces thermally excited carriers and hence leakage current. When bulk Si crystals were finally produced at the same quality of Ge in 1952 [4], Si took over as the predominant material in the microelectronics industry for many years. Although Si still dominates the market in complementary metal oxide semiconductor (CMOS) technology, other semiconductors including Ge and other compounds have found their place in the semiconductor industry, offering properties superior to Si in many applications.

The key property of semiconductors is that their electrical properties can be manipulated by the introduction of impurities. A defect free semiconductor will act as a perfect insulator at absolute zero. At elevated temperatures, some thermally excited charge carriers will exist in the material. Charge carriers, electrons or holes, can be introduced into the semiconductor with the addition of donor or acceptor impurities respectively. For group IV semiconductors (Si, Ge, diamond), this is a relatively simple concept, a group III element (boron (B), aluminium (Al), gallium (Ga)) will act as an acceptor and a group V element (phosphorus (P), arsenic (As), nitrogen (N), antimony (Sb)) will act as a donor. For compound semiconductors formed of combinations of group III-V or even II-VI elements, doping becomes more complex, as it depends on which atomic sites the impurities incorporate.

The combination of n-type (donor), p-type (acceptor), intrinsic (undoped / pure), dielectrics and metal interfaces are the basis of almost all semiconductor based devices. While other materials are used for specific applications, Si still dominates around 99% of the semiconductor industry, hence, compatibility with Si technology, such as being able to grow particular semiconductors on a Si substrate wafer is essential nowadays for the mass implementation of other novel materials, see Figure 1.1.

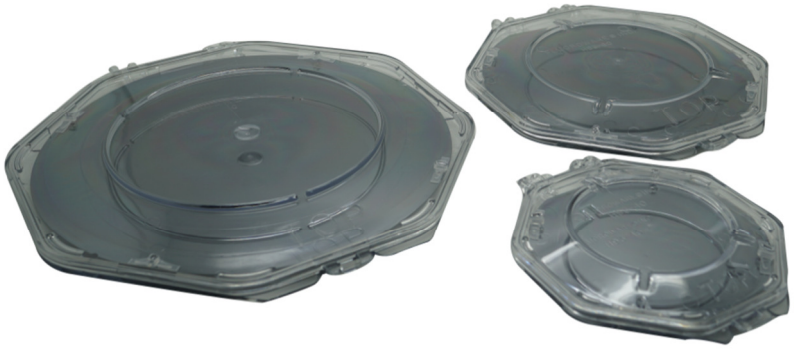

Figure 1.1 Si substrates of 200, 150 and 100 mm diameter, held in clamshell wafer trays.

1.2 Compound Semiconductors

Compound semiconductors are formed through the combination of different elements from the periodic table to give a compound with a defined crystal structure and exactly 8 electrons in its outer orbital, giving it semiconductor behaviour just like the group IV elemental semiconductors (Si, Ge, C and Sn). This can be achieved using binary compounds comprising elements from groups III-V, II-VI and I-VII or ternary or even quaternary alloys. As compound semiconductors are formed from different elements

they can become polar which leads to interesting electronic properties such as increased electron mobility and direct band gaps [5].

Compound semiconductors have various applications spanning photonics, optoelectronics and radio frequency (RF) communications. One of the most commonly used compound semiconductors in industry today is gallium arsenide (GaAs) which has been used for infrared and red light emitting diodes (LEDs) since 1962 [6] and is still prevalent in mobile devices for wireless communication [7], although SiGe alloys are becoming more competitive in mobile devices through strain and bandgap engineering [8]. Another important compound semiconductor is gallium nitride (GaN) which can exist in either cubic (zinc-blende) or hexagonal (Wurtzite) form. GaN is another direct bandgap semiconductor, but it has a large band gap of around 3.4 eV at room temperature, comparing to 1.43 eV for GaAs, which makes it ideal for light emission and detection in the ultraviolet (UV) / blue spectrum. GaN based ternary alloys form the foundation of all modern blue LEDs which are key to domestic and industrial LED lighting [9]. GaN also has applications in very high frequency RF communication devices [10] and power electronic devices for the automotive sector [11].

Although they offer many advantages in certain applications, compound semiconductors are not without their issues. Si is still by far the most commonly used semiconductor as it is easy to manipulate, large wafers (up to 450 mm) can be manufactured at low-cost and the material is extremely prevalent in the world. Compound semiconductors, however, can be difficult to work with. GaAs is one of the most mature compound semiconductors but is still limited to wafer sizes of up to 150 mm diameter in volume production [12]. These substrates are significantly more expensive than equivalent Si wafers making GaAs devices more expensive and difficult to produce on the levels commonly found in the Si industry. The situation is even worse for other compounds such as GaN which is currently limited to wafer sizes of 50 mm and can be many orders of magnitude more expensive than larger Si wafers [13]. Due to these issues with substrates, many researchers and industries have turned to growing thin films of compound semiconductors on other substrates. Si is the best option when it comes to price, quality and scalability but in some cases not suitable. GaN is an interesting case where a clear substrate choice has not yet been realised. Various substrates are used for the growth of GaN including Si, sapphire and SiC, however, each offer certain advantages and disadvantages [14]. Growing on dissimilar substrates can

lead to a huge number of issues such as increased crystal defects and high levels of stress in the heterostructures, which can lead to cracks, see Figure 1.2.

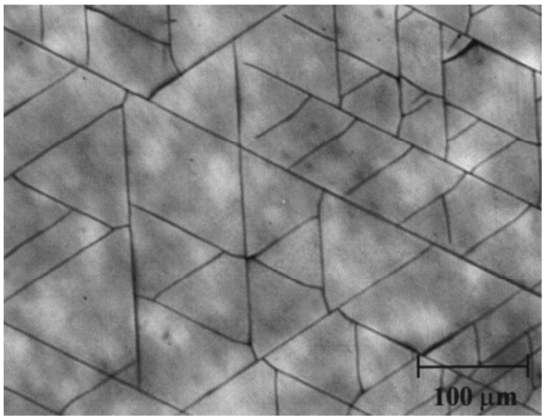

Figure 1.2 Cracks in a GaN film grown on sapphire. Taken from [15].

1.3 Silicon Carbide

Silicon carbide (SiC) is another very interesting compound semiconductor and is the primary focus of this research. SiC is the only compound semiconductor that can be formed from group IV elements (C, Si, Ge, Sn) as it possesses a defined crystal bonding structure consisting entirely of Si-C bonds (assuming defect free material). Other elements from group IV instead form alloys when combined ($Si_{1-x}Ge_x$, $Ge_{1-x}Sn_x$ etc.). SiC is a effectively a cross between pure Si and diamond and possesses many properties similar to the latter that make it ideal for a range of applications including high power, high frequency and high temperature devices, these are discussed later in section 2.3.

The first synthesis of SiC most likely goes back to 1824 when Jöns Berzelius identified Si-C bonds in one of the samples he produced [16]. In 1892 Edward Acheson used a smelting furnace to produce abrasive materials to replace diamond. By mixing silica and coke he was able to synthesise SiC, which he named carborundum [17]. Acheson discovered pockets of hexagonal crystals in his SiC samples which led to the discovery of polytypism, that SiC can exist in a number of different crystalline forms, see section 2.3.

While SiC can be used as an abrasive, its electrical properties were first exploited in 1907 with the first demonstration of an LED fabricated from SiC [18]. While SiC gained much interest in the early 1900's from researchers, the inability to commercialise any devices from the material led to its decline while other semiconductors like Si and Ge dominated the market. In 1959, W. G. Spitzer *et al.* demonstrated the first growth of

cubic silicon carbide (3C-SiC) on Si substrates [19], however, little research on SiC followed. It took until 1978 for another advance in SiC technology when Tairov and Tsvetkov invented the seeded sublimation process for growing SiC crystals which made use of a thermal gradient from a sublimed Si/C source to a cooler seed crystal [20]. This process allowed ingots of SiC to be produced which could later be sliced and polished into wafers, thus producing the SiC substrate.

In 1987 a process for epitaxially growing high quality SiC films on "off-axis" SiC substrates was invented in a process known as step-controlled epitaxy [21]. This led to the creation of Cree Inc. in 1987, a company that still today one of the leading suppliers for SiC based materials and devices. While SiC devices have still not penetrated the mass market, SiC wafers continue to be sold as substrates for GaN which is then used for LED, RF and power applications [22].

Although SiC substrates have been in production for many years they are still limited to smaller wafers sizes and are significantly more expensive that equivalent Si wafers. One of the most attractive solutions to this issue is to grow 3C-SiC on Si substrates which combines the properties of SiC with the cost point and scale of Si. There are various issues with this process that will be discussed later, however, one of the most detrimental to this concept is the thermal mismatch between SiC and Si, which leads to high levels of thermal stress in the heterostructure. This leads to an effect known as wafer bow, see Figure 1.3, which distorts 3C-SiC/Si wafer making them unsuitable for device fabrication.

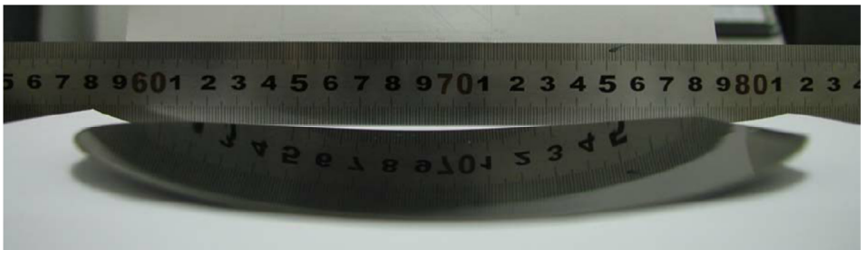

Figure 1.3 Wafer bow of a 6.7 µm thick 3C-SiC epilayer grown on a 150 mm diameter Si (111) substrate. Taken from [23].

After years of research in the growth of 3C-SiC on Si there is yet to be a breakthrough in the process that allows the full integration of this wide bandgap compound semiconductor into the microelectronics industry. This is the primary focus of the research presented here.

Chapter 2
Theoretical Background

2.1 Semiconductors

Semiconducting materials such as Si, Ge and other compound semiconductors tend to be crystalline. A crystal is a solid with a regular repeated atomic structure which can be defined by the repetition of a simple unit cell. Although there are some applications of amorphous semiconductors, such as amorphous silicon in solar cells, the lack of order in amorphous materials leads to inferior electronic properties, however, production of a-Si is significantly cheaper than its crystalline form which can overcome reduced electrical properties for certain applications [24].

Two of the most common crystal structures of semiconductors, and the focus of materials in this thesis, are diamond cubic and zinc-blende, both of which are equivalent structures consisting of two face centred cubic (FCC) lattices where one is shifted by ¼ of a unit cell in the [111] direction. Zinc-blende differs from diamond cubic only by the fact that the 2nd FCC lattice is formed from a different element. Examples of diamond cubic include Si and Ge while gallium arsenide (GaAs) and 3C-SiC are zinc-blende. In either case, the elements are covalently bonded to each other in tetrahedral symmetry by a process known as sp^3 hybridization, whereby each atom uses its 1 s and 3 p electron states to produce 4 sp^3 bonds with other atoms, hence the tetrahedral symmetry. In the case of Si the bonding electrons come from 3s and 3p states while for germanium the electrons are from 4s and 4p states.

Semiconductors are defined by the size of their bandgap, the energy between the highest occupied energy states (valence band) and lowest empty energy states (conduction band). The origin of the bandgap can be described using various theoretical and modelling techniques, the two most common being the nearly free electron model and the tight binding approach. The periodic potential set up by the positive atomic nuclei at

lattice sites in the crystal creates energy gaps in the possible electron states, the separate bands between gaps are referred to as Brillouin zones, the unit cells of the reciprocal lattice, see Figure 2.1.

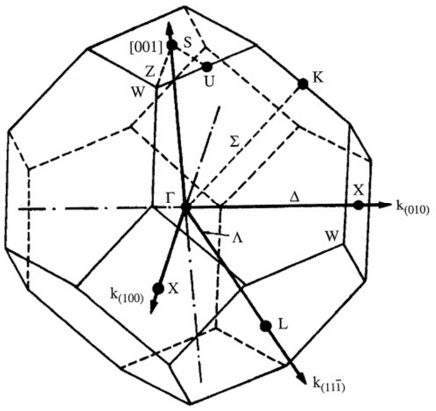

Figure 2.1 The first Brillouin zone of the group IV (Si, Ge, 3C-SiC) and compound semiconductors with zinc-blende crystal structure (GaAs). The centre of the Brillouin zone is defined as the Γ-point [25].

In the case of semiconductors, the number of valence electrons available exactly fills an integer number of Brillouin zones such that the Fermi energy (energy of the highest occupied state) lies in the energy gap between a full and empty Brillouin zone [26]. The energy gap between the highest occupied valence band and lowest unoccupied conduction band can be separated by a distance in reciprocal space (k-space). Semiconductors which exhibit this effect are referred to as indirect band gap semiconductors and include the group IV semiconductors (Si, Ge, SiC, diamond) and a handful of compound semiconductors. When there is no gap in k-space it is referred to as a direct band gap semiconductor (GaAs, GaN), see Figure 2.2. For an electron transition to occur from the valence band to the conduction band in a direct band gap semiconductor, energy incident on the material must simply exceed the band gap. This is not the case for indirect band gap semiconductors, as incident energy that exceeds the band gap must also coincide with a momentum transfer in k-space. This can be provided by a sufficient lattice vibration (phonon), however, the probability of this occurring is significantly lower than the direct transition in a direct band gap semiconductor. Indirect band gap semiconductors such as Si or Ge are therefore poor detectors of light; the same is true for the emission of light, which is far more efficient in direct band gap semiconductors such as GaAs or GaN and justifies their use in LEDs and high efficiency photovoltaics [27].

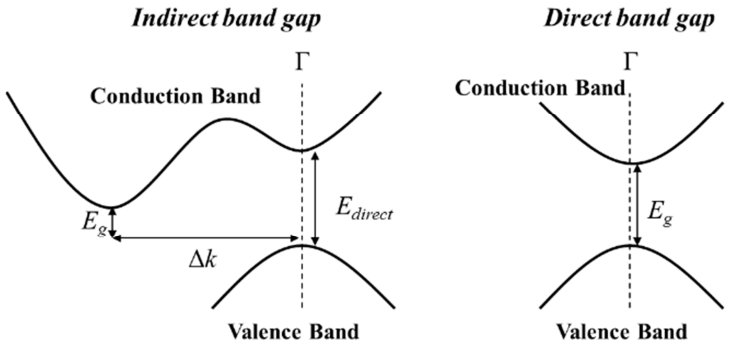

Figure 2.2 Schematic of an indirect and direct band gap system.

The unique property of semiconductors over other materials is that their electrical properties can be manipulated through doping. For a dopant to become electrically active it must take up a substitutional lattice site rather than sit interstitially in the lattice. If an element from group V is substitutionally incorporated in Si and forms the necessary four covalent bonds, it will have an additional 'unbound' electron. This electron will be loosely bound to the impurity due to the positive nature of the ion. This binding energy (E_D) is typically on the order of 10-50 meV and can normally be overcome by thermal energy at room temperature (~25 meV), allowing the additional electron to excite into the conduction band, see Figure 2.3. In this case, the impurity is referred to as a donor and the semiconductor is said to be n-type. If an element from group III is substitutionally incorporated in the lattice instead, the system gains an additional hole (lack of electron), the impurity is referred to as an acceptor and the semiconductor becomes p-type. When the temperature of a semiconductor is reduced below the binding energy the dopants cease to be fully ionised, this is referred to as freeze-out. Under normal operating conditions of doped semiconductors the number of carriers (electrons or holes) is usually entirely dictated by the impurity concentration and the semiconductor is said to be extrinsic. If the temperature increases significantly then thermally excited carriers can exceed the impurity concentration and the semiconductor is said to become intrinsic.

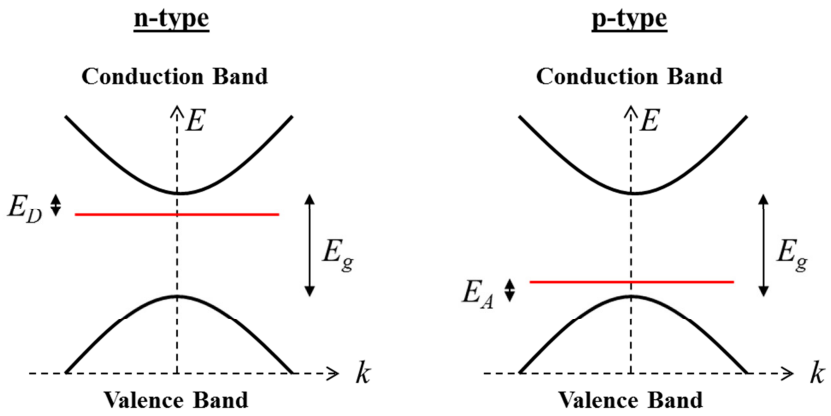

Figure 2.3 Electron energy states in n-type (left) and p-type (right) doped semiconductors.

Another important property of thin film semiconductors is that their structure can be manipulated through the introduction of strain, briefly discussed in section 2.2. Strain is when a crystal structure is altered from its natural, relaxed state and is typically induced through heteroepitaxy on a substrate of a different crystal structure. As the electrical properties of semiconductors is based on the crystal structure, strain can have a profound effect on a number of properties of semiconductors including electron and hole mobility, effective masses and even the nature of the band gap [28]. Manipulating the properties of a semiconductor with strain is known as strain engineering and has been used to increase the mobility of device channels and even alter the band gap of Ge to facilitate more direct transitions for light emission and detection [29].

2.2 Epitaxy

Epitaxy is the process of depositing a crystalline layer on top of another crystalline layer or substrate, the result of which is often referred to as an epi wafer. While Si dominates the semiconductor market offering the largest and cheapest wafers, various other substrates are available, see Table 2.1.

While many materials can be grown epitaxially on Si substrates, they are often not the best choice, due to variations in crystal structures and properties. Using other substrates can increase epilayer quality and subsequently device performance; however, cost is always a factor that must be considered for commercial applications.

Table 2.1 Typical semiconductor substrate sizes, costs and their main commercial applications. Costs were calculated from prices offered by University Wafer and MTI Corp. as of 22/09/2017.

Material	**Si**	**Ge**	**GaAs**	**GaN**	**SiC (4H/6H)**	**Sapphire**
Commercial wafer sizes (mm)	≤ 450	≤ 200	≤ 200	≤ 50	≤ 150	≤ 200
Approximate Cost ($/cm^2)	0.1	4	2	200	10	2
Common epilayers	Si, Ge, SiC, GaAs, GaN…	Ge, GaAs, graphene…	GaAs, InGaAs…	GaN, AlGaN…	SiC, GaN, graphene	GaN
Applications	CMOS, RF, Power, LEDs, Sensors	RF	RF	RF, Power, LEDs	RF, Power, LEDs	LEDs

The grown layer is referred to as an epilayer which continues the crystalline structure and orientation of the substrate and can range in thickness from single atomic layers to tens or even hundreds of microns. Epitaxy offers high quality monocrystalline thin films as well as fine control over layer thickness and doping profiles of either single or multiple, stacked epilayers [30].

The two main techniques of epitaxy include molecular beam epitaxy (MBE) and chemical vapour deposition (CVD). MBE growth occurs through the deposition of material on a crystalline substrate with a thermal beam of atoms or molecules emitted from one or more targets under ultra-high vacuum [31]. MBE is an excellent research tool as it allows fine control over growth parameters and can be used to grow complicated structures and novel compounds, but does not offer the throughput necessary for mass volume manufacturing and substrate temperatures are often limited to <1100 °C for Si and even lower for certain III-Vs.

CVD is a process of growing thin solid films on a substrate through the chemical reaction of vapour-phase precursors, which distinguishes it from other physical vapour deposition (PVD) processes such as MBE. There are a large number of ways to promote these chemical reactions from precursor sources including thermal, high frequency light (UV) or plasma assistance. While thermally induced CVD is the most commonly found growth method in the semiconductor industry other types have their advantages. Plasma enhanced CVD (PECVD), for example, makes use of electrical energy to induce chemical reactions which allows thin film growth at significantly lower growth temperatures and is often used for materials that typically require very high energies to form such as diamond [32]. Another form of thin film deposition is by using metal-

organic precursors which have been given their own acronym MOCVD. In this growth method, the growth precursors strictly must contain metal-carbon bonds; however, the term MOCVD now covers growth using a range of precursors including metal-oxygen and metal nitrogen bonds. MOCVD is the dominant growth method used for the epitaxy of GaN films and other compound semiconductors [33].

While CVD processes are very complex, the main stages of epitaxial growth can be summarised in a few significant steps, see Figure 2.4. The precursors are first transported into the reactor (1) before they undergo reactions to create intermediate and gaseous by-products (2), this step is instigated by the reaction method of CVD (thermal, plasma, UV etc.) and depends entirely on the precursor(s) used in the growth process. Mass transport of the reactants brings them to the substrate surface at which point they are adsorbed (3), this process is reversible and the precursor can be desorbed from the surface (5). Diffusion of the adsorbed species can occur allowing the new adatoms to reach nucleation sites which leads to film formation (4). Finally, mass transport of the remaining fragments from the decomposition of the precursors occurs and is removed from the reactor in the exhaust (6).

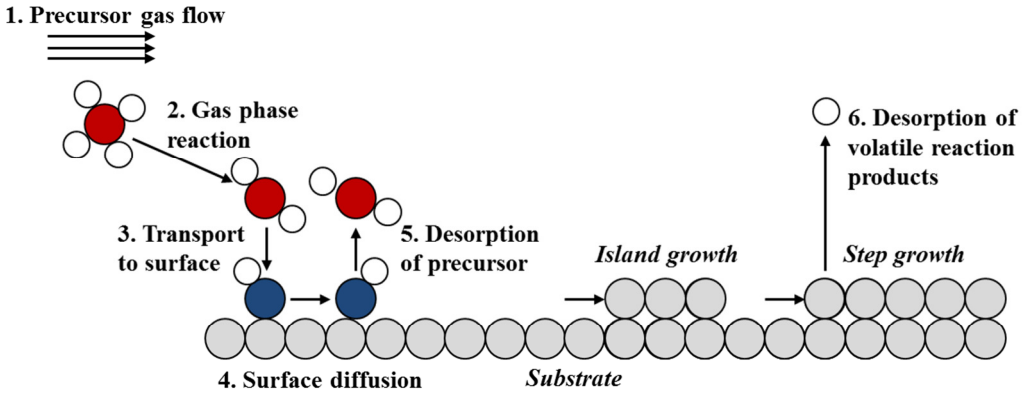

Figure 2.4 Main transport and reaction processes in the CVD epitaxy [34].

All material growth for the present research was carried out using thermal CVD. The growth rate and quality of material grown in traditional thermal CVD is dependent on a range of parameters including growth temperature, reactor pressure, precursor flow rates, compositions and others. One of the critical issues of CVD is that the effects of each of these parameters often depend on others which makes optimising growth conditions a long and iterative process. The growth rate of thin films can depend heavily on temperature in thermal CVD processes. Increasing the growth temperature speeds up the kinetics of the reactions occurring in the gas phase or on the substrate, steps 2 and 4

in Figure 2.4 and is referred to as the *kinetic regime.* In this regime there is an overabundance of reactants available in the gas phase, therefore the diffusion gradient across the boundary layer between the gas flow and the substrate surface is high. As the temperature and speed of surface reactions increases, the diffusion gradient lowers and the growth rate of the process becomes limited by the mass transport of reagents to and from the substrate surface, steps 3, 5 and 6. At this point the growth rate no longer increases significantly with temperature; this is referred to as the *mass transport regime*. The two cases can be understood by plotting the logarithmic growth rate (k) against the inverse temperature (T) in an Arrhenius plot, see Figure 2.5. Both regimes follow an exponential relationship according to

$$k = Ae^{\frac{-E_a}{k_B T}} \qquad \text{Equation 2.1}$$

where A is a constant, k_B is the Boltzmann constant and E_a is the activation energy of the reaction. The activation energy of the mass transport regime is lower than that of the kinetic regime.

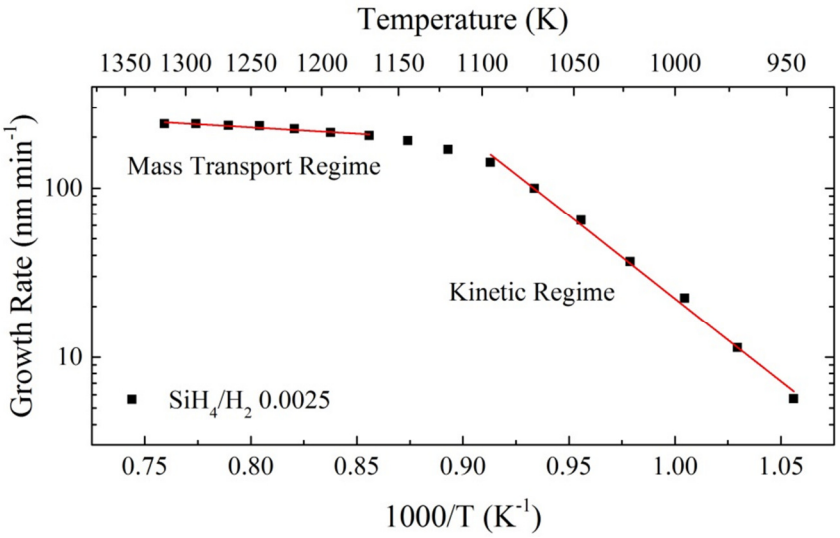

Figure 2.5 Growth rate of Si when using SiH_4 as a function of temperature, adapted from [35].

Pressure is another important factor for CVD growth as it controls the boundary layer between the gas phase reactions and the substrate surface, hence controlling the mass transport stages of epitaxy. At pressures ranging from atmospheric down to ~10 Torr both kinetics and mass transport play an important part of epitaxial growth, while at significantly lower pressures ($<1 \times 10^{-4}$ Torr) mass transport has almost no effect on growth. While it would seem ideal to grow under ultra-high vacuum (UHV) conditions for epitaxy, this significantly increases growth costs and reduces throughput as

maintaining UHV conditions is time consuming and costly. Most of the semiconductor industry tends to run growth systems either operating at atmospheric or reduced pressure (~100 Torr).

Precursors

Precursors are compounds that are used to grow epitaxial layers within the CVD system. They can come in gaseous or liquid states but are always injected into the CVD in gaseous form. Precursors are typically injected at flow rates on the order of standard cubic centimetres per minute (sccm) in a H_2, N_2, Ar or He carrier gas flowed at standard litres per minute (slm), where 1 slm is equal to 1000 sccm. Precursors decompose onto the substrate through various heat induced reactions (in a thermal based CVD) which vary depending on the precursor choice. There are several requirements that precursors must adhere to such as: high volatility at growth conditions but otherwise stable, high purity and long lifetime. Ideally precursors should also be low-cost and have a low hazard risk such that they can be handled easily.

One of the standard and most simple precursors used in the silicon industry is silane (SiH_4). However, even this simple precursor can undergo a range of different chemical reactions during epitaxy, depending on the growth conditions used. For example, silane can dissociate in the gas phase leading to the following reactions:

$$SiH_{4(g)} \leftrightarrow SiH_{2(g)} + 2H_{2(g)}$$

$$SiH_{2(g)} + (*) \leftrightarrow SiH_{2(*)}$$

$$SiH_{2(*)} \rightarrow Si_{(s)} + (*) + H_{2(g)}$$

here $(*)$ represents a crystal surface site while the subscript represents the molecule is bonded to a surface site and (g) and (s) indicate whether a molecule is in a gas or solid form. However, silane can undergo polymerization in the gas phase leading to the formation of disilane (Si_2H_6) which then bonds to a surface site and leads to deposition [36]. The use of more complex and multiple precursors can complicate these reactions even further which has led to an entire field focussed on modelling CVD growth conditions. These models will not be discussed further in this work, however, the author recommends *Chemical Vapour Deposition* by A. Jones and M. Hitchman for further reading on the topic [34].

Growth Modes

When atoms are deposited onto the surface of a crystalline substrate they are referred to as adatoms which can then migrate across the surface until they fall into a suitable lattice site. This is referred to as migration and depends on a range of parameters of the growth system including the temperature, chemical species and the strain of the system. If the migration length is sufficiently long enough then the free energy of the system is reduced most effectively by the adatoms bonding into lattice sites at the edges of steps on the substrate surface. This leads to 2-dimensional film growth with a smooth surface roughness and is referred to as Frank van der Mewre growth, see Figure 2.6 (a). However, if the adatoms lack the energy to reach a step terrace, or the surface interactions are too great, then the adatoms will instead bond to the surface of a terrace which will lead to subsequent adatoms nucleating on the same site. This results in 3-dimensional island growth which increases the surface roughness of the film and is referred to as Volmer-Weber growth, see Figure 2.6 (b). This type of growth is more likely to occur in highly mismatched systems such as growing 3C-SiC on Si as the surface energy is greater due to the presence of lattice mismatch and strain [37]. It is possible for the growth of a film to begin under the Frank van der Mewre regime, however, as surface effects become more severe due to film thickness increasing, the system can transition to Volmer-Weber growth. This occurs with Ge heteroepitaxy on Si and is referred to as Stranski-Krastinov growth, see Figure 2.6 (c). For more information on the interactions between surfaces and adatoms the author recommends *Surface Science: An Introduction* by J. Hudson [38].

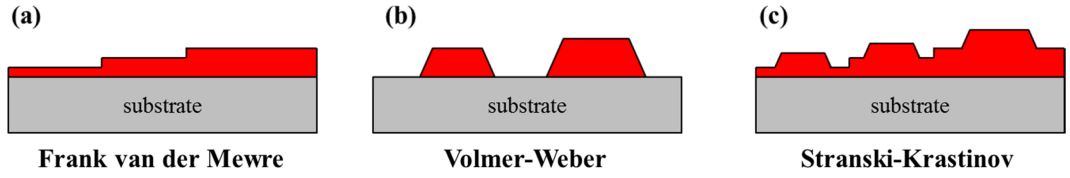

Figure 2.6 Possible growth modes of thin films through epitaxy.

Homoepitaxy and Heteroepitaxy

Epitaxy of semiconductor thin films can be categorised into two types: homoepitaxy and heteroepitaxy, see Figure 2.7. Homoepitaxy is the case where a thin film is grown on a substrate of the same material, for example Si on a Si substrate or Ge on a Ge substrate. This form of epitaxy is useful for achieving high crystalline quality epilayers

and accurately controlling the electrical properties of the films through doping with impurities or growth under ultra-high purity conditions keeping the material undoped and of high resistance. Heteroepitaxy is the process where a thin film is grown on a substrate of a different material, for example Ge on Si or GaAs on Ge. Heteroepitaxy is extremely useful for the growth of materials that either do not have native substrates such as alloys ($Si_{1-x}Ge_x$ etc.) or where substrates are either limited in quality, wafer size or are extremely expensive, such as Ge or GaN substrates. It is also crucial for the heterogeneous integration of other semiconductor materials into the silicon industry by growing epilayers on Si substrates. While heteroepitaxy seems like an ideal solution for growing high quality semiconductor films on non-native substrates, there is almost always some mismatch between the crystal structure of the substrate and the thin film which leads to either compressive or tensile strain and ultimately crystal defects in the epilayer, once the thickness exceeds some critical value.

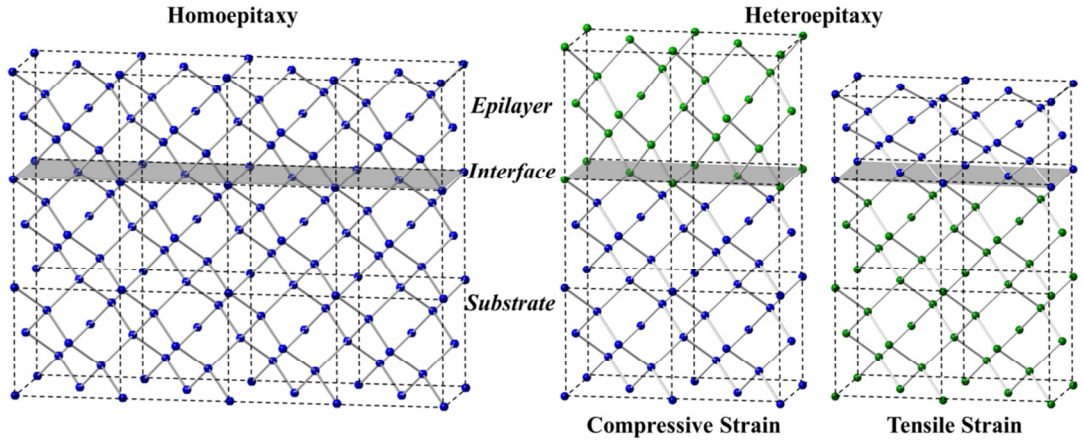

Figure 2.7 Representation of the crystal structures of thin films grown by homoepitaxy (left) and heteroepitaxy (right). The epilayer grown by heteroepitaxy is seen to distort to match the structure of the substrate. If the epilayer crystal structure has a larger lattice constant then it becomes compressively strained (i.e. Ge/Si) while if the epilayer crystal structure has a smaller lattice constant then it undergoes tensile strain (i.e. Si/Ge).

2.3 Silicon Carbide

SiC is a compound semiconductor formed from equal compositions of Carbon (C) and Si. The basic building block of SiC is the tetrahedron formed of four C atoms covalently bonded to a Si atom by sp^3 hybridization (or vice versa), see Figure 2.8.

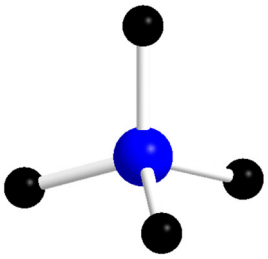

Figure 2.8 Tetrahedron formed from the covalent bonding of four C atoms to a single Si atom.

These building blocks bond with each other to create a hexagonal bilayer comprising Si atoms with C atom above it, denoted pictorially as spheres in Figure 2.9. The positions of the atoms in the first hexagonal bilayer can be assigned the letter A. The next bilayer above can take one of two positions, B or C. It is not possible for the next bilayer to take the same position as either of its nearest neighbours.

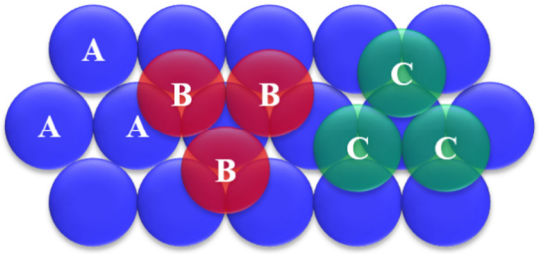

Figure 2.9 A pictorial representation of the hexagonal bilayer where the C-Si atoms are denoted by spheres.

By forming repeated stacking sequences of these hexagonal bilayers it is possible to create a large number of unique crystal structures of SiC. These are referred to as polytypes. Some of the most important polytypes include 2H-SiC (ABAB…), 4H-SiC (ABCBABCB…), 6H-SiC (ABCACBABCACB…) and 3C-SiC (ABCABC…). The notation of polytypes includes a number specifying the length of the repeated stacking sequence and a letter indicating the crystal structure, see Figure 2.10.

It is commonly stated that there are over 200 polymorphs of SiC which can result in a number of crystalline structures including hexagonal, rhombohedral and cubic. 2H-SiC is the simplest polytype and has the largest bandgap of 3.3 eV, while the only cubic structured polytype is 3C-SiC which has the smallest bandgap of all the SiC polytypes of 2.4 eV [37].

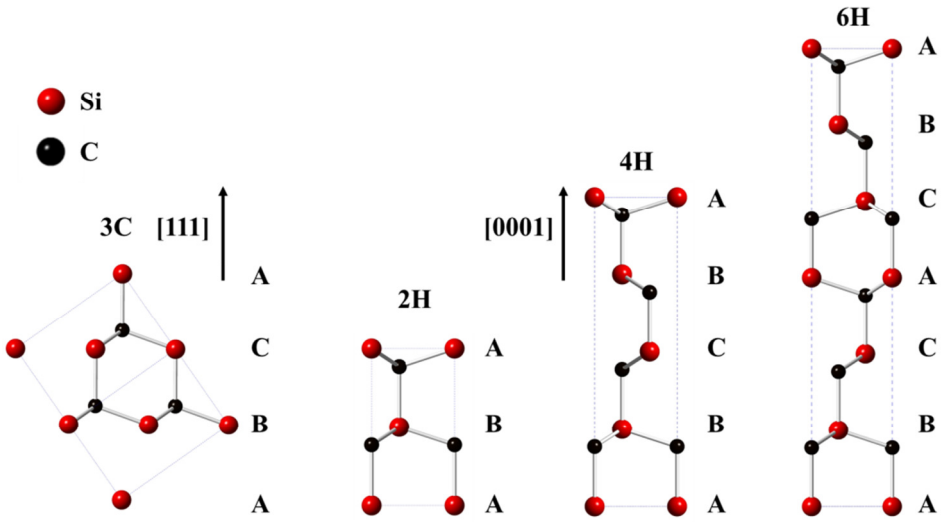

Figure 2.10 Unit cells of 3C-SiC, 2H-SiC, 4H-SiC and 6H-SiC, going from left to right. Blue dots indicate Si atoms and black dots C atoms.

One of the key differentiators between the polytypes is how their properties vary in different directions within the crystal. This anisotropy is an important factor to consider when fabricating devices and is one of the advantages of 3C-SiC as it has a purely isotropic crystal structure. One such example of anisotropy is the electron mobility which has been shown to vary in 4H, 6H and 15R polytypes depending on whether measurements were made perpendicular or parallel to the c-plane [39]. Table 2.2 gives a comparison of the most important SiC polytypes in industry and research as well as other semiconductors.

2.3.1 Physical Properties

SiC is well known for being an extremely hard substance and is commonly used as an abrasive material in its amorphous form. With a Mohs hardness of 9.2-9.3 it is one of the hardest naturally occurring substances known to man, superseded only by a handful of materials including boron nitride (~9.5) and diamond (10). SiC is chemically inert at room temperature to almost all chemicals, one exception to this is a mixture of hydrofluoric acid (HF) and nitric acid (HNO_3) which has been shown to etch polycrystalline SiC at etch rates of up to 50 Å/min [40]. Other wet etchants of SiC include molten alkaline salts, such as potassium hydroxide (KOH), at temperatures approaching 600 °C.

Table 2.2 Comparing the typical material and electrical properties of SiC polytypes with other common semiconductors and crystals at room temperature [41-46]. The electrical properties of non-cubic structures are often anisotropic and the parameters can depend heavily on crystal orientation.

Property	**Silicon**	**Diamond**	**Germanium**	**3C-SiC**	**4H-SiC**	**6H-SiC**	**GaAs**	**Sapphire**	**GaN (hexagonal)**	**GaN (cubic)**
Crystal Structure	Diamond	Diamond	Diamond	Zinc-blende	Wurtzite (Hexagonal)	Wurtzite (Hexagonal)	Zinc-blende	Rhombo-hedral	Wurtzite (Hexagonal)	Zinc-blende
Lattice Constant (Å)	5.431	3.57	5.658	4.3596	a = 3.073 c = 10.053	a = 3.073 c = 15.117	5.65	a = 4.76 c = 13.0	a = 3.189 c = 5.186	4.55
Equivalent hexagonal 'a' constant for (111) orientation (Å)	*3.840*	*2.52*	*4.002*	*3.073*	*NA*	*NA*	*3.99*	*NA*	*NA*	*3.189*
Lattice Mismatch to Si (001) (%)	0	34.3	4.2	19.7	NA	NA	4.0	NA	NA	16.2
Mohs Hardness	7	10	6	9	9	9	4.5	9	6-7	6-7
Bandgap (eV)	1.12	5.46 - 5.60	0.66	2.4	3.2	3.0	1.43	10	3.4	3.3
Dielectric Constant	11.7	5.7	16.2	9.7	9.7	9.7	12.9	11.5	9.7	9.7
Thermal Conductivity (W $cm^{-1}K^{-1}$ at 300 K)	1.5	<24	0.6	3-4	3-4	3-4	0.5	0.3	1.3	1.3
Critical Electric field (MV cm^{-1})	0.25	>10	0.1	2	2.2	2.5	0.3	*NA*	3	~3
Electron Mobility ($cm^2V^{-1}s^{-1}$)	1450	4500	3900	1000	950	500	8500	*NA*	1000	760
Hole Mobility ($cm^2V^{-1}s^{-1}$)	480	3800	1900	40	120	80	400	*NA*	30	200

While this inertness of SiC can be a hindrance during device fabrication, it makes SiC an ideal material for use within harsh environments in which devices may be exposed to physical stress or corrosive chemicals.

SiC is referred to as a wide bandgap semiconductor, a term typically given to semiconductors with a bandgap significantly greater than that of Si (1.1 eV). All SiC polytypes have indirect bandgaps, however, the magnitude of this bandgap varies between polytypes.

The intrinsic carrier concentration of a semiconductor can be approximated by

$$n_i = \sqrt{N_C N_V} e^{-\frac{E_g}{2k_B T}} \quad \text{Equation 2.2}$$

where N_C and N_V are the effective density of states in the conduction and valence bands respectively, E_g is the bandgap, k_B is the Boltzmann constant and T the temperature. Semiconductors with larger bandgaps will exhibit lower intrinsic carrier concentrations allowing them to remain extrinsic at higher temperatures. This is one of the many factors which limits the use of Si based devices at elevated temperatures, above approximately 200 °C. Wider bandgap materials such as SiC polytypes can overcome this limitation and allow devices to operate up to temperature beyond 600 °C [47].

Another important property of SiC is its high thermal conductivity which again varies between polytypes. Thermal conductivity dictates how efficiently a material can dissipate heat and influences device lifetime. SiC based power devices have been shown to dissipate heat more effectively than Si or GaN based devices and one area of interest is implementing these devices into automotive systems as it reduces the cooling systems required [48]. High thermal conductivity in SiC substrates is also utilised in GaN/SiC based power devices as the substrate has been shown to help dissipate heat more effectively from the GaN devices, improving their performance [49].

2.4 3C-SiC

Of all the SiC polytypes there is only one with a cubic structure. Cubic silicon carbide, commonly referred to as 3C-SiC or β-SiC, has a stacking sequence of ABCABC… which results in a purely zinc-blende structure. 3C-SiC has various advantages over other polytypes of SiC such as the lowest bandgap and highest potential electron mobility and saturation drift velocity, a result of reduced phonon scattering from its higher crystal symmetry [50].

At the high temperatures found in the seeded sublimation process (typically >2000 °C), 3C-SiC is an unstable polytype of SiC and the formation of hexagonal and rhombohedral SiC will dominate [51]. At low temperatures (<1400 °C), however, 3C-SiC is one of the only polytypes that can stabilise due to its cubic crystalline structure. The reduced thermal budget required to grow 3C-SiC is a key advantage and allows the material to be epitaxially grown at temperature below 1410 °C, this temperature is critical in particular as it is approximately the melting point of Si. As 3C-SiC has a zinc blende structure (Figure 2.11), equivalent to the diamond structure of Si, it is possible to heteroepitaxially grow 3C-SiC on Si. Si is the substrate of choice for 3C-SiC as it allows growth on large wafer sizes up to 300 mm, wafers are low cost and are grown to very high purity.

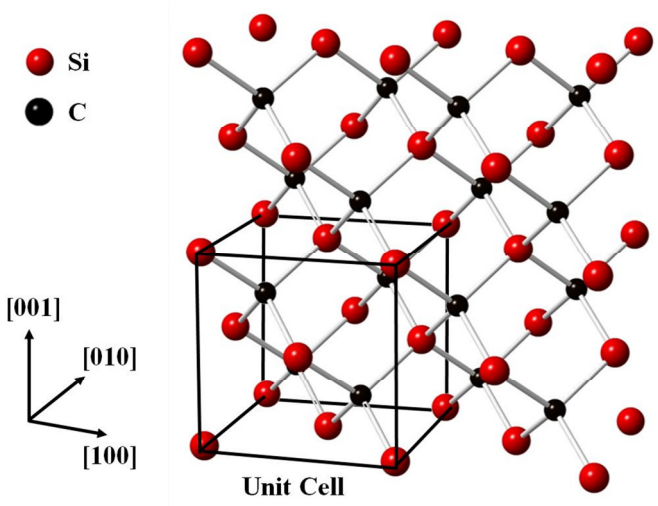

Figure 2.11 Zinc-blende crystal structure of 3C-SiC showing the cubic unit cell outlined in black.

A common drawback for the growth of 4H-SiC or 6H-SiC is that the temperatures required to grow these epilayers (>1600 °C) also allow the formation of other SiC polytypes, including 3C-SiC. Due to the thermal stability of 3C-SiC, it is almost impossible to have inclusions of other polytypes when growing 3C-SiC on Si. The downside to performing heteroepitaxy is that the lattice constant of 3C-SiC (4.3589 Å) is 19.7% mismatched from the lattice constant of Si (5.4311 Å) which leads to a high number of defects at the interface between the two materials that propagate throughout the 3C-SiC epilayer [52].

Although 3C-SiC has the smallest bandgap of all the SiC polytypes, this can also be seen as an advantage as it reduces the electric field required for channel inversion within

metal oxide semiconductor field effect transistors (MOSFET) and reduces the density of traps at SiO_2/3C-SiC interfaces which can help increase the drift mobility inside the channel [53].

2.5 3C-SiC Growth

The first growth of 3C-SiC on Si was reported in 1959 by Spitzer *et al.* [19] who reported on the infrared properties of 3C-SiC grown on a Si wafer using methane at a growth temperature of 1300 °C, simply converting the surface layer of the Si into 3C-SiC. Today, precursors containing both C and Si are used to grow 3C-SiC on Si, ideally without including any of the Si from the substrate. Research into 3C-SiC growth declined in the late 1970's as interest shifted towards hexagonal SiC polytypes. The next milestone in 3C-SiC epitaxy came in 1982, when Nishino *et al.* [54] successfully grew 3C-SiC on small Si substrates using a multi-step CVD process critically, including a carbonisation process through the use of propane before the growth of 3C-SiC at a temperature of 1330 °C. This is considered to be a crucial step in achieving high quality 3C-SiC when grown at high temperatures and has been the focus of much research into the field of 3C-SiC heteroepitaxy. Chen *et al.* developed a 4-step growth process in 2009 that includes a pre-clean step in H_2 followed by carbonisation in propane, a diffusion step in H_2 before the epilayer growth at 1420 °C using silane and propane [55]. The resulting epilayers showed higher crystalline quality and the process was found to prevent the formation of voids at the interface, see Section 2.6.4. The authors concluded that voids were prevented by the carbonisation step, while the diffusion step allowed residual C-C bonds to transform into Si-C bonds producing a more favourable surface for 3C-SiC growth.

2.5.1 Precursor Composition

The choice of gaseous precursors for the growth of 3C-SiC is vital for achieving high quality epilayers and understanding the requirements of growth conditions to achieve heteroepitaxy.

Multiple Source Precursors

One of the most common combinations of precursors for 3C-SiC heteroepitaxy is silane (SiH_4) and propane (C_3H_8) which can typically produce growth rates of around 3 μm/hr.

Many other precursor variants have been investigated including: silane and ethylene (C_2H_4) [56], trichlorosilane ($SiHCl_3$) and ethylene and acetylene (C_2H_2) and dichlorosilane (SiH_2Cl_2) [57] to name but a few. These types of multiple source precursors tend to require high growth temperatures in order to deposit crystalline 3C-SiC. This is because C source precursors require more energy to breakdown due to the higher dissociation energy of CH_3-H bonds (~104.8 kcal/mol) compared to equivalent SiH_3-H bonds (~90 kcal/mol). An interesting feature of these bonds is that the dissociation energy of the SiH_2-H bond (64 kcal/mol) is significantly lower than that of SiH_3-H allowing higher reactivity in polysilane precursors, however, the analogous bond of CH_2-H (~111 kcal/mol) is in fact larger than CH_3-H reducing reactivity further [58]. Multiple source precursors do offer an advantage in that the C/Si ratio can be accurately controlled during epitaxy by adjusting to the flow rate of either source. The C/Si ratio has been found to be a critical variable in the growth of 3C-SiC and has been studied by Chassange *et al.* in the silane propane growth system [59].

Single Source Precursors

Single source precursors are gases which contain both Si and C and can be used to grow 3C-SiC without any other precursors. They offer some advantages over multisource precursors such as simpler chemical reactions, being safer to handle and offering higher efficiency when producing Si-C bonds. A key benefit of multisource precursors is that they are often made up of weaker bonds allowing them to dissociate at reduced temperatures. This can allow the growth of 3C-SiC at temperatures closer to those found in Si epitaxy (~1100 °C). For example, the dissociation process of hexamethyldisilane ($Si_2(CH_3)_6$) has been studied and it is found that the rate limiting step is the breaking of the Si-Si bond within the $(CH_3)_3Si$-$Si(CH_3)_3$ a far weaker bond than methyl based reactions, which allows thermal decomposition at temperature below 700 °C [60]. Various single source precursors have been investigated for the growth of 3C-SiC such as: disilabutane ($CH_3SiH_2CH_2SiH_3$) at 1200 °C [61], hexamethyldisilane at 1000 °C [62] and tetramethylsilane (C_4SiH_{12}) at 1170 °C [63] to name a few. The downside of single source precursors is that the C/Si ratio is fixed by the composition of the precursor and will vary depending on the growth temperature as the reaction rates change. Ferro *et al.* showed that they could optimise the growth of 3C-SiC using hexamethyldislane by adding a small flow of propane into the growth system, thus

optimising the C/Si ratio [64]. Another issue with many single source precursors is that they are often non-standard industrial gases which inhibits their use at a commercial level.

2.5.2 High Temperature Epitaxy

The growth of 3C-SiC is typically carried out at high temperatures close to the melting point of Si (~1410 °C) in order to achieve high growth rates and good crystal quality from standard Si and C growth precursors such as in the examples discussed above in section 2.5.1. However, there are also examples of 3C-SiC growth beyond the melting point of Si such as in heteroepitaxial growth on 6H-SiC substrates [65], 3C-SiC homoepitaxy [66] or for the challenging growth of bulk 3C-SiC crystals [67]. The downside to high temperature growth of 3C-SiC is that temperatures beyond ~1250 °C are beyond the range of traditional 'cold-wall' CVDs used in the silicon industry. Instead, SiC specific 'hot-wall' reactors must be used which dramatically increase operating costs. This is discussed further in section 3.1.

2.5.3 Low Temperature Epitaxy

Low temperature growth of 3C-SiC is interesting from a variety of commercial and practical standpoints. If the growth of high quality 3C-SiC can be brought below ~1200 °C then it will be possible to perform heteroepitaxy within 'cold-wall' CVD reactors. These types of reactors are commonly used by the silicon industry due to their high throughput and reduced maintenance costs, primarily due to the reduced depositions on the quartz chamber walls. As these reactors are the mainstream for the silicon industry, the growth system technology is significantly more mature than the 'hot-wall' SiC reactors and fully automated reactors capable of growing on wafers up to 300 mm in diameter can be commercially purchased from suppliers such as Advanced Semiconductor Materials International (ASM) or Applied Materials either in the form of single chamber reactors or cluster tools, see Figure 2.12.

Figure 2.12 Typical 300 mm growth systems from ASM. Left – the 3200 single chamber RP-CVD and right the 300 mm Intrepid XP cluster tool capable to growing in up to 4 chambers simultaneously [68].

Lower temperature growth would allow the incorporation of 3C-SiC into the well-established silicon industry and allow integration between wide bandgap (SiC) and narrow bandgap (Ge, $Ge_{1-x}Sn_x$) semiconductors within a single, low-cost, growth process.

Another key advantage of growing at reduced temperatures is the potential to significantly reduce the effect of wafer bow, primarily caused by the mismatch in thermal expansion coefficient between 3C-SiC and Si [53]. There are many sources which quote different values of thermal expansion for 3C-SiC and Si, therefore it is difficult to quantify how much of an impact growing at lower temperatures can reduce this thermal mismatch. However, it has been shown that growing at reduced temperatures can reduce the plastic deformation of 3C-SiC during growth due to a process known as the creep phenomenon, by which a solid deforms permanently due to mechanical stresses and is more prevalent at higher temperatures [69, 70].

2.6 Defects

2.6.1 Misfit dislocations

There is a mismatch of ~19.7% between the lattice constants of 3C-SiC and Si. When 3C-SiC is heteroepitaxially grown on Si, there is a large strain field between the two crystals which is relieved by the formation of defects at the interface. The dominant defects at the interface are misfit dislocations, the formation of which is shown schematically in Figure 2.13. A pair of 60° partial dislocations forms at approximately

every 5th 3C-SiC{111} lattice plane in order to fully relax the epilayer. When considering defects in a 2-dimensional slice of the 3C-SiC/Si heterostructures, two dislocations form at each point, one in the (111) direction and another in the $(\bar{1}\bar{1}1)$ direction. These two defects combine to form a pure edge misfit dislocation with a Burger's vector of $\frac{a}{2}[110]$ parallel to the interface between the 3C-SiC and the Si [71].

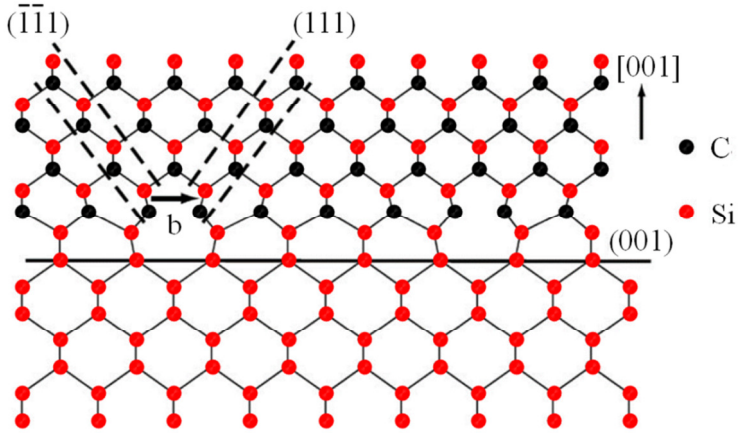

Figure 2.13 Schematic showing the formation of edge misfit dislocations at the interface between 3C-SiC and Si (001), adapted from [71].

2.6.2 Stacking Faults and Microtwins

Relaxing the lattice mismatch at the interface leads to the insertion of additional monolayers of Si-C in the 3C-SiC crystal. These defects are referred to as stacking faults as they disrupt the stacking sequence of the lattice. The exact formation of these defects is not well understood, but it is believed that stacking faults form when the two 60° partial dislocations formed at the interface do not join to form a perfect misfit dislocation and instead each form a pair of 30° and 90° partial dislocations resulting in stacking faults [72]. While pure 3C-SiC has the stacking sequence of ABCABC… the insertion of additional monolayers alters this sequence, introducing hexagonality and dangling bonds. Song *et al.* observed a higher electrical activity of these stacking faults equivalent to a N doping level of ~5×10^{18} cm^{-3} and suggested that this could be caused by the accumulation of background N at the stacking faults through drift diffusion [73]. Recently, Xi *et al.* investigated the effect of point defects near stacking faults in 3C-SiC and found that the stacking faults shorten the distance between tetrahedral site nearest neighbours and making the system unstable instead forming dangling bonds inducing defects in the bandgap as well as creating vacancies [74].

Stacking faults are considered 'device killers' for power electronic device applications in that they induce significant leakage current in vertical rectifying devices. Various studies have assessed the leakage current through stacking faults. Chung *et al.* [75] showed significant leakage current in vertical Schottky diodes while Eriksson *et. al.* [76] used conductive atomic force microscopy (AFM) to show the high conductivity of stacking faults on the surface of 3C-SiC.

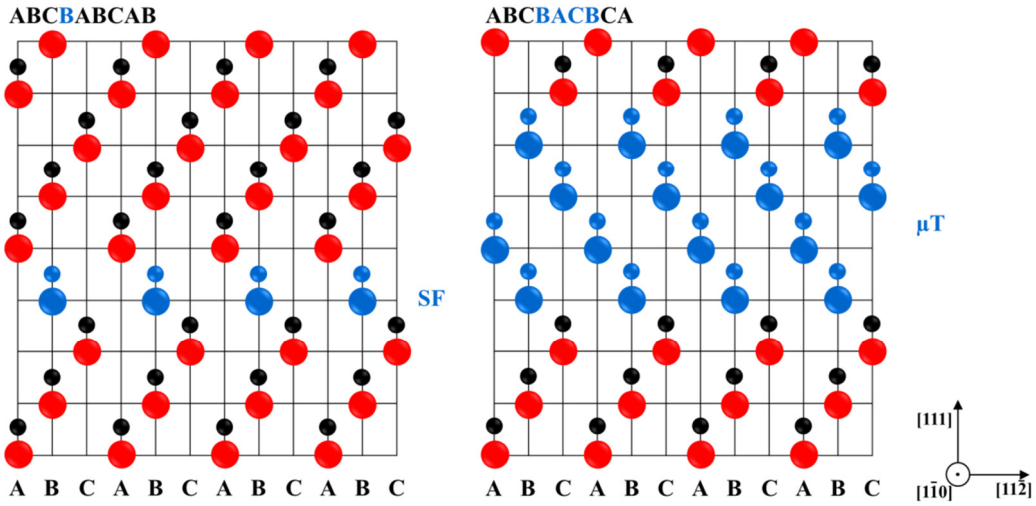

Figure 2.14 Cross sectional schematic through the 3C-SiC crystal structure showing the formation of a stacking fault (SF) and a microtwin (μT) and the resulting disruption to the stacking sequence [77].

Microtwins are similar to stacking faults as they are also planar defects that result from disruptions in the crystal structure, however, while stacking faults involve only one atomic bilayer, microtwins involve several atomic planes. The result is the formation of regions where the crystal stacking sequence is reversed which, like stacking faults, travel up the {111} planes [78]. Microtwins can also annihilate when they intercept each other in the same way that stacking faults do and as such the density of both planar defects decreases with increasing epilayer thickness, see section 2.7. Examples of stacking fault and microtwin formation are shown schematically in Figure 2.14.

2.6.3 Inversion Domain Boundaries

Other common defects in heteroepitaxially grown 3C-SiC include inversion domain boundaries (IDBs), commonly referred to anti-phase domains (APDs). An IDB in 3C-SiC is an interface between two domains of the crystal which differ from each other by the exchange of C and Si lattice site positions, see Figure 2.15. The (111) planes of Si

are non-polar and equivalent which is why IDBs are not found in diamond structured crystals such as Si and Ge. 3C-SiC and other compound semiconductors including GaAs lack inversion symmetry which results in the formation of different domains. The origin of the domains is due to the initial island nucleation of 3C-SiC on the Si lattice. On-axis substrates typically have mono-atomic steps which lead to the formation of these non-equivalent domains. When the islands spread to form an epilayer, the domains meet and form IDBs [79]. A simple way to avoid IDBs is to grow on a Si substrate with diatomic steps, which can be achieved using off-axis wafers, typically a few degrees offcut in the (110) direction [77]. More recently, researchers have shown that diatomic steps can be promoted in Si substrates through hydrogen based thermal annealing prior to epitaxial growth [80].

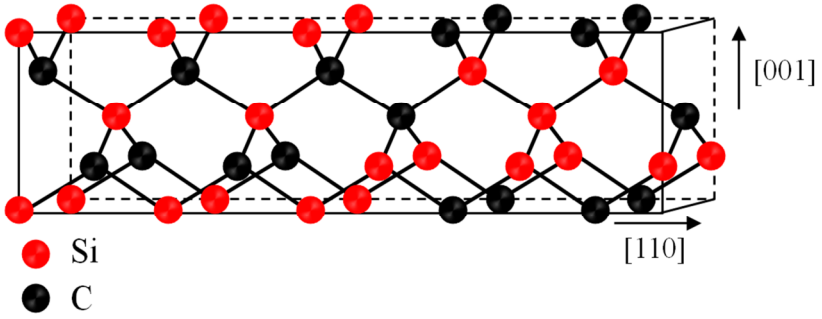

Figure 2.15 3C-SiC (110) inversion domain boundary formed by the positions of the Si and C atoms swapping on in different domains in the crystal. The result is highly stressed boundaries formed by C-C and Si-Si bonds, adapted from [79].

For much the same reasons as with the effects of stacking faults, IDBs are a source of leakage current in 3C-SiC based power devices due to the effects of Si-Si and C-C bonds on the bandgap, causing a similar effect to high level doping. It has been shown that when Si-Si bonds relax from significant strain the p-type like bonds can push states up into the conduction band leading to a semi metallic state at the IDB [79]. These defects have been shown to be more significant killers to device performance than stacking faults, causing power devices such as Schottky diodes to short, losing all forward and reverse bias characteristics [76].

2.6.4 Voids

Voids can often be observed in the Si substrate at the interface with 3C-SiC and are caused by the out-diffusion of Si atoms from the substrate during growth and are

typically shaped like inverted pyramids. The formation of voids at the interface is a significant problem for vertical device applications such as heterojunction bipolar transistors where a high quality interface is essential [81]. The formation of voids can be reduced by growing at lower temperatures [82], however, the easiest way to prevent void formation is by proper optimisation of a buffer layer between the 3C-SiC and Si. This is typically achieved through carbonisation at reduced temperatures, typically between 900-1300 °C [83].

2.6.5 Vacancies

Semiconductors can also suffer from point defects which includes vacancies. A vacancy is an unoccupied site within the crystal lattice and in SiC this can occur either on a Si or a C site creating Si or C vacancies. Vacancies tend to create deep levels in the band gap which can trap carriers in the semiconductor, causing negative impacts on electrical performance. Vacancies can be intentionally introduced into 3C-SiC through irradiation with electrons or protons for specific applications, however, they are usually an unwanted result of ion implantation, which can lead to non-stoichiometric atom distribution in compound semiconductors [84]. While vacancies are typically viewed as a detrimental defect in semiconductors, they have been shown to provide unique electrical properties in SiC which have potential applications in single photon LEDs and even as qubits for quantum computing [85, 86]. They are not, however, a focus for the research presented here and therefore will not be discussed further, for more information on the origin and effects of vacancies the author recommends *Silicon Carbide Volume 1: Growth, Defects and Novel Applications* by P. Friedrichs *et al.* [87].

2.6.6 Polytype Inclusions

Another type of defect in SiC is the inclusion of other polytypes during growth. As all polytypes of SiC are identical when viewed from the perspective of the hexagonal bilayers, (111) for cubic or c-plane (0001) for hexagonal polytypes, see Figure 2.9, it is possible for other polytypes to grow during epitaxy. This is mainly an issue with the homoepitaxy of 4H-SiC or 6H-SiC which can be plagued with 3C-SiC polytype inclusions, affecting the electrical performance and lifetime of devices by trapping electrons [87]. Inclusions can be suppressed by growing on off-axis substrates as the additional steps in the substrate helps promote the growth of the underlying polytype. Today, all commercial 4H-SiC and 6H-SiC epilayers are homoepitaxially grown on off-

axis substrates (typically 4°) to avoid this problem in a process known as step-flow epitaxy [21]. At the typical growth temperatures of 3C-SiC (<1400 °C) it is very rare for other polytypes to stabilise. As such, with the exclusion of stacking faults which have 2H-SiC characteristics, heteroepitaxially grown 3C-SiC does not typically suffer from polytype inclusions and therefore can be grown on on-axis substrates.

2.7 Reducing Defects

Stacking faults exist in the four equivalent {111} planes within a 3C-SiC structure. Taking a 2D slice of the crystal viewed through the (110) plane leads to two stacking fault planes $(1\bar{1}1)$ and $(\bar{1}11)$ the dissociations of which are defined by their Burger's vectors as

$$\frac{a}{2}[101] \rightarrow \frac{a}{6}[211] + \frac{a}{6}[1\bar{1}2]$$
$$\frac{a}{2}[0\bar{1}\bar{1}] \rightarrow \frac{a}{6}[\bar{1}\bar{2}\bar{1}] + \frac{a}{6}[1\bar{1}\bar{2}]$$

respectively, where the two terms on the right hand side of the expressions are the Burger's vectors for a 30° and 90° partial dislocation. When stacking faults meet in the crystal one or both of the defects tends to annihilate, this can be explained by the reaction between the two 30° partial dislocations given by

$$\frac{a}{6}[211] + \frac{a}{6}[\bar{1}\bar{2}\bar{1}] \rightarrow \frac{a}{6}[1\bar{1}0]$$

which results in a Lomer-Cottrell dislocation [72]. As such, the stacking fault density in 3C-SiC decreases with increasing thickness as more defects are able to annihilate.

There are also methods to reduce stacking fault densities further such as growing on undulant Si which causes stacking faults to form on symmetric {111} planes, allowing the defects to annihilate more effectively. Other, more complicated processes include switch-back epitaxy, in which standard 3C-SiC heteroepitaxy is performed on undulant Si before the Si substrate is removed, the 3C-SiC epilayer thinned from the interface side then homoepitaxy of 3C-SiC is carried out. This method, although complex, forces stacking faults to propagate back in on themselves such that they annihilate [77].

Selective Epitaxy

A common method of reducing planar and interfacial defects in heteroepitaxially grown semiconductors is selective epitaxy on a patterned substrate. Selective epitaxy is the process by which deposition only occurs on the exposed crystalline substrate and not on the mask that has been used to pattern the wafer. The masking layer is typically formed of silicon dioxide (SiO_2) but in some cases other materials such as silicon nitride (Si_3N_4) have been used. SiO_2 is the mask of choice for most applications as it can easily be removed from the substrate post growth through wet or dry etching. Another process associated with selective epitaxy is epitaxial lateral overgrowth (ELO) in which the crystal growth continues such that the epilayer grows laterally over the masking layer. Both techniques are often used in industry for the selective growth of Ge and $Si_{1-x}Ge_x$ alloys but has also been demonstrated on other mismatched systems including GaAs on Si [88], GaN on Si [89] and GaN on 4H-SiC [90]. Selective epitaxy and ELO are both used to reduce the number of defects in heteroepitaxially grown epilayers as growing on small areas can reduce the interface stress and dislocations and other defects can terminate at the mask layer, see Figure 2.16.

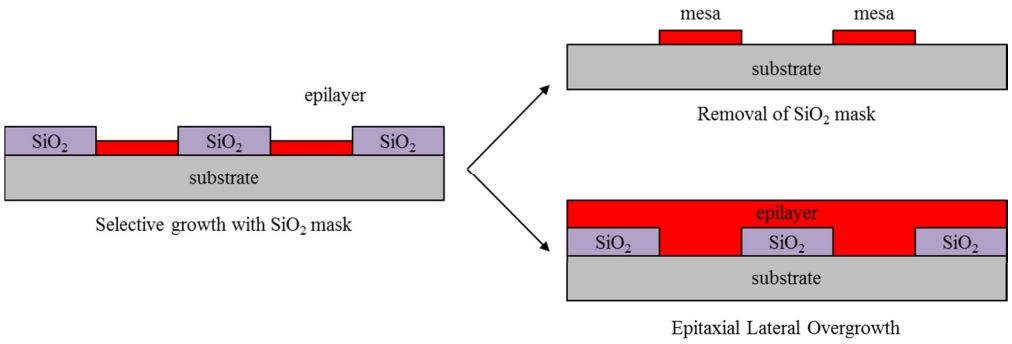

Figure 2.16 Schematic diagrams of selective growth followed by either mask removal or ELO.

Selective growth techniques offer various advantages with 3C-SiC growth such as reducing the tensile stresses in the epi wafer, reducing interfacial and planar defects by growth confinement or ELO and can be used to grow mesas, removing the need for etching of the 3C-SiC after growth [91]. While the melting temperature of SiO_2 and Si_3N_4 are higher than the melting point of Si, pattern distortion occurs at much lower temperatures of ~1000 °C and can be etched in the H_2 carrier gas [92]. This is why these materials are not routinely used for the selective epitaxy of 6H-SiC, 4H-SiC and 3C-SiC polytypes.

2.8 Doping

Doping was briefly described earlier in section 2.1 for semiconductors in general. 3C-SiC offers a few additional challenges when introducing impurities. As a group IV semiconductor, donors and acceptors are still group V and III elements respectively as with Si and Ge, however, N can also act as an n-type dopant as it can sit substitutionally on C lattice sites. This presents a problem for growing undoped 3C-SiC (and SiC is general) as N_2 gas is almost always present in a growth system as a background impurity and can lead to background doping as high as 10^{17} cm^{-3} [93]. While N is often used as an n-type dopant it is interesting to note that P is a more efficient donor as it can occupy both the C and Si sites leading to fewer interstitials [94].

There are two main methods for introducing impurities in 3C-SiC epilayers, ion implantation and in-situ doping during epitaxy. Ion implantation is achieved by accelerating ions towards the surface of a semiconductor at high energies which embeds the ions within the epilayer to a particular depth. Ion implantation typically damages the crystal structure of a semiconductor. To recover the crystal structure and allow the impurities to take up substitutional sites within the lattice the semiconductor is treated post implantation, this is normally achieved through thermal annealing. One issue with ion implantation of 3C-SiC is that the energies required to embed the ions within the crystal are significantly higher than those required for Si or Ge implantation. Another concern is that 3C-SiC is a very stable crystal and difficult to recover. Thermal annealing of 3C-SiC is limited to the melting point of the Si substrate (~1414 °C) and hence it can be very difficult to electrically activate implanted impurities in 3C-SiC. Ion implantation of 3C-SiC can be achieved with both n-type dopants (N, P) and p-type dopants (B, Al). For n-type, the electrical activation is typically in the region of 10% [95, 96], while for p-type dopants the activation can be as low as 1% [97]. The advantage of ion implantation is that dopants can be implanted into the epilayer selectively, using a masking layer such as photoresist, which can be used for doping device channels or contacts.

In-situ doping is achieved by flowing a relatively small amount of impurity containing precursor during the epitaxy of 3C-SiC which then incorporates in the lattice during growth. In-situ doping of 3C-SiC is not an area that has been well documented in literature with only a handful of authors who have directly measured the incorporated impurities as well as the electrical activity. While both N and Al in-situ doping in 3C-

SiC has been published the electrical activity is still low [98]. The advantage of in-situ doping is that if done correctly, electrical activation is not required as dopants can be incorporated substitutionally during growth. Also, unlike ion implantation, in-situ doping can produce either uniform or graded doping profiles in any thickness epilayer and can be applied to grow buried doped layers.

The maximum achievable impurity levels through ion implantation N or P within 3C-SiC are around 6×10^{20} cm^{-3}, however, electrical activation at this level of implantation can be around 12%, saturating the free donors at $\sim 7 \times 10^{19}$ cm^{-3} [95] and leaving a high number of interstitial impurities in the crystal. Doping levels achieved through in situ doping during epitaxy of 3C-SiC can be poor with activation levels as low as 0.1% being reported for in situ doping of Al at electrically active levels of 2×10^{17} cm^{-3} [98].

2.9 Applications of 3C-SiC

2.9.1 Power Electronics

One of the most promising applications for SiC is in power devices [99]. Demand for high frequency, power density and blocking voltage rectifying devices has pushed the traditional material of choice, Si, to its limits. SiC has a critical electric field breakdown that is approximately 10 times higher than that of Si which results in lower on-resistance for equivalent devices fabricated from SiC than Si, see Figure 2.17. SiC also has a higher thermal conductivity than Si, allowing it to operate with higher power densities and frequencies as heat can be dissipated from devices more effectively. In addition to this, SiC has very little to no reverse recovery when switching from forward to reverse bias, a property which Si lacks. This leads to reduced losses and increased switching speeds [41]. Another potential candidate for higher performance power devices is GaN, a wide bandgap III-V compound semiconductor. While GaN can theoretically operate more effectively at higher voltages, it struggles with blocking voltages above 1-2 kV due to poor crystal quality and lower thermal conductivity [41].

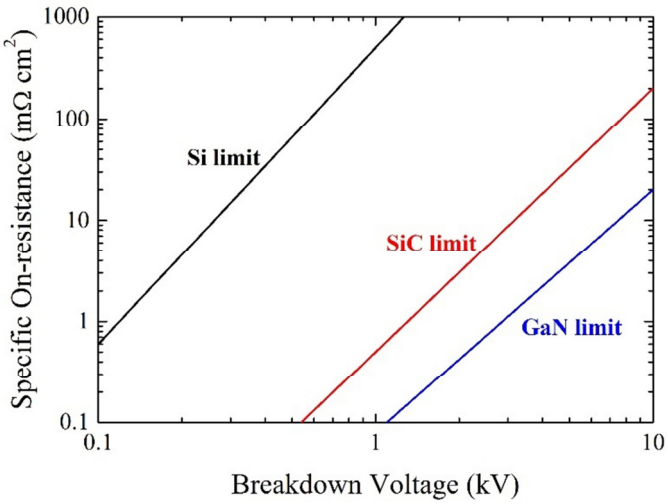

Figure 2.17 The typical limits of power devices fabricated from Si, SiC (4H-SiC) and GaN, although there are several examples of insulated gate bipolar transistors (IGBTs) that have exceeded these limits. Adapted from [100].

While SiC power devices are more traditionally made from hexagonal polytypes including 4H and 6H-SiC, 3C-SiC offers several advantages including: larger potential wafer sizes, higher hole mobility, cubic isotropy and the fact that defects in 3C-SiC are immobile and therefore device operation is unaffected during use, although defects can have a significant impact on device performance. In addition, the reduced bandgap of 3C-SiC reduces the electric field required for channel inversion in MOSFETs and reduces the number of traps at the SiO_2/3C-SiC interface [101, 102]. The issue that has limited the use of 3C-SiC in power electronic applications is the high density of leakage inducing defects in the heteroepitaxially grown layers.

2.9.2 MEMS

The high mechanical strength, thermal conductivity and wide bandgap of SiC makes it ideal for applications in demanding applications, see Table 2.2, 3C-SiC in particular offers a unique advantage in chemical etch selectivity which allows various structures to be formed that are suitable for a range of microelectromechanical system (MEMS) applications, see section 3.3.6. While almost all MEMS devices are based on Si, applications in corrosive environments or at elevated temperatures above 300 °C are of interest to various sectors including automotive, aerospace and industrial [47]. MEMS are devices that convert a mechanical response to a real world parameter (pressure, temperature, gas flow etc.) to an electrical response in a device, hence their operation is

far less dependent on crystalline defects or leakage current, which makes them a more suitable application for 3C-SiC/Si heterostructures [53]. Various work on 3C-SiC based pressure, temperature and gas flow sensors, to name but a few, are areas of active research with device operation temperatures exceeding 500 °C [103-105].

2.9.3 Virtual Substrates

Another major application for 3C-SiC is as a virtual substrate for the heteroepitaxy of GaN for LED, RF and power electronics applications, see Figure 2.18.

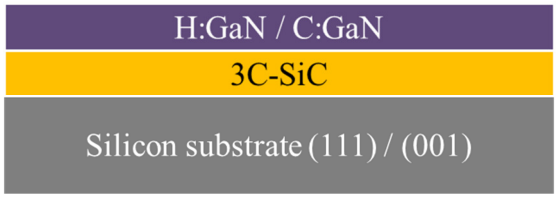

Figure 2.18 Cross sectional schematic of hexagonal (H) and cubic (C) GaN grown on a 3C-SiC virtual substrate.

3C-SiC offers a unique advantage for GaN epitaxy as the lattice mismatch between the two materials is low (~3.5%) and offers high thermal conductivity, see Table 2.2, while still allowing the growth of GaN on a Si substrate. Even relatively thin 3C-SiC buffer layers of ~700 nm have been shown to improve GaN LED performance by more than doubling the output intensity compared to growth on pure Si [6]. In addition, 3C-SiC offers the unique advantage that it can be grown on both the (111) and (001) crystal orientations, providing ideal templates for the growth of hexagonal and cubic GaN respectively. Cubic GaN is of particular interest as it can increase efficiency of green LEDs overcoming the "droop effect" typically observed at green wavelengths in GaN based ternary compounds [106].

2.10 Silicon Carbon

Another semiconductor based on Si and C is silicon carbon ($Si_{1-y}C_y$) which, unlike 3C-SiC, is an alloy formed by the substitutional incorporation of C into the Si lattice that enables the manipulation of electrical, chemical and physical properties from that of pure Si, see Figure 2.19. $Si_{1-y}C_y$ has a diamond cubic lattice structure with a high density of substitutional C atoms in Si lattice sites (typically ~1% or greater).

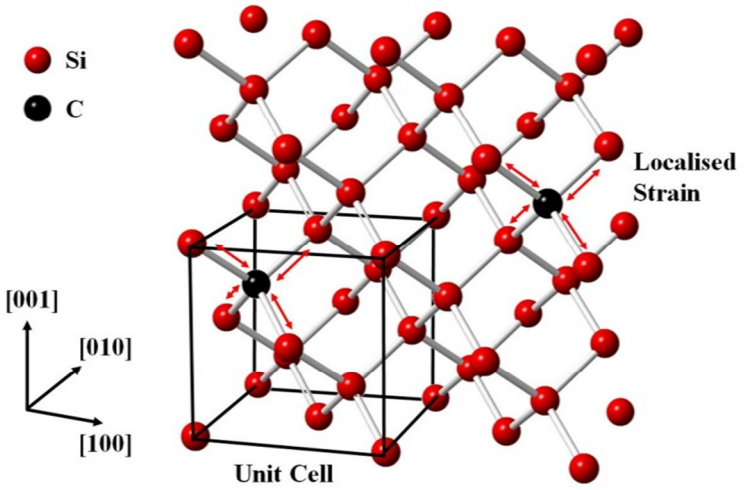

Figure 2.19 Representation of the crystal structure of $Si_{1-y}C_y$ alloy showing the cubic unit cell.

Many properties of $Si_{1-y}C_y$ epilayers vary as a transition between the properties of Si and 3C-SiC such as the reduction of the lattice constant and increase in bulk modulus [107]. However, while $Si_{1-y}C_y$ has the same lattice structure as 3C-SiC the huge chemistry difference between Si and C has been shown to result in an initial drop in the bandgap under various simulation conditions and experimental results, due to the localized strain caused by C atoms [108], see Figure 2.20.

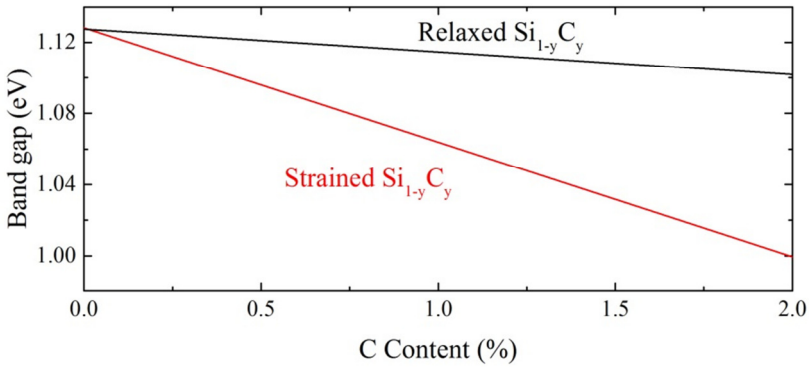

Figure 2.20 Dependence of C content in $Si_{1-y}C_y$ alloys on the bandgap of the epilayer, adapted from [108].

The origin of the reduced bandgap is the lowering of the conduction band by the introduction of strain the epilayer. This drop occurs up to a certain threshold of C composition (approximately 10%) after which the bandgap is expected to rise up to the value of 3C-SiC, although there is currently no experimental data to support these simulation results at C contents this high.

Due to the huge lattice mismatch between diamond and Si, the incorporation of C in the Si lattice reduces the lattice constant quite significantly. The resultant strain induced in $Si_{1-y}C_y$/Si heterostructures is around 10 times greater than the strain induced in $Si_{1-x}Ge_x$/Si heterostructures of equivalent substitutional composition. As a result, the main applications of $Si_{1-y}C_y$ alloys are found in strain engineering, such as inducing strain within MOSFET channels to increase mobility [109] or compensating for the strain induced by Ge in $Si_{1-x-y}Ge_xC_y$ ternary alloys, such that the band structure can be modified whilst still matching the lattice structure of Si [110]. The incorporation of C in the Si lattice has also been shown to reduce "transient enhanced diffusion" [111]. This property has been utilized in various silicide applications such as increasing the maximum anneal temperature of platinum (Pt) and nickel (Ni) silicides [112, 113] as well as reducing the Schottky barrier height with the aim to significantly reduce contact resistance [114]. Silicon carbon alloys have been implemented in strained MOSFET channels for over 10 years now with IBM being one of the first companies to develop and commercialise the technology [115] while more recently they have been combined with Si:P alloys to further enhance source-drain technology [116].

Chapter 3
Experimental Techniques

The following Chapter describes the Physics and technology behind the growth of semiconductor materials and a number of key characterisation techniques utilised within this research.

3.1 Epitaxial Growth

The reduced pressure chemical vapour deposition reactor (RP-CVD) is a common type of CVD which operates at pressures from sub atmospheric (760 Torr) down to ~10 Torr and can run at growth temperatures ranging from around 100 °C all the way up to beyond 2000 °C. One of the leading suppliers of epitaxial reactors into the semiconductor industry is ASM, who have supplied the silicon industry with Epsilon reactors for over 30 years. The ASM Epsilon 2000 is a single wafer RP-CVD capable of growth on circular substrates ranging from 100 mm to 200 mm in diameter. The Epsilon 2000 comprises a quartz chamber in which the substrate sits upon a SiC coated graphite susceptor heated with infrared (IR) lamps. The gas flow is injected from one end of the chamber through 5 injectors and extracted at the opposite side of the chamber after which the toxic elements are removed through abatement systems before being ejected back into the atmosphere. The system is referred to as a 'cold-wall' reactor as the quartz chamber is not intentionally heated by the IR lamps, which limits depositions on the chamber walls. Under high temperature growth conditions, the chamber walls can be heated through convection of the heated gases within the chamber and must be maintained at a low enough temperature, achieved using blowers which direct chilled ambient air onto the outside of the chamber, keeping it cooler.

The ASM Epsilon 2000 RP-CVD system was the predominant growth system used within this research and is the tool responsible for the growth of all $Si_{1-y}C_y$ and $Si_{1-x}B_x$ alloys as well as low temperature grown 3C-SiC. The system is fully automated and can

hold up to 26 wafers in either load lock, which are then sequentially transferred into and out of the growth chamber with a Bernoulli wand which ensures the surface of the wafers remain clean during transfer, see Figure 3.1. The system can be programmed to grow an identical recipe on 26 wafers or have individual recipes assigned to each substrate.

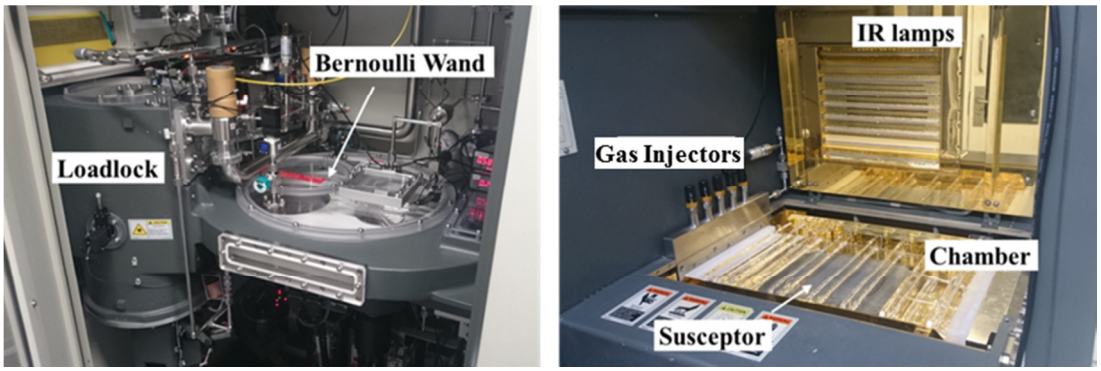

Figure 3.1 Photographs of the wafer handling section (left) and growth chamber section (right) of the ASM Epsilon 2000 RP-CVD.

Another growth system which was used for a short study within this research is the LPE ACIS M8 RP-CVD which is capable of growing at temperature beyond 1800 °C. It achieves this by using a SiC coated graphite chamber which can withstand such temperatures. The chamber and susceptor are heated simultaneously with RF coils and as such this CVD is referred to as a 'hot-wall' CVD. The advantage of such a system is that is can reach the high temperature required for hexagonal SiC polytype growth (1600-1750 °C), however, a hot chamber leads to significant depositions (equivalent to epitaxial growth) which dramatically increases maintenance, down time and overall running costs. The technology of the LPE 'hot-wall' CVD pales in comparison to the ASM Epsilon system as there is no wafer handling section. Instead, users must manually load wafers into the chamber, which is directly exposed to the cleanroom. This results in the residual toxic and corrosive gases from the CVD chamber being ejected into the cleanroom which raises safety concerns, see Figure 3.2.

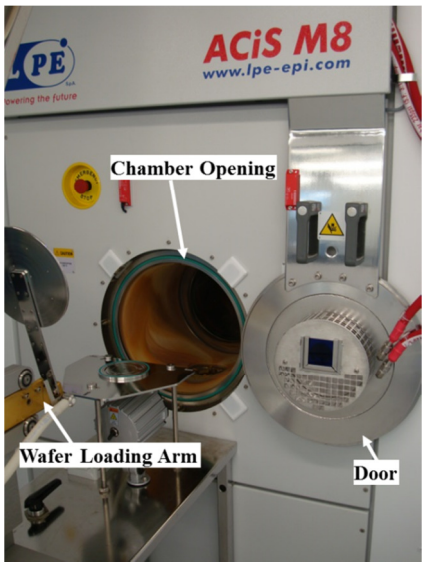

Figure 3.2 Photograph showing the front of the LPE ACIS M8 RP-CVD with the wafer loading arm and chamber opening.

Epitaxy is highly sensitive to surface contamination on the starting substrate surface, therefore all Si wafers are subjected to a pre-clean process known as an RCA clean. The process, developed by Werner Kern while working for the Radio Corporation of America (RCA), involves several stages. First, the wafer is cleaned in a mixture of H_2O:ammonium hydroxide (NH_4OH): hydrogen peroxide (H_2O_2) in a ratio of 5:1:1 at ~80 °C for ~10 mins to remove any organic contaminants, this is known as RCA1. This step is then followed by a short dip in a weak (~2.5%) aqueous HF solution to strip any oxide. Secondly, any ions are removed from the surface of the wafer using a mixture of H_2O:hydrogen chloride (HCl):H_2O_2 in a ratio of 6:1:1 at ~80 °C for ~10 mins, this is known as RCA2. This process leaves a thin protective oxide layer on the Si wafer which prevents any subsequent contamination. When loaded into the CVD, the wafers are immediately baked under H_2 flow at a temperature of 1100 °C or above to strip the oxide and leave a H passivated surface ready for epitaxy [117].

3.2 Material Characterisation Techniques

3.2.1 Fourier Transform Infrared Spectroscopy (FTIR)

FTIR is a non-destructive technique that can operate in one of two modes: transmittance or reflectance. Transmittance mode measures the absorption of light through a sample and for semiconductor samples this can offer information on the material bandgap and

certain defects and impurities in the crystal, such as O and C [118]. Reflectance mode uses the interference of light to determine the thickness of thin films. Both modes operate using the same principle, the basis of which is the Michelson interferometer. The Michelson interferometer operates by splitting a beam of 'white light', emitted from a source, through an appropriate beamsplitter. Each of the split beams is reflected off a mirror, one of which is at a fixed distance from the beamsplitter, while the other moves towards and away from the beamsplitter which alters the path length of one of the split beams. Both of these beams are then redirected towards the sample and detector by the beamsplitter upon their return. The interference of the two beams results in a unique spectrum of light which is dependent on the position of the moving mirror.
The combined beam is then focused through a sample. When operating in transmittance mode the path of light carries on through the sample and a detector records the intensity of light that is passed through the material. When operating in reflectance mode, the light that is reflected off the surface and any subsequent interfaces in the sample is recorded, see Figure 3.3.

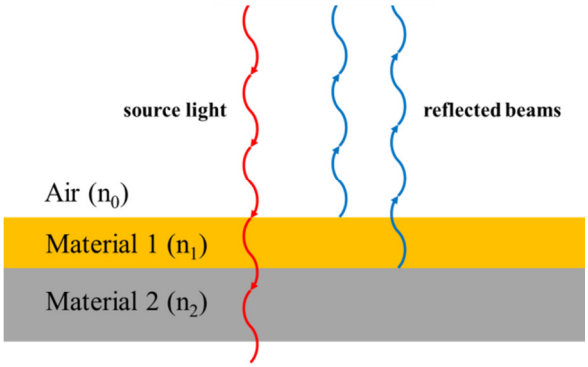

Figure 3.3 Representation of how light from the FTIR reflects off interfaces in thin film samples. Reflection occurs when $n_0 \neq n_1 \neq n_2$ and the thickness of the thin film of material 1 will affect the interference of the two reflected beams. The beams are separated laterally for clarity.

Constructive interference occurs when

$$m\lambda = 2dn_1 \qquad \text{Equation 3.1}$$

is satisfied, assuming the refractive index of air is 1, where m is an integer, λ is wavelength and d the layer thickness. A wavelength dependent spectrum from the FTIR is produced by acquiring a series of intensity measurements at different outputted light beams from the Michelson Interferometer. A Fourier transform is required to convert the raw data into the desired spectrum. The advantage of obtaining data through this

method is that a large intensity of light can be measured over a range of wavelengths which significantly increases the signal to noise ratio compared to other methods of spectroscopy which operate over narrow ranges of light. A Bruker Vertex 70v was used for FTIR measurements throughout this research.

3.2.2 X-ray Diffraction

X-ray diffraction (XRD) is a powerful characterisation technique for crystalline semiconductor materials, offering information on many important factors including crystal structure, quality, composition, tilt and strain state. The principle behind XRD is based on Bragg's Law

$$n\lambda = 2d\sin(\theta) \qquad \text{Equation 3.2}$$

where n is an integer value, λ to the incident X-ray wavelength, d the distance between crystal planes and θ the incident angle of the beam with respect to the crystal plane surface, see Figure 3.4.

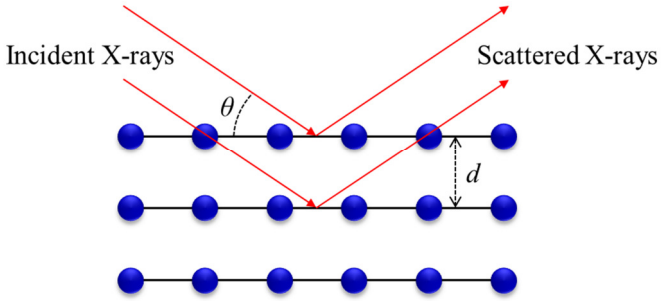

Figure 3.4 Schematic of X-rays elastically scattering off a crystal plane, leading to the derivation of Bragg's Law.

XRD can occur on a variety of crystal planes, depending on whether these diffraction conditions are 'allowed' or 'forbidden', this phenomenon is defined by the structure factor of the particular crystal and the Miller indices of the crystal planes. The structure factor F_{hkl} defines how strongly the incident X-rays interact with the crystal planes. Si and 3C-SiC defined by two FCC crystals of basis (0,0,0) and (1/4,1/4,1/4), which leads to the following expressions for Si and SiC:

$$F_{hkl}^{Si} = (F_{FCC}^{Si} + F_{FCC}^{Si} e^{\frac{i\pi}{2}(h+k+l)}) \qquad F_{hkl}^{3C-SiC} = (F_{FCC}^{Si} + F_{FCC}^{C} e^{\frac{i\pi}{2}(h+k+l)}) \qquad \text{Equations 3.3}$$

where F_{FCC}^{Si} and F_{FCC}^{C} are the structure factors of Si and C atoms in an FCC structure which each expand to

$$F_{FCC} = f[1 + (-1)^{h+k} + (-1)^{h+k} + (-1)^{h+k}]$$ Equation 3.4

where f is the atomic form factor of either Si or C atoms. When expanded out, Equations 3.3 give the selection rules shown in Table 3.1.

Table 3.1 XRD selection rules for Si and 3C-SiC.

Miller Indices Conditions	**Example Reflections**	$\|F_{Si}\|^2$	$\|F_{3C\text{-}SiC}\|^2$
h,k,l mixed parity	(123), (158), (225)	0	0
h,k,l all odd	(111), (133), (135)	$32f_{Si}^2$	$16[f_{Si}^2 + f_C^2]$
h,k,l all even and (h+k+l = 4n)	(004), (008), (022)	$64f_{Si}^2$	$32[f_{Si} + f_C]^2$
h,k,l all even and (h+k+l = 2n) but (h+k+l ≠ 4n)	(002), (006), (222)	0	$32[f_{Si} - f_C]^2$

All lab-based XRD measurements were carried out in a high-resolution X-ray Diffraction (HR-XRD) Panalytical X'Pert Pro MRD diffractometer using Cu $K\alpha_1$ radiation with a wavelength of 1.5406 Å. This tool can be fitted with two detectors making it capable of operating in both receiving slit (double axis) and triple axis modes. A schematic of the system is shown in Figure 3.5.

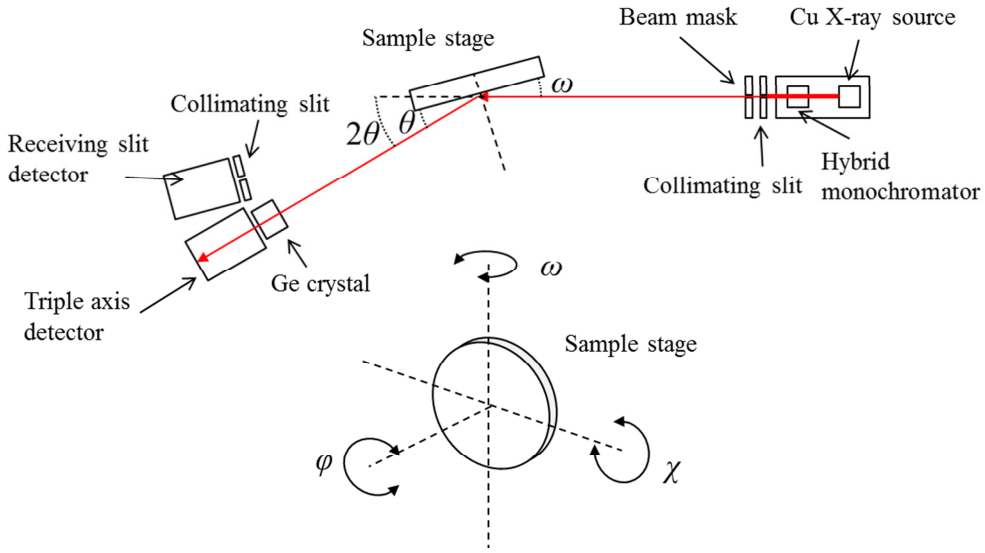

Figure 3.5 Schematic of the lab based HR-XRD set up defining all angles the system is capable of moving within.

Two mains types of measurements were made with the HR-XRD system: ω-2θ coupled scans and reciprocal space maps (RSMs).

ω-2θ coupled scans

In this set up, a particular line within reciprocal space is scanned along by manipulating both ω and θ such that Bragg's Law is satisfied at all times i.e. the diffraction vector is kept constant at a normal to the crystal plane being analysed. Coupled scans are used to assess the composition of crystalline materials, determine whether a crystal is monocrystalline, polycrystalline or amorphous and give an indication of quality and strain state. Within these investigations, coupled scans were exclusively carried out for the (004) planes in which Bragg diffraction was achieved by setting $\omega = \theta$.

Reciprocal Space Maps

It is possible to map out an area of reciprocal space which can give further information on the positions of Bragg peaks and, in particular, can be used to analyse crystalline tilt and strain. For a (001) surface orientated sample such as 3C-SiC/Si (001), reciprocal space is mapped out as in Figure 3.6.

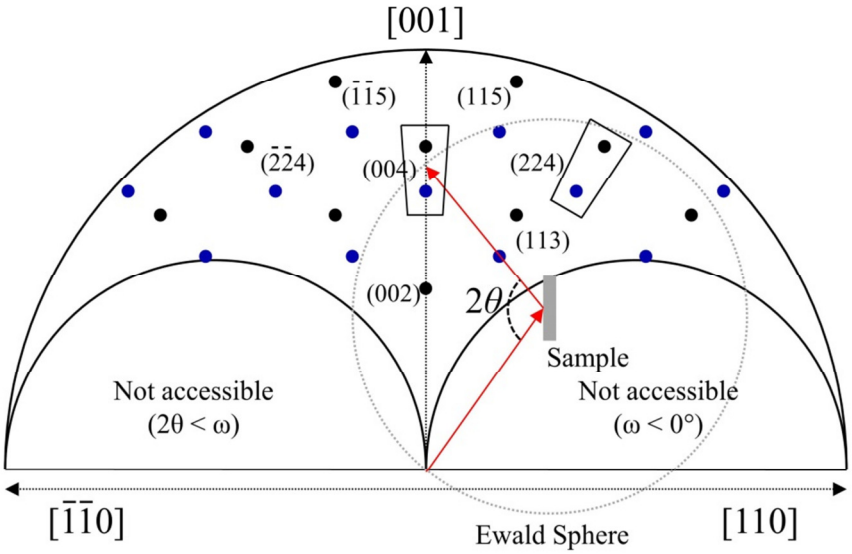

Figure 3.6 Two dimensional cross section of reciprocal space for a 3C-SiC/Si (001) sample. The blue dots indicate the approximate positions of Si Bragg peaks and the black dots represent the 3C-SiC Bragg peaks.

In the case of the lab-based HR-XRD system an RSM is formed by the acquisition of multiple coupled scans each applying a slightly different offset to ω-2θ. This allows

small areas such as the two shown in Figure 3.6 to be mapped out which allows one to calculate the position of particular Bragg peaks in both the in-plane <110> and out-of-plane <001> directions. The in-plane ($q_{||}$) and out-of-plane ($q_{\perp}$) reciprocal lattice vectors are given by

$$q_{||} = \frac{2}{\lambda}\sin(\theta)\sin(\omega - \theta) \quad \text{Equation 3.5}$$

$$q_{\perp} = \frac{2}{\lambda}\sin(\theta)\cos(\omega - \theta) \quad \text{Equation 3.6}$$

and the in-plane and out-of-plane lattice parameters, $a_{||}$ and $a_{\perp}$ respectively, are calculated using

$$a_{||} = \frac{\sqrt{h^2+k^2}}{q_{||}} \quad \text{Equation 3.7}$$

$$a_{\perp} = \frac{\sqrt{l^2}}{q_{\perp}} \text{ [119].} \quad \text{Equation 3.8}$$

In order to properly convert from the reciprocal lattice to lattice parameters, tilt must first be corrected for. Crystalline tilt occurs when an epilayer is grown at a slight tilt to the underlying substrate and is typically observed between highly mismatched materials and linked to the strain relaxation process [120]. The presence of tilt will rotate all Bragg peaks from an epilayer by an angle in reciprocal space which can lead to erroneous values of lattice parameters. Tilt can be corrected by observing a Bragg peak with a component solely normal to the orientation of the crystal i.e. the (004) RSM in a (001) crystal. As the (004) Bragg peaks have no component in the <110> directions, any shift in this axis must be attributed to tilt and is defined as

$$tilt = \text{atan}\left(\frac{q_{||}}{q_{\perp}}\right)_{004} \quad \text{Equation 3.9.}$$

After the tilt has been corrected in the epilayer Bragg peaks, an accurate measurement of the in-plane and out-of-plane lattice parameters can be made. Using these values the strain of a thin film can be determined. Strain is defined as the variation of a crystals structure from its relaxed structure and is defined in-plane ($\varepsilon_{||}$) and out-of-plane ($\varepsilon_{\perp}$) by

$$\varepsilon_{||} = \left(\frac{a_{||} - a_0}{a_{sub}}\right) * 100 \quad \text{Equation 3.10}$$

$$\varepsilon_{\perp} = \left(\frac{a_{\perp} - a_0}{a_{sub}}\right) * 100 \quad \text{Equation 3.11}$$

where a_0 is the relaxed lattice constant of the epilayer and a_{sub} the lattice constant of the substrate and is expressed as a percentage.

3.2.3 Micro X-ray Diffraction

Micro X-ray diffraction can be carried out at synchrotron facilities with sufficiently powerful X-ray sources, allowing the beam to be focused down to a few microns across while still maintaining high intensity. This method allows one to measure crystallinity and tilt as a function of position across different samples. In the present research, micro XRD experiments were carried out on suspended structures (see Section 3.3.6) and were performed on beamline B16 at the Diamond Light Source synchrotron using X-rays with an energy of 14.6 keV (λ = 0.849 Å). A compound refractive lens was used to focus the X-ray beam with a spot size of approximately 4 μm [121]. Samples were mounted on a piezo stage (50 nm precision) on top of an XYZ stage (0.5 μm precision) in a five circle diffractometer allowing the sample to be moved through the beam, see Figure 3.7.

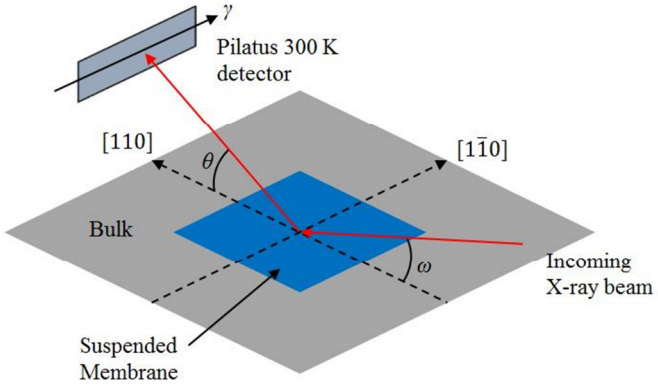

Figure 3.7 XRD scattering geometry for the acquisition of (004) RSMs.

Scattered X-rays were collected by a large PILATUS 300 K area detector capable of mapping the position of Bragg peaks in both 2θ (the scattering angle) and γ (the angle between the detector arm and the vertical plane). The 2D slice acquired by the PILATUS detector for a given angle of incidence (ω) does not lie in the [001]-[110] plane in reciprocal space. Each column and row of pixels corresponds to a different 2θ and γ given by

$$2\theta = \text{atan}\left(\frac{w(p_m - p_i)}{L}\right) + 2\theta_m \qquad \gamma = \text{atan}\left(\frac{w(p_m - p_i)}{L}\right) + \gamma_m \qquad \text{Equation 3.12}$$

where p_m is the middle pixel, p_i the index of the pixel in either the row or column, w = 172 μm and is the width of a single pixel, L is the distance from the sample to the detector (1.5 m) and $2\theta_m$ and γ_m are the angles the detector is centered on. RSMs were obtained across samples as a function of position by rocking ω around the (004) and (115) reflections at various spatial points. Each variable was individually fit to using 1D Gaussians by projecting the data against the other two variables.

The addition of the 2D detector allows the full three dimensions of reciprocal space to be mapped, this can be seen in Figure 3.8.

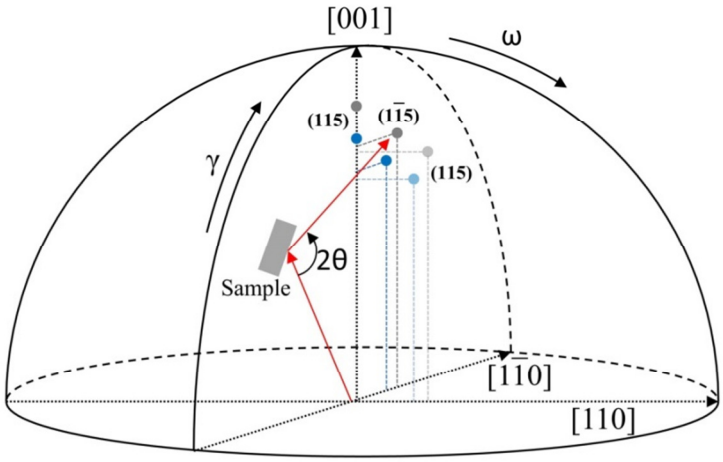

Figure 3.8 Three dimensional reciprocal space showing the (004) symmetric Bragg peak and two of the {115} asymmetric Bragg peaks.

Whereas with lab-based XRD (section 3.2.2) only the in-plane [110] and out-of-plane [001] coordinates are considered, in this case it is possible to define all three axes q_x [110], q_y [1$\bar{1}$0], and q_z [001] with

$$q_x = \frac{\lambda}{2}\sin(\theta)\sin(\omega - \theta) \qquad \text{Equation 3.13}$$

$$q_y = \frac{\lambda}{2}\sin(\theta)\sin(\gamma) \qquad \text{Equation 3.14}$$

$$q_z \cong \frac{\lambda}{2}\sin(\theta)\cos(\omega - \theta) \cong \frac{\lambda}{2}\sin(\theta)\cos(\gamma) \qquad \text{Equation 3.15}$$

for the symmetric (004) RSM where, as before, the calculation for q_z only takes into account movement of the Bragg peak in one of the axes [110] or [1$\bar{1}$0] .

The in-plane and out-of-plane lattice parameters of the crystal layers were calculated by taking RSMs around the (1$\bar{1}$5) Bragg peak which was located by setting γ to 15.79°

(the angle between the (004) and $(1\bar{1}5)$ planes) from the normal. In this case the in-plane and out-of-plane lattice parameters are defined by

$$q_{||} = \frac{\lambda}{2}\sin(\theta)\sin(\gamma - tilt) \quad \text{Equation 3.16}$$

$$q_{\perp} = \frac{\lambda}{2}\sin(\theta)\cos(\gamma - tilt) \quad \text{Equation 3.17}$$

where the *tilt* is defined as

$$tilt = \text{atan}\left(\frac{q_y}{q_z}\right)_{(004)}. \quad \text{Equation 3.18}$$

This is only the case for these XRD measurements as in order to get into the condition for Bragg diffraction the sample was rotated in γ rather than in ω as with lab-based HR-XRD measurements. The high intensity of X-rays produced by the synchrotron allows RSMs to be collected within minutes rather than hours, hence maps across the sample can be produced in a reasonable timeframe.

3.2.4 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a surface characterisation technique that is used to map the fine surface detail of materials and measure the surface roughness. The technique was invented by Binnig *et al.* in 1986 [122] and combines the operational principles of a scanning tunnelling microscope and a stylus profilometer. The surface of a sample is scanned with a sharp tip attached to a cantilever which interacts with the surface by both attractive (chemical forces, van der Waals and electrostatic) and repulsive forces (ionic repulsion). As the tip is rastered over the surface of a sample any raised features will cause the tip to bend. This is not how the AFM is used to measure surface morphology, however, instead the tip is driven close to the surface of the sample to a point where there are strong interactions and the height of the tip is varied using a piezo motor to keep the tip at a constant distance from the surface. This height offset that must be applied is then used to map the surface roughness of the sample [123].

All of the AFM data presented in this work was carried out using a Veeco Multimode AFM (Figure 3.9) using Si_3N_4 tips. This is a general purpose system that can image surface topology in both contact and tapping modes.

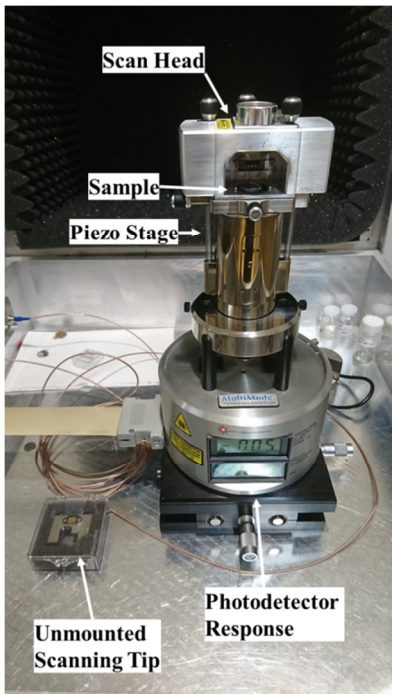

Figure 3.9 Veeco Multimode AFM.

Contact Mode

Contact mode is the simplest form of AFM as it relies solely on the deflection of the cantilever as the tip is scanned across a sample surface when in direct contact. To begin with, the tip is lowered down onto the surface slowly until the attractive forces cause it to "snap" into contact with the sample. The tip is then lowered further until the piezo stage has to increase its height (z) to a certain set-point in order to maintain a constant repulsive force between the sample and tip. The most common feedback system to control z is an optical deflection technique in which a laser is reflected off the cantilever and onto a position sensitive photodiode. A proportional-integral-derivative (PID) controller then analyses the feedback from the photodiode and sets the position of z using the piezoelectric motor to ensure the laser spot remains in the centre of the diode.

Tapping Mode

AFM can also be carried out in such a way that the tip is not in contact with the surface, instead resonating above the sample. This method, known as non-contact AFM was invented in 1987 by Martin *et al.* [124]. The method was then modified by Zhong *et al.* [125] who increased the amplitude of the cantilever resonance and also used cantilevers with a higher stiffness. The result was referred to as tapping mode as the tip was now

being influenced by the repulsive force from the sample surface. Tapping mode operates on the principle of the cantilever oscillating at a particular frequency. The cantilever is driven to resonance by an actuator before being lowered towards the sample surface. The repulsive forces between the surface and the tip cause the amplitude and phase of the resonance to change as the tip gets closer to the sample surface. Once a set-point has been reached the scan begins and as with contact mode, a feedback loop ensures that the oscillation amplitude remains constant. The main advantage of using tapping mode is that the tip is no longer in constant contact with the sample surface as the scan is being carried out. This significantly reduces damage to soft samples but also decreases damage to the tip when scanning hard samples, which is the case with SiC.

3.2.5 Scanning Electron Microscopy (SEM)

The scanning electron microscope (SEM) uses a focused beam of electrons to image samples. As electrons travelling at extremely high velocities can have very short wavelengths, as given by the de Broglie equation

$$\lambda = \frac{h}{p} \qquad \text{Equation 3.19}$$

where h is Planck's constant and p the momentum of the electrons, SEMs can achieve very high resolution down to ~1 nm. As visible light (400-700 nm) is significantly larger than this, one is able to image significantly smaller features using an SEM than a traditional optical microscope. In a standard SEM, the electron beam is typically rastered over the sample which produces a range of interactions and signals from which information on the sample composition and topology can be obtained. The optical column of an SEM comprises several key components, see Figure 3.10. The electrons that impinge on the sample surface can lead to a number of interactions which produce various signals such as: backscattered electrons, secondary electrons, Auger electrons and X-rays. The most commonly used signal is that of secondary electrons.

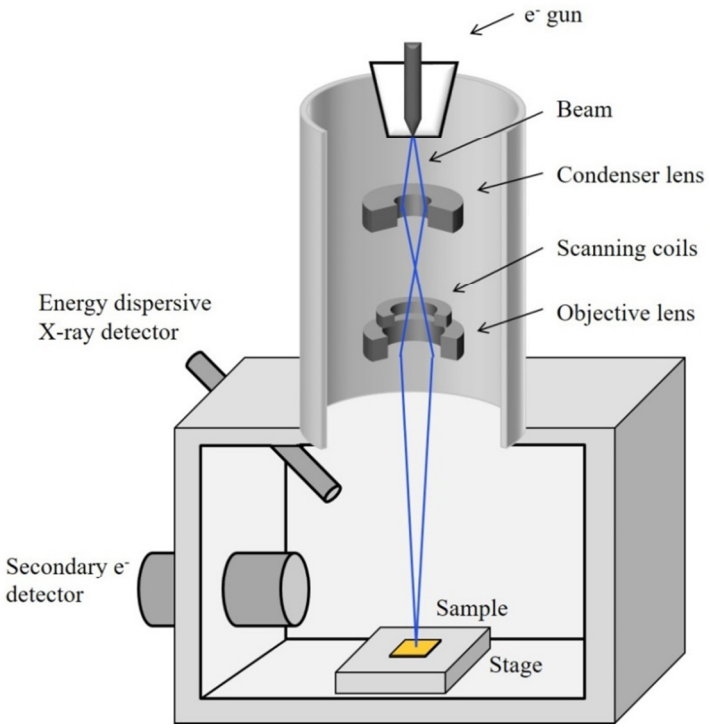

Figure 3.10 Simplified cross sectional schematic of an SEM with secondary electron detection and energy dispersive spectroscopy capabilities. Electrons are produced by an electron gun which can be either a tungsten filament, lanthanum hexaboride (LaB_6) crystal or field emission source. The emitted beam is then focused by the condenser lens which controls the spot size on the sample. The beam is then rastered by the scanning coils which also control the magnification of the image. An objective lens then focuses the beam onto the sample in order to produce a sharp image

The high energy electron beam ionises atoms in the surface of the sample which subsequently emit so-called secondary electrons. The intensity of secondary electrons depends on the atomic composition of the sample which leads to contrast between different materials. Secondary electrons can only be emitted from very close to the sample surface and as such, the surface morphology affects the intensity of electrons emitted from the sample, Figure 3.11. The secondary electron detector is typically positioned to the side of the sample which leads to a shadow effect as the detector will capture more electrons from parts of the sample that are orientated towards the detector position.

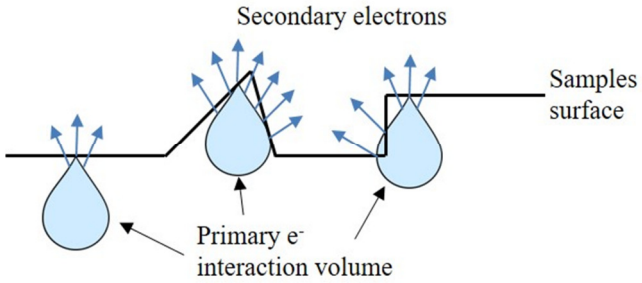

Figure 3.11 The teardrop interaction volume is produced where the electron beam strikes the sample. As secondary electrons can only be emitted from near the surface of the sample the morphology of the surface affects the number of electrons emitted.

Electrons in the beam can also excite atomic electrons in the sample from inner shells, leaving holes that outer electrons can fill. The transition of electrons from higher energy shells emits characteristic X-rays from different materials and can be used to map elemental composition in samples. This technique is called energy dispersive X-ray spectroscopy (EDS). For the work presented here SEM was carried out using a Zeiss SUPRA 55-VP which uses a field emission gun. The system is set-up with a range of detectors including: secondary electrons, backscattered and in-lens imaging modes. In addition, the system has an EDAX spectrometer for EDS measurements [126].

3.2.6 Transmission Electron Microscopy (TEM)

Another important electron microscope is the transmission electron microscope (TEM) which can be used to directly observe and analyse the crystalline structure and elemental composition of semiconductor samples. The main feature that distinguishes TEM from SEM is that electrons pass through the specimen before being focused onto an image capturing device, for this to occur the samples must be electron transparent i.e. thin enough for electrons to pass through the sample with only minimal interactions in the material itself. This requires careful preparation techniques briefly described below.

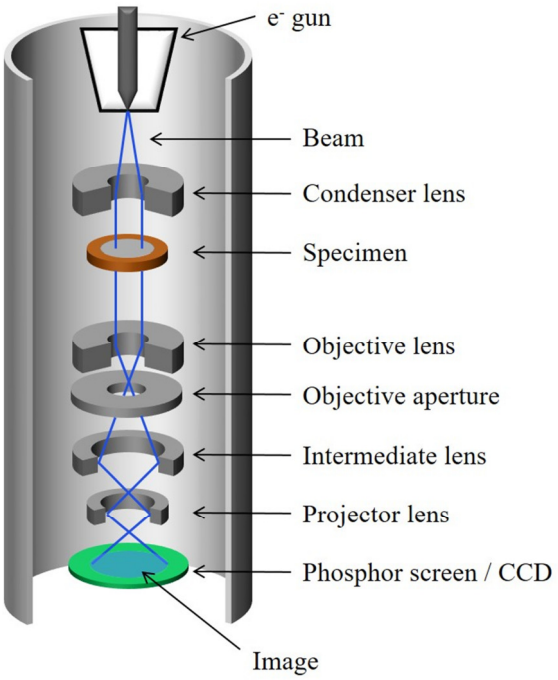

Figure 3.12 Simplified schematic of a typical TEM imaging column.

Figure 3.12 shows a cross sectional schematic through a typical TEM system and highlights the main components required for image formation. As with the SEM, electrons are generated by a source then passed through condenser lenses which set the spot size of the electron beam and directs the beam onto the specimen. After the electrons pass through the sample, the beam is focussed by an objective lens and can then be filtered by an objective aperture. The role of the objective aperture is critical for forming diffraction images which are described below. The beam then passes through a series of focusing lenses referred to as a singular intermediate lens before being focused by a final projector lens onto a phosphor screen or CCD image capturing device.

When the electron beam passes through a crystalline material, elastic scattering occurs which leads to Bragg diffraction. The result in the TEM is multiple beams emanating from the specimen which are focused by the objective lens forming a diffraction pattern, the beam of electrons which passes directly through the specimen is referred to as the straight through (ST) beam, see Figure 3.13.

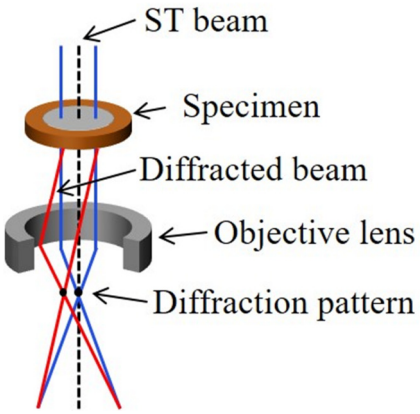

Figure 3.13 Showing how diffraction patterns are formed in the TEM.

Using a tilting specimen holder, it is possible to tilt the sample in such a way that diffraction of the straight through beam occurs on a specific set of crystal planes. The objective aperture can then be positioned such that either just the straight through beam or the diffracted beam is allowed to pass through. These two imaging modes are referred to as bright field and dark field respectively. Dark field TEM images can be used to observe the crystallinity of thin films, as areas which have the same crystal structure as the substrate will be lit up, assuming diffraction imaging on the TEM has been set up relative to the substrate. Under the same conditions, polycrystalline or amorphous regions of the crystal will be darker or invisible. Dark field imaging can also be used to highlight specific defects in crystals and observe strain effects. For more information of TEM and imaging modes the author recommends *Transmission Electron Microscopy* by Williams and Carter [127].

Sample Preparation

As previously mentioned, samples for TEM imaging need to be electron transparent, which for standard semiconductor samples means thicknesses close to or below 100 nm. There are a couple of methods to achieve this, the most convenient of which is through mechanical grinding and polishing, see Figure 3.14.

SiC epilayers grown by homoepitaxy on SiC substrates cannot be prepared in this manner as the grinding pads are not hard enough to thin the SiC material, diamond coated grinding paper or other methods must instead be used. Crystalline 3C-SiC/Si can be processed in the described manner if the epilayer is relatively thin (up to a couple of microns). The author has found that beyond this thickness the Si substrate etches far

more rapidly in the PIPs compared to the 3C-SiC making it impossible to find a region of 3C-SiC and Si that are both electron transparent.

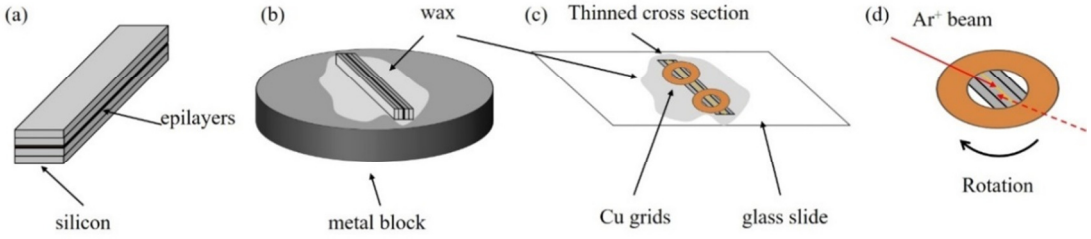

Figure 3.14 The main steps carried out in TEM sample preparation. (a) Epilayers are glued together into a stack and sawn in half, (b) The sample is bonded to a metal block using molten wax, (c) The sample is thinned using amorphous SiC grinding paper and Cu rings are glued to the cross section, (d) The sample is thinned further using a beam of Ar^+ ions within a precision ion polishing system (PIPs) until an electron transparent region is formed.

3.2.7 Focused Ion Beam Scanning Electron Microscopy (FIB-SEM)

For thicker 3C-SiC samples, or in specific cases where a TEM cross section has to be extracted from a particular point on a sample, a FIB-SEM lift-out technique can be used. A FIB-SEM is similar to an SEM with additional functionality, namely a focused ion beam (FIB) column entering the specimen chamber at a different angle to the SEM column. The FIB column differs from an SEM column as it focused ions rather than electrons onto the sample. The incident ions still give off characteristic secondary electrons that can be measured by a detector, however, the higher energy of the FIB beam (due to the greater mass of the ions) can be used to etch samples where the beam is incident, allowing features to be etched into samples. In addition to the FIB, FIB-SEM systems typically have gas sources which can be broken down by the ion beam resulting in deposition.

For the research presented below, a Jeol 4500 FIB-SEM was used which consists of a 30 kV SEM column with a LaB_6 electron source and a 30 kV FIB column with a Ga^+ ion source angled at 52° from the vertical SEM column. The intensity of the FIB beam can be adjusted by selecting different apertures. The system is fitted with two gas sources of C and tungsten (W) (only C was used during this research) and a micromanipulator consisting of a very fine needle which can be moved in XYZ with great precision, see Figure 3.15.

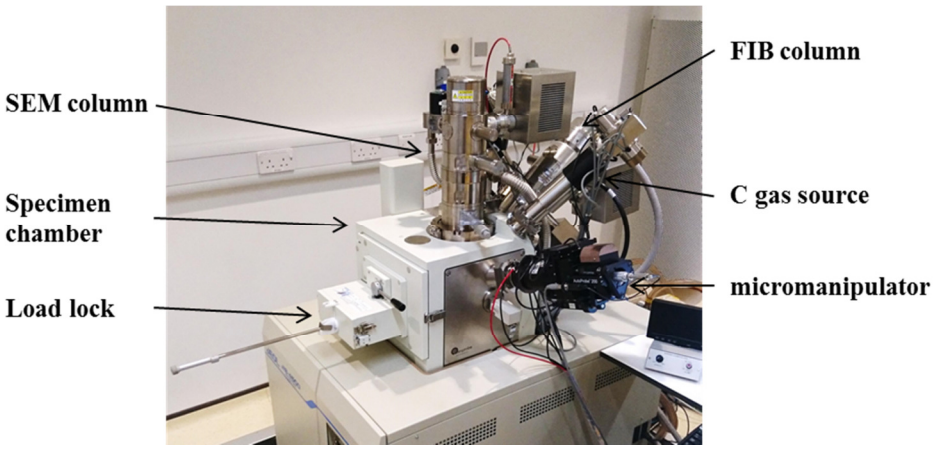

Figure 3.15 Jeol 4500 FIB-SEM used for TEM preparation through lift-out.

The lift-out process is shown best in Figure 3.16. A C strip is first deposited using a low intensity FIB beam to avoid any additional damage to the surface of the sample to be extracted (step A). Two trenches are then etched using a high intensity FIB beam ensuring that the depth is beyond the desired height of the extracted cross section (Step B). The micromanipulator is then bonded to the top of the cross section using C and cut out with the FIB (step D). The cross section is then bonded to a TEM grid, again using C, and the manipulator needle is cut away (step E). The sample is then thinned with the FIB using progressively lower intensity beams to minimise damage to the cross section (step F). The centre of the sample is thinned as much as possible to obtain electron transparency, typically below 100 nm).

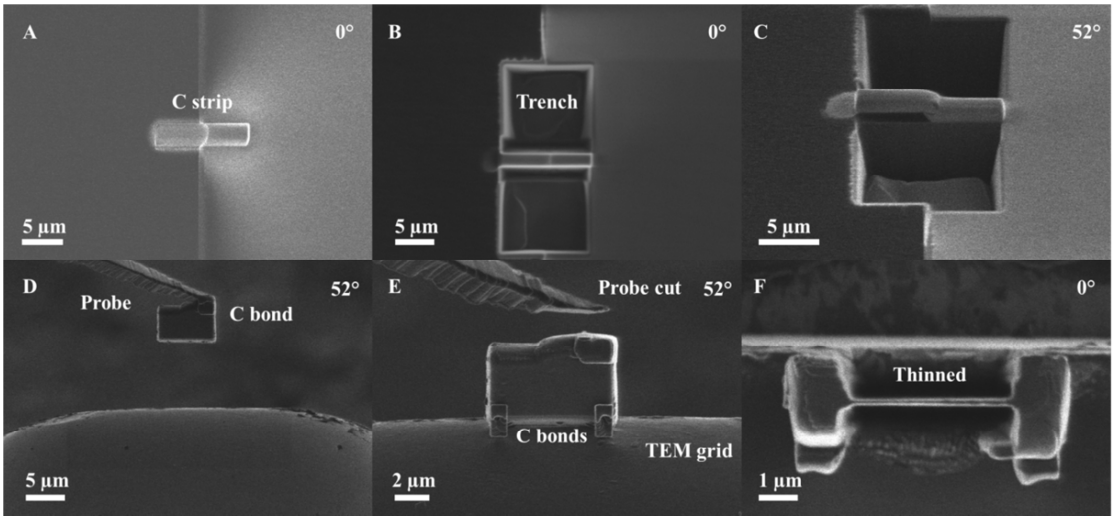

Figure 3.16 The main steps in the lift-out process carried out by the Jeol 4500 FIB-SEM. All images are taken through SE measurements from the FIB column frame of reference.

3.2.8 Raman Spectroscopy

As 3C-SiC possesses a zinc-blende crystal structure it exhibits two types of lattice vibrations known as acoustic and optical phonons. Raman scattering is a non-destructive characterisation technique that can be used to measure the optical phonon modes giving information on the structure, quality and strain state of semiconductor crystals as well as various other uses across chemistry, biology, security and inspecting fraudulent artwork. Optical modes in 3C-SiC are formed by the difference in electronegativity of the Si and C atoms resulting in out-of-phase atomic movements in the lattice. These modes can be split into transverse (TO) and longitudinal (LO) optical modes and lead to vibrational energy states within the crystal.

Raman spectroscopy involves exciting molecular vibrations with a laser source, typically in the UV, Visible or near IR wavelength. The majority of the energy states will return to their original level resulting in elastic scattering (Rayleigh scattering) of the incident photons, however, a small number of photons will be emitted with slightly higher or slightly lower energies as vibrational modes relax to different vibrational energy states, see Figure 3.17.

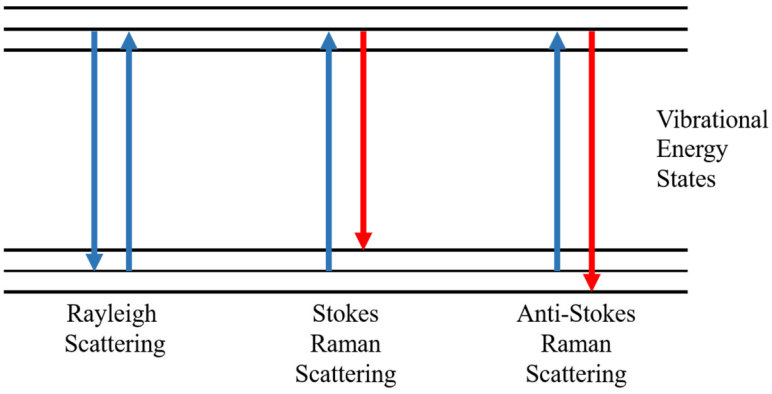

Figure 3.17 Interactions of incident light on vibrational energy levels within a crystalline structure. In most cases light scatters elastically as with Rayleigh Scattering, however, transitions can drop to excited states (Stokes) or begin from excited states dropping to the ground level (Anti-Stokes) which results in a Raman shift dependent on the vibrational modes in the crystal.

A Raman spectrometer filters out the strong Rayleigh scattered light and measures the shift between the Raman peak and the incident wavelength giving the Raman spectrum as a series of peaks measured in Raman shift, typically expressed as a wavenumber (cm^{-1}). The TO and LO Raman peaks for 3C-SiC are found at shifts of approximately

794 cm^{-1} and 968 cm^{-1} respectively [128]. Si is a non-polar semiconductor and hence only exhibits a single 1st order Raman peak at 520.5 cm^{-1}, which is often used for calibration purposes. For a more detailed description of Raman spectroscopy there are a number of useful textbooks including *Introduction to Raman Spectroscopy* by J. R. Ferraro [129].

3.3 Electrical Characterisation Techniques

3.3.1 Transfer Length Method (TLM)

The transfer length method (TLM) is an experimental technique that allows one to measure the sheet and contact resistance of a semiconductor device test structure. Various test structures can be used to perform these measurements, one of the most reliable device structures is that of the linear transfer length method (l-TLM) which consists of a series of Ohmic contacts on a semiconductor mesa of different separation, see Figure 3.18. For l-TLMs a mesa is required to ensure the current path is restricted to a well-defined volume which allows an accurate measurement of sheet resistance to be made.

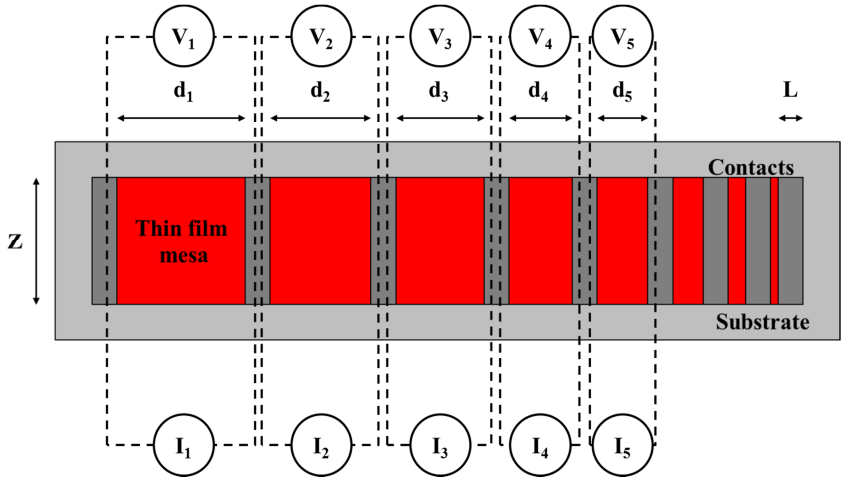

Figure 3.18 Typical linear TLM test structure.

The total resistance (R_T) is a combination of the contact resistance (R_C) from both contacts and the sheet resistance (R_{Sh}) of the semiconductor sample given by

$$R_T = \frac{R_{Sh}d}{Z} + 2R_C. \qquad \text{Equation 3.20}$$

By measuring the resistance between different metal contacts it is possible to build up a linear plot of separation distance against resistance, see Figure 3.19. The gradient and y-axis intercept can be extracted from this plot and give the sheet and contact resistance.

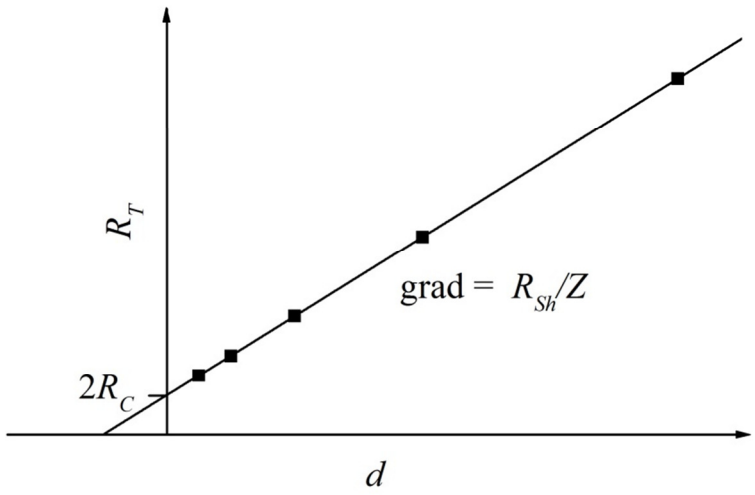

Figure 3.19 Plot of total resistance against separation length for a l-TLM test structure.

3.3.2 Hall and Resistivity Measurements

The Hall Effect is observed in a conducting material when a magnetic field (B) and current (I) are applied in non-parallel orientation, usually perpendicular. A Hall voltage is generated in the direction perpendicular to both B and I as a result of the Lorentz force acting upon charge carriers. This Hall voltage (V_H) is typically measured using one of two methods: Hall Bars and van der Pauw structures.

Hall bars offer a well-defined test structure where the mesa and contact dimensions as well as the current path are well known, see Figure 3.20.

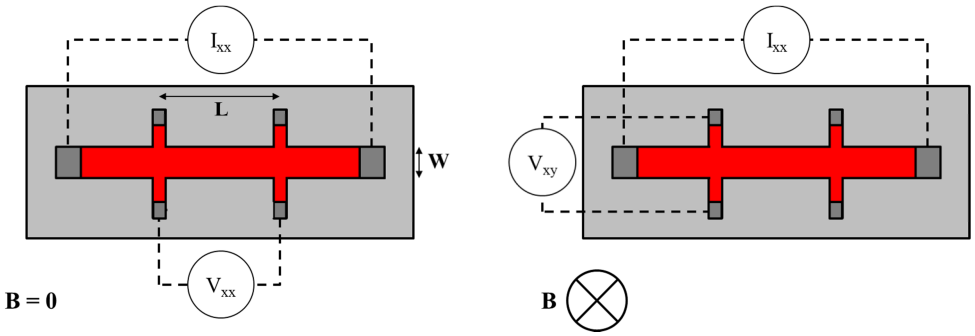

Figure 3.20 Hall Bar device structure measurement set-up for measuring sheet resistance (left) and Hall voltage (right).

The sheet resistance is calculated using

$$R_{Sh} = \frac{W}{\mathrm{L}} \frac{V_{xx}}{I_{xx}}$$ Equation 3.21

when a magnetic field (B) is applied to the test structure the sheet carrier density is given by

$$n_{Sh} = \frac{BI_{xx}}{qV_{xy}}$$ Equation 3.22

using both of these equations gives the Hall mobility

$$\mu_H = \frac{V_{xy}}{R_{Sh} I_{xx} B} = \frac{1}{q n_{Sh} R_{Sh}}$$ Equation 3.23.

The van der Pauw method operates in a similar way and works on the concept that the specific resistivity of an arbitrary shaped flat sample can be measured without knowing the exact path of the current. This only works if the test structure meets the following criteria: contacts are at the circumference of the device, the contacts are small and the sample thickness is uniform. A typical structure is shown in Figure 3.21.

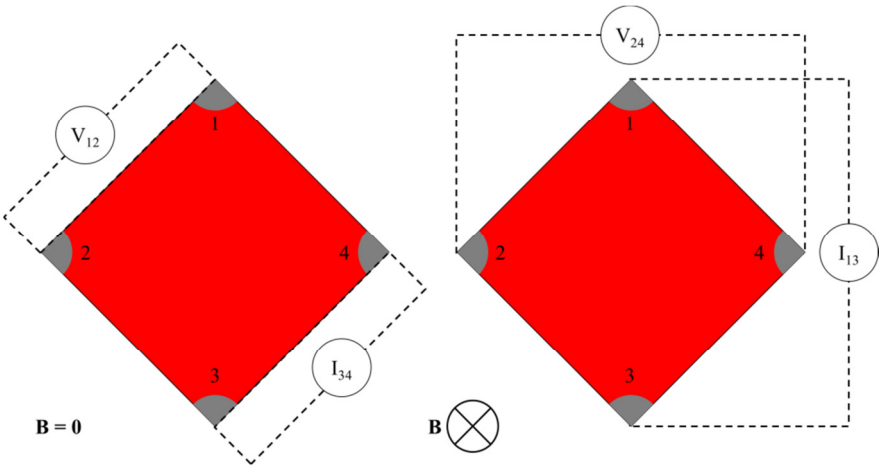

Figure 3.21 van der Pauw device structure measurement set-up for measuring sheet resistance (left) and Hall voltage (right).

TLM and Hall measurements require test device structures which are typically fabricated through a combination of lithography, metal deposition and etching processes. These techniques are also used to fabricate other devices or semiconductor structures and are briefly described below.

3.3.3 Lithography

Lithography is the general term given to the process of defining features on a semiconductor (or other material) surface using a particular masking agent. For this research, a particular form of lithography known as photolithography was used. A chemical, sensitive to particular bands of UV light (photoresist), is deposited onto the surface of the semiconductor and spun at high speed to form a uniform thin film. The photoresist is typically solvent based and cured after spinning at high temperatures. Parts of the resist film are then exposed to UV light, which affects the polymers within the resist in a certain way, by passing light selectively through a mask. The exposed resist can either then be removed with a developing chemical (positive resist) or hardened through subsequent curing such that the non-exposed resist is later removed (negative resist), see Figure 3.22. Negative and positive photoresists are used in different circumstances as they result in different side wall slopes which can affect steps later in the fabrication process such as metal deposition and lift off.

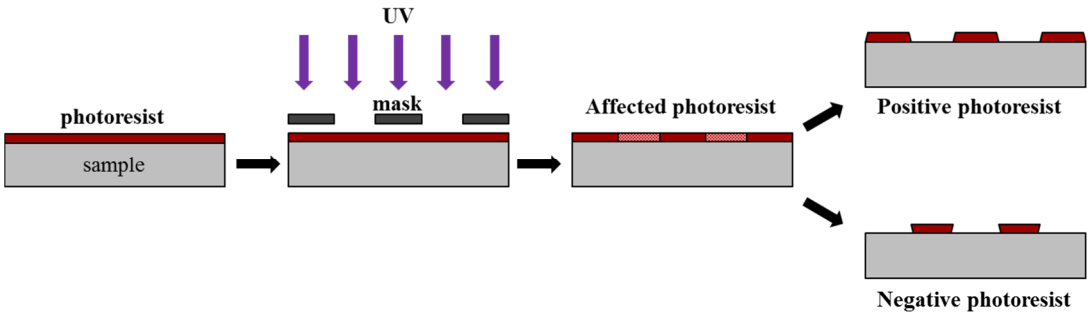

Figure 3.22 The main steps involved in photolithography.

3.3.4 Metal Deposition

Another critical process for device fabrication is metal deposition, which can be used for creating low resistance Ohmic contacts, gates or other structures on semiconductors. Metal deposition is typically carried out using physical vapour deposition (PVD) techniques which can include evaporation and sputtering; both techniques were used in this study. Evaporation is a deposition process in which a target material is evaporated into its gas phase. This can be achieved in a range of methods, such as through resistive heating (thermal evaporation) or bombardment with electrons (e-beam evaporation). Sputtering is achieved by the emission of particles from a source target through bombardment with other energetic particles [130]. This can be carried out in a range of

different ways, however, sputtering in this case was achieved within an Ar^+ ion plasma. Sputtering is a useful technique for depositing materials with high melting temperatures where evaporation can be troublesome.

In both cases of evaporation or sputtering, deposition is carried out under vacuum conditions (1×10^{-2} to 1×10^{-7} mBar) in order to increase the mean free path of the deposited materials and remove any contamination such as moisture or O_2.

3.3.5 Etching

Etching is a broad term which relates to the removal of material from a sample. In semiconductor device fabrication both wet and dry etching are carried out. Wet etching is a process in which a material is etched or completely removed through the use of appropriate chemicals. Depending on how the chemical reacts with the etched material, the process can either be isotropic or anisotropic. Dry etching is a similar process to sputtering, however, in this case the sample is bombarded with reactive ions in order to etch the surface to a particular depth. Typically, fluorine or chlorine based gases are used to dry etch semiconductors in a process known as reactive ion etching (RIE). Dry etching is a directional process and highly anisotropic. Standard photoresists or metal masks can be used to resist the effect of dry etching, allowing fine features to be formed in semiconductor samples. Dry etching is particularly useful for SiC which is inert to almost all wet etching processes and can be used for routine etching of SiC.

For more information on device fabrication processes the author recommends *Semiconductor Devices: Physics and Technology* by S. Sze [131].

3.3.6 Suspended Structures

Anisotropic wet etching can be achieved using particular chemicals that are sensitive to different crystal planes. When etching Si, a range of different alkaline chemicals can offer this selectivity such as KOH, sodium hydroxide (NaOH) and tetramethylammonium hydroxide (TMAH) [132]. One of the most common etchants used for etching Si is KOH and the effect of the etchant on different Si crystal planes has been well investigated [133]. It is well known that the etch rate of the Si {111} planes is significantly slower than other crystal planes in Si which could be a result of its tight packing crystal structure. Typical etch rates of Si (111) can be below 0.005 µm/min compared to Si (001) which etches at around 0.8 µm/min, depending on temperature (typically 70 to 90 °C) and KOH concentration [134]. At the temperature

required to etch Si, the etch rate of SiC is negligible (<20 Å/hr. for amorphous films [47]) and instead temperatures exceeding 600 °C are required for SiC etching [135]. Alkaline etchants offer a highly selective method of etching underlying Si from 3C-SiC heterostructures and opens up opportunities to fabricate a range of suspended structures, including membranes, cantilevers and wires. These structures are investigated later in this work where specific fabrication techniques are discussed in more detail.

Chapter 4
High Temperature 3C-SiC Heteroepitaxy

4.1 Introduction

3C-SiC is typically grown at high temperatures very close to the melting point of Si (~1410 °C) in order to achieve high crystal quality growth and maintain high crystallinity and growth rate when growing thick epilayer of 10's of microns for power electronic applications. To investigate the material properties of 3C-SiC grown under these conditions, a commercially available 3C-SiC/Si (001) heterostructure was purchased and used as a reference sample. 3C-SiC was then grown using similar conditions within an LPE ACIS M8 RP-CVD system in order to understand the issues with high temperature growth and attempt to replicate the commercially available material.

4.2 Commercial Grade Material

The sourced 3C-SiC heterostructure was approximately 10 μm thick and grown on an on-axis, 100 mm Si wafer. Due to the thickness of the epilayer, standard grinding and polishing with SiC based grinding pads is difficult and incredibly time consuming. To achieve a uniformly thin cross section from the heterostructure a FIB-SEM lift out was performed to remove a thin slice of the 3C-SiC/Si going down to the substrate. This sample was thinned using the FIB on a low power to below 100 nm thick and imaged within a JEOL JEM 2000FX TEM system, see Figure 4.1. In the cross sectional TEM (X-TEM) bright field (BF) image it is possible to observe a void in the Si substrate at the interface, a common effect when growing at high temperatures due to the out-diffusion of Si from the substrate during growth. In the dark field (DF) image the

defects in the 3C-SiC have been highlighted. While these have been labelled as stacking faults, at this level of magnification it is impossible to distinguish between stacking faults and microtwins, to do this requires lattice resolved images at much higher magnification not possible within this TEM system.

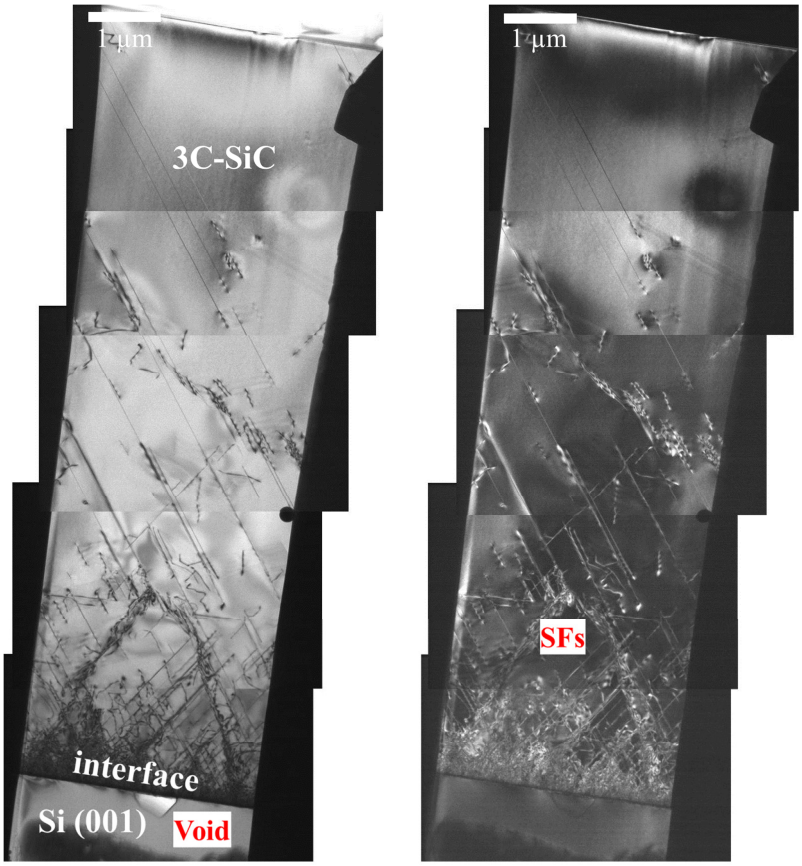

Figure 4.1 X-TEM images of commercially available 3C-SiC taken under BF(220) (left) and DF(220) (right) conditions, highlighting the propagation of stacking faults (SFs) through the 3C-SiC epilayer.

Using the TEM images it is possible to estimate the linear defect density as a function of thickness in the 3C-SiC epilayer. The result of this analysis is shown in Figure 4.2. The number of defects decreases with thickness due to the annihilation of planar defects in the epilayer, this phenomenon can be observed in Figure 4.1 which shows an almost exponential decay of defect density with thickness.

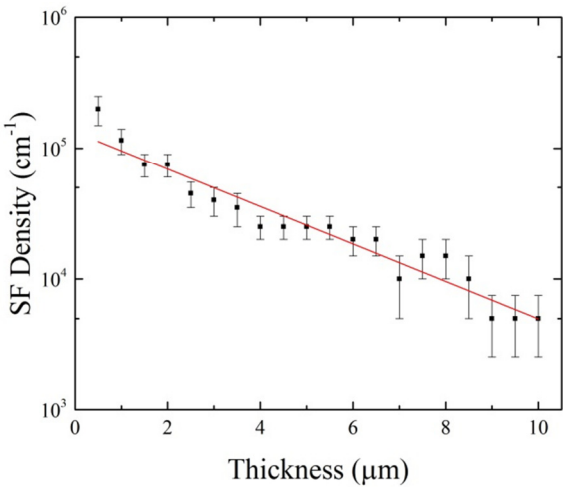

Figure 4.2 Stacking fault or microtwin density as a function of thickness through the 3C-SiC epilayer, extracted from cross sectional TEM.

The surface of the 3C-SiC is incredibly smooth as the epilayer has undergone chemical mechanical polishing (CMP) resulting in a root mean squared (RMS) roughness below 0.19 nm, see Figure 4.3. The surface roughness of as-grown 3C-SiC/Si (001) epi wafers can exceed 100 nm and increases dramatically with layer thickness [136]. The track marks in the 3C-SiC surface are indicative of the CMP process because of the diamond polishing pads used to grind and polish the rough SiC surface. Although the surface of the sample is smooth, there are small features present on the 3C-SiC epilayer. It is possible that these are a result of the CMP process, but could also be due to external contamination or features of the crystal itself.

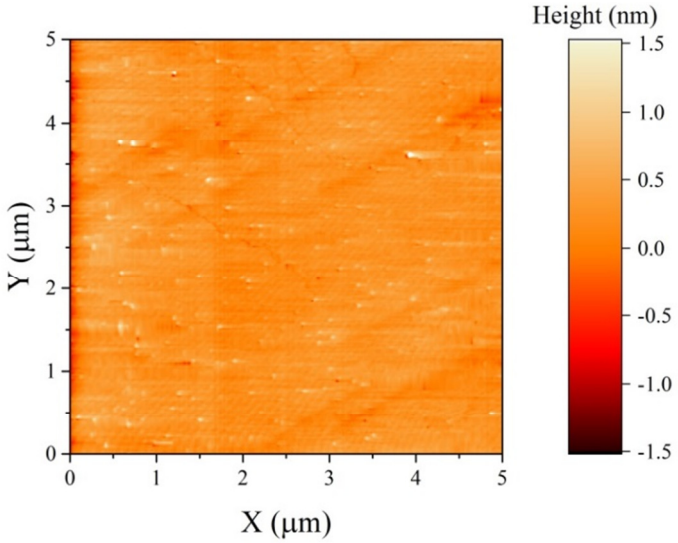

Figure 4.3 AFM surface roughness scan of the commercially available 3C-SiC, taken in contact mode showing track marks indicative of post growth CMP.

A common issue with the high temperature growth of 3C-SiC, and other polytypes of SiC, is the unintentional incorporation of Nitrogen (N) in the growth process. As N atoms can occupy the C lattice site in the SiC crystal the element acts as an n-type dopant in SiC which can be an issue for the use of SiC in power electronic devices, leading to high leakage currents and reduced breakdown voltages due to a narrowing of the depletion region. To assess the level of incorporation in the commercially available 3C-SiC, simple van der Pauw devices were fabricated through the evaporation of Ni contacts through a shadow mask onto the 3C-SiC surface. By cleaving the sample, squares of ~5 mm sides were formed with contacts in each quarter as shown in Figure 3.21. The contacts were found to be Ohmic without the need for thermal annealing making them suitable for Hall measurements which were carried out in a closed cycle cryostat at a magnetic field of 400 mT from room temperature down to 50 K at which point the contacts were no longer Ohmic. The resulting temperature dependence of carrier concentration and resistivity are shown in Figure 4.4.

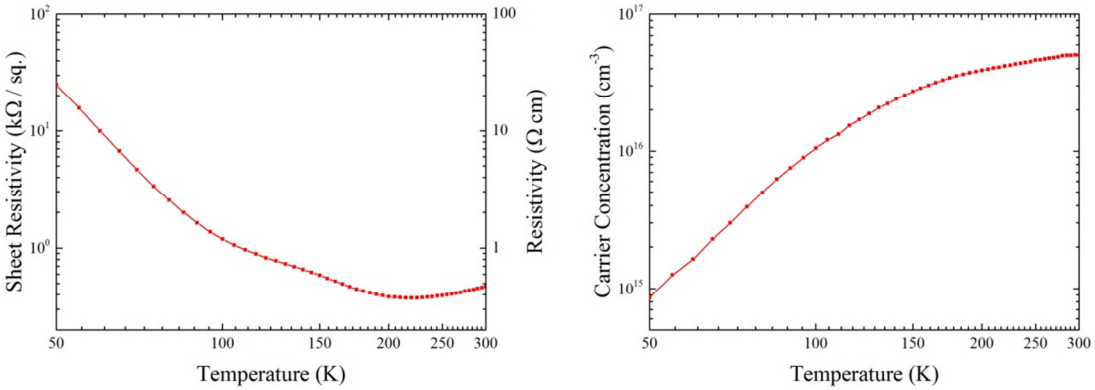

Figure 4.4 Sheet resistance (left) and carrier concentration of commercially available 3C-SiC extracted from van der Pauw Hall measurements.

As 3C-SiC is a wide bandgap semiconductor, thermally excited carriers have little effect at room temperature, thus the electrically active carriers in the epilayer are dominated by impurities, in this case N. The carriers are observed to freeze out at temperatures below ~150 K, however, at room temperature the level of impurities is approximately 5×10^{16} cm^{-3}. The electron mobility of the 3C-SiC sample was found to be ~329 cm^{2}V^{-1}s^{-1} at room temperature, almost 1/3 of the theoretical value implying defects within the epilayer are negatively impacting the electrical properties.

4.3 Epitaxial Growth

High temperature 3C-SiC growth was carried out in the LPE ACIS-M8 RP-CVD system at a growth temperature of 1350 °C and pressure of 100 Torr. The Si was first carbonised with ethylene at lower temperature before growth commenced using ethylene and Trichlorosilane (TCS). The growth process is shown diagrammatically in Figure 4.5 and produced an epilayer approximately 5 µm thick. For this growth the ratio between the C/Si atoms in the gaseous precursors injected into the CVD was fixed at 1.4 by manipulating the flow rates of the TCS and ethylene appropriately. To achieve crystalline 3C-SiC growth, the amount of C and Si adatoms reacting on the substrate surface should be stoichiometric, however, due to the varying reactivity of the two precursors this rarely corresponds to equal precursor flow rates. As C based precursors are usually less reactive than Si ones, 3C-SiC is typically grown at a C/Si ratio that is greater than 1, however, the exact value depends on the gases, temperature, pressure and CVD reactor itself.

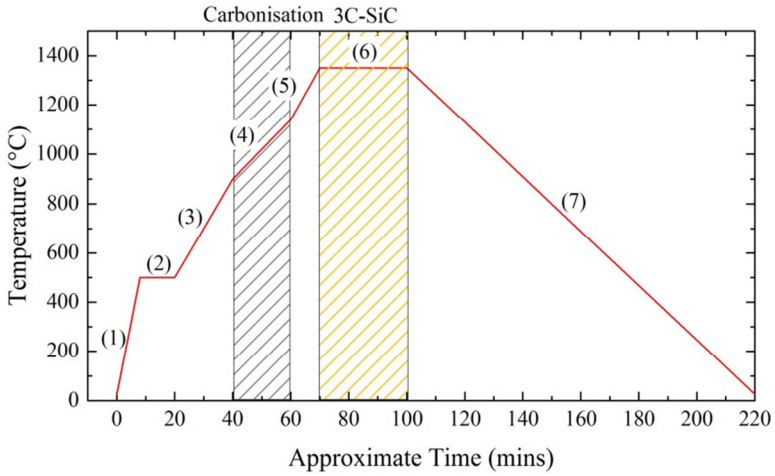

Figure 4.5 Growth process for the 3C-SiC/Si heterostructure. (1) – Si wafer is loaded at room temperature, (2) – Temperature ramped to ~500 °C for bake out, (3) – temperature raised to 900 °C for thermal desorption of SiO_2, (4) – carbonisation with ethylene as temperature is raised from 900 to 1140 °C, (5) – temperature raised to 1350 °C, (6) – growth carried out for 30 mins using a C/Si ratio of 1.4, (7) – temperature brought back to room temperature for unloading.

4.4 Material Characterisation

As expected, the 3C-SiC epilayer grown at high temperature exhibited an extreme level of wafer bow in excess of 1 mm at the edges, see Figure 4.6. The extreme wafer bow is

a combination of the thermal mismatch caused by the high growth temperature and the thickness of the 3C-SiC epilayer.

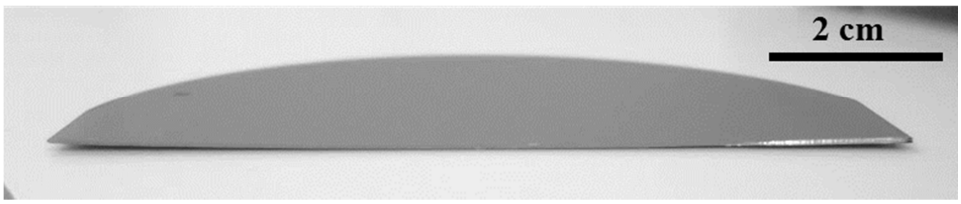

Figure 4.6 Photograph of high temperature grown 3C-SiC cross section showing wafer bow caused by the effects of thermal mismatch..

The wafer bow of the 3C-SiC/Si epi wafer was measured using a stylus profilometer over a quarter of the wafer and extrapolated to give a cross section over the wafer diameter, see Figure 4.7. The wafer bow was measured to be around 1 mm across 90% of the wafer diameter.

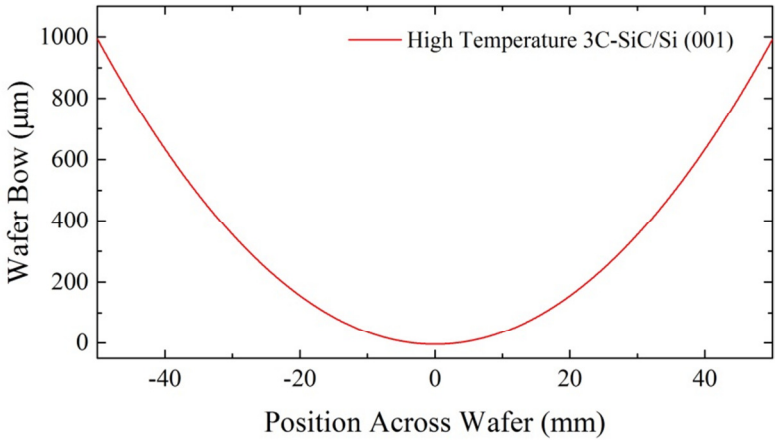

Figure 4.7 Wafer bow measured across the 3C-SiC/Si (001) 100 mm epi wafer grown at 1350 °C.

HR-XRD measurements were carried out to assess the crystallinity of the 3C-SiC epilayer, see Figure 4.8. While the sample gives strong (004) and (002) Bragg reflections, additional peaks from the 3C-SiC at (111), (220) and (311) can be observed indicating that at least part of the 3C-SiC material is polycrystalline.

The 3C-SiC epilayer was found to be free of tilt with respect to the underlying Si substrate, however, an asymmetric RSM shows that the 3C-SiC is under residual tensile strain of approximately 0.098% resulting in a shift of the 3C-SiC (224) Bragg peak to the left of the expected position for fully relaxed material, see Figure 4.9.

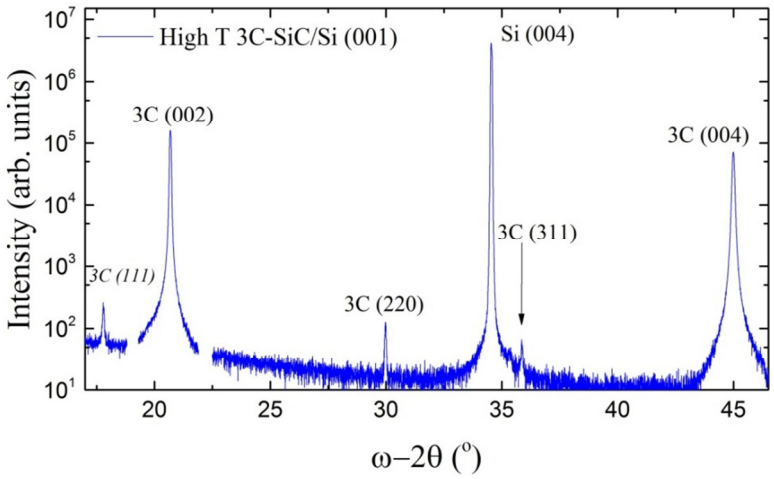

Figure 4.8 HR-XRD coupled scan of the 3C-SiC epilayer grown at high temperature within the LPE ACIS 8 RP-CVD system. For clarity Bragg peaks from the Al stage have been removed at approximately 18° and 22°.

The residual tensile strain in the layer is a result of the wafer bowing effect caused by thermal mismatch.

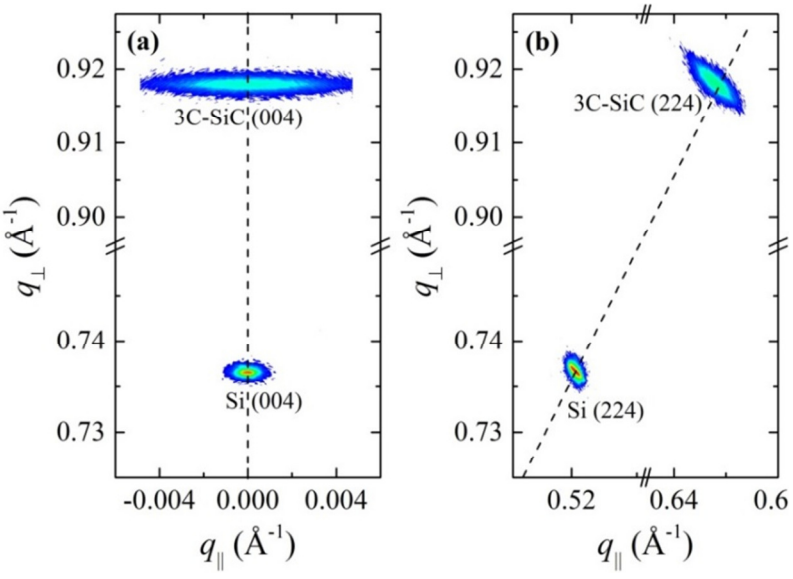

Figure 4.9 Symmetric (left) and asymmetric (right) RSMs of the high temperature grown 3C-SiC. The epilayer is free of crystalline tilt and is under residual tensile strain of 0.098% due to thermally induced wafer bow.

As the 3C-SiC was not polished subsequent to crystal growth, the surface of the epilayer is very rough leading to a non-mirror like surface with an RMS roughness in excess of 200 nm, beyond the capability of the AFM measurement process. The morphology of the 3C-SiC surface is best observed using an SEM, see Figure 4.10.

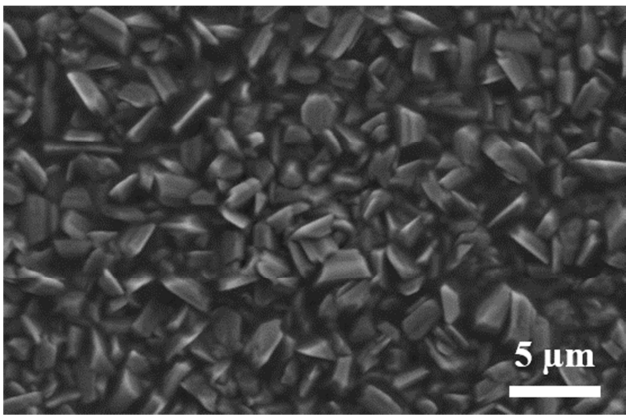

Figure 4.10 Secondary electron SEM image highlighting the surface morphology of high temperature grown 3C-SiC.

The surface of the 3C-SiC is extremely rough and is dominated by faceted islands, something that could not be observed on the commercial material as it had undergone CMP. The facets appear to be randomly orientated which would imply polycrystalline Volmer-Weber growth has occurred at some point in the growth of the 3C-SiC. The crystal quality of the as-grown 3C-SiC was further assessed by cross-sectional TEM, see Figure 4.11.

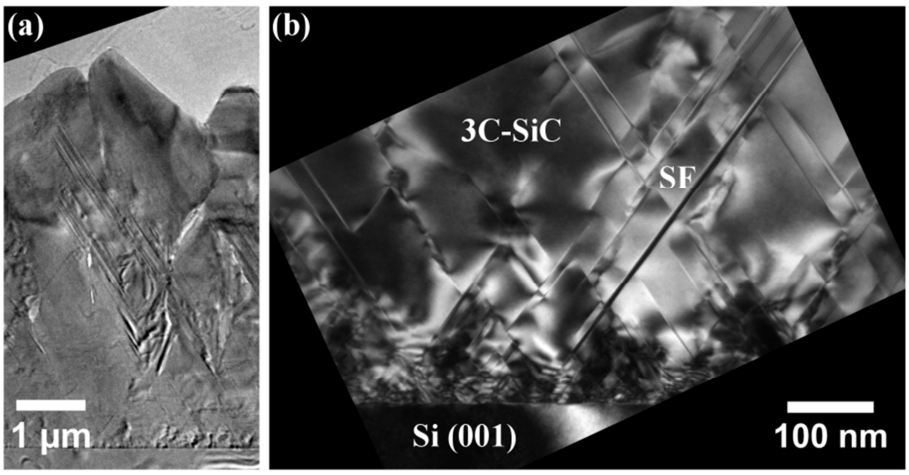

Figure 4.11 X-TEM images of the high temperature grown 3C-SiC. (a) Straight through image of the heterostructure showing the thickness of the entire epilayer. (b) Higher magnification DF(004) image of the 3C-SiC/Si interface showing the presence of planar defects (here labelled stacking faults).

The micrographs show that near the Si (001) substrate and 3C-SiC interface the 3C-SiC is monocrystalline, however, a change in the crystal quality can be observed to occur at the point where the 3C-SiC is 3-4 µm thick at which point the different grains that lead to the faceted surface being to appear.

4.5 Discussions

The crystalline quality and electrical properties of the state-of-the-art, commercially available 3C-SiC grown on Si (001) have been assessed through a number of characterisation techniques. The material is found to be crystalline, though dominated by planar defects which annihilate reaching a defect density of ~10^5 cm^{-1} at an epilayer thickness of 1 µm before decreasing to below 10^4 cm^{-1} once the epilayer was above 6 µm thick. The surface roughness of the layer could not be analysed as the heterostructure had undergone polishing post-growth. A high number of electrically active dopants were found in the 3C-SiC through Hall Effect measurements which are presumed to be due to unintentional N doping during epitaxy.

A high temperature 3C-SiC epilayer was heteroepitaxially grown in-house using the LPE ACIS M8 RP-CVD system on a standard Si (001) substrate at a growth temperature of 1350 °C at a growth rate of approximately 10 µm/hr. The material was found to be monocrystalline from the Si interface until a critical thickness of around 3 µm at which point facets began to form in multiple directions, indicating polycrystalline island growth. This would indicate that the levels of strain in the 3C-SiC/Si system increased during epitaxy eventually resulting in poor surface dynamics, which resulted in polycrystalline growth. This was observed by TEM imaging and corroborates the results observed by HR-XRD. The resulting surface was rough and unsuitable for device fabrication without polishing. The biggest concern of the epi wafers was the high levels of thermal stress and wafer bow. The wafer bow was in excess of 1 mm at the edges of the wafer which makes the epi wafer completely unsuitable for full wafer scale device fabrication and is likely to be more severe on larger wafers. While more research into the high temperature growth process could have improved the material quality, the authors felt this would be simply a wasted effort, attempting to replicate commercially available material which in itself suffers from a number of issues making it unsuitable for mass production of commercial devices. As such, it was deemed necessary to change the scope of research towards a more novel approach.

Chapter 5
Growth of Silicon Carbon Alloys

5.1 Introduction

Silicon carbon ($Si_{1-y}C_y$) is an alloy formed from the substitutional incorporation of C into lattice sites within a Si crystal and has a range of applications in strain engineering as well as acting as an effective diffusion barrier [137]. Due to the huge difference in lattice constants of ~34% between Si and C (diamond), the C solubility limit at the melting point of Si is only ~3×10^{17} atoms/cm^3 [138]. Fortunately, concentrations of up to a few percent can be achieved through the use of non-equilibrium growth conditions that are achievable within MBE or CVD techniques. The highest concentrations of substitutional C in $Si_{1-y}C_y$ layers currently stand in the region of 2.3-2.8%, as grown by the industry standard RP-CVD [139, 140]. It has been shown that lower temperatures and high growth rates are desirable for $Si_{1-y}C_y$ growth, significantly reducing the probability that C atoms will take up more energetically favourable interstitial sites within the Si lattice [141]. Consequently, successful RP-CVD growth has relied on highly reactive Si precursors such as trisilane (Silcore®) to accelerate the growth rate while maintaining a low temperature. The use of trisilane is often undesirable in industry due to its increased cost and the fact that it is a liquid source. The use of a gaseous precursor, such as disilane makes handling easier as well as decreasing the overall cost of epitaxial growth. Issues are also encountered with the growth of $Si_{1-y}C_y$ by MBE; whilst high substitutional C incorporations beyond 10% in highly defective layers have been reported [111], MBE cannot provide the high throughput of RP-CVD required within industry and does not allow selective epitaxy. Research into the growth of $Si_{1-y}C_y$ using disilane has found critical C compositions of approximately 1.5%, above which surface islands or hillocks form [142, 143]. The formation of these hillocks

is attributed to the precipitation of interstitial C, however, little is known about their formation and crystal structure.

One of the challenges of $Si_{1-y}C_y$ growth is to achieve high quality epilayers for use in the various applications outlined above, without relying on either high-cost precursors or growth techniques other than RP-CVD. The aims of this investigation were to successfully grow $Si_{1-y}C_y$ epilayers on Si (001) substrates using disilane (Si_2H_6) and a suitable C source precursor within an industrial type RP-CVD system. Candidates for this precursor included highly reactive methylsilanes such as monomethylsilane (CH_3SiH_3) (MMS) and trimethylsilane ($(CH_3)_3SiH_3$) (TMS). While both precursors were considered for this study, the results presented below focus solely on the use of TMS as it is a more reactive precursor, resulting in higher quality growth. The formation and crystallinity of surface defects encountered through the use of these relatively low-cost precursors are investigated and the density and size of these hillocks are related to the thickness and C concentration of $Si_{1-y}C_y$ layers.

5.2 Epitaxial Growth

$Si_{1-y}C_y$ epilayers were grown directly on Si (001) substrates by an ASM Epsilon 2000 RP-CVD system, using disilane and TMS as precursors. All precursors were diluted in H_2 which was also used as the carrier gas. The growth temperature and pressure were maintained at 550 °C and 100 Torr respectively for each growth. The flow rate of disilane was kept constant between growth processes at a rate that maximised the $Si_{1-y}C_y$ growth rate. The substitutional C content within the $Si_{1-y}C_y$ growth was increased from samples A-D through the increase of the TMS flow rate. The growth time was kept constant for four samples (A3, B, C, D) grown at different TMS flow rates, while for three samples (A1, A2, A3) the TMS flow rate was maintained constant while the growth time was varied. For a summary of the variable growth parameters please refer to Table 5.1.

Table 5.1 Growth parameters of as grown $Si_{1-y}C_y$/Si (001) heterostructures.

Variable	A1	A2	A3	B	C	D
Pressure (Torr)	100	100	100	100	100	100
Temperature (°C)	550	550	550	550	550	550
Growth time (mins)	3	10	30	30	30	30
TMS flow rate (sccm)	30	30	30	45	60	75

5.3 Material Characterisation

5.3.1 Composition and Crystal Structure

The crystal quality and C content of samples A-D were determined using HR-XRD coupled ω-2θ scans of the Si and $Si_{1-y}C_y$ (004) Bragg peaks.

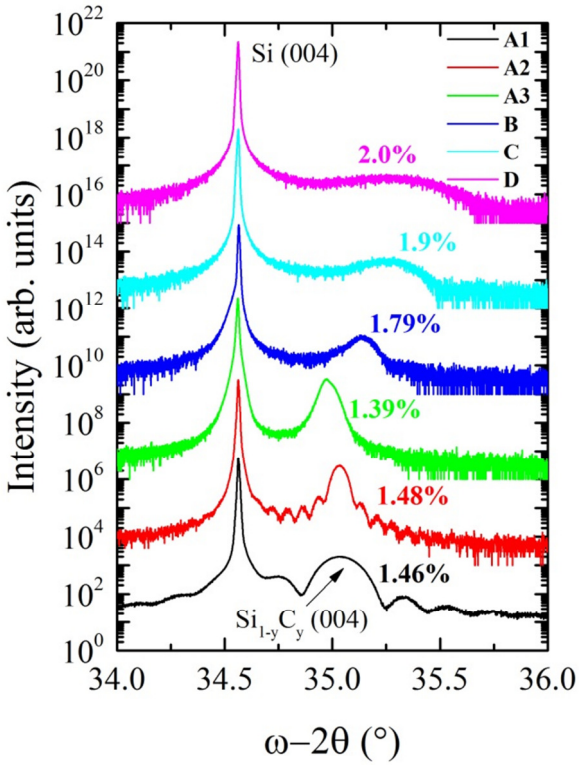

Figure 5.1 HR-XRD coupled scans of $Si_{1-y}C_y$/Si (001) heterostructures showing the 004 Bragg peaks.

Samples A1, A2 and A3 show peaks at approximately the same scattering angle, indicating a similar C composition. Thickness fringes can be observed for samples A1 and A2, by mapping the positions of these fringes it is possible to extract thicknesses of

26.5 ± 0.4 nm and 76 ± 4 nm for the epilayers respectively. It is not possible to observe thickness fringes on samples A3, B, C and D as either the epilayers are too thick or, in the case of the higher C content layers, the quality has degraded. Progressing from sample A to D, there is an increase in scattering angle of the $Si_{1-y}C_y$ Bragg peak that demonstrates an increase in substitutional C composition. However, the dramatic increase in Full Width Half Maximum of the peaks and decrease in overall intensity gives strong evidence that the crystal quality has degraded significantly as the TMS flow rate has been increased through this series of samples.

Assuming the samples are fully strained to the Si lattice, the relaxed lattice constant of the $Si_{1-y}C_y$ (a_{rel}) can be calculated from coupled scans using

$$a_{rel} = (a_{\perp} - a_{||})\left(1 + 2\frac{C_{12}(y)}{C_{11}(y)}\right)^{-1} + a_{||} \qquad \text{Equation 5.1}$$

where $a_{\perp}$ and $a_{||}$ are the perpendicular and parallel $Si_{1-y}C_y$ lattice constants respectively. $C_{12}(y)$ and $C_{11}(y)$ are the stiffness constants for $Si_{1-y}C_y$ and were calculated using a linear interpolation between the constants for Si and 3C-SiC. The value of $a_{\perp}$ can be extracted from the position of the (004) Bragg peaks in Figure 5.1 using

$$a_{\perp} = \frac{2\lambda}{\sin(\omega - 2\theta)} \qquad \text{Equation 5.2}$$

where λ is the wavelength of the incident X-rays (1.54056 Å), and $a_{||}$ is equal to the Si lattice constant only when the epilayer is fully strained and not tilted. A conservative estimate of the substitutional C composition of the samples can then be determined using a modified Vegard's Law [107]

$a_{rel} = a_{Si} - 2.439y + 0.5705y^2$ Equation 5.3

the values of which are shown in Figure 5.1.

The assumptions made when relying solely on coupled ω-2θ scans can lead to incorrect values of C content. To be more precise with calculations it is possible to extract both the in-plane and out-of-plane lattice parameters from tilt corrected asymmetric RSMs. Symmetric (004) RSMs were taken for $Si_{1-y}C_y$/Si samples in order to determine the tilt of the epilayers and correct the positions of the Bragg peaks in asymmetric (224) RSMs, see Figure 5.2.

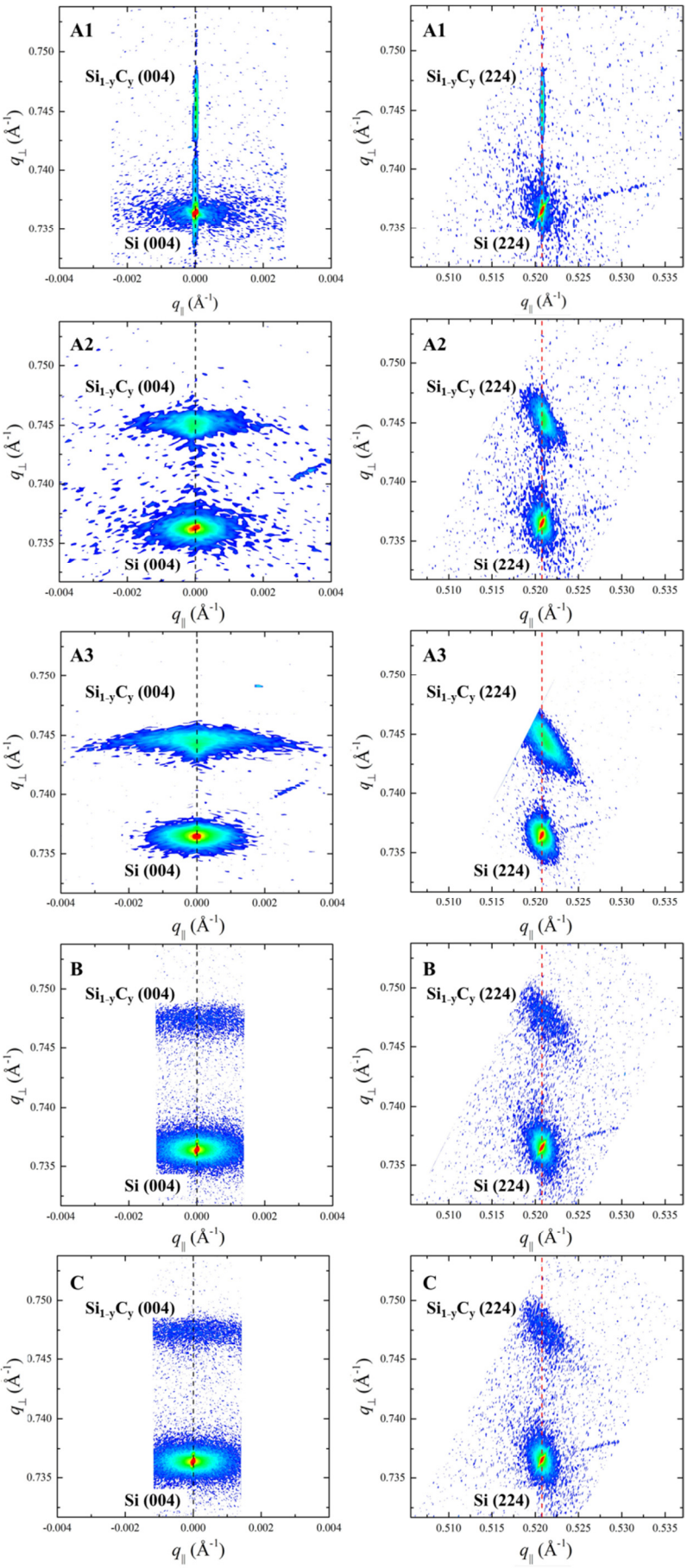

Figure 5.2 Symmetric (left) and asymmetric (right) RSMs for $Si_{1-y}C_y$ heterostructure samples.

The RSMs show that while sample A1 has a very narrow and well defined peak in $q_{\perp}$, the Bragg peaks of samples A2 and A3 increase their spread in-plane for the (004) RSM which is caused by a broadening of the Bragg peak in ω and implies an increase in mosaicity of the thicker samples. While the peaks can be seen for samples B and C, they are very weak and difficult to resolve as the crystal quality is too poor by the increase in C content in the lattice. The strain state and C content of each of the layers was extracted from the RSMs again using Vegard's Law (although this time calculating a_{rel} from the measured lattice parameters), the values of which are later shown in Table 5.2.

X-TEM images were acquired using a JEOL JEM-2000FX TEM operating at 200 kV in order to assess the crystal structure of the as-grown $Si_{1-y}C_y$ epilayers and how the quality varies with increasing C content and thickness, see Figure 5.3. These images highlight the issues involved with the growth of thicker and higher C content $Si_{1-y}C_y$ epilayers. Below the layers' surface, amorphous regions can be observed that protrude through the epilayers of samples A2 and A3 to form hillocks on the surface. These amorphous regions begin to form at various points throughout the epilayers, suggesting that the formation of these regions is not linked to chamber contamination or discreet changes in growth conditions. The origin of these amorphous regions is clearly linked to the TMS flow rate and hence the incorporated substitutional C. A far higher density of defects can be seen in sample B, C and subsequently sample D, than in samples A2 and A3. As such, we hypothesise that these defects are formed from adatoms that have insufficient energy to diffuse into proper lattice sites; instead they form clusters upon which there is accelerated amorphous growth that results in the aforementioned hillocks. The increase in C content increases the strain in the epilayers, which will affect the surface energy and hence increase the likelihood of point defects forming.

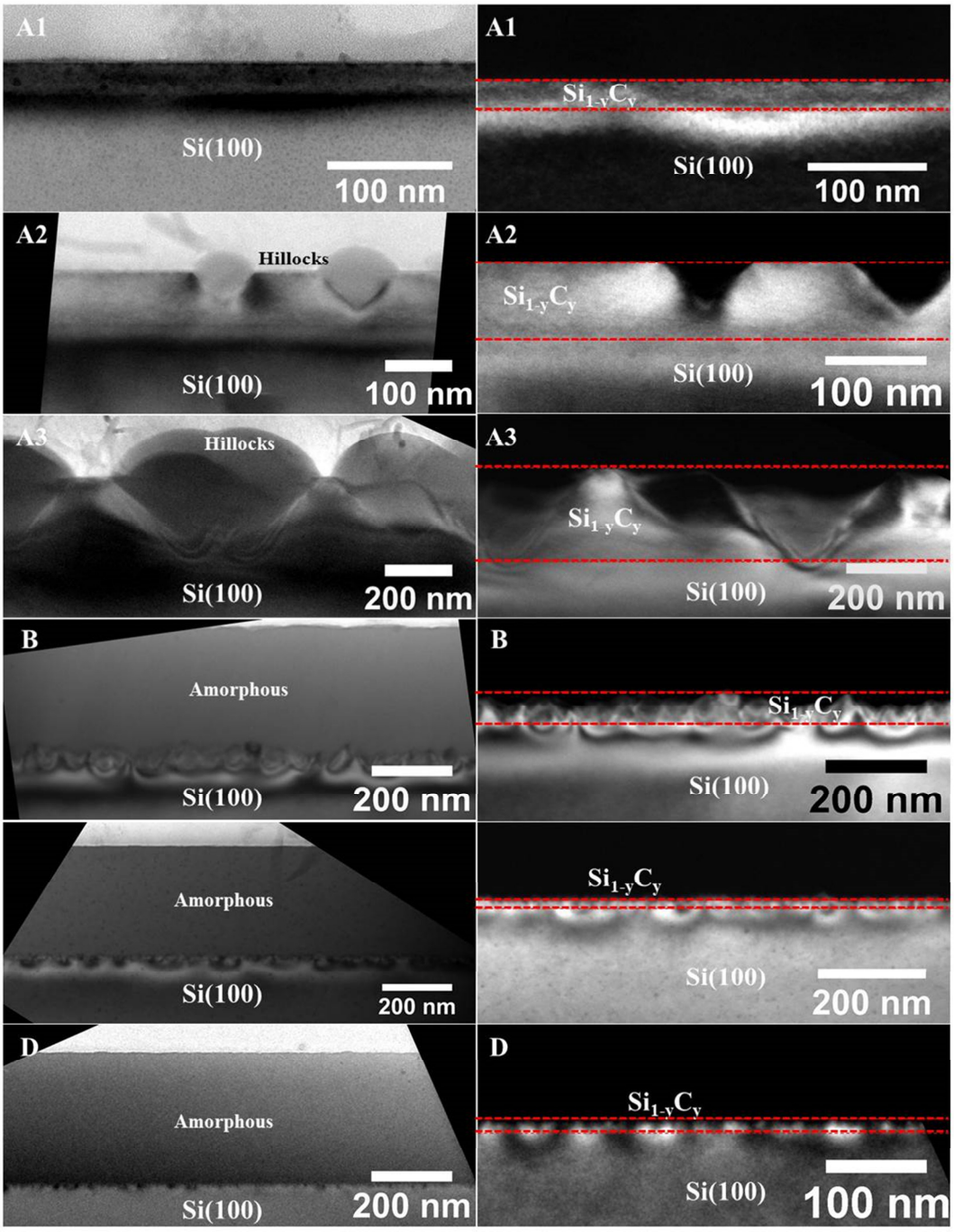

Figure 5.3 BF (left) and (004) DF (right) X-TEM images of samples A-D. Dashed red lines indicate the transitions between Si (001) and crystalline and amorphous $Si_{1-y}C_y$. Hillocks can be seen forming on the surface of the crystalline $Si_{1-y}C_y$ layers emanating from point defects within the epilayers in samples A2-D. Neither the hillocks nor the underlying growth show the same crystallinity as the $Si_{1-y}C_y$ epilayers, as indicated by the dark field images. The density of hillocks is seen to increase with layer thickness and more significantly with C composition. Large variations of strain can be observed in the higher C content epilayers which may be a contributing factor to the presence of growth defects.

Another important feature to note in the X-TEM images is the presence of an amorphous region atop the $Si_{1-y}C_y$ epilayer in samples B, C and D. We attribute this layer to fusion of the hillocks that produce a purely amorphous capping region. It can be observed that there is a critical thickness of $Si_{1-y}C_y$ that can be grown before these hillocks fuse to form a complete amorphous layer and that this critical thickness decreases with increasing C content. A similar effect to this has been observed before in low temperature Si growth by MBE [144]. The crystallinity of the $Si_{1-y}C_y$ and hillocks is verified by the selected area electron diffraction (SAED) patterns shown in Figure 5.4.

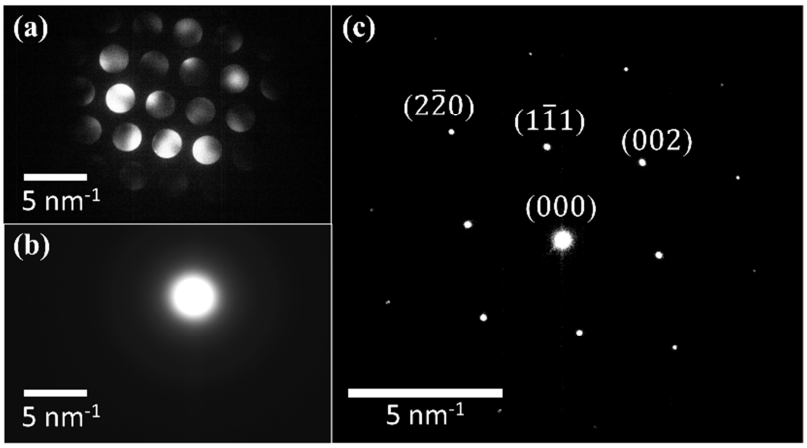

Figure 5.4 Electron diffraction patterns for (a) the $Si_{1-y}C_y$ epilayer, (b) a hillock and (c) the entire $Si_{1-y}C_y$/Si (001) heterostructure for sample A2 (1.48%) acquired from X-TEM. The diffraction pattern for the hillock shows only the straight through beam with ring patterns around it confirming the feature is amorphous. As the C content in the $Si_{1-y}C_y$ is low and the epilayer is almost fully strained to the Si substrate it is almost impossible to distinguish diffraction peaks between the two layers.

It is interesting to note that sample A1 (1.46%) does not show any significant hillock formation, this is because the epilayer grown in sample A1 is thin enough to avoid the clustering of C during growth. A high resolution X-TEM image of sample A1 was performed using a JEOL 2100 TEM again operating at 200 kV and shows that the $Si_{1-y}C_y$ epilayer is perfectly strained to the underlying Si substrate, see Figure 5.5.

The same high resolution TEM was used to image the lattice structure of a hillock formation on sample A2 and is shown in Figure 5.6. The image again confirms the lack of crystallinity in the structure, instead showing that the hillock is amorphous making it difficult to distinguish from the glue on the surface of the $Si_{1-y}C_y$ epilayer.

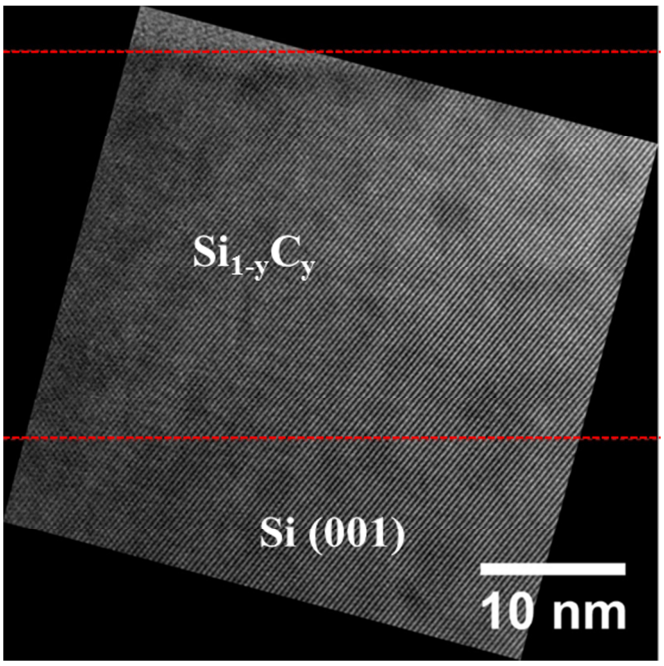

Figure 5.5 High Resolution straight through X-TEM image of sample A1 showing the crystal planes are perfectly aligned with the underlying Si substrate.

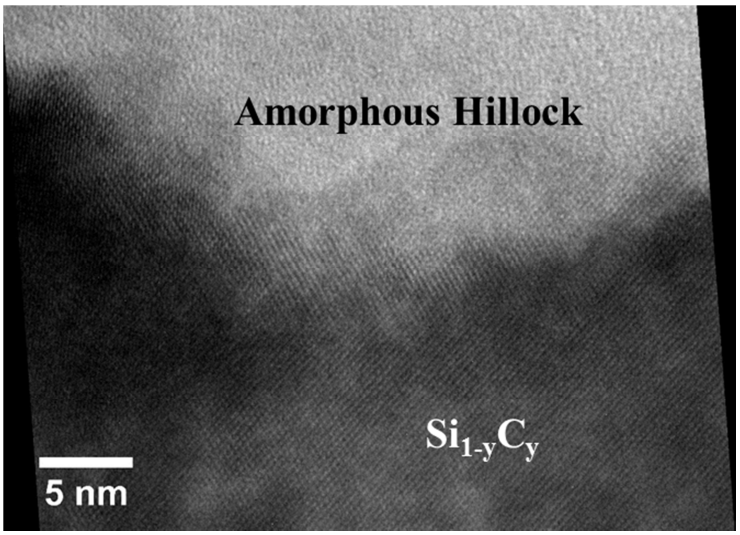

Figure 5.6 High resolution straight through X-TEM micrograph of a hillock formation on sample A2.

5.3.2 Surface Morphology

AFM scans across the surface of each sample yield similar results that give information on the density and morphology of the hillocks as well as the RMS roughness of the overall mapped area. A comparison of the AFM scans of samples A1 (26 nm), A2 (74 nm) and A3 (232 nm), shown in Figure 5.7, shows that the hillocks are larger and

also more closely packed for sample A3 than for sample A2. This is expected as, in the thicker layer, amorphous growth can occur for longer in the direction parallel to the epilayer surface before emanating from the surface to form the hillocks, as seen in Figure 5.3.

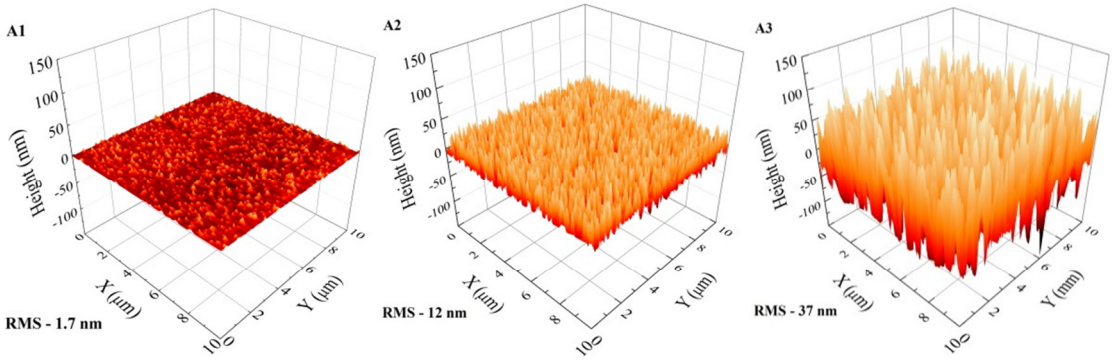

Figure 5.7 AFM scans of range 10 × 10 μm across samples A1, A2 and A3 demonstrating the dramatic increase in surface roughness with increased epilayer thickness.

The formation of hillocks on the surface is more easily observed using SEM, see Figure 5.8. The distribution of the hillocks appears random and there is no obvious clustering of the features on the sample surface. In addition, the size of the spherical hillocks varies across the sample, indicating that the formation of the underlying cause of the features does not occur at a single definable point in the growth process. This eliminates the possibility of contamination in the CVD system affecting the epilayer growth.

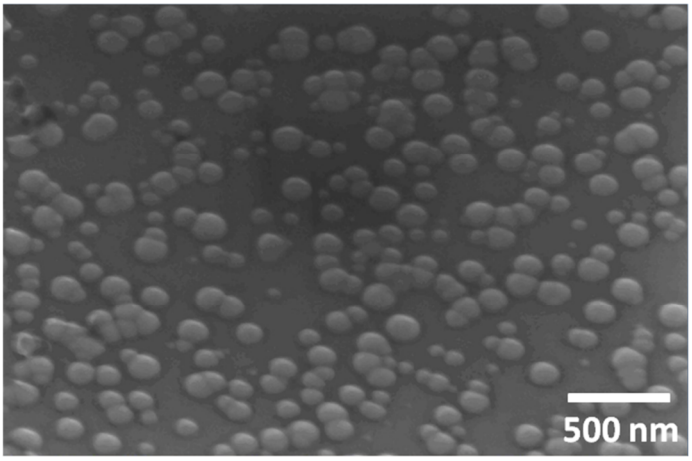

Figure 5.8 Secondary electron SEM image of the surface morphology of sample A2 showing an isotropic distribution of amorphous hillocks.

5.3.3 Summary of Results

The main results of material characterisation carried out on samples A-D are compared in Table 5.2. The first important parameter to observe in the $Si_{1-y}C_y$ epilayer is the atomic concentration of C that has been substitutionally incorporated in the lattice under each set of growth conditions. Samples A1 and A2 show the same C content while the content is slightly reduced in A3, however, this may be due to the increased uncertainty in the position of the Bragg peak in A3 due to the reduced crystal quality, but could also be due to increased interstitial impurities in the structure. The layers with higher TMS flow rates exhibit an increase in incorporated C up to 2.0%. These values do not scale linearly with the TMS flow rate which implies that the deposition process has saturated or that the C atoms are taking interstitial sites in the crystal lattice. It is important to note here that all C compositions were calculated by mapping both the in-plane and out-of-plane lattice parameters through RSM measurements and in each case the $Si_{1-y}C_y$ epilayers were found to be almost fully strained to the Si substrate. The only exception to this is sample D in which it was not possible to acquire sufficient diffraction signals to form an accurate RSM. As such, the C incorporation percentage has been estimated from the coupled scan alone for sample D and we have assumed that the epilayer is again fully strained. If there is significant relaxation in the $Si_{1-y}C_y$ then the C content will be higher than the value shown in Table 5.2.

The surface roughness of the epilayers is another important feature of the $Si_{1-y}C_y$ alloys. While the roughness of the thinner sample A1 is low, the roughness increases with thickness due to the formation of the previously observed amorphous hillocks forming on the crystal surface. When the C content is increased, these formations occur at a significantly increased rate which leads to a fusing of the amorphous hillocks into a smooth capping layer. The relation of the amorphous growth region to the crystalline epilayer is also quantified and with samples B, C and D it can be seen that while the overall layer thickness remains relatively constant, the crystalline region shrinks down to a minimum of ~11 nm, equating to around 3% of the total layer thickness. Finally, the strain in the epilayers shows that as the samples A1, A2 and A3 are grown thicker, the tensile strain of the epilayers with respect to the underlying Si substrate is shown to decrease. This is expected as the $Si_{1-y}C_y$ continues growth beyond its critical thickness it will begin to relax. Samples B and C actually show an increase in tensile strain up to 0.85%. It was not possible to map the strain of sample D again due to the reduced XRD

signal. As the C content is increased, the critical thickness decreases, however, the presence of the amorphous growth features dominates in the disruption of the crystal and the tensile strain of the epilayers continues to increase with C content. This is an important result as the main application for $Si_{1-y}C_y$ is in strain engineering, therefore thin, higher C content epilayers would be more appropriate to these applications as they can induce the maximum strain.

Table 5.2 Important properties of characterised $Si_{1-y}C_y$ epilayers. Both the layer thickness and the thickness of the crystalline region, before epitaxy breaks down, are quoted, as measured from cross sectional TEM.

Sample	A1	A2	A3	B	C	D
C Composition (at.%)	1.46%	1.48%	1.39%	1.79%	1.90%	2.0%*
Surface Roughness (nm)	1.7 ± 0.3	12 ± 2	37 ± 7	1.93 ± 0.05	0.65 ± 0.01	0.54 ± 0.01
Crystalline Thickness (nm)	26 ± 1	74 ± 1	232 ± 2	60 ± 10	16 ± 4	11 ± 4
Total Layer thickness (nm)	26 ± 1	74 ± 1	232 ± 2	360 ± 10	350 ± 10	330 ± 10
In-plane Strain (%)	0.65%	0.63%	0.54%	0.76%	0.85%	-

* Estimated from coupled scans only, assuming epilayers are fully strained

5.4 Higher Temperature Growth

The growth temperature of 550 °C was selected as an appropriate condition for $Si_{1-y}C_y$ growth based on previous published work [139]. However, higher temperature growth can increase growth rates giving C atoms less time to fit into more energetically favourable interstitial sites. A short study in which the optimal growth conditions for $Si_{1-y}C_y$ alloy growth at 550 °C was carried out at a range of temperatures up to 700 °C and epilayers were characterised by HR-XRD coupled scans, see Figure 5.9. The downside of increasing the growth temperature is that C has a tendency to segregate from the lattice during growth, resulting in C precipitation on the surface and as a consequence growth of non-crystalline $Si_{1-y}C_y$ layers. Increasing the growth temperature too high will put the growth process out of non-equilibrium and the incorporation of C in the Si lattice will instead be governed by the solubility limit.

The increase in temperature up to 600 °C shows an increase in the C composition of the epilayer with an observable shift in the peak to the higher angles, however the intensity of the peak drops somewhat and the thickness fringes are no longer visible, indicating

that the quality of the epilayer is poor and that it is no longer fully strained. This increase in C content is similar to effects observed when simply increasing the C flow rate in Figure 5.1. Temperatures beyond 600 °C yielded no discernible $Si_{1-y}C_y$ indicating that the incorporation of C into the Si lattice had been suppressed due to C segregation. The results suggest that while it may be possible to increase the C content of $Si_{1-y}C_y$ epilayers by increasing the growth temperature beyond 550 °C, with the use of disilane and TMS as precursors, it is not possible to grow $Si_{1-y}C_y$ epilayers at temperatures beyond 600 °C.

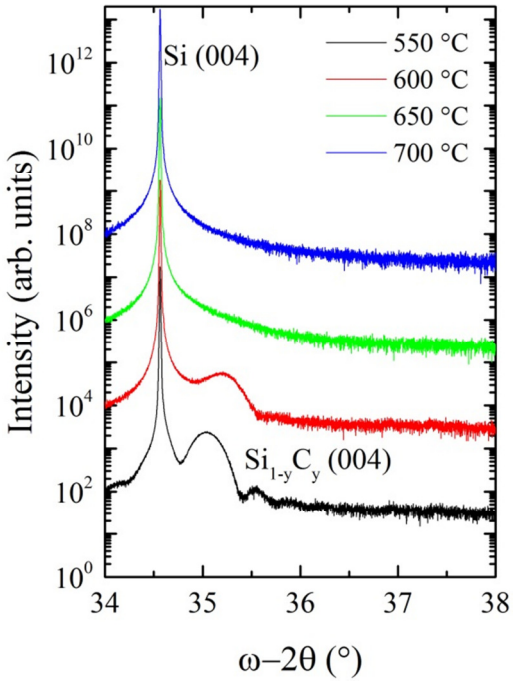

Figure 5.9 HR-XRD coupled scans of $Si_{1-y}C_y$ epilayers grown at different temperatures.

5.5 High Temperature Annealing of $Si_{1-y}C_y$

As discussed previously, carbonising a Si substrate is shown to improve subsequent 3C-SiC epilayer quality and suppress Si out-diffusion from the substrate. The carbonisation process, however, is not without its issues. Many years have been spent optimising the carbonisation process and still, reports in literature are unclear on the best methods of initiating growth. The high temperatures required to form the carbonised layer (>900 °C) can lead to out-diffusion of Si from the substrate, an issue that the buffer layer is supposed to suppress. This can often lead to surface roughening which degrades future 3C-SiC epilayers. The carbonisation process itself is also not suitable for low temperature epitaxial reactors due to the high levels of C deposition and low reactivity

of C based precursors. Instead, it has been proposed that a $Si_{1-y}C_y$ epilayer could act as an appropriate buffer layer for 3C-SiC epitaxy by preventing the out-diffusion of Si from the substrate [145] although the successful growth of high quality 3C-SiC on such an epilayer has not been demonstrated. $Si_{1-y}C_y$ has been shown to precipitate into 3C-SiC at temperature above 900 °C which offers an ideal template for 3C-SiC heteroepitaxy [146]. To investigate the effects of thermal annealing on $Si_{1-y}C_y$ an epilayer was subjected to a 1000 °C anneal under H_2 flow after epitaxy and compared to a reference, unannealed sample. HR-XRD coupled scans show that the $Si_{1-y}C_y$ (004) Bragg peak shifted closer to the Si substrate peak, see Figure 5.10, as reported previously in literature. This is attributed to the out-diffusion of C and precipitation of 3C-SiC, although longer range scans did not show any 3C-SiC Bragg peaks.

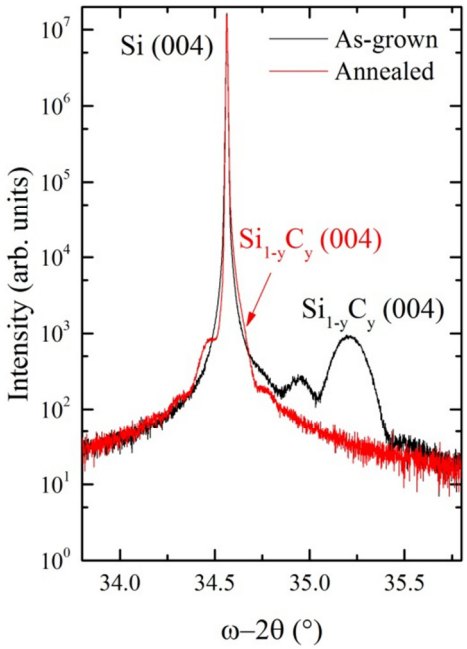

Figure 5.10 HR-XRD coupled scans of $Si_{1-y}C_y$ epilayers as grown and after thermal annealing at 1000 °C under H_2 atmosphere.

X-TEM micrographs show that the $Si_{1-y}C_y$ experienced an obvious change to its crystallinity after annealing, see Figure 5.11. The surface of the epilayer shows a visible change in contrast which could indicate that C has out diffused from the $Si_{1-y}C_y$ epilayer and formed a separate layer. This top layer is shown to be crystalline under dark field diffraction conditions and also shows signs of stacking fault formation which could imply that 3C-SiC precipitates have formed.

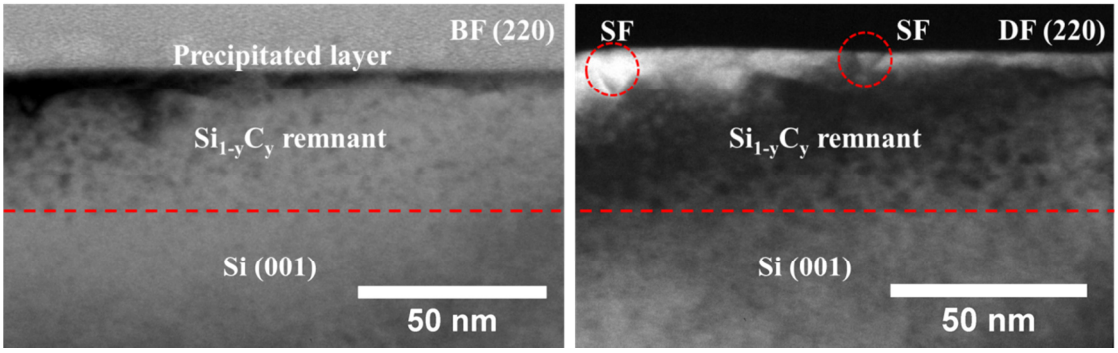

Figure 5.11 BF and DF (220) X-TEM micrographs of annealed $Si_{1-y}C_y$ epilayer.

5.6 Discussions

Trimethylsilane and disilane have been demonstrated as potential low-cost alternative precursors for the growth of $Si_{1-y}C_y$ epilayers on Si using RP-CVD growth process. As traditionally highly reactive precursors such as trisilane have been needed to grow the alloy, the work presented here shows that this is not always necessary, an important step towards incorporating the low-cost growth of $Si_{1-y}C_y$ into the Si industry. However, there are certain drawbacks to using less reactive precursors. The use of disilane and TMS results in a reduced growth rate allowing C atoms to reach interstitial sites, especially when growing higher C composition layers. Amorphous clusters are seen to form within the epilayers, an effect which increases with increasing C content and epilayer thickness.

In addition to deteriorating the crystal quality of the $Si_{1-y}C_y$ epilayers, the amorphous hillocks forming on the surface of the epilayer cause a dramatic increase in surface roughness which will have detrimental effects on device performance. This surface roughness increases with hillock size and density until fusion of the surface defects occurs and a smooth amorphous capping layer forms. The density and size of these hillocks increases with layer thickness, due to C precipitation and as a consequence the higher probability of point defects forming and allowing the accelerated growth to occur for a greater distance within the epilayer. The density of hillocks was also observed to increase greatly with the increase of TMS flow rate, and hence amount of C incorporation. This may be a result of changes in surface energy due to strain in the higher C content $Si_{1-y}C_y$, the higher C content in the precursor mixture simply oversaturating the epilayers, or a combination of both these effects.

$Si_{1-y}C_y$ epilayers have been demonstrated with C contents up to ~2.4% as grown by RP-CVD and over 5% as grown by MBE in literature [111, 139, 140]. The results presented here demonstrate that the low cost and safer precursor combinations TMS and disilane is able to reach 1.5% C content in epilayers below ~30 nm thickness while still maintaining high crystal quality and surface roughness of below 2 nm. The epilayers grown using this method may not be high enough composition to induce significant strain enhancements within MOSFET channels, but are still suitable for a number of commercial applications. C contents of below 1.5% in $Si_{1-y}C_y$ alloys have been demonstrated to reduce Schottky barrier heights [147] and improve the stability of Ni silicides in source-drain contacts [148]. More detailed results and discussions have been published on this piece of research here [149].

While growth of $Si_{1-y}C_y$ at temperature beyond 600 °C resulted in little to no C incorporation, the high temperature annealing of the alloy at 1000 °C under H_2 flow was found to have significant effects on the crystal. The reduction in C content within the $Si_{1-y}C_y$ alloy implies significant out-diffusion of C atoms from the crystal and TEM images show a precipitated layer on the surface of the epilayer. Defects within this layer that resemble stacking faults suggest that small clusters of 3C-SiC may have been formed, although XRD coupled scans did not show any 3C-SiC Bragg peaks. The results indicate that the high temperature annealing of $Si_{1-y}C_y$ alloys may provide an alternative method to initiating the growth of 3C-SiC than the commonly used carbonisation process.

Chapter 6
Low Temperature 3C-SiC Heteroepitaxy

6.1 Introduction

3C-SiC is typically heteroepitaxially grown on Si substrates at very high temperatures, as close to the melting point of Si (~1410 °C) as possible. This is done in order to improve crystal quality and it has been found that growth below temperatures of ~1250 °C leads to severe crystal degradation when using standard precursors such as silane and propane [53]. Growing at lower temperature does offer many advantages, however, such as reducing thermal stresses, decreasing growth costs, permitting the use of SiO_2 selective masks and could allow the growth of 3C-SiC/Si heterostructures within cold-wall CVD reactors, which can typically only operate up to around 1200 °C.

One method of reducing the growth temperature while still achieving high quality is to use a single-source precursor (SSP) containing both Si and C. SSPs typically have much higher reactivity at lower temperature than standard multiple source precursors. A few examples of SSPs include methyltrichlorosilane (CH_3SiCl_3), tetramethylsilane ($Si(CH_3)_4$) or hexamethyldislane ($Si_2(CH_3)_6$). One of the issues when using SSPs is that it is difficult to control the C/Si ratio which is one of the key parameters to high quality growth of 3C-SiC.

The aim of this research was to validate models proposed by Dr M. Myronov to grow monocrystalline 3C-SiC thin films at low temperature within an industrial type cold-wall RP-CVD system, predominantly designed for the growth of Si and $Si_{1-x}Ge_x$ alloys. In recent years, the capabilities of this Si industry standard growth system, situated at the University of Warwick, has been substantially expanded to grow other Si and Ge based alloys including: $Si_{1-x}B_x$, $Si_{1-y}C_y$ and $Ge_{1-x}Sn_x$. Up until now, the growth of

crystalline 3C-SiC in such a cold-wall RP-CVD system has not been achieved. These reactors generally consist of a quartz chamber, limiting the CVD upper growth temperature to ~1200 °C, which makes achieving highly crystalline 3C-SiC a challenge. However, the throughput of these machines and significant reduction of deposition on the chamber walls would allow mass production of low-cost 3C-SiC/Si epi wafers. Over the past 30 years, various attempts have been made to grow 3C-SiC at low temperatures, however, often quality is poor [150] or relies of complicated growth sequences similar to those found in atomic layer deposition (ALD) systems [151] or exotic growth methods such as microwave plasma [152] or hot wire CVD [153].

In this Chapter, the results of in-depth material characterisation of 3C-SiC thin films grown on Si (001) substrates, within a standard cold-wall industrial type RP-CVD system, are presented. Once high quality, mono-crystalline 3C-SiC epilayers were achieved, dopants were introduced into the layers and preliminary work on selective epitaxy was also carried out.

6.2 Epitaxial Growth

The epitaxial growth of 3C-SiC was performed within an industrial type ASM Epsilon 2000 RP-CVD system. Following on from the knowledge and experience gained during the growth of $Si_{1-y}C_y$ alloys in Chapter 5, a methylated silane such as TMS or MMS presented as the most obvious choice of precursor for 3C-SiC growth due their low-cost and high reactivity. TMS has only been utilised as a precursor for 3C-SiC growth a few times in literature [154, 155]. Madapura *et al.* claimed the first growth of 3C-SiC with TMS in 1999 by growing films at low pressure (3.2 Torr) in a rapid thermal CVD system. They achieved very high growth rates of 30 μm/hr. and XRD results showed the layers had some crystallinity, although the authors failed to note whether the material was mono or polycrystalline. In addition, the SEM images showed that the carbonisation process was unable to prevent the formation of voids at the interface [156]. Similar results have been achieved using MMS, however, growth using this precursor often leads to polycrystalline epilayers and void formation is again an issue [157, 158]. A range of Si precursors including silane (SiH_4), disilane (Si_2H_6), dichlorosilane (SiH_2Cl_2), trichlorosilane (SiHCl3) and trisilane (Si_3H_8) could act as a highly efficient Si source as all are very reactive at growth temperatures between 1100-1200 °C. Dichlorosilane was selected as the precursor of choice for this study as the

chlorine species in the gas phase will help prevent Si nucleation and limit chamber depositions. A similar effect could have been achieved using a silane and HCl, however, this adds an additional parameter for epitaxial growth. All of the following 3C-SiC epitaxy was carried out using TMS as the C source precursor.

6.3 Initial Growth Trials

Initial 3C-SiC growth experiments were carried out using a C/Si ratio of 1, attempting to achieve stoichiometry in the reaction system. This was achieved by controlling the Si and C source precursor flow rates, which were flowed in a carrier gas of H_2. The growth of 3C-SiC was performed on a $Si_{1-y}C_y$ buffer layer to help prevent the out-diffusion of Si and improve material quality, see Figure 6.1. The 3C-SiC growth was carried out at a temperature of approximately 1200 °C within the ASM Epsilon 2000 RP-CVD at reduced pressure (~100 Torr). The growth was performed on 100 mm Si (001) substrates that were of standard 525 µm thickness and on-axis. The growth details are shown in more detail in Figure 6.2 and described in more detail here [159].

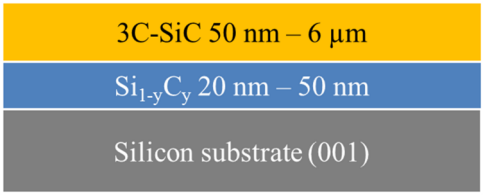

Figure 6.1 Cross sectional schematic of the 3C-SiC epilayer grown on Si (001) with a $Si_{1-y}C_y$ buffer layer.

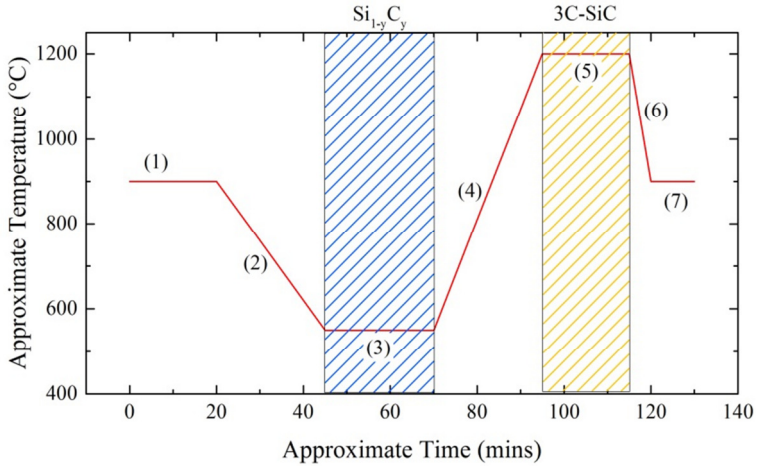

Figure 6.2 Growth process of 3C-SiC/$Si_{1-y}C_y$/Si. (1) – Si wafer is loaded at 900 °C and subjected to a H_2 bake to remove any native oxide on the Si surface, (2) – Temperature reduced to ~550 °C, (3) – $Si_{1-y}C_y$ buffer layer grown, (4) – Temperature ramped up to ~1200 °C, (5) – 3C-SiC growth, (6) temperature dropped back to 900 °C for unloading (7).

Cross sectional and surface SEM images of the as-grown epilayer film can be seen in Figure 6.3 and Figure 6.4 respectively. The thin film is measured to be approximately 10 μm thick giving a growth rate exceeding 50 μm/hr. This growth rate remained unchanged with increasing flow rate of precursors, implying the precursors were not being fully depleted during the growth process. It is interesting to note that no Si out-diffusion was observed during the growth of the film as no voids are present at the interface. This may be due to the buffer layer preventing out-diffusion, but could also be explained by the fact that the film quality is poor and hence crystal growth has not occurred across the entirety of the film. The surface of the film is extremely rough (~ ±1 μm) and cannot be measured using AFM techniques. The surface appears to be dominated by clusters of amorphous growth.

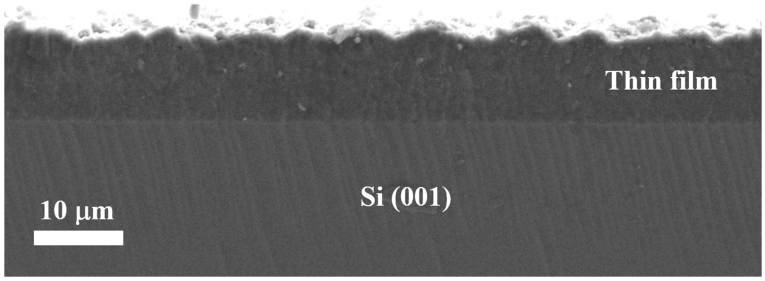

Figure 6.3 Secondary electron SEM image of the as-grown 3C-SiC/Si heterostructure cleaved cross section.

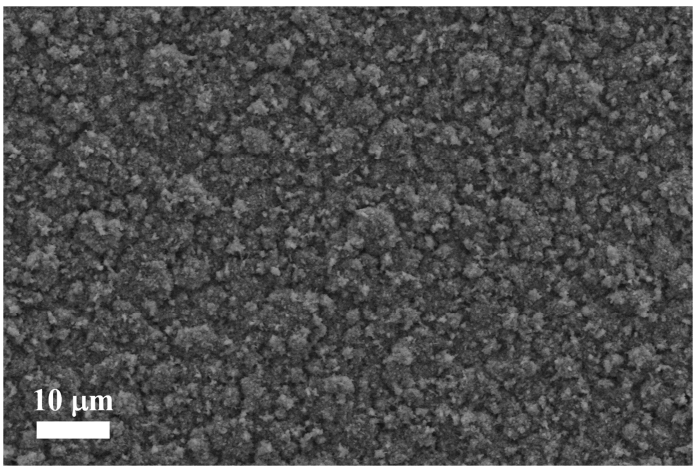

Figure 6.4 Secondary electron SEM image of the surface of the as-grown 3C-SiC/Si heterostructure.

HR-XRD coupled scans were performed on the samples and again no change was observed between growth conditions. The coupled scan for one of the samples can be seen in Figure 6.5. The presence of peaks at the expected angles for 3C-SiC (111), (220)

and (311) indicates that the layer has at least some polycrystalline components, although the intensity of the peaks would imply that the majority of the thin film is non-crystalline. In order to collect signal from the XRD peaks the counting time for the coupled scan was set ~10 times longer than usual, which led to the measurement of strong XRD signals from the Al stage of the diffractometer. These peaks were masked to avoid confusion leading to breaks in the data.

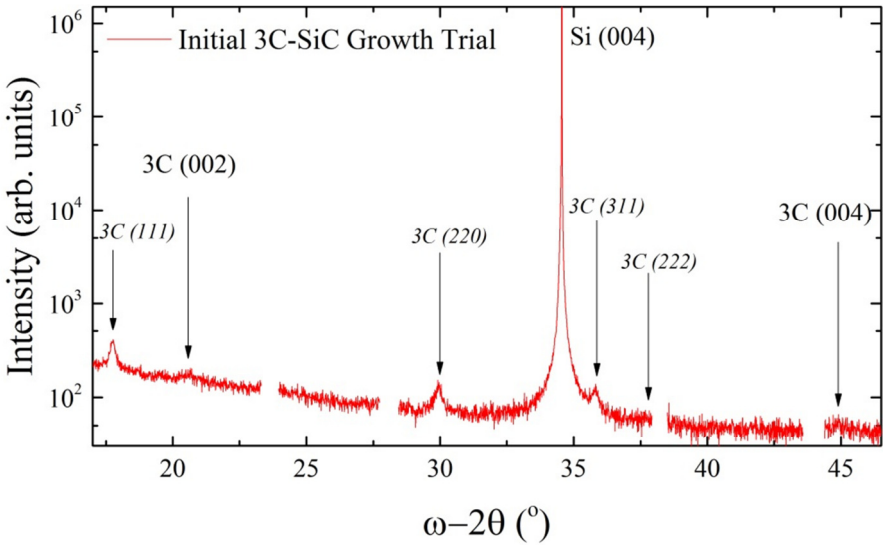

Figure 6.5 HR-XRD coupled scan of the as-grown 3C-SiC/Si heterostructure grown at C/Si ratio of 1. The plot shows peaks associated with various crystal planes within 3C-SiC. Due to the high counting time required to acquire the image, peaks from the Al stage were observed and have been masked from the data set.

Due to the thickness of the epilayer film, standard grinding and polishing of the 3C-SiC/Si heterostructure was not possible for TEM sample preparation. Instead an FIB-SEM lift-out was performed on the sample and imaged within a Jeol 2000FX TEM system, see Figure 6.6. The Dark field TEM images show signs of crystallinity is a predominantly polycrystalline/amorphous film, corroborating the results from the HR-XRD. The crystallinity does not appear to improve as the thickness of the film increases. Although the contrast is weak, it is possible to observe the remnant of the $Si_{1-y}C_y$ buffer layer at the interface of the film and Si substrate and a dark band can be seen at the base of the 3C-SiC film, which is believed to be from the out-diffused C from the $Si_{1-y}C_y$ buffer layer during the ramp up to growth temperature. Although the TEM micrographs are taken over a much smaller area than the SEM images, again no void formation can be seen at the interface.

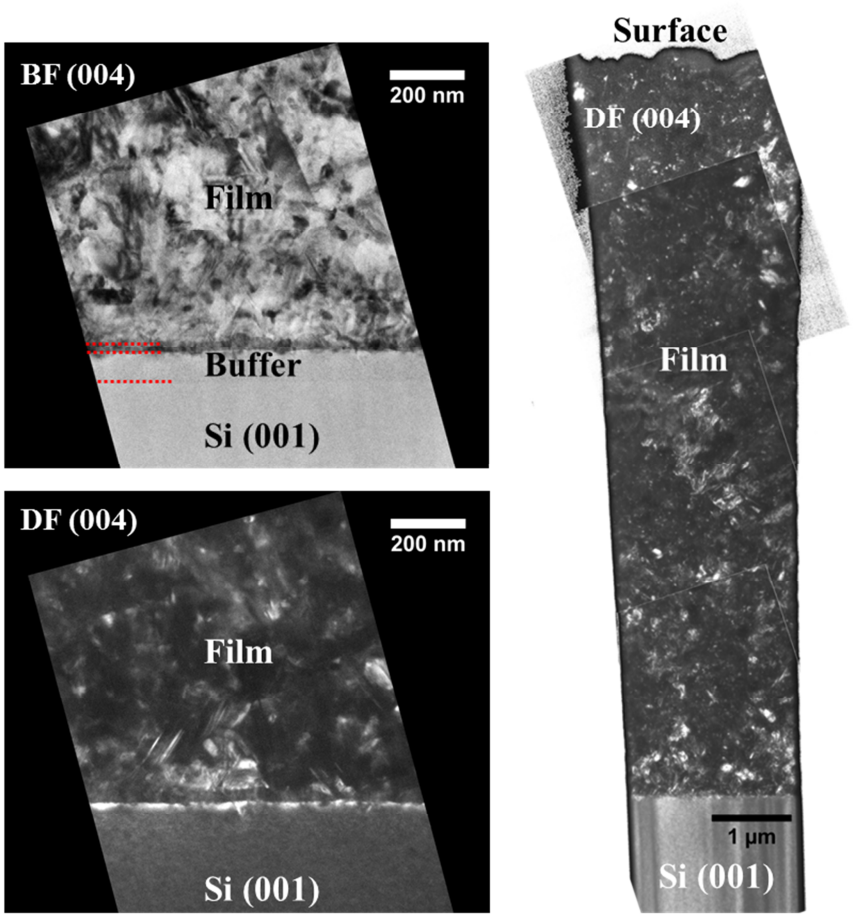

Figure 6.6 X-TEM images taken from the 3C-SiC/Si heterostructure after FIB-SEM lift-out. On the BF (004) micrograph it is possible to make out the remnant from the $Si_{1-y}C_y$ epilayer and a dark band at the interface between the thin film and the substrate believed to be the out-diffused C from the buffer layer.

While it is possible to observe Bragg peaks from specific crystal planes in the 3C-SiC, which may imply that the material is crystalline, more in-depth material characterisation with X-TEM has revealed that the material is predominantly amorphous with only small regions of crystallinity throughout the film. The conclusion drawn from these initial trials is that 3C-SiC growth may indeed be possible using this combination of precursors within the growth system although significant process optimisation is still required. One immediate modification to the process would be to reduce the growth rate as 50 µm/hr is almost unprecedented for 3C-SiC epitaxy and may be affecting the growth process. Typically, lower growth rates produce higher quality films during epitaxy as it allows adatoms more time to reach suitable atomic sits in the lattice. Another important factor here is the C/Si ratio which was fixed at a value of 1, research

published in literature describes a wide range of optimal ratios for 3C-SiC epitaxy which a highly dependent on the growth system and precursors.

6.4 C/Si Ratio Dependence on 3C-SiC/Si (001) Growth

As part of the optimisation process, the growth conditions such as the gas flow rates were manipulated to reduce the growth rate which also showed to improve material properties. A study was then carried out to optimise the quality of the as-grown 3C-SiC epilayers on Si (001) substrates by manipulating the C/Si ratio with the flow rates of the C and Si precursors. The quality of the material was quantified through the full width at half maximum (FWHM) of the 3C-SiC (002) Bragg reflection, taken from coupled ω-2θ scans and the RMS roughness from 20 μm × 20 μm tapping mode AFM scans.

The C/Si ratio was varied from approximately 0.75 to 1.7 and the growth times were reduced to reduce the film thickness, making routine TEM sample preparation more feasible. The flow rate of dichlorosilane was maintained at 30 sccm for all growth runs while the C/Si was manipulated by adjusting the flow rate of TMS into the CVD. For these growth tests, the $Si_{1-y}C_y$ buffer was removed from the process in order to assess the formation of voids at the 3C-SiC/Si interface. The typical growth rate of the 3C-SiC films was found to be around 10 μm/hr and found to produce far higher quality material than previously shown in section 6.3. Selected HR-XRD coupled scans and AFM surface maps are shown in Figure 6.7. A significant dependence on the C/Si ratio was found for the 3C-SiC growth, however, unlike with the previous growth study at higher growth rates, no polycrystalline growth was observed in the 3C-SiC thin films. Low C/Si ratio growth, down to 0.75, showed no 3C-SiC Bragg peaks while high ratios showed broader and reduced intensity peaks, however, no peaks associated with other Bragg reflections in the 3C-SiC were observed, even at a ratio of 1.5. It is possible the C/Si ratio was not high or low enough to promote polycrystalline growth, but it is more likely that the lack of polycrystallinity is due to the reduced growth rate of the 3C-SiC films.

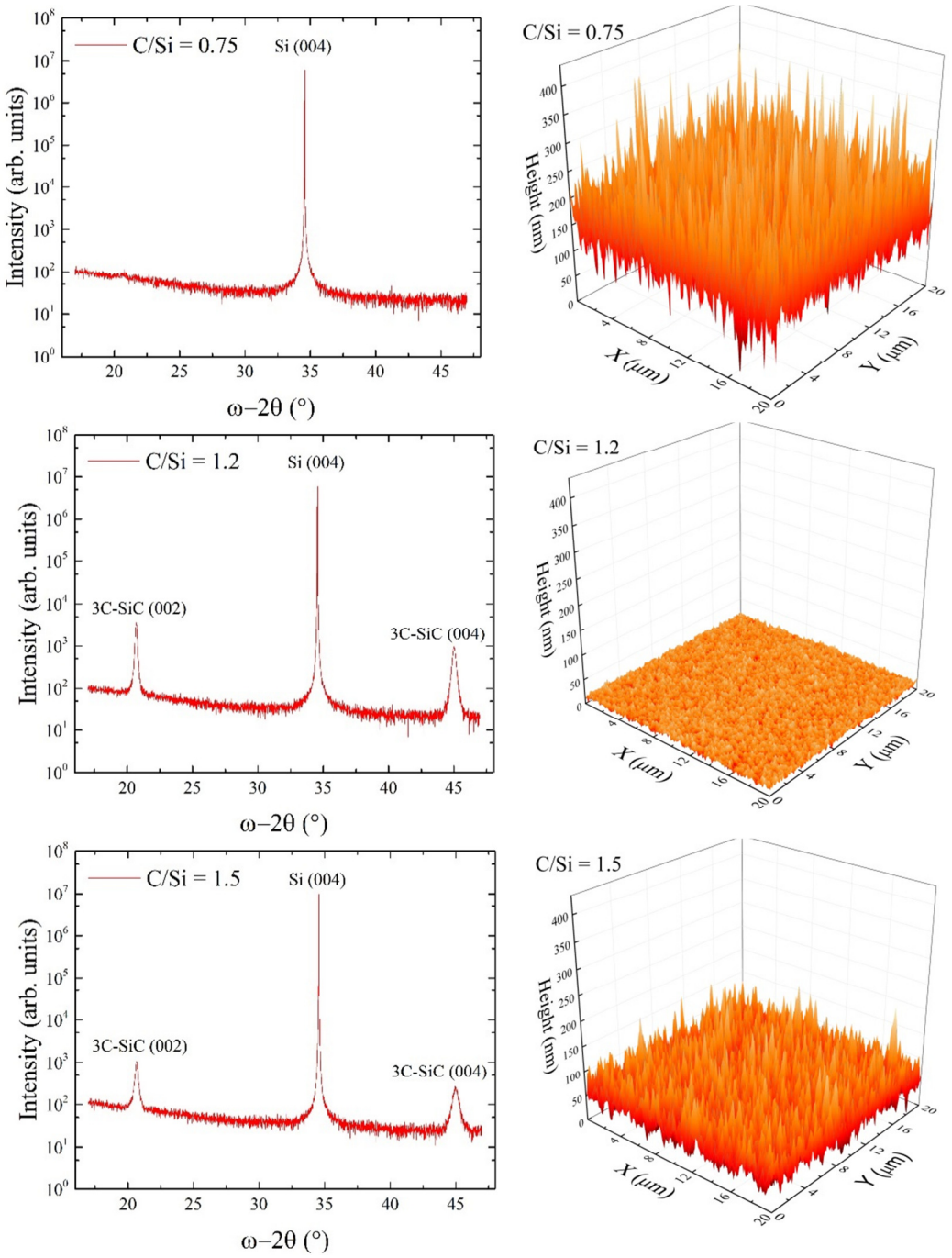

Figure 6.7 Selected HR-XRD ω-2θ coupled scans (left) and 20 × 20 μm AFM surface roughness scans (right) for 3C-SiC epilayers grown using different C/Si ratios. The approximate thickness of the 3C-SiC is 250 nm in each epilayer.

Cross sectional TEM was carried out on the samples grown at different C/Si ratios to better understand the crystallinity and morphology of the 3C-SiC/Si (001) heterostructures, see Figure 6.8. When growing at high (~1.5) and low (0.75) C/Si ratios the crystal quality is poor. In both cases the initial growth, of the first 10's nm, appears crystalline, however, epitaxial growth soon breaks down and amorphous material is

grown with extremely high surface roughness. It is interesting to note that in the case with high C/Si ratio, voids can occasionally be seen at the interface between Si and 3C-SiC where Si has out diffused during growth, possibly due to the lack of $Si_{1-y}C_y$ buffer at the interface. This implies that the C/Si ratio is an extremely important factor when it comes to suppressing void formation in 3C-SiC epitaxy. This is also an important result which explains how Bragg diffraction is observable in the higher C/Si ratio samples (see Figure 6.7) as the ratio is reduced by the addition of Si from the substrate. There is no method to balance C/Si ratio when the growth system ratio is too low, thus the XRD signal is weak or fully suppressed.

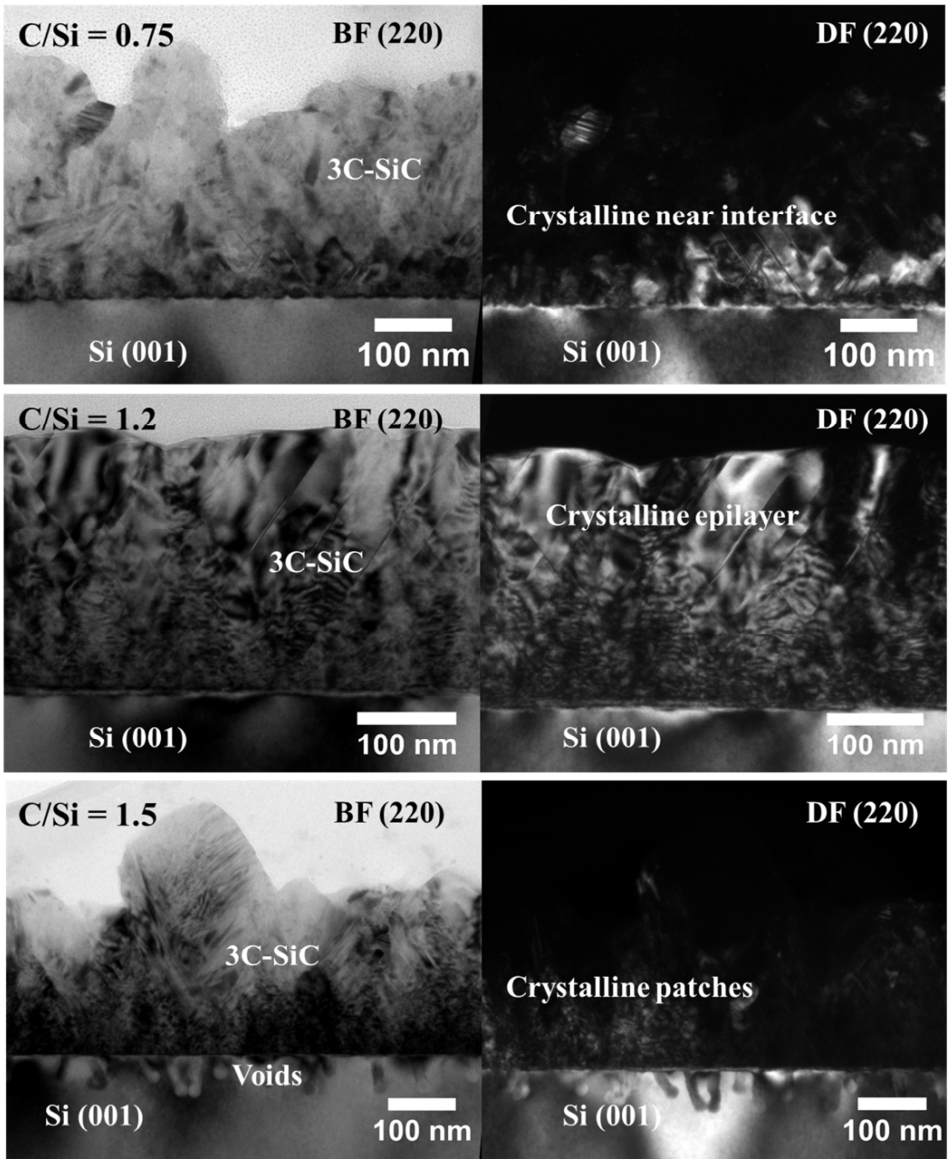

Figure 6.8 X-TEM micrographs of selected samples grown at different C/Si ratios. In each case a BF and DF TEM image was captures under the (220) diffraction condition to highlight crystallinity in the 3C-SiC films.

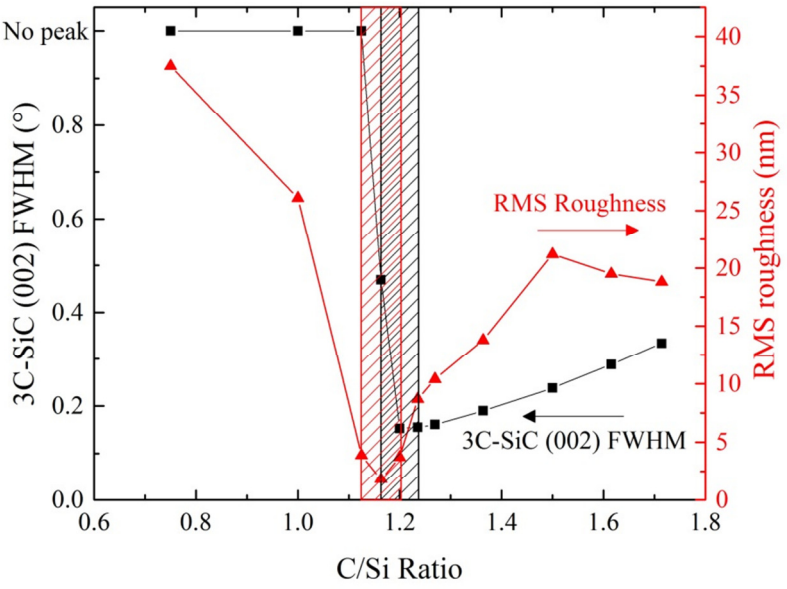

Figure 6.9 Surface roughness and crystalline quality, as determined by the 3C-SiC (002) Bragg reflection FWHM, dependency on C/Si ratio during growth of 3C-SiC. The growth rate was 10 μm/hr. The optimal regions for surface roughness and crystalline quality are highlighted.

The data plotted in Figure 6.9 clearly show a significant dependence for C/Si ratio on both the surface roughness and crystal quality of the grown 3C-SiC epilayers. Similar results have been shown by Chassagne et al. [59] who were able to give an explanation of the different effects observed.

Figure 6.9 can be split into three different sections when it comes to how surface roughness and crystallinity depend on the C/Si ratio:

- C/Si < 1.2 – The lack of C in the reactor means the concentration of C is below the equilibrium partial pressure but can still partly react to form SiC, leading to unstable growth. It has been proposed that the excess Si in this region, leads to the formation of Si aggregates which later carbonise into SiC creating additional SiC/Si interfaces which in turn result in more growth defects reducing crystallinity.
- C/Si >1.2 – When there is an excess of C in the growth system it can be observed that the surface roughness increases, however, the crystallinity of the layer remains relatively constant and only a gradual increase in the (002) FWHM can be observed. This can be explained by the effect of homogeneous nucleation of C atoms leading to surface roughening. However, unlike with the case of excess Si, the sticking coefficient of C adatoms to a C terminated surface

is very low [160] therefore the predominant structure formed with excess C is still SiC.

- C/Si = 1.2 – In the particular case of this CVD reactor and its growth conditions, the optimal C/Si ratio is approximately 1.2, leading to a balance between high crystal quality and low surface roughness. This ratio was also found to prevent the formation of voids at the 3C-SiC/Si interface.

This plot is extremely useful for the calibration of 3C-SiC growth within a CVD reactor and can give an indication of whether the C/Si ratio is too high or low by measuring the crystal quality and surface roughness of an epilayer. However, it must be stressed that these plots are only for a specific growth rate, set of precursors and even reactor and full independent calibration must be carried out if this process is to be carried out on a new deposition tool.

The $Si_{1-y}C_y$ interface layer was found to inhibit void formation at high C/Si ratio growth, however, upon removal it was found to be less essential to the growth of high quality 3C-SiC, which instead relies heavily on growing at the optimal C/Si ratio. The growth of 3C-SiC without a $Si_{1-y}C_y$ buffer layer at a ratio of 1.2 was found to produce highly crystalline 3C-SiC with no void formation indicating the suppression of voids can be achieved through fine control of the precursor flow rates alone. Consequently, the $Si_{1-y}C_y$ buffer layer was removed from the epitaxial process as it simplified growth and had no additional benefits, assuming the optimal C/Si ratio was maintained.

6.5 Optimised 3C-SiC/Si (001) Characterisation

Once an optimal growth process was determined from analysing the effect of the C/Si ratio on the growth of 3C-SiC thin films, further material and electrical characterisation was carried out.

6.5.1 Thickness Uniformity

As 3C-SiC is a wide bandgap semiconductor and consequently semi-transparent to visible light, the apparent colour of the 3C-SiC film depends on the layer thickness due to the interference of light, see Figure 6.10. It is therefore possible to visually analyse the variation of thickness across grown 3C-SiC epi wafers. This can be controlled through proper tuning of the RP-CVD temperature variation and gas flow across the Si substrate during growth.

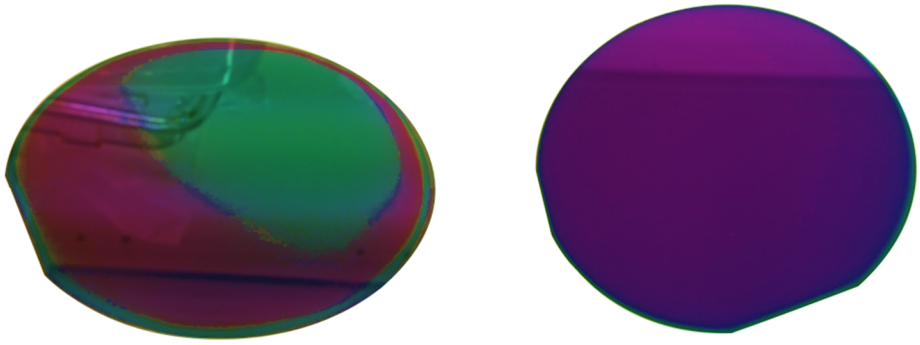

Figure 6.10 Photographs of two 100 mm 3C-SiC/Si (001) epi wafers. The one of the left shows a clear colour change across the wafer due to poor thickness uniformity (>3%), the wafer on the right is a single colour across the wafer indicating excellent thickness uniformity (~1% or less).

In order to determine the exact uniformity of the 3C-SiC epilayer thickness, the as-grown 3C-SiC/Si epi wafers were analysed using FTIR mapping. The FTIR reflectance spectrum of a ~1 µm thick 3C-SiC/Si heterostructure is shown in Figure 6.11 and shows the characteristic TO phonon peak, typically found at 790 cm^{-1}. In thick 3C-SiC epilayers the LO phonon peak (~970 cm^{-1}) is often also observable, however, these two peaks tend to amalgamate into a single broad peak due to the Reststrahlen effect in which high reflectivity is observed between the two phonon peaks due to resonance between phonons and lattice vibrations [161]. The thickness fringes are observed by the interference of light paths within the 3C-SiC as given by Equation 3.1.

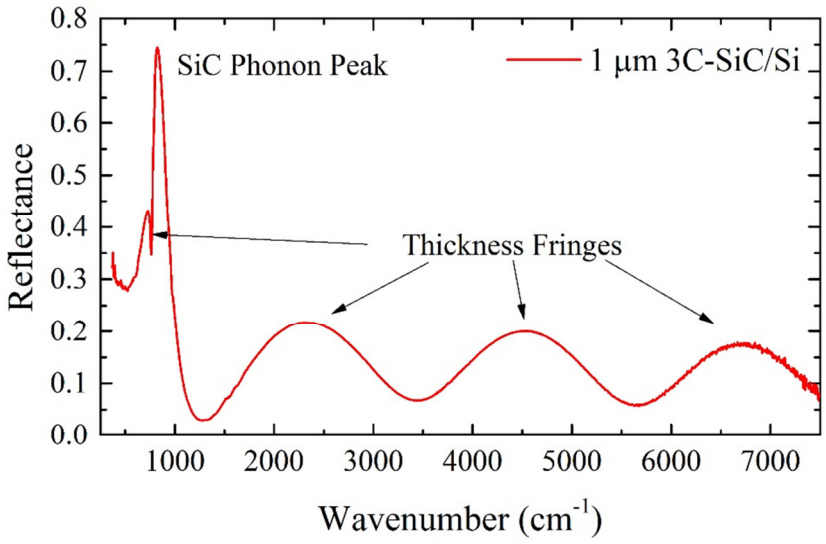

Figure 6.11 FTIR reflectance spectrum of a 3C-SiC/Si heterostructure showing the characteristic phonon peak at ~800 cm^{-1} and additional fringes from light interference.

The range of the FTIR spectra that can be acquired allows 3C-SiC epilayers of thickness down to ~300 nm to be mapped, although thicker layers exhibiting more fringes offer more accurate thickness measurements. By modelling to the reflectance data at various points across a 3C-SiC/Si epi wafer it is possible to map the thickness uniformity. By manipulating the gas and temperature distribution within the RP-CVD system it is possible to achieve 3C-SiC epilayer thickness uniformity of below 2% over 90% of the wafer and is comparable with Si epilayer uniformity in industry, see Figure 6.12. This is an important factor for commercial applications as a uniform epilayer offers a much higher yield of devices across the entire wafer.

FTIR thickness uniformity measurements are only accurate if there are sufficient thickness fringes to model to. Therefore, for the wavenumber range available on a typical FTIR system the fitting becomes subject to large uncertainties when the 3C-SiC epilayer thickness drops below ~300 nm. To overcome this, a UV source can be added to the FTIR system which dramatically increases the measurable range or other techniques such as ellipsometry can be used.

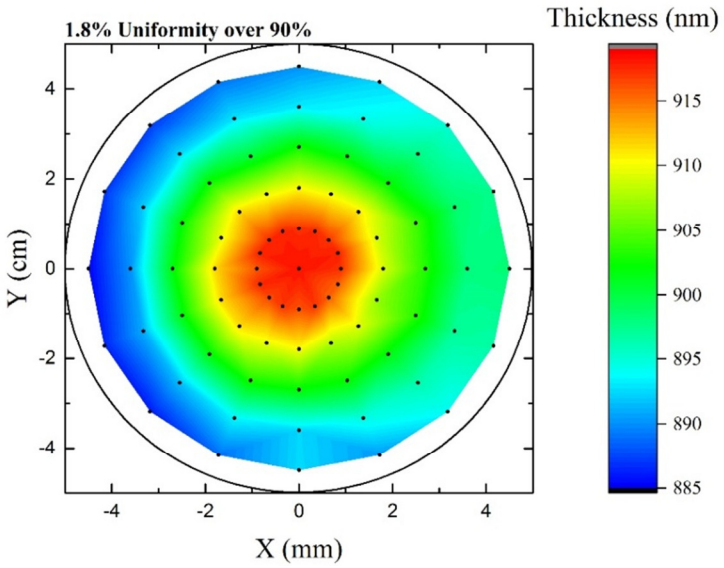

Figure 6.12 Thickness uniformity map of the 3C-SiC epilayer over 90% of a 100 mm 3C-SiC/Si epi wafer.

6.5.2 Thermally Induced Wafer Bow

The wafer bow across different thickness 3C-SiC/Si epi wafers grown at low temperature was measured using a stylus profilometer and compared to the wafer bow of the reference 3C-SiC/Si epi wafer grown at high temperature shown in Figure 4.7, see Figure 6.13.

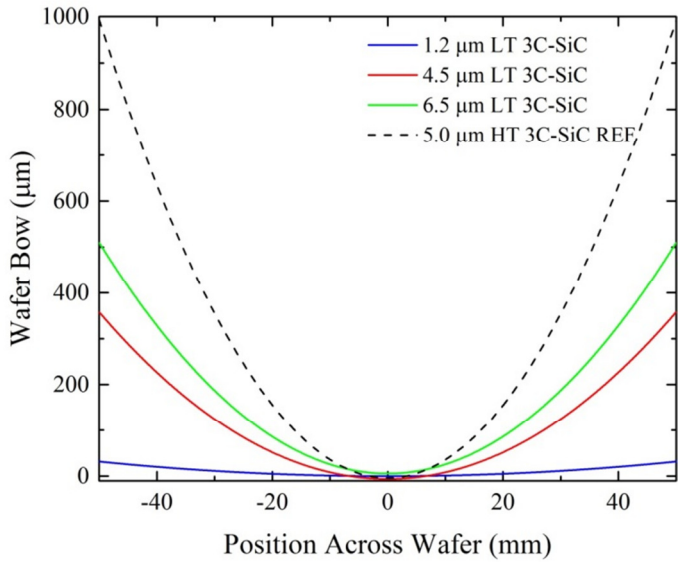

Figure 6.13 Wafer bow across a series 3C-SiC epi wafers of varying thickness grown at low temperature (LT) using the method described here. A high temperature (HT) grown epi wafer has been added for comparison.

While other parameters such as crystallinity can affect the wafer bow of the 3C-SiC/Si epi wafers the plot shows a clear decrease in wafer bow of similar thickness epi wafers of over 60% when comparing the 5 µm high temperature 3C-SiC to the 4.5 µm thick low temperature 3C-SiC. While >350 µm wafer bow is still too high for most wafer scale device fabrication techniques the 1.2 µm thick 3C-SiC epi wafer exhibits below 40 µm of bow and is suitable for almost all forms of post growth processing. Another point to make here is that the 100 mm substrates are standard 525 µm thick. Often, thick substrates are used to suppress wafer bow in high thermal mismatched systems such as 3C-SiC/Si and can easily reduce the wafer bow from the values shown here.

6.5.3 Assessing Material Crystallinity

One of the standard techniques already used to analyse 3C-SiC epilayers is through HR-XRD ω-2θ coupled scans and are used to quantify the crystal quality of the epilayers and whether the films were monocrystalline, polycrystalline or amorphous. A 3C-SiC epilayer grown using the optimised C/Si ratio is shown to be monocrystalline as evidenced by the lack of Bragg peaks associated with planes other than those equivalent to the (004) plane in 3C-SiC, see Figure 6.14.

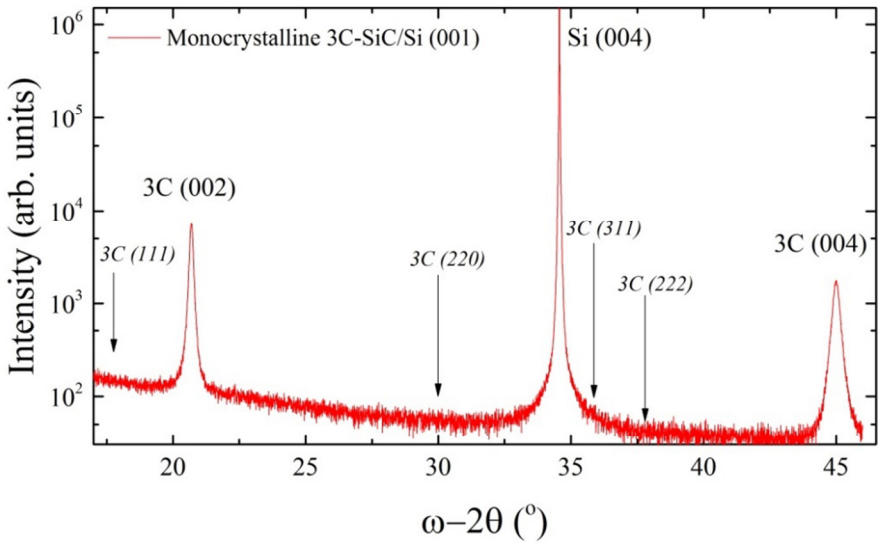

Figure 6.14 HR-XRD ω-2θ coupled scan of a 250 nm thick 3C-SiC epilayer grown on Si (001). The 3C-SiC (002) and (004) Bragg peaks are clearly seen. No other 3C-SiC peaks can be observed which implies that the 3C-SiC layer is monocrystalline.

While lab-based coupled scans are a relatively simple and fast HR-XRD technique (2-4 hours depending on resolution), they cannot give accurate information regarding the crystalline tilt or strain state of the epilayer relative to the substrate. Strain is an important factor to be considered with 3C-SiC as it is indicative of either incomplete relaxation in the epilayer film or thermally induced stress.

In order to properly assess the crystalline tilts and residual strain of the 3C-SiC epilayers it is necessary to obtain HR-XRD RSMs. For the 3C-SiC/Si heterostructures two types of RSMs were measured: symmetric (004), for evaluating crystalline tilt, and asymmetric (224), for analysing the strain in the 3C-SiC epilayers, see Figure 6.15. Due to the large separation of the 3C-SiC and Si Bragg reflections it was necessary to obtain separate, smaller area RSMs around each of the Bragg reflections individually, then stitch the data together. Without doing this the scan range would have been too large and the RSMs would have taken weeks to collect using lab based diffractometers.

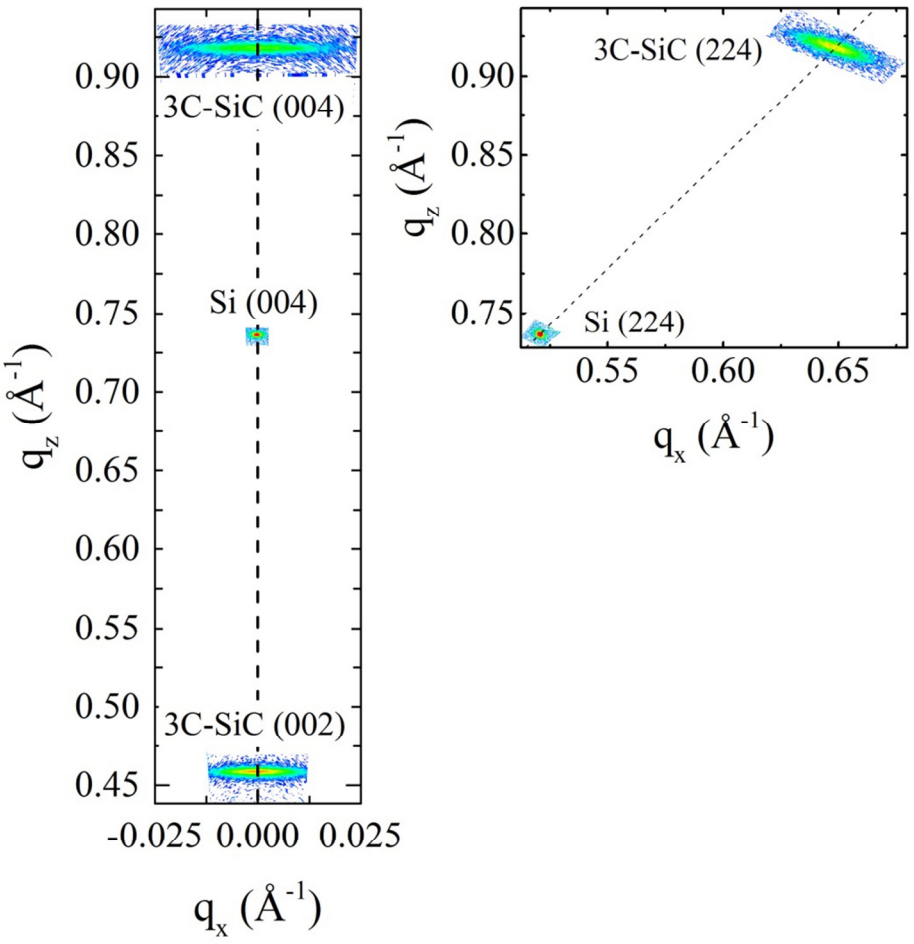

Figure 6.15 Symmetric (004) (left) and asymmetric (224) (right) RSMs of a typical high quality 3C-SiC/Si (001) heterostructure. The epilayer is free from tilt and under 0.097% residual tensile strain

The 3C-SiC/Si RSMs demonstrate that the epilayers are free from tilt and under minimal residual tensile strain.

Another HR-XRD measurement technique of interest is the acquisition of pole figures which can be used to look for Bragg reflections from different equivalent planes in a crystal. In a cubic structured crystal such as 3C-SiC (001), one would expect 4 equivalent peaks in a pole figure from any allowed Bragg reflection other than higher orders of the {001} planes. Figure 6.16 shows a pole figure around the 3C-SiC (111) reflection acquired from a 3C-SiC/Si (001) sample. The presence of the four peaks separated only by 90° in phi represent the four accessible equivalent {111} planes. In defective 3C-SiC, it is typical to observe additional peaks from {111} planes of microtwins at angles much closer to the origin due to the reversal of stacking sequence

[162]. These defect characteristic peaks are not observable in the 3C-SiC sample shown below indicating a very low density of microtwin defects in the 3C-SiC epilayer.

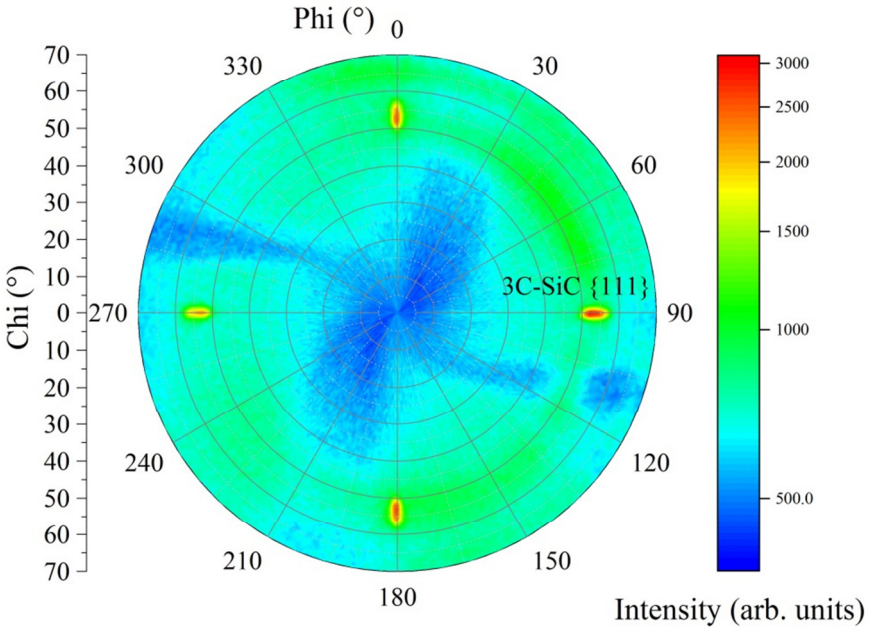

Figure 6.16 A pole figure about the 3C-SiC {111} Bragg reflections taken at chi values from 0 to 70.

6.5.4 Defect Analysis through X-TEM

Characterising defects through HR-XRD and other techniques can be convenient and give a quantifiable crystal quality of a particular heterostructure, however, it does not allow one to directly observe defects within the crystal nor extract defect densities, other than those based on empirical relationships.

To assess the defects present in the 3C-SiC epilayers, a combination of standard resolution and lattice resolved images were acquired through X-TEM measurements. The TEM micrograph of the low temperature growth 3C-SiC shown in Figure 6.17 shows that the epilayer is crystalline and is compared to a higher magnification TEM image of the commercial 3C-SiC grown at high temperature from Chapter 4. The TEM image also highlights the annihilation of planar defects in the 3C-SiC epilayer as a very high density of stacking faults and other defects can be observed at the 3C-SiC/Si interface which then decreases as the epilayer thickness increases. At the surface of the 250 nm 3C-SiC epilayer the stacking fault density is approximately 4×10^5 cm^{-1}, comparable to the defect in density in the commercial grade 3C-SiC/Si (001) heterostructure at a thickness of 500 nm from the interface. This implies that the quality

of the low temperature grown 3C-SiC is comparable, if not superior, to the commercial grade material at identical thickness.

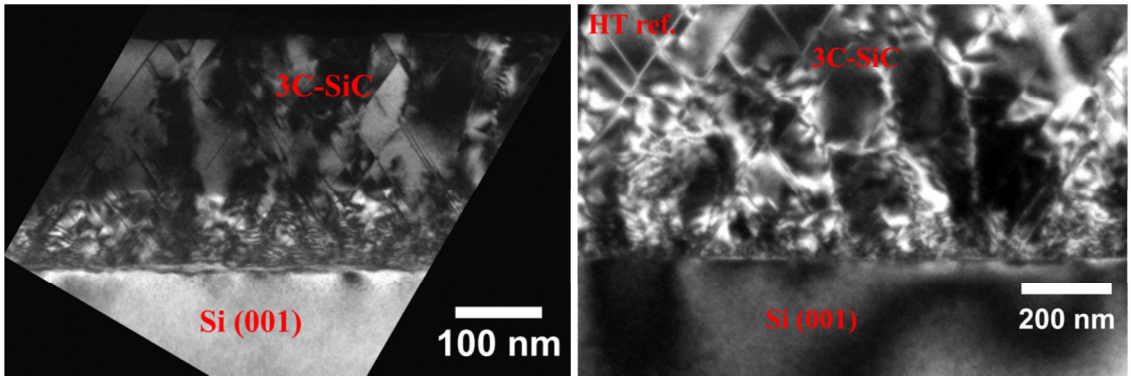

Figure 6.17 DF (220) X-TEM micrographs of: Left - a 300 nm thick 3C-SiC/Si (001) sample grown at low-temperature highlighting the crystalline quality of the as-grown epilayer. In addition, there are no voids present at the 3C-SiC/Si interface which is consistent across the entire wafer. Right – a higher magnification image of the 3C-SiC/Si interface of the ~10 µm thick commercial material shown in Figure 4.1.

During TEM analysis it is possible to directly observe the electron diffraction pattern which can be used to assess the crystal structure of an epilayer relative to the substrate. Figure 6.18 shows an SAED pattern showing the Bragg peaks associated with the Si substrate and 3C-SiC epilayer. Due to the smaller lattice constant of 3C-SiC the peaks are distributed in the same pattern as the underlying Si but are spread out by ~20% in reciprocal space.

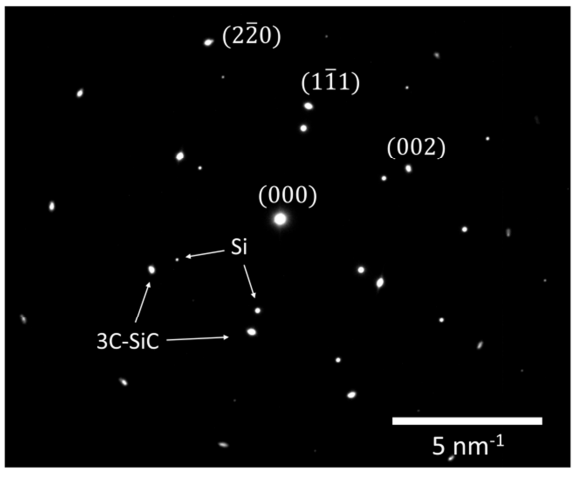

Figure 6.18 Selective area electron diffraction pattern of the 3C-SiC/Si (001) sample shown in Figure 6.17 showing Bragg peaks associated with both the Si substrate and 3C-SiC epilayer.

Observing defects through standard resolution X-TEM images can be used to estimate the defect density over a larger area, however, it is impossible to identify the exact nature of each planar defect without lattice resolution. High resolution, lattice resolved, X-TEM images were acquired after careful TEM preparation and polishing on a series of 3C-SiC/Si (001) samples. The lattice structure at the 3C-SiC/Si interface can be observed in Figure 6.19 and Figure 6.20. In the case of Figure 6.19 where the image is in focus, it is possible to see the additional lattice sites formed by the pure edge misfit dislocations to compensate the 20% lattice mismatch.

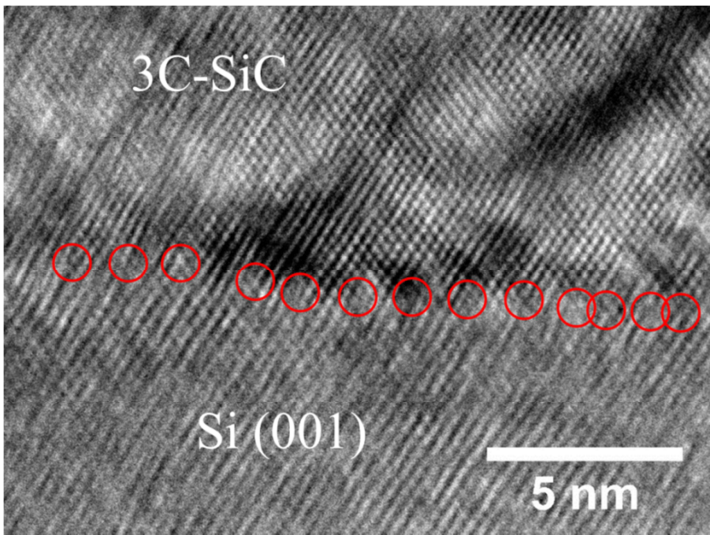

Figure 6.19 High resolution X-TEM image of a 3C-SiC/Si (001) interface. The additional lattice sites due to edge misfit dislocations are circled. In some cases observing the misfit is difficult as the break in the lattice structure blurs the lattice resolved image.

By focusing beyond the ideal focal point it is possible to resolve the (111) planes in both the Si and 3C-SiC which can be used to highlight the stacking faults emanating from the interface, see Figure 7.20. The density of misfit dislocations corresponds to approximately 1 in 5 which corresponds to the 20% lattice mismatch.

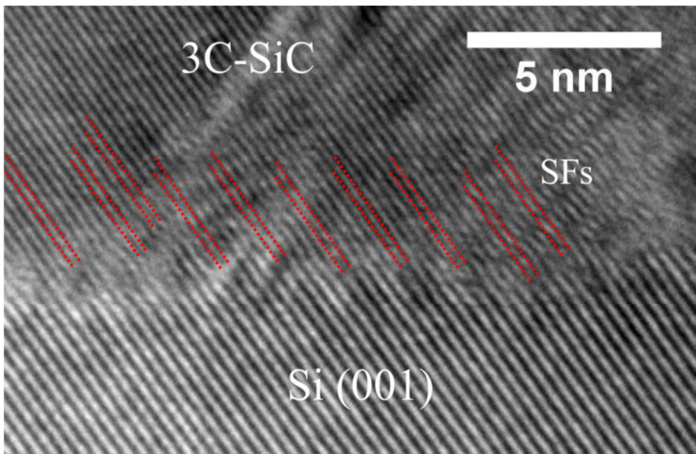

Figure 6.20 High resolution X-TEM images of a 3C-SiC/Si (001) interface, highlighting the insertion of addition 3C-SiC monolayers due to the ~20% lattice mismatch.

When two planar defects meet they tend to annihilate in 3C-SiC with a single defect emanating from the annihilation point. The phenomenon can be observed in Figure 6.21 where a series of stacking faults and microtwins can be seen to propagate throughout the epilayer and four points where defects annihilate are highlighted.

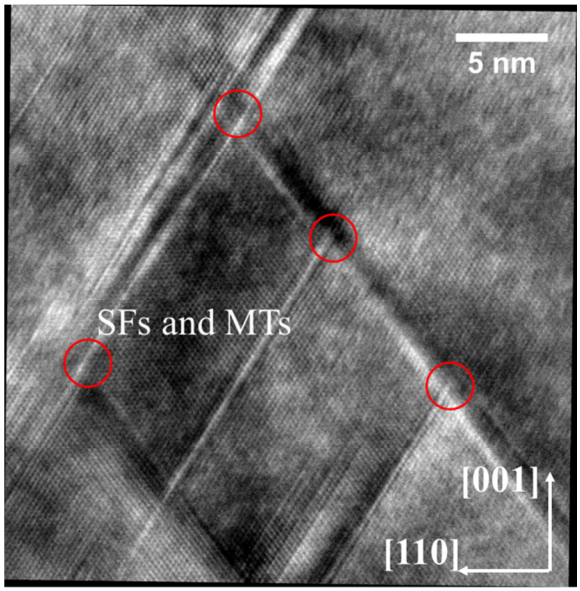

Figure 6.21 Stacking faults and microtwins in the 3C-SiC epilayer at approximately 150 nm from the 3C-SiC/Si interface. The points where two defects meet and one defect is annihilated are circled.

Once the 3C-SiC epilayer has reached 500 nm thick significantly fewer planar defects can be observed as the majority of stacking faults and microtwins have annihilated.

Figure 6.22 shows the surface of a 500 nm thick 3C-SiC epilayer with only a single microtwin propagating to the surface.

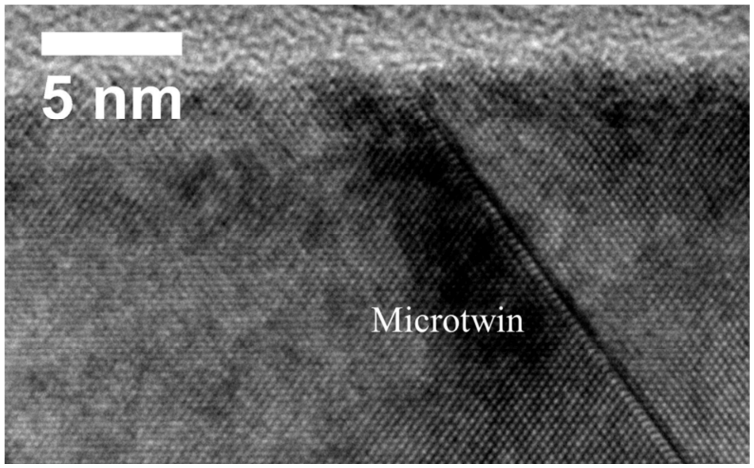

Figure 6.22 Lattice resolved X-TEM micrograph at the surface of a 500 nm thick 3C-SiC epilayer showing a microtwin emanating to the surface of the epilayer.

6.5.5 Surface Roughness

Much like crystal quality, the surface roughness was found to be highly dependent on the C/Si ratio as excess Si or C appears to lead to clustering on the epilayer growth front which roughens the surface. An extremely smooth, mirror like surface, with RMS roughness below 2 nm was achieved in the 3C-SiC/Si heterostructure, see Figure 6.23. It is also interesting to note that there are no obvious APDs on the surface which often present themselves as deep lines across the sample surface. As these epilayers were grown on on-axis substrates, APDs would typically form. However, the pre bake process carried out at the beginning of the growth run can promote diatomic steps in the Si surface if carried out under the correct conditions, which may have inhibited APD formation [80]. Alternatively, the appearance of APDs on the surface of the 3C-SiC surface may be linked to high growth temperatures and the lower growth temperature used suppressed the formation of visible grain boundaries in the 3C-SiC.

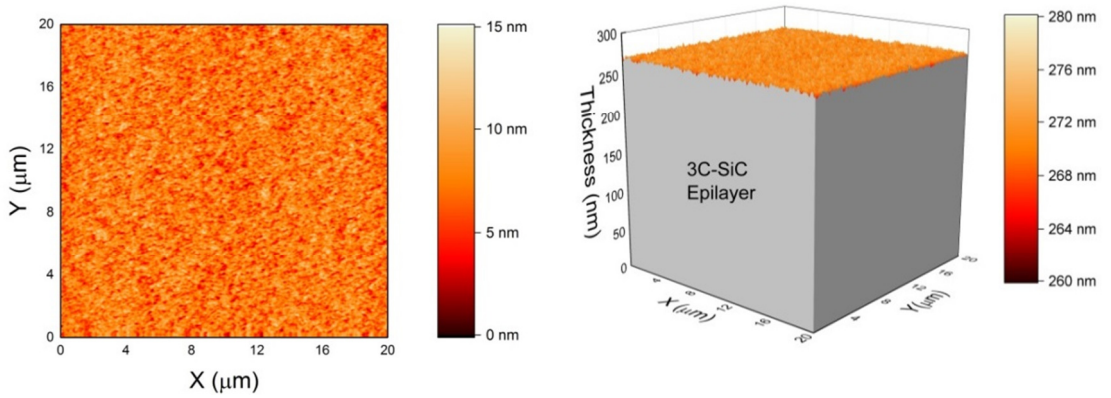

Figure 6.23 AFM scan of the surface of an as-grown 3C-SiC epilayer with an RMS roughness of 1.86 nm. The typical roughness of as-grown 3C-SiC epilayers is between 2 and 5 nm and found to increase with increasing epilayer thickness.

Surface roughness is a critical parameter for both device applications, achieving good metal contact and uniform oxide formation, as well as for further epitaxial growth in the case of using the 3C-SiC/Si structures as virtual substrates for other materials such as GaN. A rough substrate surface will affect the growth kinetics making 2D film growth almost impossible, leading to a high density of crystal defects and in most cases exaggerating the surface roughness of subsequent films.

6.6 Discussions

The low temperature RP-CVD process developed for the growth of 3C-SiC on Si (001) wafers presents a huge opportunity for the mass volume production of the wide bandgap semiconductor in the electronics industry. For decades, SiC has been plagued with high costs, small wafers, low volumes and defective crystals. The method presented offers a route to the low-cost manufacture of 3C-SiC on Si wafer sizes up to 300 mm and beyond using existing industry standard, Si based, cold-wall RP-CVD reactors. The material quality is superior to commercially available, high temperature grown 3C-SiC/Si, offers smooth surfaces that do not require post-growth polishing and reduced thermally induced wafer bow. Stacking fault densities of the low temperature grown 3C-SiC are comparable to higher temperature grown material of similar thickness, reducing planar defects will require other techniques such as selective epitaxy. By making use of highly reactive methylsilanes such as TMS along with an appropriate Si source, one is able to precisely control the growth conditions necessary for high quality

growth of 3C-SiC. Initially a $Si_{1-y}C_y$ buffer layer was used to suppress out-diffusion of Si from the substrate, however, it was later found that the C/Si ratio was more pivotal to the suppression of voids and high quality 3C-SiC could be epitaxially grown directly on Si substrates.

Monocrystalline 3C-SiC (001) has been demonstrated, therefore, the process is already suitable for a number of applications including MEMS, sensors and virtual substrates for cubic materials. Defects will always hinder power electronic applications in 3C-SiC and until the formation of these can be overcome its use in rectifying devices will be limited. If the technology can be applied to 3C-SiC growth on Si (111) substrates, it may also offer a virtual substrate for hexagonal materials such as GaN or graphene that is superior to alternative substrates on the market today.

Chapter 7
Doping of 3C-SiC

7.1 Introduction

Achieving high levels of electrically active dopants in a 3C-SiC epilayer is crucial for the formation of low resistance Ohmic contacts, controlling material conductivity and forming more intricate structures such as field effect transistors or p-type/intrinsic/n-type (PiN) diodes. One method of introducing dopants is through high energy ion implantation which typically requires post thermal annealing treatment at high temperatures to activate the dopants and restore crystallinity of damaged crystals [163]. This can be an issue with heteroepitaxially grown 3C-SiC/Si material as the upper annealing temperature is limited by the melting point of the Si wafer. The alternative approach is to dope the 3C-SiC epilayers during epitaxy by introducing gaseous precursors containing the appropriate n- or p-type impurities.

Nitrogen (N) is commonly used with SiC as an n-type dopant, however, there are certain drawbacks. Substitutional N has been shown to only occupy the C sites of the SiC lattice making it less efficient as a dopant. In addition, N has been shown to cause 'kick-out' a process by which a N atom takes a substitutional site, but knocks out a C atom from its lattice site leading to an interstitial impurity. This in-turn leads to the formation of in-active complexes which can reduce the electrical activation of the epilayer as a whole. Alternatively, P can occupy both the Si and C substitutional sites and does not lead to kick-out, making it the more efficient n-type dopant for 3C-SiC [94]. The downside to using P is that it often adheres to the chamber walls and susceptor of the CVD reactor which can lead to a memory effect and auto doping in subsequent growth runs. To avoid this issue, sufficient etch processes must be carried out after each growth run to minimise the depositions on the reactor after P doping of Si or $Si_{1-x}Ge_x$ [164]. Both N and P are shallow impurities in 3C-SiC, ideal for high levels of electrical

activation. While little has been published on the properties of P in 3C-SiC it has been shown to have an ionisation energy very similar to that of N, see Table 7.1.

Table 7.1 Ionisation energies of n-type dopants in 3C-SiC.

Dopant	Doping Concentration (cm^{-3})	Ionisation Energy (meV)	Reference
N	1×10^{19}	14	[165]
N	1×10^{18}	31	[165]
N	1×10^{16}	54	[166]
P	1×10^{16}	48	[165]

In this Chapter, n-type 3C-SiC films were grown through doping with phosphorus (P). Varying concentrations of dopants were introduced in ~50 nm 3C-SiC thin films grown on ~300 nm intrinsic 3C-SiC, see Figure 7.1.

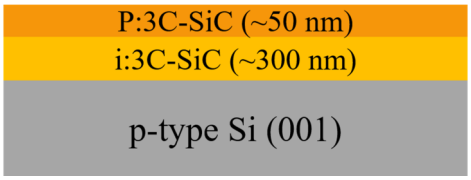

Figure 7.1 Cross-sectional schematic of the n-type 3C-SiC doped with P grown on an intrinsic 3C-SiC buffer on a p-type Si substrate.

For the growth of n-type 3C-SiC epilayers, the starting Si substrate was selected to be p-type. This was done intentionally to improve the accuracy of electrical measurements on the samples as, by setting up a PiN structure, it is far less likely any current will flow into the Si substrate, which would affect lateral electrical measurements. The doping precursor used for the growth of n-type 3C-SiC was phosphine (PH_3). The growth conditions of the doped 3C-SiC epilayers are summarised in Table 7.2.

Table 7.2 Growth parameters of doped 3C-SiC heterostructures.

Variable	P1	P2	P3	P4	P5
Estimated thickness (nm)	i – 300 n – 50	i – 300 n – 50	i – 300 n – 50	i – 300 n – 50	i – 300 n – 50
Relative dopant flow rate	200	10	1	0.1	0.01

SIMS analysis was performed to determine the concentration of impurities incorporated into the growth process for the P doped samples. Samples P1 and P2 were analysed individually, however, to save on time and investigate how dopants behave at abrupt interfaces, a multilayer was grown that incorporated the doping profiles of samples P3,

P4 and P5 with intrinsic 3C-SiC spacers, see Figure 7.2. The SIMS depth profiles are shown in Figure 7.3.

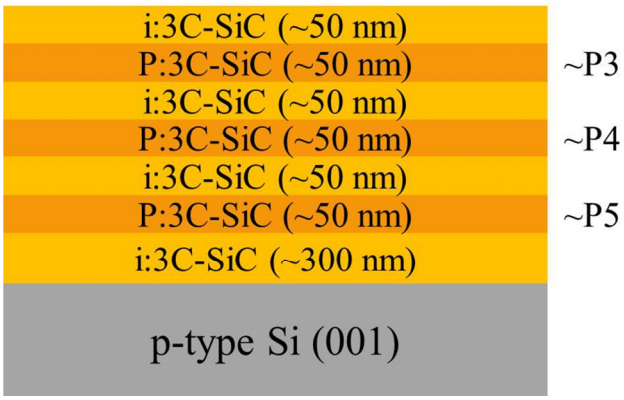

Figure 7.2 Cross sectional schematic of P doped multilayer with doped layers equivalent to those of samples P3, P4 and P5.

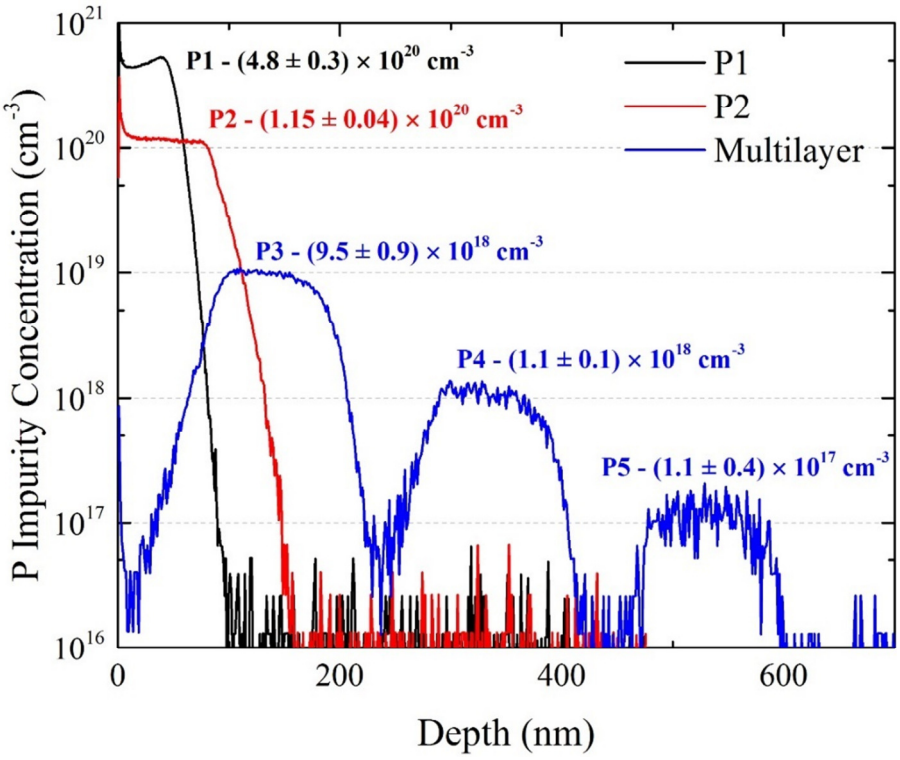

Figure 7.3 SIMS depth profiles of P impurity concentrations in samples P1, P2 and the multilayer.

The SIMS profiles of samples P1 to P5 show P incorporation in agreement with the ratio of dopant flows described in Table 7.2 with an almost perfect linear relationship between dopant flow and P concentration, see Figure 7.4.

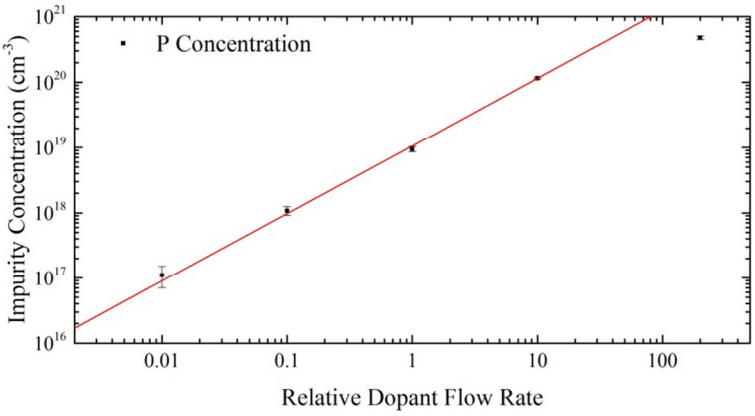

Figure 7.4 Linear dependence between dopant flow rate and impurity concentration as measured through SIMS. The highest concentration does not lie on the linear fit and implies the dopants have saturated in the 3C-SiC epilayer.

The multilayer of samples P3 to P5 also shows relatively sharp interfaces between the P doped regions and the intrinsic spacers, although this can be smeared through the SIMS analysis process or by variations in the sample thickness. This implies that the dopants are immobile within the 3C-SiC, which is to be expected due to the inertness of 3C-SiC and low diffusivity. This is an important property for the formation of abrupt interfaces in semiconductor devices structures such as in pn-junctions.

Cross sectional TEM was carried out to assess the impact of dopant incorporation in the 3C-SiC capping layers and images for samples P1 and P2 can be seen in Figure 7.5.

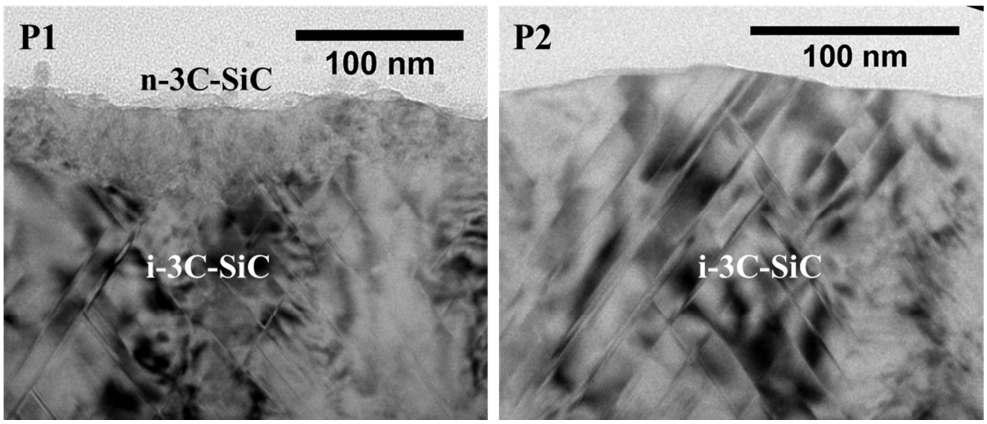

Figure 7.5 X-TEM images of sample P1 (~5 × 10^{20} cm^{-3}) and P2 (~1 × 10^{20} cm^{-3}). The n-type doped region in P1 is clearly distinguished by its severe degradation in crystal quality while sample P2 shows no signs of reduction in crystal quality through doping.

The cross sectional TEM images of P1 and P2 show that the intrinsic 3C-SiC epilayers are dominated by planar defects which is expected, however, it is possible to see the doped capping layer of sample P1 by its severe crystal degradation. This is not the case with sample P2 which shows no signs of crystal degradation. It is difficult to distinguish the n-type region from the intrinsic 3C-SiC in sample P2.

The surfaces of the 3C-SiC epilayers were assessed through tapping mode AFM scans, see Figure 7.6. While the surface of sample P1 is relatively smooth, probably a result of the amorphous 3C-SiC growth by the saturation of P atoms, the other doped samples are rougher. The surface of P2 in particular is dominated by islands of diameter approximately 100-200 nm and heights ranging up to 50 nm above the surface of the 3C-SiC epilayer. The height of these surface features decreases as the doping level is reduced from P2 to P4 thus reducing the RMS roughness, however, the density of the defects remains relatively constant across the samples. Spherical grain formations have also been observed in N doped 3C-SiC, however, the authors gave no explanation to the formation of the features [104]. High doping levels have been shown to increase surface roughness such as in P doped Ge epilayers where the increase in dopant flow was found to reduce the growth rate and increase surface roughness. This effect is thought to be caused by the interference of P complexes with growth sites impeding the growth uniformity [167]. One explanation for the unique shape of the observed hillocks could be the segregation of P atoms to the 3C-SiC surface, a common problem with n-type dopants in other semiconductors [168]. If this were the case then the AFM maps suggest that a proportion of the P incorporated in the growth may not be fully substitutional and therefore the results of the SIMS analysis may not be an accurate portrayal of the dopant concentration in the 3C-SiC epilayers. The hillock formations are visible under SEM secondary electron imaging of the epilayer surface, see Figure 7.7. An X-ray energy dispersive spectrum (EDS) of the area shows no P present, although the concentration of P may be below the detection limit for the SEM EDS detector. Mapping the presence of P by EDS was difficult due to the small size of the hillocks.

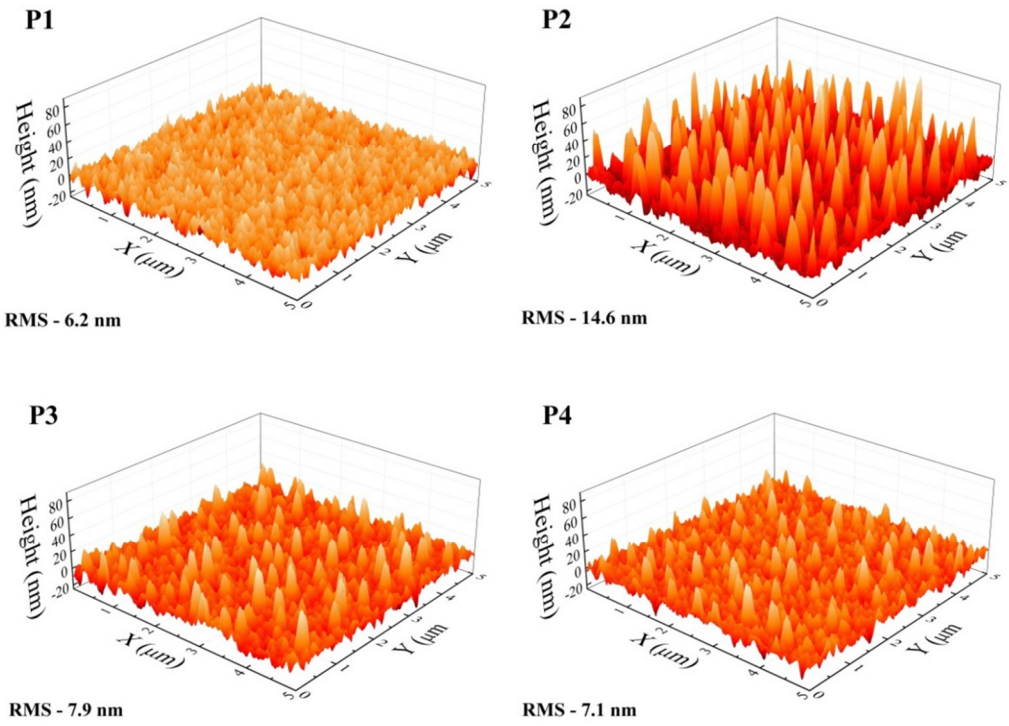

Figure 7.6 AFM surface morphology maps of samples P1 to P4 showing how the inclusion of P in the 3C-SiC affects the roughness of the samples.

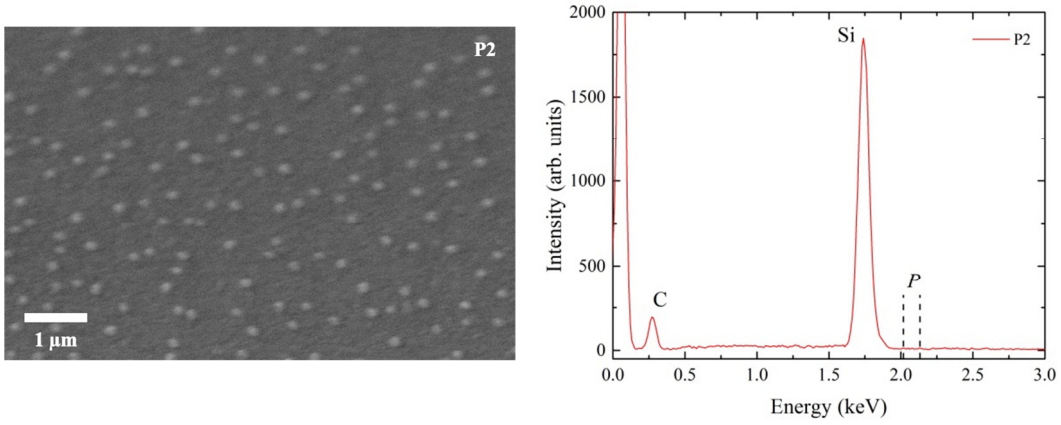

Figure 7.7 Left – Secondary electron SEM micrograph of the epilayer surface of sample P2 showing the hillock formations. Right – EDS spectrum from the SEM area showing peaks from C and Si at the expected positions. The expected positions for P peaks are shown, however, no peaks can be discerned.

The exact origin of the hillocks on the P doped 3C-SiC is still uncertain, further characterisation will be required to verify the composition and formation mechanism of the features.

7.2 Electrical Measurements

While SIMS is a useful method for assessing the total number of impurities in semiconductor samples, it cannot give information on whether dopants are electrically active or not. This can only accurately be measured with the help of electrical measurements such as the Hall and resistivity technique. In order to form test structures for the 3C-SiC samples it is first necessary to achieve Ohmic contacts. The resistance of metal contacts to semiconductors is vital for many device applications, however, strictly for 4-point Hall and resistivity measurements the contacts need only be Ohmic.

7.2.1 Contact Resistance

TLMs are an effective test structure for measuring sheet and contact resistance of thin film semiconductor samples. TLM structures were fabricated using photolithography, sputtering and dry etching techniques, see Figure 7.8.

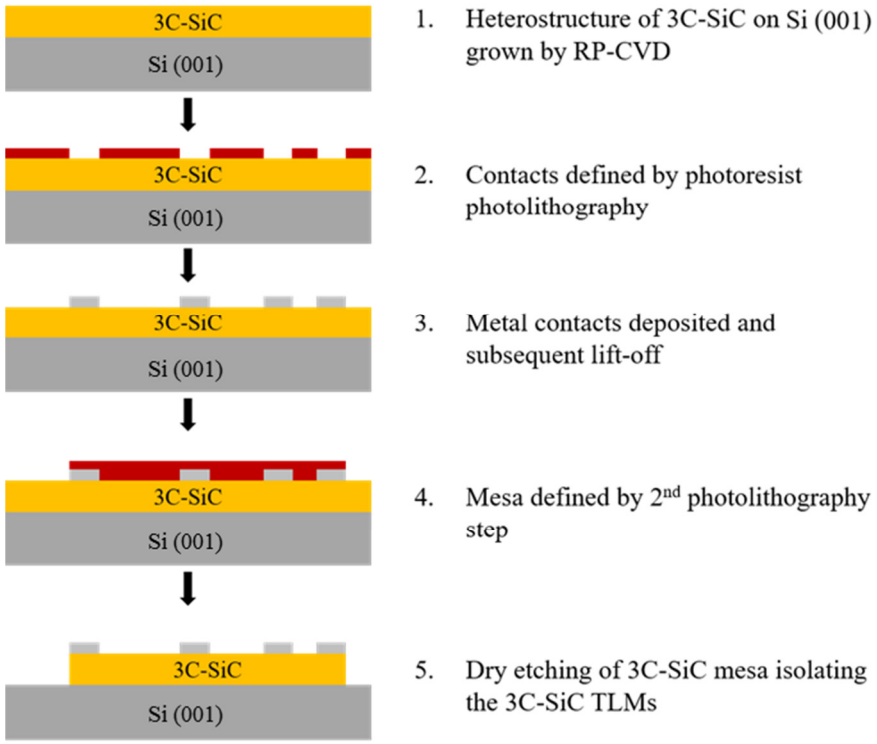

Figure 7.8 Fabrication process of linear TLMs.

In order to form Ohmic contacts to the n-type 3C-SiC epilayers, nickel chromium (NiCr) contacts were deposited by sputtering. NiCr (20% Cr) was chosen as a contact for the 3C-SiC as it has been shown to provide good Ohmic contacts to n-type 4H-SiC and 6H-SiC through the formation of Ni silicides at high temperature annealing [169].

NiCr was shown to act in a very similar method to Ni, however, it can offer higher stability, better adhesion with Au capping layers and can be sputtered more easily as a non-magnetic metal. Another reason to bet on NiCr as a contact for 3C-SiC is that the work functions of the two materials are similar. The work function of NiCr varies with Cr content but often this relationship is linear in alloys [170] therefore our NiCr alloy will have a work function of approximately 4.9 eV. The work function of 3C-SiC can be calculated by the electron affinity (4 eV) [171] with the energy gap between the conduction band and the Fermi level ($E_C - E_F$) meaning n-type doped 3C-SiC will have a work function between 5.2 eV (undoped) and 4 eV (degenerative). This simplistic model assumes no Fermi level pinning at the interface between the metal and semiconductor.

The fabricated TLM structures can be seen in Figure 7.9. Four-point electrical measurements were carried out at room temperature to extract the sheet (ρ_{sh}) and contact resistance (R_C) of the NiCr TLMs. TLMs were fabricated from samples P1 to P4 and were subjected a thermal anneal within a tube furnace under 5 slm Ar flow at 600, 700 and 800 °C for 10 mins.

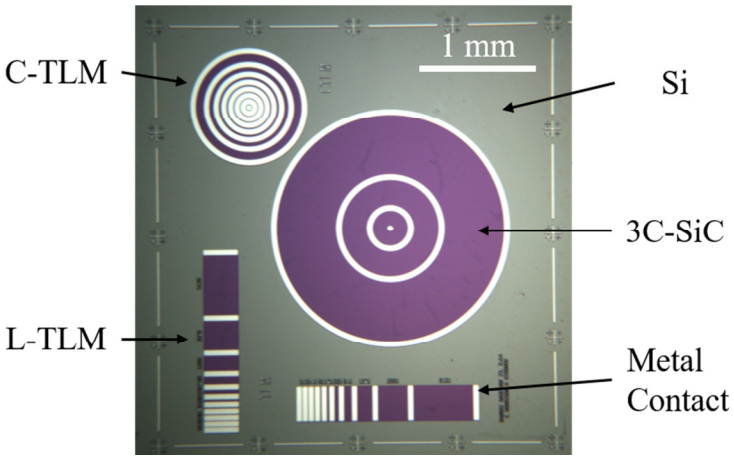

Figure 7.9 Optical image of 3C-SiC TLMs fabricated with NiCr metal contacts.

The electrical data were acquired through 4-point measurements in order to remove the impact of series resistance in the probes and wires between the sample and a semiconductor parameter analyser used to acquire I-V curves, an example plot of resistance vs separation for sample P2 can be seen in Figure 7.10.

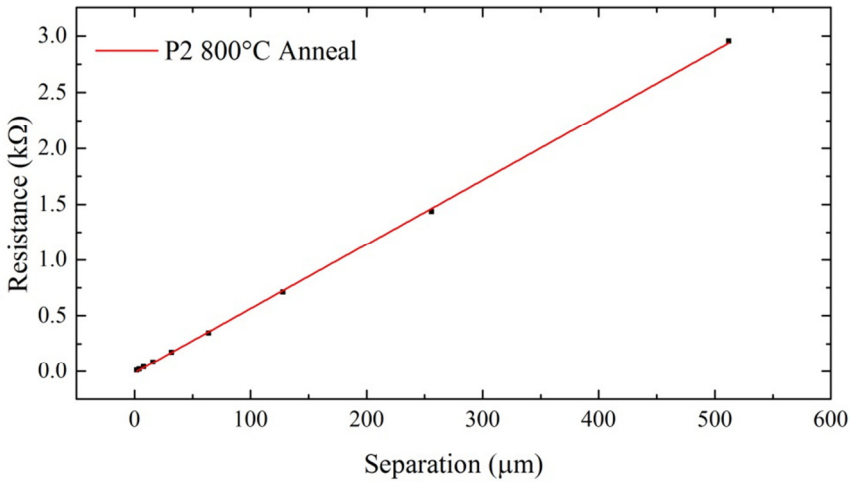

Figure 7.10 Resistance curve for a NiCr TLM sample with a weighted least-mean square linear fit.

The data were analysed according to the equations shown in Section 3.3.1 and are shown in Figure 7.11. The uncertainties on the resistance values were determined from the errors on the linear fits to the TLM data. While this appears reasonable for the contact resistance, the sheet resistance varies well beyond these uncertainties. It is more likely that these fluctuations are caused by the non-uniform distribution of dopants across the epi-wafer or potentially the thickness variations of the epilayer itself. As each sample may have been extracted from a different part of the central area of the epi wafer, these fluctuations are expected. That having been said, the sheet resistance of the sample appears to vary in proportion to the doping levels introduced into the epilayers, as shown by the SIMS data.

The sheet resistance is mainly unchanged after the annealing process indicating that the thermal treatment is not having a significant effect on the number of electrically active carriers in the epilayers, although these temperatures would be unlikely to affect this. The contact resistance, however, shows a strong dependency on the annealing temperature with each sample exhibiting a drop in contact resistance of up to 2 orders of magnitude when annealed at 700 °C. Increasing this anneal temperature has little effect on the highest doped samples P1 and P2, however, samples P3 and P4 appear to undergo another decrease in contact resistance with the 800 °C anneal. The lowest contact resistance recorded was for sample P1 at $1.5 \times 10^{-5}\ \Omega\text{cm}^2$, although the uncertainty on this value is high due to the nature of these TLM measurements. Higher accuracy measurements would require smaller contact separations which can only be achieved with other device fabrication techniques such as e-beam lithography. The

smallest resolvable separation of the NiCr TLMs fabricated here was typically 2 ± 1 µm.

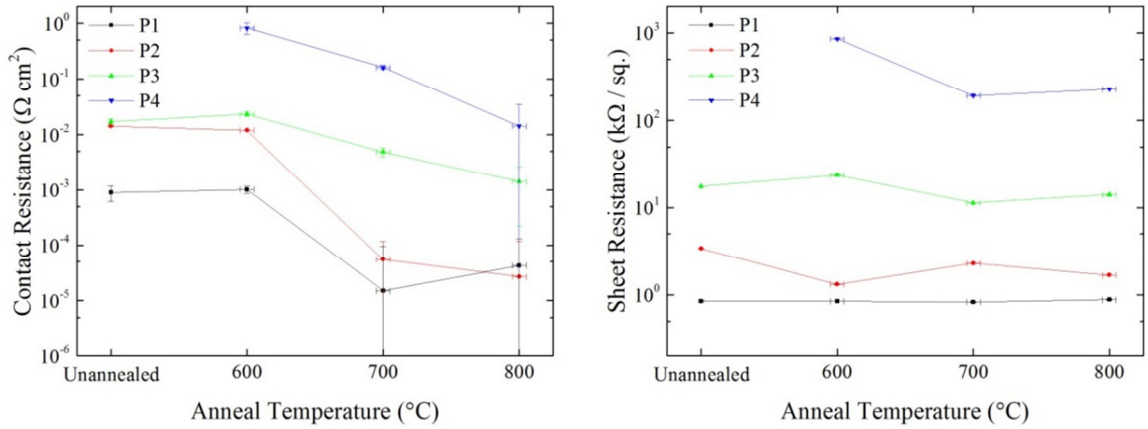

Figure 7.11 Contact resistance (left) and resistivity (right) of samples P1 to P4 under different anneal temperatures, including unannealed i.e. as deposited.

7.2.2 Carrier Concentrations

While TLMs can be used for measuring contact resistance and sheet resistance (giving an indication of carrier concentration) they rely on multiple measurement points and cannot be used to quantify doping levels or carrier mobility. Hall measurements offer an advantage as they can be used to measure Hall voltage in the presence of a magnetic field applied perpendicular to the sample surface. Hall bars were fabricated for the P doped samples in an identical process to the TLMs shown in Figure 7.8 and the resulting Hall bars can be seen in Figure 7.12. An SEM image of a selected Hall bar taken at an angle of 30° to the normal can be been in Figure 7.13 and gives a 3D depth view of the structures.

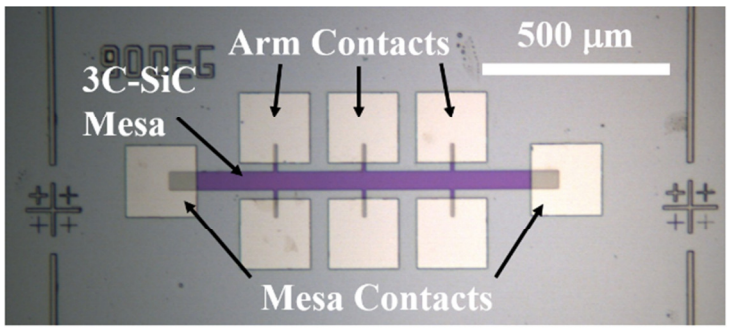

Figure 7.12 Optical images of 3C-SiC Hall Bars.

The 3C-SiC Hall bars with various doping concentrations were measured within a He^4 closed cycle cryostat (CCC) over a temperature range of 300 – 20 K with an AC current of 1 μA passed across the 3C-SiC bar in a magnetic field of ±150 mT for Hall measurements. I-V sweeps were taken at each temperature to ensure the contacts remain Ohmic over the measurement range.

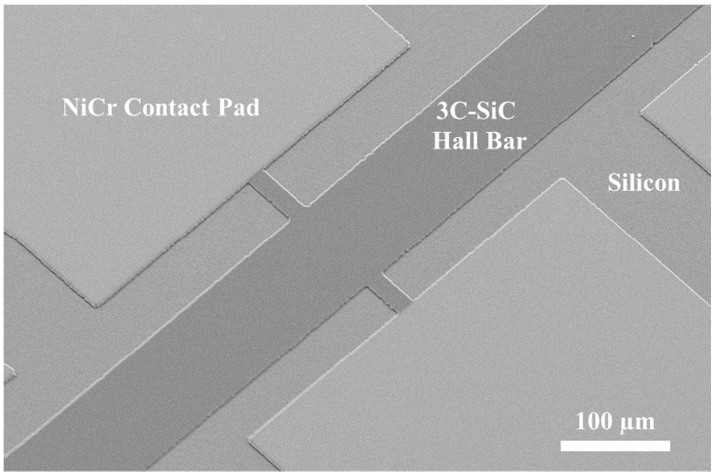

Figure 7.13 SEM image of a 3C-SiC Hall bar taken at 30° to the surface normal in secondary electron mode.

The measured sheet resistance of samples P1 to P4 are shown in Figure 7.14 while the carrier concentrations are shown in Figure 7.15.

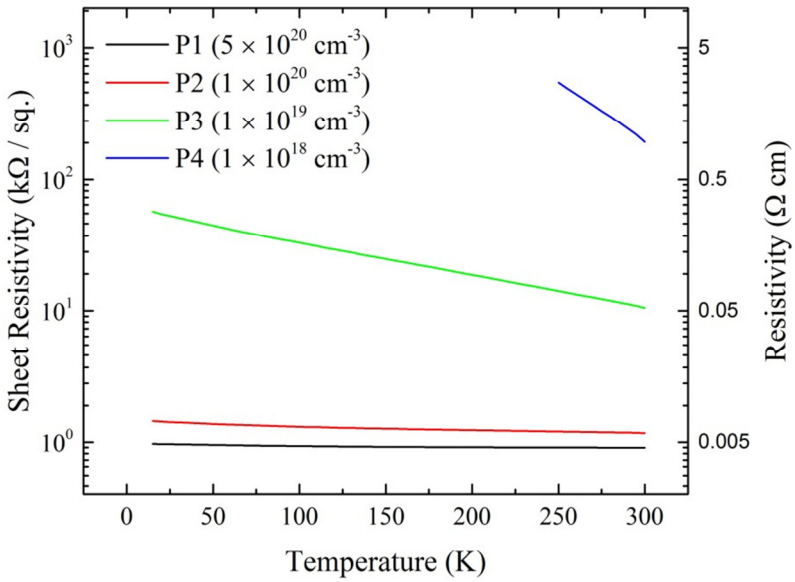

Figure 7.14 Sheet resistance of P doped Hall bars taken down to as low a temperature as possible before the resistance became too great for the measurement set-up or when the contacts were no longer Ohmic.

The resistivity of highly doped 3C-SiC epilayers remains almost completely unchanged over the range of the temperature measurements while the lower doped epilayers experience an increase in resistance with decreasing temperature.

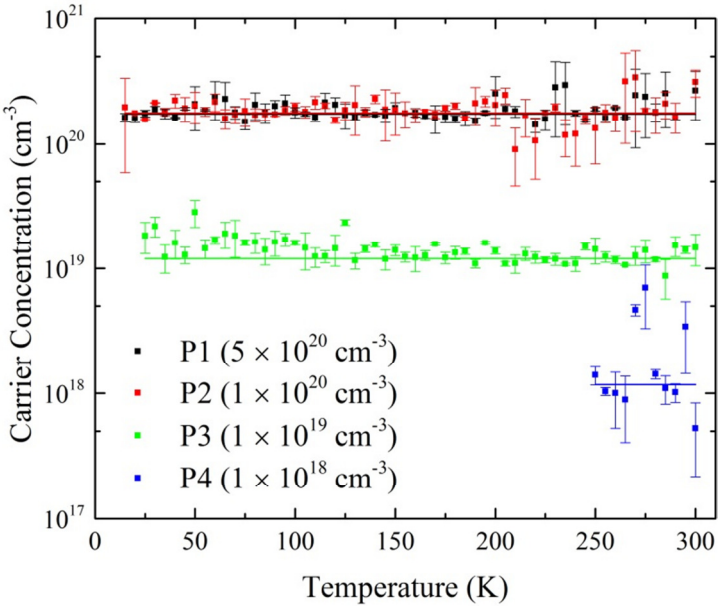

Figure 7.15 Electrically active carrier concentrations of samples P1 to P4, the impurity concentration as measured through SIMS is labelled. Uncertainties are derived from the standard deviation of repeat measurements. The room temperature electron mobility of sample P1 and P2 was approximately 5.2 $cm^2V^{-1}s^{-1}$ while for P3 the mobility was slightly higher at 8.6 $cm^2V^{-1}s^{-1}$.

The electrically active carrier concentration of samples P2 and P3 are in good agreement with the concentration of impurities measured by SIMS analysis, indicating a very high level of electrical activation. Sample P1 shows a similar doping level to P2 according to electrical measurements even though SIMS measured around 5×10^{20} cm^{-3} P atoms present in the layer. These measurements show that the phosphorus in sample P1 has saturated with only ~40% electrically active impurities. This gives an upper limit on P doping in low temperature grown 3C-SiC of around 2×10^{20} cm^{-3} which is amongst the highest value found in literature, see Table 7.3. The carrier mobility of the doped 3C-SiC is lower than that of undoped material typically 100-300 $cm^2V^{-1}s^{-1}$ due to the increased scattering off dopant ions.

Table 7.3 Typical doping levels achieved through ion implantation and epitaxy in 3C-SiC epilayers.

Dopant	Method	Impurity Conc. (cm^{-3})	Electrically Active Conc. (cm^{-3})	Activation Level (%)	Reference
P	Ion Imp.	6×10^{20} (SIMS)	-	NA	[172]
N	Ion Imp.	6×10^{20} (SIMS)	7×10^{19} (Hall)	11.7	[95]
N	Ion Imp.	1×10^{20} (simulated)	6×10^{19} (Hall)	60	[96]
Al	Epitaxy	2.1×10^{20} (SIMS)	2×10^{17} (Hall)	0.1	[98]
P	Epitaxy	2×10^{20} (SIMS)	2×10^{20} (Hall)	100	This Work

The excess P atoms appear to have led to the crystal degradation observed in the X-TEM images in Figure 7.2 and can be explained by the incorporation of a high number of interstitial impurities disrupting the growth of the 3C-SiC crystal. The effects seen in sample P1 are similar to those observed during high energy ion implantation [173] and perhaps the crystal structure could be partially restored by thermal annealing at very high temperatures above 1300 °C.

Sample P4 gave erroneous results for electrically active carriers and resistivity measurements were only possible down to 250K as the number of thermally activated carriers decreased, increasing the sample series resistance beyond the values capable of being measured in either AC or DC configuration of the cryostat. This is limited by the impedance of the measuring systems and would require more specific equipment such as electrometers to measure the Hall signals accurately. The thermal effect on carriers within samples P2 and P4 are shown in Figure 7.16, while the resistance of sample P2 is almost independent of temperature, sample P4 suffers from a significant increase in resistance when the temperature is reduced. Subsequently, it was not possible to measure the electrical characteristics of sample P5. As mentioned, this issue could be fixed by altering the measurement set-up but could also be aided by the growth of thicker doped 3C-SiC epilayers, which would reduce the series resistance across the samples.

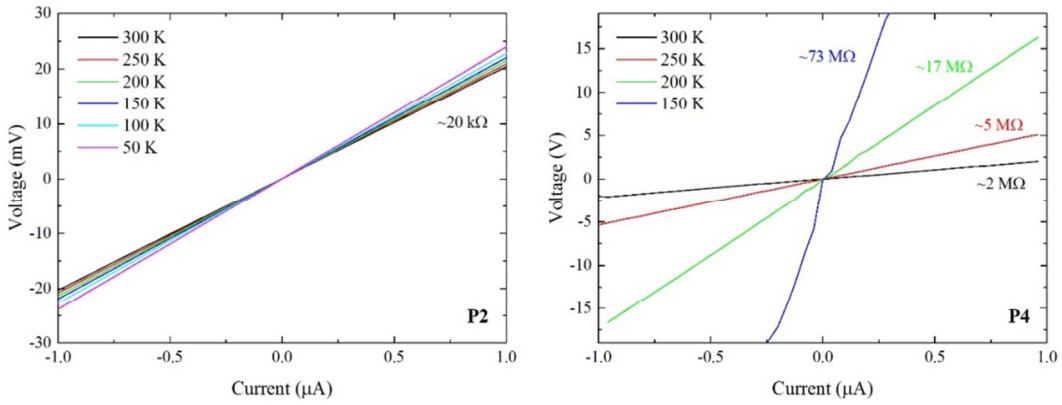

Figure 7.16 2-point I-Vs across the Hall bars fabricated from samples P2 (left) and P4 (right).

The electrically active dopants of samples P1 to P4 have been compared against the values measured by SIMS analysis in Figure 7.17. The errors have been derived through repeat measurements in Hall measurements and the variation of each plateau in SIMS measurements. There is good agreement between the two measurements although a systematic error is present between the two plots which has either overestimated the electrically active dopants (possibly due to doped region thickness uncertainty) or underestimating the SIMS measurements. As this error is very similar between P2, P3 and P4, it can be assumed that there is in fact very good agreement between the two measurements, indicating an activation level of close to 100% in these samples, while P1 is lower at only ~40%.

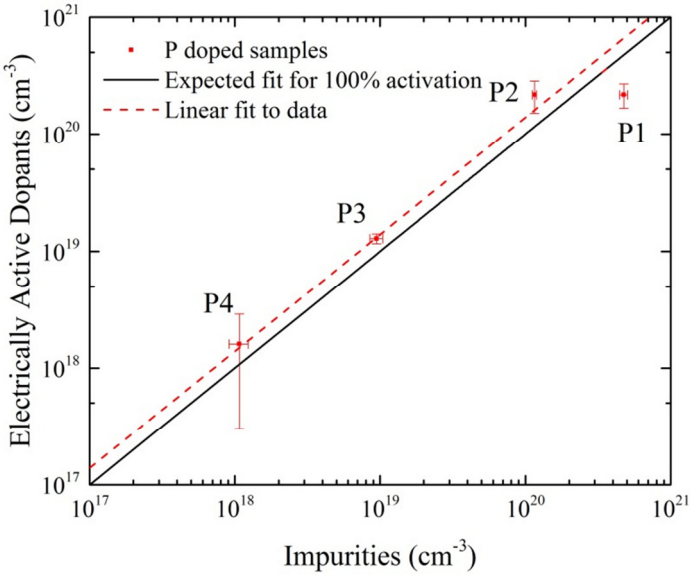

Figure 7.17 SIMS impurities against electrically active dopants measured by Hall effect measurements at room temperature.

To test the linearity of the magnetic field response and dependence on temperature of highly doped 3C-SiC devices, a Hall bar fabricated from sample P2 was placed into a cryostat with a superconducting magnet operating up to ±4 T and down to temperatures below 1 K. The Hall voltage was measured and expressed as a Hall resistance (V_H/I) where I is the current applied between the source and drain of the Hall Bar. In this case the current was fixed at ~10 μA for the duration of the experiment by passing 1 V across a 100 kΩ resistor in series with the Hall Bar. A field sweep from 0 T up to +4 T, down to -4 T and back to 0 T again was carried out at around room temperature (288 K) and 0.5 K, see Figure 7.18.

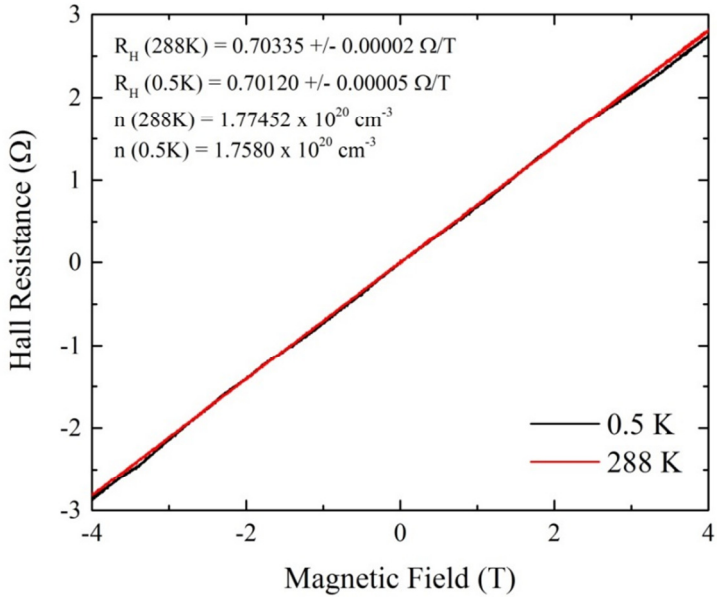

Figure 7.18 Magnetic field response of a Hall bar fabricated from sample P2 carried out at 0.5 K and 288 K.

The magnetic response was found to be linear at both temperature ranges and the decrease in temperature led to a discrepancy of Hall resistance of 0.31% from that of room temperature measurements. This indicates that even at extremely low temperatures the carriers of the 3C-SiC remain electrically active and constant, as expected. The values of electrically active n-type dopants agree well with previous measurements. While this measurement only yielded a response of ~0.7 Ω/T, the active region of the 3C-SiC sample is 50 nm thick, therefore decreasing this thickness would enhance this Hall voltage. Another method is to decrease the doping level in the 3C-SiC, however, this may lead to a temperature dependency.

7.3 Isolating Current Leakage

Many MEMS devices such as gas flow or pressure sensors are based on suspended structures and being able to fabricate these suspended devices out of 3C-SiC could lead to a number of enhancements over standard Si devices such as increased operating temperatures and resistance to chemical species. Suspending 3C-SiC from the underlying Si has another useful outcome as it removes leakage paths of current in certain 3C-SiC devices as stacking faults can lead to significant leakage into the substrate. The aim of this study was to fabricate suspended 3C-SiC Hall bars in order to assess a number of factors. Firstly, is NiCr a suitable metal contact for suspended 3C-SiC devices i.e. does it resist the etching effects of KOH or TMAH. Secondly, the operation of the suspended devices will be compared to that of standard bulk devices to determine whether suspending the 3C-SiC has any undesired effects and also whether suspending the 3C-SiC away from the Si substrate reduces any leakage currents into the substrate which may be affecting the electrical measurements, see Figure 7.19.

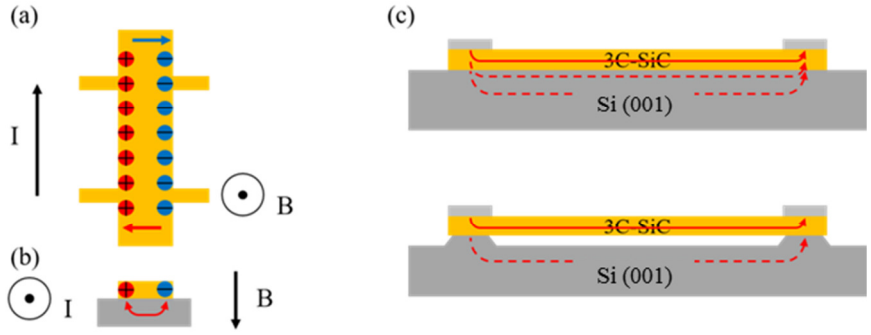

Figure 7.19 (a) The motion of charge carriers within the 3C-SiC Hall bar due to the Lorentz force experienced during the Hall effect. (b) the potential recombination of carriers via leakage paths into the Si substrate. (c) the potential leakage current paths through the Si substrate during Hall effect or resistivity measurements and how suspending a device could reduce this effect.

For this study, an intrinsic 3C-SiC with no intentional doping was used as it offers the highest resistivity and therefore increases the likelihood that current will pass through the substrate. The epilayer was ~300 nm thick and grown on a low doped p-type substrate. Hall bars were fabricated using the same method described above, however, one set of devices were suspended after fabrication by emerging them in 25% TMAH solution at 90 °C for approximately 1 hour in order to suspend the 3C-SiC bar while the contact pads remained mostly unetched. The suspended 3C-SiC Hall bar was imaged

using an SEM at varying angles of incidence, see Figure 7.20. While the bar is suspended, the contact pads are still attached to the bulk Si, although some etching occurs at the contact edges. It is worth noting that the edges of the contact pads appear to bow upwards, this could either be caused by the tiny residual intrinsic strain of the 3C-SiC or additional strain introduced by the NiCr contacts. Either way the effect is undesired and may lead to delamination effects.

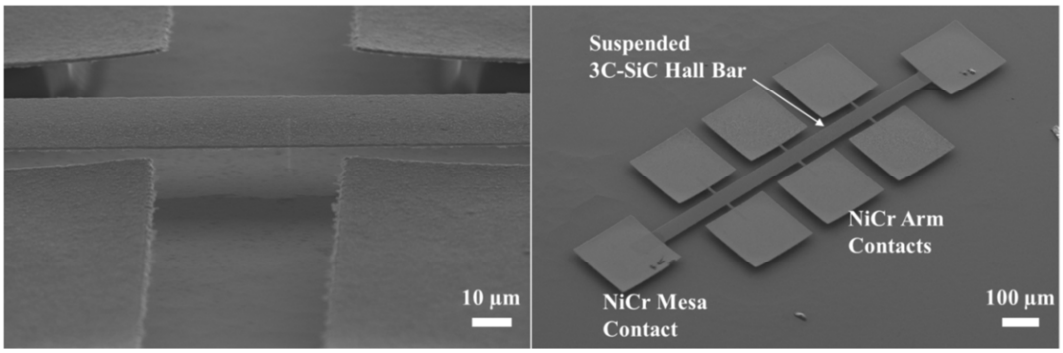

Figure 7.20 Secondary electron SEM images of the suspended 3C-SiC Hall Bar. The bar is fully suspended while the contact pads are still attached to the Si substrate.

The resistivity and carrier concentration of the 3C-SiC Hall bars were measured within the CCC system operating in DC mode. A source meter was used to apply a constant current of 100 nA over the Hall bar while the same source meter measured the sample resistivity. The source meter has an input impedance of 10 GΩ, capable of measuring the high resistance values from the undoped 3C-SiC. However, at low temperatures the source meter was unable to supply the 100 nA current source without reaching its voltage compliance. The electrical characteristics are compared in Figure 7.21.

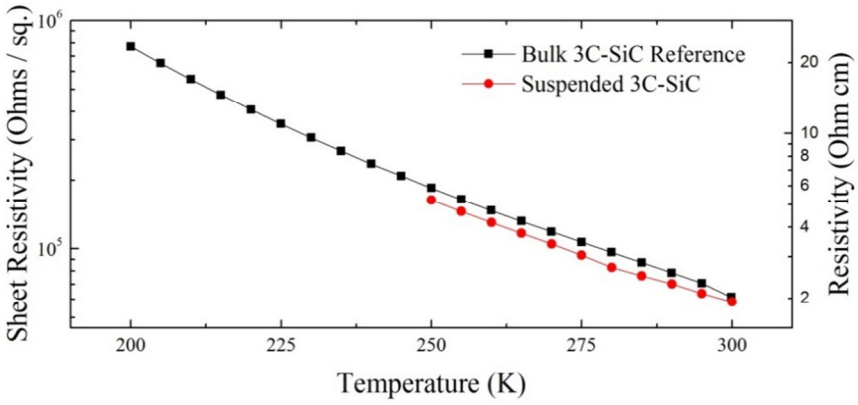

Figure 7.21 Resistivity of the undoped suspended and bulk 3C-SiC Hall bars. The carrier concentration of the two samples was measured to be $2\pm1 \times 10^{17}$ cm^{-3} with a room temperature carrier mobility of 21 $cm^2V^{-1}s^{-1}$.

While there is a slight change in the resistivity between the two samples, the suspended Hall bar exhibits a lower resistivity, rather than higher as expected, implying that either the current is not flowing through the substrate or that suspending the bar has had little impact on the current leakage paths. An unusually high carrier concentration of ~10^{17} cm^{-3} was measured leading to a low mobility around an order of magnitude lower than that of the commercial 3C-SiC from Chapter 4. The higher density of defects in the thinner 3C-SiC is thought to be the origin of the discrepancy as growth temperature below 1200 °C should not lead to high N incorporation. To verify this, SIMS measurements were carried out to investigate the level of N incorporation in the epilayers, see Figure 7.22.

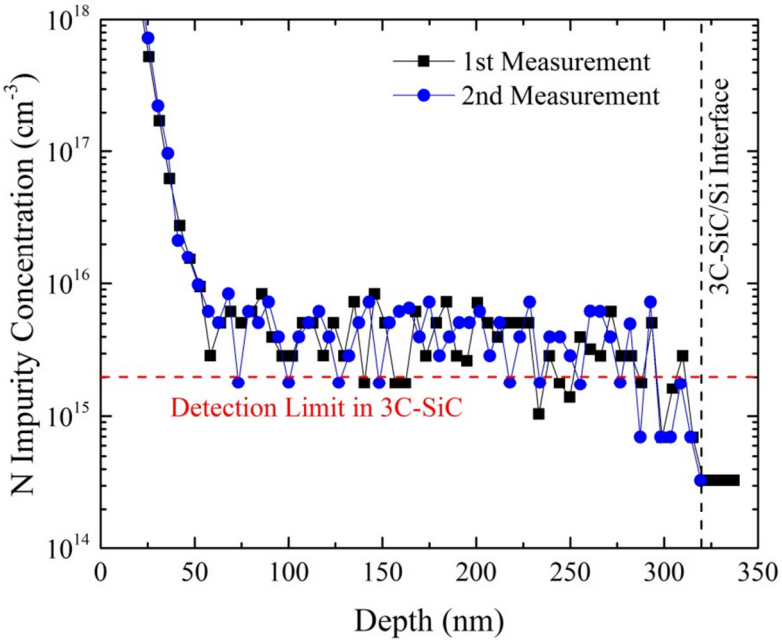

Figure 7.22 SIMS measurements for N incorporation in the 300 nm thick 3C-SiC/Si (001), unintentionally doped heterostructure.

The SIMS profile shows N levels between (2-8) × 10^{15} cm^{-3} implying low levels of incorporated N, although the measurements are close to the detection limit of N in 3C-SiC and fluctuations could instead be noise. Therefore it is possible the actual N incorporation is below this limit. The results of this spectrum shows that the low temperature growth of 3C-SiC results in very low levels of unintentional N doping, which are typically around 10^{16} – 10^{17} cm^{-3} for high temperature grown 3C-SiC/Si. This reduction could either be a result of the lower temperature leading to less incorporation, the purity of the growth precursors or the growth chamber itself leading to less residual

N in the system. Either way, the low levels of incorporation are useful for potential applications in power electronics and other electrical devices.

7.4 Discussions

An effective method for doping 3C-SiC epilayers grown at low temperatures with P has been demonstrated and can reliably be used to dope the material in a range from 1×10^{17} cm^{-3} to above 1×10^{20} cm^{-3} with effectively 100% electrical activation, although electrical data only confirmed active impurities down to 1×10^{18} cm^{-3}. The process can simplify device fabrication as it does not require activation annealing and can be used to avoid ion implantation in 3C-SiC. In-situ doping of 3C-SiC during epitaxy is shown to lead to no further crystal degradation, unless extremely high doping levels are attempted. The levels of doping achieved in this research are among the highest found in literature and 100% electrical activation is unheard of with ion implantation techniques, which typically achieve activation levels of around 10% or below, see Table 7.3. P is indeed found to be an effective n-type dopant for 3C-SiC, however, as N was not used during this method a direct comparison between the two n-type impurities cannot be made.

Being able to dope 3C-SiC to such levels is vital for creating low contact resistance Ohmic contacts. For n-type doped 3C-SiC, NiCr was found to be a suitable contact metal as it can be deposited easily by sputtering and forms an Ohmic contact without any thermal annealing treatment. High temperature annealing up to 800 °C was found to reduce contact resistance to approximately 10^{-5} Ωcm^2, around the lower limit of the TLM measurement technique used. This contact resistance is comparable or lower than those found in literature, see Table 7.4.

Table 7.4 Comparing typical contact resistances obtained from different Ohmic contact metals on n-type 3C-SiC, where Ti represents titanium.

Contact Metal	**Annealing Temperature (°C)**	**Dopant**	**Doping Level (cm^{-3})**	**Contact Resistance (Ωcm^2)**	**Reference**
Ni	1000	P	-	1.4×10^{-5}	[174]
Ni	950	N	3.5×10^{19}	1.5×10^{-5}	[175]
Al	250	N	7×10^{17}	1.8×10^{-4}	[176]
Ti/Ni	1000	N	5×10^{20}	0.8×10^{-5}	[172]
Ti/Ni	1000	P	5×10^{20}	2.0×10^{-5}	[172]
NiCr	800	P	2×10^{20}	1.5×10^{-5}	This Work

High temperature annealing was found to reduce contact resistance by around a factor of 100 for all doping levels investigated, although higher doped samples obviously exhibited lower resistances.

The magnetic field response of a highly doped 3C-SiC epilayer was found to be linear to extremely high magnetic fields (± 4 T) and vary within 0.31% with a temperature variation of 288 K down to 0.5 K, an effect caused by the combination of low levels of thermally activated carriers in the wide bandgap 3C-SiC and the high levels of electrically active dopants. This device characteristic is ideal for Hall sensors operating at such high magnetic field and where temperature insensitivity is also required [177]. Possible application sectors can include research environments and medical field but also possibly in automotive or aerospace sectors where temperature insensitivity is a desired parameter. The cryostat system used for these measurements was incapable of operating at temperatures beyond ~300 K therefore the temperature dependency of such a 3C-SiC based Hall sensor could not be tested at high temperatures and is clearly an interesting topic for further research.

Resistivity and Hall effect measurements were also carried out on suspended undoped 3C-SiC Hall bar test structures. NiCr was again found to be a suitable metal contact for this process as it is resistant to the etching effects of TMAH. The operation of the suspended device was found to be unchanged from that of the non-suspended device demonstrating that this material is indeed suitable for applications within MEMS devices. Unfortunately, suspending the device did not lead to any significant variation in electrical properties, implying either that current is not leaking through the Si substrate or that suspending the device has no effect on these leakage current paths. Further work is required to confirm which of these statements is correct, the most simple method of which is to optimise the device structure to reduce the current flow through the bulk Si even after a device is suspended, a proposed device structure is shown in Figure 7.23

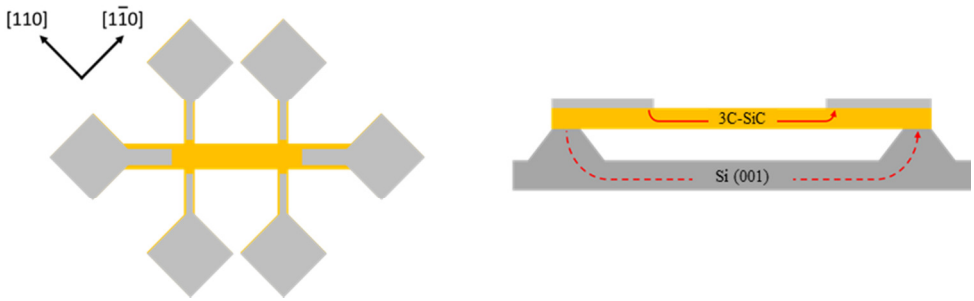

Figure 7.23 Proposed test structure for a suspended 3C-SiC Hall bar and potential current paths through the structure.

The contact pads are orientated to the {110} planes so they will not etch as fast as the bar due to the slow etch rate in the [111] direction which will also allow the bar to be etched for longer, increasing the distance between the suspended bar and the substrate. The metal contact arms extend on the bar so the current path through the 3C-SiC is reduced.

Additional improvements to the devices could be realised with other types of substrates. Floating zone (FZ) Si substrates have significantly higher electrical resistance due to their improved purity and could limit current flow through the substrate. Another approach could be use Si on insulator (SOI) wafers followed by the suspension technique described previously. By etching down to the oxide layer in the substrate one could completely remove any Si connection between the two ends of a mesa, hence forcing the current through the 3C-SiC even at elevated temperatures.

The carrier concentration of the undoped 3C-SiC was measured in the order of 10^{17} cm^{-3} which is not linked to N incorporation, as this was measured to be below 10^{15} cm^{-3} through SIMS measurements, hence, it is thought the origin of this high carrier concentration is due to the stacking fault defects in the 3C-SiC epilayer. Further work is required to reduce the impact of planar defects and increase the mobility of the undoped 3C-SiC.

Chapter 8
Properties of Suspended Structures

3C-SiC based suspended structures have a range of potential applications within MEMS and sensing devices such as in membrane based pressure sensors and micro heaters [103, 178], resonators for mass sensing in biological applications [179] and even structures for photonic confinement [180]. As a material, 3C-SiC is attractive as structures can be formed easily by the selective wet etching of the underlying Si and the high operating temperatures and resistance to chemical and radiation effects makes the devices ideal for operation within harsh environments. The following studies investigate the properties of suspended 3C-SiC and $Si_{1-y}C_y$ structures (membranes and micro-wires) and their suitability for a range of applications.

The effects of strain variation can have significant consequences on the physical properties of suspended films and structures. One such example can be directly observed in the bending of suspended 3C-SiC cantilevers [181]. There have been some attempts to investigate the effects of strain on suspended 3C-SiC structures through the use of micro-Raman (μ-Raman) mapping [182, 183]. In all cases, the 3C-SiC has been observed to undergo slight relaxation from residual tensile strain, caused by mismatch in thermal expansion coefficient [69], upon suspension. Another interesting observation made on suspended 3C-SiC structures is an increase in strain located only at the interface between suspended and supported 3C-SiC in the undercut region. This has been shown to be caused by the activation of a shear stress at the undercut region [184].

8.1 Strain Mapping of Suspended 3C-SiC Membranes

The aim of this investigation was to measure the strain relaxation of a suspended 3C-SiC square membrane through the use of micro X-ray diffraction (μ-XRD), a method which has been previously applied to crystalline Ge membranes [185]. The direct measurement of the lattice parameters through the use of XRD would firstly corroborate

the results observed through Raman peak shift, but in addition, can also give information regarding the localised tilt of the suspended structures.

8.1.1 Fabrication of suspended 3C-SiC membranes

Suspended membranes were fabricated from the 3C-SiC/Si(001) epi wafer grown at high temperature by the LPE ACIS M8 RP-CVD system, see Chapter 4. The residual strain of the suspended membranes was mapped using micro X-ray diffraction (μ-XRD) on beamline B16 at the Diamond Light Source synchrotron using the process described in section 3.2.3. Due to the large lattice mismatch of ~19% between Si and 3C-SiC there is a large separation of the Bragg peaks in reciprocal space. As a result of this, separate RSMs around the Si and 3C-SiC peaks were performed with the detector centred on the Si and 3C-SiC 2θ respectively.

Symmetric (004) and asymmetric (115) RSMs were acquired at various points across a 1.3 mm × 1.3 mm 3C-SiC membrane by μ-XRD so as to map the Si and 3C-SiC Bragg peaks in a line scan profile through the centre of the membrane and onto the supporting bulk Si along the $[1\bar{1}0]$ direction. The in- and out-of-plane strain profiles are shown in Figure 8.1. While both profiles are dominated by noise, the uncertainties of the in-plane profile are far more significant and are exaggerated by the calculation of lattice parameters from the (115) RSMs. The in- and out-of-plane lattice parameters ($a_{\parallel}$ and $a_{\perp}$ respectively) were determined from the (115) RSMs after being corrected for the tilt measured from the (004) RSMs using

$$a_{||} = \frac{\sqrt{2}}{q_{||}} \qquad a_{\perp} = \frac{5}{q_{\perp}} \qquad \text{Equation 8.1}$$

The use of (224) RSMs would decrease this error as variations in $q_{||}$ would be larger and the Bragg diffraction intensity is larger due to the (224) reflection has a stronger structure factor, however, these were not feasible with the experimental set-up. The out-of-plane strain suffers from less noise and a profile can be observed with the strain varying from $\varepsilon_{\perp}$ = (-0.09 ± 0.01) % on the supported edges to $\varepsilon_{\perp}$ = (-0.07 ± 0.01) % in the central 25% of the suspended membrane. The errors were calculated by taking the standard deviation from the mean of the strain values in each specified region. Although no profile can be directly ascertained from the in-plane profile shown in Figure 8.1, it is safe to assume that the in-plane strain varies with the out-of-plane strain according to

$$\varepsilon_{||} = \frac{-2C_{12}}{C_{11}}\varepsilon_{\perp}$$ Equation 8.2

where C_{12} and C_{12} are the elastic constants of 3C-SiC, for the central region of the membrane, which will exhibit biaxial strain. This implies that upon suspension the membrane itself undergoes partial relaxation from residual tensile strain. This result is in agreement with those found in literature using μ-Raman strain mapping techniques [182, 183].

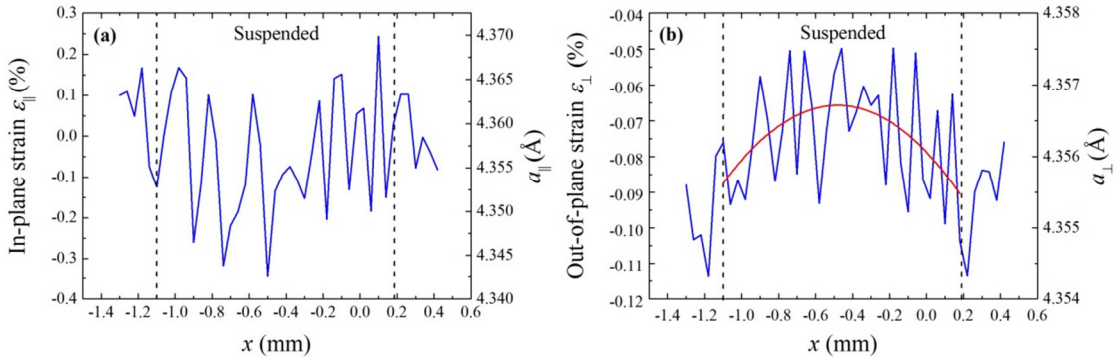

Figure 8.1 In-plane (a) and out-of-plane (b) strain profiles across the centre of the 3C-SiC membrane calculated from tilt corrected (115) RSMs. The borders of the membrane are highlighted by the locations of the dashed lines.

The variation of epilayer tilt was mapped over the corner of the membrane by acquiring symmetric (004) RSMs using a piezo scan. In this case, the tilt is defined as the variation of the crystalline orientation of a layer relative to itself. For this, a reference point was taken on the bulk region of the 3C-SiC/Si and defined to have a tilt of zero. The tilt variation of the Si and 3C-SiC can be seen in Figure 8.2. The tilt map of the 3C-SiC epilayer is again dominated by noise, a result of the high density of stacking faults in the crystal which dramatically broadens the 3C-SiC Bragg peak in $q_{||}$. The tilt map of the Si, however, shows a distinct variation at the border of the membrane. Assuming that the 3C-SiC epilayer remains bound to the Si over this region, this would imply that the 3C-SiC must also exhibit the same variation in tilt which would cause the shear strain found at the undercut of the Si substrate [182]. As Raman measurements neglect crystalline tilt, this effect can easily be misinterpreted as an increase in tensile strain simply by mapping Raman peak shift. A similar effect has been observed at the edges of Ge membranes and used to justify why membranes undergoes a slight increase in tensile strain [185]. In the case of 3C-SiC, however, it would appear the removal of the

underlying Si substrate dominates in removing the tensile strain brought about by wafer bow, which explains why the majority of the suspended 3C-SiC exhibits strain relaxation while edge effects can induce a localised increase in shear strain caused by crystalline tilt.

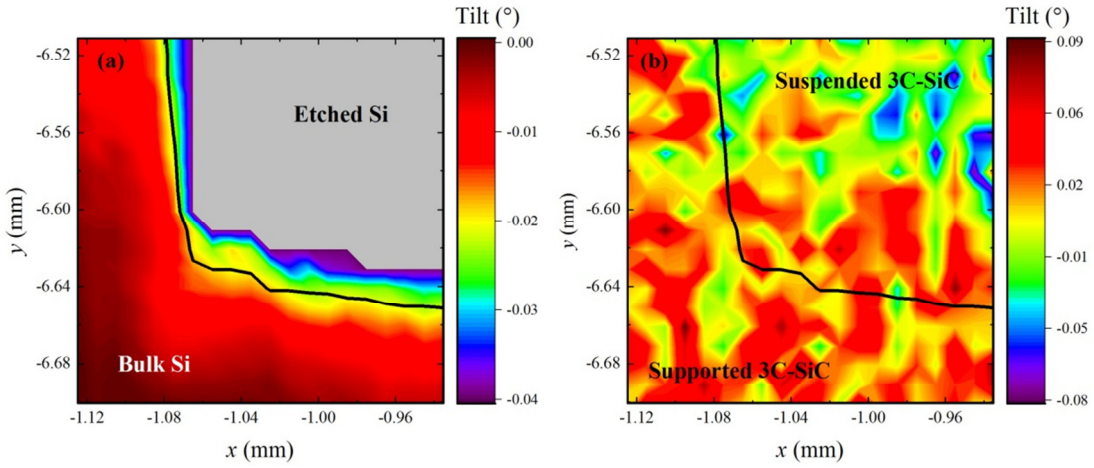

Figure 8.2 The tilt of the underlying Si (a) and the 3C-SiC epilayer (b) at the corner of the membrane, calculated from (004) RSMs. The tilt is defined as the orientation of a crystalline layer relative to itself, for each layer (3C-SiC and Si) the reference point was taken at (-1.125, -6.701) with the tilt at this point defined as zero. The black line indicates the point at which the Si Bragg peak intensity has dropped by 50%, and is defined as the corner of the membrane.

Discussions

The micro X-ray diffraction technique is a useful tool for measuring the strain and tilt of 3C-SiC suspended membranes, however, the poor material quality of heteroepitaxially grown 3C-SiC can make it more difficult to map these parameters compared to higher quality materials such as Ge or $Si_{1-y}C_y$. The strain relaxation observed across the 3C-SiC membrane is in agreement with data from other investigation using Raman shift measurements and other techniques [182] [186]. The results presented have revealed further information about the origin of edge effects in 3C-SiC membranes, suggesting that increases in shear strains commonly observed at the edges of suspended structures is due to slight distortions in the tilt of the 3C-SiC/Si.

Further information can be found in the related publication to this research here [187].

8.1.2 Annealing of 3C-SiC membranes

The annealing of semiconductors is a well-known method for activating dopants and restoring crystallinity after the damage induced by ion implantation. Although the annealing of 3C-SiC is limited to melting point of the underlying Si substrate, many studies have shown that annealing even at temperatures of 1350 °C can at least partially recover the 3C-SiC crystallinity [163, 188]. Some studies have investigated the effect of laser pulsed annealing on the stacking faults within 3C-SiC epilayers and suspended membranes. Results have shown that temperatures of 1627 °C can cause a narrowing of the 3C-SiC transverse optic Raman peak which is attributed to the annealing of stacking faults [189, 190]. While these studies achieve temperatures beyond the melting point of Si, they rely only on localized heating of areas on the micron scale. To date, no attempt has been made to map the effect of thermal annealing on the residual strain and crystalline quality of suspended 3C-SiC membranes.

The aim of this investigation was to determine the effects of continual high temperature annealing on a suspended 3C-SiC membrane to simulate the operation of a 3C-SiC MEMS device operating at the maximum possible temperature, as limited by the melting point of the Si substrate. Being released from the underlying substrate, the high temperature may be able to manipulate the crystal structure of the suspended 3C-SiC. Alternatively, the differences in thermal expansion coefficients between the Si frame and suspended 3C-SiC may cause irreversible damage to the membrane. The crystal quality and strain state of the suspended membrane was measured before and after high temperature thermal annealing by the use of synchrotron based μ-XRD as previously discussed.

Suspended square membranes were fabricated from 3C-SiC grown in an LPE-ACIS M8 RP-CVD as described previously. After the removal of the masking ProTEK PSB photoresist and thorough cleaning in a piranha etch process, one set of membranes was annealed in the presence of Ar at a temperature of 1350 °C for 30 minutes within the LPE ACIS M8 RP-CVD system, while another set of membranes were left unannealed as the control batch.

Symmetric (004) RSMs were acquired at various points across an as-grown and annealed 1.3 mm × 1.3 mm 3C-SiC membrane so as to map the Si and 3C-SiC Bragg peaks in a line scan profile through the centre of the membranes and onto the supporting bulk. The FWHM of the 3C-SiC and Si (004) Bragg peaks are shown as functions of

real space in Figure 8.3. The FWHM of the (004) 3C-SiC peak for both $q_{\parallel}$ and $q_{\perp}$ is the same for the suspended and supported 3C-SiC. The broadened peak along $q_{\parallel}$ (i.e. along [110]) is a result of diffuse scattering from the stacking faults present in the 3C-SiC layer [191]. The fact that the FWHM along $q_{\parallel}$ is identical for the supported and suspended 3C-SiC confirms that there is no reduction in number of stacking faults or mosaicity in the layer upon suspension (either due to slight changes in strain or due to the possibility that the faults may etch away more readily than the bulk material). Likewise there is no reduction in the stacking fault density upon thermal annealing of the membrane. This confirms that the suspended 3C-SiC crystal quality is unaffected by the annealing process.

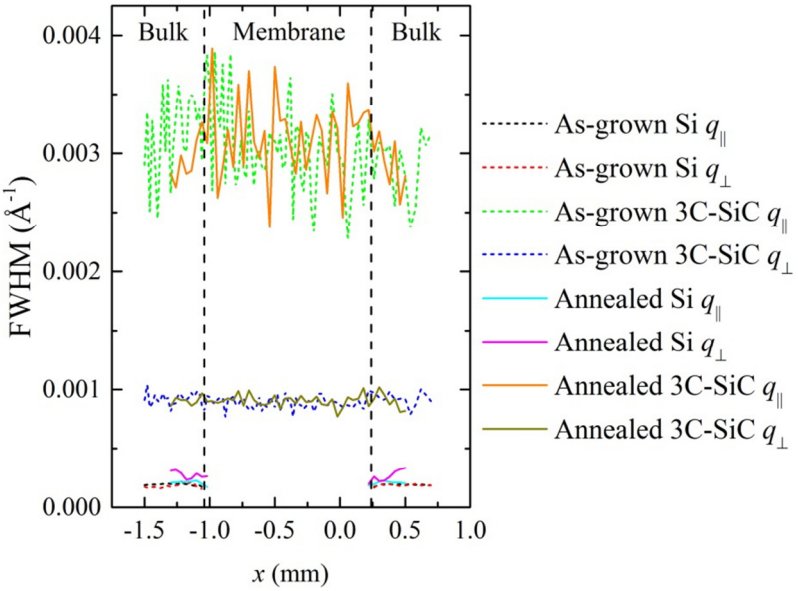

Figure 8.3 FWHM of Si and 3C-SiC Bragg peaks across the centre of an as-grown and annealed suspended membrane.

It was hypothesized that the crystal quality may improve in the suspended 3C-SiC region by the thermal annealing of the 3C-SiC stacking faults made possible by the release from the underlying Si substrate. While this may have provided a significant step towards the production of defect free 3C-SiC, unfortunately, this was not the case. The limited thermal budget for annealing 3C-SiC (set by the melting point of Si) could not supply enough thermal energy to cause any noticeable change in the 3C-SiC crystal structure. Instead, however, the results of this investigation have demonstrated the thermal stability of suspended 3C-SiC membranes and their capability to withstand temperatures up to the melting point of Si without any variation in the crystal structure

of either the suspended 3C-SiC or underlying substrate when returned back to room temperature. The out-of-plane strain of an annealed and unannealed 3C-SiC/Si membrane was measured through the acquisition of (004) symmetric RSMs, see Figure 8.4.

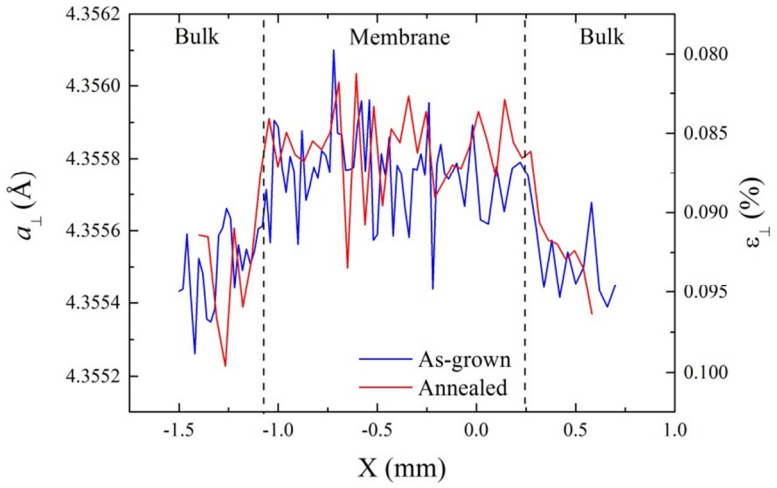

Figure 8.4 The tilt corrected out-of-plane lattice parameters and strains of the as-grown and annealed suspended 3C-SiC as functions of position through the centre of the square membranes. The averaged out-of-plane strains across the as-grown and annealed membranes are (-0.088 ± 0.003) % and (-0.087 ± 0.003) % respectively.

Again as with the FWHM of the Bragg peaks, no discernible difference in the strain relaxation can be observed between the as-grown and thermally annealed 3C-SiC/Si membrane with the strain values almost in complete agreement.

Discussions

MEMS gas and pressure sensors depend on physical variations within suspended 3C-SiC beams or membranes. While these devices can be calibrated to different operating conditions, to be reliable their physical properties must remain unchanged after being subjected to high temperatures. The results of this investigation have shown that both the crystal quality and strain state of the suspended 3C-SiC membranes are unaffected by temperatures up to the melting point of Si. The 3C-SiC epilayers used in this study are reasonably thick (~5 μm), while many MEMS structures use 3C-SiC layers of the order of microns [103, 192, 193], other applications may require significantly thinner

material which was not assessed in this investigation. The effect of high temperature is therefore uncertain on thinner 3C-SiC layers and is an area for further investigation.

8.2 Strain Mapping of Suspended 3C-SiC Microwires

For this investigation, the commercially purchased 3C-SiC/Si (001) heterostructure was used to fabricate suspended microwires and the strain state across the structures was measured using the μ-XRD technique described previously and compared to that of micro-Raman (μ-Raman) shift mapping. As the commercial 3C-SiC epilayer was monocrystalline throughout and possessed a significantly smoother surface, the X-ray Bragg peaks should be sharper which will reduce the uncertainty in their positions and consequently the noise in the strain maps. Suspended microwires were fabricated using topside lithography, dry etching and wet etching processes, see Figure 8.5.

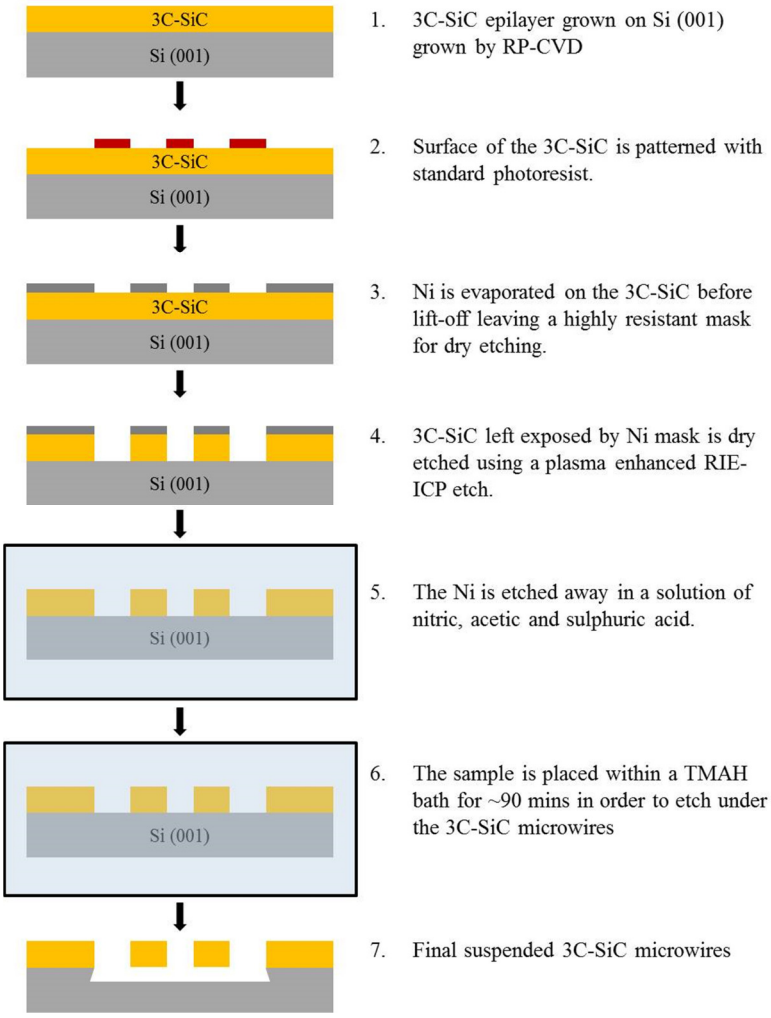

Figure 8.5 Fabrication process of suspended 3C-SiC microwires.

An SEM image of the resulting suspended 3C-SiC microwires can be seen in Figure 8.6.

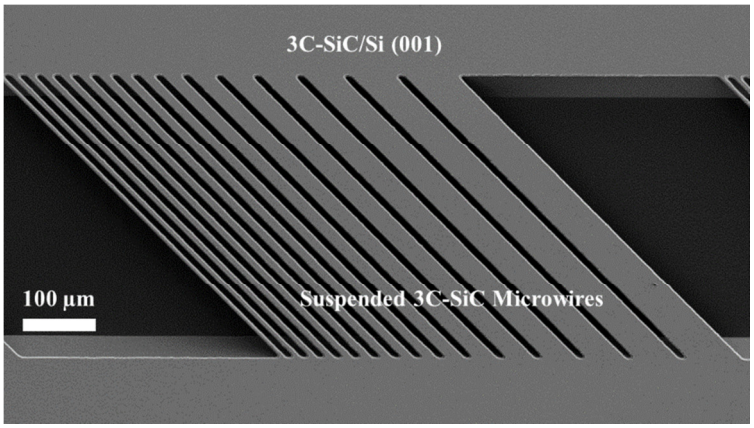

Figure 8.6 Secondary electron SEM image of suspended 3C-SiC microwires.

8.2.1 Mapping Strain by µ-XRD

The residual strain of the microwires was again mapped using micro µ-XRD on beamline B16 at the Diamond Light Source synchrotron using the same procedure as discussed above. The tilt and out-of-plane lattice constants of 3C-SiC suspended microwires were calculated from symmetrical (004) RSMs while the in-plane lattice constants were extracted from asymmetrical (115) RSMs.

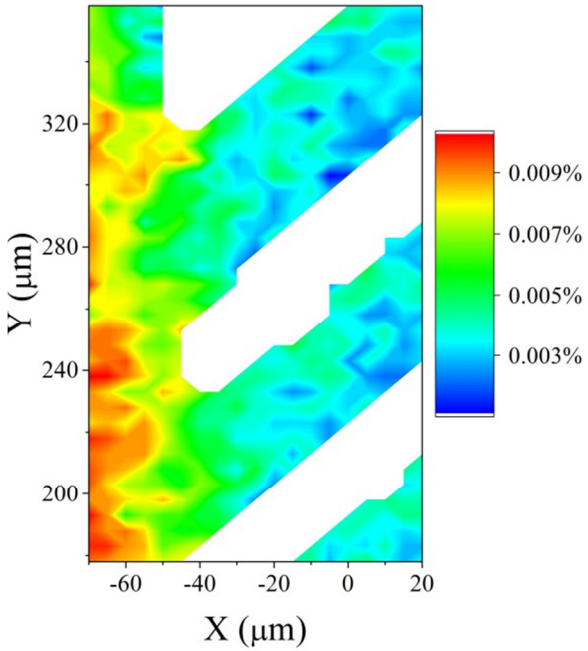

Figure 8.7 In-plane tensile strain map of the 3C-SiC suspended microwires using µ-XRD.

While the commercial 3C-SiC epilayer is under only small levels of residual tensile strain (~0.01%) the strain map in Figure 8.7 shows almost full relaxation from this value.

8.2.2 Mapping Strain by μ-Raman

For comparison, a map of the characteristic 3C-SiC LO Raman peak shift was acquired on the suspended microwires using a 442 nm laser excitation source on a Renishaw inVia Reflex Raman Microscope with automated stage. The peak positions were calibrated to the position of the first order Si Raman peak. The Raman shift was converted into an approximate value of the residual tensile strain at each point on the wires using the empirical expressions derived by Olego and Cardona [194].

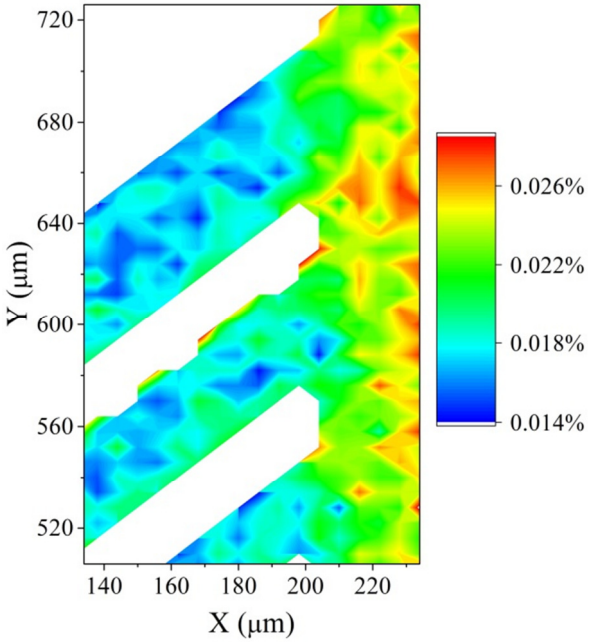

Figure 8.8 In-plane tensile strain map of 3C-SiC microwires using the shift of the 3C-SiC LO Raman peak, the positions of X and Y are arbitrary and do not correspond to a certain location in Figure 8.7.

As with the results from μ-XRD, the tensile strain is seen to decrease in the suspended microwires as the epilayer is allowed to relax without the presence of the underlying Si substrate. A comparison of the strain variation across the microwire as measured by the two techniques is shown in Figure 8.9.

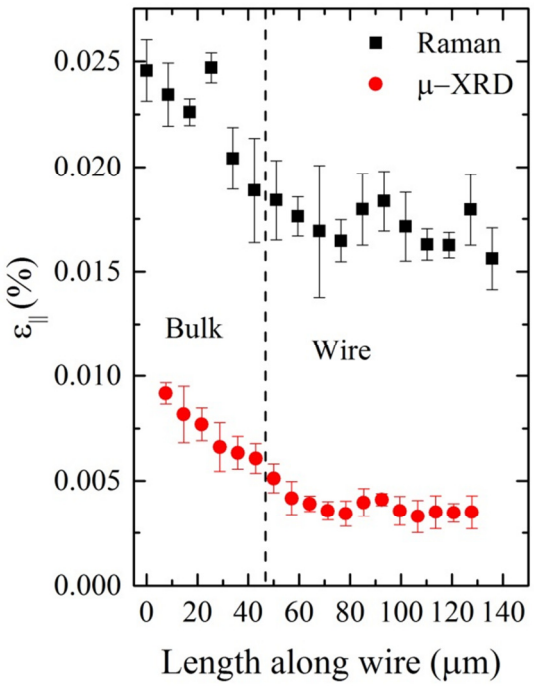

Figure 8.9 Strain profiles along an equivalent suspended 3C-SiC microwire. The points are determined by taking the mean strain across the central 50% portion of the wire at each point along its length. The uncertainties are derived from the standard deviation of these strain values from the mean.

Similar levels of strain relaxation can be observed in both the μ-XRD and Raman shift maps. However, the strain profiles along the microwires shown in Figure 8.9 demonstrate a wider spread of data and greater uncertainties observed with Raman shift. Another point to note is that the equations used to calculate strain from Raman shift introduce an uncertainty of ~24% for a shift of 1 cm^{-1} (typical of the shifts observed in 3C-SiC residual strain relaxation). This justifies why it is uncommon to find values of strain relaxation explicitly quoted in literature, instead commenting solely on the degree of Raman shift. The discrepancy between the absolute values of strain between the strain profiles is possibly due to the error introduced during strain calculations or by the temperature dependence of the Raman peaks being affected by localized heating of the sample [190]. These effects can be eliminated in μ-XRD measurements because firstly the lattice parameters, and hence strain, are obtained directly from the positions of the Bragg peaks and secondly the heating caused by the X-rays is negligible. In addition, the Si Bragg peaks are simultaneously measured in the RSMs which can be calibrated to the well-known lattice constant of Si.

Discussions

Suspended membranes and micro wires can form the basis of a number of MEMS device structures such as pressure, temperature or gas flow sensors. Due to its resistance to etching chemicals, 3C-SiC is an ideal material for these structures and therefore understanding the effects suspending the 3C-SiC epilayers is crucial to the production of reliable devices.

The sensitivity of μ-XRD mapping is superior in the case of the measurements presented, although adjusting counting times for each technique would improve this. While Raman is a fast and convenient method of mapping the variation of strain in suspended 3C-SiC structures, it cannot provide a direct measurement of strain from lattice parameters as can be achieved in μ-XRD. As such, these techniques are complimentary for the mapping of residual strain in 3C-SiC.

For further information regarding this research please consult the related publication [195].

8.3 Optical Transmission Through 3C-SiC

Ultraviolet (UV) photodetectors have many applications in the industrial sector, environmental sensing and safety. UV sensing can offer better efficiency in curing and sterilization processes as well as protect humans from the damaging effects of prolonged exposure to radiation from the sun. Low-cost UV sensors would satisfy a large demand from various sectors. As such, Si is the material of choice for UV photodiodes as it offer low-cost and volume manufacturing, however, Si detectors are limited in operating temperature and can be degraded by constant exposure to UV radiation, decreasing device sensitivity and increasing noise [196, 197].

SiC is an excellent material for UV photodetectors in terms of its ability to operate in harsh environments and withstand the damaging effects of ionizing radiation [198, 199]. All polytypes of SiC exhibit an indirect bandgap, however, for bulk materials this has little impact as optical absorption will occur as long as the incident light exceeds this bandgap. However, 3C-SiC can be heteroepitaxially grown on Si substrates to very thin thicknesses which can manipulate the absorption edge. In addition, the inclusion of impurities in the epilayer can also be used to affect the absorption of UV light within semiconductor films. Tuneable photodetectors have been demonstrated with III-V

ternary alloys such as aluminium gallium nitride (AlGaN) by controlling the Al impurity concentration to manipulate the bandgap of the material [200]. However, one of the downsides to III-V based semiconductors is that they cannot be grown within Si based growth processes which means that heterogeneous integration of wide bandgap III-Vs with Si can only really be achieved using discrete devices or wafer bonding techniques. As well as offering greater flexibility to device design, 3C-SiC/Si based devices can significantly reduce the cost of UV photodiodes compared to those fabricated purely from hexagonal SiC or GaN based compounds.

Another potential application of 3C-SiC that has attracted attention in previous years is as a virtual substrate for the heteroepitaxy of the direct bandgap semiconductor GaN for LED, RF communications and power electronic applications. GaN LEDs are often fabricated using a flip-chip technique to increase heat dissipation and efficiency, in which the light is emitted from the underside of the GaN epilayers, typically through the sapphire substrate [201]. In order for 3C-SiC/Si to replace sapphire in the LED industry and minimise disruption to device architecture, it would be beneficial if the 3C-SiC was optically transparent to the emitted wavelengths from UV to green (200-550 nm). During device fabrication, the Si substrate can easily be removed by chemical wet etching while leaving the 3C-SiC epilayer intact as a protective coating for the GaN, providing it does not absorb light emitted from the GaN LED, see Figure 8.10. Even relatively thin 3C-SiC buffer layers of ~700 nm have been shown to improve LED performance by more than doubling the output intensity [202].

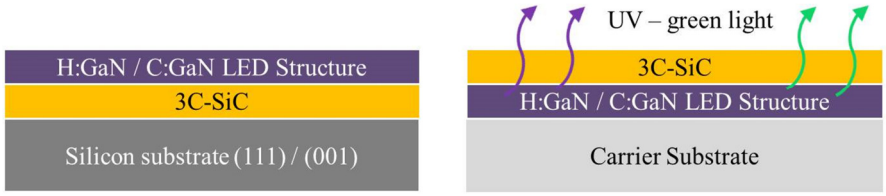

Figure 8.10 Proposed fabrication process for a GaN based LED grown on a 3C-SiC/Si heterostructure after the removal of the Si substrate.

The aim of this study was to measure the dependency of light transmission through suspended 3C-SiC membranes of varying thickness and doping. Thin 3C-SiC epilayers were grown at low temperatures by RP-CVD within an ASM Epsilon 2000 single wafer, cold wall quartz chamber system, please refer to Chapter 6.

8.3.1 Effect of Epilayer Thickness

For thickness dependency measurements, a single epilayer ~1.2 µm was grown and thinned post-growth. To reduce the thickness of the 3C-SiC membranes, the 1.2 µm thick epilayer was thinned using dry etching which allowed more parameters of the epilayers such as doping and surface roughness to be kept constant, opposed to growing multiple layers. Optical transmission measurements were carried out through suspended 3C-SiC square membranes. The use of suspended membranes allows true absorption measurements of suspended epilayers to be made without having to consider the impact of the epilayer/substrate interface and Si substrate itself. Transmission measurements were carried out at room-temperature by placing the suspended membranes in the path of a beam of light produced by a tungsten and deuterium lamp with wavelength of 200 nm to 1000 nm while complimentary reflectance measurements were carried out using a multi fibred cable, see Figure 8.11.

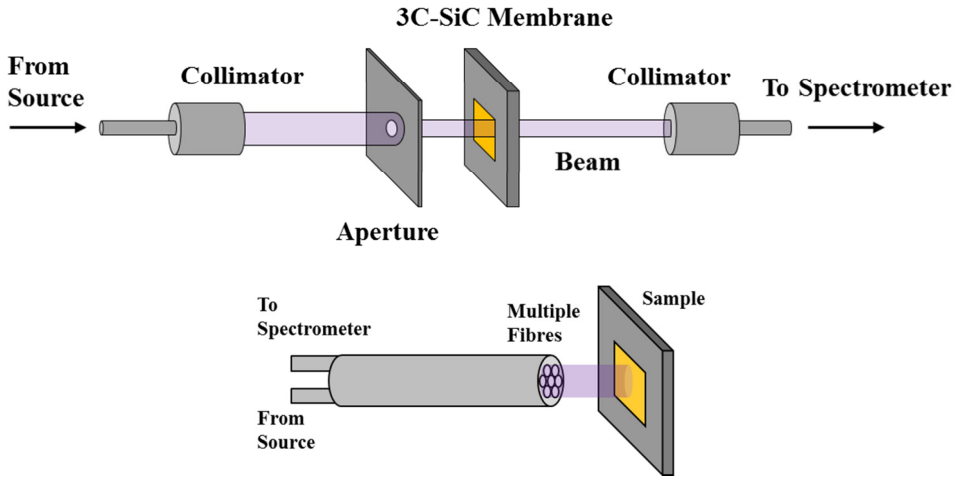

Figure 8.11 Top - Experimental set-up for transmission measurements. Collimators were used to focus the beam through an aperture which limited the beam spot size such that it could pass through a 3C-SiC membrane. Bottom – Experimental set-up for reflectivity measurements. A multi fibred optical cable was used to both transmit and receive the beam.

The optical transmission through the membranes leads to fringes due to the interference of light within the epilayer with constructive fringes occurring at positions defined by

$$m\lambda = 2n_{3C-SiC}(\lambda)d \qquad \text{Equation 8.3}$$

where m is an integer value, $n_{3C\text{-}SiC}$ (λ) is the refractive index of light through 3C-SiC for a specific wavelength (λ) and d is the thickness of the film. Mapping the positions of these fringes allows one to extract thickness, assuming refractive index of the 3C-SiC is

known over the wavelength range. The transmission of light was measured through membranes of thicknesses ranging from 130 nm to 1270 nm, see Figure 8.12.

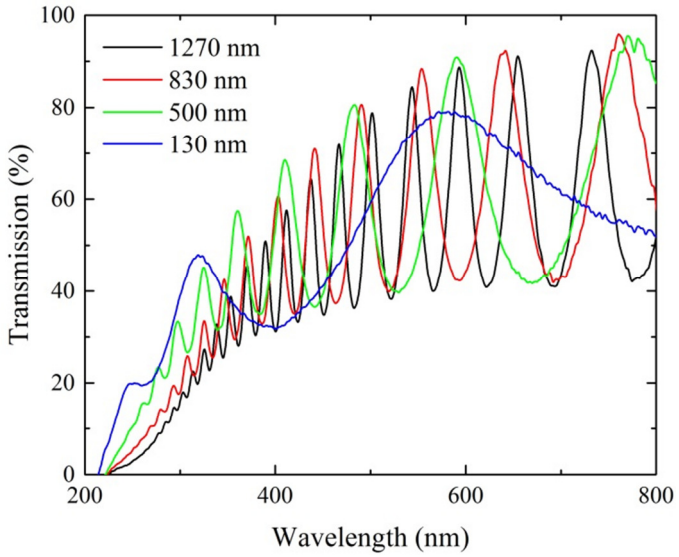

Figure 8.12 Selected room temperature absorption spectra of 3C-SiC epilayers of thicknesses in the range of 130 – 1270 nm.

The variation in the transmission at low wavelengths is shown in Figure 8.13, where the wavelength at which <5% of light is transmitted has been measured as a function of the membrane thickness. The value of 5% was chosen as certain thin samples exhibited complete absorption below the measurement threshold of the Si diode used in the optical measurements.

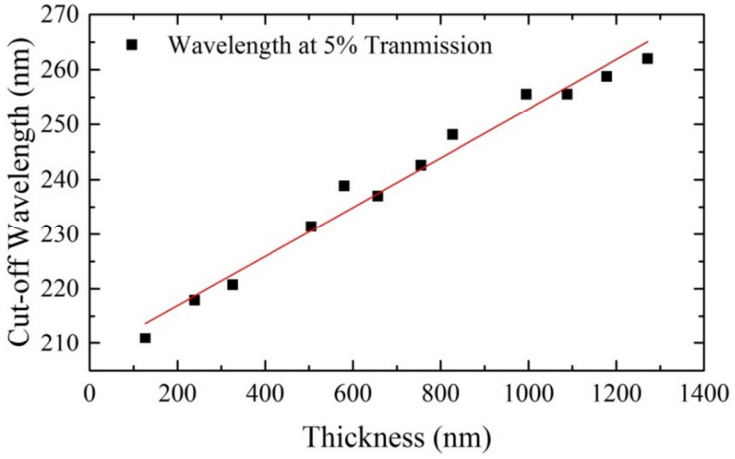

Figure 8.13 Wavelength at which below 5% of incident light is transmitted as a function of 3C-SiC thickness.

An almost linear dependency is observed with the defined 5% cut-off wavelength implying that the absorption of light at these wavelengths is dominated by phonon assisted transitions which depend on the interaction volume of the thin film, hence the transmission decreases with increasing thickness. The reflectance spectrum was obtained for the sample of ~580 nm thickness, see Figure 8.14.

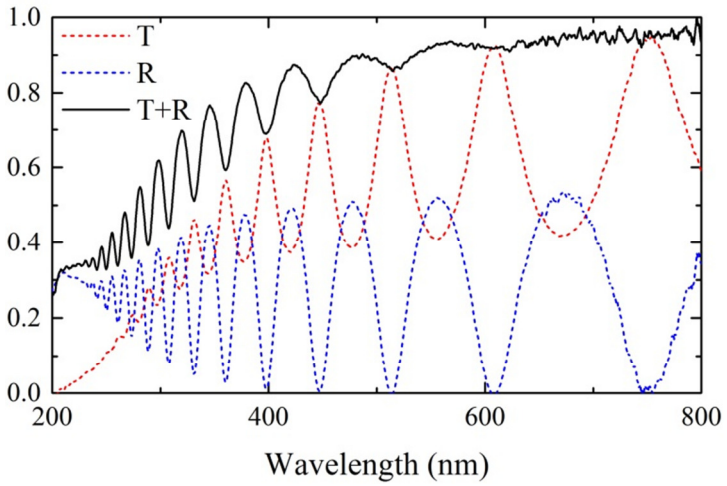

Figure 8.14 Transmission (*T*) and reflectance (*R*) coefficients of a 580 nm thick 3C-SiC suspended membrane.

Reflectance fringes align well with those from the transmission signal. As the wavelength reduces, the reflectance signal decreases as it becomes dominated only by the initial reflectance off the epilayer surface, whereas at longer wavelengths the reflectance includes the signal due to reflection off the rear interface. The reflectance coefficient decreases to 0.3 at 225 nm wavelength which corresponds to a 3C-SiC refractive index of 3.58 using the Fresnel equation for reflectance given by

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2. \qquad \text{Equation 8.4}$$

There is a slight error between the two plots for *T* and *R* as the fringes do not eliminate entirely when the coefficients are added which is likely due to the fact that both coefficients were measured using separate measurements. It is also worth noting that the total light measured at long wavelengths does not add up to 100% indicating that light is either being scattered by the surface of the epilayers or that defects within the 3C-SiC crystal are enabling sub-gap absorption.

The total amount of light not absorbed (or scattered) by the sample is given by T+R and can be approximated by

$$T + R = e^{-\alpha t}$$ Equation 8.5

where t is the thickness of the sample. From this, the penetration depth (δ) can also be calculated using

$$\delta = \frac{1}{\alpha}$$ Equation 8.6

which is plotted in Figure 8.15.

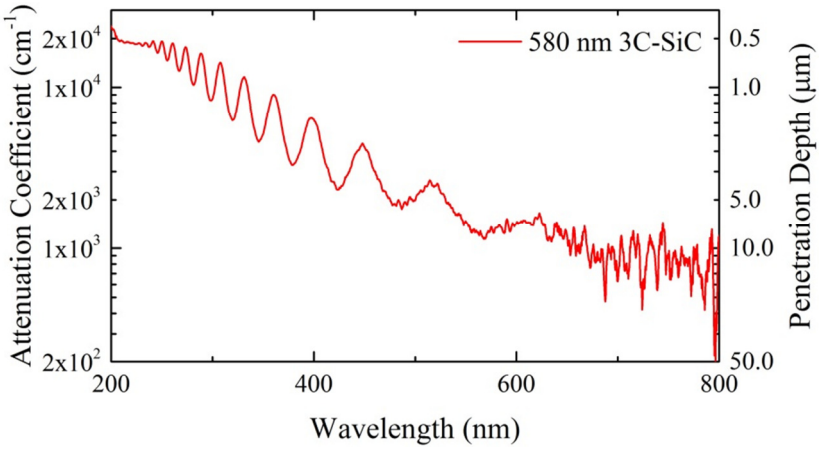

Figure 8.15 The attenuation coefficient and penetration depth for the 580 nm thick 3C-SiC as a function of wavelength.

The attenuation coefficient is valid only for shorter wavelengths where interference fringes are not observed as Equation 8.5 does not take into account any light that is reflected back off the rear interface of the membrane which leads to an overestimation of light absorption.

8.3.2 Effect of Epilayer Doping

Transmission spectra were also obtained for heterostructures with high levels of P doping and a noticeable shift in the spectra at low wavelengths can be observed indicating that even the presence of a thin ~50 nm doped 3C-SiC epilayer within a larger heterostructure can have an effect on the absorption of light within the layer, see Figure 8.16. Samples equivalent to P1, P2 and P3 from Chapter 7 with impurity concentrations of approximately 5×10^{20} cm^{-3}, 1×10^{20} cm^{-3} and 1×10^{19} cm^{-3} respectively, were used for this study. The influence of doping is an important factor to be considered when designing a photosensitive 3C-SiC based device and could potentially influence the operation of other devices where highly doped regions of 3C-SiC are introduced to reduce contact resistance.

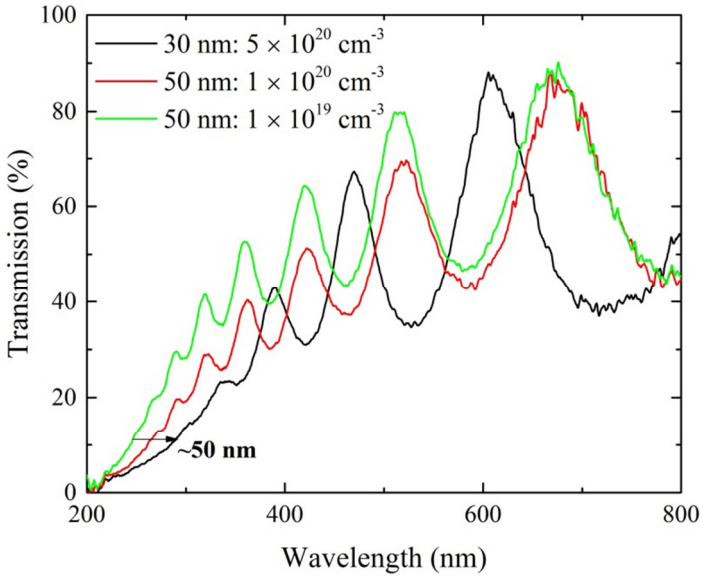

Figure 8.16 Transmission of light through 3C-SiC samples with capping layers of varying P doping concentrations. The thickness of the capping layers is also stated.

A slight increase in absorption at lower wavelengths can be observed within increasing doping level. The origin of this cannot be ascertained using the measurements carried out in this study. The incorporation of high levels of n-type dopants has been modelled to reduce the bandgap of 3C-SiC by ~200 meV at doping levels of 10^{20} cm^{-3} which would increase optical absorption [11]. Alternatively, the presence of P in the band structure could offer intermediate states for electron excitation. As P is a shallow impurity in 3C-SiC, typically at around 48 meV from the conduction band the effect would only be subtle as shown in the presented results [12]. Either of these effects could explain the shift in the transmission data.

Discussions

The results of this investigation demonstrate that 3C-SiC may offer a route to tuneable UV photodetectors or can act as a protective coating on UV susceptible devices by simply manipulating the thickness and doping profile of the material. As a potential virtual substrate for GaN growth, traditional flip-chip fabrication techniques will need to be altered for the growth of hexagonal GaN on (111) orientated material as the 3C-SiC will not transmit sufficient UV or blue light and cannot be selectively removed from the GaN surface through chemical etching. However, the results of this study show that if buffer layers of sufficiently thin (<500 nm) 3C-SiC can be used to grow high quality cubic GaN for green LED applications, then the 3C-SiC may not necessarily

need to be removed from the surface of the LED device and can in fact offer a highly resistive coating to the device structures and could be later manipulated to enhance the emission of light from the GaN based LEDs.

Further information on this research can be found in the recently published journal article.

8.4 Strain Mapping of $Si_{1-y}C_y$ Suspended Membranes

8.4.1 Introduction

One of the main applications of $Si_{1-y}C_y$ epilayers is in strain engineering for reducing contact resistance or manipulating the mobility of MOSFET channels. However, as described in Chapter 5, it is very challenging to increase the C content of $Si_{1-y}C_y$ layers beyond around 1.5% without inducing significant densities of defects and amorphous inclusions during growth. The only way around this issue is to use more reactive and expensive Si and C based precursors or resort to non-conventional growth methods. The strain of a $Si_{1-y}C_y$ epilayer is related to the C content by Vegard's Law (Equation 5.3), as such, the issues involved with growth make it difficult to increase the strain within epilayers.

Suspended membranes have already demonstrated various advantages over bulk material in Ge grown on Si such as reduced misfit dislocations, slight enhancements of tensile strain as well as the potential for use as growth platforms for further epitaxy [203]. $Si_{1-y}C_y$ membranes may offer suspended growth platforms for 3C-SiC, providing a thin, compliant and crystalline template for further heteroepitaxy. One of the major issues when growing 3C-SiC directly on Si substrates is the out diffusion of Si into the growth of the 3C-SiC, leading to the formation of voids in the Si at the interface. Growing on $Si_{1-y}C_y$ suspended growth platforms should avoid this issue as the diffusion of material through $Si_{1-y}C_y$ is significantly reduced when compared to pure Si [111].

For $Si_{1-y}C_y$ membranes to be of use as growth platforms they must remain flat upon suspension, ideally without the edge effects that have previously been observed in suspended Ge membranes [185]. The strain state and crystalline quality of suspended $Si_{1-y}C_y$ must also be understood in order to determine its suitability as a suspended growth platform for 3C-SiC. The aims of this investigation were to demonstrate the fabrication of $Si_{1-y}C_y$ membranes and assess their material properties through strain mapping. The fabrication of $Si_{1-y}C_y$ membranes is a challenge in itself as the physical

properties of $Si_{1-y}C_y$ are very similar to that of Si and as such it is not etch resistant to typical alkaline etchants of Si. Once fabricated, the strain and tilt of the membranes were assessed by XRD carried out at the Diamond Light Source synchrotron using an X-ray spot size of a few microns in size.

8.4.2 Heterostructure Growth

For this study, a heterostructure was grown that consisted of a ~20 nm thick $Si_{1-y}C_y$ epilayer. The thickness of the $Si_{1-y}C_y$ epilayer was kept low as thinner layers have been shown to suffer from fewer surface defects, see Chapter 5. Unlike 3C-SiC and Ge, $Si_{1-y}C_y$ is not resistant to standard alkaline Si wet etchants such KOH and TMAH and therefore a suitable etch stop layer must be included in the heterostructure. An alloy of silicon boron ($Si_{1-x}B_x$) was chosen for this purpose as its lattice parameter reduces with increasing B content, as with $Si_{1-y}C_y$ and has been shown to resist the etching effect of TMAH [204]. $Si_{1-y}C_y$ layers were epitaxially grown on top of epitaxial $Si_{1-x}B_x$ layers on 100 mm diameter, 525 µm thick Si (001) substrates within the ASM Epsilon 2000 RP-CVD system. The $Si_{1-x}B_x$ layer was grown using diborane (B_2H_6) and disilane (Si_2H_6) precursors at 700 °C then immediately followed by the growth of the $Si_{1-y}C_y$ epilayers using disilane and TMS precursors at 550 °C. To act as a suitable etch stop a slightly thicker $Si_{1-x}B_x$ layer was grown at ~50 nm, see Figure 8.17.

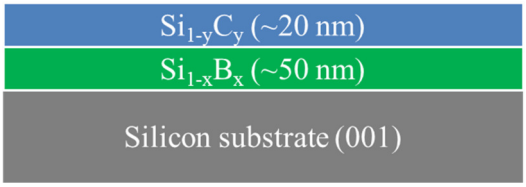

Figure 8.17 Cross-sectional schematic of epitaxially grown heterostructure.

8.4.3 Material Characterisation

Before membrane fabrication the heterostructures were characterised using a range of in-house techniques to assess the crystalline quality and strain state.

Composition and Crystal Structure

A coupled scan showed that the inclusion of the $Si_{1-x}B_x$ buffer layer had little impact on the crystallinity of the $Si_{1-y}C_y$ epilayer as both (004) Bragg peaks can be seen from each layer, see Figure 8.18. The broadness of the $Si_{1-y}C_y$ epilayer Bragg peak in the scan is a

result of its low thickness. Thickness fringes can be seen in the plot also, however, the limited number of peaks visible makes it difficult to resolve the fringes due to each epilayer individually and cannot be used for thickness calibration.

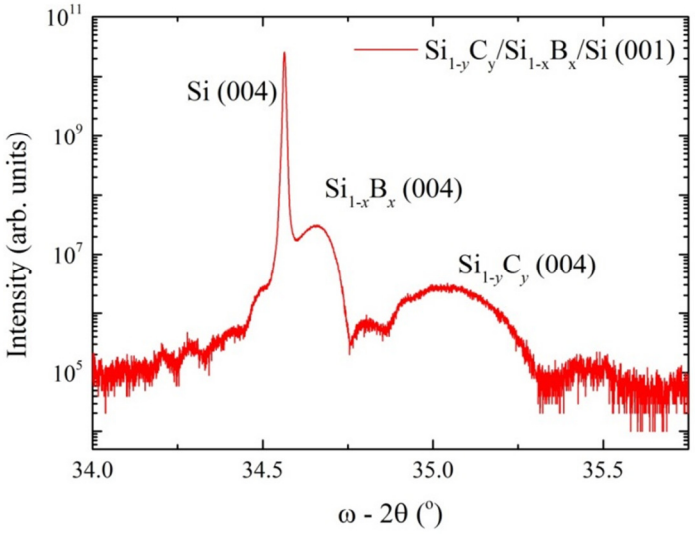

Figure 8.18 ω-2θ coupled scan of the $Si_{1-y}C_y/Si_{1-x}B_x/Si$ (001) heterostructure. Bragg peaks associated with each epilayer can be distinguished. The interference pattern of the thickness fringes resulting from each layer can also be seen.

Symmetric and asymmetric RSMs were performed on the heterostructure using in-house HR-XRD to assess the tilt and strain state of the $Si_{1-y}C_y$ and $Si_{1-x}B_x$ epilayer, see Figure 8.19.

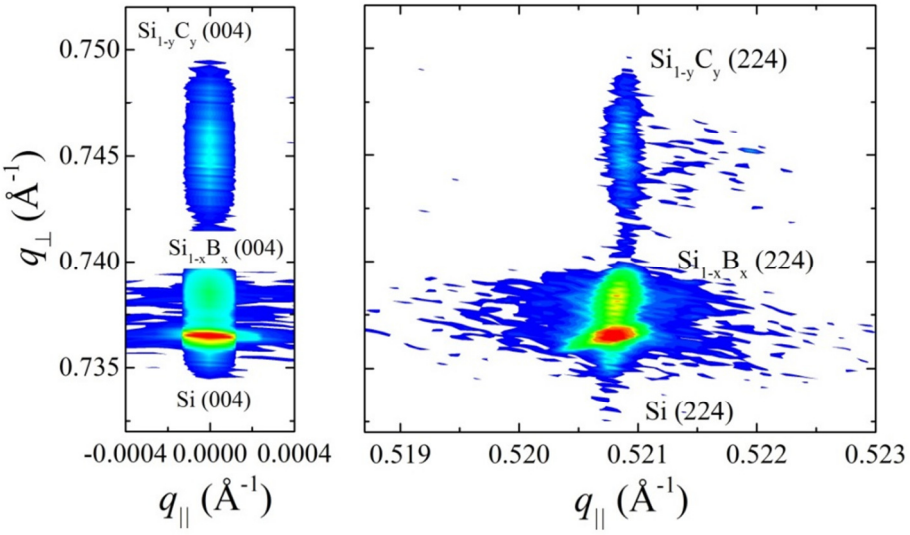

Figure 8.19 : Lab based RSMs around the (004) (left) and (224) (right) reflections. The $Si_{1-x}B_x$ and $Si_{1-y}C_y$ epilayers are tilt free and under 0.125% and 0.677% tensile strain respectively. The C content of the $Si_{1-y}C_y$ was calculated to be 1.5%.

The epilayers were found to be free of tilt and almost fully tensile strained to the Si substrate with strain values of 0.125% and 0.677% for the $Si_{1-x}B_x$ and $Si_{1-y}C_y$ epilayer respectively. The C content in the $Si_{1-y}C_y$ is calculated to be 1.5% while the B content (N_B) in the $Si_{1-x}B_x$ was found to be approximately 0.5% using

$$\frac{\Delta a}{a_{Si}} = \beta N_B \qquad \text{Equation 8.7}$$

where a lattice contraction coefficient (β) of 5×10^{-24} cm^{-3} was used [205].

An X-TEM micrograph is shown in Figure 8.20, from which the thicknesses of the $Si_{1-x}B_x$ and $Si_{1-y}C_y$ epilayers were measured. Both epilayers are crystalline, however, amorphous hillocks can be observed in the $Si_{1-y}C_y$ epilayer resulting from the oversaturation of C. The thickness of the $Si_{1-y}C_y$ is measured to be (18 ± 1) nm while the $Si_{1-x}B_x$ is measured to be (52 ± 3) nm.

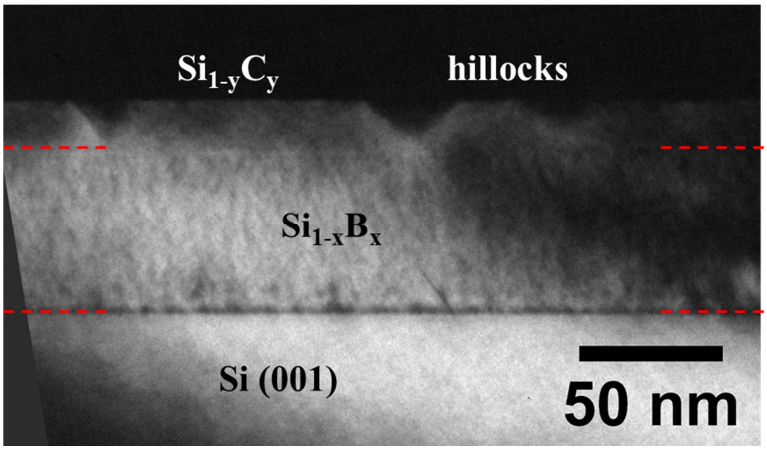

Figure 8.20 DF (004) cross-sectional TEM micrograph of the heterostructure, highlighting the crystallinity of the epilayers. The interfaces between the epilayers and substrate have been partially highlighted for clarity.

Surface Morphology

The surface of the $Si_{1-y}C_y$ epilayer was found to be rough due to the presence of hillocks on the surface. While the size of these defects was small their density was found to be very high on the heterostructure surface possibly due to the presence of the intermediate $Si_{1-x}B_x$ epilayer, see Figure 8.21.

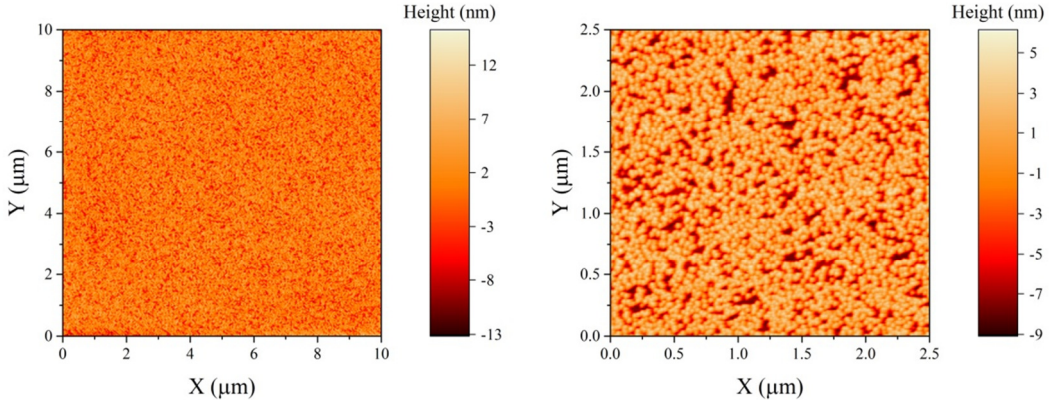

Figure 8.21 AFM surface roughness scans of the heterostructure with a surface roughness of ~2.8 nm. The scans were taken using contact mode AFM.

8.4.4 Membrane Fabrication

The suspended $Si_{1-y}C_y/Si_{1-x}B_x$ membrane is fabricated in several stages. Windows, over which the $Si_{1-y}C_y/Si_{1-x}B_x$ membranes were suspended, were first defined by optical lithography on the underside of the Si (001) substrate, using an alkaline etch resistant ProTEK PSB photoresist. The $Si_{1-y}C_y$ surface was also protected by this photoresist. Then, the samples were etched in a 25%wt. TMAH bath at 90 °C for approximately 16 hours in order to etch through the entire Si substrate. The TMAH selectively etches the {001} Si planes whereas the {111} planes are etch resistant. It is necessary to protect the $Si_{1-y}C_y$ layer as it is otherwise also etched away in the TMAH bath. The fabrication of the suspended $Si_{1-y}C_y$ is only possible due to it being masked by the photoresist on the top side and the etch-resistant $Si_{1-x}B_x$ on the underside. The $Si_{1-y}C_y/Si_{1-x}B_x$ membrane remains under tensile strain as it fixed to the $Si_{1-y}C_y/Si_{1-x}B_x$ on Si (001) frame. Finally, the samples were treated in a piranha etch (4:1, concentrated sulphuric acid (H_2SO_4) to 30%wt. H_2O_2) for ~5 mins to remove the ProTEK photoresist followed by a 2.5 % HF dip for 30 s to remove any formed oxide on the $Si_{1-y}C_y$ surface. See Figure 8.22 for a diagram of the full process.

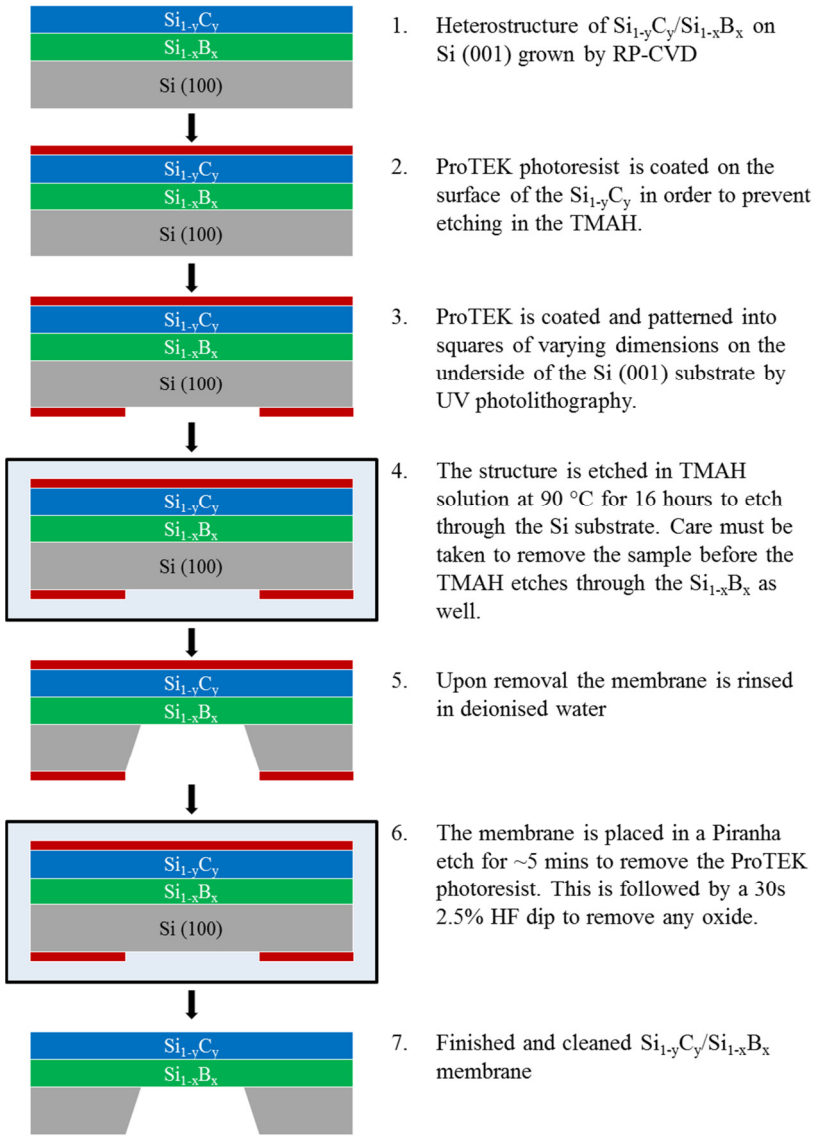

Figure 8.22 $Si_{1-y}C_y/Si_{1-x}B_x$ membrane fabrication process.

Square membranes of varying sizes were fabricated using the process shown in Figure 8.22 by varying the size of the squares patterned on the backside of the Si substrate. An optical image of three membranes (stitched from multiple images) can be seen in Figure 8.23. The red/purple colour of the membranes is a result of the interference of light from the epilayers in the membrane structure. The membranes are transparent as the semiconductor epilayers are thin and have indirect bandgaps, allowing certain low wavelengths to pass through without interacting.

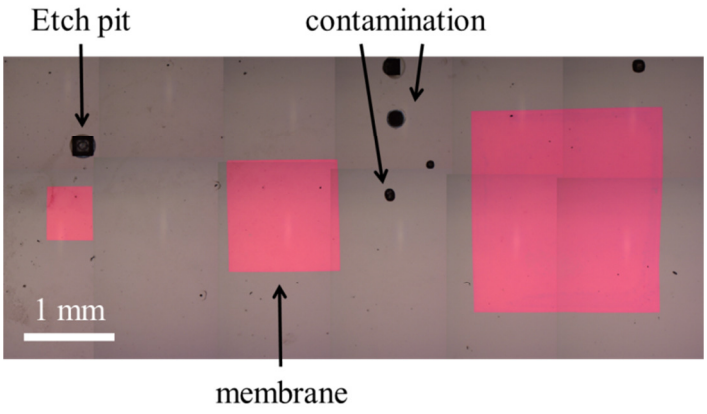

Figure 8.23 Optical image of suspended $Si_{1-y}C_y/Si_{1-x}B_x/Si$ membranes.

While the membranes were cleaned with a piranha etch, there is still some contamination (remnants of ProTEK photoresist) on the surface of the sample, although the worst of these are not situated on membranes and should not interfere with strain measurements. Another interesting feature seen in the optical image is an etch pit on the surface of the sample. This is the result of a break in the surface protective ProTEK film, possibly caused by contamination on the $Si_{1-y}C_y$ during the spinning process, which has allowed TMAH to etch through from the surface to form a self-terminating pit.

8.4.5 Strain and Tilt Mapping By µ-XRD

Strain and tilt measurements were carried out on a 2 mm square membrane, the largest shown in Figure 8.23 using beamline B16 at the Diamond Light Source synchrotron.

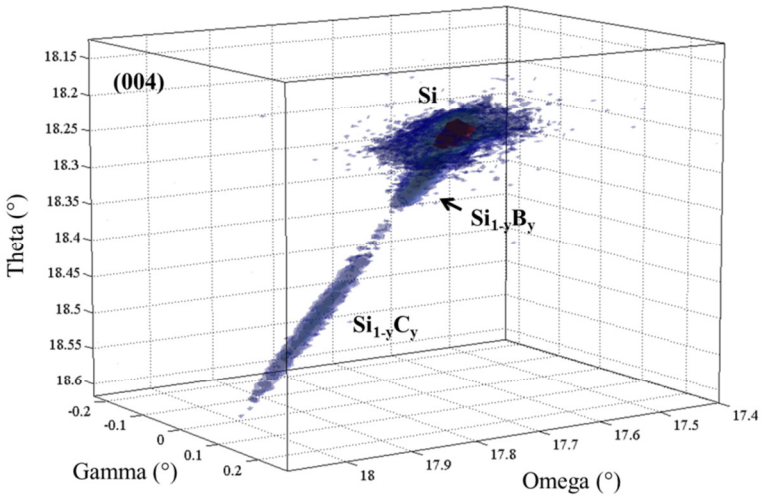

Figure 8.24 4D plot showing intensity iso-surfaces in the XRD measurement coordinates.

Strain profiles for the suspended $Si_{1-x}B_x$ and $Si_{1-y}C_y$ were characterized by measuring symmetric (004) and asymmetric (115) RSMs every 10 μm along the $[1\bar{1}0]$ direction across the membrane edge along the middle of the sample. Once the edge was traversed the step size was increased to 25 μm along the membrane and subsequently reduced to 10 μm again as the other edge was approached. The membrane edge, incident and scattered X-rays were all parallel to the [110] direction of the crystal and the spatial resolution of the RSMs is given by the spot size. A 4D plot of the data acquired from each point of the sample in the detector angle reference frame is shown in Figure 8.24. The addition of the piezo stage allows fast maps to be generated; a 95 μm x 95 μm region is scanned in 5 μm increments for a given ω. Upon completion ω is incremented and the process repeated. This process continues until ω is scanned across the Si, $Si_{1-x}B_x$ and $Si_{1-y}C_y$ (004) peaks. Once this area is mapped the *XYZ* stage is moved and the piezo scan repeated. Such a map can be obtained in approximately half the time compared to the generation of the same map from a series of line scans.

8.4.6 Strain Profiles

The strain profiles, taken along the $[1\bar{1}0]$ direction of the suspended $Si_{1-y}C_y/Si_{1-x}B_x$ membrane are shown in Figure 8.25. An increase of in-plane tensile strain can be observed across both the $Si_{1-x}B_x$ and $Si_{1-y}C_y$ suspended epilayers of approximately $\Delta\varepsilon_{||} \approx 0.09\%$ and $\Delta\varepsilon_{||} \approx 0.15\%$ respectively, see figs. 3(a) and (c). However, the uncertainty on these values is large due to nature of the in-plane calculations from the (115) reflection, see Equation 8.1, as such we will instead focus on the out-of-plane strain, which is inversely proportional to the in-plane strain assuming we have pure biaxial strain. The out-of-plane lattice parameter contracts for the suspended $Si_{1-x}B_x$ and $Si_{1-y}C_y$ ($a_\perp$ = (5.4166 ± 0.0001) Å and (5.3633 ± 0.0002) Å) compared to the supported material ($a_\perp$ = (5.4192 ± 0.0002) Å and (5.3667 ± 0.0004) Å) resulting in the suspended material becoming more tensile strained than the bulk material, see Figure 8.25 (b) and (d). The reduction in the out-of-plane lattice parameter upon suspension is similar for both materials with $\Delta a_\perp \approx 0.003$Å ($\Delta\varepsilon_\perp \approx 0.05\%$) although the uncertainties on the $Si_{1-y}C_y$ lattice constants are greater due to the reduced crystal quality. The out-of-plane strain is constant across the suspended structures with a very clear transition between the bulk and suspended material.

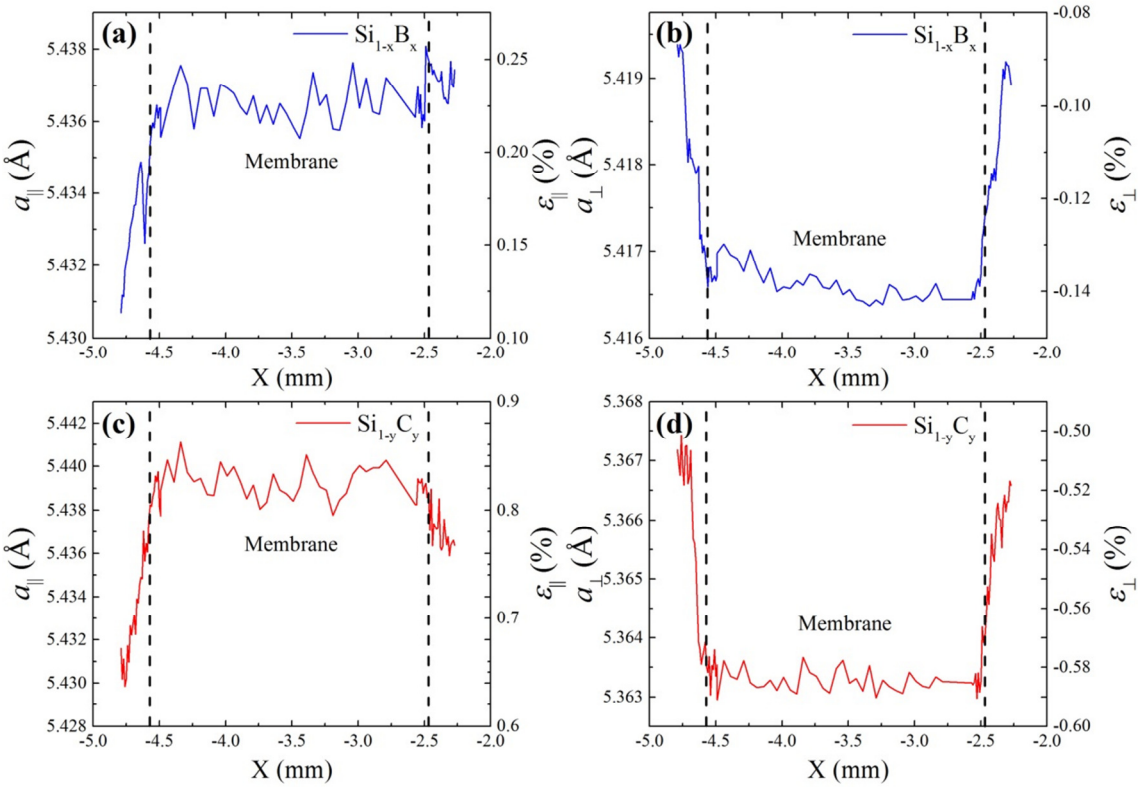

Figure 8.25 The (a) $\varepsilon_{\parallel}$ and (b) $\varepsilon_{\perp}$ profiles across the suspended $Si_{1-x}B_x$ epilayer and (c) $\varepsilon_{\parallel}$ and (d) $\varepsilon_{\perp}$ profiles across the suspended $Si_{1-y}C_y$ epilayer.

The strain and tilt variations were mapped over a 2D area by performing a piezo scan across the corner of the membrane by the acquisition of (004) RSMs. Maps of the $Si_{1-x}B_x$ and $Si_{1-y}C_y$ out-of-plane lattice parameters are shown in Figure 8.26.

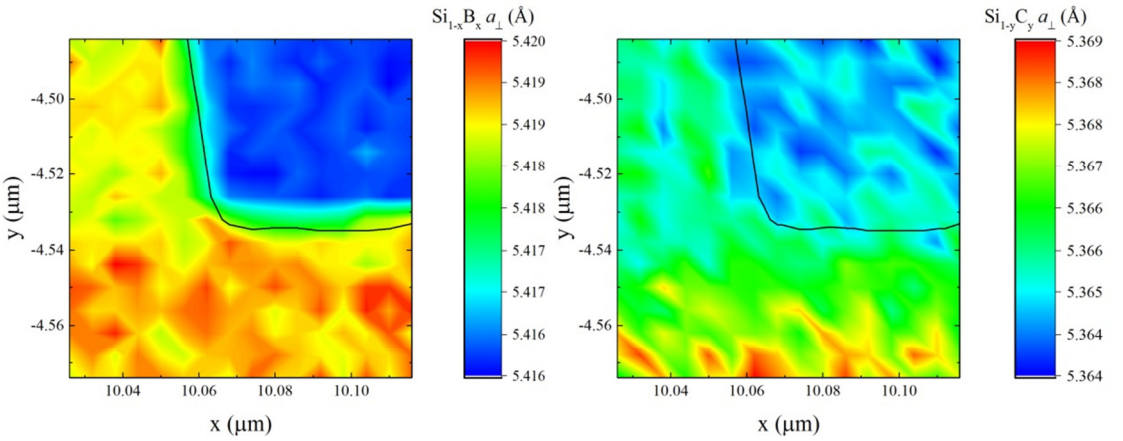

Figure 8.26 2-dimensional maps of the out-of-plane lattice parameters of the $Si_{1-x}B_x$ and $Si_{1-y}C_y$ suspended membrane corners. The boundary of the membrane is denoted by the black line and is defined by a decrease in the Si (004) Bragg peak intensity by 50%.

As shown before in the line scan profiles (Figure 8.25), the out-of-plane lattice parameter is seen to decrease upon suspension from the Si substrate. This implies that the in-plane lattice parameter has increased and as such the membrane is under more in-plane tensile strain. The area scans show no corner or edge effects in the strain variations of either the epilayers. Significantly more noise can be observed in the area map for the $Si_{1-y}C_y$ epilayer due to the presence of crystalline defects.

It had previously been suggested that tilt effects at the edge of suspended Ge membranes are the origin of this strain enhancement across the membrane entirety [185]. In order to access this explanation in more detail the tilt was calculated for the suspended membrane in both the q_x and q_y directions, see Figure 8.27. In this case, the tilt refers to the variation of an epilayer crystal orientation with respect to itself. To make this possible, a reference point was taken upon the supported region of the structure and defined to have a tilt equal to zero.

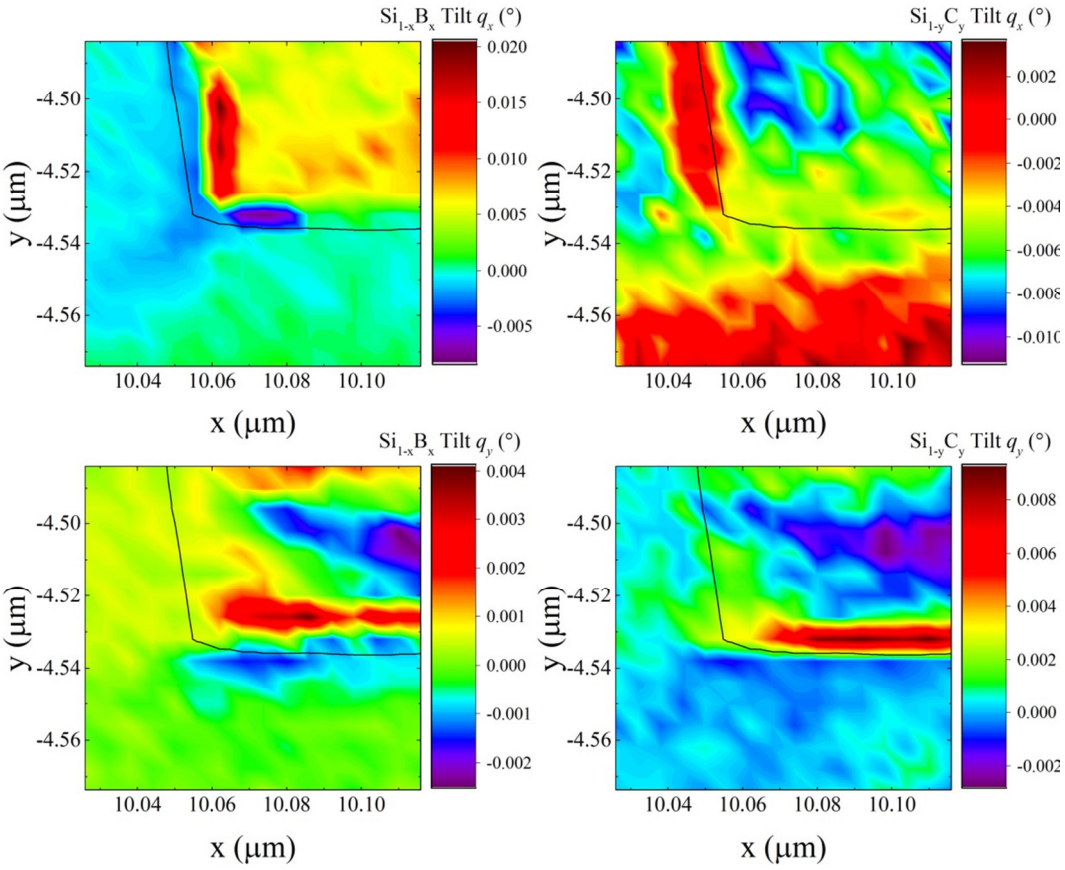

Figure 8.27 2-dimensional maps of the crystalline tilt resolved in both the q_x and q_y directions. In each case the tilt was defined as zero for the position at (10.03,-4.57). The boundary of the membrane is denoted by the black line and is defined by a decrease in the Si (004) Bragg peak intensity by 50%.

The tilt maps of both epilayer materials show significant tilt variation across the borders of the membrane. The fact that this tilt variation is dependent on the crystal planes and is not biaxial indicates the presence of shear strains along the membrane borders. These strains can account for the increase of in-plane lattice spacing found across the central region of the membrane which likely demonstrates biaxial strain (although this was not investigated). As with the out-of-plane lattice spacing, similar tilt variations can be observed in both the suspended $Si_{1-x}B_x$ and $Si_{1-y}C_y$ epilayers. This indicates that the epilayers undergo the same physical distortions, which is expected assuming the crystalline layers remain bound to one another and do not undergo any delamination. There is a slight misalignment between the positions of these tilt variations between the two epilayers; this is thought to be due to a slight shifting of the sample on the stage during the measurement process.

Discussions

In other systems where strain has been measured across suspended semiconductor structures (Ge or 3C-SiC), the initial tensile strain has always been a residual effect from thermal expansion mismatch and upon suspension the increase or decrease of tensile strain has been a combination of relaxation from thermal mismatch and strain increase from shear stresses due to tilting of the epilayers. As the system measured here is under tensile strain due to lattice matching the $Si_{1-x}B_x$ and $Si_{1-y}C_y$ to the Si substrate, there is little impact of thermal mismatch.

The work presented here is the first example of strain mapping across a $Si_{1-y}C_y$ suspended structure and one of the first examples of a system under a high level of tensile strain. The fabricated membranes are found to remain intact after fabrication and can even undergo an aggressive piranha etch during the removal of a protective surface film. The process of suspended $Si_{1-y}C_y$ is shown to increase the in-plane strain of the system by approximately 20% of its original value (0.67% bulk to ~0.82% suspended). This level of tensile strain in a $Si_{1-y}C_y$ epilayer is equivalent to a C content of ~1.85%, using the modified Vegard's law Equation 5.1, an increase of 0.35% C from the epilayers actual composition of 1.5%. This increase in strain has been shown to be a result of the shear stresses and resulting tilt at the edges of the suspended membranes. While the increase in strain is modest it could be utilised to increase the performance of certain devices making use of a $Si_{1-y}C_y$ channel. A more ideal structure for this application could be with suspended $Si_{1-y}C_y$ wires which would not only restrict the

current flow to certain dimensions but may further increase strain uniaxially in the direction of the current flow. Suspended membranes may be strained further by the presence of external stimuli such as physical force on the membrane or the creation of a pressure difference across the membrane, both of which would result in bowing and possibly further tensile strain enhancement in the material.

With the exception of edge effects, the membranes remain flat and therefore may present applications as compliant growth platforms for other materials, such as 3C-SiC, this topic is briefly investigated later in Chapter 9.

A journal article covering the topics in this Chapter is currently under preparation and will be published in due course.

Chapter 9
Further Material Growth

The following studies focus on additional research relating to material growth, carried out on both $Si_{1-y}C_y$ alloys and 3C-SiC grown within the ASM Epsilon 2000 RP-CVD system.

9.1 $Si_{1-y}C_y$ Multilayers

Heteroepitaxy can offer significantly more advantages that just allowing the growth of a foreign material on a dissimilar substrate. It can lead to the integration and incorporation of various different materials together, allowing certain properties to be exploited including the alteration of a material's energy band structure. The growth of multilayers is an excellent way to demonstrate and exploit this growth technique. In this study, multilayers have been fabricated from the growth of $Si_{1-y}C_y$ alloys with Si spacers and Ge thin films. Previous work in Chapter 5 has shown that the growth of $Si_{1-y}C_y$ epilayers of up to 20 nm and beyond can lead to significant structural planar defects, however, the impact of these defects on any subsequent growth has not yet been investigated. $Si_{1-y}C_y$ has also been shown to have a lower bandgap than Si for C contents up to several percent, see Figure 2.20, which could lead to quantum confinement through the formation of a 2-dimensional carrier gas by layering the $Si_{1-y}C_y$ epilayer between Si with a higher band gap.

To test the impact of $Si_{1-y}C_y$ defects on subsequent heteroepitaxial growth, a multilayer consisting of a thin $Si_{1-y}C_y$ epilayer sandwiched between Si spacer layers was grown by RP-CVD. The sequence of $Si_{1-y}C_y$ followed by Si spacer was repeated 20 times before being capped off with a Si epilayer, see Figure 9.1.

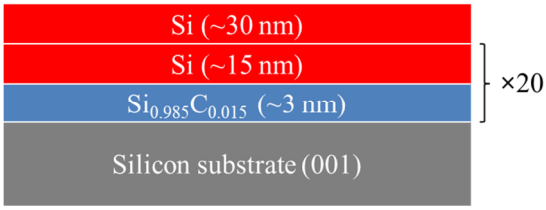

Figure 9.1 Cross sectional schematic of $Si_{1-y}C_y$ multilayer structure. The sequence of $Si_{1-y}C_y$ followed by ~15 nm Si was repeated 20 times during a single growth run.

The multilayer structure was characterised by HR-XRD coupled scans, however, the spectrum is dominated by the interference fringes from the multiple layers. Modelling to the spectrum gives a thickness of the Si and $Si_{1-y}C_y$ of 12 nm and 2 nm respectively within the multilayer stack with a C composition of 1.45%, see Figure 9.2.

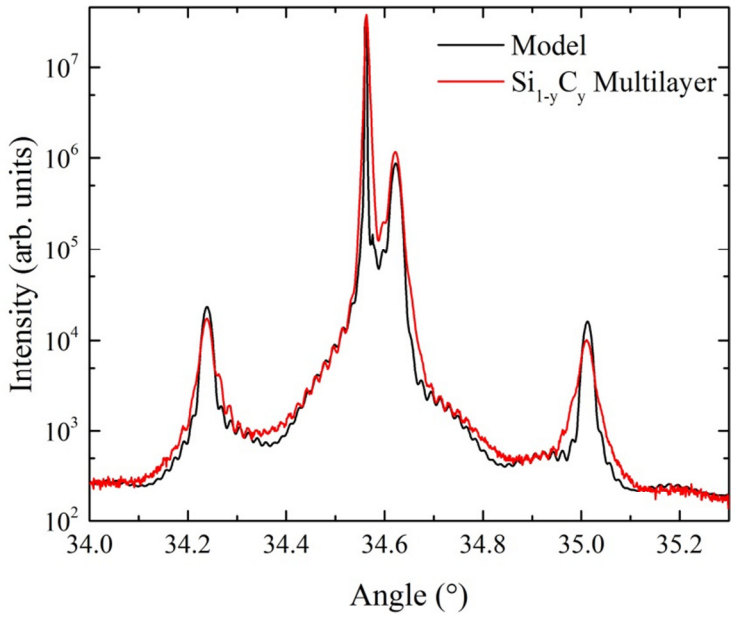

Figure 9.2HR-XRD coupled scan of the $Si_{1-y}C_y$ multilayer structure showing the Si (001) Bragg peak as well as thickness fringes associated with the Si spacing epilayers and the entire stack itself. The model was simulated using the software package RADS.

The heterostructure was imaged by X-TEM within the Jeol 2100 TEM and distinct epilayers can be resolved from the thin $Si_{1-y}C_y$ and Si epilayers, see Figure 9.3. While there are several defects appearing on the surface of the structure, none can be seen within the multilayer stack. This indicates that either defects are not forming due to the low thickness of the $Si_{1-y}C_y$ epilayers or the introduction of Si spacers is preventing the defects from propagating. The results show that there appears to be no negative effects of growing heteroepitaxially on $Si_{1-y}C_y$ epilayers.

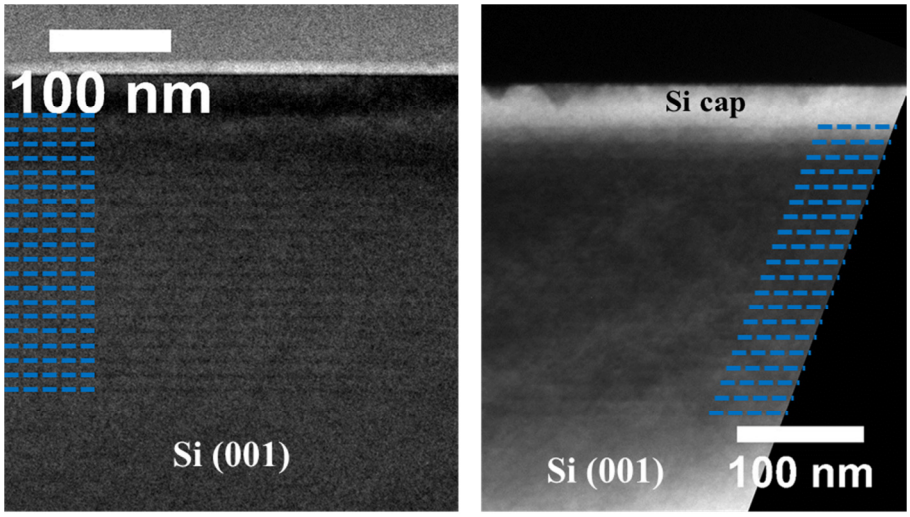

Figure 9.3 X-TEM micrographs of the multilayer heterostructure shown in Figure 9.1 in BF(004) (left) and DF(004) (right) diffraction conditions. The blue lines indicate the locations of the $Si_{1-y}C_y$ epilayers.

Ge is often used in strain engineering with quantum wells and other novel applications such as quantum cascade (QCL) lasers for terahertz detection [206], however, n-type dopants readily diffuse out of Ge making it difficult to form the abrupt interfaces necessary for optimal device performance [207]. One such solution to this issue could be in the integration of $Si_{1-y}C_y$ epilayers with Ge growth. As $Si_{1-y}C_y$ alloys have a very low diffusion coefficient they are ideal for preventing dopant diffusion and could replace pure Si as a lower bandgap alternative spacer between Ge quantum wells. To test whether this was possible, another multilayer heterostructure was grown with thin Ge epilayers grown using germane (GeH_4) sandwiched between $Si_{1-y}C_y$ and Si epilayers, see Figure 9.4.

Again, X-TEM images of the heterostructure multilayer were acquired and can be seen in Figure 9.5, which clearly shows distinct layers from the Ge, Si and $Si_{1-y}C_y$ epilayers within the multilayer. The growth of $Si_{1-y}C_y$ on Ge appears trivial with very little stagnation during the initial stages of growth. The sample shows no variation between the interfaces of Si/Ge and $Si_{1-y}C_y$/Ge, which is something that must be analysed with high levels of dopants and secondary ion mass spectroscopy (SIMS) analysis.

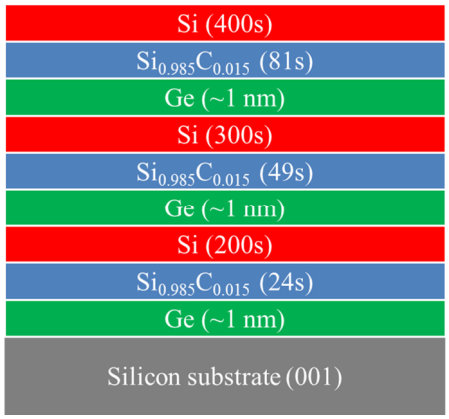

Figure 9.4 Cross sectional schematic of multilayer heterostructure of Ge heteroepitaxially grown on fully strained $Si_{1-y}C_y$ epilayers showing the growth times of the Si and $Si_{1-y}C_y$ epilayers.

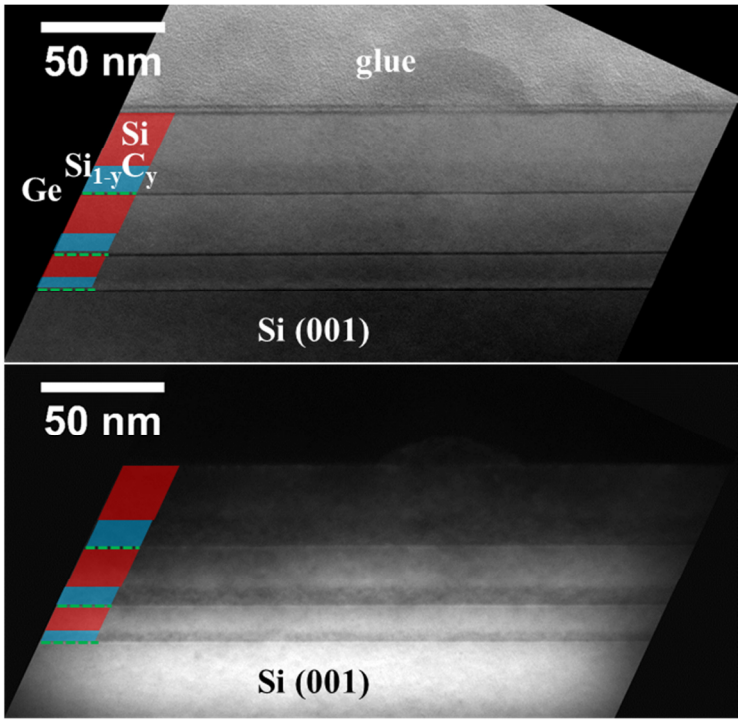

Figure 9.5 X-TEM micrographs of the heterostructure shown in Figure 9.4 in the BF(004) (top) and DF(004) (bottom) diffraction conditions. The epilayers have been identified using the same colour scheme as in the schematic shown in Figure 9.4.

Using the multilayer structures it is possible to extract an accurate growth rate and stagnation time for the growth of the $Si_{1-y}C_y$ and Si epilayers, see Figure 9.6.

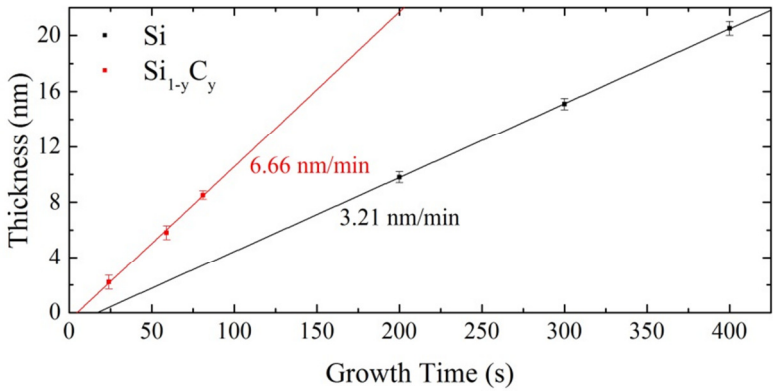

Figure 9.6 The thickness of epilayers grown in the multilayer shown in Figure 9.5, thicknesses were extracted from X-TEM measurements.

The growth rate of the $Si_{1-y}C_y$ was found to be 6.7 nm/min while the stagnation time before growth initiates is found to be 5.1 s assuming a linear dependence of thickness with growth time.

Discussions

$Si_{1-y}C_y$ alloys have been incorporated into multilayer structures with both Si and Ge interlayers. Multilayers with $Si_{1-y}C_y$ and Si show that additional defects do not form with the subsequent growth of Si on $Si_{1-y}C_y$ and defects that may form within the $Si_{1-y}C_y$ do not propagate through the Si. Only thin (~2 nm) $Si_{1-y}C_y$ epilayer were grown in the multilayer therefore whether the Si spacers can prevent defects formation or propagation with thicker, more defective epilayers has not been verified.

$Si_{1-y}C_y$ epilayers were also grown on Ge interlayers which were found not to interfere with the growth of the alloy. Being able to grow $Si_{1-y}C_y$ on Ge layers could have applications in forming Ge quantum well structures as the reduced diffusion coefficient or $Si_{1-y}C_y$ could be exploited to keep dopants within the Ge layers for QCL structures.

9.2 3C-SiC Deposition on SiO_2 and Selective Epitaxy

Selective epitaxial growth is desirable in many 3C-SiC applications as it can: simplify device fabrication steps by removing the need to etch 3C-SiC, allow easier integration of 3C-SiC with other semiconductor devices, reduce stresses induced in the epi-wafer by the thermal expansion coefficient mismatch between 3C-SiC and Si and crucially can reduce defect densities by limiting growth to restricted dimensions, allowing

stacking faults to terminate at SiO_2 sidewalls [91]. The first example of selective epitaxy of 3C-SiC on Si was demonstrated in 1989 [208], however, selective epitaxy of monocrystalline 3C-SiC has only been reported a few times in literature [209, 210].

As the invented growth process developed here is carried out at temperatures close to 1200 °C it offers the opportunity to carry out selective epitaxy using standard SiO_2 masks. Si wafers, coated in ~1 µm SiO_2, were patterned through photolithography and dry etching such that a variety of structures were formed of exposed Si substrate. The wafers were briefly cleaned in a 2.5% HF dip for 30s to clean the surface of the Si without inducing significant damage to the SiO_2 mask, before being loaded into the ASM Epsilon 2000 RP-CVD system.

Several growth runs were carried out with varying parameters. In the following initial trials, 3C-SiC was grown using the standard process previously described in Chapter 6 to assess the deposition process of 3C-SiC on an oxide mask. Figure 9.7 shows a full wafer after epitaxy.

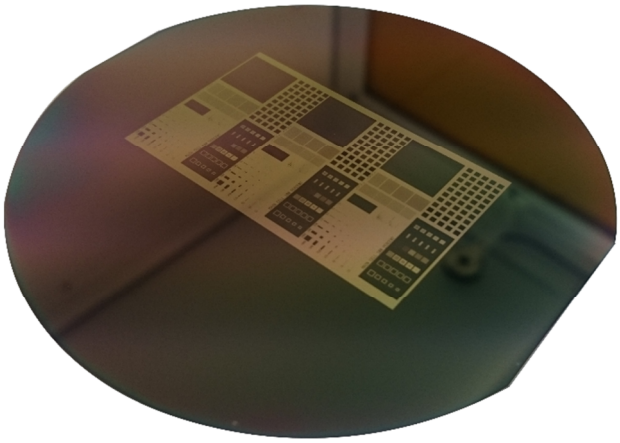

Figure 9.7 Selectively grown 100 mm epi-wafer, the lighter features are the SiO_2 mask. The image was taken after material deposition.

9.2.1 Standard Growth Process

Optical images of a spider web feature on the selectively patterned wafer are shown in Figure 9.8 and show that there has indeed been deposition on the SiO_2 mask. A higher resolution SEM image can be seen in Figure 9.9 and show that the grown material is dominated by islands. Without appropriate lattice sites for the adatoms to bond to, it appears the 3C-SiC has clustered on the surface of the SiO_2 creating nucleation points for further growth to occur by the Volmer-Weber mechanism.

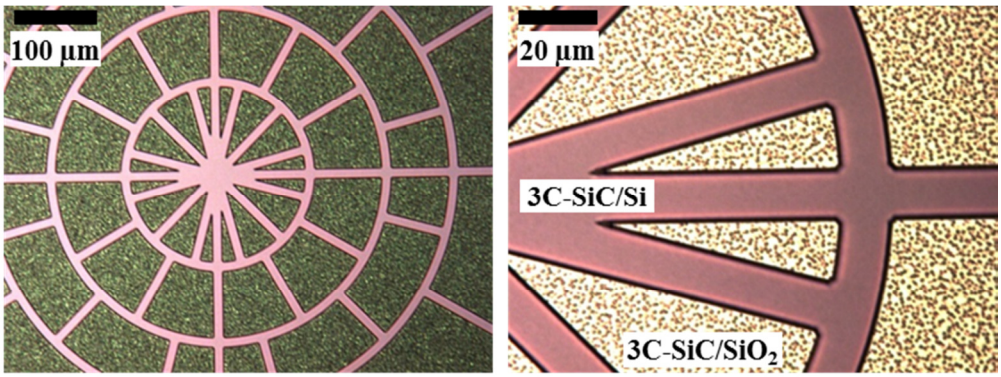

Figure 9.8 Optical images of selectively grown wafer after deposition. The lighter patches are where the channels of Si were and where 3C-SiC has been grown directly on the substrate.

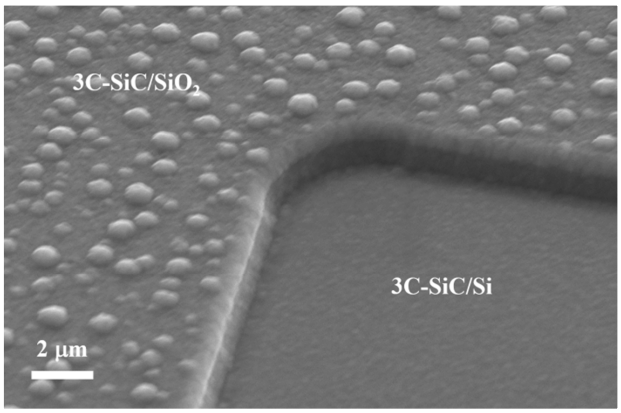

Figure 9.9 Edge of a square feature after selective growth.

The FIB-SEM was used to extract a cross section from the selectively grown epi-wafer covering a portion of the 3C-SiC that was grown on Si and SiO_2 and can be seen in Figure 9.10.

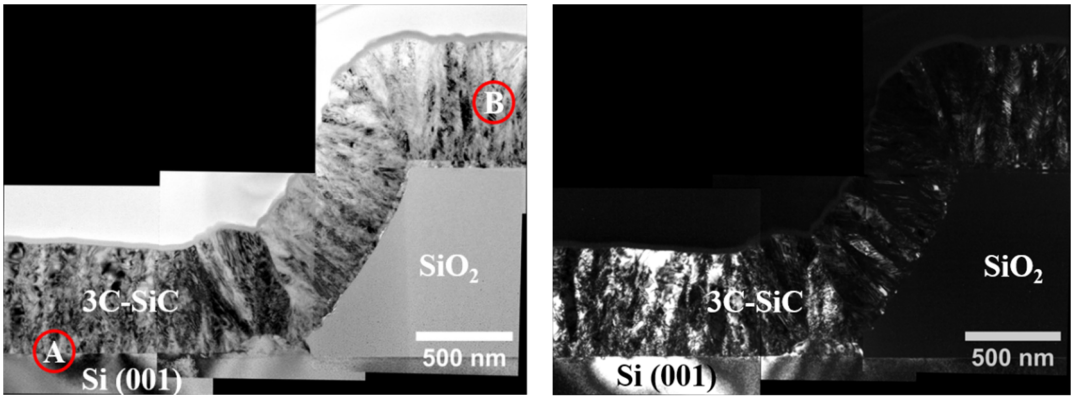

Figure 9.10 Cross sectional TEM micrographs of selectively grown monocrystalline 3C-SiC. Left – BF (004) showing two areas (A and B) where the SAED patterns shown in Figure 9.11 were taken from. Right – DF (004).

The X-TEM measurements show that almost equivalent deposition thicknesses were achieved on both the Si and SiO_2, however, the dark field image shows that the material grown on Si is crystalline, while the layer grown on the SiO_2 only shows some signs of crystallinity. To assess the form of this crystallinity, SAED patterns were taken at points A and B and can be seen in Figure 9.11. The material grown on Si is found to be monocrystalline, as indicated by the positions of the Bragg peaks in relation to the underlying substrate, while the material grown on the SiO_2 is amorphous with some polycrystallinity.

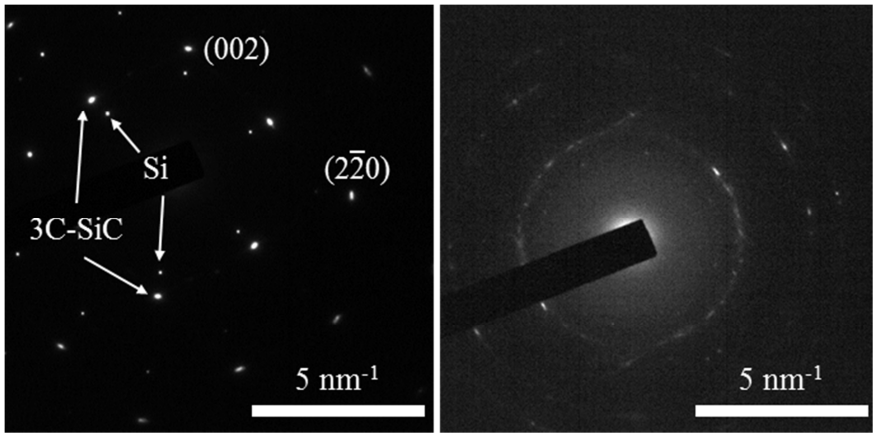

Figure 9.11 SAED pattern of points A (left) and B (right) as indicated in Figure 9.10.

9.2.2 Modified Growth with HCl

While growth of polycrystalline 3C-SiC on SiO_2 may have applications, true selective epitaxy requires no depositions on the masking layer. To prevent nucleation on the oxide, HCl was flowed through the growth system during epitaxy at flow rates up to 300 sccm, to etch away any depositions on the SiO_2. The addition of HCl may negatively impact the growth conditions by affecting the C/Si ratio, or could also affect the depositions of 3C-SiC on the crystalline Si substrate. Optical images of the resulting selective growth are seen in Figure 9.12.

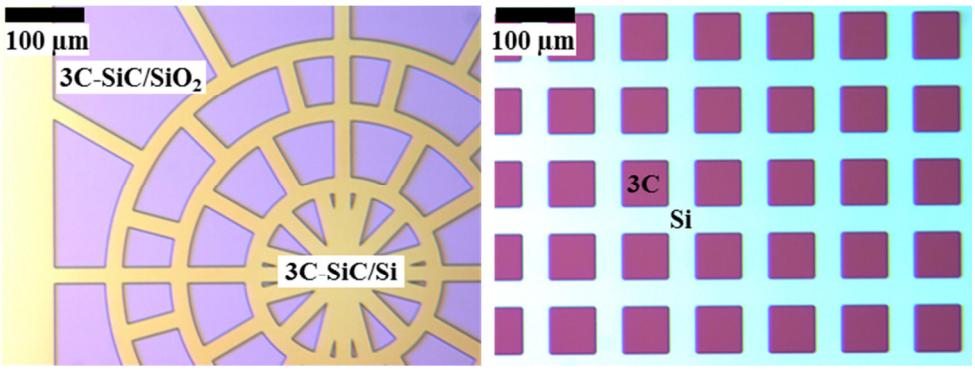

Figure 9.12 Optical images of true selectively grown 3C-SiC epilayer features. In the left image the lighter regions are 3C-SiC while on the right these sections are the darker squares. This variation in contrast is assumed to be due to thickness variation across the SiO_2 mask.

The addition of HCl to the growth of 3C-SiC appears to result in true selective epitaxy. 3D maps of the spider web structure were mapped using a stylus profilometer system before and after the SiO_2 was stripped off by chemical etching in a 2.5% HF solution, see Figure 9.13. The maps show that the SiO_2 was completely removed in the HF etch indicating that either 3C-SiC was not deposited on the mask at all or that there were sufficient breaks in the deposited material to allow the oxide to etch off.

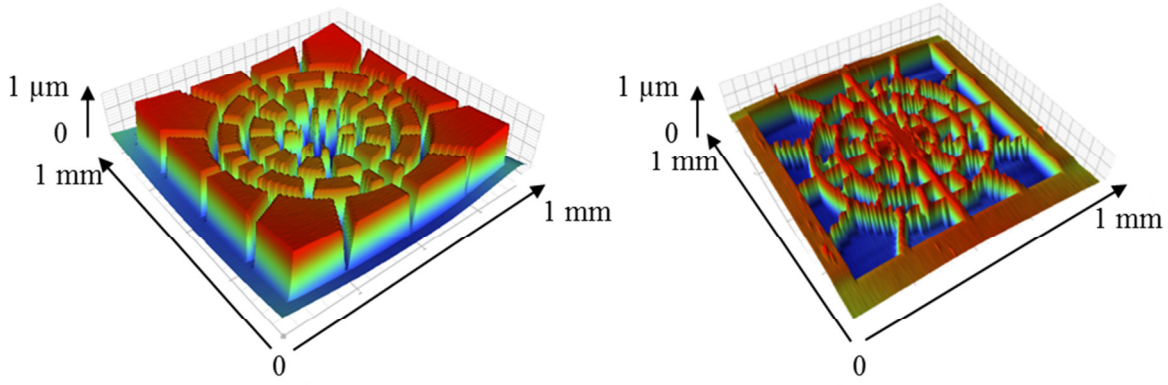

Figure 9.13 3D maps of a selectively grown spider web pattern taken using a stylus profilometer with an automated area stage before (left) and after (right) removal of the SiO_2 in an HF dip. Apparent bow in the surface plots is an artefact caused by the surface profile removal tool applied to the scans which removed the sample tilt caused by how the sample sits on the stage.

Unlike the image shown in Figure 9.9, the SEM of the selectively grown 3C-SiC with additional HCl flow shows no island formation or 3D features on the SiO_2 mask. The mask is fully removed after wet etching in HF solution allowing the formation of features ranging from several up to 100s of microns in size, see Figure 9.14.

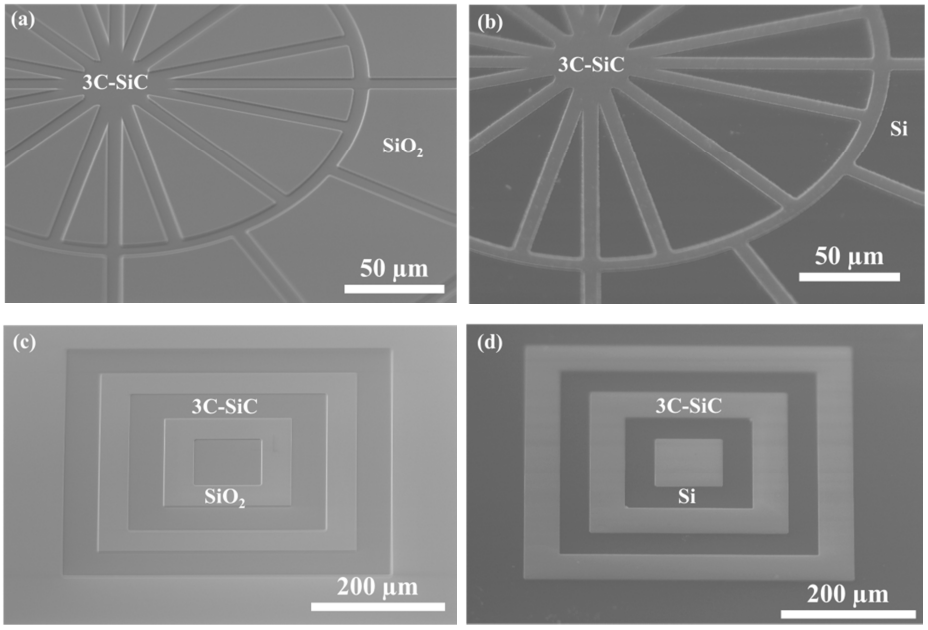

Figure 9.14 Secondary electron SEM images of selective grown 3C-SiC before (a,c) and after SiO_2 mask removal in HF solution.

A FIB-SEM lift out was performed on selectively grown 3C-SiC sample as before and imaged by X-TEM, see Figure 9.15.

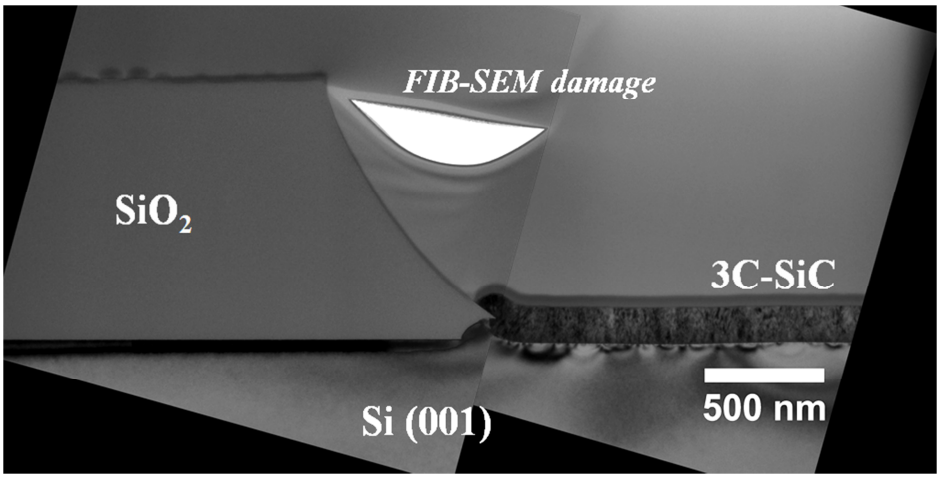

Figure 9.15 BF(004) cross sectional TEM micrograph of 3C-SiC grown using a DCS buffer layer.

The TEM image shows no 3C-SiC depositions on the SiO_2 mask, proving that the additional of HCl to the growth system has suppressed deposition build up on the mask. As with the previous FIB-SEM lift-out sample, there is some damage on the surface of the SiO_2 which could be mistaken for 3C-SiC, however, this effect is also observed on the 3C-SiC in both Figure 9.15 and Figure 9.10.

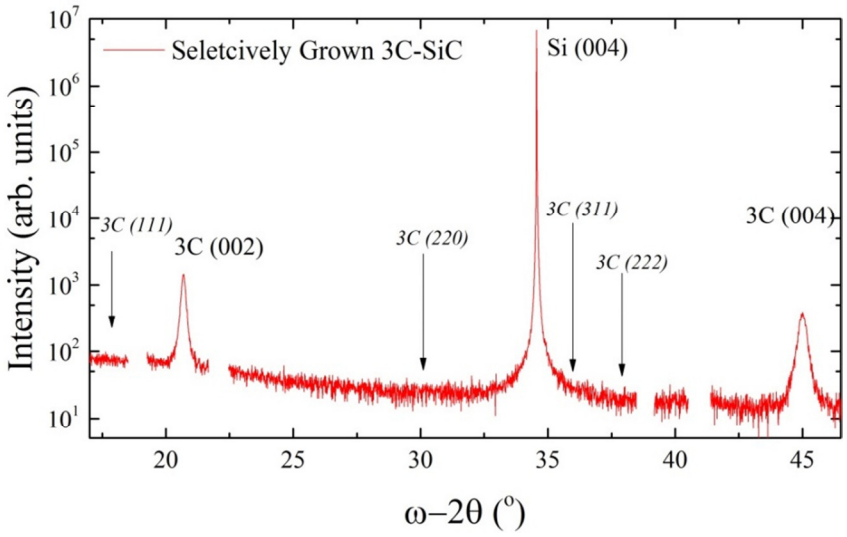

Figure 9.16 HR-XRD coupled scan of the HCl containing 3C-SiC growth sample showing that the epilayer is monocrystalline. Bragg peaks from the Al stage have been removed for clarity.

The HR-XRD coupled scan shown in Figure 9.16 shows that the 3C-SiC epilayer in monocrystalline. The quality of the 3C-SiC according to both HR-XRD and X-TEM is poor compared to previous non-selective growth and is likely due to the addition of a high HCl flow during growth increasing the effective C/Si ratio by reducing the reactivity of the Si adatoms during growth.

Discussions

Selective epitaxy in 3C-SiC is troublesome as the typical growth temperatures used to achieve high crystal quality (~1400 °C) destroy and distort standard masks such as SiO_2 or Si_3N_4 used for selectivity. Growth at low temperatures has been explored before in order to achieve selective growth, however, growth often results in polycrystalline 3C-SiC films or depositions on the oxide mask. The results presented in this section demonstrate a commercial route to the selective epitaxy of monocrystalline 3C-SiC on Si, using a standard SiO_2 mask. This has been achieved through chlorine precursor chemistry with the addition of HCl to supress deposition on the SiO_2 mask.

Selective growth has various advantages in semiconductor epitaxy as it can help reduce defects and strain effects as well as form of the basis of integrating different epilayers into devices structures. This step in selective growth allows the integration of selectively grown 3C-SiC into the Si industry.

The work presented here is only the first step towards many possibilities that selective epitaxy can bring to 3C-SiC and the semiconductor industry in general. The addition of

HCl to the growth of 3C-SiC has been found to affect the optimal growth conditions, resulting in more defective, although still monocrystalline, material. The process requires much calibration to achieve higher quality material.

More confined dimensions of the selectively grown 3C-SiC must be carried out to investigate the effect of the SiO_2 side walls on defect termination and the author would like to see the selective epitaxy process performed on thinner SiO_2 mask layers such that ELO can be investigated.

A journal article describing these results in more detail is currently under preparation.

9.3 $Si_{1-y}C_y$/Si Growth Platforms for 3C-SiC

Following on from the successful fabrication of suspended $Si_{1-y}C_y$ epilayers in Chapter 8 and the development of a low temperature 3C-SiC growth process, it is possible to evaluate whether these membranes can act as platforms for further epitaxy of 3C-SiC. Heteroepitaxial growth on thin substrates has theoretically been shown to reduce the formation of defects and increase the critical thickness of pseudomorphic epilayers [211]. In terms of 3C-SiC growth this could result in fewer defects in the epilayer as the thin substrate becomes compliant. From a practical standpoint, producing a substrate close to the critical thickness of a heteroepitaxially grown crystal is almost impossible. However, membranes could offer an alternative method for achieving such an effect, see Figure 9.17.

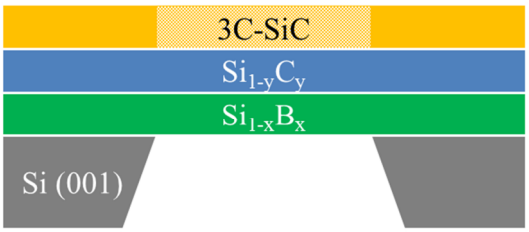

Figure 9.17 Proposed cross sectional schematic is 3C-SiC growth on a suspended $Si_{1-y}C_y/Si_{1-x}B_x$ membrane. If done correctly, a variation in the crystal quality should be expected in the 3C-SiC grown upon the thin suspended substrate.

A preliminary study was carried out with the aim to demonstrate that it is possible to suspend $Si_{1-y}C_y$ in square membranes over a 100 mm diameter substrate and perform further heteroepitaxy without the destruction of the membranes.

9.3.1 Wafer Scale Membrane Fabrication

$Si_{1-y}C_y/Si_{1-x}B_x$ suspended membranes were fabricated using the same method as previously described in Chapter 8 only the process was carried out on a full 100 mm wafer opposed to small pieces. A total of 45 square membranes (2 mm × 2 mm) were fabricated in a grid-like pattern as seen in Figure 9.18. Unfortunately, 15 membranes broke during the violent piranha etch process. This can be overcome in the future by either diluting the piranha etch or fabricating smaller membranes, which will be more robust. An alternative method which was not investigated would be to use SiO_2 as a alkaline resistant layer on the surface and underside of the epi wafer. It would then be possible to remove the SiO_2 layer using a more gentle 2.5% HF dip.

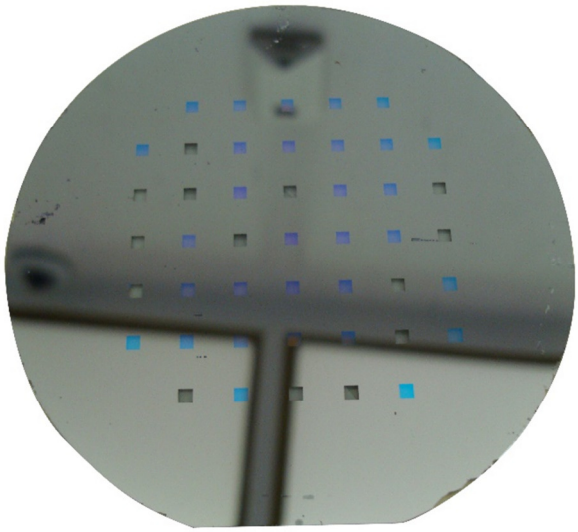

Figure 9.18 $Si_{1-y}C_y/Si_{1-x}B_x$ membranes on a 100 mm diameter Si wafer after having gone through the piranha and HF clean stages. 30 out of 45 membranes survived the fabrication process. Any other imperfections with the epi-wafer have been caused by non-uniform coverage of ProTEK on the topside, which has allowed certain areas to etch within the TMAH bath.

The epi-wafer was then run back through the ASM Epsilon 2000 RP-CVD system and 3C-SiC was grown upon it. For details on the growth process please refer to Chapter 6. The resulting epi-wafer can be seen in Figure 9.19.

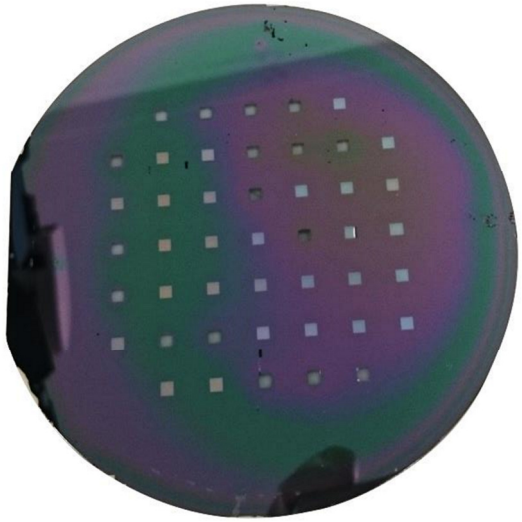

Figure 9.19 3C-SiC grown on suspended $Si_{1-y}C_y/Si_{1-x}B_x$/Si (001) membranes. The variation in colour across the wafer indicates non-uniform growth across the substrate due to non-optimal conditions within the reactor.

9.3.2 3C-SiC Membrane Characterisation

The 3C-SiC grown upon suspended $Si_{1-y}C_y/Si_{1-x}B_x$ membranes was characterised using a range of in-house techniques in order to assess how the material grown upon the suspended membranes differs from that grown on bulk material.

Assessing Crystal Structure

The crystallinity of the heterostructure was analysed using HR-XRD coupled scans and show that 3C-SiC was heteroepitaxially grown on the substrate indicating that the presence of membranes on the wafer surface had little or no effect on the epitaxial growth process, see Figure 9.20. Unfortunately, the X-ray spot size obtained by in-house HR-XRD techniques was larger than the 3C-SiC membranes and as such the XRD signal from the membranes would not be isolated. Other techniques or the use of a synchrotron with a significantly smaller X-ray beam will be required to compare the crystalline structure between the 3C-SiC grown on the bulk and suspended virtual substrate. The higher resolution coupled scan shown in Figure 9.20 that focuses on the Si substrate shows a shoulder to the Si peak which is associated with residual $Si_{1-x}B_x$.

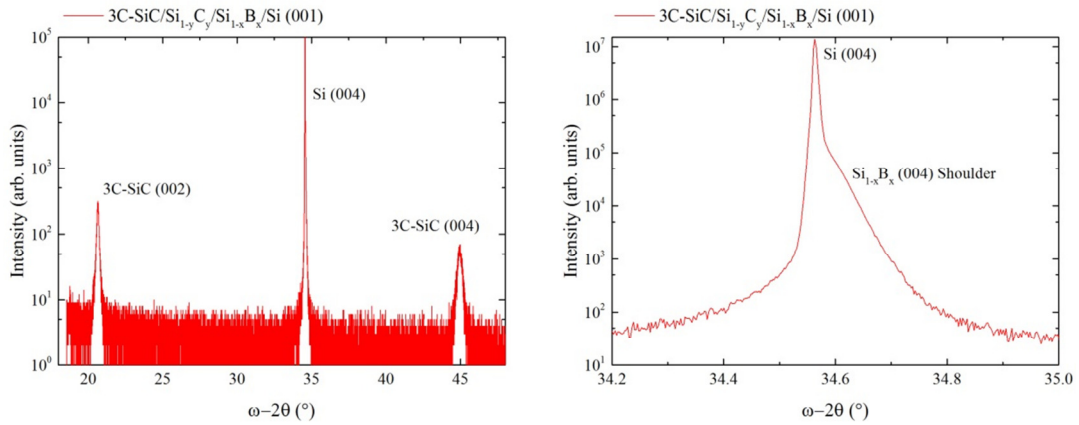

Figure 9.20 HR-XRD ω-2θ coupled scans demonstrating that the 3C-SiC is crystalline. The plot on the right shows that there is still a shoulder to the Si (004) peak in the expected position of the $Si_{1-x}B_x$ (004) Bragg peaks.

Surface Morphology

The surface morphology of the corner of a membrane was analysed using contact mode AFM, see Figure 9.21. While the surface of the bulk 3C-SiC is relatively smooth, the membrane shows strong variations in the topology. The larger area scan indicates that there may be some regularity to the hills and troughs seen in the membrane which tend to vary by approximately ±20 nm. This indicates that the growth of the 3C-SiC is either non-uniform across the membrane or, more likely has buckled under compressive strain. This could be explained if the $Si_{1-y}C_y/Si_{1-x}B_x$ suspended substrate is compliant and has adhered to the crystal structure of the 3C-SiC, hence introducing compressive strain to the heterostructure.

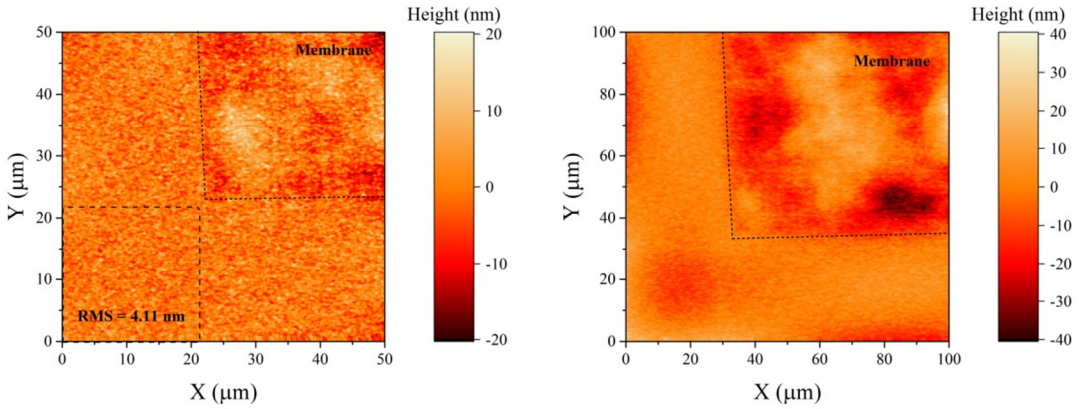

Figure 9.21 Surface morphology of the corner of a 3C-SiC/$Si_{1-y}C_y/Si_{1-x}B_x$ membrane. The RMS roughness of the sample is calculated in the smaller square shown on the left AFM scan to be 4.11 nm.

Crystal Variation Across the Membranes

Without immediate access to a synchrotron capable of micro-beam XRD measurements it is difficult to confirm whether the quality of the 3C-SiC is improved when grown on the suspended membranes. However, Raman spectroscopy can give some indication on the quality of the 3C-SiC. The Raman spectrum obtained from the 3C-SiC/$Si_{1-y}C_y$/$Si_{1-x}B_x$ membrane is shown in Figure 9.22 and was carried out using a 532 nm excitation laser. While the reference 3C-SiC membrane sample shows only the characteristic 3C-SiC TO and LO peaks, the 3C-SiC/$Si_{1-y}C_y$/$Si_{1-x}B_x$ membrane shows additional peaks from the underlying Si peak. This shows that the underlying alloys remain intact after 3C-SiC heteroepitaxy.

Raman spectra identical to those shown in Figure 9.22 were obtained over a 2D area covering the corner of a 3C-SiC/$Si_{1-y}C_y$/$Si_{1-x}B_x$ membrane. The FWHM of the 3C-SiC TO peak is plotted for this area in Figure 9.23. The TO peak is observable across the entire map proving that 3C-SiC has grown across the entire structure. While the FWHM is observed to decrease across the 3C-SiC grown on the membrane it is unclear whether this is due to an improvement on crystal quality or due to reduced background noise from the underlying substrate and further characterisation techniques are required to determine the variation in crystal quality between the two areas of the sample.

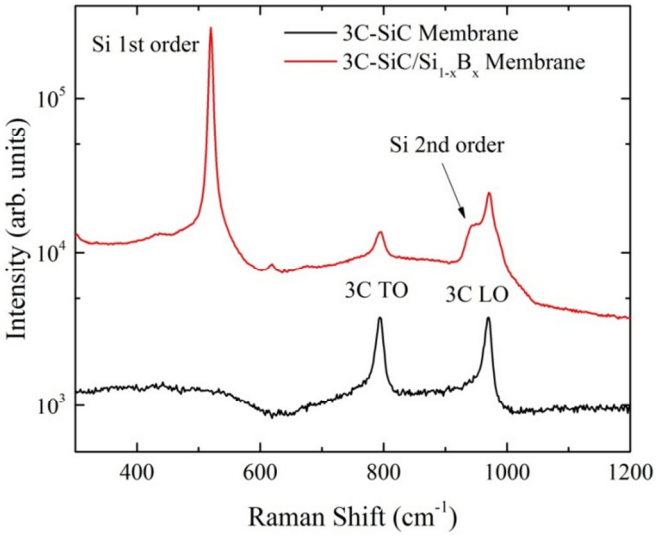

Figure 9.22 Raman spectra of the 3C-SiC grown on the $Si_{1-y}C_y$,/$Si_{1-x}B_x$ membranes and a 3C-SiC membrane formed after standard heteroepitaxial growth on Si for comparison.

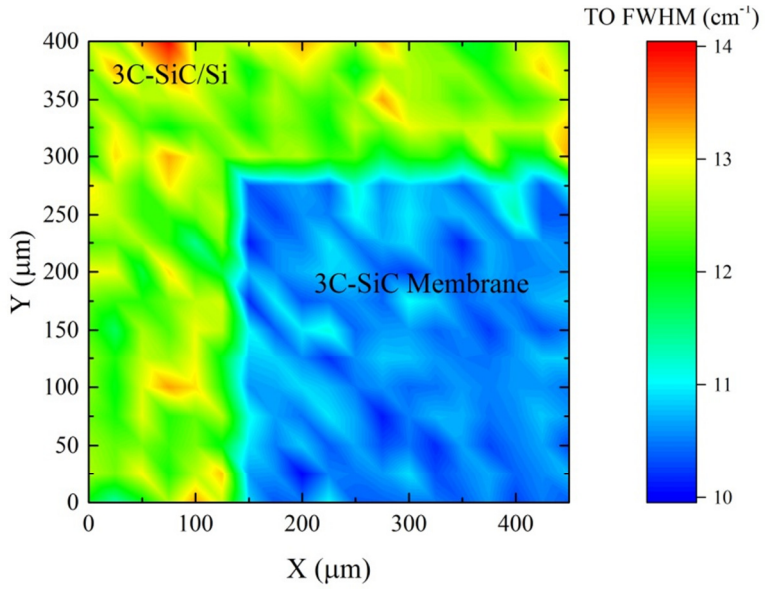

Figure 9.23 FWHM of the 3C-SiC TO Raman peak mapped across the corner of a 3C-SiC/$Si_{1-y}C_y$/$Si_{1-x}B_x$ membrane.

Obtaining a cross sectional TEM image of the membrane proved to be difficult as the 3C-SiC membrane was indistinguishable from the surrounding material under SEM imaging, hence a cross section lift-out spanning the membrane and bulk could not be obtained through the FIB-SEM technique. Instead, however, it is possible to determine certain properties of crystalline membranes through plan-view (PV) TEM imaging. PV-TEM imaging is the process of observing a thin sample vertically through the film, i.e. down the [001] direction in a (001) crystal. This is normally achieved using polishing processes previously described with X-TEM imaging, however, suspended membranes can offer electron transparent structures without thinning. In this case the 3C-SiC film was approximately 500 nm thick and needed thinning before it could be imaged. A dry etching system was used to thin the 3C-SiC sample down to ~100 nm from the topside, similar to the process used in section 8.3.1. The only caveat of doing this is that the dry etching process is rather aggressive and could have damaged the crystalline structure of the 3C-SiC. The membrane was then loaded into a specially designed TEM sample holder as shown in Figure 9.24.

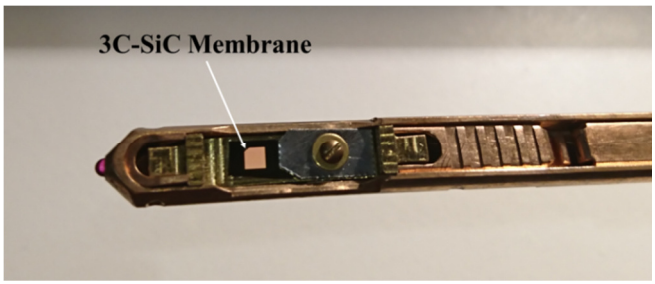

Figure 9.24 Single tilt TEM sample holder suitable for the loading of bulk samples.

PV-TEM micrographs were taken through the membrane at the corner with the bulk supporting crystal, see Figure 9.25. The image starts to become blurred at the corner of the membrane due to the increasing thickness caused by the supporting crystal. It is still unclear whether there is any improvement of the crystal structure.

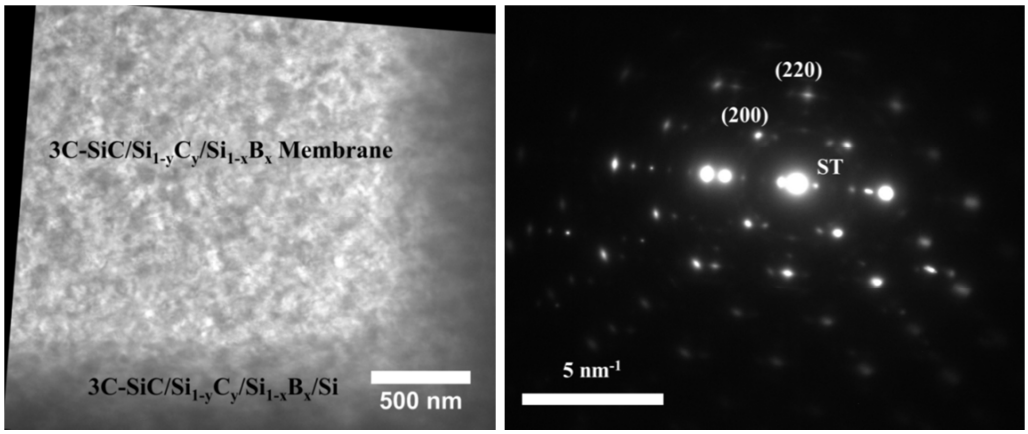

Figure 9.25 Straight through PV-TEM micrograph of the corner of the 3C-SiC/$Si_{1-y}C_y$/$Si_{1-x}B_x$ membrane (left) with an SAED pattern of the membrane showing diffraction peaks (right).

The electron diffraction pattern proves that the membrane material is crystalline. The plot shows multiple peaks associated with a monocrystalline material. Additional peaks in the plot may be a result of the buckling of the membrane as seen in the AFM scans or indicate regions of polycrystallinity. Some rings around the straight through beam are visible which would imply there is some amorphous material in the structure, possibly a result of the dry etching process.

Discussions

To conclude, 3C-SiC growth has been carried out on suspended membranes for the first time in an attempt to improve crystallinity and explore novel routes to reducing

defectiveness is heteroepitaxially grown crystals. The resulting 3C-SiC epilayer was found to be crystalline through HR-XRD and Raman mapping, however no discernible improvements in crystal quality could be ascertained through the techniques available. Micro XRD mapping would be an ideal technique to assess any variations in crystal quality across the membrane structure, however, this would require access to a synchrotron facility and not something that can be carried out readily in the lab. AFM surface mapping revealed interesting buckling effects at the edges of the membranes that were not present before the 3C-SiC epitaxy which could imply some interesting strain effects within the system. We speculate that if the $Si_{1-y}C_y$ epilayer is acting partially compliant with the 3C-SiC grown upon it, then the alloy would experience compressive strain which could lead to these edge effects.

The work presented here demonstrates the first example of wafer scale epitaxy on suspended membranes. While the improvement on crystal quality is yet to be verified, the process of growing on membranes has been executed on a full 100 mm substrate without any issues in wafer handling on pressure on the membranes themselves. Any breakages in the membranes occurred prior to epitaxy. The process allows one to grow heteroepitaxially on extremely thin substrates which could help to increase the critical thickness of other materials such as Ge, $Si_{1-x}Ge_x$ and $Ge_{1-x}Sn_x$ for growing thick, defect free epilayers. Further work on this area of research is still required in order to understand this process in more depth and the potential benefits it can offer.

Chapter 10
Conclusions and Further Work

The results presented include a number of enhancements within the epitaxy of C containing semiconductor materials, an understanding of their material properties and in some cases particular applications. Advancements were made in the field of $Si_{1-y}C_y$ through the successful growth of high quality alloys up to ~1.5% C content, using the low cost precursors TMS and disilane, a step towards cost reduction. In-depth characterisation of crystalline defects within the epilayers led to a greater understanding of C segregation and limitations on this combination of precursors. Additional strain enhancement in the $Si_{1-y}C_y$ was found to be possible through the fabrication of suspended membranes, a technique that can be applied to various other tensile strained heterostructures.

The greatest technological advancements made within this piece of research focus on the incorporation of 3C-SiC epitaxy into the repertoire of Si based growth technology. Low temperature epitaxy of high quality, monocrystalline 3C-SiC thin films on standard Si substrates offers a highly commercial process capable of enhancing Si based technologies as well as enabling a number of additional materials including GaN and graphene, offering suitable virtual substrates. This work paves the way towards a greater understanding of 3C-SiC as a material as well as its heteroepitaxy and applications.

The processes described in this work were able to grow epilayers of thickness up to ~6 μm, which are more than suitable for use in virtual substrates or sensors/MEMS. Another potential application of 3C-SiC is within power electronics, in which epilayers can range in thickness up to 10 μm and above for blocking voltages in the range of >1 kV. The process developed in this work has not been tested in detail up to these thicknesses and is something that will require further research in the future. The primary concern of growing epilayers of these thicknesses will be managing depositions on the

walls of the quartz chamber and their subsequent removal. One method to reduce these depositions will be to reduce the growth temperature further below 1200 °C which will in turn reduce the wall temperature and deposition rates. Whether this will compromise crystalline quality or not is something that will need researching.

This research investigated the electrical properties of doped and undoped 3C-SiC. The doping carried out in this research was all based on phosphorus. N-type doping provides one part of the solution to more complex device structures, but p-type doping will also need to be achieved to unlock other devices structures such as PiN, PN or CMOS based systems. On a similar theme, native oxide formation on 3C-SiC is critical for a number of MOS applications and is a topic that was not covered in this initial research.

3C-SiC offers an excellent platform for a number of suspended device structures such as pressure sensors, gas flow and optical devices. Even in the case of electrical systems, the Si substrate often leads to parasitic effects and the removal of this substrate is desirable. Many implications and benefits of removing the Si substrate have been investigated such as the strain effects, prospects of improving crystalline quality through annealing or heteroepitaxy on suspended structures and investigating optical properties. The next steps in this field of research would be to use the knowledge of the material properties and previous doping and electrical properties to prototype various device structures from this low temperature grown 3C-SiC. The huge advantage this process offers is the opportunity to incorporate the growth into the standard Si industry based processes offering low-cost and large scale. Various MEMS and sensor devices have been tested in literature but 3C-SiC is yet to penetrate the semiconductor markets precisely due to the issues that this research has solved.

Selective epitaxy is another important process for heteroepitaxial growth as it can reduce defects, thermal stresses and can lead to interesting heterostructures and ultimately heterogeneous integration. While others have struggled with selective growth in the past, work presented here has demonstrated that monocrystalline 3C-SiC can be selectively grown using the appropriate growth conditions and temperatures using a standard SiO_2 mask. Further work looking into this process as well as epitaxial lateral overgrowth could be a route to defect free 3C-SiC and integrate this material with other group IV semiconductors.

This work offers a building block for a significant number of technological advancements and the author wishes good luck to anyone who decides to take up the exciting challenge of 3C-SiC heteroepitaxy.

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