4H-SiC trench MOSFET with integrated fast recovery MPS diode

Tianxiang Dai✉, Chun Wa Chan, Xc Deng, Huaping Jiang, Peter M. Gammon, Mike R. Jennings and Phil A. Mawby

A 4H-SiC trench metal–oxide–semiconductor field-effect-transistor (MOSFET) design with an integrated merged PiN Schottky (MPS) diode is proposed. The Schottky contact is embedded on the bottom of the trench structure for the first time. The low electric field in the oxide and Schottky contact surface can be achieved simultaneously using the proposed integration design which enhances the oxide reliability and reduces leakage from the Schottky diode. The integration of the MPS diode reduces the total chip area and the required number of dies compared with the conventional method of using an external Schottky diode.

Introduction: The superior electrical and thermal properties of silicon carbide material make it a suitable candidate for applications at elevated power and temperature range. Unlike planar-gate metal–oxide–semiconductor field-effect-transistors (MOSFETs) with their necessary junction-gate field-effect-transistor (JFET) region, trench MOSFETs allow much greater cell density. It was reported in [1] that {1120} crystal plane on 4H-SiC substrate exhibited higher mobility, and therefore, the trench MOSFET structure also allows greater current density with reduced specific on-resistance.

External Schottky diodes [Schottky barrier diode (SBD)] are usually connected antiparallelly to MOSFETs in a H-bridge configuration to improve the switching performance in applications like motor drives and any other inverter circuits. If the Schottky diode can be embedded into the MOSFET structure, the chip count in the power module can be reduced while the circuit performance is not compromised. A planar gate SiC MOSFET with built in Schottky diode was proposed in [2] which showed a smaller reverse recovery charge and lower switching loss compared to conventional MOSFET with PiN body diode. Trench MOSFETs with integrated Schottky diode were fabricated in [3], however, the integrated devices only share the termination region and the active regions were still separated. This Letter proposes a U-shape trench MOSFET (UMOS) design with integrated merged PiN Schottky (MPS) diode (MPS-UMOS) where the active regions of the Schottky diode and the trench MOSFET merge together. The proposed design will have lower switching loss compared to the conventional UMOS structures with and without external Schottky diodes.

Design and simulation: Fig. 1*a* shows the conventional UMOS structure while Fig. 1*b* presents the proposed UMOS design integrated with MPS diode. The p+ implant in the conventional UMOS structure is used to shield the high electric field away from the gate trench bottom oxide [4].

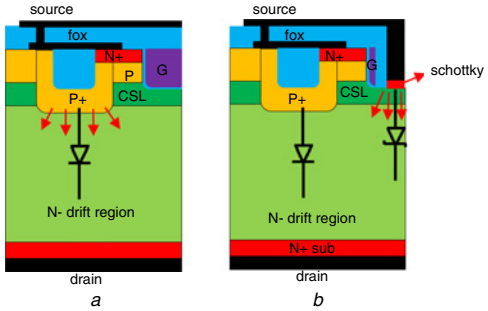

Fig. 1 *Device two-dimensional cross section for*
a Conventional UMOS structure
b Proposed MPS-UMOS design with Schottky contact embedded at trench bottom

A common design element in the UMOS and MPS diode structures is the p+ implant. The trench bottom oxide needs protection under high electric field (>3 MV/cm) while the Schottky contact has a similar requirement, it is possible to integrate the structures together as shown in Fig. 1*b*. The Schottky contact does not need an extra p+ region for electric field protection due to the existing, surrounding p+ regions. This reduces the total size compared to using an external/individual MPS diode.

Simulations of the proposed structure have been carried out in Silvaco, and the result of varying the p+ implant depth is shown in Fig. 2. This shows that Schottky reverse leakage current reduces with increased p+ implant depth as the Schottky surface becomes more effectively shielded from the peak of the electric field. With 2 µm p+ implant depth, the Schottky surface electric field is as low as 1.1 MV/cm and the trench bottom oxide electric field is below 1.3 MV/cm. The Schottky forward voltage drop increases slightly with increased p+ implant depth, however, it is not as sensitive as studied in [5]. A p+ implant depth of between 2 and 2.5 µm is a preferred design choice since it reduces the oxide and Schottky surface electric field and keeps a very low Schottky reverse leakage current without sacrificing a significant on-state performance.

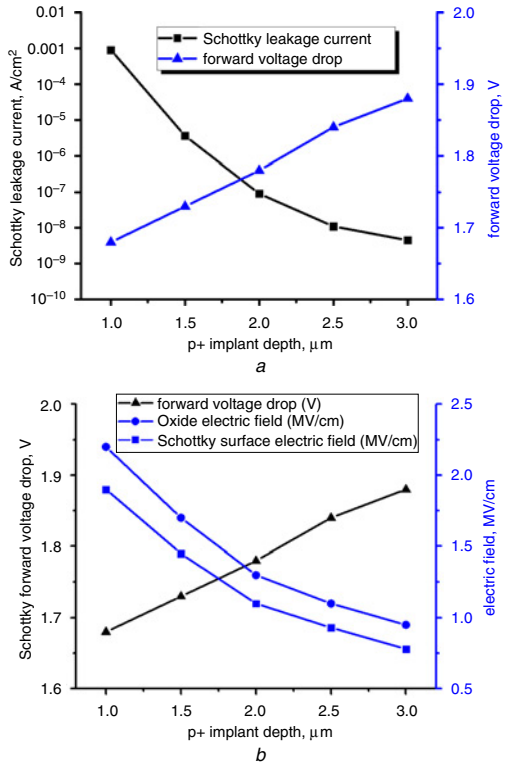

Fig. 2 *Simulated trade-off plot of Schottky forward drop at 200 A/cm²*
a Versus reverse leakage current density at 1000 V
b Versus trench bottom oxide electric field and Schottky surface electric field at 1000 V

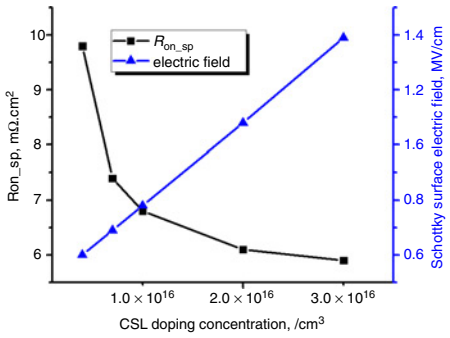

Fig. 3 *Trade-off for CSL doping concentration*

Another design parameter is the current spreading layer (CSL) doping concentration. There will be a trade-off between the specific on-resistance (R_{on_sp}) and Schottky surface electric field referring to Fig. 3. A proper doping concentration between 1×10^{16} and 2×10^{16} cm^{-3} is most suitable to keep both R_{on_sp} and Schottky contact surface electric field at relatively low levels.

Silvaco mixed mode tool is used to simulate the dynamic performance of the MPS-UMOS structure in comparison with conventional

UMOS with and without external SBD. Fig. 4 shows the clamped inductive switching circuit diagram used in mixed mode simulation. A standard double pulse test was used to characterise device turn-on and turn-off performance. The chip dimension is fixed at 0.1 cm^2 for UMOS, MPS-UMOS and external SBD.

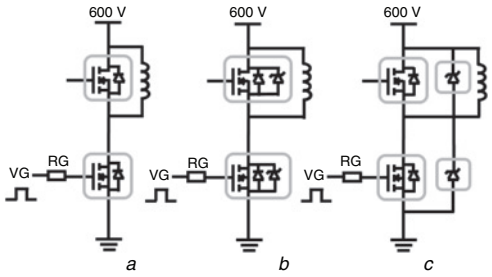

Fig. 4 *Double pulse simulation circuit for*
a Conventional UMOS
b MPS-UMOS
c Conventional UMOS with external SBD

It is shown in Fig. 5 that if the body diode of conventional UMOS is used for freewheeling, there is significant reverse recovery charge Q_{rr}. The proposed MPS-UMOS has suppressed the peak current due to the high side diode recovery since the integrated Schottky diode is responsible for current freewheeling. The UMOS/SBD setup has a high current flowing into the UMOS during turn-on. This is because the use of external SBD increases the total chip area, hence increasing capacitive charge. This capacitive stored energy will be released into the MOSFET for each switching cycle, which is why UMOS/SBD has higher turn-on loss compared to MPS-UMOS. In addition, using an external Schottky diode increases the total chip count and hence affects the package design. After embedding Schottky diode into the MOSFET structure, the power module can be made more compact with higher power density.

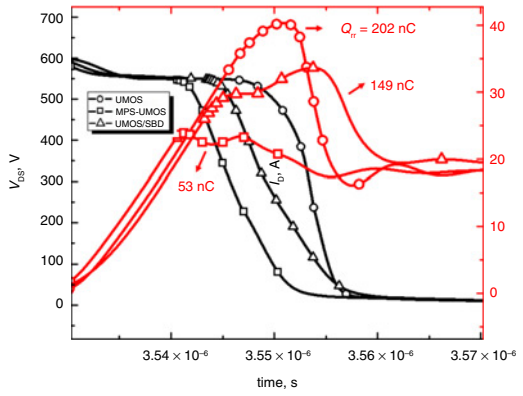

Fig. 5 *Turn-on switching transient for low-side UMOS where lifetime τ is set to 100 ns and* $R_G = 10\ \Omega$

Minority carrier lifetime is the dominant factor when considering minority carrier charge storage in a bipolar device. For MPS-UMOS and UMOS/SBD configurations, the Schottky diode is responsible for current freewheeling, therefore lifetime has no effect on the switching performance. In Fig. 6, it is shown that if the carrier lifetime (τ) reduces to 10 ns, the switching energy loss of conventional UMOS becomes very similar to the UMOS/SBD and the proposed MPS-UMOS setups. The MPS-UMOS and UMOS/SBD setups start to have advantages over the conventional UMOS when the lifetime is above 30 ns. With $\tau = 1$ µs, the effect of using Schottky diode instead of MOSFET body diode becomes significant since it reduces the switching energy loss by nearly 50% which is preferable for high-frequency switching circuit design.

Although the proposed MPS-UMOS design has great advantages over the conventional UMOS structure, it also adds two extra steps to the fabrication processes which is the self-aligned gate material etch and Schottky contact formation. The processing difficulty and cost are increased at the initial stage, however, this will no longer be an issue after process development and should bring the benefits into the system design.

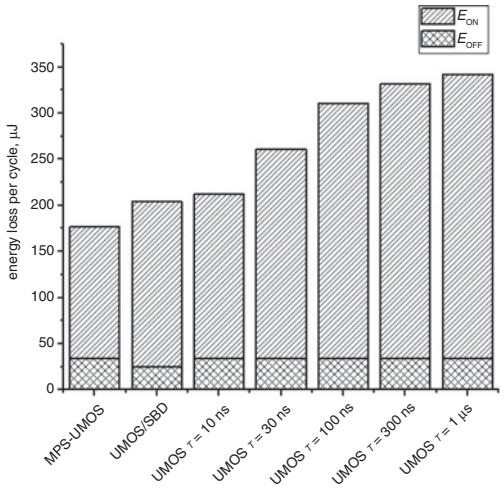

Fig. 6 *Switching loss of low-side MOSFET against different configurations*

Conclusion: The proposed MPS-UMOS structure which features a Schottky diode embedded at the trench bottom has shown reduced switching energy loss compared to the conventional UMOS with body PiN diode conduction. This is due to the elimination of reverse recovery by using the embedded Schottky diode for freewheeling. The Schottky contact in the proposed MPS-UMOS device uses the deep p+ region in the UMOS structure to form MPS diode which saves the total chip area effectively compared with UMOS and external Schottky diode. Power module packaged without external diode will have less chip counts and hence more compact design is possible. The same design can also be extended to high-voltage device structures.

Acknowledgment: This work was supported by EPSRC (grant EP/L007010/1). All data are provided in full in this paper.

Submitted: *20 August 2017* E-first: *13 December 2017*
doi: 10.1049/el.2017.3198
One or more of the Figures in this Letter are available in colour online.

Tianxiang Dai, Chun Wa Chan, Peter M. Gammon, Mike R. Jennings and Phil A. Mawby (*School of Engineering, University of Warwick, Coventry CV4 7AL, United Kingdom*)

✉ E-mail: T.Dai@warwick.ac.uk

Xc Deng (*School of Engineering, University of Electronic Science and Technology of China, Chengdu 610054, People's Republic of China*)

Huaping Jiang (*Dynex Semiconductor Ltd., Lincoln, United Kingdom*)

References

1 Liu, G., Ahyi, A.C., Xu, Y., *et al.*: 'Enhanced inversion mobility on 4H-SiC (11-20) using phosphorus and nitrogen interface passivation', *Electron Device Lett.*, 2013, **34**, (2), pp. 181–183
2 Jiang, H., Wei, J., Dai, X., *et al.*: 'SiC MOSFET with built-in SBD for reduction of reverse recovery charge and switching loss in 10-kV applications'. 29th Int. Symp. on Power Semiconductor Devices and ICs (ISPSD), Sapporo, Japan, May 2017, pp. 49–52
3 Calafut, D.: 'Trench power MOSFET lowside switch with optimized integrated Schottky diode'. 16th Int. Symp. on Power Semiconductor Devices and ICs, 2004, Kitakyushu, Japan, May 2004, pp. 397–400
4 Harada, S., Kobayashi, Y., Ariyoshi, K., *et al.*: '3.3-kV-class 4H-SiC MeV-implanted UMOSFET with reduced gate oxide field', *Electron Device Lett.*, 2016, **37**, (3), pp. 314–316
5 Zhu, L., and Chow, T.P.: 'Advanced high-voltage 4H-SiC Schottky rectifiers', *Trans. Electron Devices.*, 2008, **55**, (8), pp. 1871–1874