Performance of SiC Cascode JFETs under Single and Repetitive Avalanche Pulses

S.N Agbo, J. Ortiz-Gonzalez and O. Alatise

Abstract

In this paper, we investigate the single and repetitive avalanche performance and characteristics of different SiC device technologies including SiC cascode JFETs and SiC Trench MOSFETs. SiC Cascode JFETs exhibit a different failure mode from SiC MOSFETs due to the interaction between the low-voltage (LV) silicon MOSFET and the high-voltage (HV) SiC JFET through the resistance connecting the MOSFET source to the JFET gate. MOSFETs fail in avalanche typically due to parasitic BJT latch-up and/or thermal hot-spotting leading to a source-to-drain short. However, cascode JFETs can fail with the low voltage MOSFET still functional and a low resistance measured between the cascode terminals. The failure point of SiC Cascode JFETs in avalanche is therefore not clearly identifiable and the failure criteria will have to be reassessed. Measurements and simulations show that the connection between the JFET gate and the MOSFET source influences the avalanche duration and avalanche power. Finite element simulations show that increased leakage through the gate resistance of the SiC JFET at higher temperatures causes delayed transients in the V_{DS} turn-OFF. Hence, the result is low-voltage avalanche turn-OFF where only the LV silicon MOSFET goes into avalanche and the JFET goes into linear mode. SiC Cascode JFETs show reduced performance under repetitive avalanche due to degradation of the JFET gate resistance and increased linear mode conduction of the SiC JFET. Failure analysis proves that the low voltage silicon MOSFET is unaffected while the avalanche current flows through the SiC JFET gate which appears to be shorted.

1. Introduction to SiC cascode

SiC MOSFETs are now an established power device technology competing with silicon MOSFETs and IGBTs in the 650 V to 1200 V application space [1]. Improved energy conversion efficiency is widely cited as a benefit of SiC devices along with high temperature operation and fast switching rates. The reliability and robustness of SiC devices is also increasingly under scrutiny. SiC MOSFETs are well known for good avalanche performance in comparison with silicon MOSFETs and IGBTs [2-10]. This is due to the wide bandgap and high critical electric field characteristics of SiC which means more energy is required to generate electron-hole pairs through impact ionization [9]. SiC has a higher electric field and therefore a reduced rate of impact ionization. Although SiC MOSFETs have smaller active areas and higher junction-to-case transient thermal impedance, they are nevertheless very rugged under single and repetitive avalanche cycling. However, SiC devices continue to have reliability challenges regarding the performance of the gate oxide under short circuits [11, 12], threshold voltage shift from bias temperature instability [13-16] and time dependent dielectric breakdown [17]. Stand-alone SiC JFETs have negative threshold voltages and therefore operate in depletion mode with high input gate standby (static) currents. Since this is not suitable for traditional power electronics that use normally-OFF devices with low standby gate currents, SiC JFETs were not widely accepted by the industry.

To avoid issues regarding gate oxide reliability in SiC MOSFETs while providing normally-OFF operation with low standby currents, SiC cascode JFETs have been proposed [18]. These cascode JFETs use low voltage (LV) silicon MOSFETs as the input and high voltage SiC JFETs for voltage blocking [19]. Since the source of the SiC JFET is connected to the drain of the silicon LV MOSFET and the gate of the SiC JFET is connected to the source of the silicon LV MOSFET, the switch combination will act as a normally-OFF device as long as the breakdown voltage of the LV-MOSFET is higher than the absolute value of the SiC JFET threshold voltage. When conventional MOSFETs fail under UIS, it is either due to

parasitic BJT latch-up with temperature/current hot-spots or average junction temperature rise exceeding the device thermal limits [8, 20-23]. The first failure mode is associated with short duration and high-power avalanche pulses (where there is insufficient time for heat to diffuse from the junction) while the second failure mode is associated with low power and long duration avalanche pulses (where there is sufficient time for heat flow from the junction to the case). Failure modes of power MOSFETs under repetitive avalanche are different from those under single-shot avalanche. Under repetitive avalanche conditions, degradation of the gate oxide due to hot-carrier-injection has been reported in SiC MOSFETs [2, 11, 24-26].

Less is known about how the SiC Cascode JFET fails in single or repetitive avalanche although some investigations have been made regarding the performance of these devices under short circuit conditions [27]. In this paper, we investigate failure modes and peculiarities of SiC cascode JFETs under single and repetitive pulses of unclamped inductive switching (UIS). In section 2, we show experimental measurements of the avalanche performances of SiC Trench MOSFETs and Cascode JFETs under UIS and explain how the failure modes differs between them. In section 3 we use finite element simulations from SILVACO to explain the failure mode in SiC cascode JFETs. In section 4 we present the performance of the devices under repetitive UIS. In section 5 we discuss the results and introduce failure-analysis techniques used for analysing SiC Cascode JFETs while in section 6 we conclude the paper.

2. Single Pulse Avalanche

The avalanche ruggedness of power devices is tested using the unclamped inductive switching circuit shown in Fig. 1(a) for the SiC cascode JFET and Fig. 1(b) for the conventional SiC MOSFET. A gate pulse is applied to the device under test (DUT) which conducts a current thereby charging the inductor. As the DUT is turned-OFF, the inductor discharges its energy into the DUT thereby setting it into avalanche since there is no channel to conduct the current. The peak current is set by the duration of the gate pulse while the avalanche duration is set by the size of the inductance.

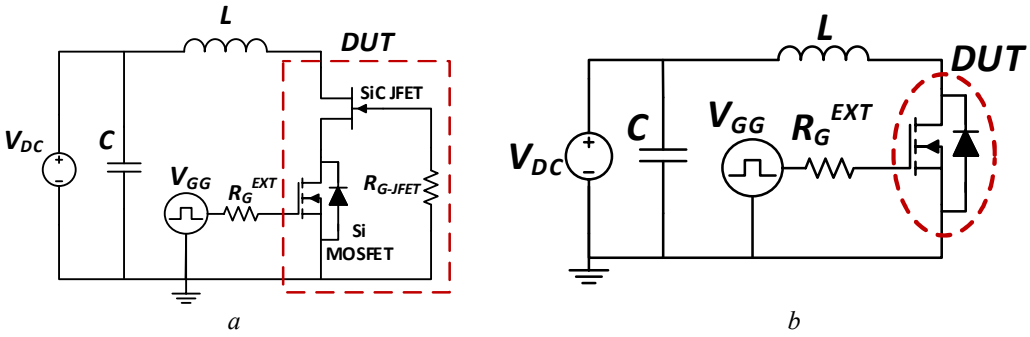
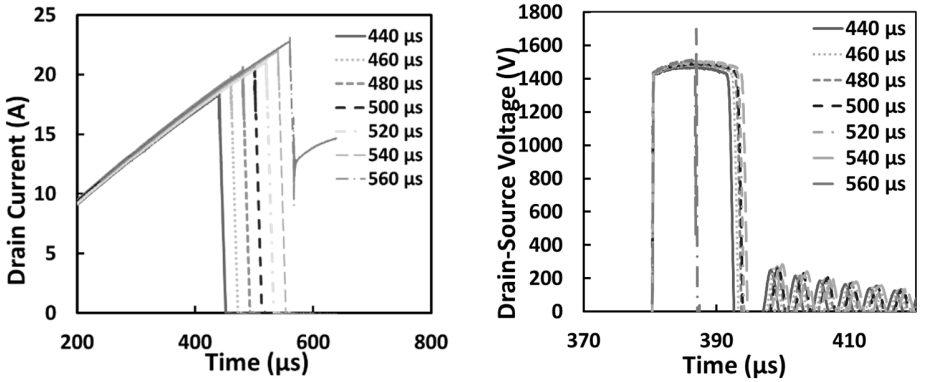


Fig. 1 Single shot avalanche test circuit for (a) SiC Cascode JFET and (b) SiC MOSFET

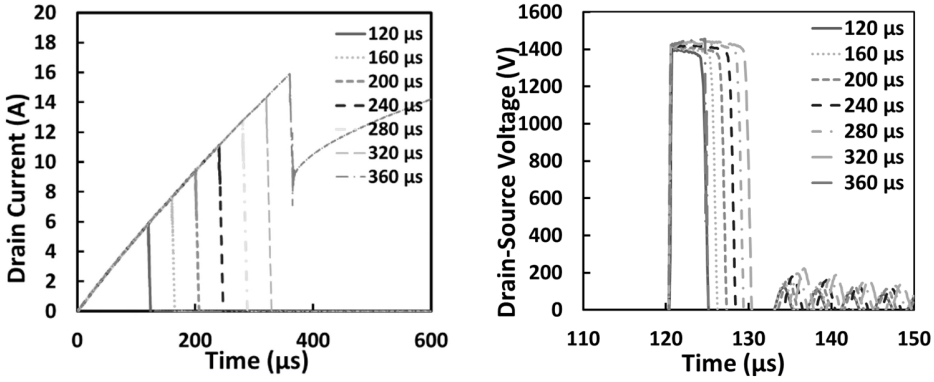
Tests were performed on a 650V SiC Trench MOSFET with datasheet reference SCT3060AL and a 650 V SiC Cascode JFET with datasheet reference UJ3C065080K3S. By using an electric heater attached to the back side of the device, single pulse UIS tests were performed at ambient (25 °C) and at high case temperatures (105 °C). By ensuring sufficient time for the system to reach thermal steady-state, it can be assumed that the junction and case temperatures are equal before the avalanche pulse. The avalanche pulse then increases the junction temperature to peak determined by avalanche power pulse and the junction-to-case transient thermal impedance of the device. By increasing the length of the gate pulse, the avalanche current was increased until the device failed during avalanche conduction. Fig. 2(a) shows the avalanche current waveforms for the SiC trench MOSFET while Fig. 2(b) shows the corresponding measured avalanche voltage waveforms. Failure is evident at the point where the avalanche current starts rising which

coincides with the point where the avalanche voltage drops to zero. The measurements performed at a case temperature of 105 °C are shown in Fig. 3(a) and Fig. 3(b) for the avalanche currents and voltages respectively. By comparing the high and low temperature measurements, it is evident that increasing the temperature reduces the peak avalanche current before failure. In terms of avalanche energy, increasing the case temperature from 25 °C to 105 °C reduces the maximum avalanche energy before failure from 229.25 mJ to 94.46 mJ.



a *b*

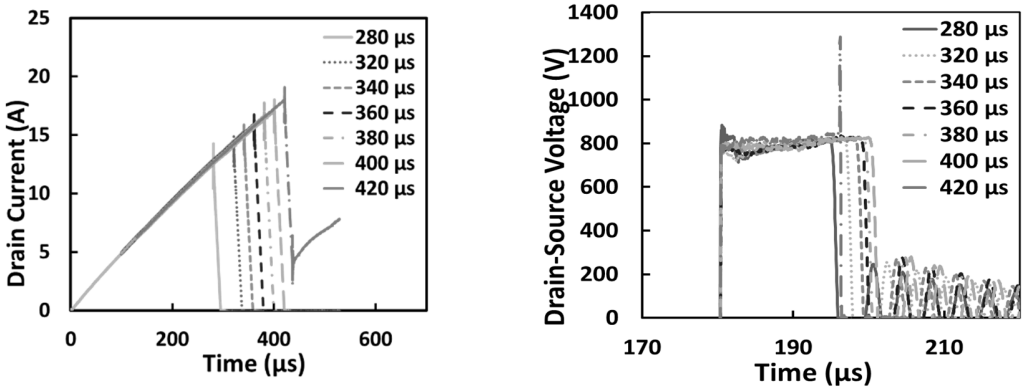
Fig. 2 (a) Avalanche current waveforms for SiC Trench MOSFET at 25 °C, (b) Avalanche voltage waveforms for SiC Trench MOSFET at 25 °C



a *b*

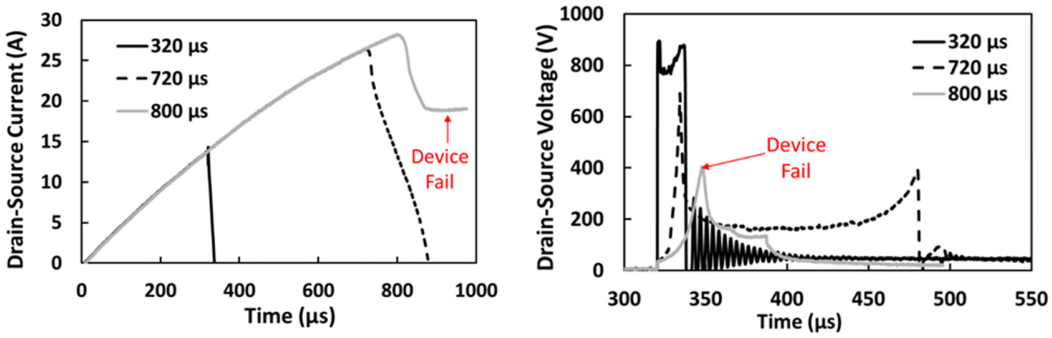
Fig. 3 (a) Avalanche current waveforms for SiC Trench MOSFET at 105 °C (b) Avalanche voltage waveforms for SiC Trench MOSFET at 105 °C.

Similar single shot avalanche measurements were performed on the SiC cascode JFET. Fig. 4(a) shows the incremental avalanche currents until device failure at 25 °C while Fig. 4(b) shows the corresponding avalanche voltage measurements. However, as the case temperature is increased to 105 °C, the avalanche characteristics in the SiC Cascode JFET exhibits non-typical characteristics. These include delayed voltage rise during turn-OFF and reduced peak avalanche voltages with prolonged avalanche duration at higher energy pulses. The avalanche energy dissipated by the SiC Cascode JFET was 154.03 mJ at 25 °C and 230.5 mJ at 105 °C.



a *b*

Fig. 4(a) Avalanche current waveforms for SiC Cascode JFET at 25 °C (b) Avalanche voltage waveforms for the SiC Cascode JFET at 25 °C

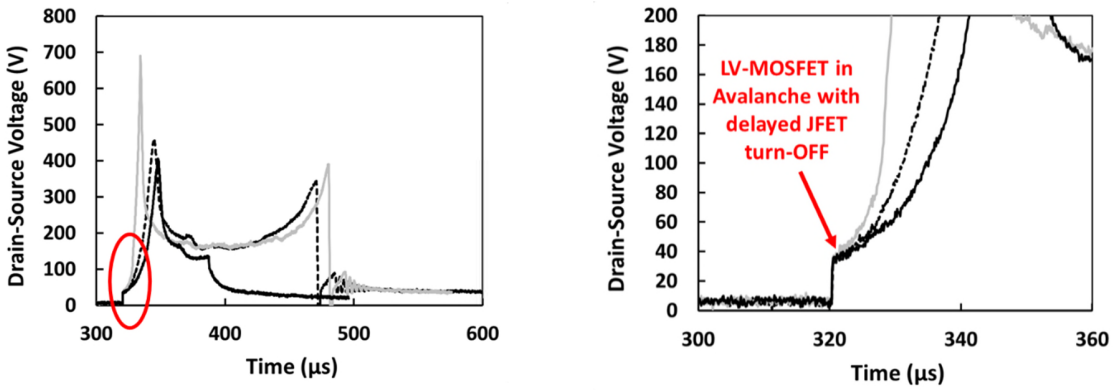


a *b*

Fig. 5(a) Avalanche current waveforms for SiC Cascode JFET at 105 °C (b) Avalanche voltage waveforms for the SiC Cascode JFET at 105 °C.

Closer inspection of the avalanche voltage characteristics of the SiC cascode JFET shown in Fig. 5(b) shows that the SiC JFET undergoes delayed turn-OFF while the LV Silicon MOSFET goes into avalanche. Fig. 6(a) shows a closer inspection of the avalanche voltage transient of the SiC cascode JFET while Fig. 6(b) shows the zoomed in version. The knee-point in Fig. 6(b) shows that the LV silicon MOSFET is in avalanche while the SiC JEFT undergoes a delayed turn-OFF. This means that the SiC JFET operates in the linear mode (high voltage and current) while the LV-MOSFET is in avalanche. To further understand

this, finite element simulations of SiC Cascode JFETs in avalanche have been performed alongside SiC trench MOSFETs.



a *b*

Fig. 6(a). Avalanche voltage transient showing delayed turn-OFF of the SiC JFET while the LV Si MOSFET is in avalanche. (b). Zoomed in version of A.

3. Finite Element Simulations

In this section, we show SILVACO finite element simulations of Unclamped Inductive Switching (UIS) in SiC Trench MOSFETs and Cascode JFETs to explain the observations in the SiC Cascode JFET. The SiC devices are designed in SILVACO with appropriate meshing and parameters defined in Table 1. Since failure under avalanche is electrothermal, the simulations here include the heat-flow equations invoked by the simulator using LAT.TEMP. The heat-flow equation is coupled with the Poisson-continuity equations and the thermal boundary condition is specified using lumped parameters. By specifying the ambient (case) temperature and the thermal conductance of the model, junction temperature excursions can be accounted for. The mobility models used account for temperature dependence and electric-field dependence. Since the avalanche duration in the simulations and measurements (which is in µs) are significantly smaller than the packaging thermal time constants (which ranges from milliseconds and seconds), for this study, it can be assumed that the case-to-ambient remains isothermal i.e. there is insufficient time for the heat generated from avalanche to diffuse through the multi-layer packaging system including solder and lead-frame. The impact ionization model used in the simulation is the Selberherr model which accounts for hot and cold carrier populations [28]. Using the mixed-mode circuit simulator, the meshed device is simulated in a circuit similar to that in Fig. 1. The avalanche current and voltage waveforms extracted from the simulator are shown in Fig. 7(a) and Fig. 7(b) for the SiC Trench MOSFET under UIS. Three points (A, B and C) in the avalanche current transients have been selected for closer investigation. Point A is an instant in time when the device is conducting current normally through the channel and charging the inductor. At point B, the MOSFET is in avalanche, but has not undergone parasitic BJT latch up while at point C, the device is undergoing BJT latch-up. Thermal failure in the simulation occurs when the temperature limit of the semiconductor is reached. The thermal limit is set by the density of thermally generated carriers. Since the simulation assumes that the temperature is uniformly distributed across the chip area, the theoretical thermal limit of the semiconductor is reached. However, in a real device, electrothermal non-uniformities across the chip means that thermal hot-spots are generated hence, the average temperature of the chip is well below the thermal limits. Furthermore, the thermal limits of the source metallisation and wirebonds are lower than that of the semiconductor. Using the TonyPlot tool in SILVACO, 2-dimensional cross-sectional images have been extracted to further investigate the current flow paths during avalanche. The current densities and electric fields within the device during stages A (conduction), B (avalanche) and C (electrothermal failure) have been extracted.

Table 1 Parameters used for finite element simulations of the SiC Trench MOSFET and Cascode JFET

SiC Trench MOSFET Parameters	Value	SiC Cascode JFET Parameter	Value
Trench depth	1.2 µm	LV-MOSFET Breakdown Voltage	28 V
Drift layer thickness	5.8 µm	MOSFET gate oxide thickness	50 nm
Substrate doping	1x19 cm-3	MOSFET p-body doping	8x17 cm-3
N-source doping	1x19 cm-3	SiC JFET drift layer thickness	6.2 µm
p-body doping	4x17 cm-3	SiC JFET drift layer doping	2.33x16 cm-3
Oxide thickness	50 nm,100 nm	SiC JFET channel width	1 µm
Drift layer doping	$6.5x10^{15}$cm-3	SiC JFET gate p-doping	1x19 cm-3
SiC MOSFET gate resistance	10 Ω	Cascode JFET gate resistance	Varies
Avalanche Inductor	1 mH	Avalanche Inductor	1 mH

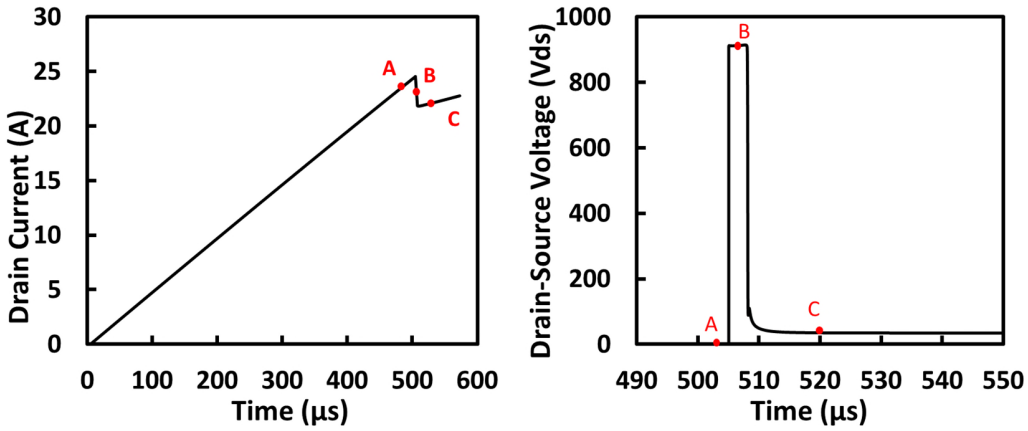
Fig. 8 shows the simulated current density while Fig. 9 shows the simulated internal electric field for the SiC Trench MOSFET during time instants A, B and C. The Trench MOSFET is clearly labelled with the body diode. It can be seen from Fig. 8 that

a) At point A, when the device conducts current normally through the channel, the current density is highest near the gate sidewall and spreads through the drift region. The electric field is confined to the channel.
b) At point B when the device is in avalanche, current diverts to the embedded PN body diode away from the channel and the peak electric field moves to the PN junction indicating that the device is blocking voltage while conducting a high current.
c) At point C, when the MOSFET is undergoing electrothermal failure, the current spreads through the NPN structure. Here, the internal electric field drops thereby indicating the device no longer blocks voltage.

Finite element simulations have also been performed for the SiC cascode JFET under UIS. Simulated avalanche current and voltage transients are respectively shown in Fig. 10(a) and Fig. 10(b). The avalanche characteristics of the SiC Cascode JFET are similar to that of the SiC Trench MOSFETs however, due to the differences between the MOSFET and the JFET, the internal current flow paths are different. Fig. 11 and 12 shows the current densities and electric fields within the JFET at points A, B and C. Unlike the SiC Trench MOSFET, in the JFET, the current flow path during conduction, and avalanche are similar with the only difference being that in conduction, the channel is open, hence the electric fields are low (seen in Fig. 12(a)), whereas in avalanche, the channel is pinched OFF as evident by the high electric fields seen in Fig. 12(b) and reduces after failure as in 12(c).

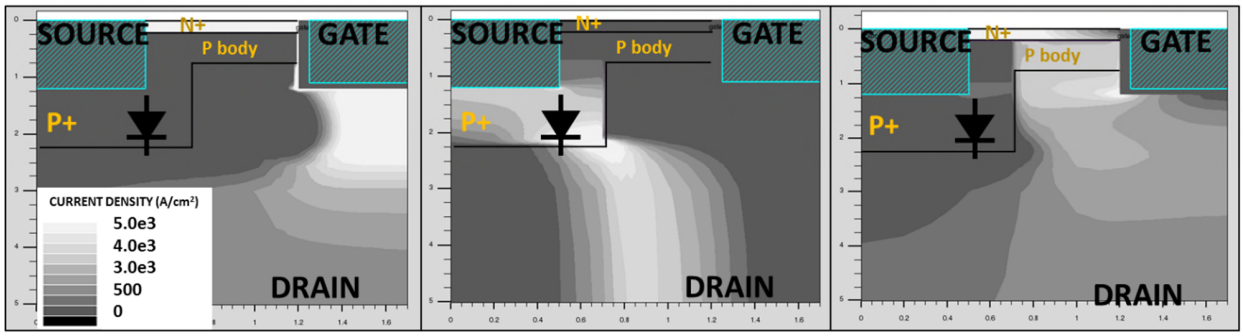
As will be recalled from Fig. 6, the SiC Cascode JFET shows atypical avalanche characteristics evident in the delayed avalanche voltage transient resulting in low voltage turn-OFF. There was also a dip in the avalanche voltage waveform indicating that the SiC JFET was operating in linear mode (partially ON). This characteristic was evident at higher case temperatures, thereby indicating that a temperature induced mechanism was causing the JFET turn-OFF dV/dt to reduce. SiC cascode JFETs have a resistance connected between the source of the LV-MOSFET and the gate of the HV SiC-JFET [29]. This gate resistance ($R_{G\text{-}JFET}$) is fundamental for dV/dt control of the cascode device [30]. To reproduce the experimental observations shown in Fig. 6, the resistance between the JFET gate and LV-MOSFET source (R_{GJFET}) is varied in the simulator. Fig. 13 and 14 shows the results of the simulations for $R_{G\text{-}JFET}$=1 Ω and 400 Ω respectively. The high value of $R_{G\text{-}JFET}$=400 Ω is chosen to emulate the characteristics of the cascode JFET under UIS conditions where some electrothermal damage has occurred most likely through high current flow through $R_{G\text{-}JFET}$ combined with high case/junction temperatures. It can be observed that Fig. 13 models the SiC Cascode JFET avalanche characteristics at room temperature while Fig. 14 models the characteristics at higher external temperatures. The dual slope in the avalanche current indicates the partial turn-ON of the SiC JFET during avalanche. This occurs at the same time as the dip in the V_{DS} waveform.

Also shown in Fig. 13 and 14 are the current flow paths for the different avalanche conditions. The SiC Cascode JFET goes into linear mode because of the significant voltage drop across the gate resistance thereby partially turning the JFET on.



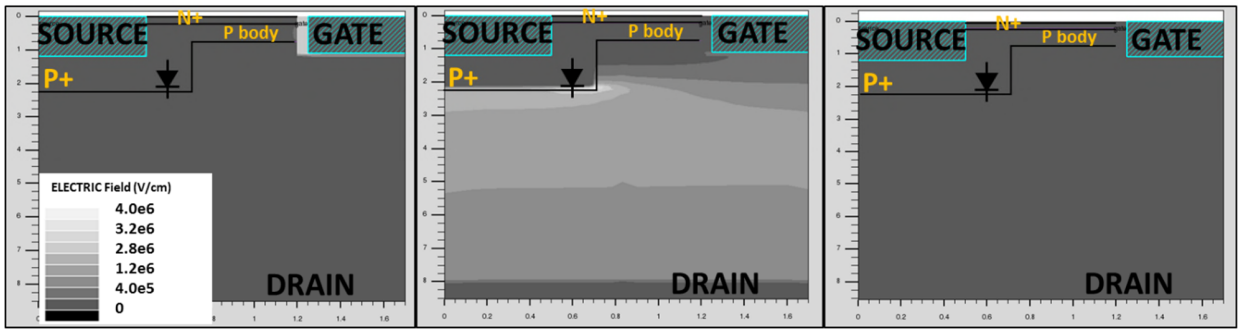
a *b*

Fig. 7. Simulated avalanche (a) Current and (b) Drain-source voltage of SiC Trench MOSFETs undergoing failure under UIS



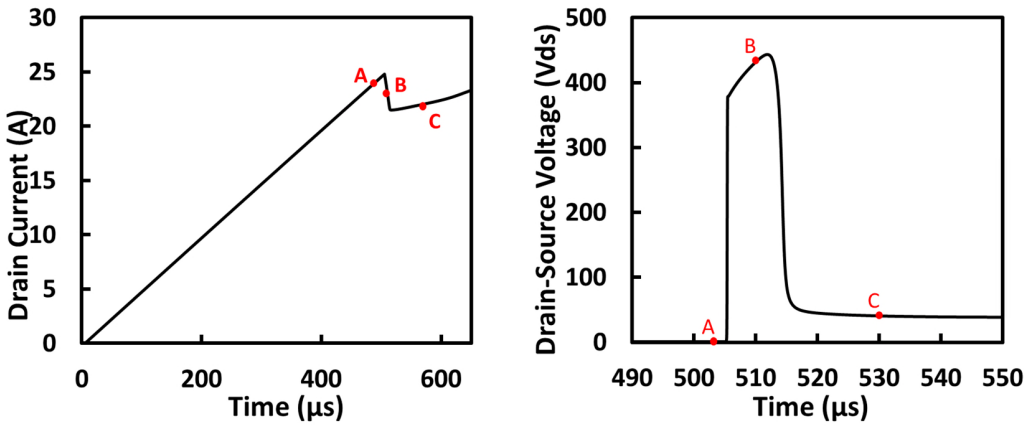
a *b* *c*

Fig. 8. 2D-Current density contour plots showing current flow path at points A, B and C in the SiC Trench MOSFET



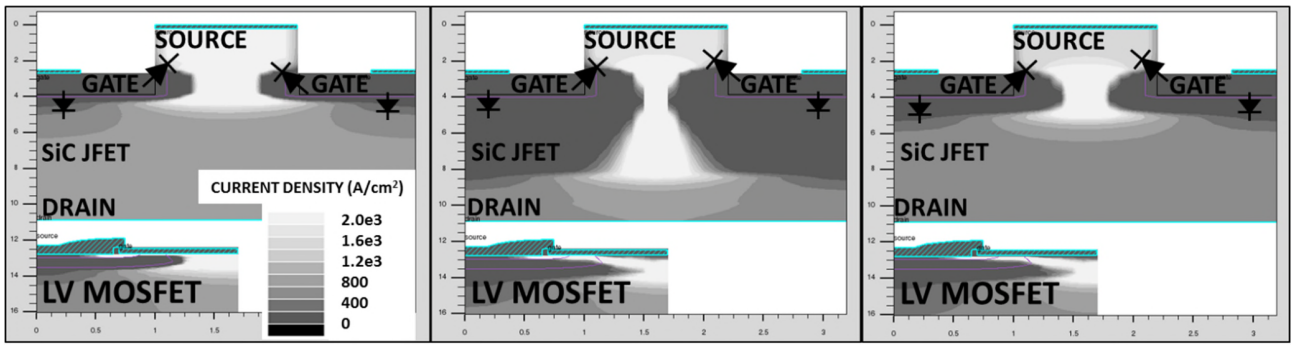
a *b* *c*

Fig. 9. 2D-Electric Fields contour plots showing E-field lines at points A, B and C in the SiC Trench MOSFET



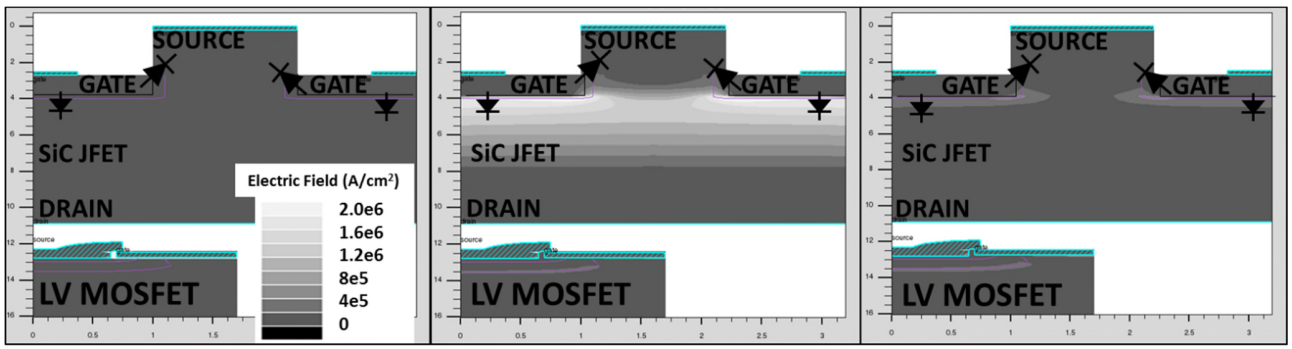
a *b*

Fig. 10. Simulated Avalanche (a) current and (b) Voltage for the SiC Cascode JFET during UIS showing conduction (A), avalanche (B) and electrothermal failure (C).



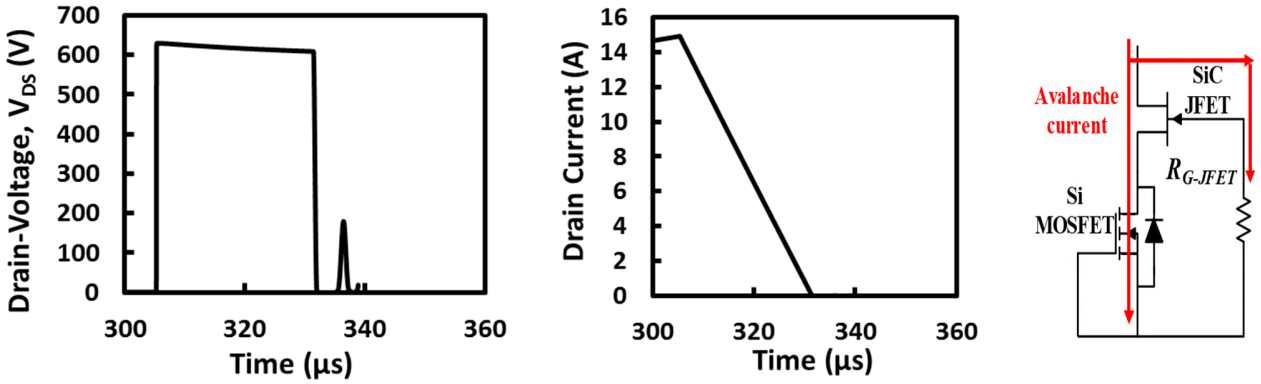
a *b* *c*

Fig. 11. 2D-Current density contour plots showing current flow path at points A, B and C in the SiC Cascode JFET



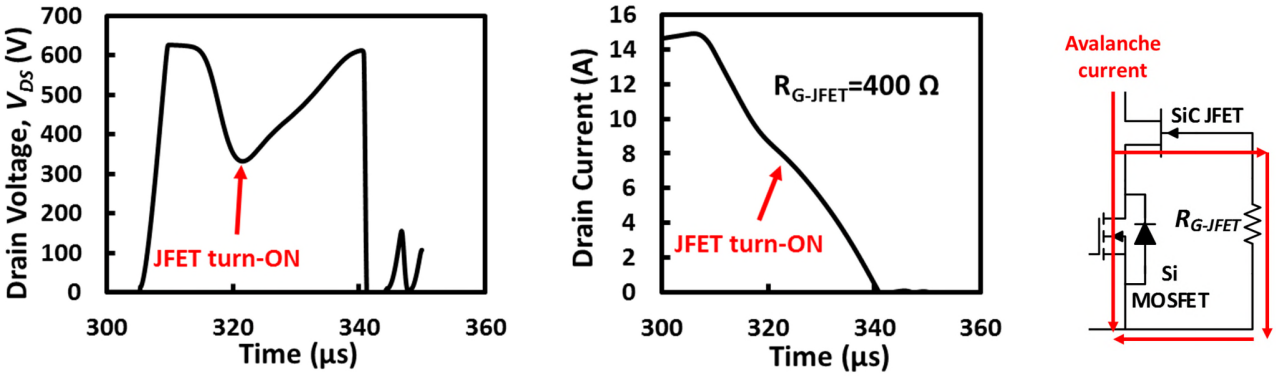
a *b* *c*

Fig. 12. 2D-Electric Fields contour plots showing E-field lines at points A, B and C in the SiC SiC Cascode JFET



a *b* *c*

Fig. 13. Simulated (a) V_{DS} and (b) I_G for SiC Cascode JFET with $R_{G\text{-}JFET}$=1Ω and (c) Current path

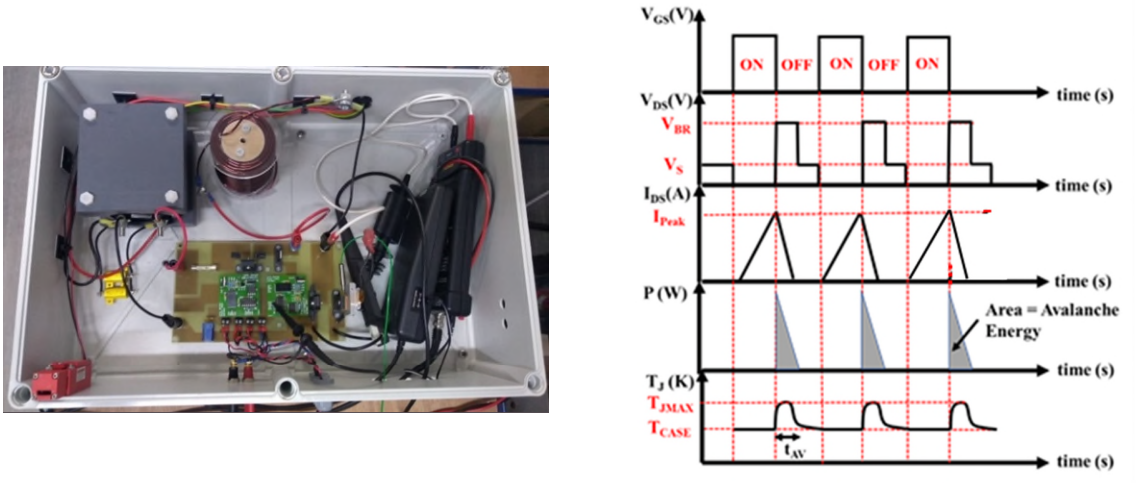


a *b* *c*

Fig. 14. Simulated (a) V_{DS} and (b) I_G for SiC Cascode JFET with $R_{G\text{-}JFET}$=400Ω and (c) Current path

4. Repetitive Avalanche Measurements

The repetitive avalanche tests are performed using the circuit below with the picture in Fig. 15(a). Shown in Fig. 15(b) is a generic representation of the repetitive avalanche transient voltages, currents and idealized power and temperature plots. Devices under repetitive avalanche undergo periodic junction temperature excursions proportional to the avalanche power dissipated. The repetitive avalanche tests were performed in order to investigate the evolution of the anomalous V_{DS} transients in the SiC cascode JFET.

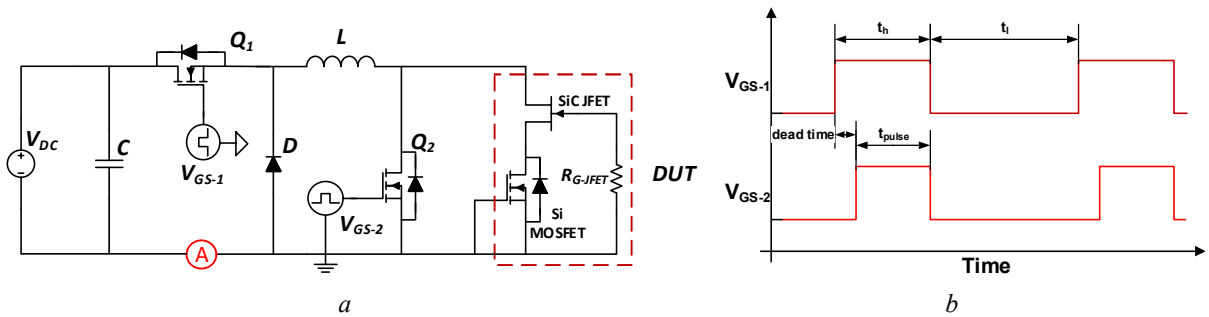


a *b*

Fig. 15 (a) Repetitive avalanche circuit, (b) Repetitive avalanche waveforms

In the repetitive avalanche circuit, there are three additional devices (2 transistors and a diode) along with the DUT. This circuit has been designed to enable failure analysis by separating the failure of the SiC JFET from the LV silicon MOSFET. Auxiliary transistor Q1 is required for isolating the DC power supply from the DUT, which is highly relevant for the SiC Cascode JFET tests, since the failure of the JFET into short circuit can lead to the LV silicon MOSFET being exposed to full DC voltage (which is higher than the rated voltage of the LV silicon MOSFET). The test sequence is as follows

1) First Auxiliary transistor Q1 is turned ON while the other devices are OFF. If there are no fails, there should be no current, hence, this stage is for checking for short circuit fails.
2) After a short deadtime, auxiliary transistor Q2 is also turned ON thereby charging the inductor to a desired current value depending on the load inductance and the pulse duration.
3) Both auxiliary transistors Q1 and Q2 are simultaneously turned OFF thereby causing the inductor to discharge its stored energy in the DUT while the diode D1 ensures the circuit is closed.



a *b*

Fig. 16. (a) Repetitive avalanche circuit showing auxilliary devices (b). Test sequence pulses for the auxildliary devices.

It is important to note that the current and voltage ratings of the auxiliary transistors should be higher than the DUT. The inductor used in the repetitive avalanche measurements is a 1 mH inductor and the DC voltage used is 50 V. A heatsink was attached to the device and the case temperature was monitored. The time interval between each avalanche pulse is sufficient to ensure that the case temperature rises by less than 3-4 °C. Since the peak avalanche current plays a critical role in the performance of the device, investigations in this paper have been performed with different peak avalanche currents, as summarised in Table 2 and Table 3.

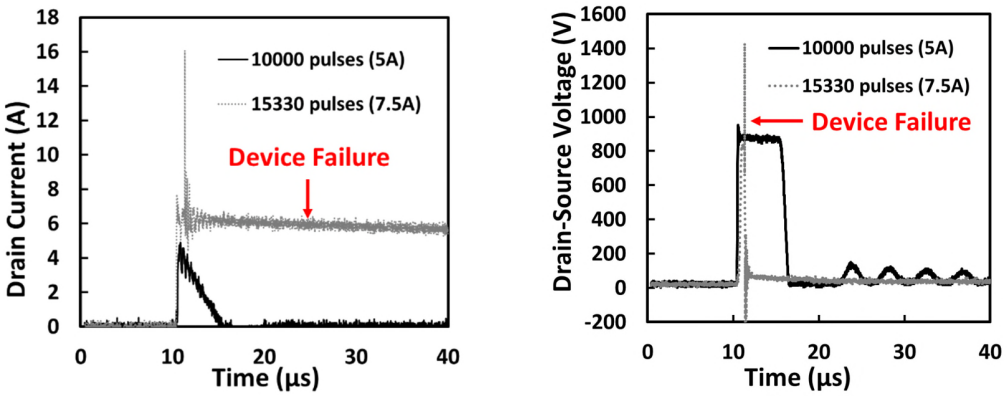
Cycle number	Avalanche current (A)
1-20000	5
20001-40000	7.5

Table 2. Repetitive avalanche pulses for device A

Cycle number	Avalanche current (A)
1-20000	5

Table 3. Repetitive avalanche pulses for device B

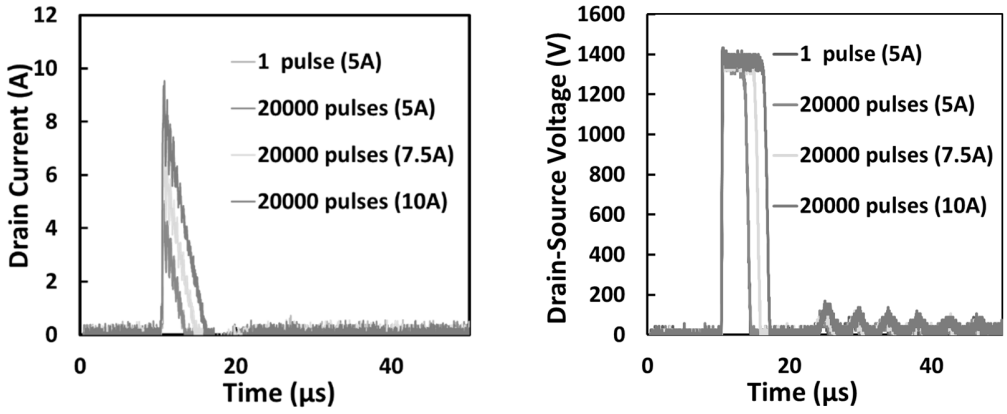
Fig. 17(a) shows the avalanche current waveform after 10,000 pulses of 5 A peak current along with the last avalanche pulse where failure occurs. Fig. 17(b) shows the corresponding avalanche voltage transients. It can be observed that during the failure pulse, the current through the device does not fall to zero while the voltage across the device drops to zero early in the avalanche pulse.



a *b*

Fig. 17. Cascode Repetitive Avalanche (a) current and (b) voltage after 10000 pulses and during failure

Repetitive avalanche measurements have also been performed on the SiC Trench MOSFETs under identical conditions. Fig. 18(a) and (b) respectively show the avalanche current and voltage waveforms after 20000 cycles at each avalanche current level, from 5 A to 10 A. It is apparent that no anomalous avalanche characteristics are observed, and the device exhibits the typical characteristics.



a *b*

Fig. 18. (a) Repetitive avalanche current characteristics for SiC Trench MOSFET (b) Repetitive avalanche voltage characteristics for SiC Trench MOSFET

5. Failure Analysis

Failure analysis has been performed on the SiC trench MOSFETs and SiC Cascode JFET. As part of failure analysis, the source-drain resistance (R_{SD}) as well as drain source resistance (R_{DS}) was measured across devices that have failed in avalanche to determine the nature of the short circuits across the device terminals. These measurements were made with the gate shorted to the source. Generally, R_{SD} was equal to R_{DS} in both devices. While the SiC Trench MOSFETs exhibited very low R_{SD} (0.5 to 2.4 Ω) thereby indicating a short circuit between the source and drain, the SiC Cascode JFET exhibited a higher R_{SD} (between 5.2 and 23.8 Ω) in failures under repetitive avalanche.

Gate capacitance measurements were also performed on both the SiC Trench MOSFET and Cascode JFET to determine the state of the oxide. While the gate-source terminal in the SiC Trench MOSFET was shorted (indicating a damaged oxide), in the case of the Cascode JFET, the gate oxide was still capable of blocking voltage. Fig. 19 shows the gate voltage charging measurements on one unstressed SIC cascode JFET device and three other devices that failed under repetitive avalanche. The measurements indicate that the LV silicon MOSFET that acts as the gate input into the Cascode arrangement may still be functional.

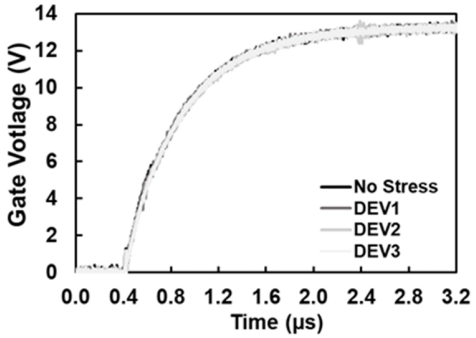


Fig. 19. Gate voltage charging measurements with 220 Ω gate resistance.

Further FA tests were performed on the SiC Cascode JFET to determine the state of the body diode of the LV silicon MOSFET. For the SiC Cascode JFET, assuming that the JFET has been short-circuited from avalanche over-stress, Fig. 20(a) and (b) below show the equivalent circuits. If a drain-source voltage is applied, the LV MOSFET body diode is reverse biased, hence, current flows through the shorted JFET and its gate resistance ($R_{G\text{-}JFET}$). On the contrary, if a sufficient source-drain voltage (V_{SD}) is applied to forward bias the body diode, then there is a current divider between the forward biased diode and the SiC JFET gate resistance ($R_{G\text{-}JFET}$). This is shown in Fig. 20(b). In this case, the current divider depends on whether or not the body diode is forward biased. If the V_{SD} voltage is below the body diode knee voltage, then current only flows through the SiC JFET gate resistance ($R_{G\text{-}JFET}$). If the V_{SD} voltage is above the diode knee voltage, then current will flow mainly through the LV MOSFET body diode since it will have a lower on-state resistance.

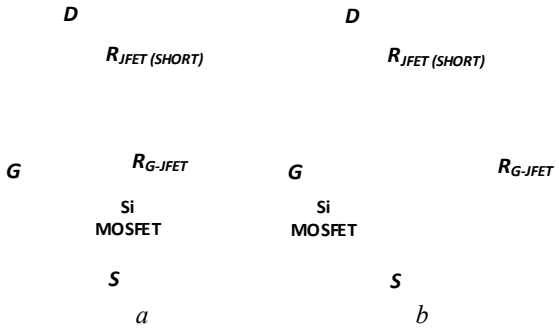


Fig. 20. Equivalent circuits for the failed SiC Cascode JFET

To verify this, the 3rd quadrant characteristics (with V_{GS} = 0V) were measured for the unstressed and failed devices. When observing these characteristics, it is important to note that at low V_{SD} (below the knee voltage of the diode), a properly functioning Cascode JFET should not have any current flow since the diode is not forward biased and the JFET is not ON. This is shown in Fig. 21(a). However, in a Cascode device with a shorted JFET (due to failure under avalanche), at low V_{SD}, there will be current flowing in the circuit. This is shown in Fig. 21(b) where a non-zero current is evident before the knee voltage of the body diode.

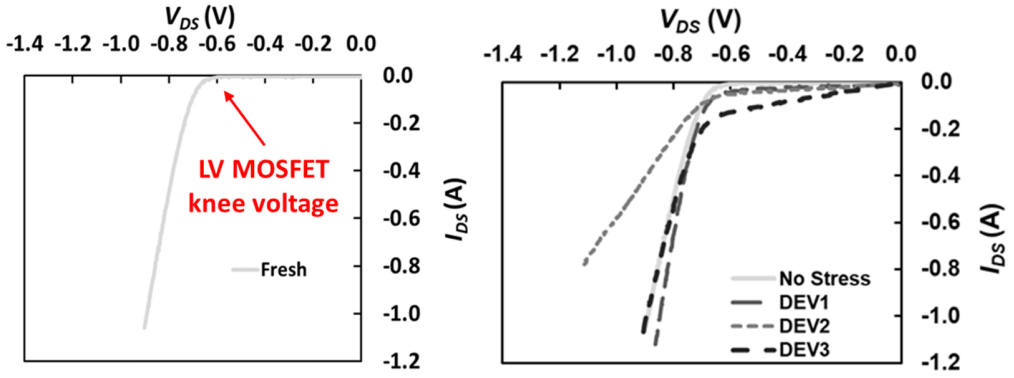


Fig. 21. 3rd qudrant characteristics of (a) unstressed SiC Cascode JFET and (b) damaged SiC Cascode JFET Devices (1,2, and 3)

If the low voltage Si MOSFET is not damaged it will be possible to turn it ON and the current will flow through the channel of the MOSFET. In order to verify this assumption, a test has been defined, with the schematic shown in Fig. 22. It consists of a resistive load switching test, where the current (I_S) and voltage across the device V_{DS} are measured. The selection of the resistive load is important as the failed devices are not able to block voltage. In this test, the current will flow through the series combination of R_{DEVICE} and R_{LOAD} as defined by equation (1).

$$I_S = \frac{V_{DC}}{R_{DEVICE}+R_{LOAD}} \qquad (1)$$

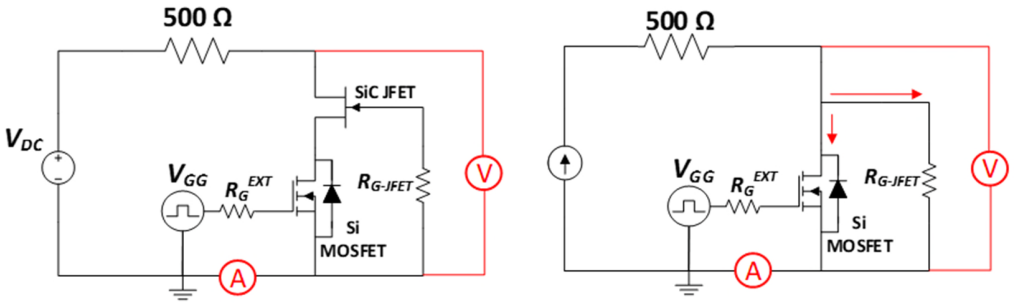
The voltage across the device is given by a resistive divider, where R_{DEVICE} is a function of the gate voltage level and the measured voltage is determined by equation (2).

$$V_{DS} = \frac{R_{DEVICE}}{R_{DEVICE}+R_{LOAD}} V_{DC} \qquad (2)$$

For an unstressed device, if the device is turned ON, $R_{DEVICE} = R_{DS\text{-}ON\ (cascode)}$ and the current will flow through the channel of the LV Si MOSFET and the SiC JFET. If the unstressed SiC JFET cascode is OFF, the cascode will block voltage (R_{DEVICE} in the range of MΩ) and there is no current flowing through the device. The measured V_{DS} will be equal to V_{DC} according to the voltage divider equation in (2). Using a power supply voltage V_{DC}= 30 V, a resistive load R_{LOAD} = 500 Ω and a pulse of 2 seconds, the measurement results of this test for an unstressed device are shown in Fig. 23. Here it can be seen that the voltage across the device in the OFF-state is equal to 30 V i.e. the device is an open circuit.

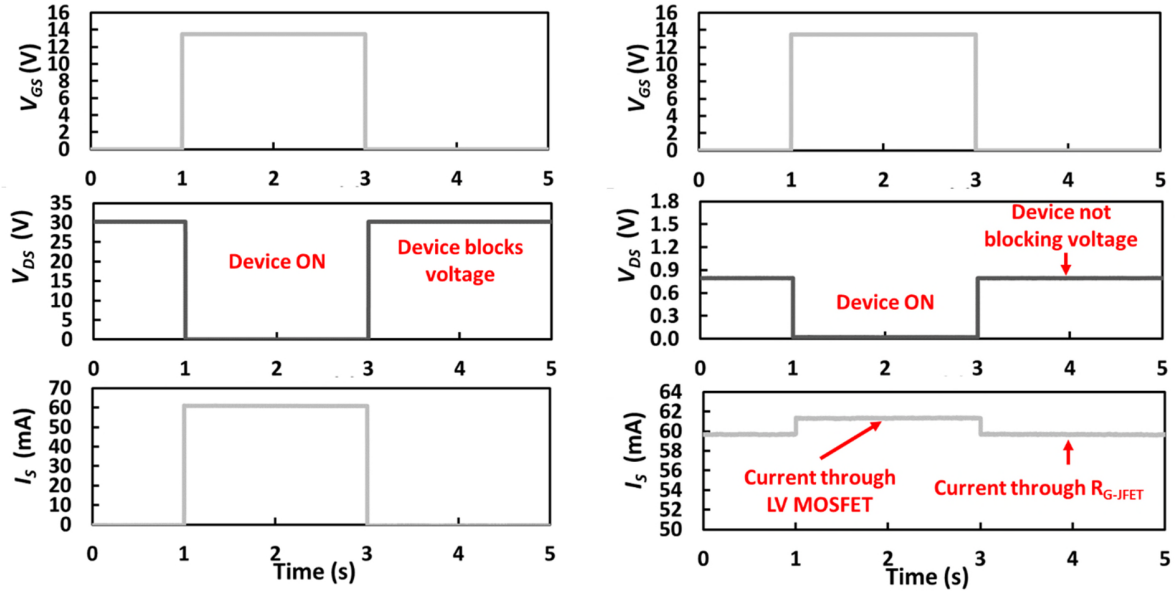
In the case of a damaged Cascode device where the SiC JFET is shorted, if the gate is OFF, R_{DEVICE}= $R_{G\text{-}JFET}$ hence there will be current flowing through the $R_{G\text{-}FET}$, as defined by equation (1). This can be seen in Fig. 23(b) where approximately 60 mA flows through the device in the OFF-state. If the gate is ON, the current will flow through the parallel combination of $R_{DS\text{-}ON\ (Si\ MOSFET)}$ and $R_{G\text{-}JFET}$, however, since R_{DSON} is much smaller than $R_{G\text{-}JFET}$, then according to the current divider rule, it will mainly flow through the LV-MOSFET. It can be seen from Fig. 23(b), that the measured V_{DS} across the SiC Cascode JFET in the OFF-state is approximately 0.8 V, therefore indicating that the device is unable to block voltage.

From these measurements it can be verified that the LV Si MOSFET is still fully functional and has not been damaged by the UIS, however the presence of $R_{G\text{-}JFET}$ in parallel with the LV Si MOSFET impedes the blocking voltage capability of the device. The SiC JFET has lost its blocking voltage capability and the current flows through the gate of the JFET to the source terminal of the cascode, bypassing the low voltage Si MOSFET. The interaction between the low voltage Si MOSFET and the SiC cascode due to the presence of $R_{G\text{-}JFET}$ is key for this failure mechanism.



a *b*

Fig. 22. Test circuits for isolating LV silicon MOSFET from High-Voltage SiC JFET



a *b*

Fig. 23. V_{GS}, V_{DS} and I_S for (a) unstressed and (b) damaged SiC Cascode JFET

6. Conclusions

SiC Cascode JFETs have been tested under single and repetitive avalanche pulses along side SiC Trench MOSFETs. The test results show that under high temperature conditions or after several thousand cycles of repetitive avalanche, SiC Cascode JFETs exhibit a different failure mode from MOSFETs. It has been shown that damage to the resistance between the silicon MOSFET source and the SiC JFET gate during avalanche causes delayed voltage turn-OFF of the device as well as linear mode conduction of the JFET during avalanche. Finite element simulations of the SiC Cascode JFET shows that this partial turn-ON of the SiC JFET causes the device to operate in linear mode while the LV silicon MOSFET is in avalanche. The increased JFET gate current during avalanche is accelerated by temperature due to its positive temperature coefficient. Subsequent failure analysis shows that the LV silicon MOSFET is still functional with a working gate oxide while the SiC JFET is short circuited. The SiC Trench MOSFET however, is completely shorted between the gate and source since the gate oxide is unable to block any voltage. These results show the importance of ensuring the high power capability of the internal cascode JFET gate resistance since damage to the resistor can cause reduced avalanche performance.

Acknowledgement

The authors would like to acknowledge the EPSRC for funding this research through grant reference EP/R004366/1

References

[1] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and Reliability Review of 650V and 900V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," *IEEE Transactions on Industrial Electronics,* pp. 1-1, 2019.

[2] A. Fayyaz, L. Yang, M. Riccio, A. Castellazzi, and A. Irace, "Single pulse avalanche robustness and repetitive stress ageing of SiC power MOSFETs," *Microelectronics Reliability,* vol. 54, no. 9, pp. 2185-2190, 2014/09/01/ 2014.

[3] C. DiMarino and B. Hull, "Characterization and prediction of the avalanche performance of 1.2 kV SiC MOSFETs," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 263-267.

[4] P. Alexakis, O. Alatise, J. Hu, S. Jahdi, L. Ran, and P. A. Mawby, "Improved Electrothermal Ruggedness in SiC MOSFETs Compared With Silicon IGBTs," *IEEE Transactions on Electron Devices,* vol. 61, no. 7, pp. 2278-2286, 2014.

[5] N. Ren, H. Hu, K. L. Wang, Z. Zuo, R. Li, and K. Sheng, "Investigation on single pulse avalanche failure of 900V SiC MOSFETs," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 431-434.

[6] V. Pala, B. Hull, J. Richmond, P. Butler, S. Allen, and J. Palmour, "Methodology to qualify silicon carbide MOSFETs for single shot avalanche events," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 56-59.

[7] A. Fayyaz *et al.*, "UIS failure mechanism of SiC power MOSFETs," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 118-122.

[8] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, "SiC power MOSFETs performance, robustness and technology maturity," *Microelectronics Reliability,* vol. 58, pp. 164-176, 2016/03/01/ 2016.

[9] M. D. Kelley, B. N. Pushpakaran, and S. B. Bayne, "Single-Pulse Avalanche Mode Robustness of Commercial 1200 V/80 mΩ SiC MOSFETs," *IEEE Transactions on Power Electronics,* vol. 32, no. 8, pp. 6405-6415, 2017.
[10] I. Dchar, M. Zolkos, C. Buttay, and H. Morel, "Robustness of SiC MOSFET under avalanche conditions," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2263-2268.
[11] J. Wei, S. Liu, S. Li, J. Fang, T. Li, and W. Sun, "Comprehensive Investigations on Degradations of Dynamic Characteristics for SiC Power MOSFETs Under Repetitive Avalanche Shocks," *IEEE Transactions on Power Electronics,* vol. 34, no. 3, pp. 2748-2757, 2019.
[12] T. Nguyen, A. Ahmed, T. V. Thang, and J. Park, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Transactions on Power Electronics,* vol. 30, no. 5, pp. 2445-2455, 2015.
[13] J. O. Gonzalez and O. Alatise, "Impact of the Gate Oxide Reliability of SiC MOSFETs on the Junction Temperature Estimation Using Temperature Sensitive Electrical Parameters," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 837-844.
[14] H. Yano, N. Kanafuji, A. Osawa, T. Hatayama, and T. Fuyuki, "Threshold Voltage Instability in 4H-SiC MOSFETs With Phosphorus-Doped and Nitrided Gate Oxides," *IEEE Transactions on Electron Devices,* vol. 62, no. 2, pp. 324-332, 2015.
[15] J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018/09/01/ 2018.
[16] J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC mosfets," *IEEE Transactions on Power Electronics,* vol. 34, no. 6, pp. 5737-5747, 2019.
[17] Z. Chbili *et al.*, "Modeling Early Breakdown Failures of Gate Oxide in SiC Power MOSFETs," *IEEE Transactions on Electron Devices,* vol. 63, no. 9, pp. 3605-3613, 2016.
[18] R. Xie, Y. Shi, and H. Li, "Study of 1200 V SiC JFET cascode device," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 316-320.
[19] A. Bhalla *et al.*, "Ultra-high speed 7mohm, 650V SiC half-bridge module with robust short circuit capability for EV inverters," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, pp. 191-194.
[20] J. Hu, O. Alatise, J. A. O. González, R. Bonyadi, L. Ran, and P. A. Mawby, "The Effect of Electrothermal Nonuniformities on Parallel Connected SiC Power Devices Under Unclamped and Clamped Inductive Switching," *IEEE Transactions on Power Electronics,* vol. 31, no. 6, pp. 4526-4535, 2016.
[21] J. Hu, O. Alatise, J. A. Ortiz-Gonzalez, P. Alexakis, L. Ran, and P. Mawby, "Finite element modelling and experimental characterisation of paralleled SiC MOSFET failure under avalanche mode conduction," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-9.
[22] J. Hu *et al.*, "Robustness and Balancing of Parallel-Connected Power Devices: SiC Versus CoolMOS," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 4, pp. 2092-2102, 2016.
[23] A. Fayyaz, B. Asllani, A. Castellazzi, M. Riccio, and A. Irace, "Avalanche ruggedness of parallel SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 666-670, 2018/09/01/ 2018.
[24] J. Wei *et al.*, "Investigations on the Degradations of Double-Trench SiC Power MOSFETs Under Repetitive Avalanche Stress," *IEEE Transactions on Electron Devices,* vol. 66, no. 1, pp. 546-552, 2019.
[25] X. Zhou *et al.*, "A Deep Insight Into the Degradation of 1.2-kV 4H-SiC mosfets Under Repetitive Unclamped Inductive Switching Stresses," *IEEE Transactions on Power Electronics,* vol. 33, no. 6, pp. 5251-5261, 2018.
[26] S. Liu, C. Gu, J. Wei, Q. Qian, W. Sun, and A. Q. Huang, "Repetitive Unclamped-Inductive-Switching-Induced Electrical Parameters Degradations and Simulation Optimizations for 4H-SiC MOSFETs," *IEEE Transactions on Electron Devices,* vol. 63, no. 11, pp. 4331-4338, 2016.
[27] D. Marroqui, A. Garrigos, J. M. Blanes, R. Gutierrez, E. Maset, and F. Iannuzzo, "SiC MOSFET vs SiC/Si Cascode short circuit robustness benchmark," *Microelectronics Reliability,* vol. 100-101, p. 113429, 2019/09/01/ 2019.
[28] SILVACO, "ATLAS users manual. Silvaco Simulation Software," ed, 2016.
[29] J. B. Anup Bhalla, and Xueqing Li, "Robustness of SiC JFETs and Cascodes," *Bodo´s Power Systems,* pp. 48-50, 2015.
[30] D. Aggeler, F. Canales, J. Biela, and J. W. Kolar, "Dv/Dt -Control Methods for the SiC JFET/Si MOSFET Cascode," *IEEE Transactions on Power Electronics,* vol. 28, no. 8, pp. 4074-4082, 2013.