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Gate stresses and threshold voltage instability in normally-OFF GaN HEMTs

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Keywords

«Gallium Nitride (GaN)», «Reliability», «Wide bandgap devices»

Abstract

This paper presents a study of gate stress and threshold voltage instability in commercially available 600/650V GaN high electron mobility transistors (HEMTs). The technologies evaluated are an ohmic gate GaN HEMT and a Schottky gate GaN HEMT. The gate leakage currents have been evaluated for two different gate contact technologies and its temperature dependency is presented. It is shown that the gate leakage current could be a temperature indicator for both technologies evaluated, with a higher temperature sensitivity in the case of the Schottky gate HEMT (showing a sixtyfold increase from 22°C to 150 °C). A novel characterization method based on the third quadrant operation of the device was applied to the two selected GaN HEMTs and the role of temperature, stress level and duration on the threshold voltage instability of GaN HEMTs has been evaluated. The method can capture both the peak shift and transient recovery. The results highlight the clear differences between both gate contact technologies with the Schottky gate HEMT exhibiting higher threshold voltage instability due to gate stress compared to the ohmic gate devices. The Schottky gate HEMT shows a positive threshold voltage shift for a gate stress voltage of 3 V, whereas at 5.5 V the shift is dependent of the stress time. For both HEMTs, the recovery transient after stress removal is accelerated with temperature.

Introduction

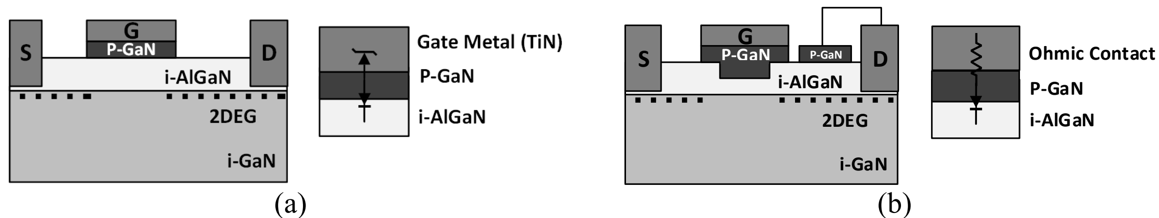
Wide bandgap (WBG) power devices, namely silicon carbide (SiC) and Gallium Nitride (GaN), are currently experiencing a phase of wide industrial adoption. The superior properties of WBG semiconductor materials enable low specific ON-state resistance, fast switching transients and operation at high temperatures, resulting in power devices superior to silicon-based power devices [1, 2]. WBG power devices will be fundamental for enabling more efficient power electronics systems and with a myriad WBG power devices available from different manufacturers, the time for WBG-based power electronics has come. GaN high electron mobility transistors (HEMTs) appear to be more suitable for high-frequency high-efficiency converters, at low DC link voltages, targeting the application areas in the 100-600 V range [3], whereas SiC MOSFETs are contenders for application areas targeting voltages between 600 V and 3.3 kV [3].

In order to replace Si devices, WBG power devices have to demonstrate not only a superior energy conversion performance compared to traditional Si power devices but will also have to at least match the reliability performance of Si devices. This is challenging given the decades of field operation in

silicon devices. The properties of the WBG semiconductor materials add new challenges to the well-stablished qualification techniques for Si power devices [4]. Hence, it is key to develop suitable methods for evaluating the reliability of WBG power devices. Focusing on GaN, these include dynamic ON-state resistance and threshold voltage (V_{TH}) instability [5, 6]. Developing such techniques may be challenging, as the gate interface of the commercially available GaN HEMTs is more complex than the conventional insulated gate of IGBT/MOSFETs.

GaN HEMT power device structure and test prototypes

Commercially available GaN power devices are lateral devices [1]. The main feature of these power devices is the AlGaN/GaN heterojunction and band-offsets which contain a 2D electron gas (2DEG) that results in high carrier density and enhanced mobility due to reduced columbic and acoustic phonon scattering. Due to spontaneous polarization at the band discontinues of the AlGaN/GaN heterojunction, GaN HEMTs are normally-ON however they can be made normally-OFF by using a cascode configuration with a low voltage Si MOSFET as the input [7]. Using gate electrode engineering, normally-OFF GaN HEMTs can be achieved by using the depletion widths of OFF-state diodes to close the 2DEG [2]. Two main gate structures [6] have been adopted by the manufacturers: (a) a p-GaN gate on AlGaN using a Schottky Contact [8] and (b) a p-GaN gate on AlGaN using an Ohmic Contact, which is also known as Gate Injection Transistor (GIT) [9]. The two device and gate structures are shown in Fig. 1.



(a) (b)

Fig. 1: GaN HEMT device and gate structures, adapted from [3, 8, 9]
(a) Schottky Gate GaN HEMT (b) Ohmic Gate GaN HEMT

The different gate structures of the normally-OFF GaN HEMTs will have a clear impact on the reliability and driving circuitry used. In the investigation presented in this paper, studies have been performed on a 600V/31A Ohmic Gate (OG) GaN HEMT from Infineon with datasheet reference IGOT60R070D1 and a 650V/30A GaN HEMT from GaN Systems, with datasheet reference GS66508T. The gate of this HEMT is identified as p-GaN in [10]. No further description has been made available by the manufacturer, as mentioned in [2, 11], but in [12] it is identified as Schottky Gate (SG) GaN HEMT.

These discrete devices are not packaged using the conventional TO-220/TO-247 package used for Si and SiC power devices hence a PCB prototype was required in order to have good access to the terminals for performing the required tests. The prototypes are shown in Fig. 2 (a) and Fig. 2(b) for the OG and SG GaN HEMT respectively. The terminals of the power device are accessible by 4 mm banana connectors, as shown in Fig. 2(c). The selected devices have a thermal pad on the top side, allowing the use of an external DC heater to set the operating temperature of the device, which is shown in Fig. 2(d).

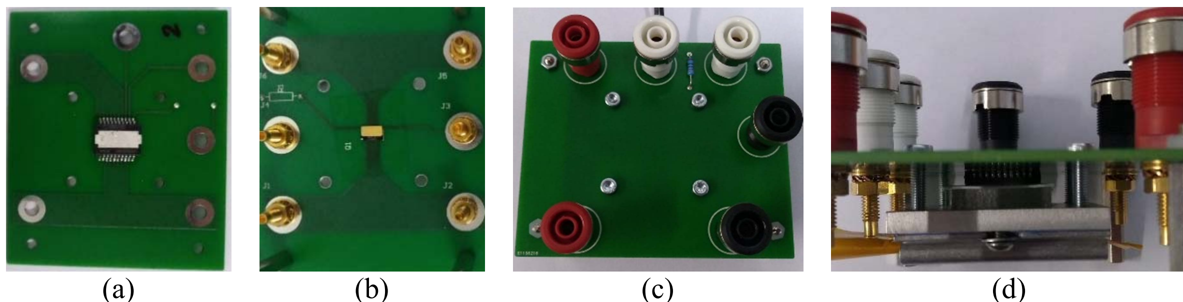
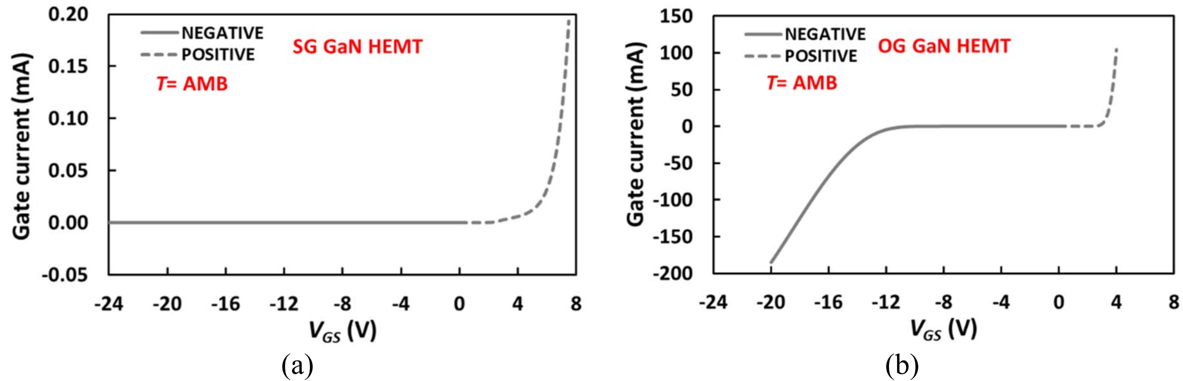

(a) (b) (c) (d)

Fig. 2: Test prototype designs (a) OG GaN HEMT(b) SG GaN HEMT,
(c) Top view of the PCB prototype (d) Detail of the DC heater connection

GaN HEMT gate characteristics and impact of temperature

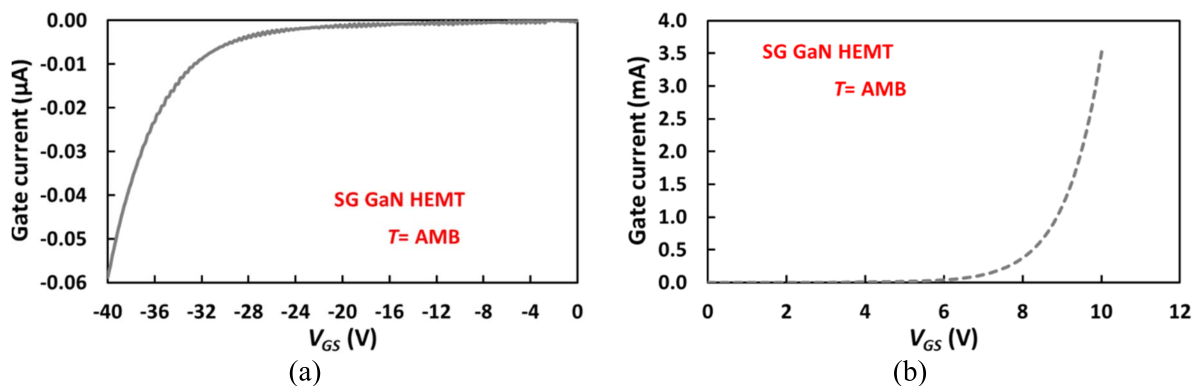
First, it is important to identify and compare the limitations for driving the two selected devices, including the maximum gate voltages and the impact of temperature on the gate leakage currents. Using a source measurement unit (SMU) Keithley model 2602B, positive and negative gate bias sweeps were performed for both HEMTs. The results, measured at ambient temperature (22 °C), are show in Fig. 3(a) for the SG HEMT and Fig. 3(b) for the OG HEMT. Comparing both figures, it is clearly observed how the gate leakage currents are higher for the OG HEMT.



(a) (b)

Fig. 3: Gate voltage sweep and gate leakage current at ambient temperature (22 °C)
(a) SG GaN HEMT, (b) OG GaN HEMT

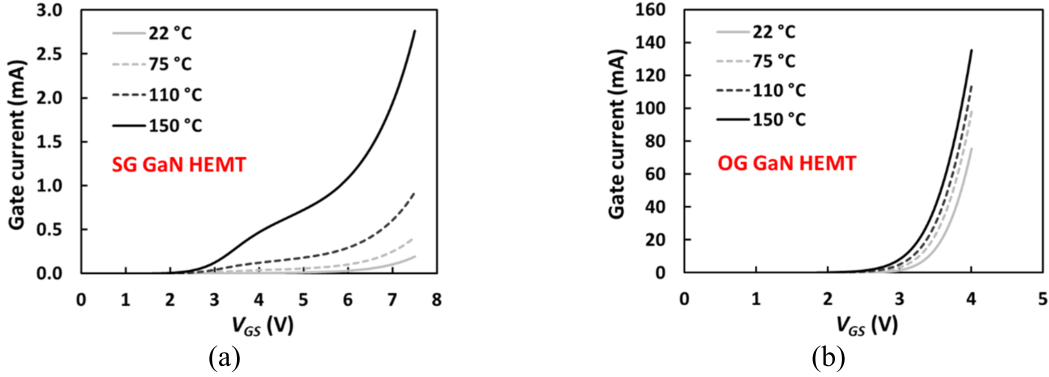
Analyzing the negative gate bias, it can be concluded that it would be possible to use a negative voltage of -20 V with the SG HEMT, whereas for the OG HEMT the gate current will be approximately -200 mA in that situation. A knee voltage of around -12 V is observed in the OG HEMT, caused by an internal protection diode structure [3, 13]. In the case of the SG HEMT, the negative gate voltage can be increased up to -40 V with minimum gate leakage current, as the results in Fig. 4(a) show. For this device, increasing the positive gate voltage sweep to 10 V caused the gate leakage current to increase considerably, as shown in Fig. 4(b).



(a) (b)

Fig. 4: SG gate HEMT (a) Negative gate sweep up to -40V (b) Positive gate sweep up to +10 V

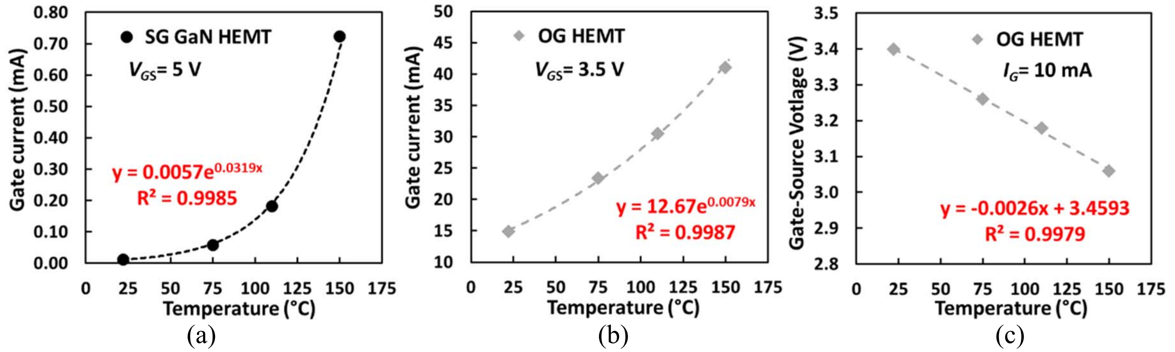
For understanding the differences between the devices and their limitations, it is important to evaluate the impact of temperature on the gate leakage current. This has been done for both gate technologies and the results are shown in Fig. 5. The results in Fig. 5(a) show that temperature plays a fundamental role in the gate leakage currents in the SG gate HEMT. For this device, considering a gate voltage of 6 V, which is the maximum gate voltage according to the datasheet, the gate leakage current increases from 32 µA at ambient temperature to 1.09 mA at 150 °C. Analyzing the results of the OG GaN HEMT in Fig. 5(b), the temperature dependency of the gate leakage shows the expected performance of the ohmic contact gate structure (a resistor and a forward biased diode as indicated in Fig. 1(b)) with a leftwards shift of the gate leakage current with temperature.



(a) (b)

Fig. 5: Impact of temperature on positive gate voltage sweeps. (a) SG HEMT, (b) OG HEMT

This increase of the gate leakage current with temperature will have to be considered when designing gate driver circuits for GaN HEMTs, however it could also be used as temperature indicator. The calibrated relationship between the gate leakage current and temperature is shown in Fig. 6(a) and Fig. 6(b) for the SG and OG HEMT respectively. These results indicate that the gate leakage currents could be a Temperature Sensitive Electrical Parameter (TSEP) for GaN devices [14], which can be added to the TSEPs already presented in [15, 16]. In the case of the SG HEMT, for a gate voltage of 5 V, the gate leakage current increases almost 60 times, whereas in the case of the OG HEMT the increase is 2.7 times when a gate voltage of 3.5 V is used. Moreover, as already presented in [17] and shown in Fig. 6(c), the gate voltage measured at a fixed gate current I_G is a good TSEP in OG GaN HEMTs.



(a) (b) (c)

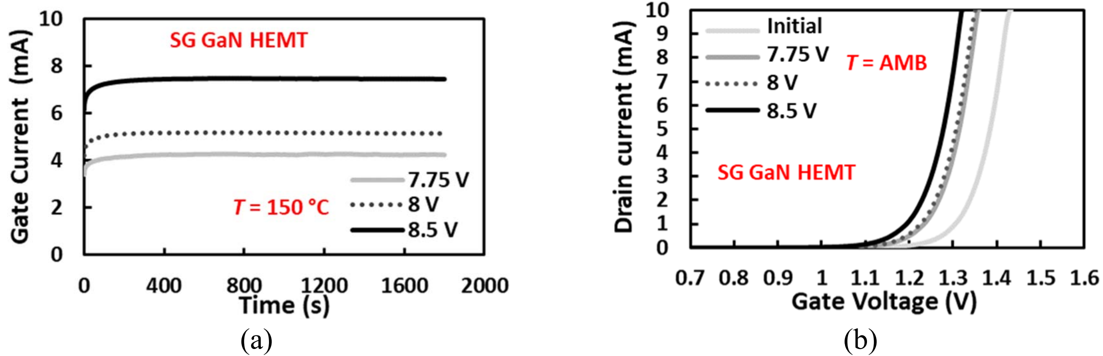
Fig. 6: Impact of temperature on gate current at fixed gate voltage
(a) SG GaN HEMT, (b) OG GaN HEMT. (c) Temperature sensitivity of V_{GS} – OG GaN HEMT

Accelerated gate stress tests in GaN HEMTs

Accelerated stress tests are performed to evaluate the reliability and lifetime of power devices, both at gate level [18] and packaging level [19]. In this paper, preliminary accelerated gate stress tests have been performed to evaluate the impact of gate biasing on the gate transfer characteristics of both GaN HEMT technologies. The stresses were performed at different stages increasing the stress level (gate voltage for the SG HEMT and gate current for the OG HEMT). Fig. 7(a) shows the measured gate current for the SG HEMT for the different cumulative gate voltage stress levels. The stress duration was 30 minutes for each stress step, with characterization at ambient temperature after recovery at V_{GS}=0 for at least 90 minutes. Fig. 7(b) shows the gate transfer characteristics, measured at ambient temperature after each stress stage, with V_{GS}=V_{DS}. Fig. 8 shows the results for the OG HEMT stress tests, consisting in different gate current applied to the device for 1000 s. The stresses for the OG HEMT were done at ambient temperature, whereas they were performed at 150 °C for the SG HEMT.

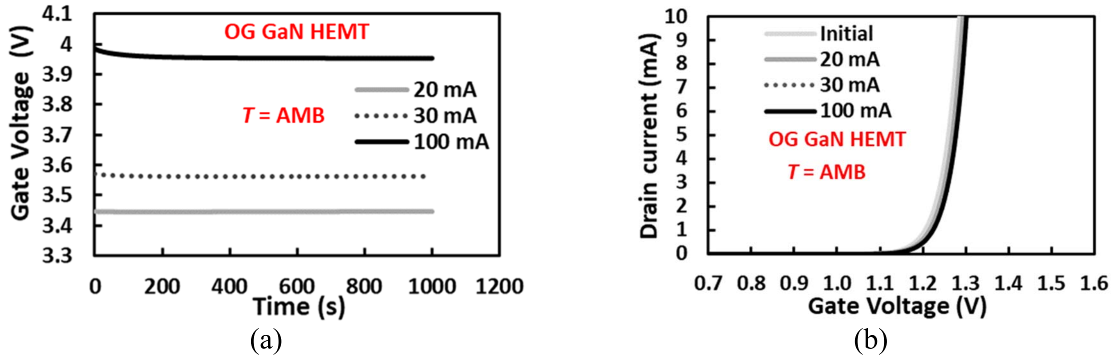
The results in Fig. 7 and Fig. 8 show that for the selected stresses there is a negative shift of V_{TH} for the SG HEMT, which is in agreement with [12], whereas in the case of the OG HEMT there is no significant shift. The negative shift in V_{TH} for the SG GaN HEMT is due to positive charge injection from the gate into the heterojunction thereby reducing the voltage necessary to from the 2DEG. Evaluating the stress itself, in the case of the OG HEMT, it can be observed that the stress voltage is dependent on the gate

current, making the stress in terms of voltage complex: Increasing the stress voltage means a higher leakage current, causing a high power dissipation on the device. In the case of the SG HEMT, Fig. 7(a) shows an initial exponential rise of the gate leakage current during the stress, which reaches a steady value after 300 s. This increase can be attributed to charges being trapped in the gate stack, shown in Fig. 1. This increase of gate current at high gate stress was also reported in [12]. In the case of the OG GaN HEMT there is a modest reduction of gate voltage, which can be attributed to self-heating of the device due to the higher power dissipated.



(a) (b)

Fig. 7: Accelerated gate stresses. SG GaN HEMT. (a) Gate leakage current during stress, (b) Transfer (V_{GS}=V_{DS})



(a) (b)

Fig. 8: Accelerated gate stresses. OG GaN HEMT. (a) Gate voltage during stress (b) Transfer (V_{GS}=V_{DS})

Accelerated stress tests are useful for understanding the limitations of the power devices, however these tests are time consuming hence it is paramount to define the right stress levels and durations that do not activate undesired failure mechanisms [4]. Moreover, there is a clear limitation for capturing transient and recovery phenomena. This has been proven particularly relevant for assessing threshold voltage instability in SiC power MOSFETs [20] and dynamic ON-state resistance [21, 22] in GaN HEMTs. The use of conventional methods for V_{TH} characterization in GaN is also under study [23], due to the complexity of the device structure and impact of bias history. The next section evaluates a method that can capture the dynamic threshold voltage shift caused by gate stresses in GaN HEMTs.

Third quadrant characteristics and threshold voltage instability in GaN

One of the peculiarities of GaN HEMTs is that they do not have a body diode. The reverse conduction in the third quadrant is enabled by a mechanism called self-commutated reverse conduction (SCRC) [2]. In the first quadrant, the device turns ON when a gate-source voltage exceeding $V_{GS\text{-}TH}$ is applied to the device, whereas in the third quadrant it turns ON when a gate-drain voltage higher than reverse threshold voltage ($V_{GD\text{-}TH}$) is applied. If the device is conducting in the reverse direction, $V_{GD}=V_{GS}-V_{DS}$. If higher than the threshold, the device turns ON (SCRC) and the third quadrant voltage V_{SD} is given by (1) [2].

$$V_{SD}=V_{GD\text{-}TH}-V_{GS}+I\cdot R_{SD} \quad (1)$$

Focusing on threshold voltage characterization, the value of V_{GD-TH} and V_{GS-TH} can be assumed equal [2] and at low currents the voltage drop in the resistance R_{SD} can be considered negligible. Analyzing (1), it can be concluded that during reverse conduction of a small sensing current at V_{GS}=0, V_{SD} is an indicator of V_{TH} ($V_{SD} \approx V_{TH}$). Measurements have been done for both SG and OG GaN HEMTs and the results are summarized in Table I. The threshold voltage was measured with $V_{GS}=V_{DS}$ and forcing a current of 10 mA.

Table 1: Measured V_{SD} and V_{TH} at ambient temperature

	V_{TH} (V) $V_{GS}=V_{DS}$ @ I= 10 mA	V_{SD} (V), V_{GS}=0, @ I = 10 mA
OG GaN HEMT	1.478	1.483
SG GaN HEMT	1.597	1.576

The direct relationship between V_{SD} and V_{TH} indicates that the method presented in [24, 25] could be used for monitoring V_{TH} shift in GaN HEMTs. This method is similar to the use of the body diode voltage as a TSEP in MOSFETs [14]. The test circuit for its implementation as a V_{TH} monitoring technique in GaN HEMTs is shown in Fig. 9. The circuit consists of a gate driver which is used for stressing the gate of the device under test (DUT) while a low I_{SD} current circulates through the device in reverse direction. In the case of SG HEMT the stresses are defined in voltage by adjusting the driver supply voltage V_{GG}, whereas in the case of the OG HEMTs the stresses are defined as current by using a fixed V_{GG} and adjusting the value of R_G. The circuits are shown in Fig. 9(a) and Fig. 9(b) and the operation of the method is presented in Fig. 9(c), for the SG GaN HEMT.

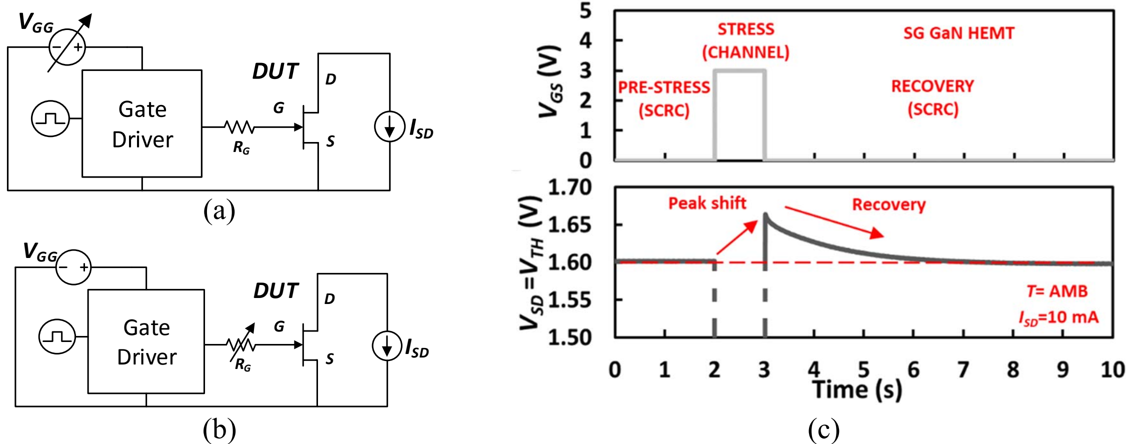


Fig. 9: Circuit for evaluation of V_{TH} instability on GaN HEMTs (a) Gate voltage stress for SG HEMT (b) Gate current stress for OG HEMT (c) Circuit operation for the SG HEMT

Depending on the gate voltage, the current circulates by means of SCRC or channel conduction. In the pre-stress stage, V_{GS}=0 and the current flows by means of SCRC and as mentioned previously, the measured V_{SD} can be considered equivalent to V_{TH}. During the stress phase, the device is turned ON at a determined gate stress voltage (adjustable in the circuit) and the current circulates through the channel of the DUT. After stress removal, V_{GS}=0 and the device operates again in the SCRC mode. The measured V_{SD} shows the peak shift of V_{TH} and recovery after stress removal. The circuit allows to study the impact of the stress duration, stress level and temperature on V_{TH} shift and recovery.

Gate stress and characterization of the Schottky gate GaN HEMT

In the case of the SG GaN HEMT, 3 stress levels have been evaluated, namely V_{GS} = 3, 5.5 and 7.5 V at both ambient and high temperature (150 °C). These stress levels were applied to the device for three different stress duration times (1, 10 and 100 s) while a current I_{SD}= 10 mA was circulating through the device. The control pulse applied to the gate driver was generated using a waveform generator model AFG3022C from Tektronix and the resulting V_{SD} voltage was captured using an oscilloscope model TDS5054B from Tektronix. The results for the stresses for the SG GaN HEMT at ambient temperature

are shown in Fig. 10. The values have been normalized with respect to the measured pre-stress V_{SD}. The time t=0 was defined at the peak shift and the logarithmic time scale allows to capture the different time constants of the recovery transient. There was a recovery time of 40 minutes between each stress-characterization sequence, to allow the full recovery of V_{SD} to the pre-stress value.

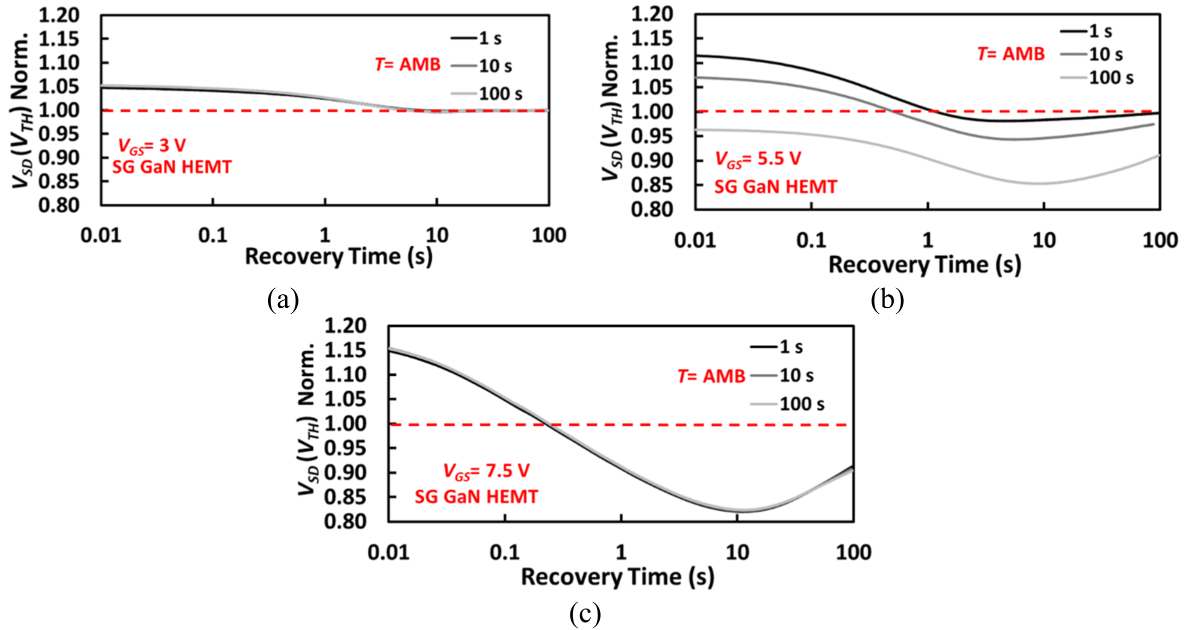


Fig. 10 Stress results for SG GaN HEMT at ambient temperature and different stress durations. (a) Stress voltage = 3 V, (b) Stress voltage = 5.5 V (c) Stress voltage = 7.5 V

From the results in Fig 10, at ambient temperature the stress voltage has a clear impact on the measured threshold voltage shift. In the case of the 3 V stress, as shown in Fig. 10(a) and in agreement with [26], the evaluated SG HEMT shows a positive V_{TH} shift caused by trapping of electrons in the AlGaN/GaN interface [26]. For the 7.5 V stress, as presented in Fig. 10(c), an initial positive V_{TH} shift is observed (+17%), followed by a fast drop (-18%) and a long recovery transient to the pre-stress value, in the range of minutes. For these two stress levels (3 V and 7.5 V) and the evaluated stress duration range (1 s to 100 s), the stress time has no significant impact on the measured peak shift and recovery characteristics.

The situation changes for a stress voltage of 5.5 V, as the results in Fig. 10 (b) show. In this case the stress duration time plays a fundamental role on the peak shift and recovery of the SG GaN HEMT. For a stress duration of 1 s, a positive peak shift is captured (+11.8%), with a fast recovery to the pre-stress value. As the stress duration is increased, the peak shift reduces its value, with a positive peak shift of +7.3 % for the 10 s stress duration and a larger negative dip after the initial recovery phase (-5.7%). This is clearer for the 100 s stress measurement, as peak shift is now negative (-3.6%) and the negative dip after the initial fast transient has also increased (-14.7%). In [26], using a novel methodology and measuring windows of 10 µs, similar characteristics were observed for medium gate voltage stress levels. The different shifts were attributed to three different mechanisms [26]: electron trapping at the AlGaN/GaN interface, hole trapping in the AlGaN barrier and hole depletion. The traps have different time constants and this method allows to capture the transients during the recovery phase.

It is also important to evaluate the impact of temperature on the gate stress and recovery. The characterization measurements were performed at 150 °C and the results for the SG GaN HEMT are shown in Fig. 11, for stress voltages of 3, 5.5 and 7.5 V. Analyzing the results at 150 °C, the first and most obvious conclusion is that the recovery transients are accelerated for all the stress voltages evaluated. The initial drop after the peak shift is now in the range of several milliseconds, whereas the long recovery transient is in the range of seconds. Evaluating the stresses at 5.5 and 7.5 V, as shown in Fig. 11(b) and Fig .11(c), increasing the stress duration causes an increase of the dip after stress removal and there is no significant impact on the initial positive peak shift. This peak shift is higher for the 7.5 V stress (+18% for 1 s stress) than the 5.5 V stress (+13% for 1 second stress).

More relevant are the results for the 3 V stress at 150 °C, shown in Fig. 11(a). They show a trend similar to the 5.5 V stresses at ambient temperature, with a reduction of the positive peak shift as the stress duration is increased (+10.5% for 1 s stress and +8.8% for 100 s stress), as well as the presence of a negative dip (-2.5% for 100 s stress). Another interesting observation is that for a stress of 5.5 V and a duration of 100 s, at ambient temperature the peak shift is negative (-3.6%), whereas at 150 °C it is positive (+12.8%). Similar results were reported in [26], highlighting the complexity of gate stress and V_{TH} shift in GaN HEMTs. This is especially important for long duration stresses, relevant for power cycling.

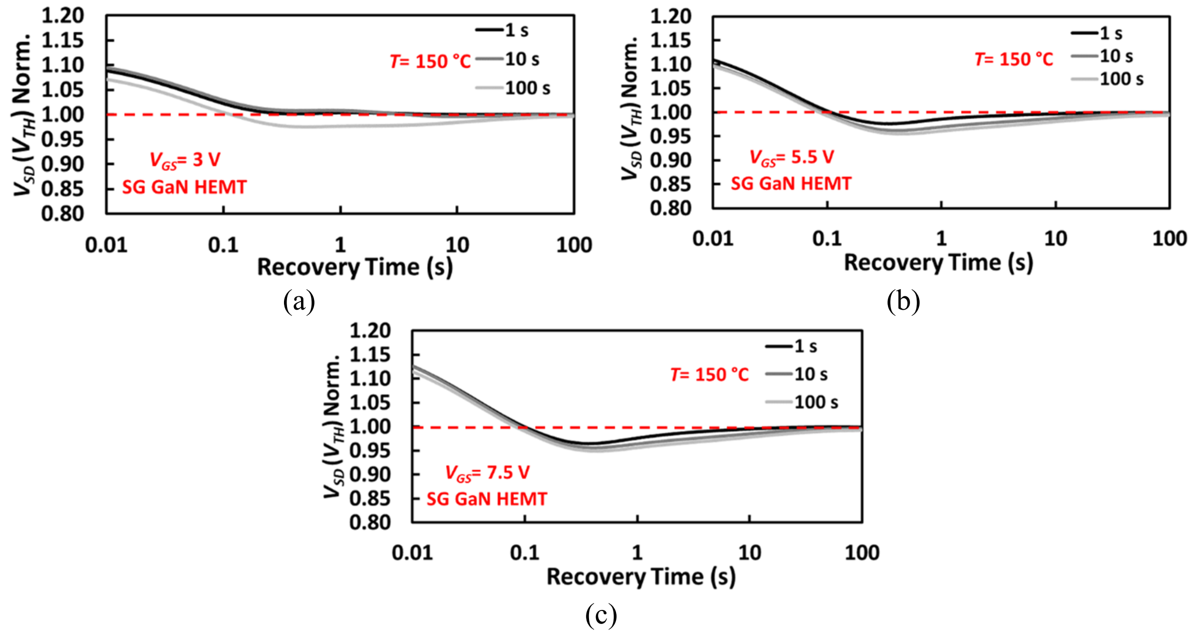


Fig. 11 Stress results for SG GaN HEMT at 150 °C and different stress durations.
(a) Stress voltage = 3 V, (b) Stress voltage = 5.5 V, (c) Stress voltage = 7.5 V

Gate stress and characterization of the ohmic gate GaN HEMT

The OG GaN HEMT was also subjected to gate stress tests. As described previously, the stresses are done in current, using the circuit shown in Fig. 9(b) and adjusting the gate resistance. Two gate current (I_G) stress levels were considered, namely I_G=5.2 mA and I_G= 73 mA, which result in gate voltage stresses of 3.2 V and 3.96 V respectively.

Compared with the SG HEMT, the results in Fig. 12 show a lower V_{TH} shift for the OG HEMT (-2.5% for I_G=5.2 mA), even for the higher gate stresses level (-4% for I_G=73 mA). This negative shift is in agreement with the results in [6]. Fig. 12(a) shows how increasing the stress level has a slight impact on the negative V_{TH} shift, which is more apparent for the high stress current, as shown in Fig. 12(b). The recovery time is in the range of seconds for both stress levels.

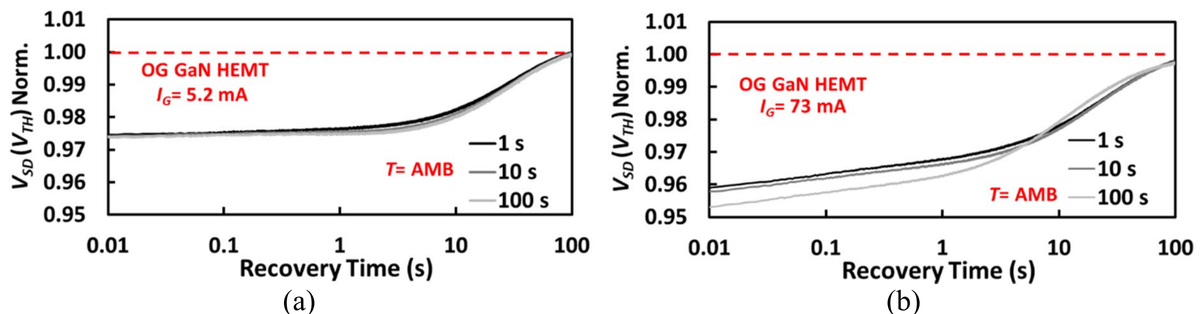


Fig. 12: OG GaN HEMT at ambient temperature and different stress durations
(a) I_G=5.2 mA, (b) I_G=73 mA

It is important to mention that at high gate currents, the high power dissipated in the gate may cause the self-heating of the device during the long gate stress pulses. This self-heating and subsequent cooling after stress removal may affect the characterization measurements at high gate current stresses, especially in the case of 73 mA, which is beyond the maximum continuous gate current of 20 mA.

It is also key to characterize the impact of temperature and this has been done for the high current stress. The results are shown in Fig. 13 and, as it was the case of the SG HEMT, at 150 °C the recovery is accelerated with no apparent V_{TH} shift. This is clearly shown in Fig. 13(b) where the complete stress sequence is shown and no apparent shift respect to the pre-stress V_{TH} is observed. From these results, the OG GaN HEMT has a superior performance regarding gate stress and threshold voltage instability.

The circuit used in these experiments is based in a voltage source gate driver and the current was adjusted by varying the gate resistance R_G in Fig.9(b). At high temperatures, the internal gate voltage drop of the OG GaN HEMT reduces, as shown in Fig. 5(b). This causes a slight change of the gate current during the stress, which at 150 °C is 78.2 mA. Using a current source gate driver may produce better results for stress and characterization of the OG HEMT, as it will enable a more precise gate current adjustment.

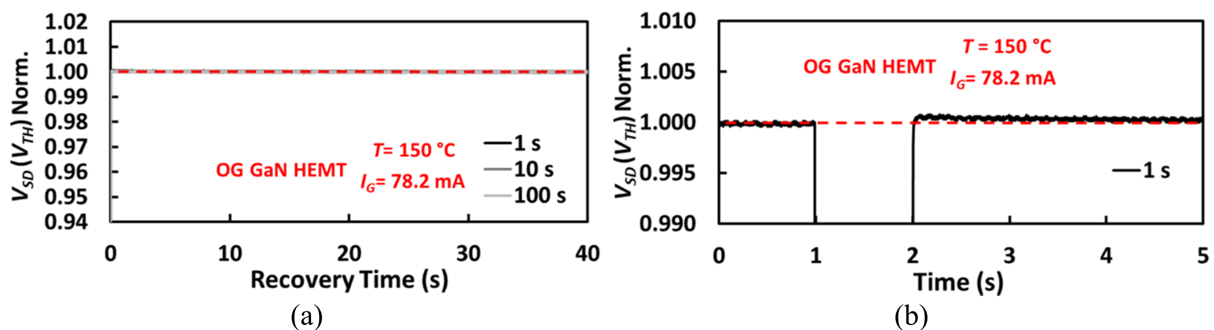


Fig. 13: Stress results for OG GaN HEMT at 150 °C. (a) Recovery for different stress durations (b) Complete sequence for 1 s stress

From the point of view of power cycling and junction temperature determination, the impact of the gate stress on TSEPs for GaN should be evaluated, as it has been done with SiC MOSFETs in [27, 28]. This can be particularly relevant for lifetime estimation of GaN HEMTs.

Conclusion

This paper has evaluated the gate characteristics and threshold voltage instability of Schottky Gate and Ohmic Gate GaN HEMTs. The gate leakage currents have been characterized as a function of temperature and it is shown that in the case of the SG HEMT it can be a clear indicator of temperature. Accelerated gate stress tests have been performed and it is shown that the SG GaN HEMT is more susceptible to threshold voltage instability. A novel characterization technique and the impact of stress level, stress duration and temperature has been evaluated, confirming that the SG GaN HEMT has higher threshold voltage instability compared with the OG HEMT. At intermediate gate stress levels, the SG GaN HEMT shows a non-monotonic V_{TH} shift as function of the stress duration. For both gate technologies, the recovery is accelerated at high temperatures. The results presented in this paper could be fundamental for assessing the impact of gate stress on power cycling of GaN HEMTs.

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