Measurement and Simulation of Short Circuit Current Sharing under Parallel Connection: SiC MOSFETs and SiC Cascode JFETs

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Abstract

Short-Circuit (SC) current sharing in parallel connected SiC MOSFETs and SiC Cascode JFETs have been investigated using experimental measurements and finite element models. Device parametric variation between parallel devices contributes to uneven current sharing and reduced module robustness against SC events. Experimental measurements show that threshold voltage variation is the most critical parameter in SiC MOSFETs, more so than device switching rate and initial junction temperature. The temperature coefficient of the ON-state and saturation resistance of SiC Cascode JFETs is higher than that of the SiC MOSFETs, hence, the short-circuit energy is lower because the SC current is limited more quickly in the SiC Cascode JFETs compared to SiC MOSFETs. Also, the input silicon MOSFET in the Cascode arrangement ensures better performance regarding V_{TH} mismatch between parallel devices under SC. This is because the threshold voltage variation is less in silicon MOSFETs compared to SiC MOSFETs. Finite element models have been used to explore the differences between SiC MOSFETs and SiC Cascode JFETs under SC conditions and to explain why JFETs are better at supressing SC currents than MOSFETs.

1. Introduction

In high power applications where parallel connected power devices are required for large current conduction capability, current sharing under short-circuit (SC) conditions is critical. Variations in device parameters (threshold voltage, switching rate, thermal impedance and junction temperature) can negatively impact current sharing under SC and therefore reduce module robustness under SCs [1-4]. Non-uniformities caused during the SiC device fabrication process can cause variations in V_{TH} in co-fabricated devices. This is less of a problem in silicon MOSFETs because of the better quality gate dielectric interface formed during the thermal oxidation process. Furthermore, differential rates of degradation can cause non-uniformities in device parameters like switching rates (through degrading gate resistance) and junction temperature (through degrading solder joints). For example, the thermal impedance of a power device is known to increase over time due to thermo-mechanical stresses that result from differences in the coefficients of thermal expansion at the chip to packaging interface. SiC Cascode JFETs have silicon MOSFETs as the input device hence they are not affected by Bias Temperature Instability (BTI) in the same way than SiC MOSFETs are [5, 6]. Moreover, the temperature coefficients of the ON-state and saturation resistance in JFETs are different from MOSFETs, hence, SC current limitation will occur differently. This paper uses experimental measurements and Finite element simulations to investigate short circuit current sharing in SiC MOSFETs and SiC Cascode JFETs. Section 2 details the experimental set up while section 3 introduces the finite element models.

2. Experimental Measurements on Short Circuits in Single Devices

Fig. 1(a) shows the circuit diagram for the short circuit test set-up while Fig. 1(b) shows the picture. The IGBT module is a 1200 V/1000 A that is used for connecting and disconnecting the DUTs to the DC power supply and DC link. The DUTs are 1200 V/20A SiC MOSFETs from ST with datasheet reference SCT20N120 while the SiC Cascode JFETs are 1200 V/ 18.4A devices from United SiC with datasheet reference UJ3C120150K3S.

Fig. 2(a) shows the SC currents for the SiC Cascode JFET at different DC link voltage V_{DC} while Fig. 2(b) shows similar measurements for the SiC MOSFET. These SC measurements are done with reduced V_{DS} and over a longer duration. Fig. 2(c) compares the normalized SC currents for both technologies, Fig. 2(d) compares the drain-source voltages during the short circuit while Fig. 2(e) compares the gate-source

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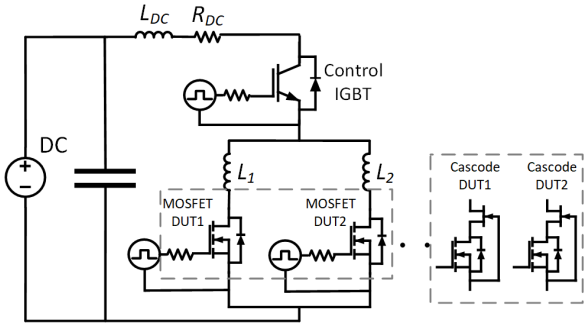
voltages. All the measurements have been performed on single devices.



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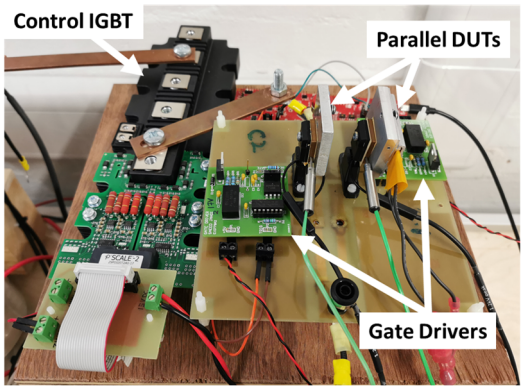
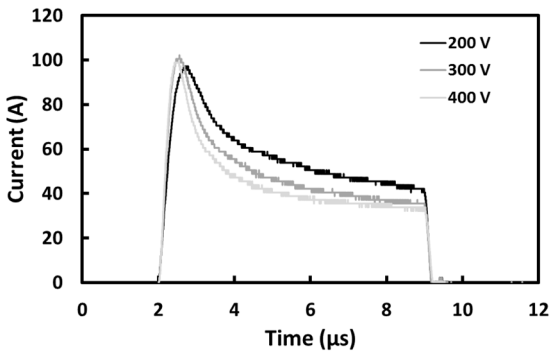


(b)

Fig. 1 (a) Experimental test-rig circuit diagram for short circuit measurements (b) Experimental test-rig Picture

It can be seen from Fig. 2 that the SC current is limited more quickly in the SiC Cascode compared to the SiC MOSFET. Also, the peak SC current is higher in the SiC MOSFET than in the Cascode JFET although both devices have similar ON-state resistances. Short circuit currents are limited by the positive temperature coefficient of the ON-state resistance due to joule-heating.



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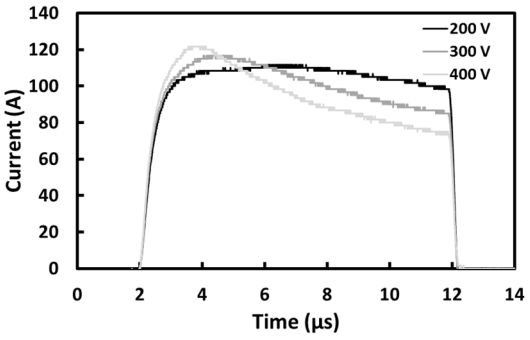

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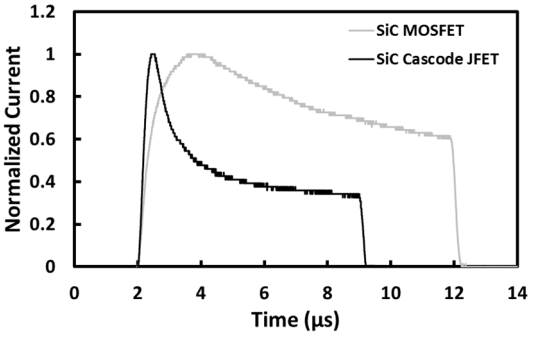

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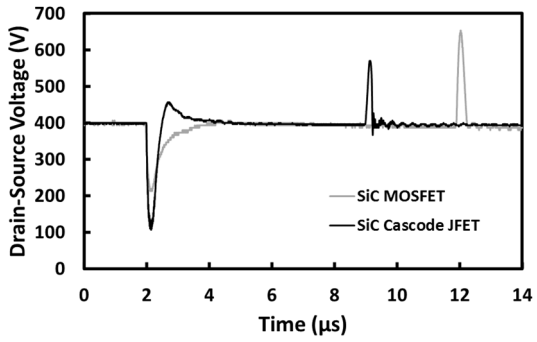

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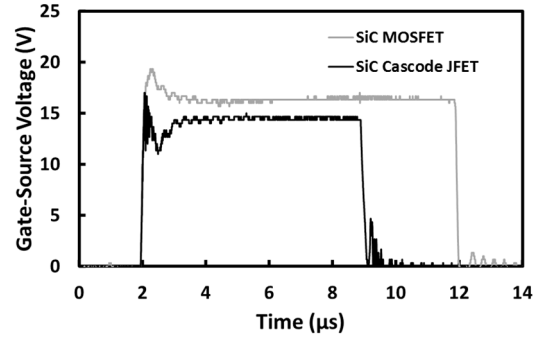


(e)

Fig. 2 Short circuit characteristics at different V_{DC} (a) 1200 V SiC Cascode JFET (b) 1200 V SiC MOSFET; (c) Normalised SC transient for both technologies (d) Short Circuit Drain Voltage waveforms (e) Short Circuit Gate-source voltage

The reason for the different SC characteristics is down to the different temperature coefficients of the

ON-state and saturation resistances of both devices. Comparing the temperature dependencies of the output/transfer characteristics on the datasheets, it is clear that the SiC Cascode JFET is more temperature sensitive than the SiC MOSFET. The drain current equation for MOSFETs and JFETs are given below as equations (1) and (2) respectively, where β is the MOSFET gain factor, V_G is the gate source voltage, V_{TH} is the MOSFET threshold voltage, i_{DSS} is JFET saturation drain current at V_G = 0 V and V_P is the pinch-off voltage of the JFET.

$$i_{DS} = \frac{\beta}{2}(V_G - V_{TH})^2 \quad (1)$$

$$i_{DS} = i_{DSS}\left(1 - \frac{V_G}{V_P}\right)^2 \quad (2)$$

The temperature coefficents of the drain currents in both devices can be written as shown below as (3) for MOSFETs and (4) for JFETs

$$\frac{di_{DS}}{dT} = \frac{(V_G - V_{TH})^2}{2}\frac{d\beta}{dT} - \beta(V_G - V_{TH})\frac{dV_{TH}}{dT} \quad (3)$$

$$\frac{di_{DS}}{dT} = 2i_{DSS}\left(1 - \frac{V_G}{V_P}\right)\left(\frac{V_G}{V_P^2}\right)\frac{dV_P}{dT} + \left(1 - \frac{V_G}{V_P}\right)^2\frac{di_{DSS}}{dT} \quad (4)$$

In SiC MOSFETs, the negative temperature coefficient of V_{TH} (dV_{TH}/dT) causes the SC current to increase with temperature because of increasing carrier generation from temperature-induced bandgap narrowing. In this case, the Fermi level moves closer to the conduction band meaning the carrier concentration is increased with temperature. Also, interface trapped charges can become dislodged at higher temperatures. However, in MOSFETs the negative temperature coefficient of the electron effective mobility (reflected in $d\beta/dT$) causes the SC current to reduce with temperature. The point where the 2 temperature coefficients are equal is referred to as the zero-temperature coefficent (ZTC) point i.e. the drain current is temperature invariant. This is for the condition when equation 3 is equal to zero. Since the ZTC point occurs at a gate voltage V_{GS} that is usually lower than the rated V_{GS}, devices under SC at rated conditions have a SC current that always decreases as the junction temperature rises. In SiC Cascode JFETs, the negative temperature coefficient of the pinch-OFF voltage (dV_P/dT) causes the drain current to increase with temperature while the negative temperature coefficient of I_{DSS} (dI_{DSS}/dT) causes the drain current to decrease with temperature. It is beneficial for power devices to have SC currents with high negative temperature coefficients since the SC current will be strongly limited thereby preventing device failure under SCs.

Since the SiC MOSFET and SiC Cascode JFET have similar transient thermal impedances, it follows that the JFET will have a lower junction temperature since it clearly dissipates less short circuit energy. This is due to the fact that the saturation resistance in the JFET is more temperature sensitive than that of the SiC MOSFET, hence the short circuit current is limited more quickly.

Fig. 3 shows that increasing the gate voltage increases the peak SC. Fig. 3 also shows the tail current evident in SC failures in SiC MOSFETs. In the literature, this tail current has been attributed to the leakage current of the body/drift PN junction [7] and reduced V_{TH} as a result of the high temperatures caused by the SC [8]. SiC MOSFETs are also known to have gate oxide failures during SCs [9, 10]. This is due to the high current densities and temperatures that occur adjacent to the gate oxide during SC events, coupled with the less reliable oxide/semiconductor interface in SiC MOSFETs. Subsequent measurements on the SiC MOSFET showed significantly reduced gate impedance, thereby implying gate damage in agreement with other studies of SiC MOSFET failure during SC [10, 11].

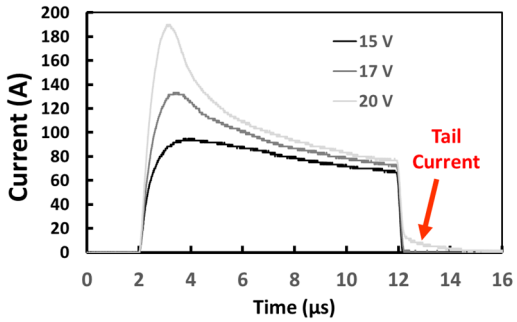


Fig. 3. Measured Short circuit current for 1200 V/20A SiC MOSFETs showing tail current indicating device failure

3. Experimental Measurements on Short Circuits in Parallel Devices

Parallel connected SiC MOSFETs have been tested under SC conditions. The devices have a 25% variation in V_{TH}. The results are shown in Fig. 4 with the device with the lower V_{TH} conducting a higher SC current compared to the device with the higher V_{TH}.

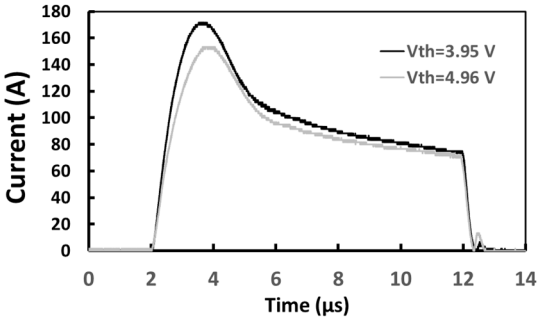


Fig. 4. Measured Short circuit current for parallel 1200 V/20A SiC MOSFETs with 25% difference in V_{TH}

It is important to mention that V_{TH} imbalance is a challenge in SiC MOSFETs because of the higher variability due to varying fixed oxide and interface trapped charge as well as incomplete p-dopant activation following post-implantation anneal [12]. Furthermore, even when V_{TH} variability is reduced when designing power modules by selecting devices with the same V_{TH}, variation in V_{TH} drift [13] over the lifetime of the module can become a problem. V_{TH} drift due to BTI is a challenge in SiC MOSFETs, whereas SiC Cascode JFETs do not have this problem since the input device is a low voltage silicon MOSFET and the V_{TH} in silicon MOSFETs is stable with low variability [14].

In JFETs, the pinch-OFF voltage depends on the PN-junction built in voltage, the drift layer doping and the cell pitch. These parameters are better controlled in a silicon fabrication process flow, opposed to the case of SiC MOSFETs, where fixed oxide and interface charges in SiC MOSFETs play a key role on the V_{TH} of the device [15]. In other words, since the occurrence of fixed oxide charge in SiC MOSFET gate dielectrics is highly probabilistic, there can be a greater spread/mismatch in V_{TH} in SiC MOSFETs compared to pinch-OFF voltages in JFETs.

To investigate the role of temperature imbalance, measurements have been performed on parallel SiC MOSFETs with different case temperature T_C (25°C vs 50 °C) and (25°C vs 150°C). The results are shown in Fig. 5 for the SiC MOSFETs and Fig. 6 for the SiC Cascode JFETs. The results in both cases show that the device with the higher initial case temperatures conducts a lower SC current.

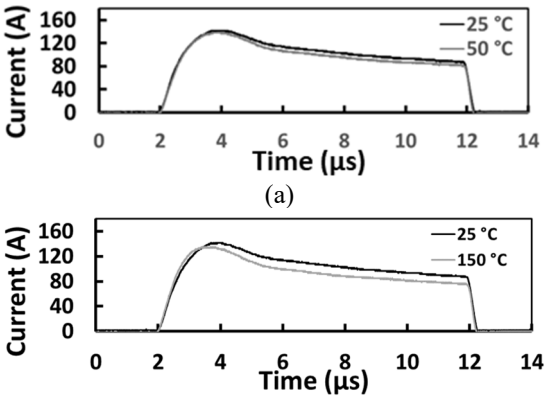


Fig. 5. Measured SC current for parallel 1200 V/20A SiC MOSFETs: (a) 100% and (b) 500% difference in T_C

The difference in the SC currents for a 100% difference in case temperature is marginal whereas the difference in SC current for a 500% difference in case is more apparent. Hence, it can be concluded from Fig. 5 and 6 that variation in the initial junction temperatures between parallel devices is not a significant factor in determining SC current sharing, opposed to the case of unclamped inductive switching where the difference in temperature in parallel devices plays a fundamental role in avalanche ruggedness [16].

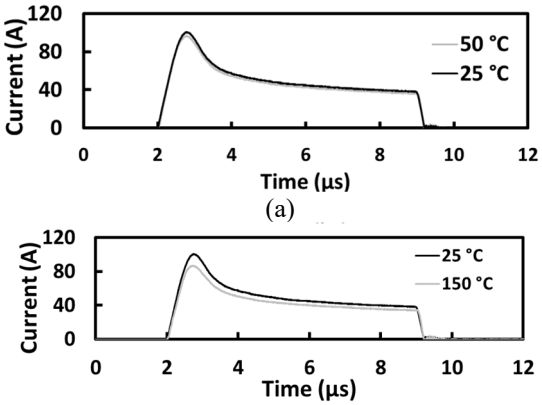


Fig. 6. Measured SC current for parallel 1200 V/20A SiC Cascode JFETs: (a) 100% and (b) 500% difference in T_C

4. Finite Element Simulations of Short Circuits

Finite Element (FE) simulations of SiC Cascode JFETs and SiC MOSFETs under short circuit conditions have been performed using SILVACO. The objective of the simulation is to understand the internal current density distribution in the devices as well the internal temperature distribution, which cannot be determined during the experiments. The simulation parameters are shown in Table 1. These parameters were selected for obtaining a 1200 V SiC MOSFET and a 1200 V SiC JFET.

The junction-to-case thermal resistance of the simulated device has been optimized to be the same order of magnitude as what is specified on the datasheet. The simulations will also be used to understand why SiC Cascode JFETs are better at suppressing SC currents than SiC MOSFETs.

Table 1. Simulation parameters for the SiC devices

Parameter	MOSFET	JFET
Source doping (cm^{-3})	$1x10^{19}$	$1x10^{19}$
Channel Length (µm)	0.2	1.2
Drift layer thickness (µm)	8.0	10.0
Drift layer doping (cm^{-3})	$1.5x10^{15}$	$1.5x10^{15}$
Drain doping (cm^{-3})	$1x10^{19}$	$1x10^{19}$
P-body doping (cm-3)	$2.5x10^{17}$	-
Oxide thickness (nm)	50	-
JFET gate doping (cm^{-3})	-	$1x10^{19}$

Fig. 7 shows the simulated SC characteristics for the SiC MOSFET and Cascode JFET, for a DC link voltage of 400 V and a SC duration of 4 µs. The gate-source voltage used was 20 V. The simulations also show that the JFET is more effective in suppressing the SC current than the MOSFET and that this results in lower thermal stress since both devices have similar junction-to-case thermal impedances.

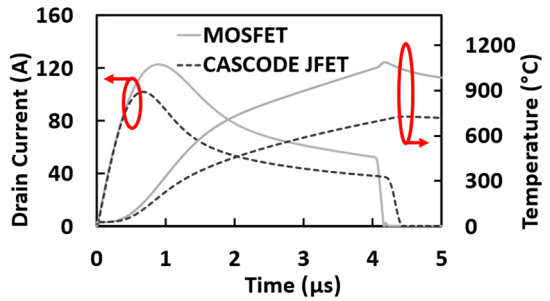
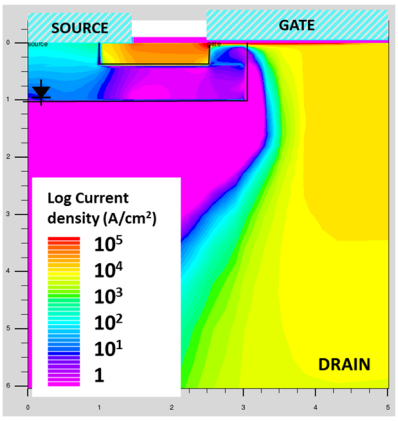


Fig. 7 FE simulation of Short Circuit current and junction temperature of the SiC MOSFET and Cascode JFET

The agrees with the experimental characteristics shown in Fig. 2. The temperatures plotted in Fig. 7 correspond to the hot-spot within the devices and not the average temperatures, hence these temperatures are much higher than what will be deduced from a compact model like SPICE. The simulations also show that the junction temperatures in the SiC Cascode JFET are smaller than those of the SiC MOSFET.

Fig. 8 shows the finite element simulation 2D log current density and 2D temperature contour plots for the SiC MOSFET and the SiC Cascode JFET. Fig. 8(a) shows the 2D current density plot for the SiC MOSFET and Fig. 8(b) shows the same for the SiC Cascode JFET. Fig. 8 shows that for the SiC MOSFET, the highest current densities during the SC occur adjacent to the drain end of the gate oxide interface. In the case of the SiC Cascode JFET, the highest current densities occur midway between the JFET gates. The differences in the current density distributions account for why the SiC Cascode JFET is more effective in supressing SC currents.

The magnitude of the negative temperature coefficient of the SiC MOSFET appears to be less than that of the SiC Cascode JFET due to the more effective mobility reduction resulting from thermally induced phonon scattering in JFETs. Comparing the datasheets of both devices, the ON-state resistance for the SiC MOSFET is 169 mΩ at 25 °C and 189 mΩ at 150 °C. For the Cascode JFET, it is 150 mΩ at 25 °C and 285 mΩ at 150 °C. Hence, the ON-state and saturation resistances are more temperature dependent in JFETs than in MOSFETs. The improved SC performance of SiC JFETs has been evaluated in [17]. SiC Cascode JFETs are capable of higher switching rates compared to SiC MOSFETs [18] (due to reduced parasitic capacitances) while maintaining similar ON-state resistances for similar current ratings. This means JFETs are designed with lower specific ON-state resistances taking advantage of the simpler JFET design since MOS gates are not present. The improved SC performance in JFETs may be attributed to the fact that the drift resistance (with its positive temperature coefficient) dominates the total resistance whereas in MOSFETs, the channel resistance (with its negative temperature coefficient) is a more significant proportion of the total ON-state/SC resistance. Since effective mobility is more effectively temperature limited in the bulk than in the channel, JFETs are more effective in supressing SC currents.



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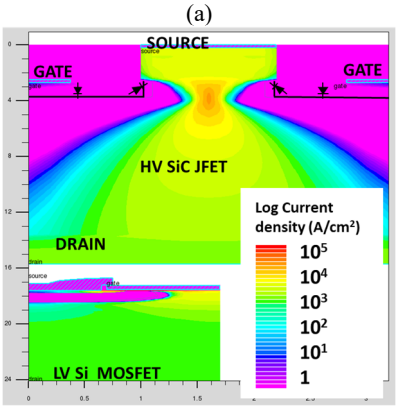
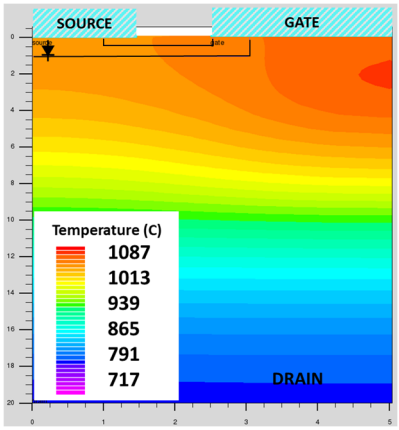


(b)

Fig. 8 2D log current density plots taken 4 µs into the Short circuit for (a) SiC MOSFET (b) SiC Cascode JFET

In [19], repetitive short circuit tests were performed in SiC MOSFETs and Cascode JFETs. The results showed reduced peak SC current in the MOSFET with increasing number of cycles and this was attributed to increased V_{TH} due to BTI and/or reduced effective V_{GS} due to increased gate leakage. No such reduction on peak SC current was observed for the Cascode JFET.

2D temperature distribution plots are shown in Fig. 9(a) for the SiC MOSFET and Fig. 9(b) for the Cascode JFET. Unsurprisingly, the thermal hot-spots coincide with the regions of highest current density for both devices.



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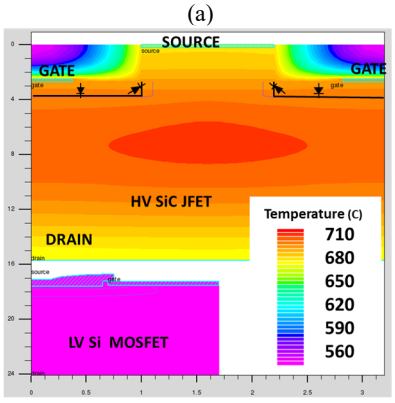
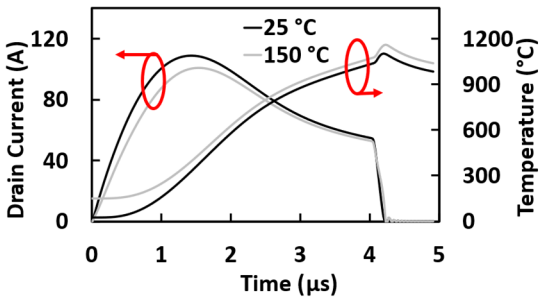


(b)

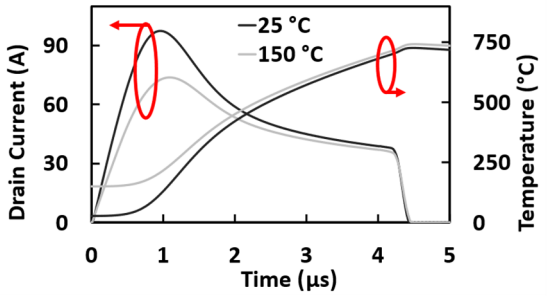
Fig. 9 2D temperature distribution plots taken at 4µs into the Short circuit pulse for the (a) SiC MOSFET and (b). SiC Cascode JFET

Finite element simulations of parallel connected SiC MOSFETs and Cascode JFETs were performed (with different junction temperatures and different threshold voltages) to investigate the current sharing under non-ideal conditions. In the case of unequal initial junction temperatures, the results are shown in Fig. 10(a) for the SiC MOSFET and Fig. 10(b) for the SiC Cascode JFET.

For both devices, the device with the higher initial junction temperature undergoes a smaller junction temperature excursion due to the higher short circuit resistance (and therefore lower peak short circuit current). The higher temperature coefficient of the Cascode JFET short circuit resistance means that the junction temperature difference between the 2 devices narrows more quickly compared to the SiC MOSFET. Hence, temperature difference between parallel devices undergoing short circuits is inherently self-regulating since the device with the higher initial junction temperature experiences a smaller temperature transient, as well as a reduced short-circuit current. In the case of parallel devices with different threshold voltages, the simulation showed wider temperature hot-spots in the device with the lower V_{TH} compared to the device with the higher V_{TH}. Fig. 11 shows simulation results for parallel connected SiC MOSFETs with different V_{TH} (3.14 V vs 4.76 V). The thermal plots are taken 4µs into the short circuit and it shows a wider area of the thermal hot-spot for the device with the lower V_{TH}.



(a)



(b)

Fig. 10 Simulated Short circuit current and hot-spot temperature for parallel connected devices with different junction temperatures for (a) SiC MOSFET (b). SiC Cascode JFET

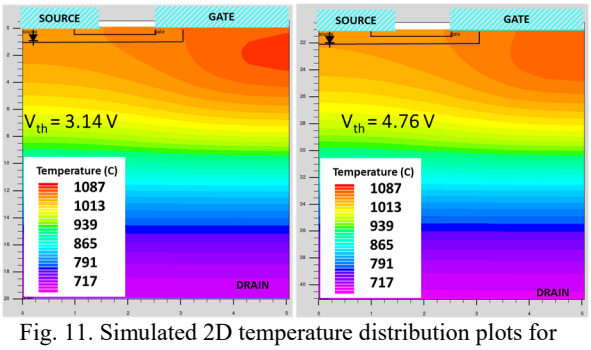


Fig. 11. Simulated 2D temperature distribution plots for parallel connected SiC MOSFETs with different V_{TH} taken at 4µs into the short circuit.

4. Conclusions

Using experimental measurements and finite element simulations this paper has investigated the short-circuit performance of SiC MOSFETs and cascode JFETs in parallel connection. The preliminary results show that temperature difference in parallel devices is not a significant factor in short-circuit robustness since the dynamics between short circuit current and initial junction temperature is self-limiting i.e. the device with the higher initial junction temperature takes a reduced peak short circuit current. However, differences in threshold voltage between parallel connected SiC MOSFETs does impact overall short circuit robustness since the device with the lower threshold voltage takes a higher peak short circuit current. This is less of a problem in SiC Cascode JFETs since V_{TH} variability is less of a problem in the low voltage silicon MOSFET driving the high voltage SiC JFET. Finite elements simulations show the clear differences in current distribution and peak internal chip temperature in parallel SiC MOSFETs with different V_{TH}. The finite element simulations also show that the higher positive temperature coefficient of the saturation resistance limits the SC energy in SiC cascode JFETs.

Acknowledgements

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