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Current Sharing of Parallel SiC MOSFETs under Short Circuit Conditions

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Keywords

«Reliability», «Semiconductor Device», «Wide Bandgap Devices», «Short Circuits», «Paralleling»

Abstract

Device-to-device parametric variations (e.g. threshold voltage V_{TH}, gate resistance R_G and junction temperature T_J) can cause variations in the short-circuit currents conducted through parallel-connected devices. In this paper, the impact of variations in V_{TH}, R_G and T_J on current sharing under short-circuits is investigated using measurements and electrothermal modelling. The results show that V_{TH} is the most critical parameter affecting short-circuit current sharing and directly impacts the peak short circuit current. Variations in gate resistance do not impact the short circuit current sharing unless the variation is over 400% thereby indicating catastrophic failure of the gate wirebond. Variation in the initial junction temperature is also not as critical as variations in V_{TH} since the higher temperature device takes less short circuit current. Electrothermal simulations of parallel connected SiC MOSFETs have been developed to analyze how V_{TH} mismatch impacts short circuit current sharing. These simulations allow for the investigation of the impact of V_{TH} mismatch on the electrothermal stresses of the parallel connected MOSFETs.

Introduction

Uniform current sharing under short circuit conditions is critical for the short-circuit robustness of SiC power modules comprised of parallel connected SiC MOSFETs. Short circuits can occur in power converters either through gate misfiring or short circuits at the load. Although power converters are designed to have mitigation systems to protect the power devices from excessive electrothermal stresses due to short circuits, the devices are however required to withstand the short circuit for a given timeframe. SiC power MOSFETs have been reported to have reduced short circuit withstand times compared to similarly rated silicon devices [1, 2]. The reason for this has been cited as higher thermal resistances and reduced gate oxide reliability [3-7]. The higher thermal resistance, resulting from smaller die size in SiC, results in higher junction temperatures.

While the short circuit performance of devices is down to the individual robustness of the power device, in power modules comprised of parallel connected power devices, the SC performance will depend more on current sharing and electrothermal uniformity between the devices. Under ideal conditions, these devices should share short circuit currents equally. However, parametric differences between parallel

connected devices, (e.g. threshold voltage V_{TH}, gate resistance R_G and junction temperature T_J) can cause variations in the short circuit currents conducted through each device [8-13]. Studies of short circuit performance in SiC power modules have shown poor current sharing to be the primary cause of reduced robustness [9, 14]. Even when devices are initially matched, phenomena like differential V_{TH} drift from different rates of charge trapping of parallel connected SiC MOSFETs can cause small differences in V_{TH} over the operational life of the device [15-18]. Furthermore, the short-circuit characteristics comprise of 2 phases namely (i) an initial rise in current (determined by the series inductance and threshold voltage) and (ii) the reduction of current due to resistive heating. The rate of current reduction during the 2nd stage of the short circuit will depend on the magnitude of the temperature coefficient of the short circuit resistance. Differences in V_{TH}, junction temperature, series parasitic inductance and gate resistance may impact these stages differently.

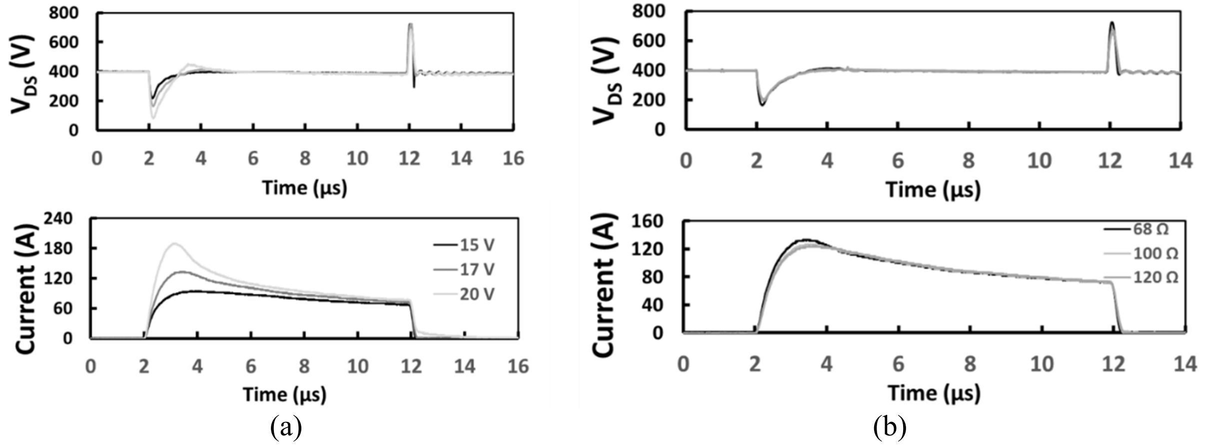
In this paper, the impact of variations in V_{TH}, R_G and T_J between parallel connected SiC MOSFETs on current sharing under short circuit conditions is investigated. An electrothermal model that can accurately predict the short circuit current mismatch as a function of junction temperature difference and threshold voltage difference has been developed. By extending the model to more parallel devices, design guidelines for parallel connection of SiC MOSFETs are provided. Section II presents that experimental measurements of short circuits in parallel connected SiC MOSFETs with parametric variation. Section III presents the electrothermal model calibrated with datasheet parameters and matched with the experimental measurements. Section IV concludes the paper.

Experimental Set-up and Measurements

The circuit diagram of the experimental set-up for the short circuit measurements is shown in Fig. 1(a) while a picture of the test rig is shown in Fig. 1(b). The circuit comprises of a DC voltage source, a 90 µF DC link capacitor, a control 1.7kV/1000A silicon IGBT module with datasheet reference FF1000R17IE4 and the devices-under-test (DUTs). The current through the parallel devices is measured using a Rogowski coil from Powertek. The current and voltage waveforms are captured using an oscilloscope from Teledyne LeCroy. The DUTs are 1.2kV/20A SiC MOSFETs from STMicroelectronics with datasheet reference SCT20N120 and 1.7kV/5A SiC MOSFETs from Cree with datasheet reference C2M1000170.

Fig. 1: (a) Circuit diagram of the test rig, (b) Picture of the test rig and close-up of the of the parallel DUTs circuit.

Fig. 2(a) shows the measured short circuit current and drain-source voltages measured with different gate-source voltages (V_{GS}) for the 1.2kV/20A SiC MOSFET. As expected, the peak short circuit current and short circuit energy increases with increased V_{GS} due to the lower channel resistance [18, 19]. Fig. 2(b) shows short circuit measurements with different R_G where it can be seen that there is a marginal increase in the peak short circuit current as R_G is reduced. As the gate resistance is increased from 68 Ω to 100 Ω and 120 Ω, the short circuit energy decreases from 0.364 J to 0.363 J and 0.362 J respectively.



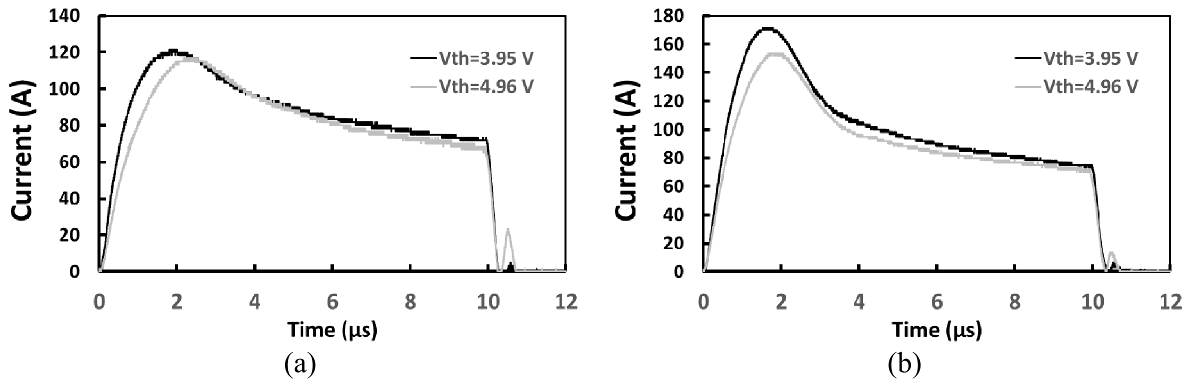
(a) (b)

Fig 2: (a) Impact of gate voltage on SC transients of SiC MOSFET at R_G=100ohm, (b) Impact of gate resistance on SiC transients of SiC MOSFET at V_{GS}=17V.

To evaluate the role of V_{TH} imbalance, short circuit measurements have been performed on SiC MOSFETs with different threshold voltages. The ON-state resistance of a MOSFET is comprised of different elements including source-metal, channel, JFET resistance, drift resistance and substrate resistance, as described in [20], but the main components of the ON-state resistance of the MOSFET can be expressed by equation (1), where the first term accounts for channel resistance while the 2nd term accounts for the drift resistance. The presence of the V_{TH} parameter in the denominator results in increased short circuit current as V_{TH} is reduced.

$$R_{DSON} = \frac{L_{ch}}{W\mu C_{OX}(V_{GS}-V_{TH})} + \frac{L_{drift}}{q\mu N_D A} \quad (1)$$

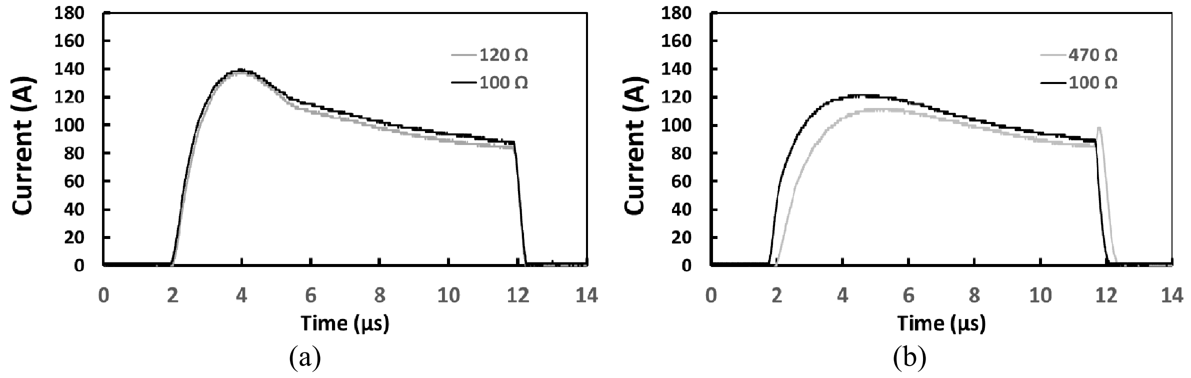
Fig. 3(a) shows the results for parallel connected SiC MOSFETs with 20% variation in threshold voltage with V_{GS} set to 15 V while Fig. 3(b) shows similar measurements with V_{GS} set to 17 V. As expected, the device with the lower threshold voltage conducts a higher short circuit current due to reduced channel resistance. The measured short circuit energy difference between the parallel MOSFETs is 5.1% at V_{GS}=15 V and 8.1% at V_{GS}=17 V.



(a) (b)

Fig. 3: Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with (a) 20% difference in V_{TH} and V_{GS}=15 V, (b) 20% difference in V_{TH} and V_{GS}=17 V.

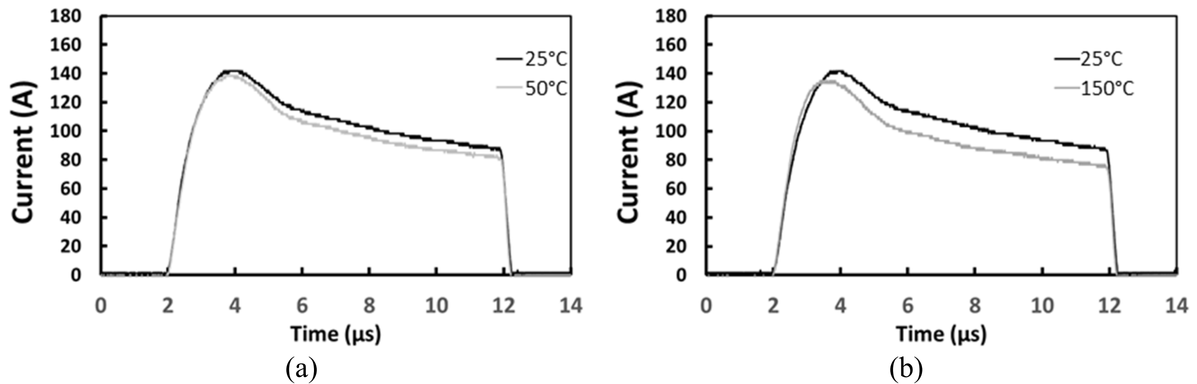
Measurements have also been performed on parallel 1.2kV SiC MOSFETs with different gate resistance. Fig. 4(a) shows measurements with a 20% difference in R_G while Fig. 4(b) shows measurements with over 300% difference in R_G. In Fig. 4(a), the difference in short circuit energy is 4.02% while in Fig. 5(b) it is 5.35% with the faster switching device dissipating more short circuit power in both cases. From the results presented here, differences in gate resistance do not contribute to significant variation in short circuit energy in the parallel pair if the differences in R_G do not exceed 50%. This is because the short circuit duration is much longer than the switching time constant of the devices, which is estimated to be 65 ns by $\tau = R_G * C_{iss}$.



(a) (b)

Fig. 4: Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with (a) 20% difference in R_G, (b) with 370% difference in R_G.

Measurements have also been performed on parallel SiC MOSFETs with different initial junction temperatures. Fig. 5(a) shows measurements on parallel devices with a junction temperature difference set at 25 °C while Fig. 5(b) shows similar measurements with the junction temperature difference set at 125 °C.

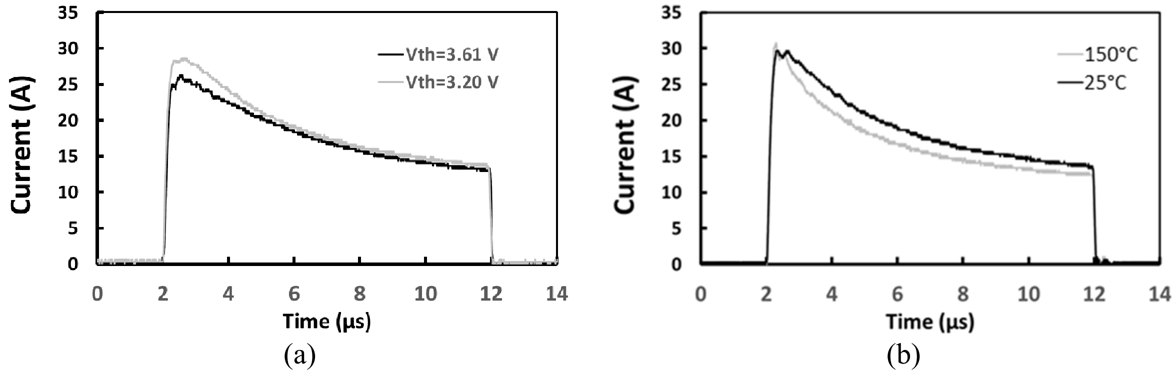


(a) (b)

Fig. 5: Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with (a) 25°C difference in T_j,(b) 125 °C difference in T_j.

In both cases, the device with the lower initial junction temperature conducts a higher short circuit current. The short circuit energy in the device with T_J set to 25 °C is 0.301 J while that of the device with T_J set to 50 °C and 150 °C is 0.283 J and 0.268 J respectively. The positive temperature coefficient of the short-circuit resistance means that the device with the initially higher junction temperature will conduct a smaller short circuit current.

It is expected that V_{TH} difference becomes less important as the voltage rating of the devices increase, since channel resistance becomes dominated by the drift resistance i.e. the 2nd term in Equation (1) dominates the first term. Fig. 6(a) shows short-circuit measurements on parallel 1.7kV/5A SiC MOSFETs with 11.1% difference in V_{TH} while Fig. 6(b) shows similar measurements with 125°C difference in initial junction temperature. For the 1.7kV MOSFETs, an 11.1% difference in V_{TH} between parallel devices results in a 5.5% difference in short circuit energy while a 500% difference in T_J results in a 9.98% difference in short circuit energy. These results presented correspond to different voltage and current rated devices from different manufacturers. Further results on more devices will give a fuller representation on how V_{TH} mismatch impacts different voltage ratings.



(a) (b)

Fig. 6: Measured Short circuit current for parallel 1.7kV/5A SiC MOSFETs with (a) 11.1% difference in V_{TH} , (b) 125 °C difference in T_J.

Electrothermal Modelling of Short Circuits

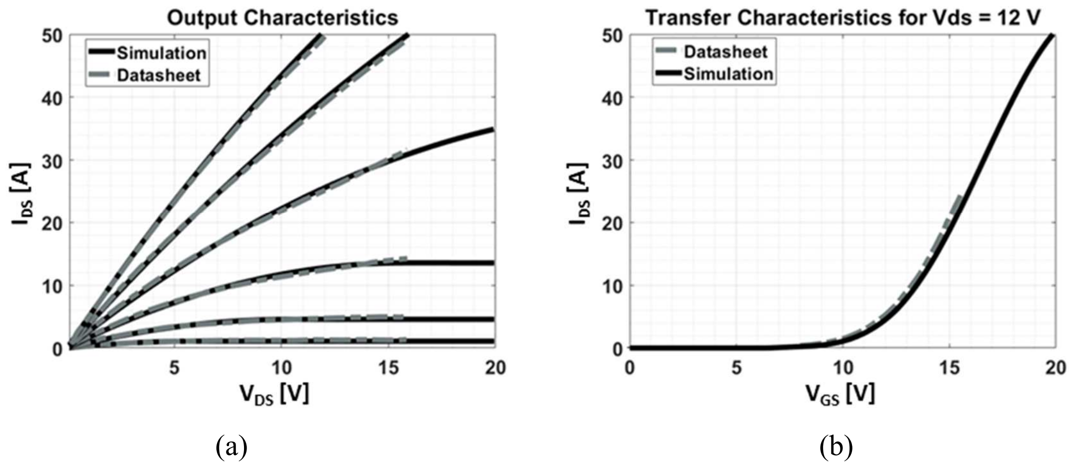
Electrothermal models could be fundamental to investigate the role of parameter mismatch in short circuits in parallel devices, allowing to easily investigate the role of mismatch in parameters like V_{TH}. In this section, an electrothermal model for parallel devices in short circuits is introduced and used to predict the short circuit performance of parallel connected SiC MOSFETs. The static and dynamic characteristics of the model are first developed so that there is good matching between the model and experimental measurements. The static characteristics of the SiC MOSFETs are modelled using equations for I_{DS} as a function of the overdrive voltage (V_{GS}–V_{TH}) and temperature T_J. Equation 1 models that channel current in the ohmic region while equation 2 models the channel current in saturation.

$$I_{chi} = K_i\left[(V_{GS} - V_{TH})V_{DS} - (1+\alpha)\frac{V_{DSi}^2}{2}\right](1+\lambda V_{DS}) \qquad V_{GS} \geq V_{TH} \text{ and } V_{DS} < \frac{(V_{GS}-V_{TH})}{(1+\alpha)} \quad (1)$$

$$I_{chi} = \frac{K_i}{2(1+\alpha)}(V_{GSi} - V_{THi})^2(1+\lambda V_{DSi}) \qquad V_{GS} \geq V_{TH} \text{ and } V_{DS} \geq \frac{(V_{GS}-V_{TH})}{(1+\alpha)} \quad (2)$$

where I_{chi} is the channel current, K_i is the transconductance (or gain) parameter of the MOSFET (which depends on the oxide thickness, die area, effective mobility, and channel length), V_{GS} is the gate-source voltage, V_{TH} is the MOSFET threshold voltage, α is a temperature dependent fitting parameter, λ is the channel length modulation factor.

Using datasheet parameters and characteristics, the electrothermal model has been parameterized for the 1.2kV SiC MOSFET. The temperature dependency of the ON-state resistances and threshold voltage has been accounted for along with the non-linear inter-terminal capacitances. Fig. 7(a) shows the matched output characteristics between the model and the datasheet while Fig. 7(b) shows matched gate transfer characteristics.



(a) (b)

Fig. 7: Simulated characteristics for the 1.2kV SiC MOSFET compared with datasheet (a) output characteristics, (b) transfer characteristics.

The dynamic section of the model is based on the derivation of current and voltage equations using KCL and KVL on the circuit shown in Fig. 8. Table 1 shows the parameters used in the model and the datasheet derived values.

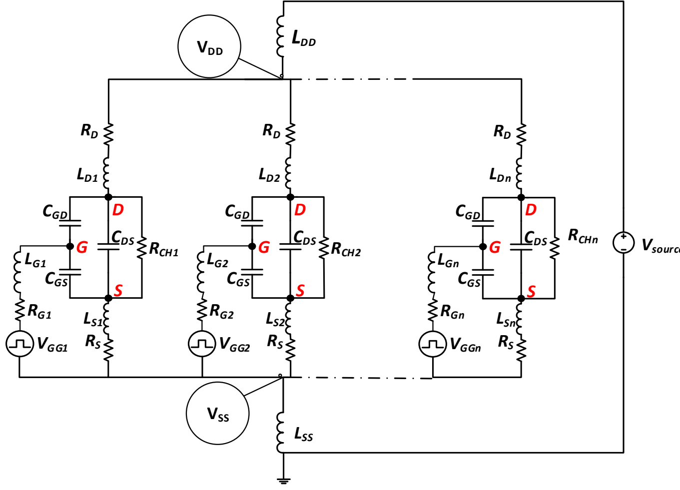


Fig. 8. Equivalent circuit of parallel connected SiC MOSFETs in short circuit set-up.

Parameter	Value
C_{GD}	14 pF
C_{GS}	51 pF
C_{DS}	636 pF
L_{D1}, L_{D2}	15 nH
L_{G1}, L_{G2}	0.1 nH
L_{S1}, L_{S2}	15 nH
L_{DD}	400 nH
L_{SS}	400 nH
R_{G1}, R_{G2}	100 Ω
V_{GG1}, V_{GG2}	20 V
R_{D1}, R_{D2}	1 μΩ
R_{S1}, R_{S2}	1 μΩ

Table 1: Parameters used for dynamic modelling of short circuits. C_{GD}, C_{GS}, and C_{DS} vary with V_{DS}.

Equations 3 to 8 below are generated from applying KCL and KVL to the equivalent circuits shown in Fig. 8.

$$(L_{Di}+L_{Si})\frac{di_{Si}}{dt}-L_{Di}\frac{di_{Gi}}{dt}+(L_{DDSS})\sum_{i=1}^{n}\frac{di_{Si}}{dt}-(L_{DDSS})\frac{di_{Gi}}{dt}+V_{DSi}+i_{Si}(R_S+R_D)-i_{Gi}R_D=V_{source} \quad (3)$$

$$R_{Gi}i_{Gi}+R_Si_{Si}+L_{Gi}\frac{di_{Gi}}{dt}+L_{Si}\frac{di_{Si}}{dt}+V_{GSi}=V_{GGi} \quad (4)$$

$$C_{GS}\frac{dV_{GSi}}{dt}-C_{GD}\frac{dV_{DGi}}{dt}-i_{Gi}=0 \quad (5)$$

$$(C_{GS}+C_{DS})\frac{dV_{GSi}}{dt}+C_{DS}\frac{dV_{DGi}}{dt}-i_{Si}=-I_{chi} \quad (6)$$

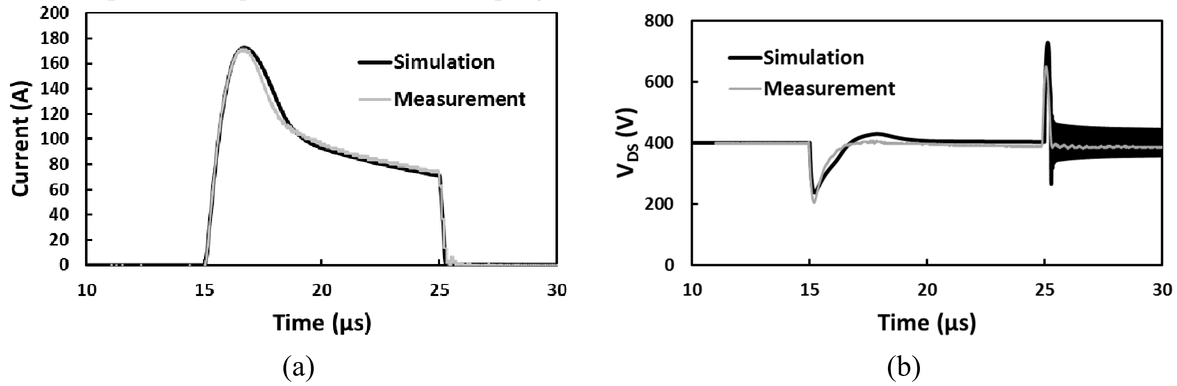
$$I_{Si}-I_{Gi}=I_{Di} \quad (7)$$

$$V_{DGi}+V_{GSi}=V_{DSi} \quad (8)$$

i is the phase number, from left to right according to Fig. 8, and n is the total number of devices connected in parallel. The short circuit model is fully electrothermal since the junction temperature is calculated using a thermal network. The thermal network is implemented as a 4-layer Foster network with the thermal resistances and capacitances derived from the transient thermal impedance characteristic given on the datasheet.

To check the accuracy of the models, the results of the simulations have been plotted together with the measurements. Fig. 9(a) shows the simulated and measured short circuit current while Fig. 9(b) shows the measured and simulated drain-source voltage across the device. In Fig. 9(b), the negative spike during the start of the short circuit is due to the voltage drop across the drain inductance during current rise while the positive spike at the end of the short circuit is due to the voltage across the drain inductance

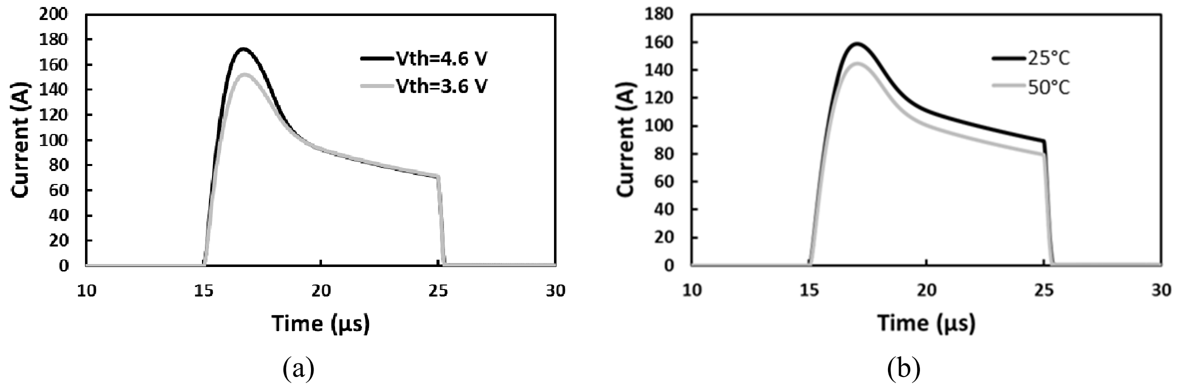
during current fall. The simulated V_{DS} shows more oscillation than what is measured is attributed to the more temperature dependent resistive damping in the measurements.



(a) (b)

Fig. 9: Comparison between simulated and measured short circuit transients in the 1.2kV SiC MOSFET (a) short circuit currents, (b) drain-source voltage.

Short circuit characteristics have also been modelled and matched with the experimental measurements presented in Fig. 10 for parallel connected MOSFETs with different threshold voltages and initial junction temperatures. Fig. 10(a) shows the short circuit simulations and experimental measurements for parallel devices with different V_{TH} while Fig. 10(b) shows a similar plot for parallel devices with different initial junction temperatures. Comparing these modeled short circuit characteristics to the measurements in Fig. 3 and Fig. 5 for the 1.2kV devices, it can be seen that the short circuit behavior of the MOSFET is captured. When the difference between the parallel devices is in V_{TH}, there is convergence in the short circuit current whereas when it is in junction temperature, there is no convergence. This is apparent both in the measurements and simulations.



(a) (b)

Fig. 10: Simulated Short circuit current for parallel SiC MOSFETs with (a) 20% variation in V_{TH}, (b) 25°C difference in $\boldsymbol{T_{CASE}}$

Conclusion

In this paper, the impact of variation in threshold voltage (V_{TH}), gate resistance (R_G) and junction temperature (T_J) between parallel SiC MOSFETs on short circuit robustness has been studied. It is shown that the most critical parameter is V_{TH}, with less impact from by T_J and R_G. V_{TH} mismatch plays a critical role in the first part of the short circuit where the peak short circuit current and its ramp rate is important. In the 2nd part of the short circuit characteristic, initial junction temperature is more important. Electro-thermal modelling is required for further investigation of how these parameters affect short circuit performance of parallel devices with regards to temperature distribution between the devices. The electrothermal model introduced allows for variation of V_{TH} between parallel devices and is capable of extension to any number of parallel devices.

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