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Performance of Wide-Bandgap Discrete and Module Cascodes at Sub-1kV: GaN vs SiC

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***Abstract*—Wide-bandgap (WBG) based cascode devices combine the advantages of the gate driveability and reliability of Silicon MOSFETs with the power conversion efficiency and switching rate of wide bandgap devices. A low voltage (rated at ∼20-30 volts) Silicon MOSFET drives a vertical JFET for the SiC cascode whereas for the GaN cascode, it drives a lateral GaN HEMT. This paper presents the first systematic comparison of the WBG discrete and module cascodes considering conduction losses, 3rd quadrant operation, switching performance, unclamped switching performance, spontaneous switchings, crosstalk as well as the temperature sensitivities. The results show that the GaN cascode outperforms the SiC cascode considerably in switching performance, however, demonstrates higher conduction losses with more temperature sensitivity in GaN. In this paper, it is also shown experimentally and theoretically that the switching rate in the GaN cascode is more sensitive to the gate resistance compared to the SiC cascode. Whilst turn-ON dI_{DS}/dt and dV_{DS}/dt have positive temperature coefficients in the SiC cascode and negative coefficients in the GaN cascode, the SiC cascode is shown to be more UIS rugged, whereas the GaN cascode is incapable of unclamped inductive switching. The impact of unwanted switching on both GaN and SiC cascodes are also shown, indicating that there is a range of optimum gate resistances where un-wanted turn-on and turn-off switchings can be avoided, with the GaN cascode experiencing a higher crosstalk-induced gate voltage due to its higher switching rates.**

***Index Terms*—Silicon Carbide, Gallium Nitride, Cascodes, Power Semiconductor Devices, Temperature,**

I. INTRODUCTION

GALLIUM NITRIDE devices have become attractive for power electronics due to blocking capability as high as 900 V and high switching rates. Compared with Silicon power MOSFETs and even SiC devices, they have low on-resistance and low recovery charge [1], [2]. GaN high electron mobility transistor (HEMT) have very fast switching capability due to the high mobility and higher saturation velocity of electrons in the GaN two-dimensional electron gas (2DEG) layer [3]. These charges result from spontaneous polarization at the AlGaN/GaN hetero-interface where band-discontinuities confine electrons in the quantum wells [4]. However, the lateral structure of the GaN HEMTs limits the rated blocking voltage (due to the presence of high electric field close to the surface) as well as the current handling capability and thermal impedance. Nevertheless, recently there has been significant developments in fabrication of high-quality bulk GaN substrates and there has been progress in development of vertical GaN technology as well. These are yet to be introduced to the commercial market. The lateral devices are fabricated on Silicon substrates with intermediate strain-relaxed buffers necessitated by lattice mismatch between Silicon and GaN. Due to spontaneous charge polarization in AlGaN/GaN, HEMTs are typically depletion mode, though enhancement-mode HEMTs are also being developed with low gate threshold voltages. These include using ohmic or Schottky gate contacts on p-doped AlGaN layers [5]. Whilst GaN power metrics are very attractive, some gate parameters are less so: the low threshold, and low gate voltage headroom, leave potential users with concerns over overall system reliability.

Emergence of Silicon Carbide (SiC) MOSFETs have also significantly improved the switching rates of MOSFETs. This is realized by the thin voltage blocking drift region resulting in low on-state resistance. However, threshold voltage instability by charge trapping at the SiO_2/SiC gate oxide interface has been reported as a significant reliability concern in SiC MOSFETs [6]. This is due to the higher oxide and interface trap density resulting from the presence of carbon atoms during the oxidation of SiC. Threshold voltage instability in SiC MOSFETs can lead to catastrophic failure from poor current sharing in high current applications where parallel devices share current. Furthermore, the energy gap between the conduction bands of the SiC and SiO_2 is lower compared with the same energy gap between Silicon and SiO_2. This also holds true when comparing the energy gaps in the valance bands. The lower available energy gap between SiO_2 and SiC compared with Silicon reduces the admissible electric field in the gate region of the SiC device, even though the critical electric field in its drift region is significantly higher than that of the Silicon. The presence of such higher electric field in close proximity of the gate oxide in SiC devices can also lead to higher gate leakage current, degradation and eventual failure [7], [8].

The aforementioned issues in GaN and SiC devices have to be addressed to ensure reliable operation. In SiC, the gate issues could be tackled by SiC junction field effect transistors (JFETs) where the need for gate oxides are avoided [9]. However, JFETs are depletion-mode (normally-on) devices which is not desirable in power electronics. A method proposed to solve this issue is cascode configurations that pair

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a 1.2 kV rated normally-on SiC JFET with a 20-30 volts rated enhancement-mode (normally-off) Silicon MOSFET [10]. This technique would enable formation of a device with normally-off characteristics while having low on-state resistance and small parasitic capacitances and no traps in the gate oxide.

Similar cascode configuration is also applied to depletion-mode GaN devices. This means normally-on GaN HEMTs are paired with low-voltage (at $\sim$20-30 volts) enhancement-mode Silicon MOSFETs with small parasitic capacitances, resulting in very high switching speeds. This enables a normally-off device with high threshold voltage while still taking advantage of high switching rates of the HEMT. This is particularly beneficial as GaN enhancement-mode HEMTs are reported to exhibit high output capacitance at very high frequencies [11] which means the cascode device will outperform the e-mode devices under 300 V and high switching frequencies due to this excessive output capacitance [11]. It is also noted that the fabrication of the enhancement-mode HEMTs require multiple stages and the subsequent annealing will only partially restore the resulting damages [12]. The low and unstable threshold voltage of e-HEMTs can also be avoided in the cascode configuration. When it comes to the SiC device, the depletion-mode SiC JFETs require more complex gate drivers and have a higher possibility of short-circuits [13]. The enhancement-mode standalone SiC JFETs typically have reduced voltage blocking capability when gate voltage is at 0 V [13] and demonstrated degraded performance at low positive gate voltages [13]. The cascode configuration of the SiC depletion-mode JFET and low voltage enhancement-mode Silicon MOSFET prevented these drawbacks.

A key application of GaN cascodes is in the MHz-switching totem-pole bridgeless power factor correction (PFC) rectifiers [14] due to its small 3rd quadrant recovery charge [15]. Applications where soft switching is necessary, i.e. in [16], is another area where the GaN cascode could be practical. This is especially true as unlike hard switching converters, the requirement of UIS rating for electrothermal stress in soft switching transients is lower [17]. An example of soft switching topologies is in the LLC resonant converters where soft switching techniques (ZVS and ZCS) can be applied, i.e. in the 1 MHz 300 W 400 V LLC resonant converter demonstrated in [18]. A synchronous buck converter using GaN HEMTs is also shown in [18] where the GaN cascode HEMT is shown to have better efficiency than the Silicon MOSFET. This is mainly due to the large junction capacitor in Silicon MOSFETs which stands in the way of easy soft switching through ZVS. The GaN cascodes also have much smaller output capacitance and hence facilitating easy soft-switching implementation [18]. Other applications of GaN cascodes could be in the non-isolated Point-of-Load (POL) buck-regulator converters [13], quadrupled boost converter based on four GaN Cascodes in [19] with potential application in domestic photovoltaic converters [20], and in [21] for active PFC converters. GaN cascode half bridge building blocks are also demonstrated in [22] with a current compensation inductor between two cascode half-bridges phase legs. On the other hand, SiC JFET cascodes enable taking advantage of the very low on-state resistance of JFETs without encountering its disadvantages. The normally-on standalone SiC JFETs are not ideal as more complex gate driver are needed while the on-state increases the possibility of the short-circuits. The depletion-mode standalone SiC JFETs also typically have reduced voltage blocking rating when gate voltage is at 0 V [13] with degraded performance at low positive gate voltages [13]. To counter these, the SiC JFET cascodes are introduced and evaluated in [13] which are shown to deliver high efficiency in power factor corrector (PFC) converters, boost converters and front-end rectifiers without suffering from the drawbacks of the standalone normally-on or normally-off SiC JFETs [23], [24]. Nevertheless, it must be noted that cascode arrangements do also have drawbacks, most notably the additional parasitic inductance added by the leads of the TO-220 and TO-247 packages, which at high switching rates aimed by the GaN devices can lead to significant oscillations.

This paper presents the first systematic comparison of the static, dynamic, 3rd quadrant operation, spontaneous switchings and unclamped switching robustness of SiC and GaN cascode devices as well as the temperature sensitivities. Such comprehensive analysis necessitates a wide range of measurements to grasp a practical understanding of GaN and SiC cascodes in power electronics. Following on, Section II discusses the fundamental structures and switching dynamics, section III discusses the static features of the cascodes, section IV analyzes the dynamic transients, section V explores the key reliability metrics while section VI concludes the paper.

II. Device Structures

Fig. 1 illustrates the simplified cross-section of a vertical SiC JFET as well as a lateral GaN HEMT. The unipolar depletion-mode devices are fabricated as N-channel due to higher effective doping of donors as well as the higher effective mobility and drift velocity of electrons. The N^- drift layer is the voltage blocking region. Applying a negative voltage to the gate of the N-channel JFET results in reverse biasing of the junction of the P-body and N-drift region and spreading of the depletion area to close the channel between the source and drain. The channel is cut-off when the depletion widths on either side of the channel merge.

GaN HEMTs are lateral devices built with heterojunctions between two materials with different bandgaps, commonly GaN and AlGaN. The band-bending at the heterojunction results in the conduction band in the GaN to bend below the Fermi level at the junction. The intrinsic electrons in the GaN move toward the energetically favorable junction. Therefore, a dense (>10^{13} cm^{-2}) thin two-dimensional electron gas (2DEG) layer will be formed in the GaN side of the heterojunction. This majority carrier channel enables effective conduction between drain and source. The devices are currently fabricated on 3” heteroepitaxial wafers with larger wafers anticipated to emerge in foreseeable future. It is commonly fabricated on a Silicon or Silicon Carbide (SiC) or Sapphire (Al_2O_3) substrate. The buffer layer in GaN power devices is usually comprised of multi-layers with nucleation layer, stress-relief

layer and compensation-doped layer to suppress the leakage. This buffer layer is especially important at higher temperatures due to the significant difference in the coefficient of thermal expansion (CTE) of GaN with Silicon as a low-cost substrate. The normally-on conduction of the 2DEG channel can be influenced by a gate metallization in close proximity to the channel in the AlGaN side, hence, it can be turned-off by applying a negative gate voltage to deplete the electrons from the 2DEG channel. P-type doped GaN can be used in the gate to raise the conduction band to above the Fermi level to partially disrupt the 2DEG layer. To ensure that the device is enhancement-mode, the gate should be highly positively doped, however acceptor doping of GaN is very challenging, and therefore this method normally results in low threshold voltages in e-HEMT devices. The channel will form by applying a positive voltage to the gate, which would attract electrons toward the 2DEG channel layer.

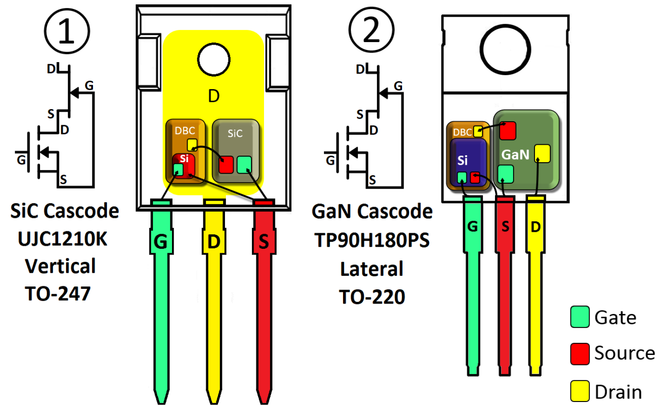


Fig. 2. In GaN cascodes, the 'lateral' HEMT in smaller TO-220 package results in terminal leads in order of GSD [26]. However, most other power transistors including SiC cascodes are 'vertical' in larger TO-247 package with GDS lead sequence [27] (the die sizes are not to scale).

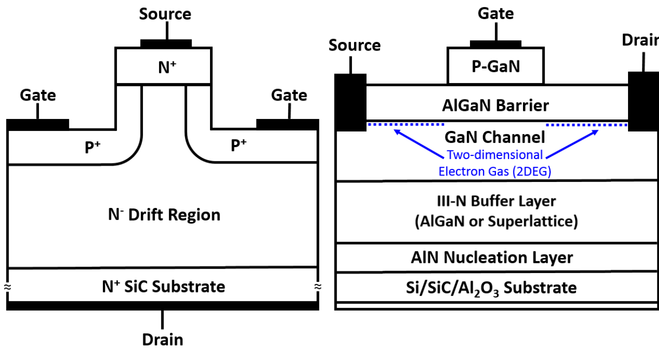


Fig. 1. Cross-section of (left) vertical trench SiC JFET and (right) lateral enhancement-mode GaN e-HEMT.

Cascodes are bundled in discrete leaded packages, such as TO-220, or more recently as modules which are easier to assemble compared with surface-mount HEMT chips. Surface-mount devices (SMD) reduce the stray inductance of leads to enable high switching rates and are soldered directly to the PCB. As shown in Fig. 2, the lateral structure of the GaN device coupled with a low voltage (rated at ∼20-30 volts) Silicon MOSFET as the driving MOSFET results in an inevitable cascode contact-terminal order of gate-source-drain. This is in contrast to the regular order of contact-terminals in power transistors which is gate-drain-source. The SiC cascode is comprised of a vertical SiC JFET and a vertical Silicon MOSFET. Therefore, by using a direct-bond-copper (DBC) layer, the standard GDS order of leads is attainable. The closeness of the gate and source leads in the GaN cascode (due to the GSD order of leads) is beneficial for design of compact gate drivers with minimal parasitics. However, this restricts its application as a choice in upgrading existing converters [25].

Since the drain of the LV Silicon MOSFET is connected to the source of the HV-WBG device and the gate of the latter is connected to the source of the former, the OFF-state drain-source voltage of the LV MOSFET is simultaneously the negative gate voltage of the HV-WBG device. Hence, the blocking voltage of the LV Silicon MOSFET should be greater than the absolute value of gate threshold of the depletion mode WBG device. The threshold in GaN HEMTs is typically about 1-2 volts [28] while in SiC JFET is as high as 5 volts [29].

Distinguished sets of devices are selected for the 'performance' and 'reliability' tests to ensure validity of assessments. In the static and dynamic performance tests, the devices with 'highest voltage rating' are used, while for the reliability tests the devices with 'closest current rating' are tested. In sections III and IV, the SiC cascode is UnitedSiC's UJC1210K device with ratings of 1.2 kV and 14 A at 100°C while the GaN cascode is Transphorm's TP90H180PS with ratings of 900 V and 10 A at 100°C. The slightly lower ratings of this state-of-the-art GaN device than the SiC device suggests that moderately poorer conduction performance and marginally better dynamics could be expected. However, the measurements will show that differences are far more substantial. For dynamic measurements in Section IV, in addition to discrete cascode devices, GaN cascode module have also been tested. This is the GaN Cascode module TPD3215M rated at 600 V and 40 A at 100°C. In absence of a similarly rated SiC module at 600 V, Silicon power MOSFET module IXFN82N60P with ratings of 600 V and 41 A at 100°C is used as the benchmark for comparison of the switching rates. For the reliability tests, the SiC cascode is UnitedSiC's UJ3C065080K3S device with ratings of 650 V and 23 A at 100°C while the GaN cascode is Transphorm's TP65H050WS with similar ratings of 650 V and 25 A at 100°C. The Silicon power MOSFET is IXYS's IXFH16N120P, the SiC MOSFET is Wolfspeed's C2M0160120D and the Silicon superjunction MOSFET is Infineon's IPW90R340C3.

III. Static Performance

A key parameter in analyzing the two cascode technologies is the static on-state conduction losses generated by the on-state resistance ($R_{DS\text{-}ON}$) which is tested here by means of forward conduction and reverse conduction measurements.

Forward Conduction: The ON-state performance of the devices is measured by passing a constant current pulse through the devices with the gate voltage at the rated value. The voltage measured across the devices will be the ON-state voltage as the product of the ON-state resistance and the current, as in Fig. 3. As the current passes through the device, the resistive heating results in a junction temperature rise that depends on the junction-to-case transient thermal impedance. The positive temperature coefficient of the ON-state resistance means that the ON-state voltage will rise with time during the pulse. Since the SiC and GaN devices have similar high temperature current ratings (but different current ratings at 25°C), the specific ON-state resistance was calculated to account for differences in the chip area. The chips were de-capsulated and the device areas were measured by microscopes as approximately 7 mm^2 for the GaN HEMT and 5 mm^2 for the SiC JFET. The measurement results are shown in Fig. 4 for both devices conducting 5 A and 10 A current for 5 seconds. The measurements indicate that the specific ON-state resistance and its temperature coefficient is one and four orders of magnitude higher for the GaN cascode device than in the SiC cascode. The datasheet values of the drain-source on-resistance of the GaN and SiC devices is higher than indicated in Fig. 4 (170 mΩ vs. 130 mΩ in GaN and 70 mΩ vs. 40 mΩ in SiC). This discrepancy is mainly due to the elevated applied gate-source voltage in the measurements compared with test conditions of the datasheet (V_{GS} of 15 V vs. 12 V). This means a more conductive channel in the driving Silicon MOSFET device, and consequently formation of a more conductive current path and lowered drain-source on-resistance.

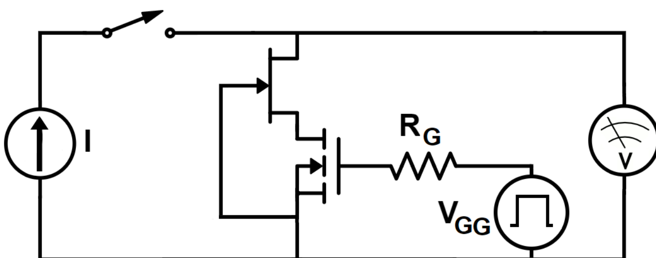


Fig. 3. Measurement schematic of characterizing ON-state resistance.

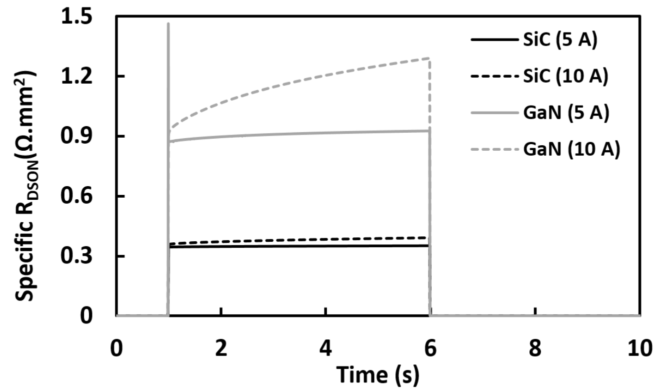


Fig. 4. Specific ON-state resistance of the SiC and GaN cascode devices conducting 5 A and 10 A and its increase by self-heating.

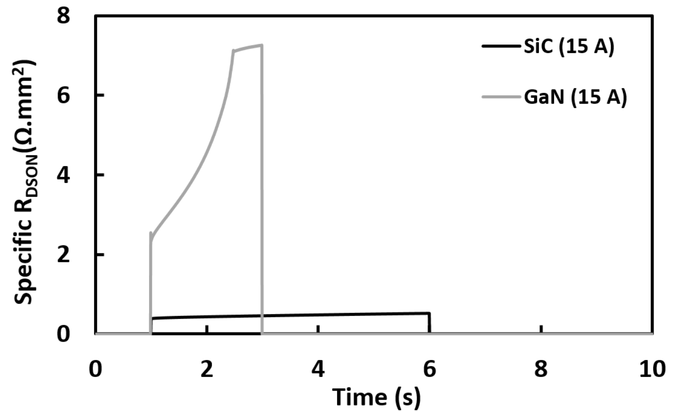


Fig. 5. Specific ON-state resistance of the SiC and GaN cascode devices conducting 15 A.

The higher temperature coefficient of the specific ON-state resistance in GaN can be attributed to: (i) the lower thermal conductivity in GaN, and (ii) the lateral architecture of the GaN-on-Si HEMT which means that, unlike vertical devices, the substrate is not available for current conduction, and (iii) the packaging of the GaN cascode, i.e. the backside could be electrically isolated (with a lateral enhancement-mode Silicon MOSFET) by the use of an insulator typically ceramic. As the load current is increased to 15 A (which is the room temperature rating of the tested GaN device), the impact of the higher thermal impedance becomes clearer as in Fig. 5. This leads to the dissipated power in the GaN device forcing the current source to saturate.

Reverse Conduction: The 3rd quadrant conduction characteristics have also been characterized for the devices by passing a current pulse through the body diode similar to the forward conduction measurements. The measurement results are shown in Fig. 6 for 5 A and 10 A reverse currents. The results show that the SiC cascode has a lower body diode forward voltage than the GaN cascode device. Since the driving Silicon MOSFETs are low voltage (rated at ∼20-30 volts) power MOSFETs with typical body diode forward voltages of less than 800 mV, the difference in the body

diode voltages and the trends in its increase with junction temperature can be attributed to the properties of the WBG material.

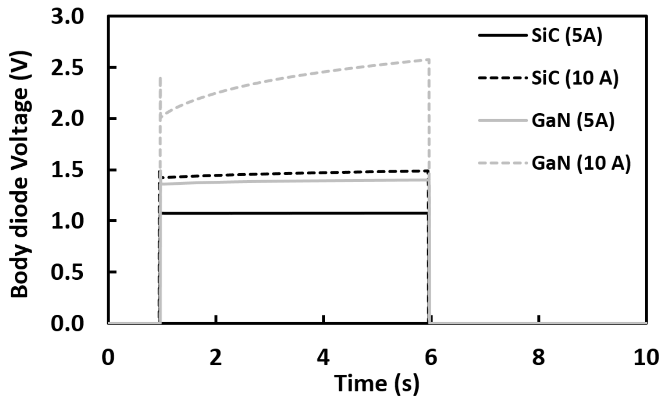


Fig. 6. Body diode forward voltages for the SiC and GaN cascode devices conducting 5 A and 10 A reverse currents and its increase by impact of increased temperature due to self-heating.

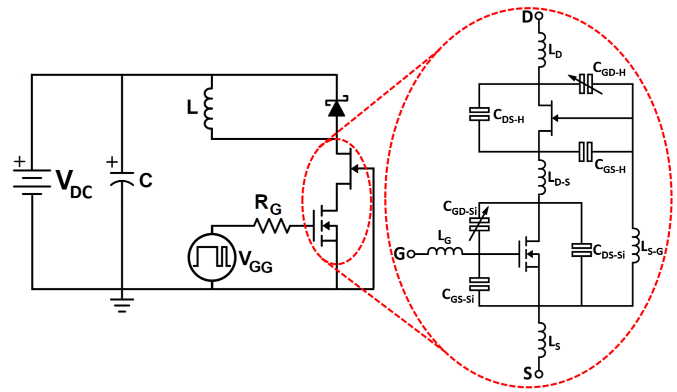
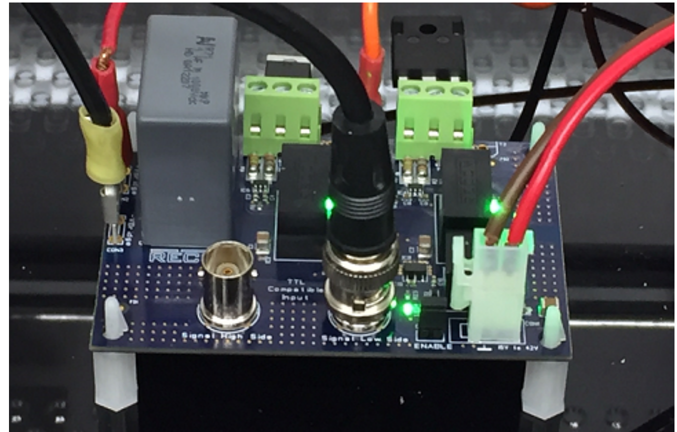


Fig. 7. The schematic of the test circuit with double pulse gate driver (V_{GG}) and cascode transistors as DUT connected to a SiC SBD along with all parasitic components.

IV. Dynamic Performance

Fig. 7 shows the double-pulse test circuit [14] that is used in these measurements to determine the dynamic transients performance, while Fig. 8 shows a photo of the rig used for evaluating the transients of the devices. As illustrated, the device under test is referenced to the low-side, while a SiC Schottky diode (SBD) from Wolfspeed (C4D08120A) is used as the high-side free-wheeling diode as in Fig. 7. In Fig. 8 only the low-side gate driver functions, and the minimum gate resistance is 10 Ω. The gate voltage is 15 V which is significantly higher than the 6 V upper limit of the standalone GaN HEMTs, thereby enabling the cascode to be driven with standard gate drivers designed for 1.2 kV rated MOSFETs and IGBTs. The devices are tested at 650 V to leave sufficient room to 900 V rating for peak overshoots while 5 A load current is set by the pre-defined length of the gate driver pulse. Only the DUT transistors are heated from 25°C to 175°C in steps of 25°C. Table I shows the values of the test components and conditions, while Table II shows the key parameters of the gate driver.



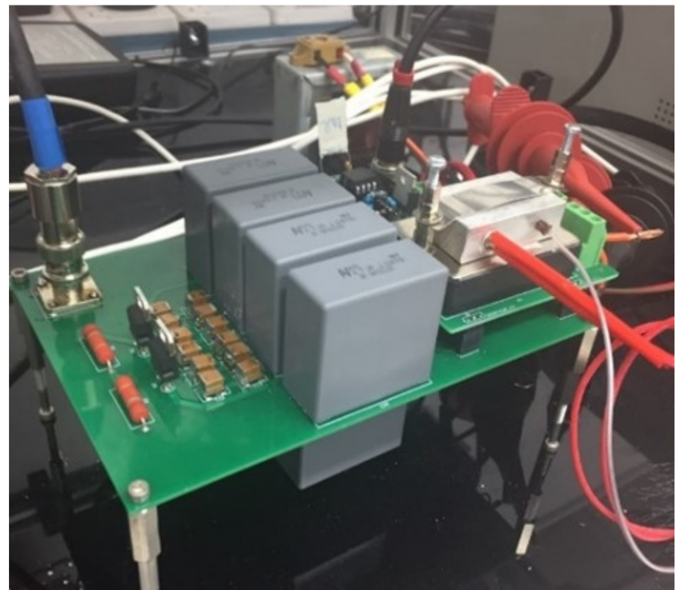


Fig. 8. The high voltage test boards used in the measurements with the connected discrete (top) and module (bottom) cascodes with the Schottky barrier diodes and on-board DC link capacitor and gate driver.

TABLE I
MEASUREMENT TEST RIG COMPONENT VALUES

Parameter	Symbol	Value
DC Capacitor	C_{DC}	5 mF
Load Inductor	L	2 mH
Voltage	V	650 V
Current	I	5 A
Charging Pulse Length	t_{q1}	15 μs
Switching Pulse Length	t_{q2}	5 μs
Gap between Pulses	$t_{q\text{-}nil}$	5 μs
Temperature Range	T	25-175°C
Gate Resistance Range	R_G	10-220 Ω

TABLE II
GATE DRIVER CIRCUIT PARAMETERS

Parameter	Symbol	Value
Driver Input Supply Voltage	V_{Sig}	5 V
Driver Input Supply Current	I_{Sig}	5 mA
Output Gate Voltage	V_{GG}	15 V
Peak Output Gate Current	I_{GG}	2 A
Gate Pulse Filter Capacitor	C_f	1 μF
Driver Filter Capacitor	C_d	100 nF
Supply Isolation Capacitance	C_{iso}	Max 300 pF
Common-Mode Transient Immunity	$\lvert CM \rvert$	Min 25 kV/μs

Fig. 9(a) shows the double-pulse currents for all devices when switched with a low R_G. As seen, the turn-off delay by the plateau voltage as a result of the Miller capacitance is short for all devices and the temperature increase to 175°C does not have a significant impact on it as in Fig. 9(b). However, as the device is slowed down, as in Fig. 10(a), the impact of the Miller capacitance on the plateau duration, which delays the drop of the transistor's current, increases. This demonstrates that not only SiC and GaN devices have faster transients, but the reaction time to gate voltage commands is not as dependant on gate resistances when compared with the Silicon counterparts. It can also be seen in Fig. 10(b) that by increase of temperature to 175°C and reduction of the threshold voltage of the device, it is slowed down and this delay is much more prolonged in Silicon devices than in SiC and GaN cascodes.

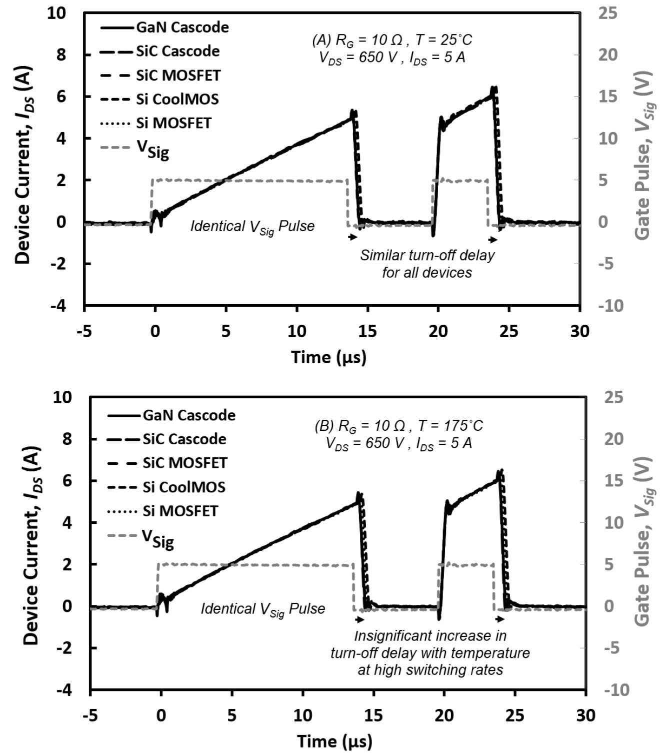


Fig. 9. The turn-off delay period at very high switching rates is almost the same for all devices with negligible temperature sensitivity.

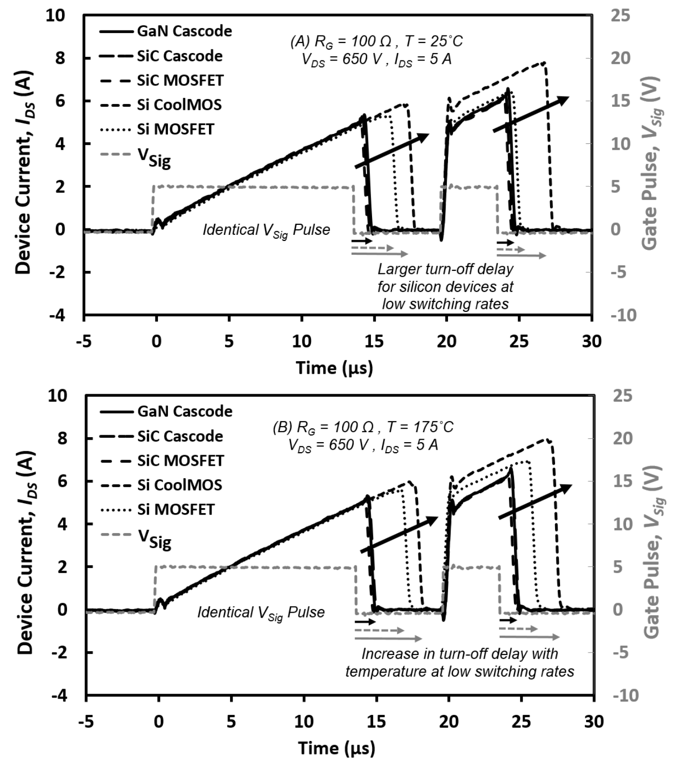


Fig. 10. The turn-off delay period at low switching rates is significantly higher for Silicon MOSFETs and it is temperature-dependant.

Turn-ON: Fig. 11 shows the turn-ON current and voltage transients of the GaN and SiC cascodes with a gate resistance of 10 Ω at room temperature. It is seen that the GaN cascode is faster than the SiC cascode, and as a result both its current and voltage transients have more pronounced oscillations. The 10 MHz frequency oscillations in both devices' current transients are coupled with the oscillations in the voltage of the SiC Schottky diode and can be damped with a small DC link de-coupling capacitor (in range of 100 nF). The faster 50 MHz ringing in the drain-source voltage of the GaN HEMT is harder to damp.

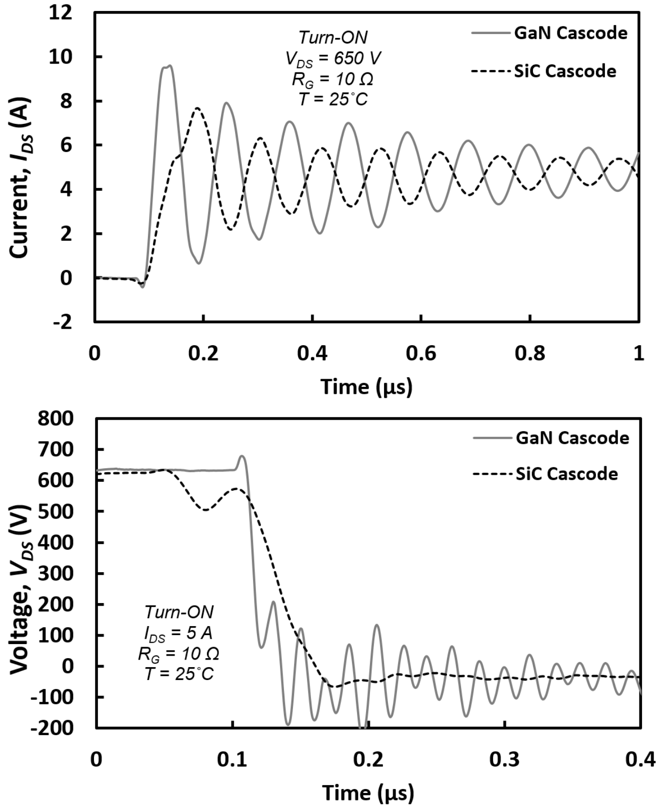


Fig. 11. Turn-ON transients of GaN and SiC cascode with R_G of 10 Ω.

Fig. 12 shows the turn-ON current transient times for both devices at the whole range of gate resistances and temperatures. It can be seen that the current transient times in GaN cascode increases with temperature while it is slightly reduced in SiC cascode. This trend in SiC is expected as by decrease of the threshold voltage with temperature, the switching rate increases. The threshold voltage of the GaN HEMT follows the same trend with the exception that mobility has a more pronounced impact as its 2DEG layer is a few times thinner [30] in GaN HEMTs than the typical channel inversion layer in MOSFETs. This is seen in static measurements by increase of the on-state resistance in Fig. 4. This results in reduction of switching rate with temperature in GaN devices. When it comes to module structures at higher current ratings (40 A vs. 10 A), it can be seen in Fig. 13 and Fig. 20 that the current transient times are longer in GaN module compared with the GaN discrete device due to its 3 times larger input capacitance. Nevertheless, when compared with similarly rated Silicon power MOSFET module, the GaN module consistently has a lower current transient time at turn-ON due to its 10 times smaller parasitic capacitances at the same ratings. This is even clearer when the gate resistance increases which indicates lower dependence on the gate current due to the smaller capacitances, enabling damping of the unwanted oscillations without a considerable impact on the switching energy.

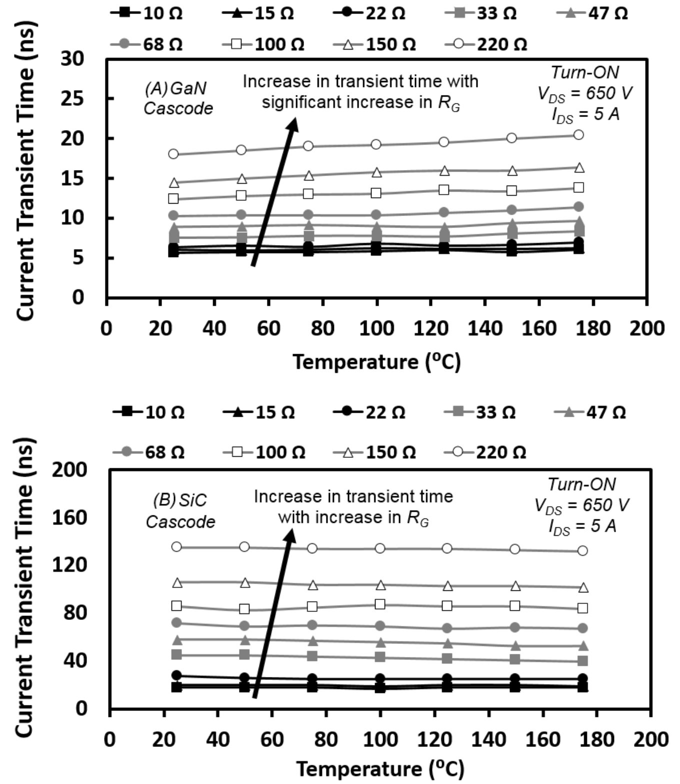


Fig. 12. The current transient time in GaN and SiC Cascode Device at turn-ON transient in wide range of gate resistance and temperature.

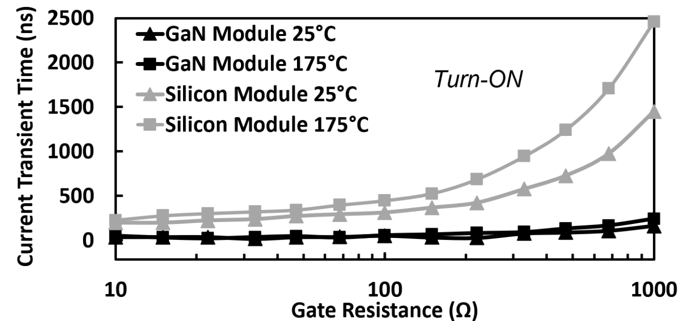


Fig. 13. The GaN module consistently has a lower transient time for the current transition at turn-ON transient due to 10 times smaller parasitic capacitances at the same ratings.

Fig. 14 shows the magnitudes of dI_{DS}/dt and dV_{DS}/dt (by 10%-90% gradients) versus R_G, for both SiC and GaN cascodes at 25°C. As seen, the gradients of both current and voltage in the GaN cascode are significantly larger than those

of the SiC cascode. The turn-ON dI_{DS}/dt in the GaN cascode device is 350% and 750% higher than that of the SiC cascode device at R_G = 10 Ω and 220 Ω respectively. The results also show that the switching rate in the GaN cascode is less dependent on R_G compared to the SiC cascode. In the SiC and GaN cascode at 25°C, the turn-ON dI_{DS}/dt drops by 600% and 250% respectively as R_G is increased from 10 Ω to 220 Ω. When the junction temperature increases to 175°C, the percentage drops in dI_{DS}/dt are 700% and 300% for the SiC and GaN cascode respectively. Hence, as the gate resistance is reduced, the GaN cascode increasingly outperforms the SiC cascode. This is partly due to the smaller input capacitance of the lateral MOSFET in GaN cascode compared with the vertical MOSFET in the SiC cascode. However, a significant element in the fast switching rate of the GaN cascode device is the rapid switching of the HEMT. This is seen clearly in the significant drop in the GaN dV_{DS}/dt with R_G, indicating that the MOSFET switching rate dominates the slower turn-on transients at low gate currents.

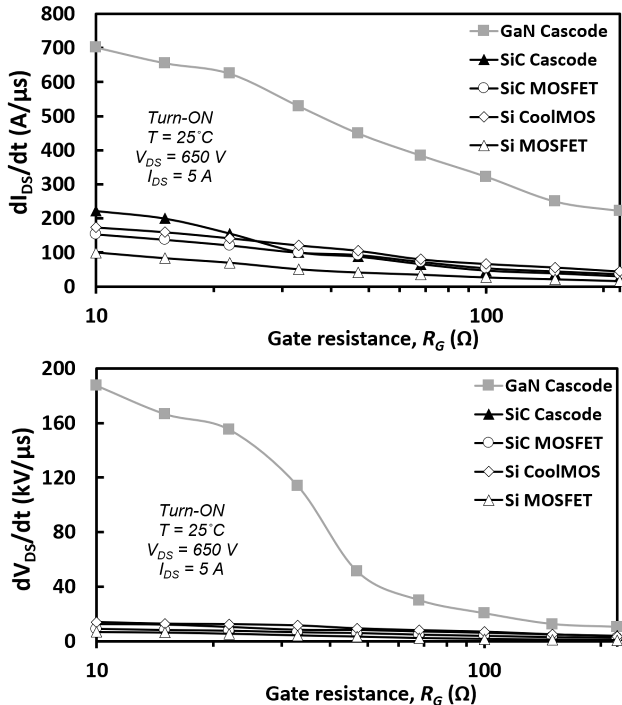


Fig. 14. Turn-ON dI_{DS}/dt and dV_{DS}/dt of GaN, SiC and Si devices at 25°C.

The temperature sensitivities of the switching rates have also been compared. The results are shown in Fig. 15 where the turn-ON dI_{DS}/dt for both technologies (switched with R_G = 22 Ω and 220 Ω) are shown as functions of temperature. Fig. 15 shows each set of measurements have been normalized by the turn-ON dI_{DS}/dt and dV_{DS}/dt at 25°C, respectively. Both plots show that the turn-ON switching rates in SiC increase with temperature while those in GaN reduce with temperature. The results indicate the increased temperature sensitivity of switching rates in GaN which correspond to the measurements in Fig. 4 that also showed higher sensitivity of the ON-state resistance to temperature. In the case of the static ON-state measurements, the increased temperature sensitivity in GaN is due to the increased junction to case transient thermal impedance (Z_{TH_J-C}) resulting from the overall smaller device size in GaN compared to SiC. However, under dynamic switching conditions of a double pulse test, there is insufficient time for dissipation of heat from the junction during the switching transients. Hence, the increased temperature sensitivity is not due to increased Z_{TH_J-C}. The reason for increased temperature sensitivity in GaN during switching transients is the mobility degradation in the 2DEG due to increased acoustic phonon scattering with temperature. This is more critical in GaN than in SiC because of less intrinsic carrier generation with temperature and reduced doping in GaN compared to SiC. As a result, there is less threshold voltage reduction due to increased intrinsic carrier density in GaN compared to SiC. The doping of body and drift region is also much higher in low voltage devices and therefore the increase of generated carrier in higher temperatures is no longer distinct. These mean both cascodes driven by a low voltage (rated at ∼20-30 volts) MOSFET are significantly less temperature dependent.

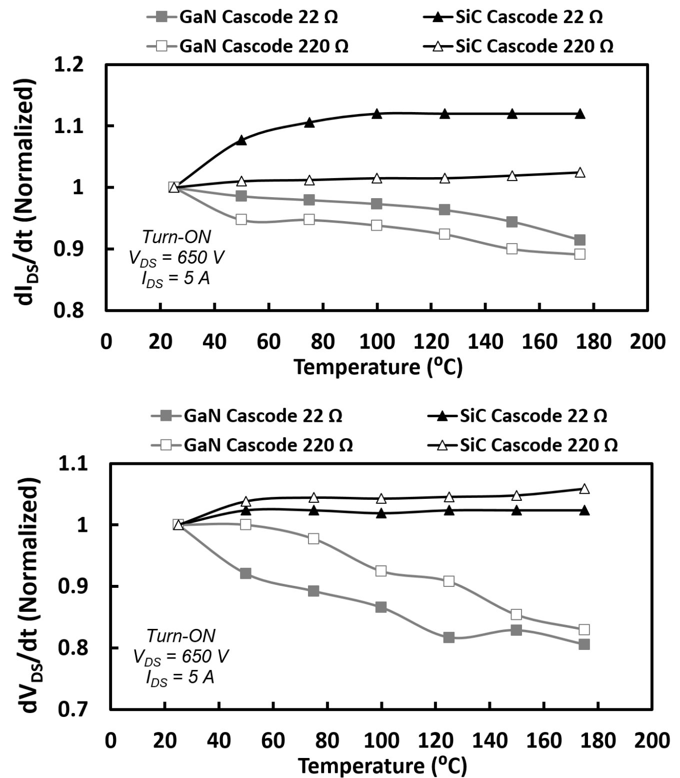


Fig. 15. Normalized dI_{DS}/dt and dV_{DS}/dt with temperature in GaN and SiC Cascode Devices at turn-ON.

The turn-ON dI_{DS}/dt and dV_{DS}/dt at 25°C and 175°C of the GaN cascode module compared with a Silicon power MOSFET modules can also be seen in Fig. 16 and 17 where the significant superiority of the GaN module can be seen, albeit with more oscillations. These transient plots indicate that the switching rate of the GaN device is not significantly impacted by the increase of the gate resistance regardless of

temperature while the Silicon power MOSFET is severely influenced, which is in-line with the observation in Fig. 13.

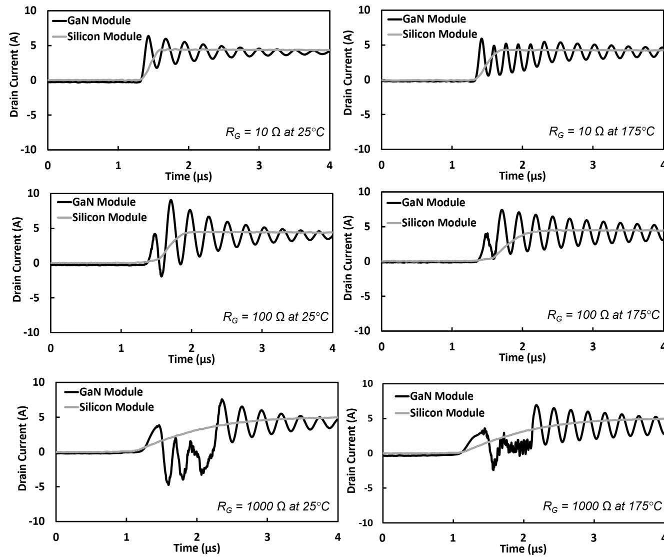


Fig. 16. The turn-ON current transient of the GaN cascode module compared with a Silicon power MOSFET modules at 25°C and 175°C and selected gate resistances.

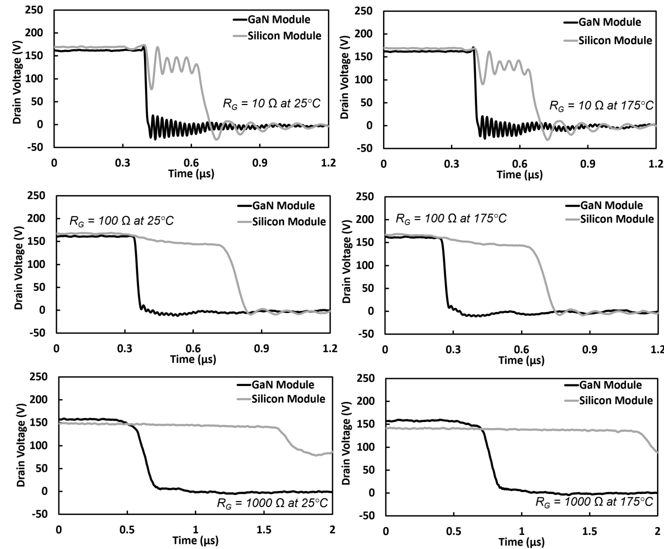


Fig. 17. The turn-ON voltage transient of the GaN cascode module compared with a Silicon power MOSFET modules at 25°C and 175°C and selected gate resistances.

Turn-OFF: Similar trends are seen at turn-OFF as in Fig. 18. The fast switching of GaN device with low gate resistances results in significant ringing on the output while this ringing is significantly less in the SiC cascode with a slower rate of rise/fall upon switching. This is mainly due to the fact that the gate charge in the GaN cascode is 5 times smaller than that of the SiC device and the input capacitance is 3 times smaller, so the device switches much faster with a smaller gate current requirement. To damp these oscillations, manufacturers have suggested using higher gate resistances on the driver, however the damping of oscillations by this method will result in a close rate of switching for the GaN and SiC cascodes, and effectively eliminating the key advantage gained by the application of GaN devices. The SiC cascode has many other advantages such as higher threshold voltage (realized by difference in the threshold voltage of the JFET and HEMT in addition to the ease of attaining higher threshold voltage in vertical MOSFET) and higher power dissipation capability by lower thermal resistance. Therefore, other methods for damping of the GaN oscillations must be applied to the gate driver, such as insertion of ferrite beads in the gate path.

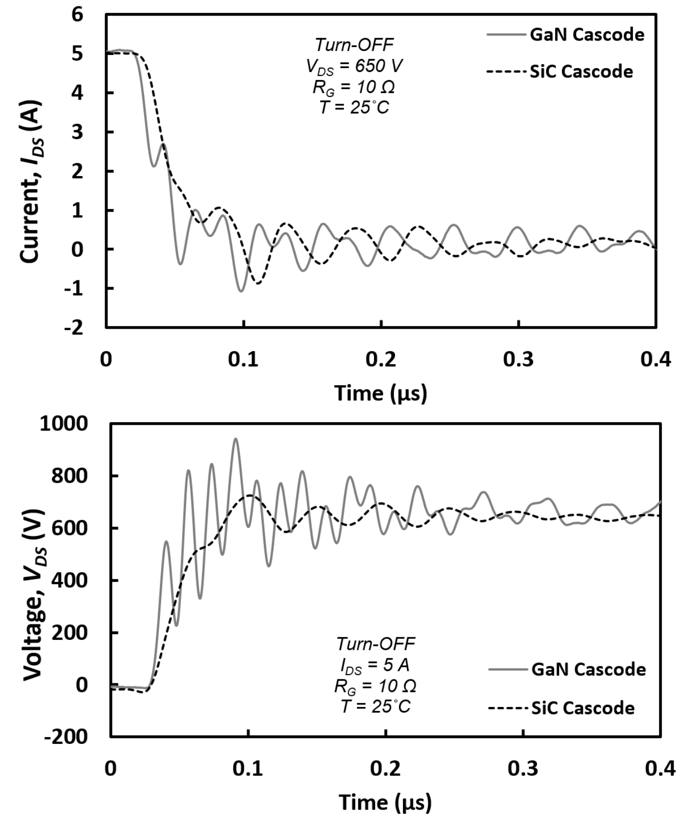


Fig. 18. Turn-OFF transients of GaN and SiC cascode with R_G of 10 Ω.

Fig. 19 shows the current transients for both SiC and GaN cascode devices at turn-OFF for the wide range of temperatures and gate resistances. As seen, the transient durations for both devices slightly increase with temperature. It can also be seen that the switching rate of the GaN device is more sensitive to the increase of the gate resistance compared with the SiC devices. The pronounced advantage of GaN devices at turn-ON, where the current transient time in Fig. 12 was much lower than that of the SiC cascode device, is less clear at turn-OFF especially when switched with higher gate resistances.

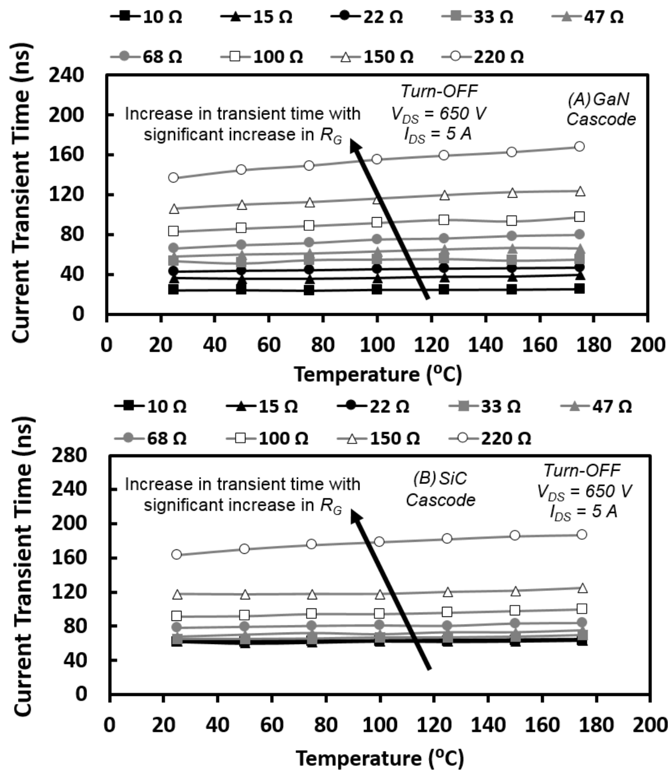


Fig. 19. The current transient time in GaN and SiC Cascode Device at turn-OFF transient in wide range of gate resistance and temperature.

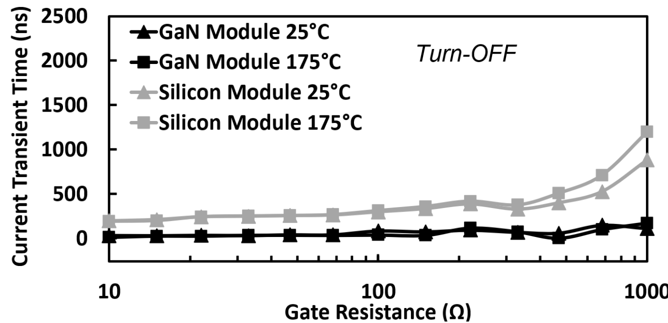


Fig. 20. The GaN module consistently has a lower transient time for the current transition at turn-OFF transient due to 10 times smaller parasitic capacitances at the same ratings.

Fig. 21 shows the turn-OFF dI_{DS}/dt and dV_{DS}/dt at 25°C for both SiC and GaN devices. Similar to turn-ON, the dI_{DS}/dt and dV_{DS}/dt are higher for the GaN cascode than the SiC cascode. However, unlike turn-ON, the GaN cascode dI_{DS}/dt is only 40% and 10% higher at 25°C and 175°C. Furthermore, as the gate resistance is increased from 10 Ω to 220 Ω, the turn-OFF dI_{DS}/dt decreases by 600% at 25°C and 300% at 175°C for the GaN cascode. For the SiC cascode, this is 400% at 25°C and 250% at 175°C. Fig. 22 shows the normalized dI_{DS}/dt and dV_{DS}/dt as a function of temperature for the 2 different gate resistances. It is seen that increasing the temperature from 25°C to 175°C causes the turn-OFF dI_{DS}/dt to decrease by 30% in the GaN cascode and 15% in the SiC cascode. For dV_{DS}/dt, this is 60% and 10% respectively. The negative slopes in GaN device is more pronounced than the SiC device and are due to the reduced threshold voltage and reduced carrier mobility which prolongs the turn-off transients.

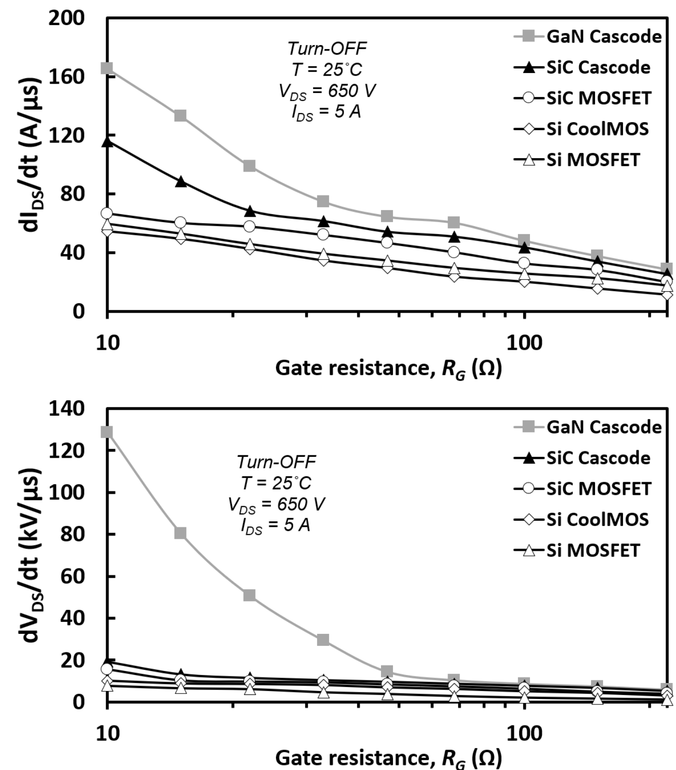


Fig. 21. Turn-OFF dI_{DS}/dt and dV_{DS}/dt of GaN, SiC and Si devices at 25°C.

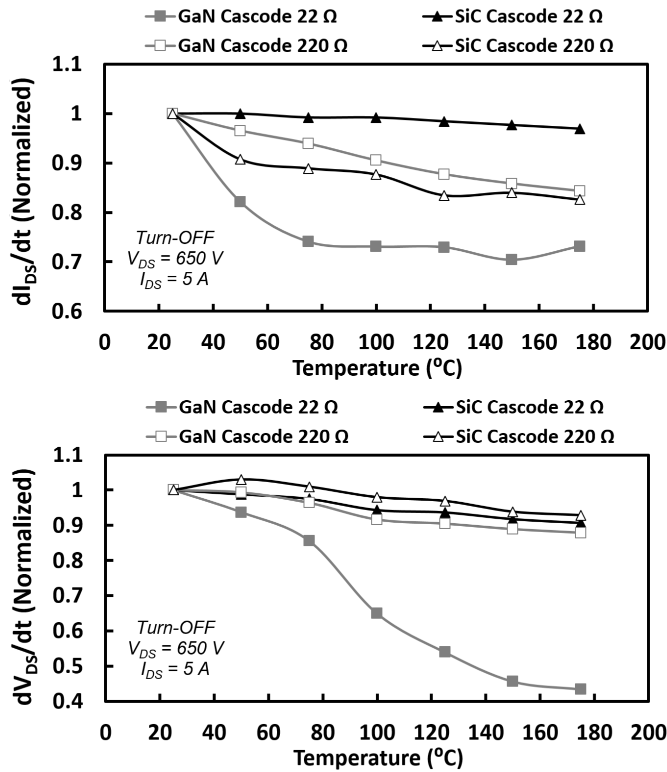


Fig. 22. Normalized dI_{DS}/dt and dV_{DS}/dt with temperature in GaN and SiC Cascode Devices at turn-OFF.

Fig. 23shows the switching energy of the SiC and GaN devices in 25°C and 175°C in 10 Ω and 100 Ω gate resistances. As seen, the GaN device has significantly lower switching energy compared with the SiC device at turn-ON. This is in-line with observation in Fig. 14. At turn-OFF, the difference between the dI_{DS}/dt and dV_{DS}/dt is not as distinct, as seen in Fig. 21, which is reflected in close switching energy in Fig. 19.

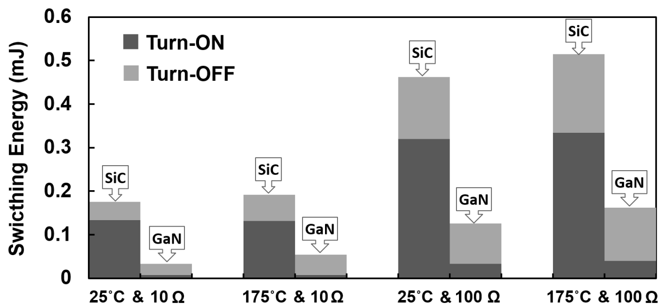


Fig. 23. Switching Energy advantage of GaN over SiC devices in 25°C and 175°C confirming the trends seen by dI_{DS}/dt and dV_{DS}/dt.

The turn-OFF dI_{DS}/dt and dV_{DS}/dt at 25°C and 175°C of the GaN cascode module compared with a Silicon power MOSFET module can also be seen in Fig. 24 and 25 where the significant superiority of the GaN module can be seen, albeit with more oscillations. These transient plots indicate that the switching rate of the GaN device is not significantly impacted by the increase of the gate resistance regardless of temperature while the Silicon power MOSFET is severely influenced, which is in-line with the observation in Fig. 20.

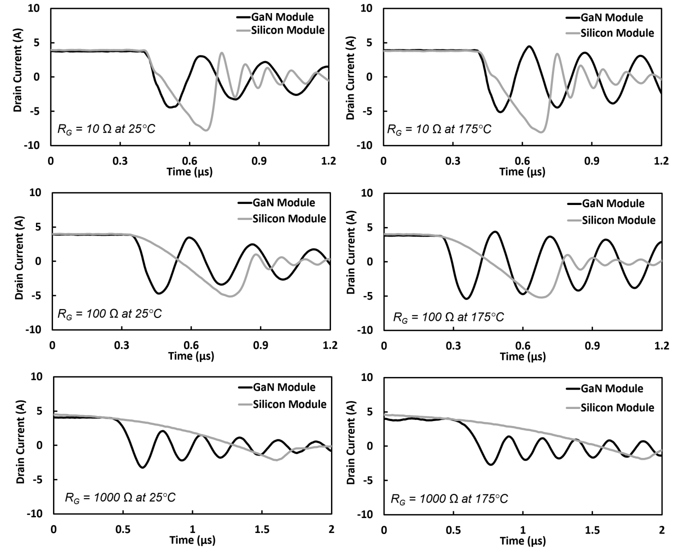


Fig. 24. The turn-OFF current transient of the GaN cascode module compared with a Silicon power MOSFET modules at 25°C and 175°C and selected gate resistances.

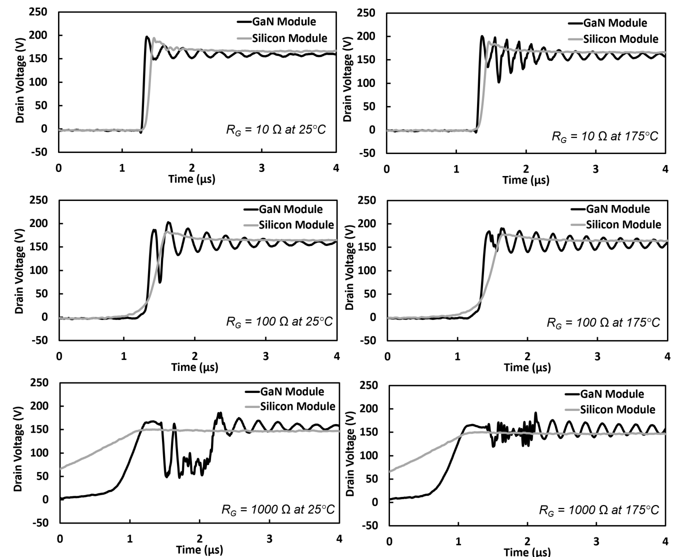


Fig. 25. The turn-OFF voltage transient of the GaN cascode module compared with a Silicon power MOSFET modules at 25°C and 175°C and selected gate resistances.

Reverse Conduction: In order to evaluate the 3rd quadrant performance of the cascode devices, the dynamic reverse conduction of their body diode is also tested. Fig. Fig. 26 shows the peak and duration of the reverse recovery current of the two cascode devices in comparison with a standalone SiC MOSFET and a Silicon superjunction MOSFET. the driving MOSFET is a low voltage device (rated at ∼20-30 volts), it has very little reverse stored charge. The HEMT and JFET

also do not contribute to recovery charge, hence the reverse recovery current in cascodes is negligible, making them ideal for where reverse conduction is necessary. Fig. 27 shows the stored recovery charge which demonstrates that the little residual charge in cascodes is temperature-invariant while the charge in stored in the standalone devices significantly rises with temperature.

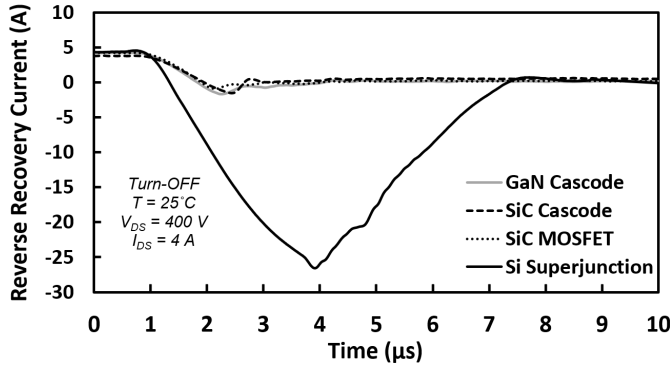


Fig. 26. The reverse recovery current of the both GaN and SiC cascode devices in comparison with standalone SiC power MOSFET and Silicon superjunction MOSFET shows negligible recovery peak and duration.

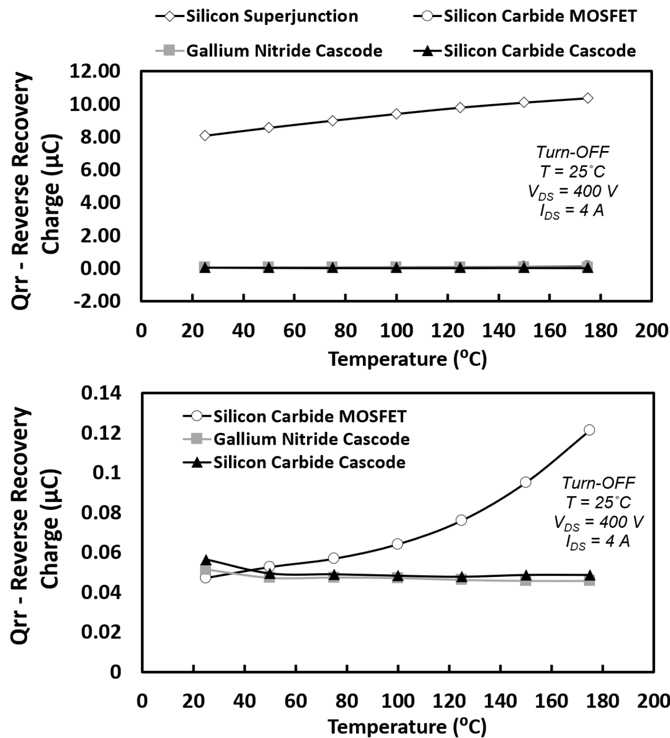


Fig. 27. The reverse recovery charge of the GaN and SiC cascode devices is not temperature variant unlike the standalone power MOSFETs.

V. Evaluation of Spontaneous Switchings

The high switching rate advantage in SiC and GaN cascodes may have unwanted side-effects. One of the potential consequences is spontaneous gate voltage spikes and unwanted turn-ON of the transistor. This is explained in literature as crosstalk with positive gate voltages, where a voltage on the gate is induced on the non-switching transistor in a half-bridge phase-leg structure of two transistors. This can lead to semi-short-circuits with large instantaneous current peaks which can lead to high temperatures and failures if repeated at high switching frequencies. A key parameter in impacting the severity and likelihood of spontaneous switchings is the threshold voltage of the devices. The threshold voltage of GaN HEMTs is typically lower than that of the Silicon and SiC power MOSFETs. This makes the GaN devices more suspectable to unwanted switchings. To understand the possibility of spontaneous switchings in these devices, it is necessary to measure the threshold voltage against temperature. As seen in Fig. 28, the threshold voltage of GaN cascode is lower than that of the SiC cascode by about 2.5 V in both cases of 650 volt devices, and the top of the voltage class range devices, further reducing in both case with temperature. This indicates that even in cascode configuration, the likelihood of unwanted switching in GaN is higher than SiC. Fig. 29 indicates the result of measurements of threshold voltage shift with temperature in GaN and Silicon Modules, where it can be seen that the threshold voltage of the GaN cascode module is also lower than that of the Silicon module by about 2 volts, making it prone to crosstalk. The GaN and SiC cascodes not only suffer from the crosstalk with positive gate voltages, but in fact the negative voltage induced on the gate can impact the switching even more severely, especially where the device is switching a negative current with high *dI/dt* into the source inductance of the packaging.

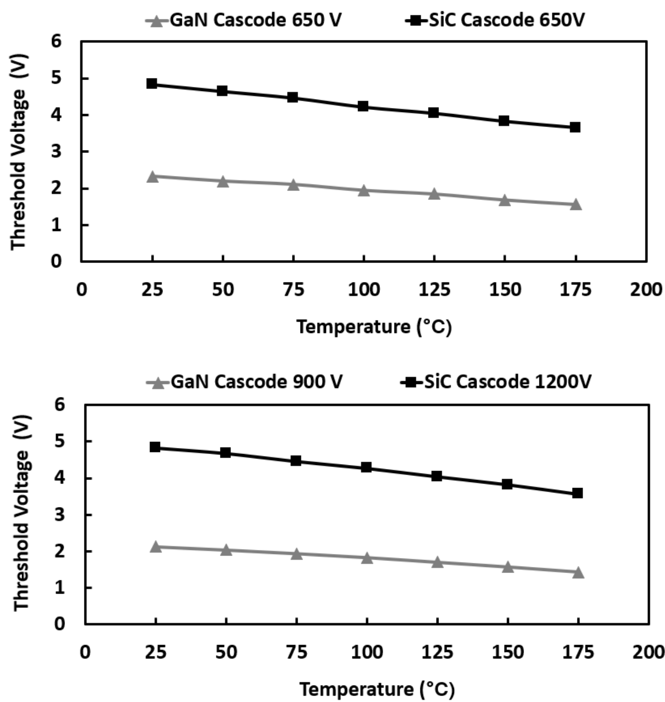


Fig. 28. Threshold voltage of the devices under test against temperature, indicating that the threshold voltage of GaN cascode is significantly lower than that of the SiC devices, making more susceptible to unwanted turn-on (crosstalk-induced switchings), further reducing with increasing of the temperature.

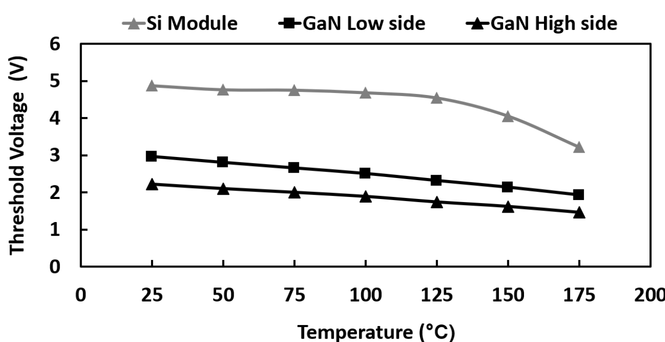


Fig. 29. Threshold voltage of the two GaN cascode devices in the half-bridge phase leg configuration against temperature, compared with that of the similarly rated Silicon power MOSFET. The threshold voltage of high-side device is slightly higher than the low-side device.

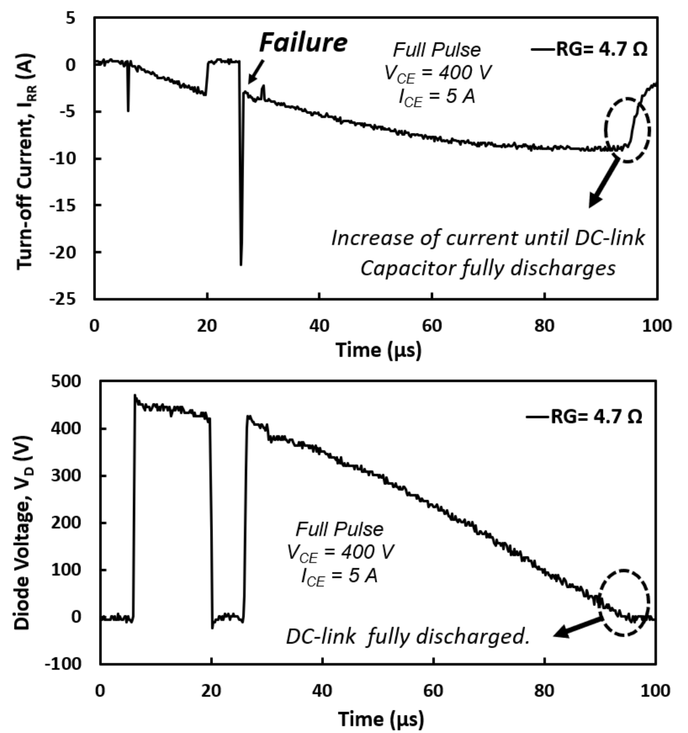


Fig. 30. The short-circuit failure of the gate by the voltage induced by *dI/dt* on source inductance, which discharges the DC link capacitors.

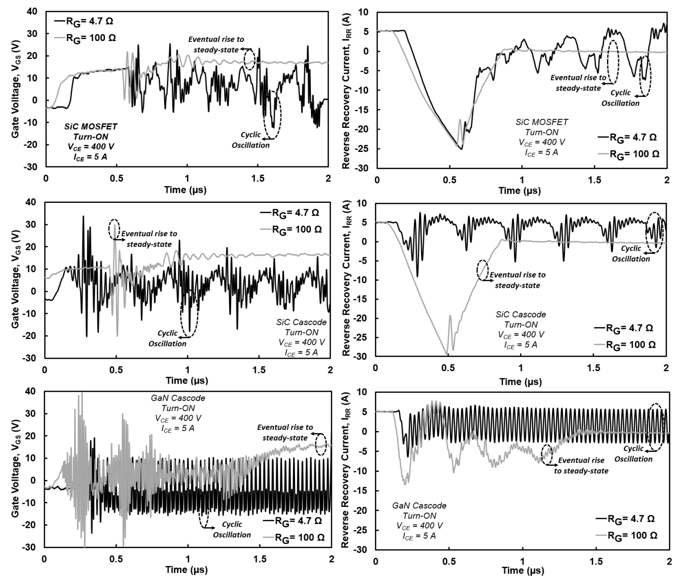


Fig. 31. The gate voltage and turn-off current measured in the drain-source of the switching transistor indicates that the spontaneous turn-on and turn-off cycles are more severe in GaN cascode, followed by the SiC cascode while standalone SiC MOSFET is unaffected.

To emulate this phenomenon and understand its characteristics, a range of experiments is arranged. A snappy diode with high current switching *dI/dt* is implemented as the free-wheeling diode in the same double-pulse test board. Measurements are performed in different switching rates adjusted by the gate resistances. It is seen that with a low

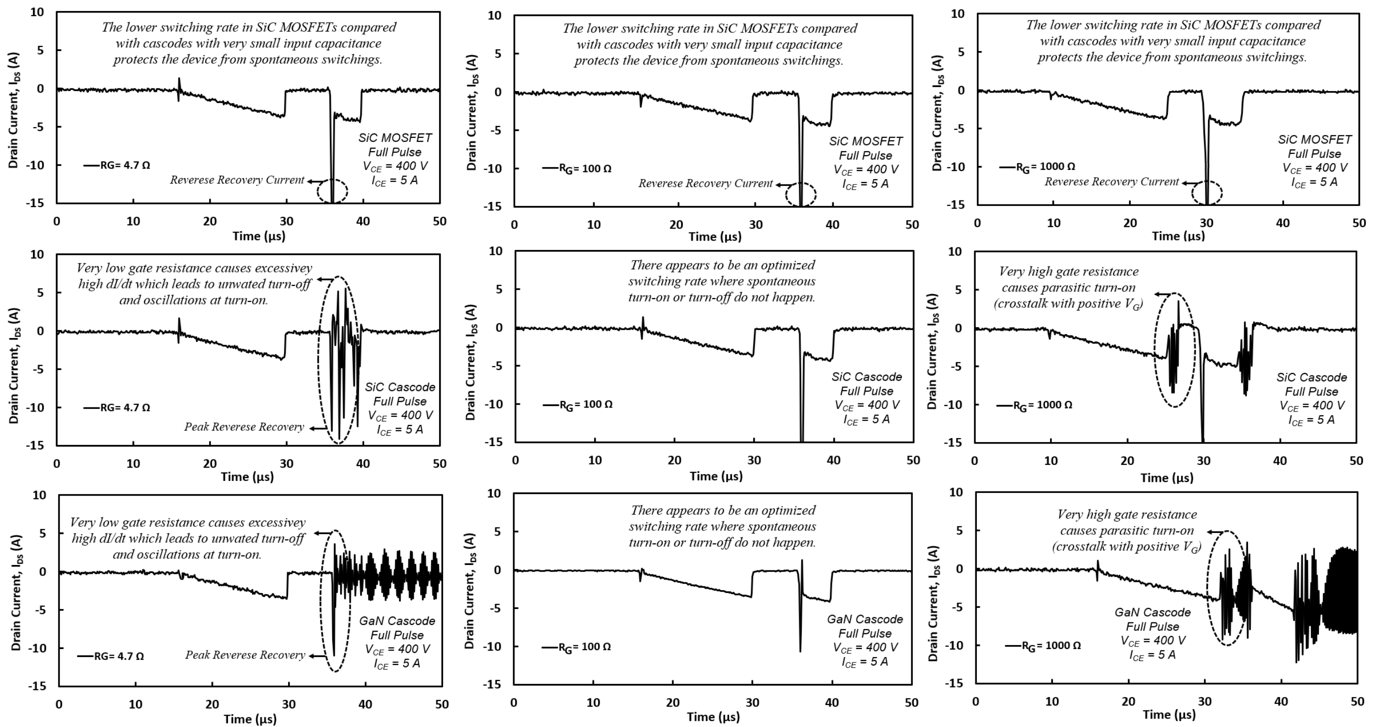


Fig. 32. Measurements on a wide-range of switching rates demonstrates that at very low gate resistances the spontaneous turn-off mechanism dominates the transients while at very high gate resistances, the induced positive gate voltage turns-on the device. Therefore, there is an optimum gate resistance to switch the SiC and GaN cascodes.

gate resistance, the very high *dI/dt* results in high negative voltage peaks induced on the gate of the cascodes. This is induced on the gate through the source inductance of the package leads. This results in spontaneous turn-OFF of the transistor simultaneously to when the gate driver is increasing the gate voltage to turn-ON the transistor. The induced gate voltage reduces the effective voltage on the transistor's gate and turning it off. As the transistor switches off, the induced gate voltage disappears as the *dI/dt* is removed while the gate driver's positive voltage is still applied on the gate. This once again increased the gate voltage and turns-on the transistor, which would trigger high *dI/dt*, a negative induced voltage on the gate, and follow-up turn-OFF. The transistor enters an oscillatory cycle of turn-ON and OFF transients which clearly would have a thermal impact. This, can lead to failure as shown in Fig. 30, especially at low gate resistances which result in higher *dI/dt*. The failure has resulted in a short-circuit into the transistor and current rises until the DC-link capacitors are fully discharged. Increasing the gate resistance to decrease the *dI/dt* could be a remedy to avoid this, however, one should note that the advantages gained by upgrading to wide-bandgap unipolar devices could be lost by this approach. Measurements on induced gate voltage of the cascodes is presented in Fig. 33 when the gate of the low side device is connected to R_G of 10 Ω, 100 Ω and 680 Ω while the high-side device is switched with R_G of 22 Ω and 100 Ω. It can be seen that the induced voltage is well above the threshold voltage in all cases, increasing in peak and duration with increase of the connected R_G on the low-side device, able to lead to unwanted turn-on. It can also be seen that the induced gate voltage is higher in the case of the GaN device with prolonged duration, which coupled with the fact the threshold voltage of GaN cascode is lower than that of the SiC device as indicated in Fig. 28, will lead to significantly higher likelihood of spontaneous switching. To reduce the likelihood of crosstalk, several techniques may be used, as discussed in [31]. These include a second gate-resistance path for gate current sink, a gate-source capacitance to absorb the induced gate current and prevent its flow in the gate resistance path, a decoupling capacitor to reduce the impact of *dV/dt* on voltage overshoot, and application of a bipolar gate driver with negative gate voltage offset to counter the crosstalk-induced gate voltage.

The aforementioned cyclic switchings are shown in Fig. 31 for the SiC and GaN cascodes alongside SiC MOSFET device. It can be seen that the unwanted turn-ON and OFF transients are less pronounced in the SiC MOSFET (as it has the largest input capacitance and internal gate resistance), followed by the SiC cascode device while the cycling switching is most severe in the GaN cascode. This is due to the fact that in two cascode transistors, the driving Silicon MOSFET is only rated at about 20 volts with very small parasitics components. This, coupled with the switching rate capabilities of the normally-ON HEMTs (due to lateral two-dimensional electron gas layer with very small parasitic capacitances) leads to very high *dI/dt* which triggers the cyclic switchings. Fig. 32 shows the current measured in the drain-source of the transistor for R_G of 4.7 Ω, 100 Ω and 1000 Ω. It can be seen that in SiC MOSFET, no unwanted switching takes place, whether turn-ON or turn-OFF. On the contrary, in both SiC and

GaN cascodes, at 4.7 Ω the devices spontaneously turn-OFF while at 1000 Ω unwanted turn-ON initiates. This is while the switching in both cases at gate resistance of 100 Ω is damped with no traces of oscillations. Although the values indicated here are not commonly used in practical applications, but demonstrate that there is an optimum switching gate resistance where unwanted positive or negative crosstalk could be avoided. The exact values for this should be determined in each specific application and device depending on the required *dI/dt*, stray inductance of the package, the internal gate resistance of the device and gate driver's current supply to charge the capacitors.

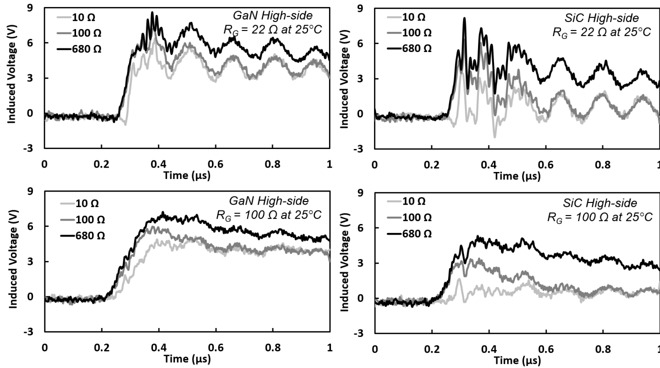


Fig. 33. Induced gate voltage on the gate of the low side device connected to R_G of 10 Ω, 100 Ω and 680 Ω when switching the high side device with R_G of 22 Ω and 100 Ω. It can be seen that the induced voltage is well above the threshold voltage in all cases, increasing in peak and duration with increase of connected R_G on the low-side device, able to lead to unwanted turn-ON.

VI. Evaluation of UIS Ruggedness

The performance of the power devices under unclamped inductive switching (UIS) is also a key indicator for the electrothermal ruggedness of the device. The widely used test methodology of unclamped inductive switching measurements is described in [32] with removal of the anti-parallel diode as demonstrated in Fig. 34. During this test, the gate voltage is switched ON, thereby charging the inductor. When the gate voltage is turned OFF, the inductor continues to drive current through the device until the inductor is discharged. Therefore, the power device is subjected to simultaneously high voltage and currents thereby causing significant instantaneous power dissipation and high junction temperature surges. This can lead to failure if the junction temperature exceeds the rated junction temperature of the device. Since failure usually occurs from hot-spots on the device resulting from temperature non-uniformities, the predicted failure point assuming uniform junction temperature is always higher than the actual failure point. In power MOSFETs, the failure mode occurs through parasitic BJT latch-up (for high power density avalanche pulses) or packaging failure (for high energy avalanche pulses) [33]. The avalanche ruggedness of power devices reduces with increased ambient temperature due to the negative temperature coefficient of the parasitic BJT base-emitter latching voltage i.e. the parasitic BJT becomes easier to trigger at higher temperatures due to an increase in thermally generated carriers [34]. The physics of failure of SiC MOSFETs under avalanche has been well studied [34]–[39]. However, the failure mechanisms in the GaN HEMTs and SiC JFETs cascodes differ and must be analysed separately.

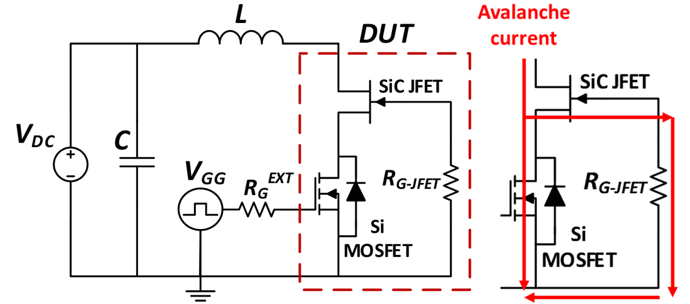


Fig. 34. SiC Cascode JFET in UIS test circuit and current path in UIS.

To analyse this, measurements are performed with an initial voltage of 50 V with a 1 mH inductor at ambient temperature. The avalanche characteristics of the SiC Cascode JFET resemble those of conventional MOSFET devices as can be seen in Fig. 35 where the V_{DS} voltage rises to the intrinsic breakdown voltage while the avalanche current falls at a rate determined by the inductor. Fig. 35 shows that the SiC cascode has been able to withstand the UIS pulse up to 20 A peak avalanche current with a gate pulse width of 25 μs (corresponding to an avalanche current of 20 A) while the voltage is raised to 800 volts. By increasing the gate pulse width just slightly further the device fails with the UIS current reaching 21 A. In SiC FETs, the avalanche currents are conducted by impact ionization through the semiconductor, hence failure can result either from the latching of parasitic components within the device or from the junction temperature exceeding its safe-operating-area by the excessive heat. Because SiC cascode JFETs comprise of a low voltage MOSFET and a HV SiC JFET (with an internal resistance between the JFET gate and MOSFET source: R_{GJFET}) as shown in Fig. 35, the failure mechanism under UIS merits special consideration.

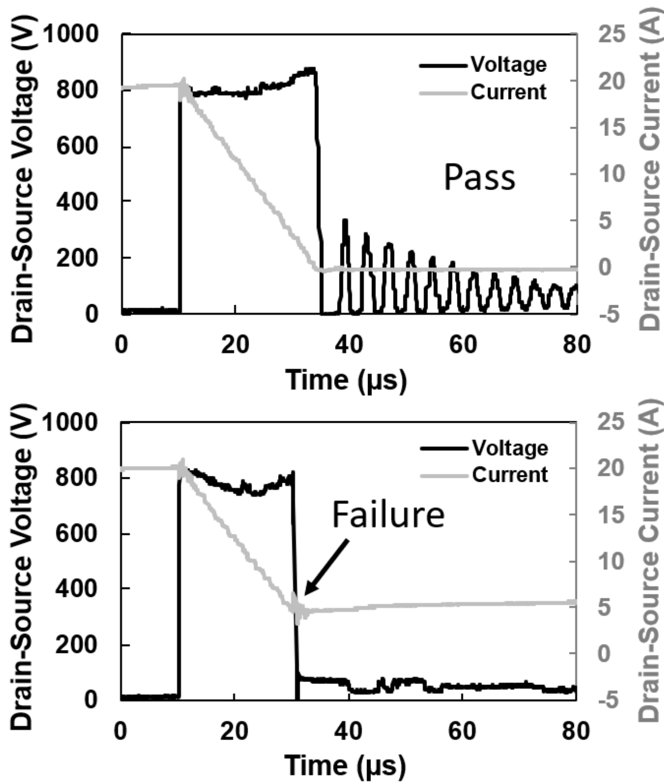


Fig. 35. The failure margin of the tested SiC cascode is at 21 A.

During UIS, due to the lack of an insulated gate in JFETs, a fraction of the avalanche current flows through the reverse biased JFET gate as shown in Fig. 34. This current flows through R_{GJFET}, potentially causing a voltage drop high enough to turn the JFET ON during avalanche. Hence, the V_{DS} voltage across the SiC cascode JFET drops during avalanche. Failure of the device under UIS can result either from JFET exceeding its rated temperature limits or from damage to $R_{G\text{-}JFET}$ during high current and high temperature avalanche pulses.

On the other hand, the primary failure mechanism in GaN HEMTs is due to the instantaneous increase of the electric field by the voltage rise across the lateral drain-source region, immediately below the gate which leads to significant charge trapping at the gate through impact ionisation [40], [41]. Once impact ionisation is complete, the electrons are absorbed by the drain while there is a significant hole trapping under the gate region. This increases the gate leakage current, which if repeated, will eventually lead to breakdown. This degradation mechanism is less pronounced in enhancement-mode HEMTs as the P-type doping on the gate reduced the density of the holes underneath the gate region while the depletion-mode HEMTs used in the cascode structure are more susceptible to this failure mode. The rapid failure of the HEMT is the underlying reason on why GaN cascodes virtually demonstrate no avalanche ratings [42]. Furthermore, the thermal conductivity of GaN is significantly lower than that of the Silicon and SiC, hence, the rate of heat generation can easily exceed the rate of heat dissipation in GaN HEMTs under UIS. The lateral channel architecture of GaN HEMTs, opposed to the vertical channel architecture in SiC MOSFETs and JFETs, also restricts the rate of heat dissipation since the bulk of the semiconductor is not used for electron flow. As a result, GaN devices typically have significantly higher junction to case thermal resistances compared with the Silicon and SiC devices. To evaluate this in these measurements, the duration of the gate voltage pulse and the size of the inductor are incrementally increased to determine the peak UIS current and its duration, so the pulse is gradually increased until failure occurs.

Fig. 36 shows a peak UIS current of just below 1 A with only 2 μs, leading to a peak voltage of about 1300 V. However, a slight increase to the gate pulse width to increase the UIS current to about 1.5 A leads to failure of the device with a peak voltage of 1600 V as in Fig. 37. This clearly demonstrate that the SiC cascode is significantly more UIS rugged than the GaN cascode, which demonstrates almost no UIS ruggedness. This trend can be seen more clearly in Fig. 38 where the three steps of increasing the gate pulse width has led to approximate drain-source currents of 0.5 A, 1 A and 1.5 A, where the latter is where the failure eventually takes place.

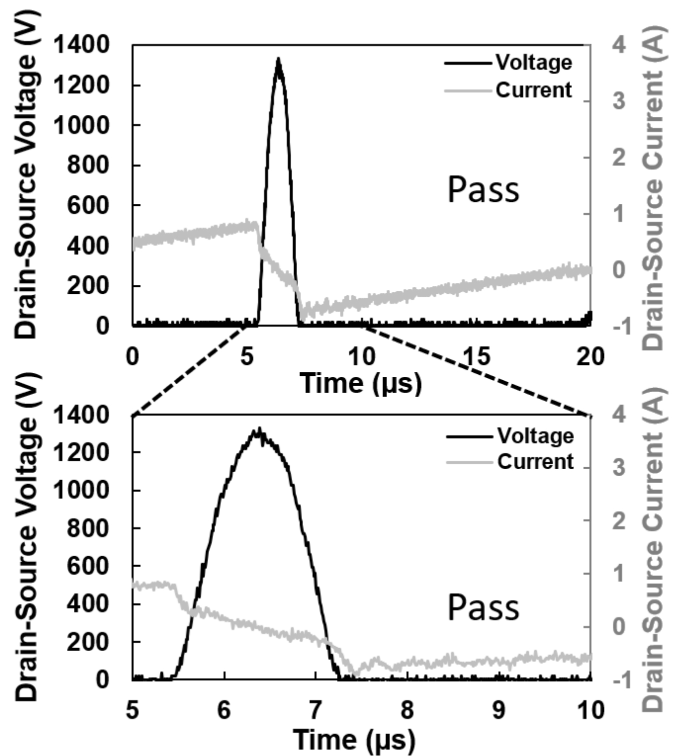


Fig. 36. The GaN cascode survives UIS of 1 A at 2 μs with a peak voltage of 1300 V.

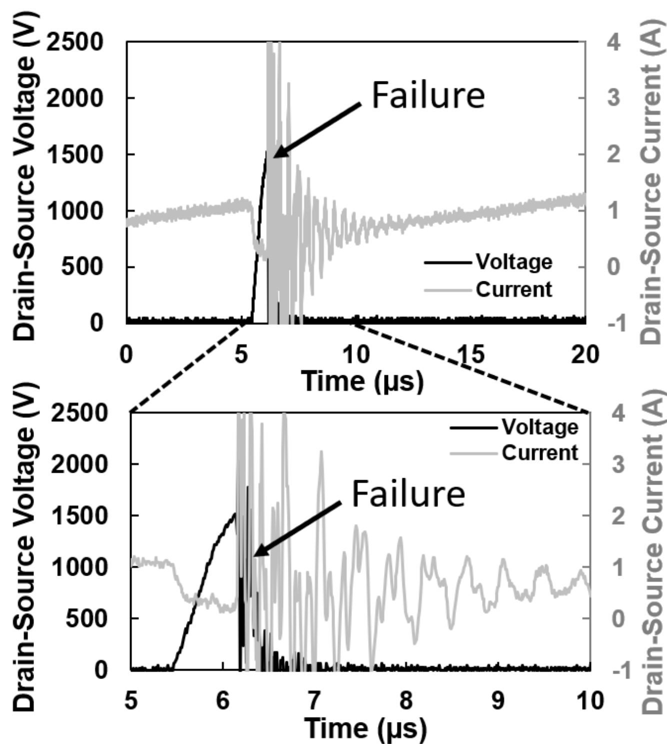


Fig. 37. . Further increase of the UIS current to 1.5 A leads to failure with the peak voltage rising to up to 1600 V.

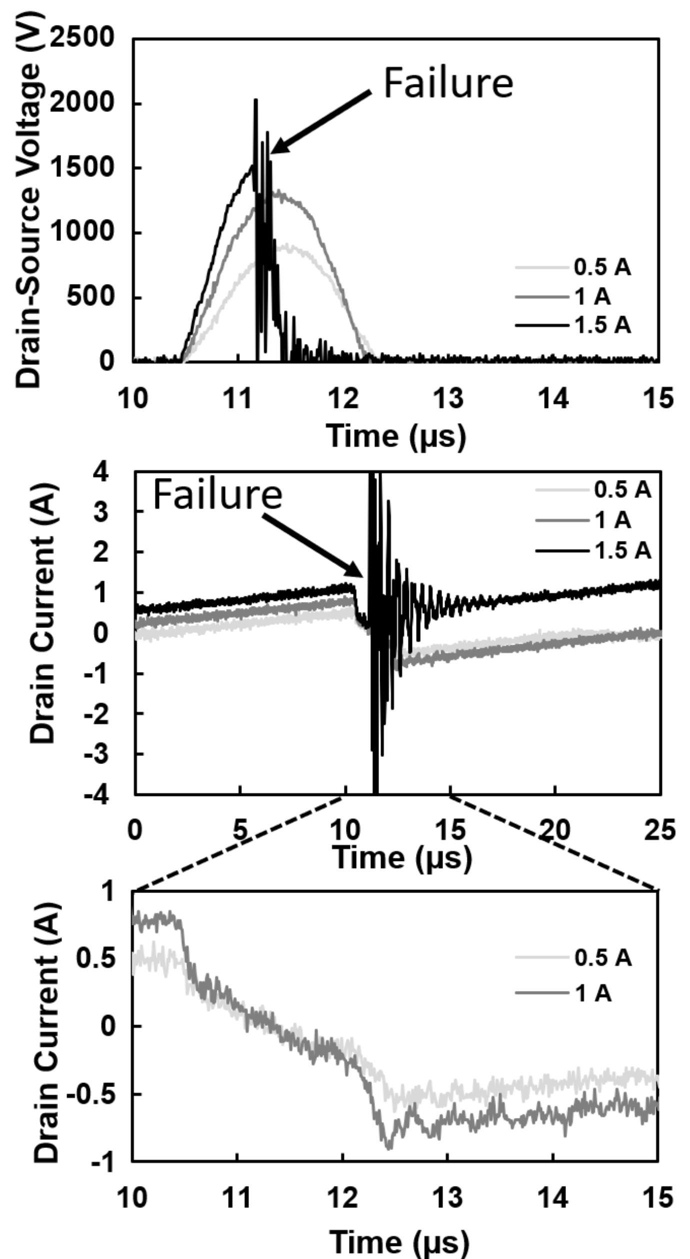


Fig. 38. The three stage of increasing the current, where the GaN cascode is seen to fail at just 1.5 A UIS current while it has survived up to 1300 volts with 1 A current earlier.

VII. Conclusion

This paper has provided the first systematic evaluation of SiC and GaN cascodes in terms of the static, dynamic, spontaneous switchings and unclamped switching performance. It is shown here that the static on-state performance of GaN cascode is worse than SiC cascode while the GaN device has a higher temperature coefficient in terms of its specific ON-state resistance. It is shown that the GaN cascode typically exhibits significantly faster switching rates with higher switching rate sensitivity to the change of gate resistance, while the SiC cascodes exhibit slower but more steady performance. This can be accounted by the larger parasitic capacitances in SiC JFET compared with the GaN

HEMT. It is also shown here that both cascode devices have excellent 3rd quadrant performance thanks to the small reverse recovery charge of the switching low voltage MOSFET, when compared with closely-rated Silicon and SiC power MOSFETs. The ruggedness of the cascode devices is also tested by means of UIS test to establish the electro-thermal ruggedness of device under stress. It is seen that the SiC device can withstand substantial electrothermal stress while GaN cascodes have virtually no UIS rating due to the absence of effective extraction mechanisms for the trapped hole in their depletion mode HEMTs. The crosstalk-induced turn-on and the source-inductance-induced turn-off transients are also shown that can have destructive consequence, with a higher measured crosstalk-induced voltage on the gate of the GaN device due to the higher *dV/dt*, but can be avoided if the gate resistance is selected in a certain range which would avoid both phenomena from occurring.

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