IEEE Open Journal of the
Industrial Electronics Society

Received 2 December 2021; revised 1 January 2022; accepted 14 January 2022. Date of publication 19 January 2022;
date of current version 31 January 2022. The review of this paper was arranged by Associate Editor Hong Li.

Digital Object Identifier 10.1109/OJIES.2022.3143946

Impact of Carriers Injection Level on Transients of Discrete and Paralleled Silicon and 4H-SiC NPN BJTs

CHENGJUN SHEN [1] (Student Member, IEEE), SAEED JAHDI [1] (Senior Member, IEEE), JUEFEI YANG [1] (Graduate Student Member, IEEE), OLAYIWOLA ALATISE [2] (Senior Member, IEEE), JOSE ORTIZ-GONZALEZ [2] (Member, IEEE), RUIZHU WU [2] (Member, IEEE), AND PHIL MELLOR [1] (Member, IEEE)

[1]Department of Electrical Engineering, University of Bristol, BS8 1UB Bristol, U.K.
[2]Department of Electrical Engineering, University of Warwick, CV4 7AL Coventry, U.K.

CORRESPONDING AUTHOR: CHENGJUN SHEN (e-mail: yf19300@bristol.ac.uk)

This work was supported in part by the UK EPSRC Supergen Energy Networks Hub under Grant EP/S00078X/2 and in part by the UK Royal Society Research Grant RGS\R2\202193.

ABSTRACT The 4H-SiC vertical NPN BJTs are attractive power devices with potentials to be used as high power switching devices with high voltage ratings in range of 1.7 kV and high operating temperatures. In this paper, the advantages of the 4H-SiC NPN BJTs in terms of switching transients and current gain over their silicon counterparts is illustrated by means of extensive experimental measurements and modelling, including investigation of high level injection, as a common phenomenon in bipolar devices that influences the switching rates and DC current gain. The two device types have been tested at 800 V with maximum temperature of 175 °C and maximum collector current of 8 A. The turn-ON and turn-OFF transition in Silicon BJT is seen to be much slower than that of the SiC BJT while the transient duration will increase with increasing temperature and decreases with larger collector currents. The common-emitter current gain of SiC BJT is also found to be much higher than silicon counterparts, increasing with temperature in low injection levels but decreasing in higher injection levels in both devices. The rate of increase of current gain slows down toward stability as the collector current increases, known as the high-level injection. Current sharing imbalance among parallel connected devices is also investigated, which are shown to be evidently dependant on temperature and base resistance in Silicon BJT, while the current collapse in also seen in SiC BJT at high injection levels with high base resistance. The turn-OFF delay is seen to be temperature dependant in single and paralleled Silicon BJTs while almost non-existent in SiC device.

INDEX TERMS Bipolar junction transistor, DC gain, high level injection, silicon carbide, temperature.

NOMENCLATURE

D_n	Electrons Diffusion Constant (cm^2/s).
D_p	Hole Diffusion Constant (cm^2/s).
D_{nB}	Electrons Diffusion Constant in Base (cm^2/s).
J_W	Webster Current Density (A/cm^2).
J_C	Collector Current Density (A/cm^2).
J_B	Base Current Density (A/cm^2).
J_{BR}	Reverse Base Current Density (A/cm^2).
J_{SCR}	Recom. Cur. at Space-Charge Reg. (A/cm^2).
J_n	Electron Current Density (A/cm^2).
J_p	Hole Current Density (A/cm^2).
L_n	Diffusion Length (μm).
L_{s2}, L_{c2}	Inductance Between Paralleled Devices (nH).
L_{s1}, L_{Stray}	Parasitic Inductance on PCB Board (nH).
N_B	Doping Concentr. of Base Region (cm^{-3}).
N_D	Doping Concentr. of Drift Region (cm^{-3}).
n_i	Intrinsic Carrier Concentration (cm^{-3}).
n	Electron Concentration (cm^{-3}).
p	Hole Concentration (cm^{-3}).
Q_{SC}	Drift Region Minority Charge (As).

Q_{nB}	Base Region Minority Charge (As).
R_{Base}	Base Resistance (Ω).
R_2	Resistance Between Paralleled Devices (Ω).
$t_{transient}$	Turn-on Base Charge Time (s).
t_{I-on}	Turn-on Current Rise Time (s).
t_{V-on}	Turn-on Voltage Fall Time (s).
t_S	Turn-off Delay Time (s).
t_{V-off}	Turn-off Voltage Rise Time (s).
t_{I-off}	Turn-off Current Fall Time (s).
t_Q	Pulse Width Period (s).
V_{GL}	Steady-State Drive Voltage (V).
V_D	Schottky Diode Voltage Drop (V).
V_{BE}	Base-Emitter Junction Voltage (V).
$V_{BE,Sat}$	Base-Emitter Junction Saturation Voltage (V).
W_B	Thickness of Base Region (μm).
W_D	Thickness of Drift Region (μm.
W_{NM}	Conductivity-Modulated Width (cm).
W_S	Charge Storage Region Width (μm).
W_E	Half of the Emitter Finger Width (μm).
X_V	Base Region Turned-Off Length (μm).
α	Common-Base Current Gain (-).
β	Common-Emitter DC Current Gain (-).
γ_E	Emitter Injection Efficiency (-).
ϵ	Relative Permittivity (F/m).
μ_n	Electron Mobility (m^2/Vs).
μ_p	Hole Mobility (m^2/Vs).
τ_n	Electron Lifetime (s).
τ_p	Hole Lifetime (s).
τ_{tot}	Total Carrier lifetime (s).
τ_{SRH}	Shockley-Read-Hall lifetime (s).
τ_A	Auger lifetime (s).
k	Boltzmann Constant (J/K).
T	Temperature ($^\circ C$).

I. INTRODUCTION

Silicon bipolar junction transistors (BJTs) have been in use for over half of a century. The low DC gain (β) in vertical Silicon BJTs makes them a not promising choice for applications in power electronics because complicated base drivers are needed for the high continuous base current. However, this is set to change with emergence of the 4H-SiC BJTs which enable a significantly higher DC current gain (β) [1]. 4H-SiC BJTs have the potential to displace gated transistors, i.e. MOSFETs and IGBTs, in some specific applications [2] due to advantages such as low on-state resistance at high currents due to the conductivity modulation and the absence of the gate channel, especially when compared with SiC MOSFETs, as the gate oxide imposes ruggedness instabilities at high temperatures [3]–[5]. Furthermore, SiC BJTs have higher transconductance when compared with SiC JFETs [3] although with lower current rating which is mainly due to the low carrier lifetime in SiC which impedes adequate conductivity modulation in the drift region in the on-state. The low carrier lifetime is mainly caused by the high electrically active defect density. Of those lifetime killing defects that have been observed in 4H-SiC, Z1/2 (EC-0.65 eV) is the main intrinsic defect while EH6/7 (EC-1.55 eV) represents the main extrinsic deep defect [6]. The reduced carrier diffusion lengths of dopants, as a result of the low lifetimes, is also a challenge in ion implantation of SiC substrates. P-N junctions in SiC also imposes a minimum forward voltage of 3 V. Therefore, further increase in carrier lifetime is still desirable.

Silicon BJTs have a positive temperature coefficient (PTC) with higher current gain, especially due to the increase of the carrier lifetime with temperature [7]. Paralleling them is challenging though as with increase of the current in the transistor its temperature rises which leads to lower impedance and higher current, causing a thermal breakdown. On the other hand, attaining a negative temperature coefficient (NTC) is feasible at high currents for SiC BJTs, due to the incomplete ionization of Aluminum dopants in the base area at room temperature and increase of the hole concentration of the base at elevated temperatures. Thanks to the lower carrier lifetime, lower carrier mobility and much smaller width of the base and drift region, SiC BJT is predicted to have faster-switching transients [4]. The DC Current gain in common emitter (CE) configuration for NPN BJTs, i.e. $\beta = I_C/I_B$, is also an important parameter which decides the loss of the transistor and the structure of the base driver [8]. The higher gain in SiC is mainly due to the smaller dimensions of the base and the drift region, achieved by the higher critical electrical field. The smaller device size also reduces the parasitic capacitance for less output oscillations.

At the low doped base region, the injected electron concentration is much higher than the base doping concentration when the high-density current is injected from the collector side. This is referred to as the high-level injection (HLI) in the base area with a large concentration of both electrons and holes. This significantly reduces the base resistance to allow a larger on-state current density and a lower on-state voltage drop. However, it is reported [9], [10] that the DC current gain is reduced under the same circumstance resulting in a low efficiency of the base driver.

For both the DC gain and the dynamic transition, the variation of temperature and collector current play an important role. The dynamic switching transition can be divided into the turn-ON and turn-OFF transitions determined by the temperature-dependent diffusion coefficient and carrier lifetime, which are also affected by the current level. In terms of the DC current gain, the hole concentration by the partial ionisation and surface recombination are temperature dependent and the current gain is determined by the recombination in the emitter-base junction.

SiC BJTs are already demonstrated in applications such as the 200 A and 50-kW DC power converter in [11], which was integrated by 4H-SiC BJTs, delivering very high efficiency for application in electric vehicles. It is demonstrated in [11] that each SiC BJT has a current density of over twice that of silicon IGBTs together with a larger current handling capability than that of SiC MOSFET [12]. High-voltage ($\geq$800 V) BJTs are

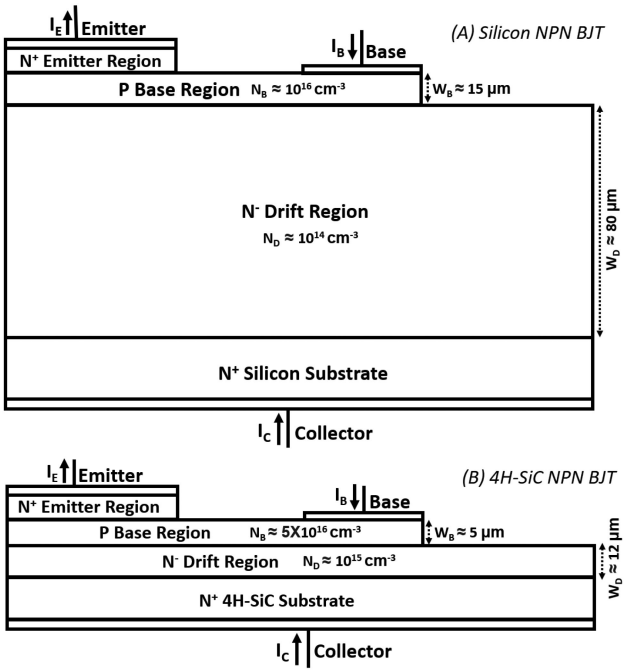

FIGURE 1. Cross-sectional of (a) Silicon and (b) 4H-SiC power NPN BJTs.

also still in demand as deflection transistors in specific electronic screens [13]. In absence of a need for reverse conduction, as the case of boost converters, SiC BJTs are also shown to have an outstanding conduction efficiency when compared with unipolar devices [14].

Novel structures of base drivers are recently proposed [15] and installed on DC/DC step-up converters fabricated by SiC BJTs, minimising the base current and hence the power loss. The theoretical capabilities of multi-kilovolt 4H-SiC BJTs, such as the small on-state and switching losses have made it a potential candidate for high voltage converters [16].

This paper demonstrates the performances of 4H-SiC BJTs compared with the silicon BJTs, with analysis of switching transients and current gain in a wide range of temperatures (25 °C to 175 °C) and collector current (1 A to 8 A). The aim of this paper is to investigate the impact of the high-level injection (HLI) on the transient slew rates and current gain of Silicon and SiC BJTs when collector-emitter current of the BJTs rise, and to analyse the current-sharing among parallel-connected Silicon and SiC BJTs to increase the overall current handling capability. Section II presents the theoretical models required to understand the switching transients and current gain of power BJTs while the experimental set-ups are shown in Section III. Section IV compares the measurement results compared with simulations while Section V concludes the paper.

II. MODELLING ANALYSIS

For both the Silicon and SiC BJT, the doping concentration of the base and drift region is much smaller than other regions, as in Fig. 1, in order to improve the emitter's injection efficiency.

Carrier mobility for holes (μ_p) and electrons (μ_n) in Silicon reduces with temperature [9], as (1):

$$\mu_n(Si) = 1360\left(\frac{T}{300}\right)^{-2.42} \tag{1}$$

$$\mu_p(Si) = 495\left(\frac{T}{300}\right)^{-2.20} \tag{2}$$

And for SiC this is as in (3):

$$\mu_n(SiC) = 1140\left(\frac{T}{300}\right)^{-2.70} \tag{3}$$

$$\mu_p(SiC) = 120\left(\frac{T}{300}\right)^{-3.4} \tag{4}$$

While temperature dependence for the diffusion coefficient can be derived by Einstein's equation [9] as (5):

$$D = \frac{kT}{q}\mu \tag{5}$$

Diffusion coefficient (D) has strong inverse temperature dependence because the temperature dependence of the of mobility is dominant, which can be determined as [9] as (6):

$$D_n(Si) \propto \frac{1}{T^{1.42}} \quad D_n(SiC) \propto \frac{1}{T^{1.70}} \tag{6}$$

$$D_p(Si) \propto \frac{1}{T^{1.20}} \quad D_p(SiC) \propto \frac{1}{T^{2.40}} \tag{7}$$

Due to the incomplete ionization of the SiC, the effective doping concentration of the SiC BJT will increase with temperature. It leads to additional ionized impurity scattering of free carriers resulting in further decrease of the mobility and hence the diffusion coefficient. The minority carrier lifetime under the same temperature range can be expressed in (8) as [17]–[19]:

$$\tau_n(Si) \propto T^{2.20} \quad \tau_n(SiC) \propto T^{1.72} \tag{8}$$

$$\tau_p(Si) \propto T^{2.80} \quad \tau_p(SiC) \propto T^{2} \tag{9}$$

Since the carrier lifetime is the reciprocal of the recombination rate, the carrier lifetime of 4H-SiC is about two orders of magnitude smaller than silicon, leading to a weak temperature dependence and faster switching transition. The HLI phenomenon will be more evident in the intermediate base area which is low-doped based on device band diagrams [20]. At large currents, the injected minority carrier exceeds the doping concentration of base region causing the surge of both carriers with respect to the charge neutrality n = p, the mobility of both carriers decreases because of the amplified mutual Coulombic interaction [9]. Assuming that the concentration of electrons is equal to the concentration of holes, the current dependence can be analyzed by the Caughey-Thomas formula [9] in (10) as:

$$\mu_n(Si)\ \&\ D_n(Si) \propto n^{0.91} \tag{10}$$

$$\mu_p(Si)\ \&\ D_p(Si) \propto n^{0.76} \tag{11}$$

$$\mu_n(SiC)\ \&\ D_n(SiC) \propto n^{0.61} \tag{12}$$

$$\mu_p(SiC)\ \&\ D_p(SiC) \propto n^{0.65} \tag{13}$$

And the current dependence of diffusion coefficient is the same. The total carrier lifetime τ_{tot} can be derived as (14) in [9]:

$$\frac{1}{\tau_{tot}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_A} \tag{14}$$

Where τ_{SRH} and τ_A are the carrier lifetime from the Shockley-Read-Hall recombination and Auger recombination process. The effect of τ_A is negligible at low collector current, therefore the total lifetime increases with rising collector current as determined purely by the τ_{SRH}. For the high injection level, the Auger lifetime plays a more important role which decreases with larger collector currents, leading to the decrease of total lifetime. In SiC, the decrease of Auger lifetime in HLI [4] and τ_{tot} will be smaller.

A. TURN-ON TRANSIENT

First, enough charge must be built up in the base and drift region to turn-ON the BJT as 'transient time,' given by [9]:

$$t_{transient} = \frac{W_B^2}{2D_n} \tag{15}$$

After the storage phase, enough minority carrier charge Q_{nB} promotes the current flow. The time can be derived as [9]:

$$t_{I-on} = \frac{W_B^2 J_C}{2D_n \beta J_B} = \frac{W_B^2}{2D_n} \tag{16}$$

Which describes the rise-time for the collector current. The D_n reduces with increasing temperature, leading to the increase in switching time, and further increased in higher collector currents. Afterward, the collector voltage drops to the steady-state level. This period is defined as the ratio of the stored minority carrier charge (Q_{sc}) to collector current as:

$$t_{V-on} = \frac{Q_{SC}}{J_C} = \frac{qW_B N_B + qW_D N_D}{J_C} \tag{17}$$

The voltage level in this phase is limited by the stored charge in the drift region, i.e. the depleted part of the drift region become smaller which lead to a smaller voltage level. Faster voltage transition is expected at high collector current. However, the smaller J_C is predicted in high temperatures because the diffusion coefficient decreases with temperature.

B. TURN-OFF TRANSIENT

At turn-OFF, a reverse base current is applied to extract the stored carrier from the base and drift regions. This time is known as the storage time or delay time and is defined by [21]:

$$t_S = \left(\frac{J_C}{J_{BR}}\right)\left(\frac{W_{NM}^2}{4D_n}\frac{J_C D_P}{J_C D_P + J_{BR} D_n} + \frac{W_B^2}{2D_n}\right) \tag{18}$$

This time is longer than the turn-ON transit time because the stored charge removal happens at both the base and drift regions. The first term can also be expressed as β so the whole expression will not be directly influenced by the base current and the collector current. For higher temperatures or collector currents, the diffusion coefficient will decrease leading to a slower depletion process. Nevertheless, the conductivity-modulated width W_{NM} decreases with increasing collector current [9] which is the dominant factor to reduce the delay time. The voltage turn-OFF time is given by [9]:

$$t_{V-off} = \frac{\sqrt{2\varepsilon q N_D V_C}}{2\dfrac{p(W_S)}{W_S} q D_p} \tag{19}$$

After the voltage rise phase, the collector current drops to off-state. This time is decided by the remaining carriers in the base after the voltage transients, and can be written as [9]:

$$t_{I-off} = \frac{W_E - X_V}{\dfrac{2W_E D_n}{\beta W_B^2} - \dfrac{D_n}{L_n}} \tag{20}$$

The temperature dependence of the diffusion length (L_n) is decided by the trade-off between D_n and τ_n. As a result, the diffusion length is almost temperature independent due to the opposite trends among D_n and τ_n. Nevertheless, the slower current drop is caused by the temperature dependent D_n. Under high current levels, the L_n is decreased because the τ_n and D_n have the same temperature dependence, leading to the increase in t_{I-off} as the decrease in D_n is more dominant.

C. DC CURRENT GAIN

When analysing the Collector-Emitter current gain model [22] in NPN BJTs, the following three factors must be considered: the recombination rate in the BJT; incomplete ionization in the SiC BJTs and Emitter injection efficiency while the Emitter injection efficiency always plays the most important role as α is proportional to the common emitter current gain:

$$\alpha \approx \gamma_E = \frac{\beta}{1+\beta} = \frac{J_n(0)}{J_n(0) + J_p(0) + J_{SCR}} \tag{21}$$

The recombination processes consist of the recombination in the emitter region, recombination in the space charge region (SCR), the surface recombination and the recombination in the base region. In this model, the electron diffusion current (I_{dn}) of the emitter current is assumed to be equal to the emitter current (I_E). At very low injection level, the current gain β is limited by the SCR recombination at the base-emitter junction determined by the forward-biased voltage at this junction. We have in (22) of [21]:

$$\alpha_T = 1 - \frac{W_B^2}{2L_n^2} \tag{22}$$

deriving the β_T as [21]:

$$\beta_T = \frac{2L_n^2}{W_B^2} \tag{23}$$

The recombination process in the SCR becomes significant at very low injection level where the current density of SCR

recombination is derived as [9], [22], [23]

$$J_{SCR} = \frac{qn_i W_D}{\tau} \cdot e^{\frac{qV_{BE}}{2kT}} \tag{24}$$

The doping concentration of SiC is larger than Silicon, and the much smaller W_B results in a much larger J_W for SiC BJT. In Silicon BJT, the lower diffusion coefficient leads to the fall of J_W at high temperatures, which results in the decrease of β in (23) with current which shifts to lower currents. When the temperature is increased, the carrier lifetime rises as shown in (8), and the emitter efficiency thus the current gain become larger. As the V_{BE} is increased, the diffusion currents exceed the recombination current and large amount of electrons start to inject into the base region, leading to increase of the emitter injection efficiency. Therefore, it is also expected to see a lower β with increasing temperature at HLI. Although the SiC BJT has a higher doping concentration, the DC current gain is always larger due to its much smaller width of the base region [23]. On the other hand, with the further increase of collector current, the injection of holes also begin in order to maintain the charge neutrality at the Base Emitter junction. The hole concentration becomes proportional to the injected electron concentration into the base region which this leads to the extra recombination in the emitter region and thus reduced injection efficiency. The significant incomplete ionization of the SiC [22], [23] leads to a much smaller effective hole density at base than the doping concentration but increases with temperature until the ionization of dopants complete. This leads to further temperature dependence of the current gain in SiC BJTs, Whereas in Silicon, the dopants are almost fully ionized at room temperature in the base region, and the density of holes can be assumed as constant at all temperatures, reducing the temperature dependence of the current gain in Silicon BJTs.

The current gain is known to decrease once the collector current density increases beyond the Webster current density J_w in (25) as HLI boundary [4], [9], [24] as:

$$J_W = \frac{qD_{nB}N_B}{W_B} \tag{25}$$

Despite the larger D_{nB} in Silicon, the Webster density for SiC is actually larger due to the higher doping concentration and much smaller dimensions of the SiC die. The onset of Webster effect can be experimentally seen when the increased collector current no longer correlates with an increase of the DC Gain (β), keeping the DC gain stable with collector current increase. This is called the onset of high-level injection. Further increased injection into the base region of the BJT will result into reduced DC gain, driving the device into HLI. High currents beyond the HLI rating of single devices must be distributed into paralleled devices.

D. PARALLELED BJTS

The key factors to consider when paralleling BJTs are [25]:

1) Differences in the device parameters.
2) Differences in position within the circuit layout.
3) Differences between the base drivers connected.

The charge stored or released from the base determines the switching performance of the BJTs. A suitable base driver generates current peaks to rapidly turn-ON/OFF the device while maintaining a low on-state base current to minimize the driver losses. Here, to eliminate the role of driver's mismatch the same base driver is used. The difference in the electrical parameters such as the DC current gain and the amount of stored charge may also cause the imbalance of output current. The circuit layout [25] also affects the switching performance of the paralleled devices, so the additional parasitic elements must be considered.

To turn-ON the transistor, a positive current spike is required to rapidly develop the stored charge in the base region and forward bias the base-emitter junction. After the BJTs are turned-ON, the base-emitter junction is forward biased whilst the injection of electrons from the base-emitter junction to the base-collector junction starts. The base current is reduced to the steady-state value. For the first of the two paralleled devices, this can be written as (26) in [26]:

$$I_{Base1,Steady} = \frac{V_{GL} - V_D - V_{BE,sat}}{R_{Base} + 0.6\Omega} \tag{26}$$

where V_{GL} is the drive voltage (5 V) at the steady state, V_D is the Schottky diode voltage drop (about 0.3 V), $V_{BE,sat}$ is the saturation voltage of the base-emitter junction (about 1.5 V for Silicon BJT and 3.45 V for SiC BJT at operating temperature of 25 °C) and 0.6Ω is added to consider the resistance of the components on the base driver. The steady base current for the 2nd device can also be written as (27):

$$I_{Base2,Steady} = \frac{V_{GL} - V_D - V_{BE,sat}}{R_{Base} + 0.6\Omega + R_{S2}} \tag{27}$$

The extra base resistance added to the second device decreases the base current and thus leads to some difference in the collector current which is proportional to the value of base current.

III. EXPERIMENTAL SET-UP

A wide range of experimental measurements and simulations are done to observe the effect of collector's high current injection and temperature on single and paralleled high voltage silicon and 4H-SiC power BJTs. These are mounted on a double-pulse test board with a specific base driver used for switching, with parameters specified in Tables 1 and 2 separately. A 1.2 kV SiC Schottky barrier diode and a 4 mH load inductor are also connected to the device under test. The base resistance of the driver is changed between 3.75 Ω and 11.75 Ω while temperature is increased from 25 °C to 175 °C in increments of 25 °C using ITC-100RL PID Temperature Controller. The devices are tested using a double-pulse test board with collector current controlled by the first charging pulse length (t_{Q1}) and increased linearly from 5 μs to 40 μs in steps of 5 μs while every 5 μs roughly equals to an increase of 1 A in collector current to maximum value of 8 A to remain within the safe operating areas of the devices. To increase

TABLE 1. The DPT Board Parameters

Parameter	Symbol	Value
C_{DC}	DC Capacitor	5 mF
C_{HF}	De-Coupling Capacitor	100 nF
L	Load Inductor	4 mH
V_{DC}	Test Voltage	800 V
I	Test Current	1-8 A
t_{Q1}	Charging Pulse Length	5-40 μs
t_{Q2}	Switching Pulse Length	8 μs
t_{Qnil}	Gap between Pulses	30 μs
T	Temperature Range	25-175°C
R_{Base}	Base Resistance Range	0-8 Ω
L_{Stray}	Estimated Parasitic Inductance	60 nH

TABLE 2. BJT Base Driver Parameters

Symbol	Parameter	Value
V_{CC}	Driver Input Supply Voltage	12 V
$I_{B,switch}$	Output Peak Base Current	4 A
$I_{B,on-state}$	Output On-state Base Current	0.35 A
t_{rise}	Output Base Voltage Rise Time	21 ns
t_{fall}	Output Base Voltage Fall Time	14 ns
C_B	Base Capacitor	10 nF
R_{B1}	Charging Resistor	1 kΩ
R_{B2}	Base Resistance	3.75 Ω

TABLE 3. Device Datasheet Parameters

	4H-SiC	Silicon
Model	GA04JT17-247	FJL6920
Manufacturer	GeneSiC	Fairchild/ON
Collector-Emitter Voltage (V)	1700	800
Collector Current (A)	15	20
Collector Current above 160°C (A)	5	20
Power Dissipation (W)	106	200
DC Current Gain - β (-)	100	8
J-C Thermal Resistance (°C/W)	1.41	0.625
B-E Saturation Voltage (V)	3.45	1.5

the overall current ratings, paralleling of the devices is also experimentally analysed.

The 8 A limitation is due to the lower current rating of SiC BJTs, especially at high temperatures as shown in Table 3. The extra turn-off delay of the Silicon BJT will lead to the higher output current than that of the SiC BJTs, while the rating current becomes lower in high temperatures, especially for the SiC BJT as shown in Table 3. High voltage bipolar devices in SiC remain challenging to fabricate unlike in Silicon where minority carrier lifetime can be engineered to yield optimal conductivity modulation.

The test board has a 5 mF DC link capacitor bank to stabilize the voltage V_{DC}. The power BJTs are the Fairchild silicon BJT and GeneSiC 4H-SiC BJT, while the high-side freewheeling diode is a CREE SiC Schottky diode. The voltage applied to both the silicon and SiC BJT is 800 volts.

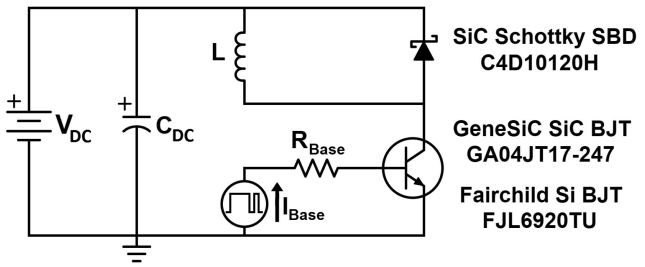

FIGURE 2. Circuit diagram of double-pulse board for single device tests [4].

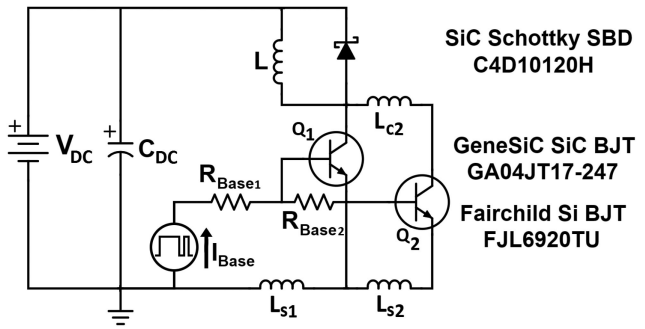

FIGURE 3. Circuit diagram of the double-pulse board for paralleled devices tests, indicating the additional parasitic components on the test circuits.

Two GW-Instek GDP-100 100 MHz voltage probes and a PEM CWTMini50HF current Rogowski coil with bandwidth of 50 MHz are used to obtain waveforms of measurement. The bandwidths of these current/voltage probes enable capturing the switching waveforms in the interest of this paper. Further increase of bandwidth enables better capturing of the potential noise on the switching transient waveforms. This, for example, would be necessary in design of gate drivers that aim to suppress the disturbances. This is especially the case for SiC devices where the switching transients are faster, and the device is more prone to oscillations and disturbance by the circuit loop inductance at the output terminals. A 100 nF de-coupling capacitor is connected between the cathode of the Schottky Barrier Diode (SBD) and the emitter side of the BJT closest to the DUTs. An Agilent 33220 A 20 MHz arbitrary waveform generator is used for adjusting the pulse lengths t_{Q1}. A stray inductance of 60 nH is calculated due to the inevitable distance among the components. A similar circuit model is designed in LTSpice [27] to model switching transients to confirm the experimental results. The measurements of single devices are done using the circuit shown in Fig. 2 while the measurements of paralleled devices are done using the circuit shown in Fig. 3 to analyse current sharing imbalance.

IV. RESULT ANALYSIS

Fig. 5 shows the double-pulse test result in two different base resistances and temperatures at 800 V under the preset collector current of 8 A. Fig. 5(A) shows a period of delay between the base turn-OFF and the collector current drop in silicon

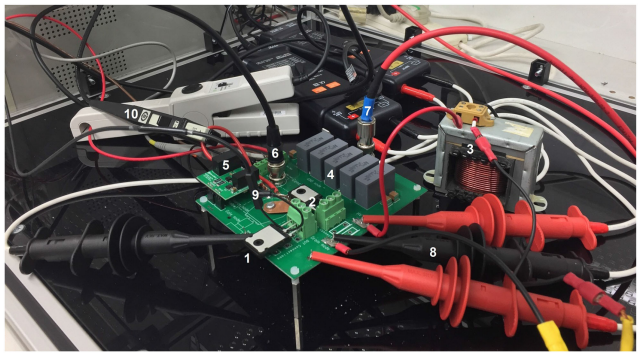

FIGURE 4. Components on the test board: 1- BJTs, 2- Schottky Diode, 3- Load Inductor, 4- DC Capacitors, 5- BJT Base Driver, 6- Input Signal, 7- HV power supply, 8- Voltage Probes, 9- Rogowski Coil and 10- Current Probe [4].

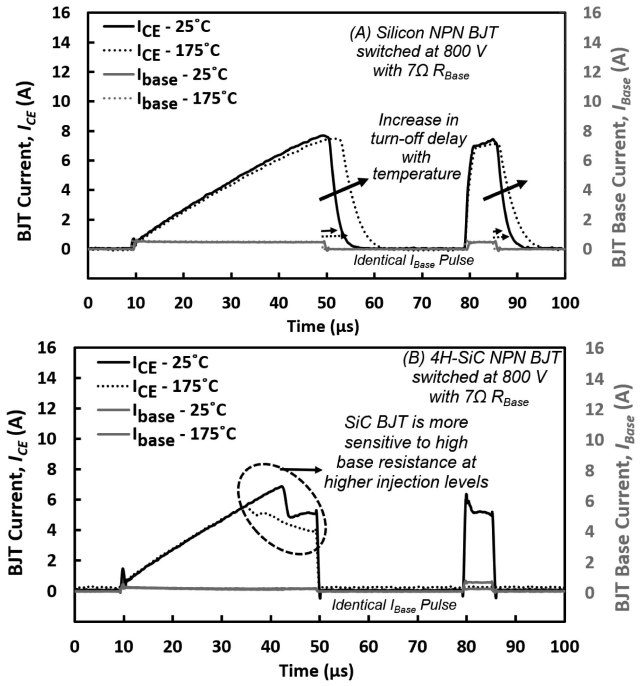

FIGURE 5. Double pulse test results of the collector and base current for (A) Silicon BJT and (B) 4H-SiC NPN BJT with the R_{base} of 7 Ω indicating the temperature-dependent delay under the same base current.

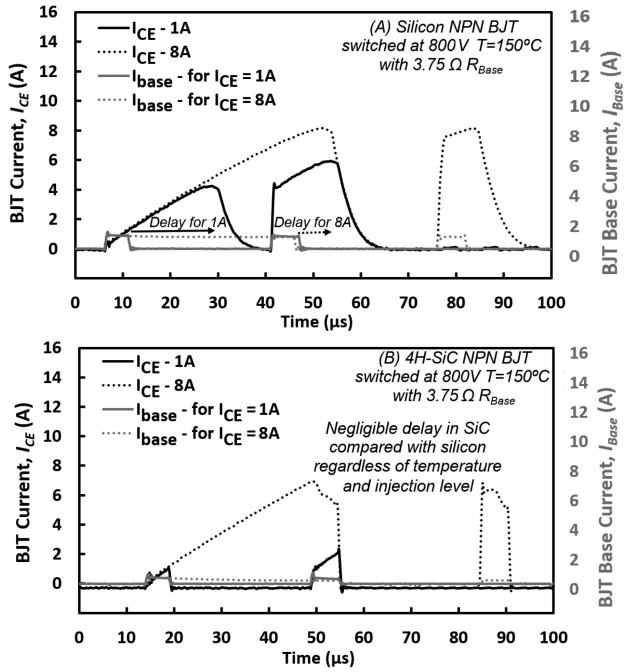

FIGURE 6. The double pulse test results regarding the collector and base current at 150 °C for (A) Silicon and (B) 4H-SiC BJT, with R_{base} of 3.75 Ω to analyze the turn-OFF delay with respect to different collector currents under the same base current.

BJT, which increases with rise of temperature. The diffusion coefficient is inversely proportional to temperature, leading to an increase of storage time as expected by (6) and (18). The base current is constant during the increase of collector current since it operates at the saturation region as the stored charge is reduced by the higher base resistance. In Fig. 5(B), both the base and collector current are turned on and off almost instantaneously for the 4H-SiC BJT, due to the much lower carrier lifetime and the significantly smaller dimensions enabling the decrease of the storage and transient time. The rating current of SiC device, as shown in Table 3, is found to decrease at high temperatures. Fig. 5(B) highlights the sensitivity issue of SiC at high base resistance during high injection (HIL) which reduces the collector current switching capability, leading to a twisted waveform. At 25 °C, the collector current dropped to an intermediate level before fully turn-OFF, reducing the current level in the second pulse. Together with the lower current rating at elevated temperatures, this waveform worsens at 175 °C as the second pulse is almost erased. This is due to the fact that by increase of the injected carriers into the base region, the injected base current had to rise beyond the capability of the base driver to maintain the device in the on-state, and this has become worse with increased minority carrier lifetime at higher temperatures.

Fig. 6 shows the double-pulse test result with respect to different collector currents at 800 V when $T = 150$ °C. The collector current applied in this case is 1 A and 8 A separately, all other parameters are the same. The average delay time is 15 μs for the Silicon BJT which deteriorates its performance, especially at high frequency as extra power losses are caused by the prolonged collector current. Meanwhile, the much lower delay time in SiC BJT in Fig. 6(B) is expected by its dimensions. The high temperature instability is also observed, i.e. the current at first pulse decreased to a lower level since the collector current of 8 A delivers the high-injection at 150 °C. Despite the significant advantages of the SiC BJTs compared with the high voltage Silicon BJTs, the inability to hold the current by the high DC gain [28] and low base driver current at high temperatures is a major drawback of the SiC BJTs [29]. Some of the results of the SiC BJT are not included in the measurements section for the case of 175 °C experiment since it failed when temperature rised above 150

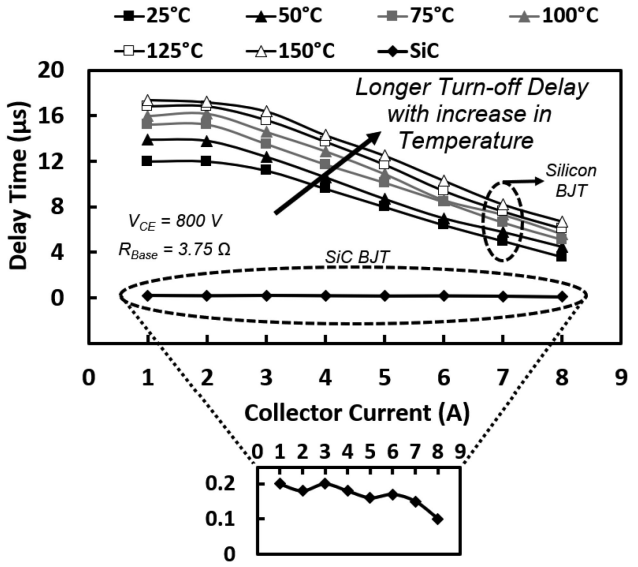

FIGURE 7. **The turn-OFF storage time is much longer in Silicon BJT with significant temperature dependence and current dependence, whereas this value is negligible in the SiC BJT.**

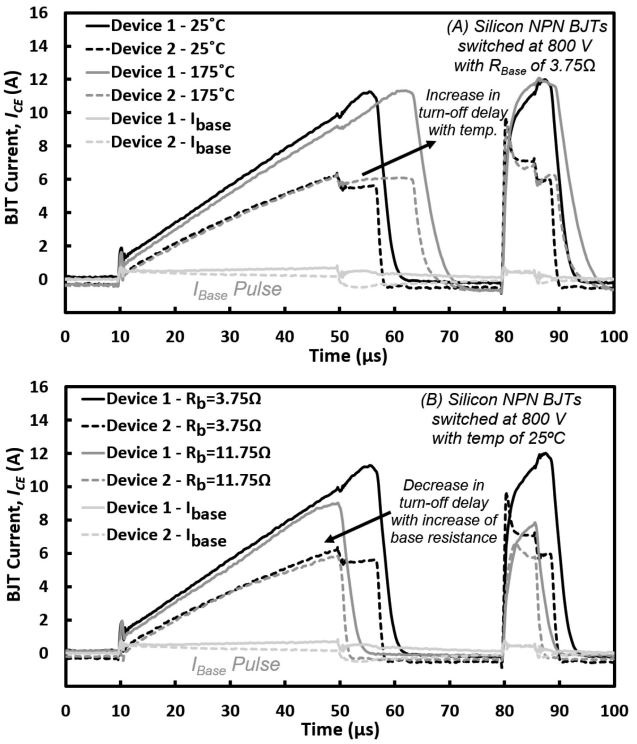

FIGURE 8. **The trends of turn-OFF delay and current imbalance in paralleled Silicon BJTs with (a) temperature and (b) base resistance.**

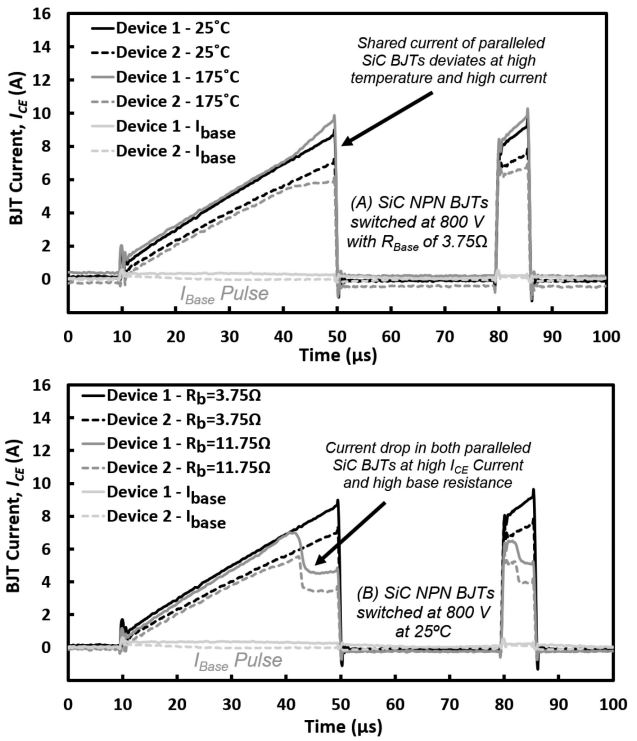

FIGURE 9. **The trends of shared current distribution and current collapse in paralleled SiC BJTs, with (a) temperature and (b) base resistance.**

°C. The Silicon BJT, on the other hand, worked well until the collector current exceeding 8 A at 175 °C. Therefore, during stressed measurements and due to the risk of damage to the device in high temperatures and currents, the temperature of up to 150 °C and collector current of up to 8 A are applied to avoid further failure.

Fig. 7 shows the delay time with temperatures and collector currents as the variables. A significant delay can be seen during the transients of the Silicon device with the average value of 10 μs while the turn-OFF delay in SiC device is about two orders of magnitude smaller, thanks to the much smaller base width in SiC BJT, and indicating a small downward trend with increase of the collector current. The delay increases at elevated temperatures, because electron's diffusion constant (D_n) decreases with increasing temperature as in (10). It is shown in Fig. 7 that at higher currents, due to the smaller W_{NM}, the delay is reduced in-line with (18).

The turn-OFF delay as in (18) also exists among the paralleled Silicon BJTs and the peak and imbalance of current deteriorates as temperature rises as seen in Fig. 8(A), while the turn-OFF delay and current imbalance is less significant when the base resistance increases as in Fig. 8(B) as the peak base driver current decreases, leading to slower transient switching rates, providing the period needed to extract the excess carriers. This suggest that turn-OFF delay at higher temperatures can be counterbalanced by increasing the base resistance at the cost of higher base current by the driver. As seen in Fig. 9, paralleled SiC devices do not demonstrate turn-OFF delay that is seen in Silicon devices in Fig. 8. However, there is a current imbalance between the two paralleled devices which deteriorates with temperature increase as shown in Fig. 9(A), while both paralleled devices suffer from the same current

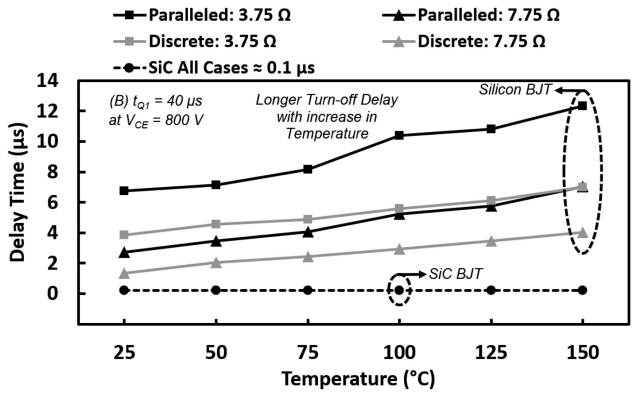

FIGURE 10. Turn-OFF delay comparison between discrete and paralleled Silicon and SiC BJTs when switched at 800 V and 8 A.

collapse seen in Fig. 5 when the base resistance increases as shown in Fig. 9(B). Fig. 10 shows the trend of turn-OFF delay in single discrete and paralleled Silicon BJTs with temperature with first pulse length of 40 μs, where it can be seen that paralleled BJTs exhibit a longer delay period compared to single devices with both base resistances, while the larger base resistance reduces the turn-OFF delay by reducing the transients' slew rate, providing the time necessary to extract the excess charge in the base region. The turn-OFF delay increases with temperature due to the increase of the minority carriers lifetime with temperature in Silicon as in (8), while in SiC the low minority carrier lifetime means there is effectively no turn-OFF delay which would be dependant on temperature.

The current imbalance among paralleled devices, as in Figs. 11 & 12, can be due to device parameters mismatch, gate drivers mismatch, power loop mismatch, or a combination of all. Most of these are shared among different transistors, however when it comes to device properties, the SiC MOSFETs and SiC BJTs exhibit significantly different features. In SiC MOSFETs, the two key parameters determining the effectiveness of current balance are on-state resistance and the gate threshold voltage drift. During on-state the impact of drain-source resistance will be partially countered by the device positive temperature coefficient (PTC) which will naturally prevent excessive current to flow through the device that experiences high junction temperatures. The device with higher junction temperature will also have lower threshold voltage that leads to early turn-on and late turn-off at the switching transients. As a result, the device may have to cope with the entire current for short periods with a potential for thermal runaway and parasitic BJT latch-up. In SiC BJTs, however, the mechanism of conduction and switching are significantly different due to the bipolar feature of the device (compared with MOSFETs as a unipolar device) in absence of gate oxides. In SiC BJTs, the parameters that influence the current imbalance are the current gain and high level injection. The current gain of BJTs drift with temperature, and is primarily determined by ionization of dopants that have not released carriers into the base region at lower temperatures. This is

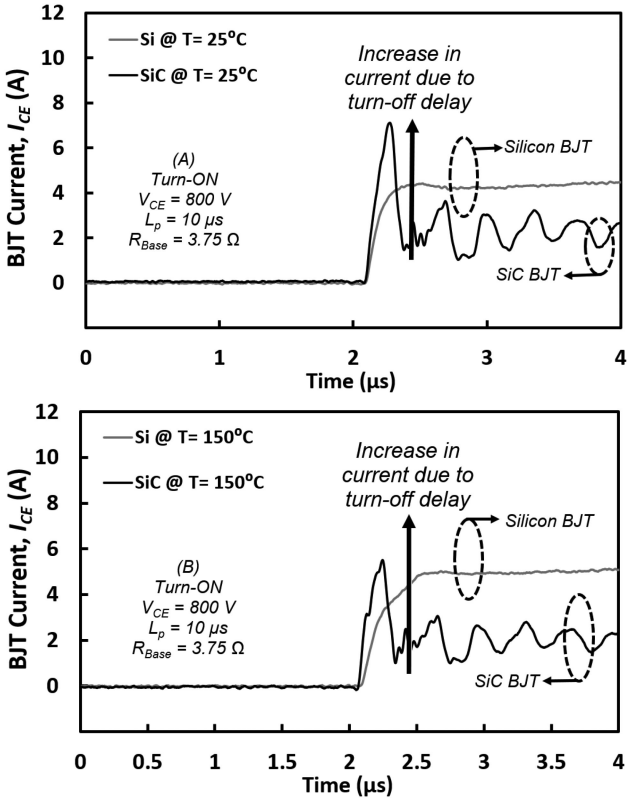

FIGURE 11. Turn-ON transient of Silicon and 4H-SiC BJT with pulse length of 10 μs with at (A) 25 °C and (B) 150 °C for the BJT collector current.

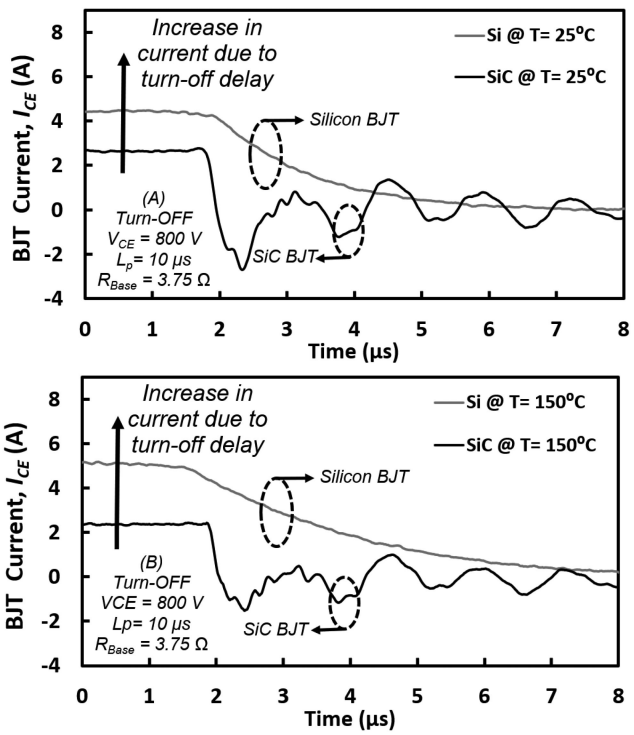

FIGURE 12. Turn-OFF transient of Silicon and 4H-SiC BJT with pulse length of 10 μs with at (A) 25 °C and (B) 150 °C for the BJT collector current.

more likely in SiC BJTs due to the higher ionization energy of dopant [9]. The onset of high-level injection at higher collector currents also means the current gain does not increase with further collector currents, i.e. higher base current is required for higher collector currents. This exacerbates the influence of the base driver variations on the current imbalance.

The collector current at turn-ON and turn-OFF transients are shown in Figs. 11 and 12 for both Silicon and SiC BJT. The turn-OFF delay is previously shown to get worse at elevated temperatures, which will in turn increase the collector current increase as the temperatures rises as effectively the length of the first pulse increases. When comparing Fig. 11(A) and Fig. (B), the much smaller W_B can be seen to play a significant role to reduce the t_{Ion} for the SiC BJT in-line with Eq. (16), while the increase of turn-ON period is expected by the decreasing of the diffusion coefficient at high temperatures as in (6), so decreasing of transient slew rates are expected to be seen at higher temperatures as shown in Fig. 11(B). The increase of temperature also impacts the turn-OFF transients as shown in Fig. 12(B). This is because of the increased carrier lifetime, and the lower diffusion coefficient which leads to a larger t_{I-off}, whereas the t_{I-off} is always lower for the SiC device because of the much lower carrier lifetime and the smaller dimensions of the die. Further measurements have indicated that as the collector current increases with the pulse width, the turn-OFF time further increases because of the decrease of diffusion coefficient as in (10), and the increase in carrier lifetime as in (14) at high currents. Although the diffusion coefficient of SiC is less dependent on the collector current, this is hard to observe since it was shown in (20) that the value of t_{I-off} is largely influenced by the square of the W_B.

The temperature dependence of switching transients can also be seen in Figs. 13 and 14 for a wide range of temperatures for the Silicon and 4H-SiC BJT. The turn-ON process of Silicon BJT in Fig. 13(A) is not significantly temperature-dependent. The reason for this is that the t_{I-on} is significantly lower than the t_{I-off}, hence making the temperature dependence not easily distinguishable. The collector current will asymptote to the on-state value which is the same as the original value before turning off. The SiC BJT turn-ON current transient is almost temperature-invariant as seen in Fig. 13(B). At the turn-OFF transition in Fig. 14, the Silicon BJT becomes slower at high temperatures, while the collector current increases with the delay. Therefore, the collector currents has some discrepancy with the expected value. The turn-OFF transient of the SiC BJT, however, is almost temperature-invariant as was the case of the turn-ON transient. This is due to the significantly lower minority carrier lifetime in SiC compared with Silicon, in addition to the smaller dimensions of the SiC BJT, thanks to its wide-bandgap, which leads to smaller parasitic elements and a narrow base and drift region. This means the charge required to switch the device into on-state is lower, and the follow-up extraction at turn-OFF will also be faster.

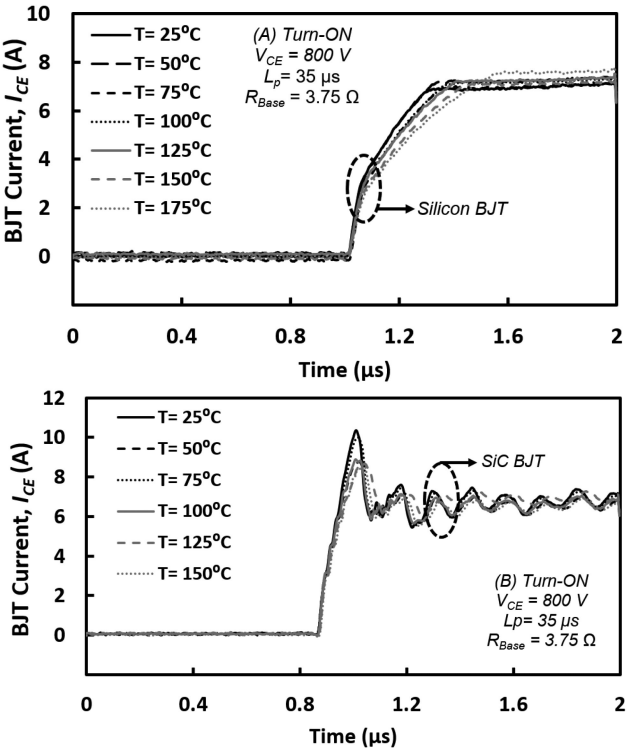

FIGURE 13. Turn-ON transient with pulse length of 35 μs for the (A) Silicon and (B) 4H-SiC BJT, for collector current at all temperatures.

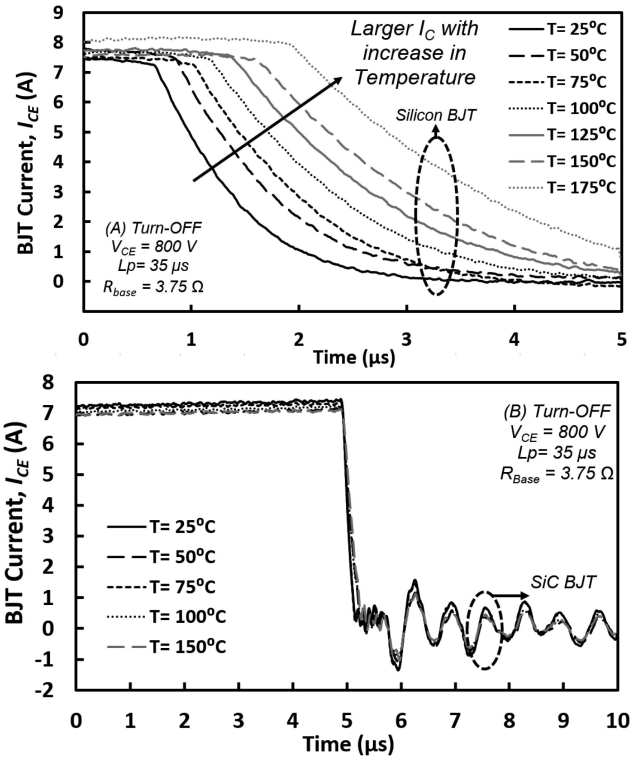

FIGURE 14. Turn-OFF transient with pulse length of 35 μs for the (A) Silicon and (B) 4H-SiC BJT, for collector current at all temperatures.

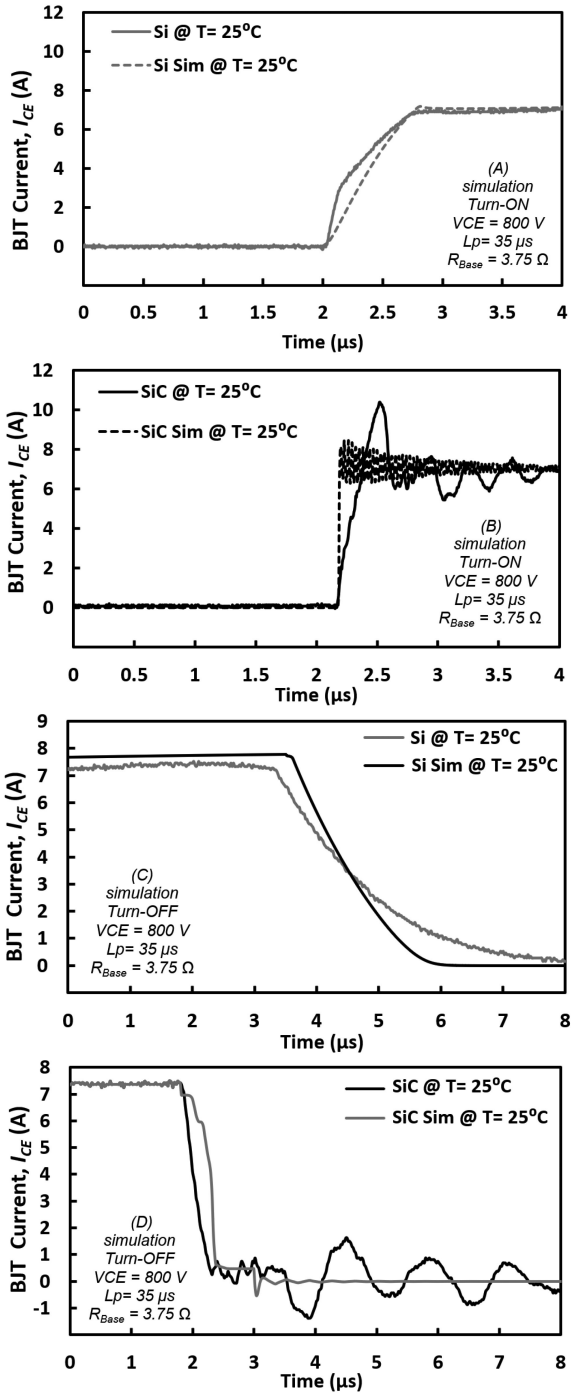

FIGURE 15. Simulation results for the measurements shown in Figs. 11 and 12 for turn-ON transients of (A) Silicon and (B) SiC BJT and turn-OFF transients for (C) Silicon and (D) SiC BJT, to evaluate the validity of the models.

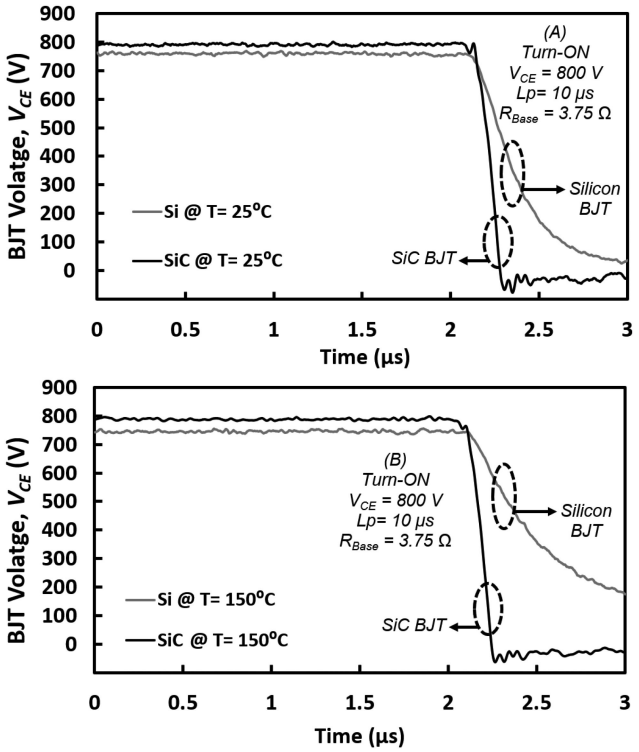

FIGURE 16. Turn-ON transient of silicon and 4H-SiC BJT with pulse lengths of 10 μs at (A) 25 °C and (B) 150 °C for BJT collector voltage.

The results of Figs. 11 and 12 match well with results of the simulations in Fig. 15. Although there is some error is modeling of the oscillations by the LTSpice, the *dI/dt* is found to be a good match in the model. It can be seen that although the frequency of oscillations in the SiC measurements are higher than what is predicted by the simulations, the slew rates in all case of simulations are close to that of the measurements, indicting that the modelling approached commonly used for the Silicon BJTs can be applicable to the case of high voltage SiC BJTs as well.

For a high collector current caused by a long base pulse, the collector voltage starts to increase early before the current fully turn-ON, because the large junction capacitor of the Silicon BJT cannot stand the high voltage for a long period before starting to being charged. This inhibits the on-state value of the collector current, leading to a lower value than expected even with consideration of the effect of the turn-OFF delay. It must be noted that the collector current of 8 A is the maximum rating current of the SiC BJT, and can lead to its breakdown at high temperatures. Despite this, the collector current of the SiC BJTs do not experience the increase by the turn-OFF delay and are in line with the equivalent pulse width, so would be easily controllable.

The SiC die has faster voltage transients in Fig. 16 and Fig. 17 as predicted by the models. At turn-ON transients in Fig. 16, the temperature-dependent diffusion coefficient decreases the J_C as in (6), leading to the prolonged voltage turn-ON period (t_{von}) as in (17), resulting in the slower transient in Fig. 16(B). The higher collector current can directly reduce the voltage turn-ON period in high injection level as in (17).

At turn-OFF transients shown in Fig. 17(A) and (B), turn-OFF process of the voltage is slower at high temperatures because of the temperature-dependent diffusion coefficient

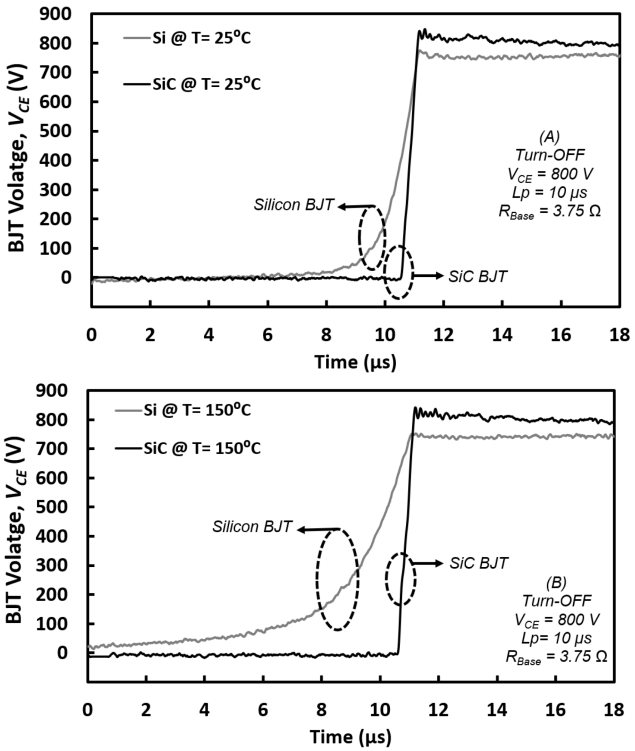

FIGURE 17. **Turn-OFF transient of silicon and 4H-SiC BJT with pulse lengths of 10 μs at (A) 25 °C and (B) 150 °C for BJT collector voltage.**

TABLE 4. **Transient Periods of Silicon and 4H-SiC NPN BJT at $T = 25$ ° C With $R_{Base} = 3.75$ Ω by the Measurements**

	Turn-ON		Turn-OFF	
	Silicon	SiC	Silicon	SiC
Stored Charge at 2 A	0.4 μs	0.06 μs	12 μs	1.2 μs
Stored Charge at 8 A	0.44 μs	0.05 μs	4.3 μs	0.09 μs
Current Transient at 2 A	0.405 μs	0.132 μs	4.8 μs	0.104 μs
Current Transient at 8 A	0.415 μs	0.130 μs	5.12 μs	0.106 μs
Voltage Transient at 2 A	1.97 μs	0.3 μs	3.6 μs	0.7 μs
Voltage Transient at 8 A	1.38 μs	0.28 μs	4.0 μs	0.75 μs

which increases the value of the voltage turn-OFF phase (t_{v-off}) as in (19). The slower performance is also due to the current dependence of holes diffusion constant (D_p) which also increases t_{v-off}. Furthermore, the stored charge in the base region (Q_{nB}) and collector region (Q_{SC}) are inversely proportionate to the diffusion coefficient, leading to more charge stored in the drift and base region, which reduces the depletion region, resulting in a smaller voltage drop at high current and temperature. The Q_{nB} and Q_{SC} built at the turn-ON is the same as that is to be removed extracted/recombined at turn-OFF, therefore the same trends for temperature- and current-dependence that was previously shown can also be seen in these figures.

The time taken to turn-ON and turn-OFF are shown in the Table. 4 for both the Silicon and SiC NPN BJTs. At the turn-ON transient, the $t_{transient}$ as in (15) of the Silicon BJT is increased with increase of the collector current as a result of the decreased diffusion constant of electrons (D_n) in high currents. The current turn-ON period (t_{I-on}) is also increased for the same reason. The voltage turn-ON period (t_{V-on}), on the other hand, decreases with collector current density (J_C) which as per (17) is the most dominant component to reduce the total turn-ON time at HLI. A faster turn-ON for the SiC BJT is predicted due to the significantly smaller dimensions of the base and drift region. In high temperatures, the transient time at turn-ON ($t_{transient}$) and current turn-ON period (t_{I-on}) are increased because of the decrease in the diffusion coefficient, while the decreased D_n also reduces the J_C and prolonging the voltage turn-ON time voltage turn-ON period (t_{V-on}). At the turn-OFF transient, the voltage turn-OFF period (t_{V-off}) of the Silicon BJT increases as the holes diffusion coefficient D_p is decreased at HLI as per (19). The current turn-OFF period (t_{I-off}) also increases because the decrease in D_n is dominant to the decrease of diffusion length (L_n). Nevertheless, the increase in these two terms is compensated by the reduction of charge stored period at turn-OFF (t_S), as the decreased width of conductivity modulated region (W_{NM}) is more significant compared to the drop of D_n, reducing the total turn-OFF time at HLI. These trends hold true for the SiC BJT at turn-OFF, even with the much smaller width of the base (W_B) and storage region (W_S), which contributes to a reduction of the turn-OFF time by an order of magnitude. It is seen that the t_S is much larger than the $t_{transient}$ since the charge depletion phase removes more carriers than those built initially. In high temperatures, the t_S and t_{V-off} are increased because of the decrease in diffusion coefficient. Since the decrease of D_n is dominant, the t_{I-off} are also increased. The DC current gain is also measured at the turn-ON and turn-OFF current gain [30]. The turn-ON gain at the second pulse is always lower than that of the turn-OFF at the first pulse because of the switching losses and the rating and sensitivity issue in SiC devices, especially in high temperatures as discussed earlier.

The results of the simulations [31], [32] indicate that the model match well with the measurements for both devices, representing the expected differences in the transient currents. Fig. 18 show the case of the two paralleled Silicon BJTs where the substantial current mismatch between the two devices seen in Fig. 8 is represented by the simulations, while Fig. 19 presents the results of the measurements and simulations of the case of two paralleled SiC BJTs, where the current mismatch, albeit at smaller value due to the absence of the turn-OFF delay [33], [34], is represented by both the measurements and simulations.

The switching transients' slew rates of the two device technologies indicate that the SiC device has a significant edge in terms of the switching rate over all temperatures, base resistance and collector-emitter current levels, while the numerical indications of the provided simulations have reconfirmed this advantage. To investigate the impact of transients' slew rates on switching energy, it is calculated for both the turn-ON and

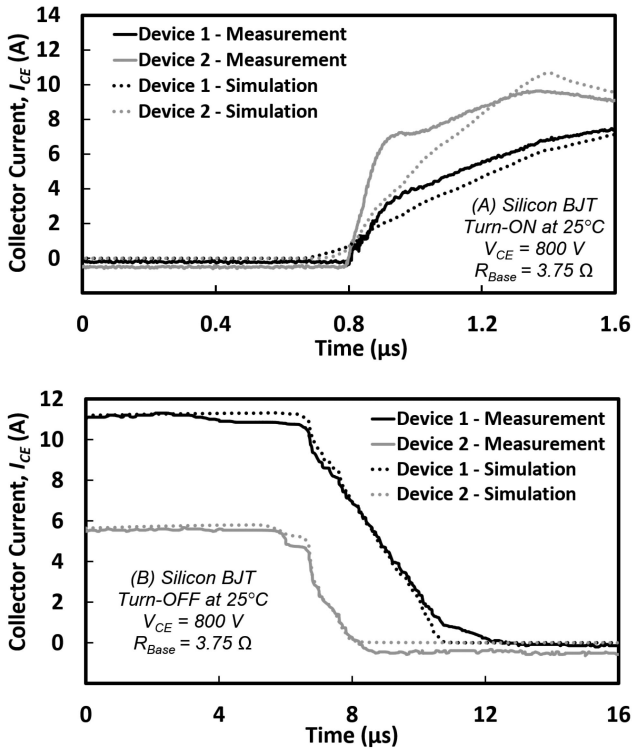

FIGURE 18. The simulations versus measurements of the collector current (A) turn-ON and (B) turn-OFF transients of the Silicon NPN BJT at 800 V.

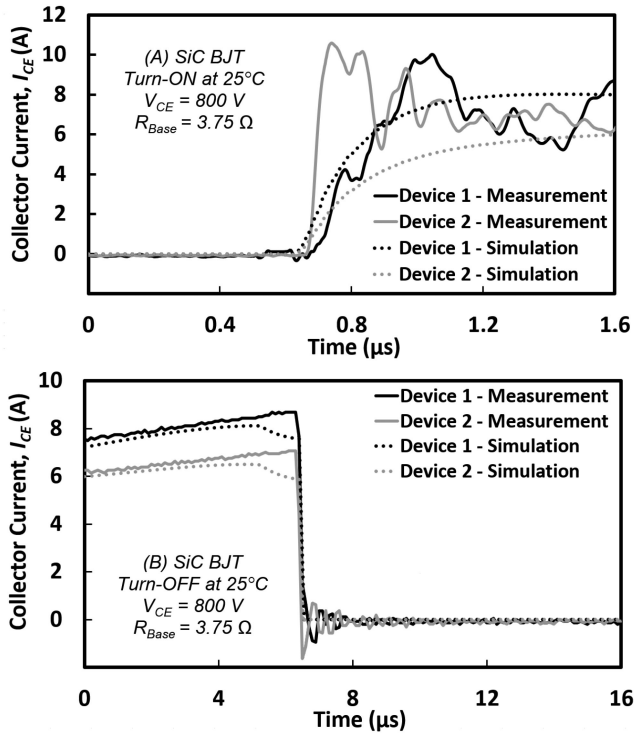

FIGURE 19. The simulations versus measurements of the collector current (A) turn-ON and (B) turn-OFF transients of the SiC NPN BJT at 800 V.

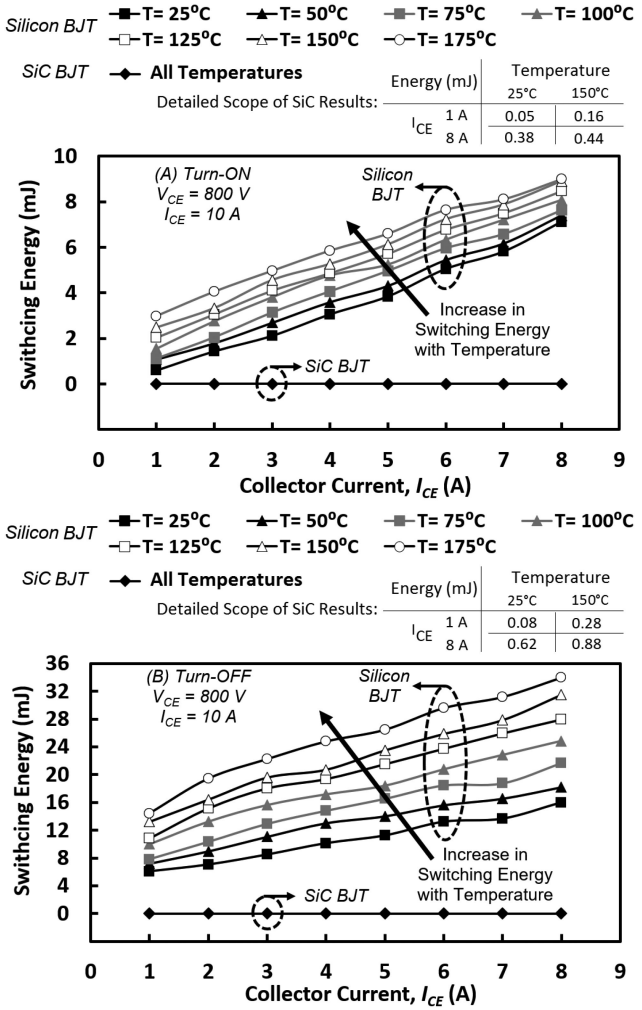

FIGURE 20. Calculated switching energy of Silicon and 4H-SiC BJTs at turn-ON and turn-OFF transients in a range of collector currents.

turn-OFF transients by integrating the transient power over its period as (28):

$$E_{Switching} = \int_{t_1}^{t_2} I_C(t) \cdot V_C(t) dt \tag{28}$$

As can be seen in Fig 20, the switching losses by the SiC device are one to two orders of magnitude smaller at both turn-ON and turn-OFF transients, while the switching energy in both silicon and SiC device increases with temperature as expected by the transient waveforms in Figs. 13–14 for the current transients and Figs. 16–17 for the voltage transients.

The HLI leads to a damping effect on the current gain (β) as the collector current increases as shown in Fig. 21. This confirms the theory that as collector current increases the high-level-injection will eventually saturates the gain. The current level at which the HLI occurs for each BJT depends on many factors, including its die area and current rating, leading to differing levels of current density. As seen in Fig. 21, the current gain is more stable at higher current density while the gain is reduced at lower current levels. It can be seen for both

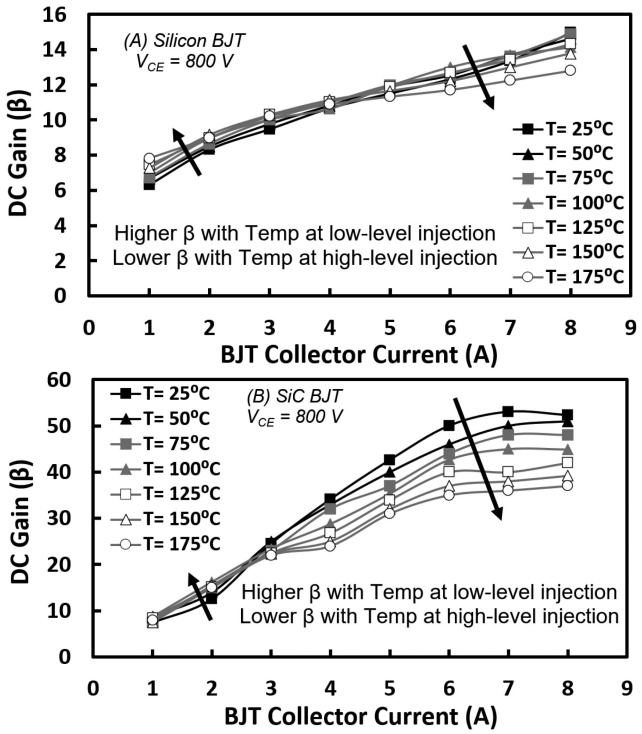

FIGURE 21. The common emitter DC current gain (β) for the (A) Silicon and (B) 4H-SiC NPN BJT at 800 V in a range of collector currents & temperatures, indicating opposing trends with increase of temperature depending on the injection level. It can also be seen that the rate of increase of β decreases as current increases due to impact of HLI.

the Silicon and Silicon Carbide BJTs that the gain is reduced at current levels below HLI, indicating boundary level of the high-level injection. This is particularly clear in the case of SiC BJT, where the trend of DC gain with collector current seen is very similar to that of [9]. In regard to trends with temperature, as seen in Fig. 21, the current gain of Silicon BJT is found to increase with temperature at low injection level ($\leq$4 A), which is expected since the current gain is largely determined by the recombination in the SCR region and the SCR recombination can be overcome by the increasing injection level, so J_{SCR} decreases at elevated temperatures as in (24). The β is larger at high temperatures because the current in the SCR region has negative temperature dependence. If the collector current continues to increase (>4 A), the DC current gain is limited primarily by the surface recombination while β increases since the diffusion current overcome the SCR recombination. With the increase of temperature at high collector currents, the lower diffusion coefficient shown in (6) leads to the fall of J_W described in (25) and thus shifts the boundary level of the high-level injection to lower current levels. The current gain is also found to decrease at high temperatures because of the increase in recombination rate and the decrease in diffusion coefficient. The effect of these two parameters reduce the surface recombination current and lead to a smaller DC gain at higher temperatures. Similar trend can also be seen at the SiC device, with the trend's twist point being at 3 A, however at a significantly higher DC gain. This smaller current level is due the high current density at emitter of SiC BJT with smaller die area.

V. CONCLUSION

In this paper, high voltage measurements of dynamic transient characteristics, DC current gain, and current sharing among paralleled Silicon and 4H-SiC NPN BJTs are presented, together with comprehensive modelling and simulation analysis. The voltage and current transient times in 4H-SiC BJT are, as demonstrated experimentally, at least 10 times shorter than that in silicon BJT because of the smaller width in the base and storage region. As for the Silicon BJT, the turn-OFF time is much larger than that of the turn-ON phase because of the substantial delay. The DC current gain is found to increase with increasing collector current in both devices at low injection levels, whereas its temperature dependence is flips at higher injection levels due to the impact of holes injected into the base and emitter region and increased recombination rate. Thereby, at low injection levels the DC gain increases with temperature in both devices while at high injections levels, it decreases with temperature. The decrease of current gain observed in Silicon BJTs as a consequence of HLI is found to be less severe than the SiC device. The current sharing among paralleled BJTs to increase the overall current rating is also investigated, and it is seen that the parasitic elements of the circuit, driver, and devices make a significant impact on current imbalance. This, in turn, leads to current deviations at high temperature and different levels of current collapse at high base resistance in case of the SiC device, while the turn-OFF delay in paralleled Silicon BJTs is conversely influenced by increase of temperature and base resistance.

REFERENCES

[1] J. Lutz *et al.*, *Semiconductor Power Devices: Physics, Characteristics, Reliability*, 2nd ed. Berlin, Germany: Springer International Publishing, 2018.

[2] T. Kim, M. Jang, and V. G. Agelidis, "Experimental performance evaluation of SiC BJT and Si MOSFET for 1.2 kW 300 kHz boost converter as a solar PV pre-regulator," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2014, pp. 284–288, doi: 10.1109/ICIT.2014.6894881.

[3] N. Zhang, "Silicon carbide bipolar junction transistors for high temperature sensing applications," Univ. California at Berkeley, Berkeley, CA, Rep. UCB/EECS-2016-170, 2016. [Online]. Available: https://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-170.pdf

[4] S. Jahdi, M. Hedayati, B. H. Stark, and P. H. Mellor, "The impact of temperature and switching rate on dynamic transients of high-voltage silicon and 4H-SiC NPN BJTs: A technology evaluation," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 4556–4566, Jun. 2020, doi: 10.1109/TIE.2019.2922918.

[5] J. Zhang, Y. Luo, P. Alexandrov, L. Fursin, and J. Zhao, "A high current gain 4H-SiC NPN power bipolar junction transistor," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 327–329, May 2003, doi: 10.1109/LED.2003.812531.

[6] S. Ichikawa, K. Kawahara, J. Suda, and T. Kimoto, "Carrier recombination in n-type 4H-SiC epilayers with long carrier lifetimes," *Appl. Phys. Exp.*, vol. 5, no. 10, Oct. 2012, Art. no. 101301, doi: 10.1143/apex.5.101301.

[7] X. Xu *et al.*, "High-voltage 4H-SiC GTO thyristor with multiple floating zone junction termination extension," in *Proc. 1st Workshop Wide Bandgap Power Devices Appl. Asia*, 2018, pp. 149–152, doi 10.1109/WiPDAAsia.2018.8734630.

[8] H. Barth and W. Hofmann, "Decrease of SiC-BJT driver losses by one-step commutation," in *Proc. Int. Power Electron. Conf.*, 2014, pp. 2881–2886, doi: 10.1109/IPEC.2014.6870090.

[9] Baliga, *Fundamental of Power Semiconductor Device*. Berlin, Germany:Springer, 2019.

[10] M. Hassan and M. Nomani, "Base-transit-time model considering field dependent mobility for BJTs operating at high-level injection," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2532–2539, Oct. 2006, doi: 10.1109/TED.2006.882269.

[11] G. Calderon-Lopez, A. J. Forsyth, D. L. Gordon, and J. R. McIntosh, "Evaluation of SiC BJTs for high-power DC–DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2474–2481, May 2014, doi: 10.1109/TPEL.2013.2273293.

[12] Y. Shi, S. Liang, F. Fang, and J. Wang, "Experimental comparison of SiC MOSFET and BJT," in *Proc. IEEE Int. Power Electron. Application Conf. Expo.*, 2018, pp. 1–6, doi: 10.1109/PEAC.2018.8590320.

[13] I. Oh, "A new base driving technique of a high voltage BJT for the horizontal deflection output using a CRT," in *Proc. 1st IEEE Asia Pacific Conf. ASICs*, 1999, pp. 67–74, doi: 10.1109/APASIC.1999.824031.

[14] J. Rabkowski, D. Peftitsis, and H.-P. Nee, "Parallel-operation of discrete SiC BJTs in a 6-kW/250-kHz DC/DC boost converter," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2482–2491, May 2014, doi: 10.1109/TPEL.2013.2283083.

[15] S. Liang, L. Deng, Z. Peng, Y. Shi, Z. J. Shen, and J. Wang, "A new proportional base driver technique for minimizing driver loss of SiC BJT," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 5485–5488, doi: 10.1109/ECCE.2018.8557373.

[16] L. Wu, J. Qin, M. Saeedifard, O. Wasynczuk, and K. Shenai, "Efficiency evaluation of the modular multilevel converter based on Si and SiC switching devices for medium/high-voltage applications," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 286–293, Feb. 2015, doi: 10.1109/TED.2014.2375875.

[17] X. Li *et al.*, "On the temperature coefficient of 4H-SiC BJT current gain," *Solid-State Electron.*, vol. 47, no. 2, pp. 233–239, 2003, doi: https://doi.org/10.1016/S0038-1101(02)00200-9.

[18] Y. Gerstenmaief, "A study on the variation of carrier lifetime with temperature in bipolar silicon devices and its influence on device operation," in *Proc. 6th Int. Symp. Power Semicond. Devices Ics*, 1994, pp. 271–274, doi: 10.1109/ISPSD.1994.583738.

[19] U. A. and V. E., "Investigation of charge carrier lifetime temperature dependence in 4H-SiC diodes," *Mater. Sci. Forum*, vol. 556/557, pp. 375–378, 2007, doi: https://doi.org/10.4028/www.scientific.net/msf.556-557.375.

[20] J. Bandyopadhyay, *Solid State Electronics Devices*, 3rd ed. Vikas Publishing House, 2017.

[21] S. M. Sze, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: Wiley, 1981.

[22] P. Ivanov, M. Levinshtein, A. Agarwal, S. Krishnaswami, and J. Palmour, "Temperature dependence of the current gain in power 4H-SiC NPN BJTs," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1245–1249, May 2006, doi: 10.1109/TED.2006.872701.

[23] P. A. Ivanov, M. E. Levinshtein, S. L. Rumyantsev, S.-H. Ryu, A. K. Agarwal, and J. W. Palmour, "Factors limiting the current gain in high-voltage 4H-SiC NPN-BJTs," *Solid-State Electron.*, vol. 46, no. 4, pp. 567–572, 2002, doi: https://doi.org/10.1016/S0038-1101(01)00215-5.

[24] W. M. Webster, "On the variation of junction-transistor current-amplification factor with emitter current," *Proc. IRE*, vol. 42, no. 6, pp. 914–920, 1954, doi: 10.1109/JRPROC.1954.274751.

[25] H. Li, S. Beczkowski, S. Munk-Nielsen, R. Maheshwari, and T. Franke, "Circuit mismatch and current coupling effect influence on paralleling SiC MOSFETs in multichip power modules," in *Proc. PCIM Europe Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2015, pp. 1–8.

[26] G. Semiconductor, "Normally- Off silicon carbide junction transistor," GA04JT 17–247 datasheet. [Online]. Available: https://www.genesicsemi.com/sic-junction-transistor/GA04JT17-247/GA04JT17-247.pdf

[27] S. Liang *et al.*, "A modified behavior spice model for SiC BJT," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 238–243, doi: 10.1109/APEC.2018.8341016.

[28] H. Miyake, T. Kimoto, and J. Suda, "4H-SiC BJTs with record current gains of 257 on (0001) and 335 on (000$\bar{1}$)," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 841–843, Jul. 2011, doi: 10.1109/LED.2011.2142291.

[29] Y. Gao, A. Q. Huang, S. Krishnaswami, J. Richmond, and A. K. Agarwal, "Comparison of static and switching characteristics of 1200 V 4H-SiC BJT and 1200 V Si-IGBT," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 887–893, May/Jun. 2008, doi: 10.1109/TIA.2008.921408.

[30] L. Lanni, B. G. Malm, M. ÃÜstling, and C.-M. Zetterling, "Influence of passivation oxide thickness and device layout on the current gain of SiC BJTs," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 11–13, Jan. 2015, doi: 10.1109/LED.2014.2372036.

[31] J. Wang, S. Liang, L. Deng, X. Yin, and Z. J. Shen, "An improved SPICE model of SiC BJT incorporating surface recombination effect," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6794–6802, Jul. 2019, doi: 10.1109/TPEL.2018.2871594.

[32] D. Johannesson and M. Nawaz, "Development of a simple analytical pspice model for SiC-based BJT power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4517–4525, Jun. 2016, doi: 10.1109/TPEL.2015.2477477.

[33] S. Liang, J. Wang, L. Deng, F. Fang, and Z. J. Shen, "Monolithic integration of SiC power BJT and small-signal BJTs for power ICs," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 24–30, Mar. 2020, doi: 10.1109/JESTPE.2019.2923671.

[34] S. Liang, J. Wang, L. Deng, Y. Shi, X. Yin, and Z. J. Shen, "An improved proportional base driver for minimizing driver power consumption of SiC BJT over wide current and temperature range," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1727–1735, Sep. 2019, doi: 10.1109/JESTPE.2019.2920888.

CHENGJUN SHEN (Student Member, IEEE) received the B.Sc. degree in electronics engineering from the University of York, York, U.K., in 2017, and the M.Sc. degree in electrical engineering from the University of Leeds, Leeds, U.K., in 2018. Since then, he has been working toward the Ph.D. degree in electrical engineering with the Electrical Energy Management Group Laboratory, School of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. His research interests include wide-bandgap semiconductor devices (specifically silicon carbide devices) in high voltage power converters, circuits, and high voltage power electronics applications.

SAEED JAHDI (Senior Member, IEEE) received the B.Sc. degree in electrical power engineering from the University of Science and Technology, Tehran, Iran, in 2010, the M.Sc. degree (with Distinction) in power systems from the City University London, London, U.K., in 2012, and the Ph.D. degree in power electronics from the University of Warwick, Coventry, U.K., in 2016. He was with the HVDC Center of Excellence of General Electric, General Electric (GE) Grid Solutions, Stafford, U.K. He is currently an Assistant Professor of power electronics with the Electrical Energy Management Group, University of Bristol, Bristol, U.K. His current research focuses on wide-bandgap power semiconductor devices in power electronics. Dr. Jahdi is a Chartered Engineer with the IET, U.K.

JUEFEI YANG (Graduate Student Member, IEEE) received the B.Sc. degree in electrical and electronics engineering in 2019 from the University of Bristol, Bristol, U.K., where he is currently working toward the Ph.D. degree in electrical engineering with the Electrical Energy Management Group Laboratory, School of Electrical and Electronic Engineering. His research interests include analysis of performance and reliability of power semiconductor devices in power electronics and wide-bandgap semiconductor devices, including silicon carbide devices in high voltage power electronics applications.

OLAYIWOLA ALATISE (Senior Member, IEEE) received the B.Eng. (first-class Hons.) degree in electrical and electronic engineering, and the Ph.D. degree in microelectronics and semiconductors from Newcastle University, Newcastle upon Tyne, U.K., in 2005 and 2008, respectively. In 2004 and 2005, he joined ATMEL North Tyneside, where he worked on the process integration of the 130-nm CMOS technology node. In June 2008, he joined the Innovation R&D Department, NXP Semiconductors, as Development Engineer where he designed, processed and qualified discrete power trench MOSFETs for automotive applications and switched-mode power supplies. In November 2010, he joined the University of Warwick, Coventry, U.K., as a Science City Research Fellow to investigate advanced power semiconductor materials and devices for improved energy conversion efficiency. Since February 2019, he has been a Professor of electrical engineering with the University of Warwick. He is the author or coauthor of more than 90 publications in journals and international conferences. His research interests include investigating advanced power semiconductor materials and devices for improved energy conversion efficiency. Prof. Alatise is an Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

JOSE ORTIZ-GONZALEZ (Member, IEEE) received the B. Eng. degree in electrical engineering from the University of Vigo, Vigo, Spain, in 2009, and the Ph.D. degree in power electronics from the University of Warwick, Coventry, U.K., in 2017. Since 2013, he has been with the School of Engineering, University of Warwick. In January 2018, he was appointed as a Senior Research Fellow of power electronics. Since August 2019, he has been an Assistant Professor of power electronics. He has authored or coauthored more than 40 publications in journals and international conferences. His current research interests include electrothermal characterization of power devices, reliability, and condition monitoring.

RUIZHU WU (Member, IEEE) received the B.Sc. degree in telecommunication engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2010, the M.Sc. degree in engineering from Xihua University, Chengdu, China, in 2014, and the Ph.D. degree in engineering from the University of Warwick, Coventry, U.K., in 2019. He is currently a Research Fellow with the School of Engineering, University of Warwick, working on reliability and applications of silicon carbide power electronics.

PHIL MELLOR (Member, IEEE) received the B.Eng. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, University of Liverpool, Liverpool, U.K., in 1978 and 1981, respectively. He is currently a Professor of electrical engineering with the Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. Prior to this, he held academic posts with the University of Liverpool, from 1986 to 1990 and the University of Sheffield, Sheffield, U.K., from 1990 to 2000. His current research interests include high-efficiency electric drives and actuation and generation systems for application in more electric aircraft and hybrid electric vehicles.