Impact of Temperature and Switching Rate on Forward and Reverse Conduction of GaN and SiC Cascode devices: A Technology Evaluation

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Abstract

This paper provides the first comprehensive study on the forward and reverse conduction and reliability performance of the Gallium Nitride (GaN) and Silicon Carbide (SiC) power cascode devices, in comparison with standard silicon & SiC power MOSFETs and the silicon superjunction MOSFETs. The impact of temperature and the external gate resistance are investigated, and a practical yet accurate analytical model has been developed to calculate the switching rate of cascode devices. The 3rd quadrant operation devices through the body diodes is also studied along with unclamped switching properties for avalanche breakdown limits of GaN and SiC cascodes.

1 Introduction

Gallium Nitride high electron mobility transistor (GaN HEMT) is a recent wide-bandgap power semiconductor device with many interesting features. The cross-section of the device is shown in Fig.1(i). The properties of GaN HEMT include wide-bandgap, high carrier mobility in the two dimensional electron gas (2DEG) layer & high critical electric field. The main disadvantage of early HEMTs was its normally-on depletion-mode characteristics [1]. Since development of HEMTs, there has been many efforts to fabricate normally-off enhancement-mode HEMTs, for example by addition of a thin AlGaN barrier layer [2], gate injections [3], p-GaN gate [4] and gate recess structures [5]. The cascode structure [6] is also suggested as an alternative approach where normally-on devices are stacked with a low voltage normally-off transistor as shown in Fig.1(ii). HEMT & JFET devices in cascodes do not have inherent body diodes, but the body diode of the low side MOSFET effectively acts as the reverse body diode of the whole cascode structure [7]. The current will then continue to flow in reverse direction through the high voltage transistor itself. The working principles of the cascode structures is shown in Fig.1(ii). As seen, at off-state the low voltage MOSFET will first block up to its rating (~20-30V). This voltage is then transferred to gate of the depletion-mode device (HEMT or JFET). This voltage will cause the high voltage device to turn-off and block most of the rest of the voltage. This continues until the low voltage MOSFET is turned-on, at which point the voltage across it is reduced and this will lead the depletion-mode device to once again turn-on. The voltage sharing between the two devices is based on the output capacitances and this must be carefully calculated [8]. In this study, comprehensive measurements are performed on forward and reverse conductions. In addition, the reliability of GaN HEMT and SiC JFET cascodes are assessed too. An analytical model for transients is also developed and validated.

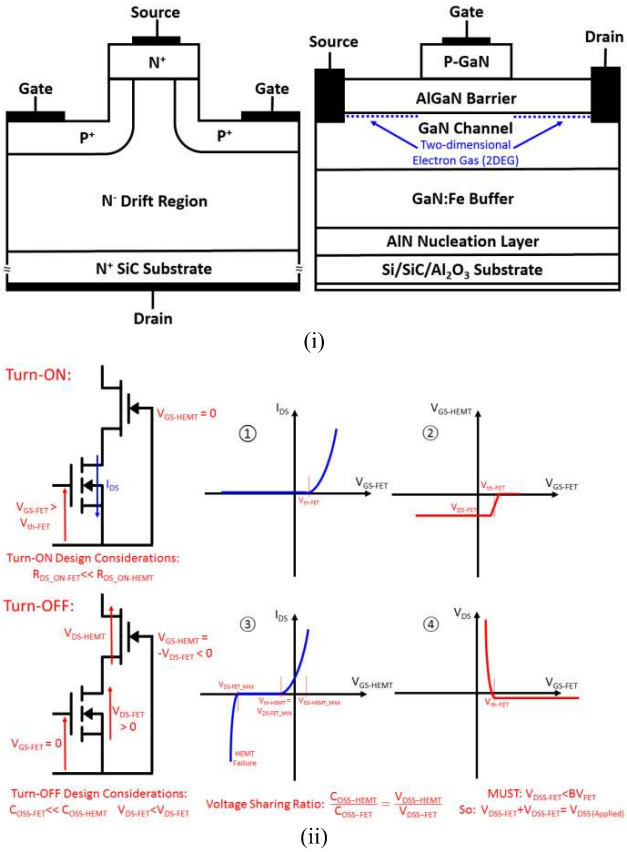
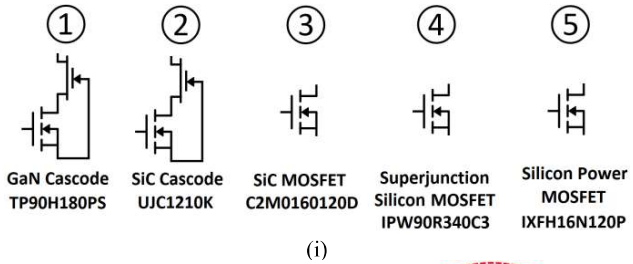


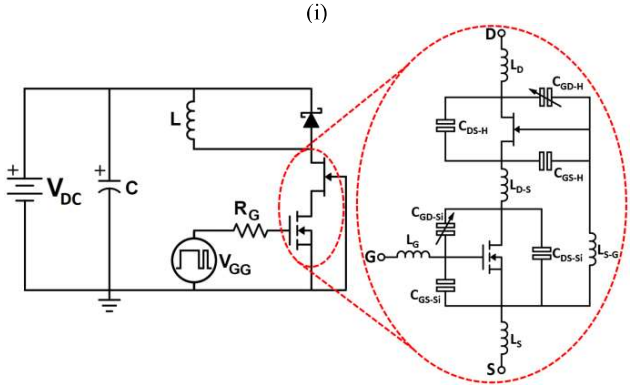
Fig. 1 (i) Cross-section of SiC JFET (left) & GaN e-HEMT (right), (ii) working principles of the cascode devices.

2 Experimental Set-up

To analyse the performance of the devices, their characteristics must be compared with similarly rated devices under the same switching conditions. The devices that are used in the measurements of this paper are shown in Fig.2(i) with their datasheet number. The circuit diagram of the double pulse inductive switching measurement tests used in the experiments of the paper is also shown in Fig.2(ii). The tests are performed with different external gate resistances on the gate driver ranging from 10 to 220 Ω with temperatures of the switching transistor ranging between 25°C to 175°C in steps of 25°C. The temperature is controlled via an electric hotplate that is directly connected to the case of the transistors. The cascode GaN device and the silicon superjunction MOSFET are rated at 900 Volts while the SiC cascode and silicon and SiC standalone MOSFETs are rated at 1.2 kV. The forward tests are performed with 650 volts and 5 A while the reverse 3rd quadrant tests are performed with reduced electrothermal stress at 400 volts and 4 A.



(i)



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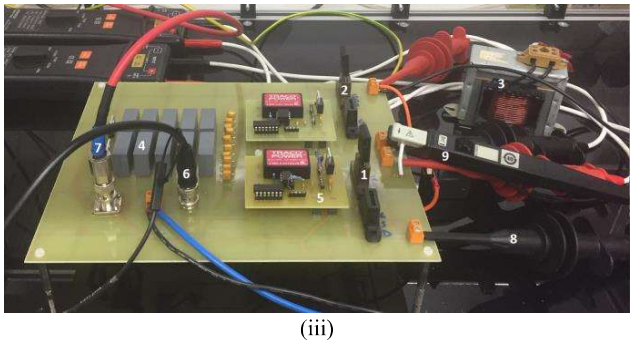


(iii)

Fig. 2 (i) The silicon, SiC & GaN power devices in the measurements, (ii) circuit diagram of the double-pulse inductive tests with all parasitic elements indicated, (iii) the test board for the measurements.

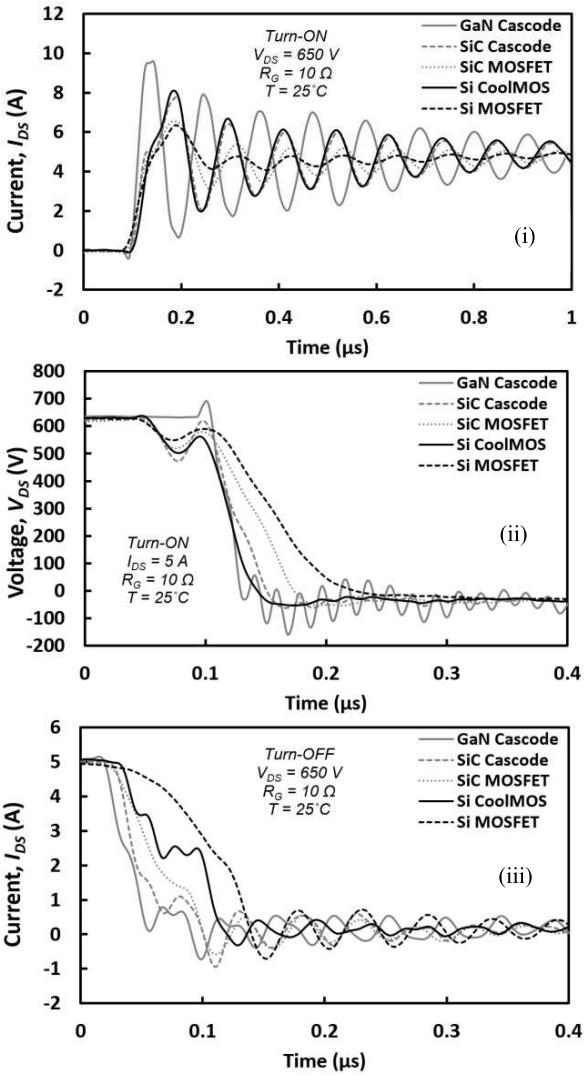
The measurements consist of the dynamic switching transients at turn-on and turn-off switching events and its comparison with standalone MOSFETs, 3rd quadrant reverse conduction of the body diodes and its stored charge in addition to avalanche breakdown limits of the two cascode devices under excessive electrothermal stress via unclamped inductive switching.

3 Experimental Measurements

To ensure on the comprehensiveness of the measurements of this study, they are divided into forward dynamic transient measurements, reverse switching transients and reliability evaluations through unclamped inductive tests. The forward conduction (1st quadrant) and reverse conduction (3rd quadrant) are evaluated for all silicon, SiC & GaN devices while the unclamped tests are performed only for the latter two.

3.1 Forward Conduction

Fig.3(i) shows the turn-on current transient of the silicon, SiC & GaN devices tested at 650 volts with gate resistance of 10 Ω and 25°C. It is seen that the GaN device has the fast current switching transient and hence the highest degree of oscillations. Fig.3(ii) also show the turn-on voltage transient of the devices in the same switching event. It can be seen that the slope of the voltage drop in the GaN device is the fastest and it is the only device that exhibits considerable ringing.



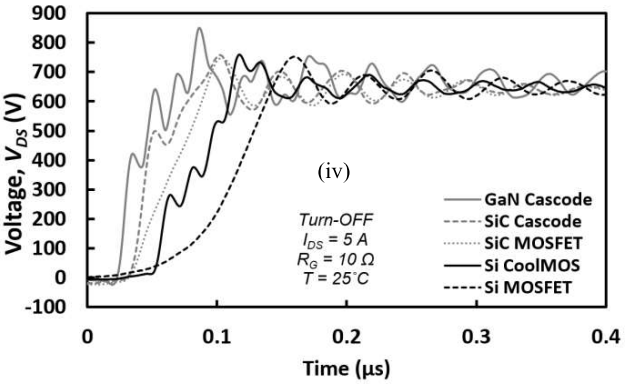


Fig. 3. The transients of the silicon, SiC & GaN devices at (i) current turn-on, (ii) voltage turn-on, (iii) current turn-off & (iv) voltage turn-off. It can be seen that the GaN device is the fastest in all switchings.

Fig.3(iii) shows the turn-off current transient of the silicon, SiC & GaN devices tested at 650 volts with gate resistance of 10 Ω and 25°C. It is seen that the current in the GaN device drops without any delay while the other devices are a bit slower. This has clearly resulted in some degree of oscillations at the output. Fig.3(iv) shows the voltage transient during the same switching event. It can be seen that similar to the current, the voltage transient in the GaN cascode is the fastest followed by the SiC cascode and SiC MOSFET.

Fig.4 shows the turn-on switching times of the (i) GaN and the (ii) SiC cascodes in comparison with each other in a wide range of temperature and gate resistances. It is seen that the switching times at turn-on for GaN cascode slightly increases with temperature while in SiC it slightly decreases due to the opposing trends in the threshold voltage of JFETs & HEMTs.

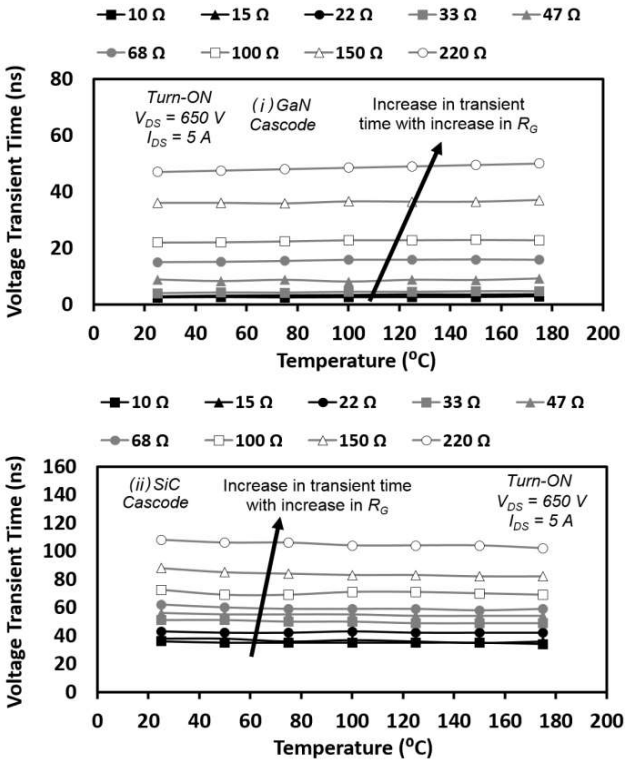


Fig. 4. Turn-on voltage transient time of GaN & SiC cascodes in a wide range of temperatures and gate resistances.

At turn-off, as shown in Fig.5, both devices have their transient times increased with temperature while GaN device in Fig.5(i) is more sensitive to gate resistance than the SiC device in Fig.5(ii). At low gate resistance, the GaN device has much lower voltage transient time than the SiC device, however as the gate resistance is increased the transient time of the GaN device rapidly increases to become similar to that of the SiC.

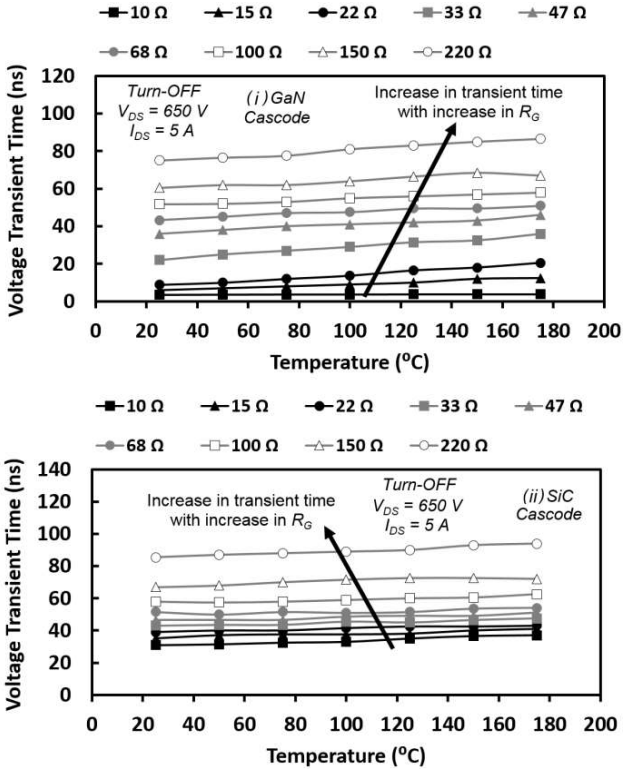


Fig. 5. Turn-off voltage transient time of GaN & SiC cascodes in a wide range of temperatures and gate resistances.

Fig.6 shows the switching rates (*dI/dt* & *dV/dt*) of (i) current transients at turn-on, (ii) voltage transient at turn-on, (iii) current transient at turn-off & (iv) voltage transient at turn-off, showing that GaN cascode is much faster than all other competing devices in all cases. The turn-on current switching rate of GaN cascode is almost 7.5 and 3.5 times higher than the SiC cascode for all temperatures when switching with 10 Ω (shown in Fig.6) and 220 Ω gate resistance (not shown in Fig.6). This is another indicator that the dependency of the GaN cascode on of the gate resistance is higher than that of the SiC cascode. This, although in essence is an advantage, but demonstrates why designing an effective gate driver and application circuit for GaN cascode can be challenging. Regarding to turn-off stage, the tendency of the current switching rate is same as turn-on stage, but the superiority of GaN is less clear in turn-off stage. Here, the current switching rate of GaN device is just 2.5 times higher than that of the SiC cascodes. Additionally, when the gate resistance is increased from 10 Ω to 220 Ω, the current switching rate is decreased by 600% and 400% for GaN and SiC cascodes respectively. The superiority of the switching rate of GaN cascode is even more clear in the voltage transients (*dV/dt*) compared with the superjunction MOSFET, SiC cascode and silicon MOSFET.

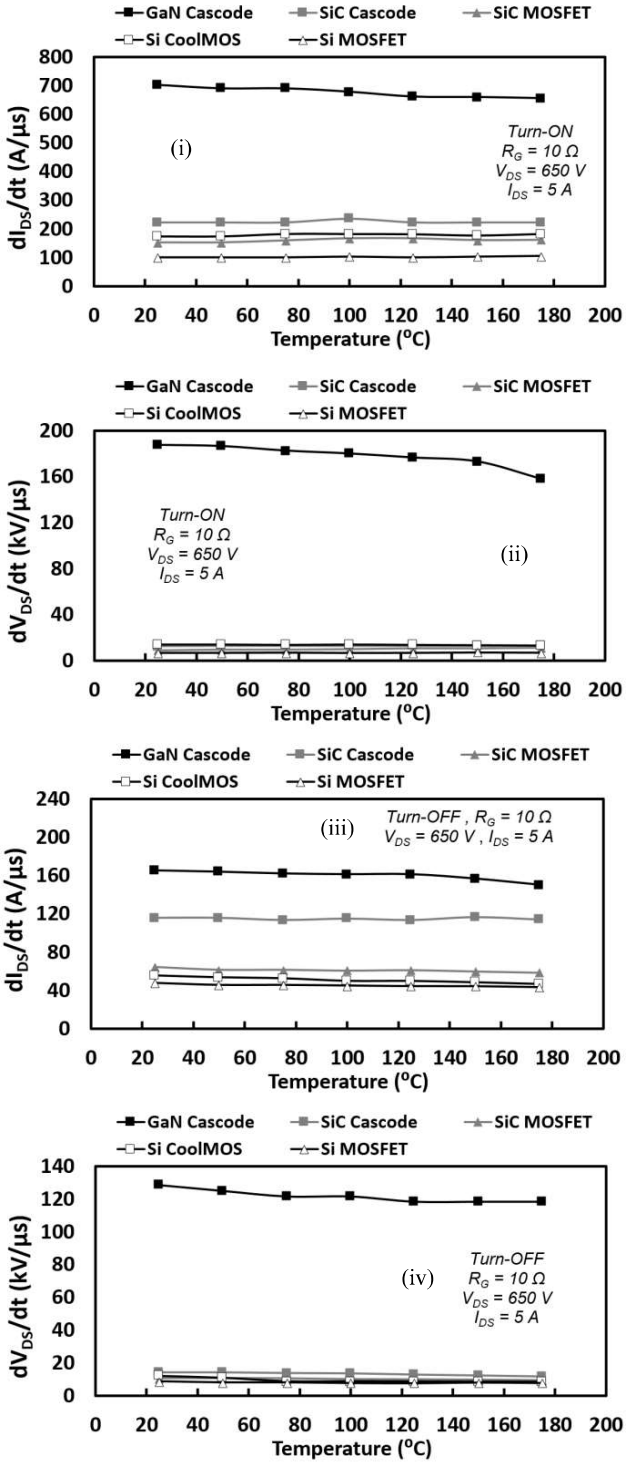


Fig.6. Switching rate at turn-on & off transients for all 5 devices, showing the superiority of GaN cascode.

3.2 Reverse Conduction

To understand the effectiveness of GaN & SiC cascode devices in comparison with standalone transistors in all applications, their 3rd quadrant operation in reverse direction is also analysed. This is an important factor as reverse anti-parallel conduction typically becomes necessary when an inductive load is present, otherwise there will be a significant voltage spike across the transistor in reverse direction with typically destructive consequences. In Fig.7(i), it can be seen that the body diode forward voltage of the GaN cascode is higher than that of the SiC cascode because of the lateral structure of the HEMT device which means the voltage blocking region between drain and source and the 2DEG channel region have the same length. Therefore, the length of the channel for a device that is rated at 900 volts will be substantial. Also, it can be seen that the conduction in SiC body diode is temperature invariant due to its lower temperature resistance compared with GaN. Fig.7(ii) also shows the reverse recovery current in turn-off switching transient, where both GaN & SiC cascode show negligible recovery charge compared with silicon superjunction MOSFET. This is because the low voltage enhancement-mode MOSFET in the cascode have very low stored recovery charge and the GaN HEMT and SiC JFET do not contribute to reverse recovery charge.

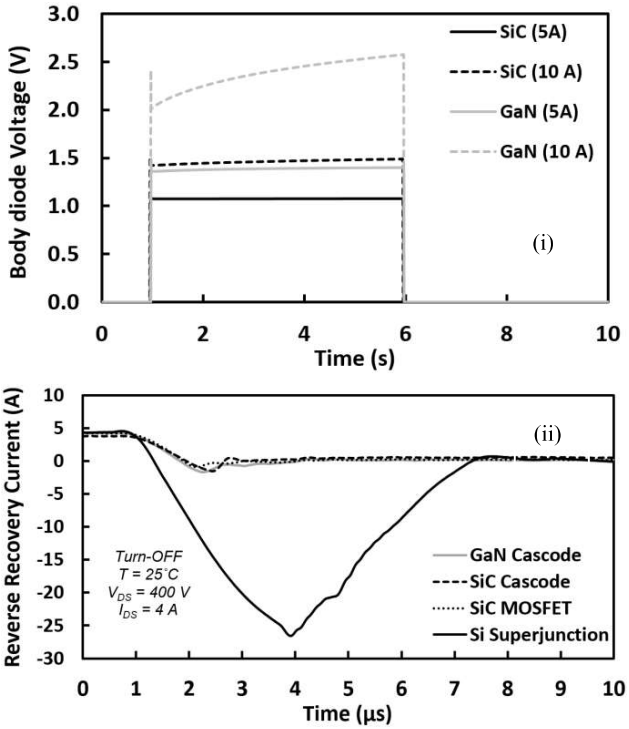


Fig. 7 (i) Forward voltage of body diodes of GaN and SiC cascodes during on-state conduction in the 3rd quadrant, (ii) the reverse recovery current in the body diodes at turn-off switching transient.

3.3 Reliability Studies

An important factor in analysis of power devices is their reliability in terms of the unclamped inductive switching (UIS) performance. To investigate this, the UIS test circuit is set up by removal of the diode in the double-pulse switching circuit and the pulse width of the gate voltage and the inductor size is differentiated to decide the peak of the avalanche current, therefore the current is constantly risen until avalanche failure happens. Fig.8(i) shows the UIS breakdown limits of the SiC cascode while Fig.8(ii) shows the same for the GaN cascode. It is seen that SiC cascode tolerates significant electrothermal stress to almost twice of its ratings, while the GaN device has virtually no avalanche robustness, failing at only 1 A. The GaN cascode failure is due to the lack of an extraction mechanism for the generated hole current in depletion-mode HEMT.

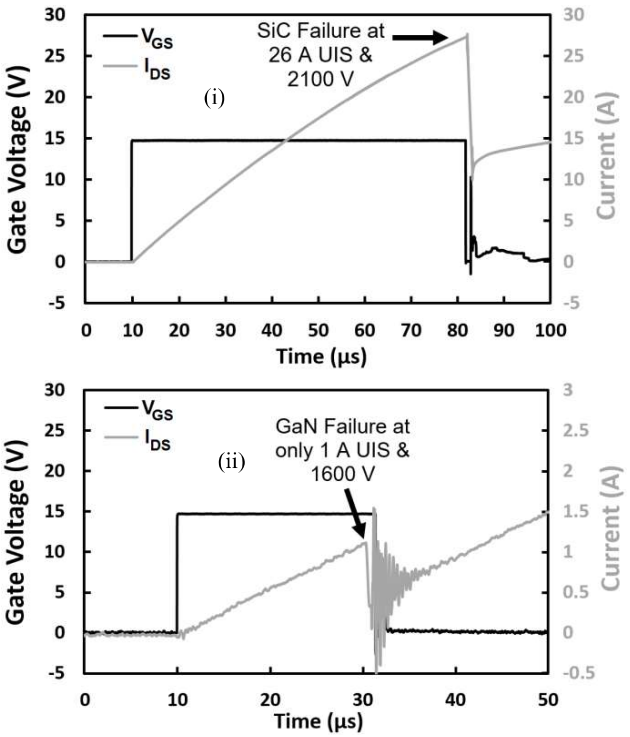


Fig. 7. The (i) SiC cascode device is capable of demonstrating very high avalanche rating with excessive electrothermal stress while (ii) GaN cascode has negligible avalanche breakdown limits.

4 Modelling Analysis

To model the performance of cascode devices, the equivalent capacitors must be first evaluated based on the 6 internal capacitances for the two devices in the cascode structure as shown in Fig.8. The overall capacitances at the output terminals of the device are given in the datasheets, based on which the internal capacitances can be calculated by using computer software, i.e. MATLAB, as in equivalent capacitors. Here, we effectively have 6 unknown variables for the 6 internal capacitors in the cascode structure and 6 total capacitor values from the datasheet graph. The model and datasheet values of the total equivalent capacitors for the GaN and SiC cascode devices is shown in Fig.9. The current in the low voltage driving MOSFET can be written as:

$$I_{DS} = \frac{W\mu C_{OX}}{2L}(V_{GS} - V_{TH})^2 \quad (1)$$

In which V_{GS} is the gate-source voltage, V_{TH} MOSFET's threshold voltage, W is the width of the device, L is the length of the device, the C_{OX} is the gate oxide capacitance and µ is the carriers' mobility. The only time-dependant parameter in (1) is the gate voltage. By taking the derivative of the equation (1) with time, the current switching rate at turn-on and turn-off transients can be written as:

$$\frac{dI_{DS}}{dt}\Big|ON = \frac{W\mu C_{OX}}{2L}(V_{GS} - V_{TH})\frac{dV_{GS}}{dt}\Big|ON \quad (2.1)$$

$$\frac{dI_{DS}}{dt}\Big|OFF = \frac{W\mu C_{OX}}{2L}(V_{GS} - V_{TH})\frac{dV_{GS}}{dt}\Big|OFF \quad (2.2)$$

Therefore, determining the time-dependant gate-source voltage is essential to be able to estimate the switching rates.

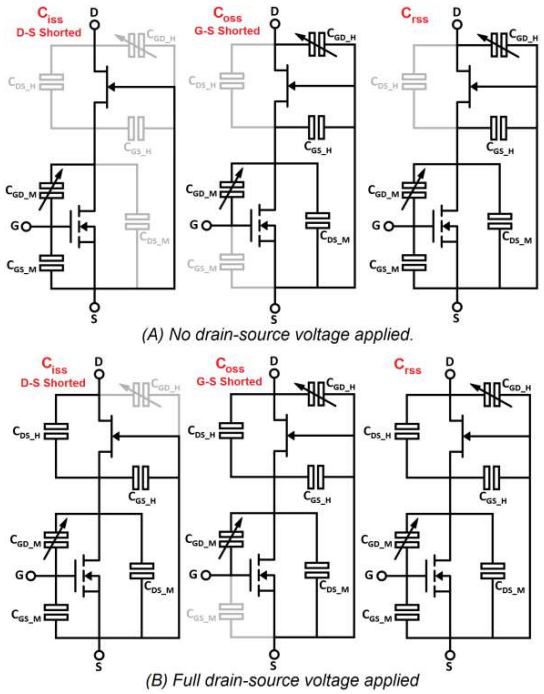


Fig. 8. The effective parasitic capacitors in the cascode structure with and without applying of drain-source voltage.

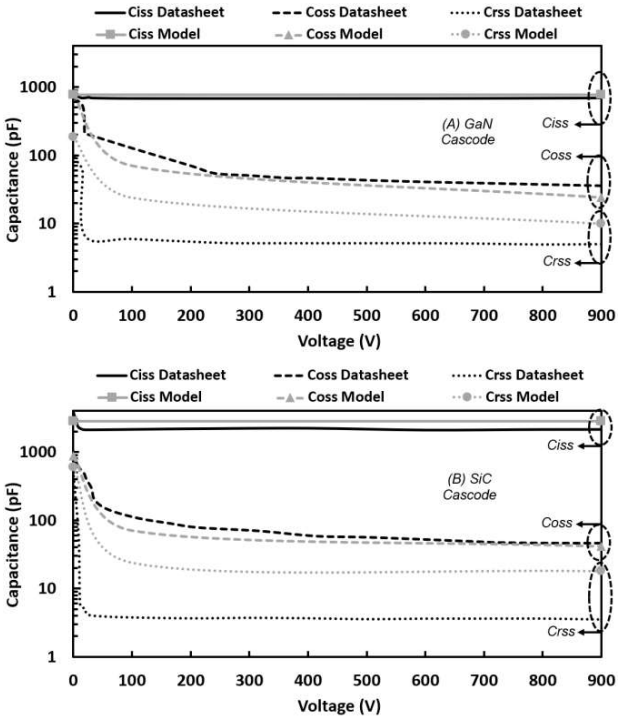


Fig. 9. The model and datasheet values of the total equivalent capacitors for the GaN and SiC cascode devices.

In order to ensure that the model is accurate all the parasitic inductances and the voltage-dependant non-linear parasitic capacitances must be considered in determination of the rate of change of V_{GS}. To solve the typical double pulse circuit in Fig 2(ii), Kirchhoff's laws are used to result in the equation 3 which is dV_{GS}/dt for the turn-on and turn-off transients. The implementation of dV_{GS}/dt of eq. (3) in (2) delivers the dI_{DS}/dt.

$$\left.\frac{dV_{GS}}{dt}\right|ON = \frac{2V_{GG}.\sin\left(\frac{t\sqrt{-C_{issHV}.R_G^2+4(L_G+L_S)}}{2(L_S+L_G).\sqrt{C}}\right)}{\sqrt{C_{issHV}.(4(L_G+L_S)-C_{issHV}.R_G^2)}} \times \frac{\exp\left(\frac{-R_G.t}{2(L_G+L_S)}\right)}{\sqrt{C_{issHV}.(4(L_G+L_S)-C_{issHV}.R_G^2)}} \quad (3.1)$$

$$\left.\frac{dV_{GS}}{dt}\right|OFF = \frac{V_{GG}}{C_{issHV}}.\exp\left(\frac{-R_G.t}{2L}\right) \times cosh\left(\frac{t\sqrt{\frac{C_{issHV}.R_G^2}{4}-L}}{L.\sqrt{C_{issHV}}}\right) - \frac{\frac{V_{GG}}{\sqrt{C_{issHV}}}\exp\left(\frac{-R_G.t}{2L}\right)R_G.\sinh\left(\frac{t\sqrt{\frac{C_{issHV}.R_G^2}{4}-L}}{L.\sqrt{C_{issHV}}}\right)}{2\sqrt{\frac{C_{issHV}.R_G^2}{4}-L}} \quad (3.2)$$

Fig.10 shows the results of the model and its comparison with measurements for the GaN & SiC cascode devices for both the (i) turn-on and (ii) turn-off switchings. It can be seen that the developed model matches well with the measurements for a range of gate resistances. The dI_{DS}/dt is decreased with increase of gate resistance in both the turn-on and turn-off transients. It is also seen that at turn-on the GaN device has 3.5 times faster switching rate while in the turn-off, this superiority is only twice that of the SiC cascode. The model, as developed in equation 2 by implementing the equation 3 has also been able to predict this trend correctly.

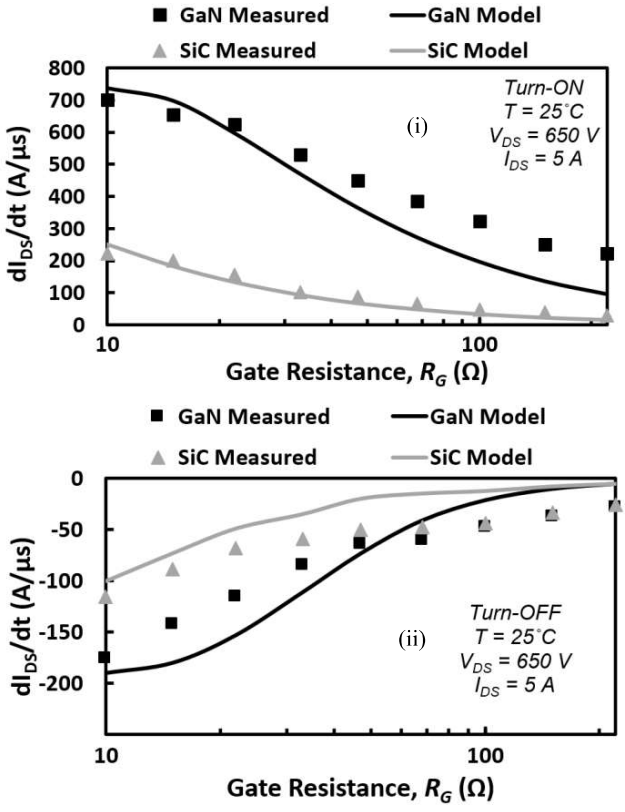


Fig. 10. The model results for dI_{DS}/dt at (i) turn-on & (ii) turn-off transients of GaN & SiC cascodes matches well with measurements.

5 Conclusion

In this paper, the key performance characteristics of the GaN and SiC cascode devices in comparison with similarly-rates silicon and SiC devices are analysed. Extensive experimental measurements on devices have shown that the GaN normally-off cascode device has superior switching rate performance in both turn-on and turn-off transients in its current and voltage waveforms, followed by the SiC cascode device, SiC standalone device and the silicon power MOSFETs. It is also shown that the switching rate of both GaN & SiC cascodes are not significantly temperature-dependant, but they are more dependent on gate resistance, especially in the case of GaN device. It is shown experimentally that the body-diode of the GaN & SiC cascodes stored very small reverse recovery charge when compared with other devices, especially the silicon superjunction MOSFET. This is due to the small low voltage MOSFETs used in cascode structure coupled with reverse conduction ability of depletion-mode HEMTs & JFETs. The unclamped inductive switching (UIS) measurements on the two cascode devices shows that the GaN device have negligible avalanche rating while the SiC device exhibits significant avalanche ruggedness. The lack of avalanche rating in the GaN device is due to the absence of an extraction mechanism of the generated holes in the GaN/AlGaN interface during avalanche process. Finally, a modelling analysis is performed for the switching rate of the two cascode devices. As the equivalent capacitance of the devices dynamically change throughout the switching the values for each of the six capacitors in each cascode structure must be first derived. The results of the model exhibit a close likeness of the measurements for both GaN & SiC cascodes.

6 Acknowledgements

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