Dual-Ferroelectric Coupling Engineered Two-Dimensional Transistors for Multifunctional In-Memory Computing

Zheng-Dong Luo,[1] Siqing Zhang,[1] Yan Liu,[1]* Dawei Zhang,[2] Xuetao Gan,[3]* Jan Seidel,[2,4] Yang Liu,[5] Genquan Han,[1,6] Marin Alexe,[7] and Yue Hao[1]

1. State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, P. R. China

2. School of Materials Science and Engineering, UNSW Sydney, Sydney NSW 2052, Australia

3. Key Laboratory of Light Field Manipulation and Information Acquisition, Ministry of Industry and Information Technology, and Shaanxi Key Laboratory of Optical Information Technology, School of Physical Science and Technology, Northwestern Polytechnical University, Xi'an 710129, China

4. ARC Centre of Excellence in Future Low-Energy Electronics Technologies (FLEET), UNSW Sydney, Sydney NSW 2052, Australia

5. School of Materials Science and Engineering, State Key Laboratory of Material Processing and Die & Mould Technology, Huazhong University of Science and Technology, Wuhan 430074, P. R. China

6. Emerging Device and Chip Laboratory, Hangzhou Institute of Technology, Xidian University, Hangzhou 311220, P. R. China

7. Department of Physics, The University of Warwick, Coventry, CV4 7AL, United Kingdom

*Email: xdliuyan@xidian.edu.cn; xuetaogan@nwpu.edu.cn

Abstract

In-memory computing featuring a radical departure from the von-Neumann architecture is promising to substantially reduce the energy- and time-consumption for data-intensive computation. With the increasing challenges facing the silicon complementary metal-oxide-semiconductor (CMOS) technology, developing in-memory computing hardware would require a different platform to deliver significantly enhanced functionalities at the material and device level. Here, we explore a dual-gate two-dimensional ferroelectric field-effect transistor (2D FeFET) as a basic device to form both non-volatile logic gates and artificial synapses, addressing in-memory computing simultaneously in digital and analog spaces. Through diversifying the electrostatic behaviours in 2D transistors with the dual-ferroelectric coupling effect, rich logic functionalities including linear (AND, OR) and nonlinear (XNOR) gates were obtained in unipolar (MoS_2) and ambipolar ($MoTe_2$) FeFETs. Combining both types of 2D FeFETs in a heterogeneous platform, an important computation circuit, *i.e.* half-adder, was successfully constructed with an area-efficient two-transistor structure. Furthermore, with the same device structure, several key synaptic functions are shown at the device level and an artificial neural network is simulated at the system level, manifesting its potential for neuromorphic computing. These findings highlight the prospects of dual-gate 2D FeFETs for the development of multifunctional in-memory computing hardware capable of both digital and analog computation.

Keywords: ferroelectric field-effect transistors, 2D materials, logic-in-memory, artificial synapse, dual-gate structure.

INTRODUCTION

Emerging intelligence applications, such as the artificial intelligence of things (AIoT), robotics and edge computing, are enabled by the high-performance computation framework that is designed to process a large amount of data in a time- and energy-efficient manner.[1-6] The performance of such data-intensive computation, however, has been evaluated to be fundamentally limited by the increasing disparity between the performance of the physically separated logic and memory blocks while implemented on a conventional von-Neumann architecture. To tackle the barrier imposed by the von-Neumann architecture, one promising solution is to blur the boundary between memory and logic units, which ultimately leads to the so-called in-memory computing.[1-4] Similar to the key attribute of the biological brain where information processing and memory are strongly intertwined,[7, 8] merged logic and memory functions are supposed to be realised within the same structure for in-memory computing,[2, 4] thus gaining significantly improved processing and energy efficiency for data-intensive computation. Towards such an efficient computing scheme, augmented circuit design and improved software techniques have been proposed to address the in-memory computing in both digital (Boolean logic-in-memory) and analog (matrix-vector multiplication for neuromorphic computing) spaces based on the conventional complementary metal-oxide-semiconductor (CMOS) implementation.[5, 9-12] Despite these early successes, the performance and functionalities of such volatile memory devices are inherently restricted by the characteristics of their enabling technology, *i.e.*, silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs); thus, these in-memory computing architectures would inevitably suffer from complex circuit design and high static power dissipation.[1, 2, 5, 13] Consequently, this motivates a bottom-up approach which focuses on radical innovations at the lowest level of computing hierarchy-the material and device level, aiming to deliver the required device functionalities and performance boost with innovative material attributes, advantageous device concepts and area-efficient architectures.

Towards a beyond-CMOS platform for high-performance in-memory computing, significant efforts are turning to conceptually efficient non-volatile memory (NVM) technologies.[1, 2] Exploiting the emerging physical attributes from the constituent nanoelectronic materials and device architectures, these NVMs can perform logic operation and/or dynamic

synaptic weight update while storing the computation states *in situ*, thus allowing to achieve non-volatile logic gates without CMOS-concerned static power dissipation[14] and mimic the plasticity of biologic synapses for neuromorphic computing.[2] Among a variety of emerging NVMs such as phase-change memories,[14] two-terminal memristors[15] and spin-orbit-torque memories,[16] 2D semiconductor-based ferroelectric field-effect transistors (2D FeFETs) have recently emerged as an appealing candidate for non-volatile logic gates[17, 18] and artificial synapses/neurons.[19-21] Leveraging the synergistic combination of the advantageous features such as aggressive thickness scaling, enhanced electrostatic control and reconfigurable ambipolarity of the atomically-thin 2D materials[22-24] as well as the non-volatile polarisation, hysteresis switching and plasticity-reminiscent domain evolution of the gate ferroelectrics,[25-27] 2D FeFETs have already demonstrated advantages for in-memory computing, including multifunctionalities, low-power and fast operation, large conductance switching ratio, high endurance and retention as well as synaptic behaviours.[21, 26, 28] Moreover, 2D FeFETs share a similar device structure with that of the conventional MOSFET-only replacing the channel and dielectric layers with 2D semiconductors and ferroelectrics, respectively, which is beneficial to provide all the benefits of the CMOS technology.[26, 28]

Despite the rich electrostatic physics and high CMOS-compatibility, simultaneous applications of 2D FeFETs in both in-memory computing criteria, *i.e.* logic-in-memory and synaptic neuromorphic computing, are, however, rare and have been constrained by the device functionalities and associated circuit design. At the device level, the basic cell for a neuromorphic computing circuit, *i.e.*, the synaptic weight update cell, can be readily realised with a single 2D FeFET;[21, 29] however, a non-volatile logic gate based on a single FeFET has been limited and would generally require a complex circuit structure involving the cascading of multiple devices and/or sequential computing operations,[30, 31] resulting in area- and operation-inefficiency (see Supporting Information Note 1). At the circuit level, a crossbar array has been actively exploited as a promising design to perform the matrix-vector multiplication for neuromorphic computing with a single resistive switching device as the synaptic weight update cell;[32] however, mapping a single non-volatile logic gate compromising several resistive switching devices into the crossbar array has been proven to be difficult and /or require a complex design (see Supporting Information Note 1).[33] Therefore, different combinations of

2D FeFETs would be necessary to form the basic digital and analog in-memory computing cells, respectively, which thus inevitably increase the manufacturing cost and complexity. An ultimate pursuit to a multifunctional in-memory computing cell would thus be a functionally-reconfigurable device that can be customised on demand, so that a single multifunctional 2D FeFET can simultaneously carry out logic and synaptic operations with a universal core circuit design. To this end, it necessitates the further tailoring/diversification of the conventional ferroelectric field-effect behaviours in 2D FeFETs by identifying ideal material systems and multifunctional device architectures.

In this work, we propose an improved 2D FeFET scheme as the basic structure to perform both digital and analog in-memory computing operations, through employing the dual-ferroelectric coupling effects and the reconfigurable polarity of the 2D transition metal dichalcogenide (TMD) channels. Unlike the overwhelmingly studied single-gate 2D FeFET (sketched in Figure 1a), the proposed device concept featuring the double ferroelectric-gates (see Figure 1b) can perform multifunctional in-memory computing operations, *i.e.* non-volatile logic gates and synaptic transistors, with a universal single-transistor structure. With independent polarisations in the respective top- and bottom-ferroelectric layer acting as two logic inputs, the dual-gate 2D FeFETs can accomplish two-input Boolean logic-in-memory operations. Specifically, the linear (AND, OR) and nonlinear (XNOR) logic functions are achieved for unipolar MoS_2 and ambipolar $MoTe_2$ dual-gate FeFETs, respectively. To illustrate the potential of the dual-gate 2D FeFETs for complex computation circuits, a non-volatile half-adder using a simple two-transistor structure has been demonstrated based on a heterogeneous foundation integrating both MoS_2 and $MoTe_2$ FeFETs. Furthermore, similar with the conventional three-terminal synaptic FeFETs,[29] the single-gate memristive operations are also shown in the proposed dual-gate 2D FeFETs by setting the polarisation state fixed in one of the ferroelectric layers. Benefiting from the fact that it can perform logic and synaptic operations within a single transistor structure, the proposed dual-gate 2D FeFETs can be efficiently mapped into the crossbar structure for both digital and analog in-memory computing circuits (see Supporting Information Note 1). The presented dual-gate 2D FeFETs exhibit the integrated digital logic-in-memory and analog synaptic behaviours, thus constituting a proof-of-concept for promising types of multifunctional in-memory computing cells.

RESULTS AND DISCUSSION

As schematically depicted in Figure 1, the device architectures along with the associated operating mechanisms for both single- and dual-gate 2D FeFETs are presented. Note that it is well-known that both unipolar and ambipolar FETs can be realised with suitable 2D TMDs as the active semiconductor channel;[24, 34] thus, we would discuss the 2D FeFETs in two aspects, *i.e.*, the unipolar and ambipolar devices. Figure 1a,c shows a typical single-gate 2D FeFET, which features a conventional three-terminal structure, *i.e.* source (S), drain (D) and gate (G). The underlying working mechanism has been well-established for such ferroelectric-field effect devices, which can be described as the effect of the strong ferroelectric coupling to the active channel.[35, 36] Taking the bottom-gated device as an example (Figure 1a,c), the spontaneous electrical polarisation in the gate ferroelectric layer can be inverted by the applied voltage, which consequently leads to the accumulation of positively or negatively charged mobile carriers in the adjacent semiconductor channel to screen the underneath polarisation field. Therefore, for a unipolar semiconductor channel (*e.g.*, *n*-type), the polarisation up (P_{up}) and down (P_{down}) states in the bottom ferroelectric could result in electron accumulation and depletion in the channel, resulting in high and low conductance states of the FeFET, respectively. By contrast, for the ambipolar semiconductor-based FeFETs, both electron- and hole-dominated high conductance levels can be enabled in the electron (under P_{up}) and hole (under P_{down}) accumulation states, respectively.[37-39] The abovementioned effect of ferroelectric polarisation on the transport properties of the semiconductor channel can be easily understood with the energy band diagrams. Figure 1e depicts the cross-sectional single-gate FeFET structure with different ferroelectric polarisation states, and the corresponding energy band diagrams along the channel from drain to source with the drain-source voltage (V_{ds}) > 0. For the *n*-type unipolar 2D FeFET, the semiconductor channel is accumulated (depleted) of electrons along with the strongly downward (upward) band bending at P_{up} (P_{down}) so that the resulting electron injection into the channel is allowed (blocked), whereas the large Schottky barrier at the drain contact would prohibit the hole injections for both polarisation states. Thus, the *n*-type unipolar 2D FeFET is at electron-dominated high and low conductance states for P_{up} and P_{down}, respectively. By contrast, the ambipolar channel is with electron- and hole-accumulation states as well as a thinned Schottky barrier at the source and drain contacts for P_{up} and P_{down}, respectively, thus

resulting in the high conductance states for both *n*- and *p*-branch.

Based on the analysis of ferroelectric coupling effect in the single-gate FeFETs, we now propose the corresponding operating principle for the dual-ferroelectric coupling engineered 2D transistors. To realise the dual-ferroelectric coupling effect, independent top (TG) and bottom gates (BG) have been added in the proposed double gate architecture (see Figure 1b,d). Note that in such a device configuration, the polarisation of the top ferroelectric layer can only manipulate the energy band profile of the top-ferroelectric-gated channel region (local channel) due to the screening of polarisation by the source/drain contact.[40] Compared with the single BG devices (see Figure 1e), as the top ferroelectric polarisation can independently determine the carrier concentration in the local channel, it is plausible that an extra barrier between the local channel and the rest region of the channel should be formed.[41-43] Therefore, extending the band diagram analysis of the single-gate FeFETs, four types of energy band diagrams corresponding to the different arrangements of top and bottom ferroelectric polarisation states can be deduced, see Figure 1f. For the unipolar 2D FeFET, as either gate can fully deplete the channel, the high conduction state would only be achieved at the electron accumulation state corresponding to the dual-gate configuration of P_{down} (top ferroelectric) and P_{up} (bottom ferroelectric), see Figure 1f(i)-(iv). For the ambipolar 2D FeFET, the situations are different. As mentioned before, when the bottom ferroelectric is at P_{down}, the device only behaves as a *p*-type FET with the electron transport prohibited, due to the facilitated hole injection through the thinned Schottky barrier at the drain contact. Through further independently modulating the top ferroelectric layer, the barrier profile of the local channel further bends up (down) under P_{up} (P_{down}), thus the injection of holes is allowed (blocked) by the TG-controlled barrier, see Figure 1f(v, vi). Consequently, both high and low hole-dominated conductance states can be expected with switching the top ferroelectric polarisation. Conversely, when the bottom ferroelectric is reversed to P_{up}, electron-dominated transport behaviour is expected in the device. Thus, a low (high) conductance state would be achieved when the electron currents are suppressed (enhanced) by the up (down) bending of the local channel potential, see Figure 1f(vii, viii). Clearly, compared with the conventional single-gate FeFETs, rich ferroelectric-field effect behaviours can be realised in the 2D FeFETs with the presented dual-ferroelectric coupling effects. Note that the dual-gate FeFETs have been explored previously focusing on two types of structures, *i.e.*, 1) double-

ferroelectric gate[44] and 2) one-ferroelectric-one-linear dielectric gate structure.[45, 46] However, as constrained by the intrinsic properties of the channel materials (conventional bulk semiconductors), these devices normally were explored to demonstrate enhanced multilevel memory states but without the ability performing any two-input Boolean logic functions.[44] Moreover, using the linear dielectric gate would result in a volatile electrostatic control, which fails to get rid of the static power consumption.[45, 46] Therefore, the presented working mechanism of our dual-gate 2D FeFET would hint at a different device operation principle which can efficiently address the abovementioned limitations found in the conventional dual-gate FeFETs. In addition, the efficient energy band profile control across the whole channel thickness direction would require a strong electrostatic coupling between the top and bottom gates and a very thin channel thickness.[34] This again emphasizes the advantages of the proposed dual-ferroelectric coupling to the atomically thin 2D semiconductors.

With the working mechanism for the dual-gate 2D FeFETs presented, we next demonstrate the structural and electronic properties of the devices. Here, model unipolar and ambipolar 2D FeFETs with MoS_2 and $MoTe_2$ as the active channels are studied, respectively. Practically, the direct integration of a 2D semiconductor channel with double ferroelectric gates is challenging since most 2D materials fail to withstand the high-temperature growth of conventional ferroelectric oxide films.[26] Thus, instead of using a ferroelectric oxide, we have turned to a polymer ferroelectric, *i.e.*, poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)), which in the past has manifested its excellent compatibility with 2D materials.[37, 38] Details of the fabrication process can be found in the Experimental Section and Figure S3 (Supporting Information). Devices constructed from various MoS_2 and $MoTe_2$ flakes were examined by Raman spectroscopy with a 532 nm excitation source, confirming the structural quality of the transferred 2D channel after the whole fabrication process, see Figure 1g. Microscopic structural properties of the dual-gate 2D FeFETs were further characterised using cross-sectional high-resolution transmission electron microscopy (HR-TEM), which indicates that the atomically-thin 2D TMD layers (bilayer for MoS_2 and trilayer for $MoTe_2$) between the top and bottom P(VDF-TrFE) polymers preserved their high single-crystalline quality with sharp interfaces, see Figure 1h.

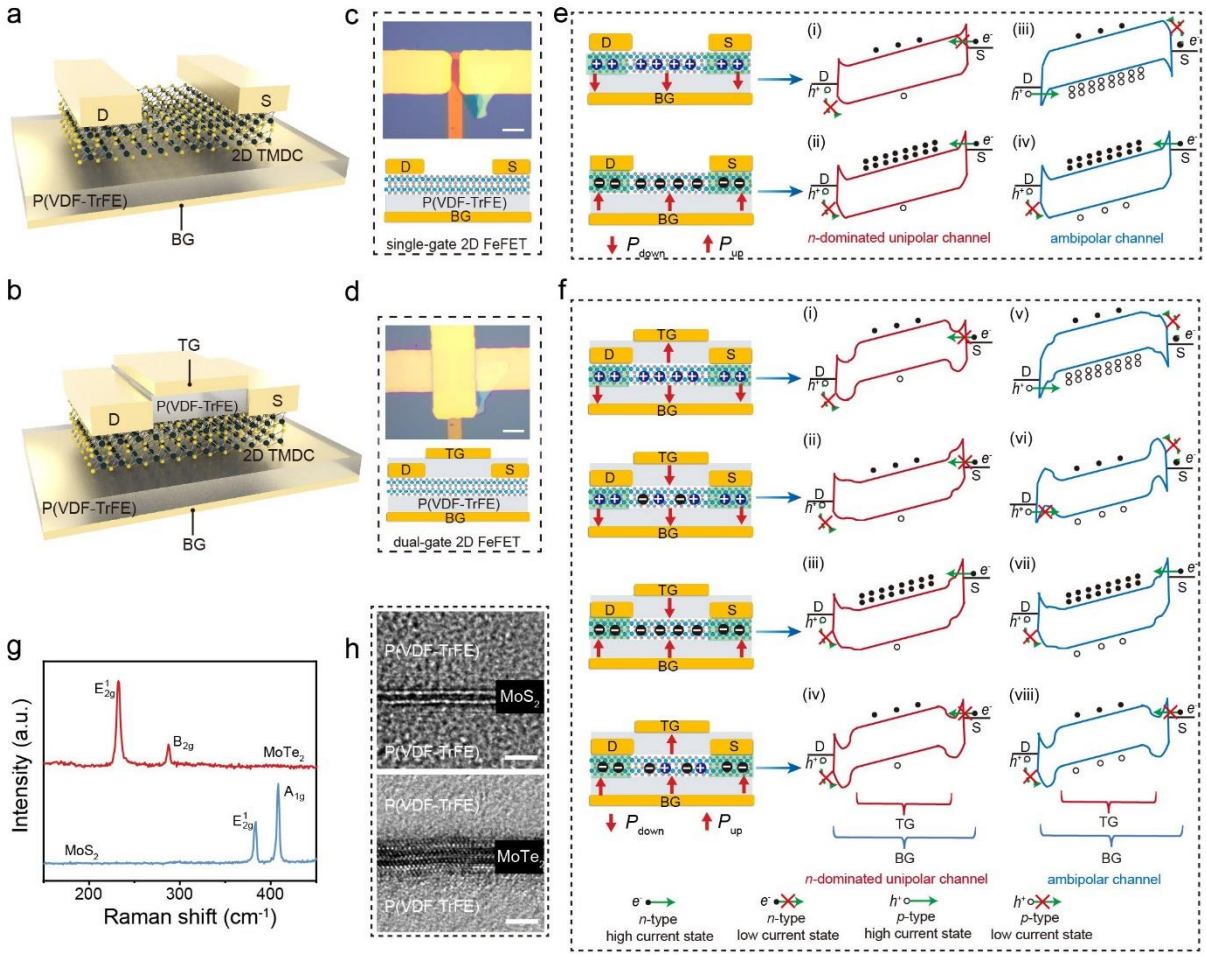


Figure 1. Device configuration and the underlying mechanism of the dual-gate 2D FeFETs. Schematic configuration of single-gate (a) and dual-gate (b) 2D FeFETs. Optical images of the representative back-gate (c) and dual-gate (d) 2D FeFET. Scale bar: 5 μm. Band diagrams for unipolar (e) and bipolar (f) 2D FeFETs with different polarisation states in the gate ferroelectric layer. The ferroelectric polarisation pointing towards/away from the channel results in electron/hole doping of the semiconductor. g) Raman spectra acquired from the MoS_2 and $MoTe_2$ flakes after capping with a top P(VDF-TrFE) layer. h) Cross-sectional HR-TEM images of the P(VDF-TrFE)/2D TMD/ P(VDF-TrFE) heterostructures. Scale bar: 2 nm.

To verify the demonstrated working mechanism for the proposed device, we measured the transport properties of both unipolar and ambipolar dual-gate 2D FeFETs (Figure 2). Transfer characteristics of these devices, *i.e.* gate voltage (V_g) dependent drain-source current (I_{ds}) were first measured with the TG and BG terminals short-connected ($V_g = V_{tg} = V_{bg}$) to reveal the unipolar and ambipolar electronic behaviours of the MoS_2 and $MoTe_2$ channels. As can be seen from Figure 2b,c, the MoS_2 FeFET demonstrates anti-clockwise I_{ds}-V_g hysteresis sweeping and the $MoTe_2$ FeFET shows anti-clockwise and clockwise hysteresis sweeping for *n*- and *p*-branch, respectively. Such hysteresis sweeping characteristics firmly prove that the electronic transport

properties of the 2D channels are controlled by the ferroelectric polarisation switching. It is obvious that the MoS_2 FeFET exhibits typical *n*-type memory behaviour with high (ON state, I_{on}) and low (OFF state, I_{off}) conductance states after applying positive and negative gate voltage (see Figure 2b), respectively. The ON/OFF ratio of the MoS_2 FeFET can be extracted from the transfer curve with the current at zero gate voltage (I_{on}/I_{off} at $V_g = 0$ V), which is around 10^5. In stark contrast to the sweeping behaviour of the unipolar MoS_2 FeFETs, a similar magnitude of the channel current under both positive and negative voltages has been observed in the $MoTe_2$ FeFET (see Figure 2c), indicating an excellent ambipolarity in the $MoTe_2$ channel.[39] We note that the ambipolar $MoTe_2$ FeFET exhibits a rather small ON/OFF ratio (~4) due to the similar electron and hole density.[47] However, this small ON/OFF ratio might lead to the degradation in the sensing margin for distinguishing the different logic states, which thus hinders the application of single-gate ambipolar FeFETs in memory-related applications. Interestingly, this problem can be tackled with the proposed dual-ferroelectric coupling effect by which the ambipolar $MoTe_2$ channel can be selectively engineered into non-volatile *p*- or *n*-type and results in specific two-input logic operations. More details can be found in the following discussions.

After discussing the basic electronic properties of the proposed dual-gate 2D FeFETs, we next illustrate the manipulation of the channel transport properties using the separated top and bottom ferroelectric polarisations, see Figure 2d. As shown in Figure 2e,f, the sole-TG controlled transfer curves of MoS_2 and $MoTe_2$ FeFETs exhibit distinct behaviours corresponding to different polarisation states in the bottom ferroelectric layer. Here, 10 ms wide positive and negative BG voltage pulses (that is, 20 V and -20 V for V_{bg}) were used to set the polarisation of the bottom P(VDF-TrFE) layer to P_{up} and P_{down}, respectively. Note that we grounded the TG terminal while applying the voltage pulses on the bottom gate to avoid the capacitance coupling of the double dielectric layers. For the unipolar *n*-type MoS_2 FeFET, the bottom ferroelectric polarisation state induces the horizontal shift of the TG-controlled hysteresis current sweeping, see Figure 2e. Specifically, only the configuration of P_{down} (top ferroelectric) and P_{up} (bottom ferroelectric) results in the ON state (of current at ~ 10^{-6} A) in the dual-gate MoS_2 FeFET, while the rest of the top/bottom polarisation arrangements all lead to a similar-level low current state with a high ON/OFF ratio of around 10^4. Obviously, the transport

behaviour of the devices under different configurations of top and bottom ferroelectric polarisations corresponds well with the energy band diagram analysis shown in Figure 1f(i)-(iv). As predicted before (see Figure 1f(v)-(viii) and related discussion), for the ambipolar $MoTe_2$ FeFET, the TG-voltage dependent transfer curves would exhibit switchable *n*- and *p*-type characteristics as controlled by the bottom ferroelectric polarisation, see Figure 2f. For the P_{down} in the bottom ferroelectric, the $MoTe_2$ FeFET only shows the *p*-type hysteresis behaviour with the electron conduction largely suppressed at positive V_{tg}. Conversely, *n*-type hysteresis behaviour can be obtained simply by switching the bottom ferroelectric to the P_{up} state. Clearly, the presented dual-ferroelectric controlled transport behaviour is fully consistent with the proposed working mechanism provided in Figure 1f. Note that above working principle only holds true when the 2D channels are thinner than their intrinsic screening length,[34, 48] where the complete depletion of the channel with either top or bottom ferroelectric polarisation is possible. With increasing the 2D channel beyond a critical thickness, the so-called "two-surface-channel" would result in distinct transport behaviour in dual-gate MoS_2 and $MoTe_2$ FeFETs,[34] see Supporting Information Note 8.

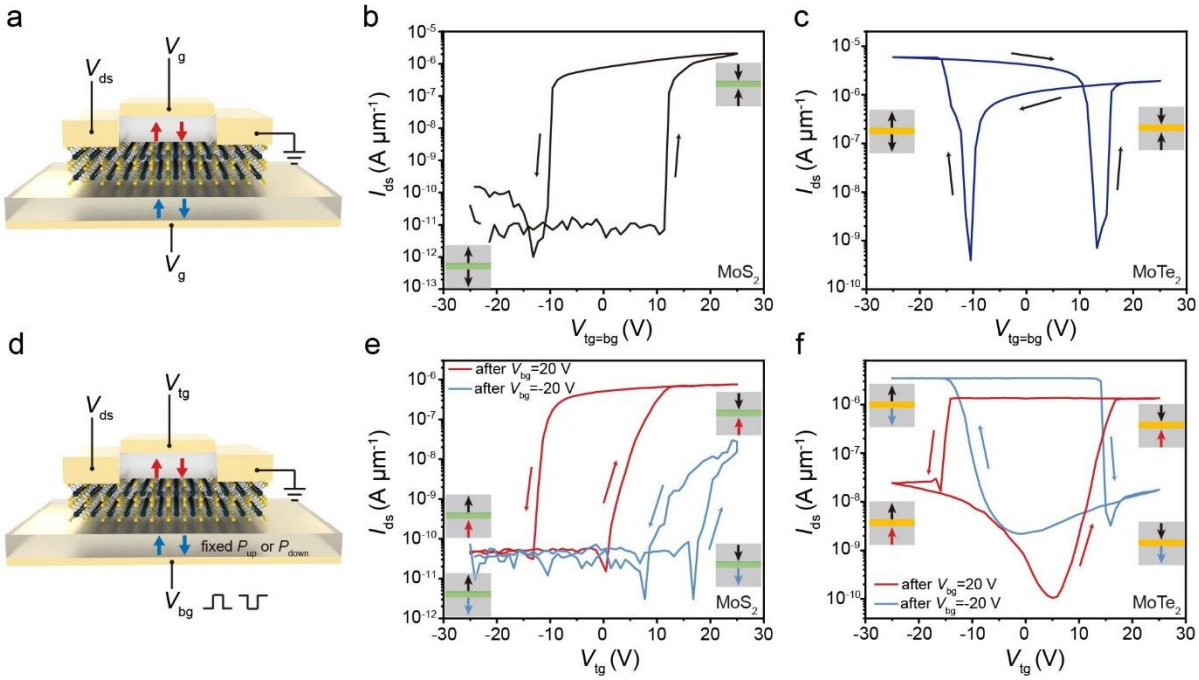
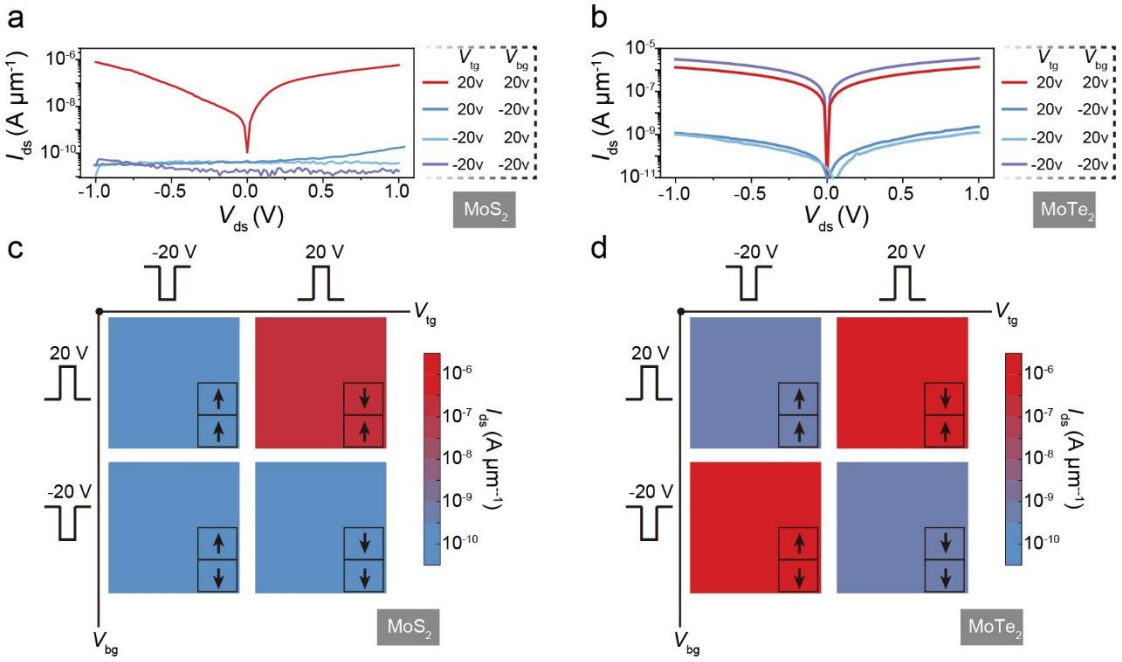


Figure 2. Transport properties for dual-gate 2D FeFETs. a) Schematic structure for the TG-BG short-connected scheme. Transfer curves of the MoS_2 (b) and $MoTe_2$ (c) dual-gate 2D FeFET with the gate voltage scheme shown in (a). d) Schematic for the dual-gate 2D FeFET under independent TG and BG voltage control. Voltage pulses of opposite polarities were applied on the BG to set the polarisation states in the bottom ferroelectric layer. Top-gate bias dependent

I_{ds} with the bottom P(VDF-TrFE) layer under opposite polarisation states for MoS_2 (e) and $MoTe_2$ (f) FeFETs.



e

Logic input (IN1,IN2)		MoS_2		$MoTe_2$	
V_{tg} (IN1)	V_{bg} (IN2)	Majority carrier type	Current state (Logic output)	Majority carrier type	Current state (Logic output)
-20 V (0)	-20 V (0)	*not applicable*	off (0)	h^+	on (1)
-20 V (0)	20 V (1)	*not applicable*	off (0)	*not applicable*	off (0)
20 V (1)	-20 V (0)	*not applicable*	off (0)	*not applicable*	off (0)
20 V (1)	20 V (1)	e^-	on (1)	e^-	on (1)

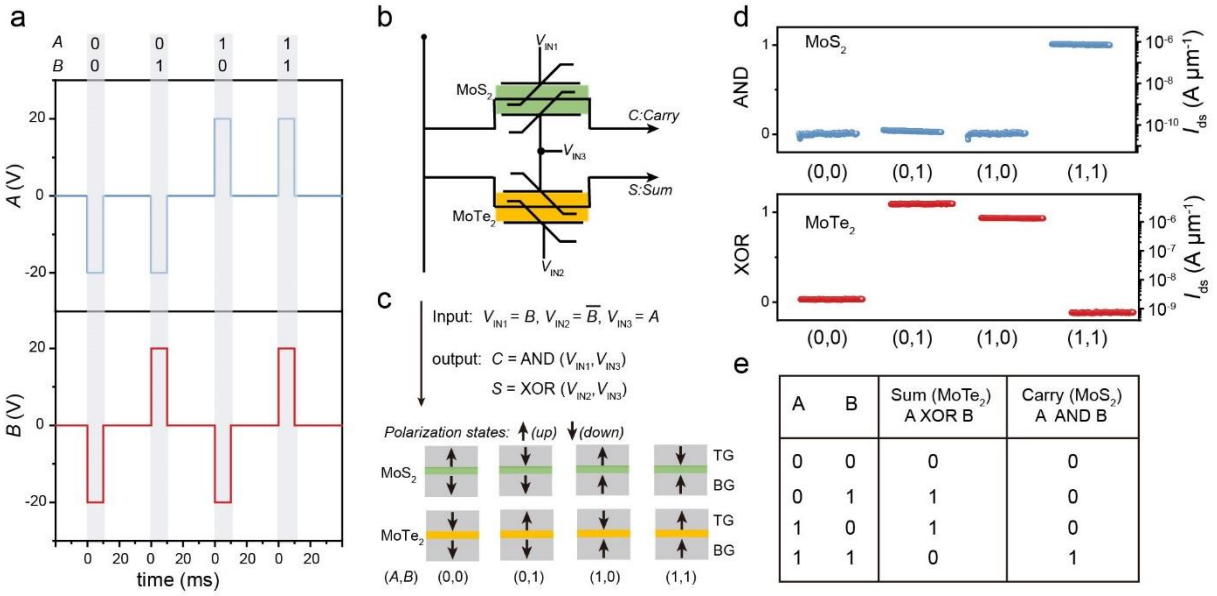
Figure 3. Demonstration of non-volatile logic gates with a single dual-gate 2D FeFET. Output characteristics for MoS_2 (a) and $MoTe_2$ (b) FeFETs after applying different voltage pulses to the TG and BG. Extracted current levels for MoS_2 (c) and $MoTe_2$ (d) FeFETs under different top and bottom ferroelectric polarisation states. e) Truth table for non-volatile AND and XNOR logic gates based on MoS_2 and $MoTe_2$ dual-gate FeFETs.

As demonstrated above, the four conductance states generated by different combinations of the polarity of top and bottom ferroelectric polarisations would naturally hint at two-input Boolean logic operations. Next, we show that non-volatile logic gates can be realised with a single dual-gate 2D FeFET structure using the V_{tg} and V_{bg} as two input parameters and the channel conductance as the logic output. 10 ms long +/-20 V voltage pulses for V_{tg} and V_{bg} were used with the source contact grounded to ensure the complete polarisation switching of the ferroelectric P(VDF-TrFE) layer. Figure 3a,b depicts the output characteristics of the MoS_2 and $MoTe_2$ transistors under different arrangements of the directions of top and bottom ferroelectric

polarisations. Note that the dual-gate voltage pulses of different combinations of polarities were simultaneously applied on the TG and BG. To better illustrate the diverse transport behaviours of the 2D FeFETs, non-volatile drain current levels with respect to different combinations of polarisations in the top and bottom ferroelectrics have been mapped in Figure 3c,d. Obviously, the output conduction levels of MoS_2 and $MoTe_2$ FeFETs can both be divided into two distinct categories with a high ON/OFF ratio (that is, ~10^4 and ~10^3 for MoS_2 and $MoTe_2$ devices, respectively), see Figure 3c,d. Note that all the conduction states for both MoS_2 and $MoTe_2$ FeFETs showed excellent retention with negligible variation up to 1000 s, proving their stable non-volatile memory capability (see Figure S10 in Supporting Information). Here, the excellent retention of the insulating state in our 2D FeFETs may be due to the large capacitance of the ultrathin 2D channels and its capacitance matching with the adjacent P(VDF-TrFE) layers.[49]

Based on the ON and OFF conductance states subject to top- and bottom-ferroelectric polarisations in the dual-gate 2D FeFETs, we can now construct a truth table showing the two-input logic-in-memory operations, see Figure 3e. In the proposed logic gates, the two input states IN1 and IN2 are represented by the voltage pulses simultaneously applied to the top and bottom ferroelectric (that is, V_{tg} (IN1) and V_{bg} (IN2)), respectively, and the non-volatile current levels (I_{ds}) are used as the output logic states. Specifically, 20 V and -20 V input voltage pulses are defined as the digital input "1" and "0", and the input voltage-determined ON and OFF conduction states feature the output logic states of "1" and "0", respectively. With such a logic gate scheme, we can deduce that the (IN1, IN2)-determined input logic states (0, 0), (0, 1), (1, 0) and (1, 1) will result in the output logic states of "0", "0", "0" and "1" for MoS_2 devices, and "1", "0", "0" and "1" for $MoTe_2$ devices. The results are summarised in Figure 3e with the dual-gate MoS_2 FeFETs manifesting the AND logic behaviour and the $MoTe_2$ FeFETs showing the XNOR logic function, respectively. Considering that the logic output-conductance state of the FeFETs has a long retention, the logic gates can thus be regarded as "non-volatile", allowing for virtually zero off-power consumption as they can keep the logic states in the fashion of the memory.[14, 17] Compared with conventional CMOS-based logic gates, the presented single-transistor logic gates can significantly reduce the involved transistor number and thus improve the circuit area-efficiency; for example, the state-of-art logic gate design with 2D MOSFETs would require 11 and 5 transistors for XOR and AND logic gates,[50] respectively. Moreover,

unlike most two-terminal memristor-enabled logic-in-memory devices featuring a multistep sequential logic operation,[2, 4, 14, 17] the logic operations in the proposed dual-gate FeFETs can be completed within the same clock pulse. These properties thus make the dual-gate 2D FeFETs superior in terms of time- and area-efficiency for logic-in-memory. Beyond the demonstrated AND/XNOR logic gates, we also found that dual-gate MoS_2 FeFETs with thicker channel thickness can instead perform OR logic operations (Figure S12 in Supporting Information), which may further enrich the device functionalities by exploiting the thickness-related properties of 2D TMDs. We note that the realisation of a low operating voltage and high speed is a critical challenge for the NVM fabrication technologies, the related material and device optimisation for such a goal would be an art in itself. The demonstrated proof-of-concept device with ferroelectric P(VDF-TrFE) would require a large switching voltage and long switching time as limited by its intrinsic ferroelectric switching mechanism. However, the switching speed of the proposed device concept can be significantly improved by using inorganic ferroelectrics. For example, it has been reported that Si-compatible hafnia-based ferroelectrics can be operated with ultrafast sub-ns switching speed and with very low operating voltage.[51] This indicates that future optimisation of the proposed device with suitable ferroelectric materials would further achieve comparable operating voltage scheme with the conventional SRAM and DRAM.[28]



A	B	Sum ($MoTe_2$) A XOR B	Carry (MoS_2) A AND B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 4. Demonstration of the non-volatile half-adder circuit based on the integration of two dual-gate 2D FeFETs. a) Input voltage waveforms for the logic operation. b) Circuit diagram for the half-adder with integrated MoS_2 and $MoTe_2$ FeFETs. c) Relationship between the logic inputs and the polarisation states in both ferroelectric layers for MoS_2 and $MoTe_2$ FeFETs. d)

Output conduction states showing AND and XOR type logic operations. e) Truth table for a non-volatile half-adder circuit.

To further explore the potential of the dual ferroelectric-gate 2D transistors for low power and high-area-efficient computational circuits, we show that a non-volatile logic half-adder with only two transistors can be constructed using the heterogeneous integration of the dual-gate MoS_2 and $MoTe_2$ FeFETs, see Figure 4. The waveform for the half-adder operation comprising the *A* and *B* logic input variables is presented in Figure 4a, where the logic inputs "0" and "1" correspond to 20 V and -20 V voltage pulses (10 ms in duration), respectively. As shown in Figure 4b,c, the half-adder circuit is made possible by adding a common input $V_{IN3} = A$ to the BGs of both devices, while the input signal at TG is $V_{IN1} = B$ for MoS_2 and $V_{IN2} = -B$ for $MoTe_2$ FeFETs, respectively. In a realistic integrated circuit design, the BGs shown here can be used as the global gate shared by multiple 2D FeFETs, which would eliminate extra area consumption for BG connects. With the proposed circuit scheme, the dual-gate MoS_2 FeFET can operate as an AND logic gate to generate the Sum signal and the second $MoTe_2$ FeFET is used as an XOR logic gate producing the Carry value. The device current states after different combinations of *A* and *B* input pulses and the simulated output logic states are summarised in Figure 4d,e, which clearly shows that the half-adder function has been successfully implemented using the proposed two-transistor structure. Note that a half-adder circuit using conventional 2D MOSFETs would require 16 transistors,[50] and that based on two-terminal memristors would consume up to 8 devices in cascading to complete the desired functionalities, see Figure S1 (Supporting Information).[52] Overall, compared with the existing technologies for logic gates, the proposed non-volatile logic gates with dual-gate 2D FeFETs have shown advantages of reduced circuit complexity, static power dissipation and transistor numbers.

So far only the binary conductance transition of the 2D FeFETs has been exploited for constructing digital in-memory computing (logic-in-memory) cells. It is well known that the circuit for such digital in-memory computing would require a different design from that of the analog in-memory computing, and the later actively exploits a crossbar array structure to perform matrix-vector multiplication.[2] In fact, a single two-input non-volatile Boolean logic gate would require the combination of several resistive switching devices, hindering mapping

it into the crossbar structure.[2, 33] This problem can be tackled by embedding a single 2D FeFET into the crossbar in which the individual FeFET can act as logic gate as well as synaptic weight update cell (see Supporting Information Note 1). We now illustrate that the functionalities of the 2D FeFETs can be further extended to realise artificial synapses, manifesting the multifunction nature of the proposed device concept for different in-memory computing schemes. In a biologic neural network, the reconfiguration of the connection strength of synapses (synaptic plasticity) between neurons provides the biologic system with learning and memory functions for processing cortical information.[8] More specifically, the flow of information through a biologic synapse is achieved by the gradual release and transmission of neurotransmitters from the pre-synaptic to post-synaptic neurons caused by the spiking action potential, see the schematic illustration in Figure 5a. Therefore, the equivalent electronic element to the synapse would exhibit multi-level conductance switching in a non-volatile fashion reminiscent of the biologic synaptic plasticity.[2] In the FeFETs (Figure 5b), the channel conductance states are expected to be sensitively coupled to the relative fraction of the mixed upward- and downward-polarised ferroelectric domains, since the overall polarisation determined by the percentage of up/down domains would lead to multi-level hole/electron doping in the adjacent channel areas. Thus, the devices can exhibit memristive multi-level conductance switching corresponding to the voltage-controlled domain configuration evolution. We next verify whether such mixed-domain configuration exists in the ferroelectric film covered with the 2D TMD layer by locally tuning the domain states in the 2D TMD/ferroeletric heterostructure, see Figure 5c. By applying a set of suitable voltage pulses on the MoS_2 flake through the probe tip of the piezoresponse force microscopy (PFM) system, the underneath P(VDF-TrFE) layer clearly exhibits a gradual domain evolution from uniformly downward- to upward-domain, which comprises various intermediate mixed-domain states in between (Figure 5c). Note that the mixed-domain state is expected to be stable with minimal relaxation as the depolarisation energy is smaller than that of the single-domain state, thus resulting in a stable non-volatile conduction state for memristive FeFETs.[53] Based on the observed mixed-domain configuration, we can now expect the analog conductance switching in the 2D FeFETs. As can be seen from Figure 5d, both MoS_2 and $MoTe_2$ transistors exhibit the analog conductance tuning as a function of the applied TG voltage pulse numbers. Note that it normally

requires only one single gate to operate the ferroelectric-based synaptic transistors (see Figure 5b),[21, 29] we thus set the bottom ferroelectric layer fixed at the P_{up} state while manipulating the memristive conductance *via* the TG voltages. As can be seen from Figure 2e,f, both MoS_2 and $MoTe_2$ devices are operated as an *n*-type FeFET. 10 V and -10 V TG voltage pulses of 500 μs are used for conductance increase and decrease, respectively. The obtained conductance switching features the key behaviour of a synaptic transistor, that is, pulse number dependent long-term potentiation (LTP) and depression (LTD), unambiguously proving the potential of 2D FeFETs as artificial synapses.[29] Further analysis of the effective conductance levels and linearity in the LTP/LTD weight updates, which is crucial for the performance of their applications in artificial neural network (ANN), can be found in Supporting Information Note 10. Note that the short-term plasticity (STP) which could describe the temporal modulation of the synaptic connection was not achieved with our device (see Supporting Information Note 9). This can be attributed to the non-volatile polarisation switching and stable mixed-domain state in the ferroelectric layers.[21] In fact, STP would be a key function to enable the emulation of biologic neuromorphic system along with the demonstrated long-term plasticity as shown in Figure 5d. A possible route to realise the STP in the FeFETs would be engineering the semiconductor channel properties as reported very recently.[54] Thus, further efforts would be needed to diversify the synaptic functionalities of the proposed FeFETs *via* using multifunctional semiconductor channel materials.

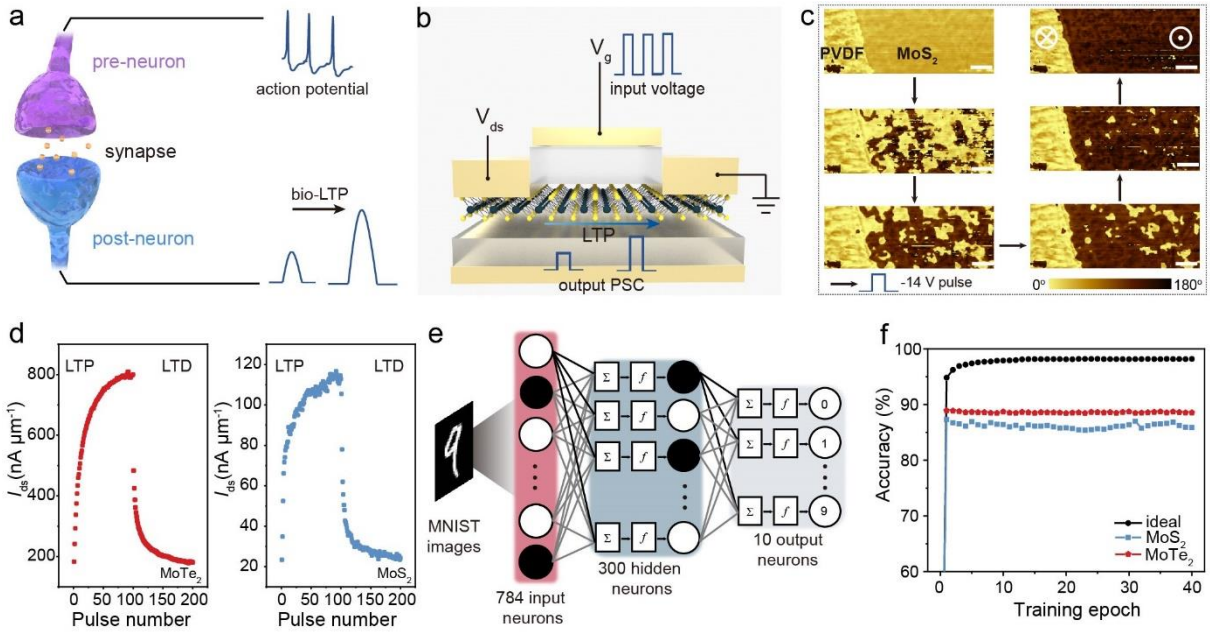


Figure 5. Device properties of the 2D ferroelectric synaptic transistors and system-level simulations of pattern recognition. a) Sketch of a biologic synapse showing the signal transmission. b) Single-gate 2D FeFET device configuration used as a synaptic transistor, the conductance can be referred as postsynaptic current (PSC). c) Locally probing the voltage-induced domain pattern evolution in a MoS_2/P(VDF-TrFE) device. Voltage pulses of -14 V and 50 ms were applied through the PFM tip. PVDF refers to the P(VDF-TrFE). Scale bar: 0.25 μm. d) LTP and LTD properties as a function of TG voltage pulse numbers for MoS_2 and $MoTe_2$ synaptic transistors. e) Schematic illustration of a three-layer (one hidden layer) neural network for recognition tasks. f) Simulated pattern recognition accuracy as a function of training epochs of MoS_2 and $MoTe_2$ synaptic transistors in comparison with the ideal case.

Based on the measured characteristics of the MoS_2 and $MoTe_2$ synaptic transistors, we further carried out simulations to perform the supervised learning of an ANN based on the back propagation algorithm. For the simulation, the Modified National Institute of Standards and Technology (MNIST) handwritten digits dataset has been used.[55] The simulation was performed using the CrossSim platform,[56, 57] a three-layer network (one hidden layer) with 784 input neurons, 300 hidden neurons and 10 output neurons was chosen, see the schematic diagram in Figure 5e. The 784 neurons of the input layer correspond to the 28 × 28 (pixels) MNIST image and the 10 output neurons correspond to 10 classes of digits from 0 to 9. Here, the 2D synaptic transistors are used as the individual memory element in a quasi-crossbar array for matrix operations as detailly explained in the CrossSim platform,[56, 57] and their conductance states have been adopted as the synaptic weight updates for executing the back propagation. The circuit diagram of a synapse layer compromising of $M \times N$ dual-gate 2D FeFET-based crossbar structure is shown in the Supporting Information note 11. As shown in Figure 5f, training of the ANN using MoS_2 and $MoTe_2$ synaptic transistors results in a similar classification accuracy of 86% and 88% after 40 training epochs, respectively. For comparison, the ideal CMOS recognition accuracy are also shown here, which approach the neuromorphic algorithm limit (~98% accuracy after 40 training epochs) and benchmark the performance of realistic device performance. Note that although the 2D synaptic transistors have a slightly lower classification accuracy than the ideal case, they are still comparable to the state-of-art non-volatile memories,[29, 58, 59] and can be further enhanced by improving the material properties and/or using different voltage pulse schemes.[29] The presented emulation of synaptic functionalities at the device level and simulation of ANN at the system-level together indicate the outstanding

performance achieved using the proposed 2D FeFETs in pattern recognition. Therefore, by simply setting the bottom-ferroelectric polarisation fixed, the dual-gate 2D FeFETs can operate in a single-gate mode with the performance comparable to conventional single-gate synaptic transistors. Taking advantage of the feasibility of switching the dual-gate 2D FeFETs between single- and dual-gate schemes, the proposed device concept has exhibited a high degree of reconfigurable functionality for logic and synaptic operations and is thus well suitable as a universal structure for both digital and analog in-memory computing.

CONCLUSIONS

We have shown that multifunctional in-memory computing capable of both digital- and analog-computation can be realised using the proposed dual-gate 2D FeFETs. Non-volatile AND, OR and XNOR logic gates have been realised *via* exploiting the dual-ferroelectric coupling effects and the ferroelectrically-controlled polarities of the 2D TMD channels. Compared with other NVM-enabled logic-in-memory devices, in which the cascading of multiple devices and/or sequential computing are required, the presented dual-gate 2D FeFETs can perform logic operations with a single-transistor structure with a one-clock cycle, thus featuring an area- and time-efficient circuit design. The half-adder, an important building block in modern processors, has also been successfully implemented by combining two dual-gate 2D FeFETs. Furthermore, memristive switching that can emulate the synaptic plasticity was identified in the proposed 2D FeFETs. Based on such synaptic properties, an ANN simulation at the system level has been conducted showing the high performance with ~88% recognition accuracy of MNIST handwritten digits. Overall, these results suggest that the proposed dual-gate 2D FeFETs would raise a highly promising device concept for non-volatile logic gates and artificial synapses, thus they are particularly amenable to next-generation low-power and high-area-efficient in-memory computing hardware.

METHODS

Device Fabrication. 2D MoS_2 and $MoTe_2$ flakes were mechanically exfoliated onto the polydimethylsiloxane (PDMS, Gel-Pak$^{@}$) supports using the Scotch tape method. Corresponding bulk TMD crystals were purchased from HQ Graphene. The TMD flakes of

interest were first identified on the PDMS by the optical microscope before the transfer process. Source and drain contacts were fabricated through dry-transfer of the Au metal layers of photolithography-define shape onto the 2D channels. Three-layer P(VDF-TrFE) (70:30 in mol%) thin films (~150 nm in thickness) as both top and bottom dielectric layers were made by repeating the sol-gel spin-coating process for 3 times. The parameters for the spin-coating were 3000 rpm and 30 s for each cycle. The P(VDF-TrFE)/2D channel/ P(VDF-TrFE) structures were finally annealed at 135 ℃ in vacuum for 6 h. A detailed fabrication flow of the dual-gate devices is also schematically shown in Figure S3, Supporting Information.

Characterizations. All the electrical measurements were carried out using a Keysight B2902 source-meter. The current of all devices was recorded with V_{ds} of 1 V for all the measurements in this work unless stated otherwise. For all the transfer curve measurements, the gate voltage scanning speed is around 0.9 V/step. Raman spectra were acquired using the WITEc Alpha 300R with a 532 nm laser at 1 mW. Scanning probe microscopy (SPM) measurements were performed using a commercial atomic force microscopy (AFM) system (AIST-NT Smart SPM 1000) under ambient atmosphere. Conductive platinum-coated tips (Mikromasch HQ: NSC35/Pt) with a force constant of ~5 N/m and a tip radius less than 30 nm have been used for all imaging modes. DC voltages were directly applied to the tip. The domain structures were acquired using PFM mode with the tip directly scanning on the MoS_2 electrode. All the PFM measurements were performed at an AC imaging bias of 2.0 V (peak to peak) with a frequency in the range of 1000-1200 kHz. TEM specimens were prepared by Focused Ion Beam (FIB) milling (FEI Helios NanoLab 600i). HR-TEM characterisation was carried out on a probe aberration-corrected JEOL JEM-ARM200F with an Oxford X-MaxN 100TLE spectrometer, operated at 200 kV.

Neural Network Simulation. The performance of the ANN using the 2D transistor electrical characteristics was simulated based on the CrossSim platform in the Python environment.[56] It was implemented in a quasi-cross bar structure as detailed in the CrossSim platform. For the 28 × 28 (pixels) MNIST image, the network size was 784 × 300 × 10. At each epoch, the ANN was trained on patterns from a 60000-image training dataset, and the recognition accuracy was tested a separate 10000-image testing dataset.[56, 57]

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at the ACS Publications website.

Comparison of the device number for logic gates and mapping the 2D FeFETs into the crossbar;

Fabrication process for the dual ferroelectric-gate 2D transistors; Ferroelectric properties of the dual-gate 2D FeFETs; Drain-source voltage-controlled transfer curve properties and the fatigue properties of the FeFETs; Electronic properties of a bottom-gate $MoTe_2$/P(VDF-TrFE) FeFET; Non-volatile memory states in the dual-gate controlled 2D FeFETs; HRTEM images of the 2D channels; The channel thickness effect for polarisation modulation of 2D channel conductance; Discussion on the STP and LTP synaptic behaviours; Analysis on the LTP and LTD characteristics of the synaptic transistors; Details of the ANN simulation (Supplementary Notes 1-11).

AUTHOR INFORMATION

Corresponding Authors

*Email: xdliuyan@xidian.edu.cn;
*Email: xuetaogan@nwpu.edu.cn

Notes

The authors declare no competing financial interest.

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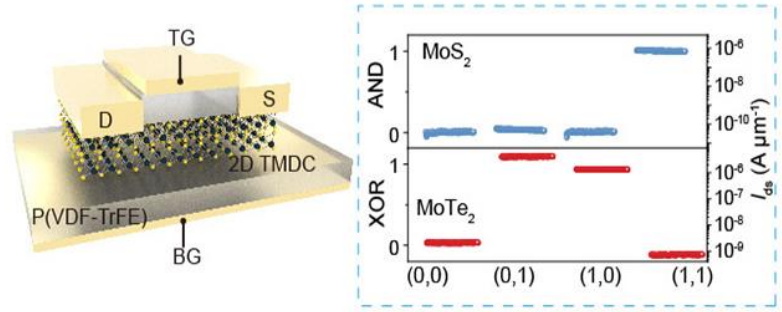
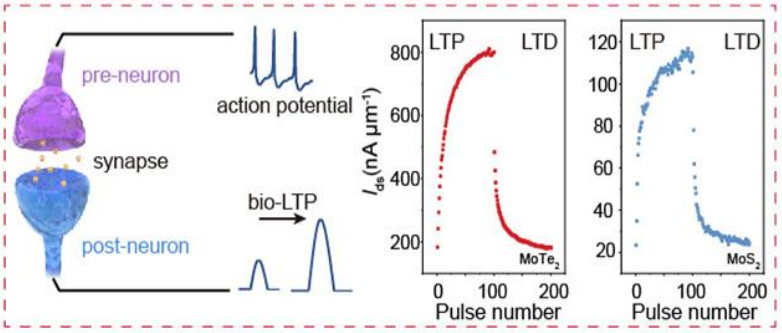


non-volatile logic gate and artificial synapse within a single transistor



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