High Voltage 3-Dimesional Partial SOI technology platform for Power Integrated Circuits

Marina Antoniou, Florin Udrea, Elizabeth Kho Ching Tee, Alex Hölke

***Abstract*— Partial SOI (PSOI) is a widely recognized technology suitable for High Voltage (HV) architectures for Power Integrated Circuits (PICs). Despite the added process complexity compared to SOI RESURF, this technology offers a wider range of voltage ratings due to the action of the depletion layer in the Handle Wafer (HW), reduced parasitic capacitances due to the extra volume of the depletion region in the HW and better heat conduction due to thinner buried oxide layer. The newly developed platform technology, featuring 3-dimensional designs to fully utilize the PSOI potential, is particularly relevant to the manufacturing of high voltage integrated circuits (HVICs) where low on-state resistance and reduced self-heating are essential requirements. This work presents a PSOI technology platform with voltage ratings ranging from 45 to 400V while providing low on-state resistance, good hot carrier injection stability as well as Electrostatic Discharge (ESD) capability of the HV devices. For example, for a 375V rated LDMOSFET, this technology achieves an on-state resistance of 1435mΩ.mm^2, an over 50% improvement compared to the state-of-the-art SOI technologies while maintaining competitive reliability.**

***Index Terms*— SuperJunction, MOSFET, Partial-SOI, Power Integrated Circuits, Reliability.**

I. Introduction

Efficient and reliable Power Integrated Circuits (PICs) have been a subject of intense research from both industrial and academic communities. The aim is to develop PICs that can handle high voltage, high current, or a combination of both, leading to significant improvements in reliability, reductions in size, weight and cost thus enabling the integration of PICs in portable, automotive and consumer products, and aerospace applications.

There are two main PIC technologies that are currently employed each with its own limitations in terms of performance and reliability; (i) the Junction Isolation (Bulk technology) is based on a RESURF effect whereby the substrate supports part of the voltage during the blocking mode. This technology has the drawback of slow switching speeds because the substrate is open and minority carriers can be injected deep down which makes their removal during turn-off very slow (e.g. in the case of body diode conduction). (ii) The SOI (Silicon on Insulator) technology is based on having deep trenches filled with oxide which reach the buried oxide layer (BOX) for effective isolation between devices. The utilization of SOI in PICs, is very beneficial in many aspects such as low cross-talk, latch-up suppression, and very low leakage currents. SOI power devices however suffer from reduced breakdown voltage, increased self-heating and increase fabrication costs compared to their bulk counterparts [1].

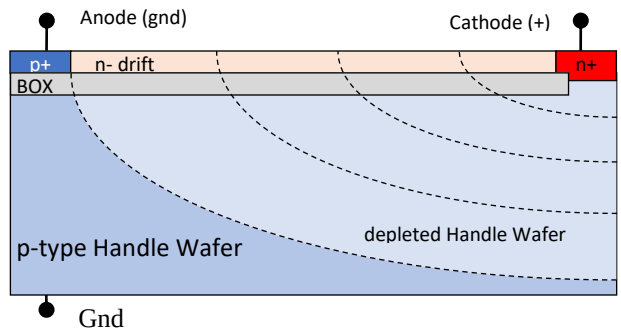

Fig. 1. Schematic Cross-Section of a classic PSOI lateral HV diode in reverse bias

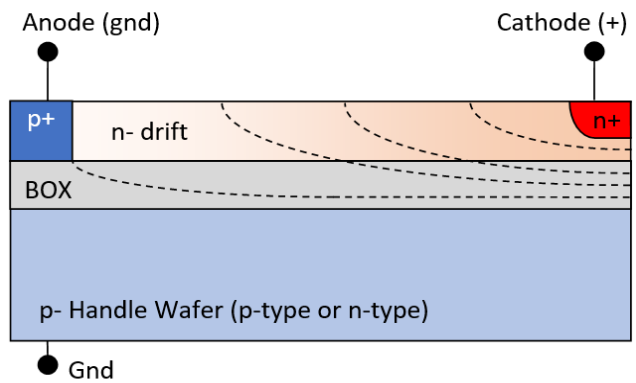

Fig. 2. The thin SOI diode with the potential vertically supported in part by the Top Silicon and the BOX. The HW acts as field plate and linear doping profile yields a laterally uniform electric field distribution.

To overcome these problems while maintaining good isolation between the low power CMOS circuits and high-power cells, the idea of using the partial SOI (PSOI) technology was proposed. Devices based on this technology have part of the buried oxide layer etched and refilled with a conductive material to connect the Handle Wafer (HW) to the Top Silicon, when used as a high voltage (HV) device architecture. The PSOI utilizes a reverse-biased junction

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depleting part of the HW under the device to support the High Voltage vertically (Fig. 1) [2]. In this technology there are no hard limits on the layer thickness of the BOX nor on the Top Silicon. This contrasts with the SOI RESURF (or thin SOI) where the high voltage is shared between the Top Silicon and the BOX (Fig. 2) [3], [4]. It is also different from very thick SOI where the supported voltage is dropped mainly within the Top Silicon. Indeed, the PSOI BOX can be made considerably thinner [5] allowing better heat dissipation and significantly reducing the self-heating effect. PSOI substrates are hence a viable high voltage alternative to thick buried oxide SOI substrates, which are more expensive, thermally inferior and difficult to manufacture due to wafer bowing and stress. In addition, PSOI devices have smaller parasitic capacitance due to the extra volume of the depletion region created within the HW, which enables fast switching. PSOI is closer in performance to the Membrane Technology [6] where the substrate effect is eliminated by completely removing the HW under HV device. However, it is free of the additional challenges of the latter such as mechanical fragility and thermal management considerations. Therefore, the PSOI has a tremendous potential and provides a major direction to be pursued for the development of the next generation of PICs. Nevertheless, this is not yet a well-established technology and the achievement of its full potential are yet to be realized.

II. State Of The Art REVIEW OF PARTIAL SOI TECHNOLOGIES

A. History and Commercial Implementations

The PSOI idea has been in fact around for many years. An early publication of a PSOI structure for a HV LDMOS goes back to 1989 by K. Shinchi from Fujitsu [7]. In 1990, the team of E. Arnold, S. Merchant and P. Shackle of Philips Co. filed a patent on PSOI [2] with focus on thicker SOI and a fully dielectrically isolated HW diode. Lateral Insulated Gate Bipolar Transistors (LIGBTs) and Superjunction (SJ) devices in PSOI were initially proposed in [7, 8, 9]. Over the years the topic was investigated by several academic teams and their achievements include the LEGO (Lateral Epitaxial Growth over Oxide) process [10].

Furthermore, Infineon Technologies first published work on a 600V PSOI technology in 2006 [11]. By 2017 the technology had matured, and Infineon Technologies is currently producing gate driver ICs up to 1200V operating

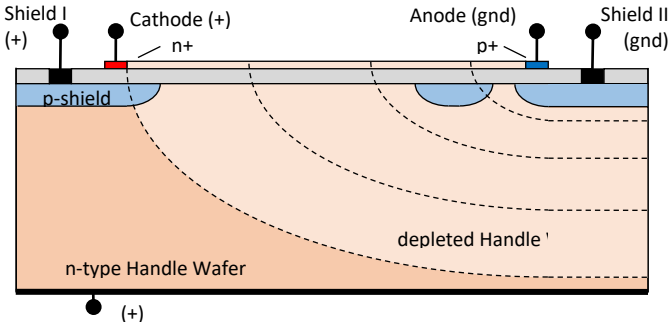


Fig. 3. Thin PSOI technology with n-type HW and metallic HW contacts [10].

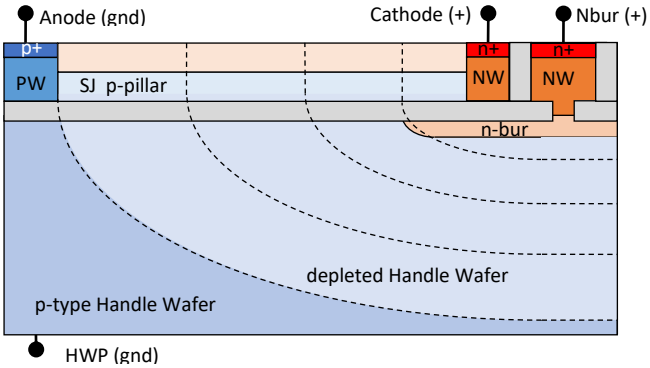


Fig. 4. The pSOI SJ technology as presented in this work.

voltage (Fig. 3). The underlying technology features a 0.4µm BOX, which compares well to the 12µm or so BOX thickness required for an equivalent SOI RESURF technology [12]. One of the challenges of this technology is that the substrate is n-type and requires a positive voltage applied (rather than ground) to enable the depletion region to expand in the HW. The positive voltage on the substrate needs to be carefully isolated from a grounded heat sink. X-FAB is currently offering an 180nm SOI technology with a PSOI option up to 200V [13], [14], [15] and has recently released the 400V rated devices. This technology is based on a p-substrate with the substrate sitting at a ground potential and therefore attaching a heat sink, or heat convection materials (such as Copper) is straightforward.

B. Applications

The PICs application range (100V up to 1kV) is very large and is constantly expanding. In particular, applications for ICs requiring operating voltage rating of 140V to 200V are piezoelectric (e.g. medical ultrasound) and capacitive actuators. Light Detection and Ranging (LiDAR) technology also requires very fast devices in that space. Subscriber Line Interface Circuits (SLIC) and increasingly battery management systems (BMS) are also targeting this range. With the advent of the 48V standard for automotive board net, DC to DC converters or battery chargers also require voltages in excess of 100V and below 500V.

Power supplies for the 220-230V grid traditionally require rather high operating voltage up to 800V. This stems from the commonly used fly-back converter architecture, with internal reflections resulting in such high voltage overshoot. However, with new more complex architectures with integrated power supplies using multiple floating switches, there is no internal overvoltage requirement and the voltage rating can thus be safely set to maximum voltage of 375V [15]. In addition, the loop inductance in integrated PICs is also very small, therefore there is practically no voltage overshoot from the gate driver to the power switches and hence, no additional overvoltage requirements. Therefore, a 400V rating is sufficient for many power supply architectures.

Furthermore, early adapters of the technology are targeting integrated power supplies for IoT for power of the order of 500mW [16] and up to 65W [17].

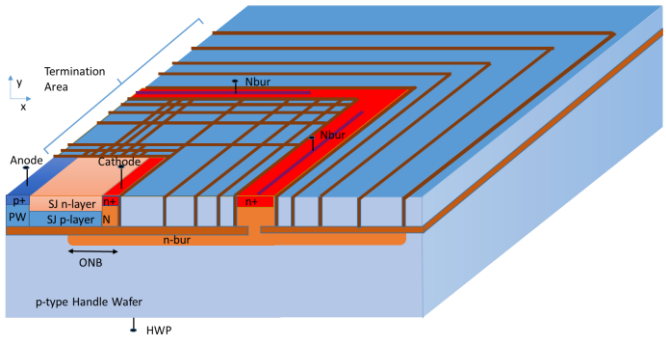


Fig. 5. The proposed 3D PSOI SJ technology (not to scale)

III. The 100-400V Partial SOI Platform Technology

In this paper, we present the 180nm SOI platform process "XT018" developed and commercially available by X-FAB with focus on the 400V voltage extension. In the next sections we will be presenting the design features (active and termination area) and the optimization approach used for this technology through simulations and experimental results. Earlier experimental results can be found in [13],[14],[15].

A. Device Fabrication and Simulation

The drift region of the active area features a SJ configuration. Unlike in a thin SOI case, where the drift region SJ charge balance is affected by the charge distribution in the back side of the BOX [18], the PSOI lateral SJs are practically charge-balanced; this is due to the fact that the junction formed with the HW removes the field-plate effect created by the substrate potential and the BOX [19]. In other words, by keeping the p-type HW contact grounded and forward biasing the top side Nbur contact (as shown in Fig. 4) the HW is depleted under the active device area, which removes any mobile charge under the BOX/drift region area. The PSOI SJ is thus inherently voltage-scalable by drift length variation alone and the SOI RESURF limitation [4] does not apply. Therefore, there is no physical limitation to increasing the voltage range from 200V to 400V (and above). The ultimate limit of this voltage is determined by the vertical breakdown at the junction between the n-bur layer and the HW. This depends on the doping of the HW and the shape of the actual junction. Extensive 2D TCAD simulations were initially carried out, however, in order to tackle the highly complex 3-dimensional interaction of the SJ, the termination area and the HW diode, advanced 3D simulations were utilized.

For the basic principle of PSOI to work, the Anode and Cathode of the Top Silicon HV diode potential lines must be aligned with the Anode and Cathode of the HW diode, (as shown in Fig. 4). If this condition is to be satisfied, the device lateral drift length (pitch) should be made significantly longer. This however directly affects the area-specific on-resistance (Ron). To achieve a low Ron with small anode-cathode pitch, both terminals of the HW diode are realized in the 3rd dimension as can be seen Fig. 5. This figure shows a schematic representation of the proposed 3D PSOI SJ technology. Table I shows the device parameters for the 375V rated device and Fig. 6 shows the simulated 3D structures.

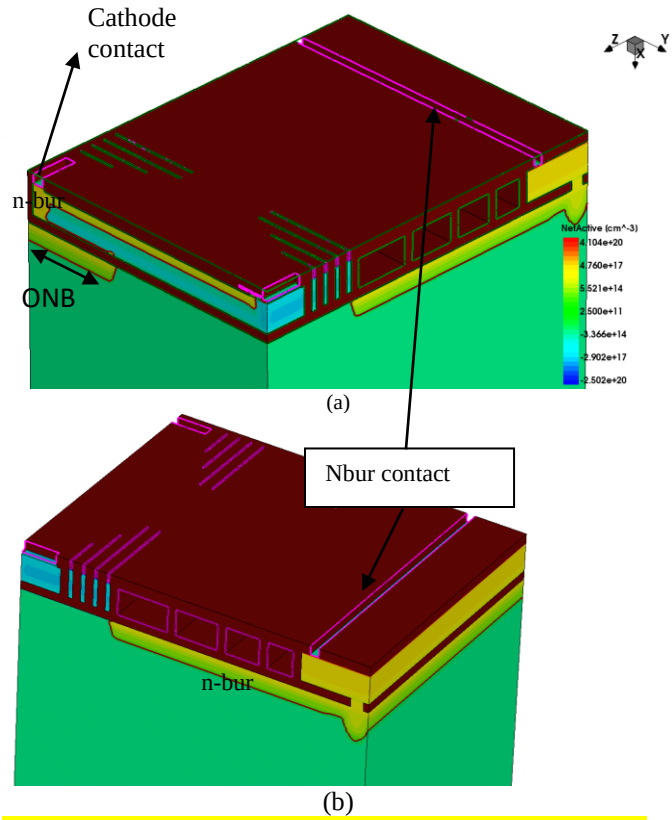


Fig. 6. 3D device representation (a) the front side showing the high voltage (active) SJ area (b) the Nbur contact and the extension of the n-bur layer under the SOI oxide layer.

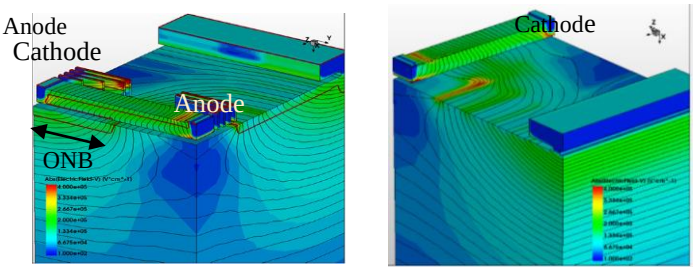
Table I: Device Parameters for the 375V device

Device parameter	**Value**
Drift Length	28µm
BOX thickness	1µm
HW thickness	725µm
Active area (double finger device)	0.005mm2
Termination area (double finger device)	0.033mm2
Active area (multi-finger device)	2.19mm^2
Termination area (multi-finger device)	0.40mm^2

A main challenge in the design of a lateral PSOI SJ structure is in engineering the 3-dimensional effects and in particular the suppression of high electric fields within the HW, the termination and the active area. The interplay between the potential distributions in these three areas is critical to the device optimization. The extension of the n-bur layer under the active area (overlap n-bur layer, ONB), as shown in Fig. 5 and 6, is of great importance to the potential distribution and therefore to the breakdown of the device and cell area consumption. Under extensive simulations and experimental investigation, we have identified the optimal 3D geometry of this layer with this being dependent on the device voltage rating. It was found that, the ONB between 3-10um (in the x-direction, as shown in Fig. 5) provides the best breakdown performance. To maintain the target breakdown voltage, this parameter value is increased with an increasing

drift region length for the 45V to 400V range.

Fig. 7 (a and b) shows the 3D complex interaction (through the electro-potential lines) between the HW and n-bur layer (ONB extension), the Deep Trench Isolation (DTI) termination and the active area. These figures also indicate the potential weak (failure) points which experience high electric field pressures within the cells. These points include the active area at Anode and Cathode sides, the transition area between the termination and HW and the HW diode under an applied V_{NBUR} and C_{athode} of 400V. For this cell design, the use of the third dimensional device configuration, i.e., the positioning of the n-bur layer in the third dimension, helps to shape and align the electro-potential lines under the BOX. Fig. 8 shows the simplified 2D simulation of the potential distribution across the device; the n-bur layer is present under the Cathode region and extends towards the Anode side.



(a) (b)

Fig. 7 (a and b). 3D interaction of the electro-potential lines) between the HW diode, DTI termination and the active area; this representation does not include the oxide layer for better visualization purposes.

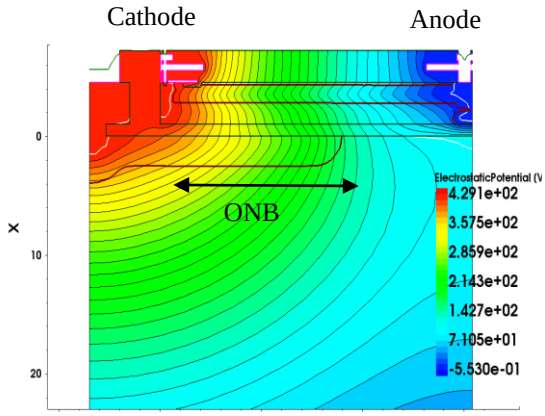


Fig. 8. Potential distribution with n-bur layer extending under BOX from the Cathode towards the Anode HV diode terminal.

The transition area has been an area that required intense optimization and a novel voltage-scalable self-termination technique using DTI to avoid crowding of potential at the edges was developed. The DTI termination comprises of two main characteristics (i) the external "square silicon tubs" of silicon isolated by oxide all around the HV device area (Fig. 9 what we call "crisscross termination" area. In particular, the width of silicon tubs has been an important parameter to the electro-potential distribution across the termination area. As shown in more detail in Fig. 9, this region features individually isolated (with the aid of oxide) silicon islands right at the perimeter of the active area. Hence, the crisscross design has been particularly effective in eliminating the high electric field peaks that were appearing at the edge of the active area. Fig. 10 shows an infrared transmission image of a fabricated MOSFET (D and S stand for Drain and Source respectively) and the DTI termination surrounding the active area. It should also be noted that the area consumption of this termination design is very small compared to the active area. In case of a 375V, 72mm multi-finger device the percentage termination/total area is less than 15% (table I).

As already mentioned above, the active area drift region consists of SJ layers of highly doped charge balanced structures. The presence of the HW diode under the BOX enables the use of uniformly charge balanced layers across the device making it voltage scalable according to the SJ theory. In terms of the drift region design two geometries (implantation strategies) were pursued; the 1xSJ drift region uses a single drift region implantation mask for both the p and n layers while the 2xSJ is based on three alternating p-n-p layers within the drift region as shown in Fig. 11. In this work SJ MOSFETs and diodes have been developed and experimentally demonstrated up to 500V breakdown.

B. Experimental Results

1) On-state and breakdown performance

The device performance parameters (area specific on-state resistance R_{dson}) for the developed NDMOS 1xSJ and 2xSJ are summarized in Table II. The upper half of the table refers to a

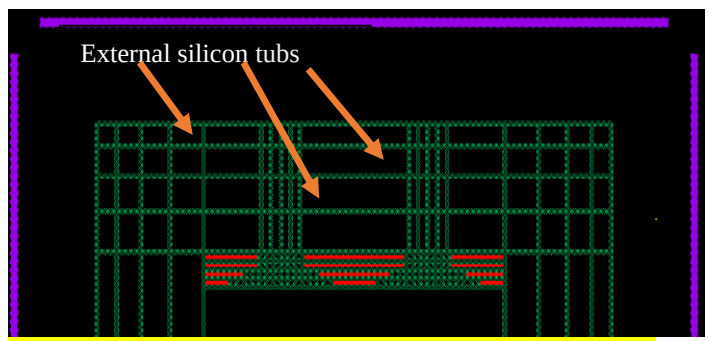


Fig. 9. The termination layout crisscross termination design right at the perimeter of the SJ active area.

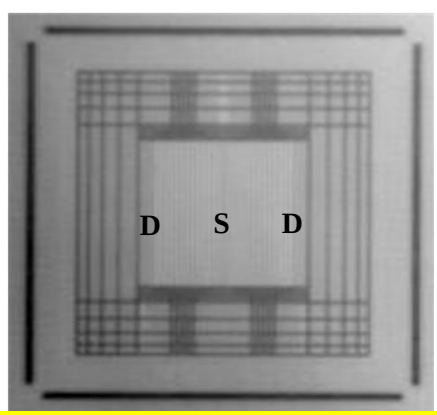


Fig. 10. IR transmission image of the active and termination design.

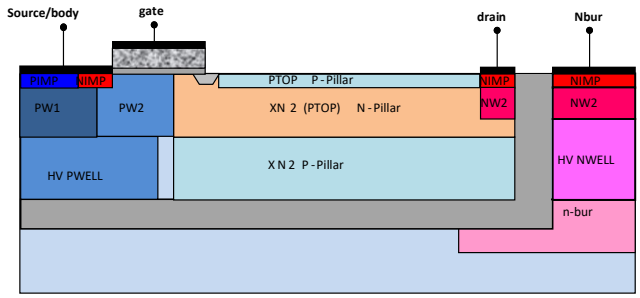


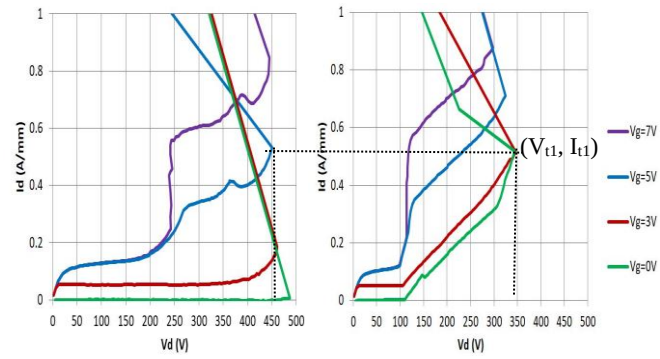
Fig. 11. The 2x SJ PSOI NMOS structure (schematic).

single 1xSJ NMOS structure whereas, the second half refers to a double (denser) 2xSJ NMOS structure. The second column refers to the device breakdown voltage with the highest value reaching 495V and exhibiting an Rdson of 4150 mOhm.mm2. Fig 12(a) shows the on-state output and drain voltage characteristic reaching 465V (at Vg=0V) (Table II – Device 10), with the N-bur contact shorted to the Drain/Cathode. The on-state output characteristic follows a typical LD MOSFET shape with the characteristic first and second current expansion regions [20]. The R_{dson} vs. V_{bd} (body-drain) benchmarking graph is plotted along with the Si limit (Fig. 13). Due to voltage scalability of the SJ on PSOI architecture these curves run in parallel with the "Silicon Limit" for a wide voltage range. As one would expect, denser SJ pillars ("2x") shift the curve down (towards lower R_{dson}) for voltages >200V and allow the device to "break the Si limit". This is because the doping concentration of 2x SJ is allowed to be increased according to the SJ theory. In the same figure, we are also plotting device performances as reported previously by XFAB [14] as well as NXP [21], STM [17], Renesas [22], UESTC/CSMC [23] and On Semi [24]. For the double SJ drift device type, the demonstrated performance outperforms these devices. In the case of the single (1x) SJ type structure, the only devices surpassing this performance is the OnSemi [24] up to 260V and UESTC/CSMC [23] at 460V. It is also important to note that the silicon limit (Fig. 13) is based on vertical devices which cannot be used in power ICs, while the technologies presented here are lateral and hence at a disadvantage in terms of the scaling between on-state resistance and breakdown voltage.

As already mentioned above, the effect of the n-bur layer overlapping the drift region and expanding from the Drain/Cathode towards the Source/Anode side (ONB dimension) on the BV was investigated. As can be seen in Fig. 14 (confirming the 3D simulations), this parameter directly affects the achieved maximum breakdown voltage.

2) *Hot Carrier Integrity*

Hot Carrier Integrity (HCI) has also been monitored through the development process. The devices were stressed under 80% operational voltage conditions and the on-state resistance was measured throughout this period. Fig. 15 shows the simulation result of the on-state current density. For the case of the 2xSJ NMOS (top) the current flows mostly away from the trap rich silicon-oxide interface, in contrast to the 1xNMOS (bottom) [25]. Fig. 16 shows the measured HCI



(a) (b)

Fig. 12. The on-state characteristic of a PSOI 1x NMOS with (a) the N-bur contact shorted to the Drain/Cathode contact (b) the N-bur contact floating.

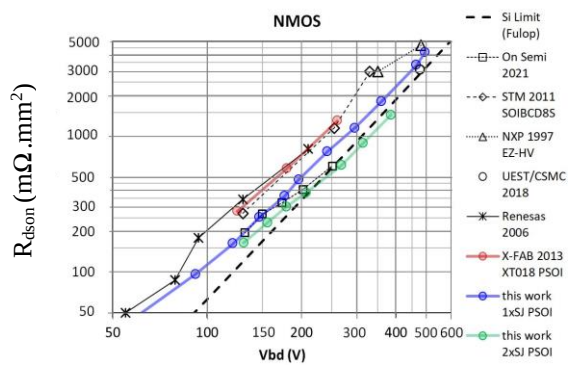


Fig. 13. The R_{dson} vs V_{bd} benchmarking graph (this work green line) along with the Si limit (black dotted line).

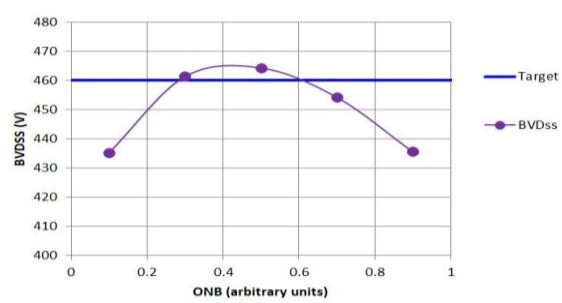


Fig. 14. The breakdown volatge (drain-source) plotted against the n-bur layer overlap (ONB) with the drift region expanding from the Cathode towards the Anode side of the 1xSJ (Table II –Device 10).

degradation of the SJ NMOS structures. From this figure, it can be observed that both the 1xSJ and 2xSJ devices, benefit from the overall device optimization compared to the previous generation results however, the degradation of the denser SJ is much lower than the 1xSJ structure. A explained above, the 2xSJ NMOS device benefits from the buried current conduction, which keeps the impact ionization away from the trap-rich oxide interfaces. More specifically, this work's SJ devices show significantly lower degradation, down to 0.8% R_{dson} degradation after 10k seconds for the denser pillar 2xSJ variant.

3) *Electrostatic Discharge (ESD)*

For the ESD evaluation of a PSOI with the separately biased N-bur contact, we considered two different scenarios.

Table II: R_{dson} Vs Breakdown Voltage Performance

Device	NLDMOS 1x	
	R_{dson} (mOhm*mm^2)	BV (V)
1	45	58
2	96	92
3	162	121
4	253	147
5	362	177
6	479	196
7	772	242
8	1150	296
9	1810	360
10	3350	465
11	4150	495
	NLDMOS 2x	
1	230	155
2	385	205
3	895	315
4	1435	380

1) Unpowered Chip: In this case the HW is floating i.e. the HW diode is not reverse biased. Fig. 12(b) shows the Transmission Line Pulse (TLP) measurement characteristics with high trigger currents I_{t1} for both Vg=0V and Vg=5V. This high trigger current allows an inherent self-protection of the large area devices. The trigger voltage V_{t1} is not as critical in this case as the device is unpowered.
2) Powered Chip: The HW diode is reverse biased. This case is relevant for small devices connected to a pad, which are not self-protected. Hence, the ESD window must be ensured and the trigger voltage V_{t1} should be sufficiently large (Fig. 12(a)).
3)

IV. SUMMARY

This paper presents aspects of a highly efficient platform for Power ICs. This platform is based on the 3D combination of SJ concept with the PSOI architecture. The SJ PSOI high voltage technology offers many advantages over conventional SOI RESURF technologies. Here we describe in detail a SJ voltage scalable structure in PSOI devices with breakdown voltages from 45V to 495V along with the HW and termination area optimization. This second generation of SJ devices on PSOI substrates have a wider voltage range, lower on-sate resistance and significantly reduced HCI degradation.

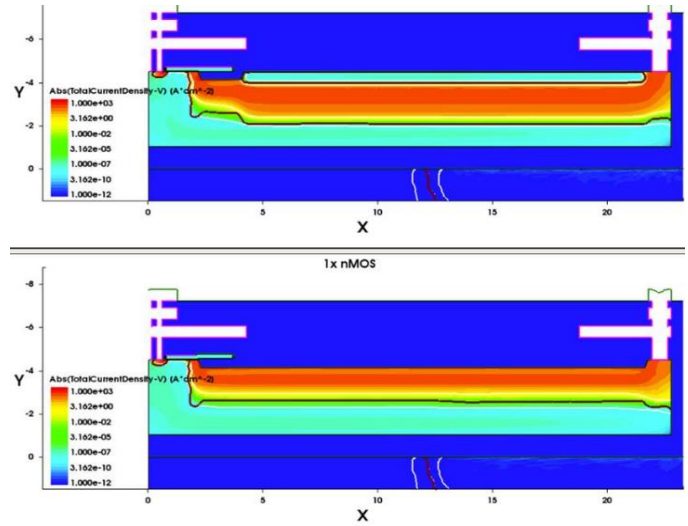


Fig. 15. Simulated on-state current density; for the 2xNMOS (top) the current flows mostly away from the trap rich silicon-oxide interface, compared to 1xNMOS (bottom).

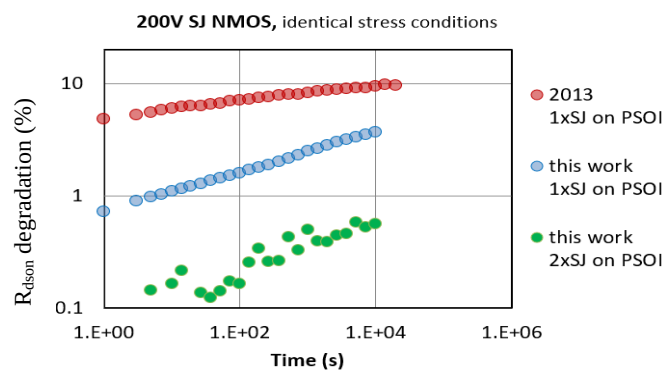


Fig. 16. HCI degradation of different generations of 200V rated (breakdown Voltage over 240V) SJ NMOS on PSOI.

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