A Thesis Submitted for the Degree of PhD at the University of Warwick

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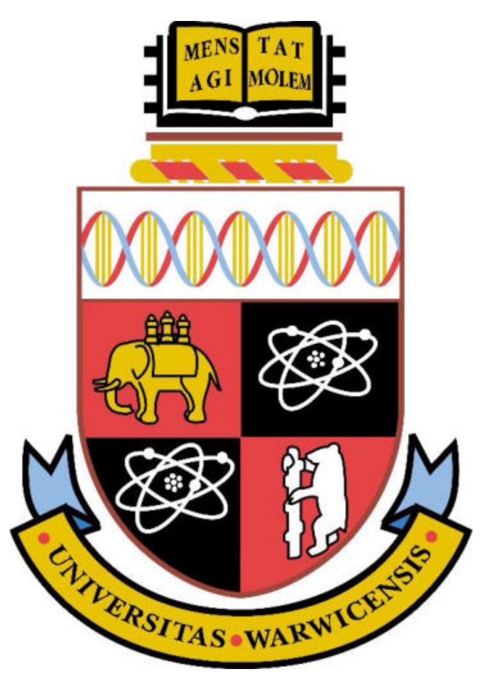
Development of Schottky and MOS interfaces for SiC power devices



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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has been composed by myself and has not been submitted in any previous application for a degree at any other University.

Except where specifically stated, all of the work described in this thesis was carried out by the author or under his direction in the School of Engineering at the University of Warwick. Parts of this thesis have been published by the author during the period of study, from November 2017 to October 2021. They are given in full detail in the Publication List section.

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List of journal publications

1. **A.B. Renz**, F.Li, O.J. Vavasour, P.M. Gammon, T. Dai, G.W.C. Baker, F. La Via, M. Zielinski, L. Zhang, N.E. Grant, J.D. Murphy, P.A. Mawby, M. Jennings, and V.A. Shah, "Initial investigations into the MOS interface of freestanding 3C-SiC layers for device applications", *Semiconductor Science and Technology*, vol. 36, no.5, p. 055006, 2021.

2. **A.B. Renz**, O.J. Vavasour, P.M. Gammon, F. Li, T. Dai, M. Antoniou, G.W.C. Baker, E. Bashar, N.E. Grant, J.D. Murphy, P.A. Mawby, and V.A. Shah, "The improvement of atomic layer deposited SiO_2/4H-SiC interfaces via a high temperature forming gas anneal", *Materials Science in Semiconductor Processing*, vol. 122, p. 105527, 2021.

3. **A.B. Renz**, V.A. Shah, O.J. Vavasour, Y. Bonyadi, F. Li, T. Dai, G.W.C. Baker, S. Hindmarsh, Y. Han, M. Walker, Y. Sharma, Y. Liu, B. Raghothamachar, M. Dudley, P.A. Mawby, and P.M. Gammon, "The improvement of Mo/4H-SiC Schottky diodes via a P2O5 surface passivation treatment", *Journal of Applied Physics*, vol. 127, no.2, p. 025704, 2020.

List of co-authored journal publications

1. F. Li, **A.B. Renz**, A. Perez-Tomas, V.A. Shah, P.M. Gammon, F. La Via, M. Jennings, and P.A. Mawby, "A study on free-standing 3C-SiC bipolar power diodes", *Applied Physics Letters*, vol. 118, no. 24, p.242101, 2021.

2. G.W.C. Baker, C. Chan, **A.B. Renz**, Y. Qi, T. Dai, F. Li, V.A. Shah, P.A. Mawby, and P.M. Gammon, "Optimization of

1700 -V 4H-SiC Superjunction Schottky Rectifiers With Implanted P-Pillars for Practical Realization", *IEEE Transactions on Electron Devices*, vol. 68, no. 7, pp. 3497-3504, 2021.

3. T. Dai, L. Zhang, O.J. Vavasour, **A.B. Renz**, V.A. Shah, M. Antoniou, P.A. Mawby, and P.M. Gammon, "A Compact Trench-Assisted Space-Modulated JTE Design for High-Voltage 4H-SiC Devices", *IEEE Transactions on Electron Devices*, vol. 68, no. 3, pp. 1162-1167, 2021.

List of conference publications

1. **A.B. Renz**, O.J. Vavasour, V.A. Shah, V. Pathirana, T. Trajkovic, Y. Bonyadi, R. Wu, J.A. Ortiz-Gonzalez, X. Rong, G.W.C. Baker, P.A. Mawby, and P.M. Gammon, "3.3 kV SiC JBS diodes employing a P_2O_5 surface passivation treatment to improve electrical characteristics", *IEEE Energy Conversion Congress & Expo (ECCE)*, accepted for publication, 2021.

2. **A.B. Renz**, O.J. Vavasour, P.M. Gammon, F. Li, T. Dai, S. Esfahani, G.W.C. Baker, N.E. Grant, J.D. Murphy, P.A. Mawby, and V.A. Shah, "Development of high-quality gate oxide on 4H-SiC using atomic layer deposition", *Materials Science Forum*, vol. 1004, pp. 547-553, 2020.

3. **A.B. Renz,** V.A. Shah, O.J. Vavasour, Y. Bonyadi, G.W.C. Baker, F. Li, T. Dai, M. Walker, P.A. Mawby, and P.M. Gammon, "Surface effects of passivation within Mo/4H-SiC Schottky diodes through MOS analysis", Materials Science Forum, vol. 963, pp. 511-515, 2019.

List of co-authored conference publications

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2. T. Dai, **A.B. Renz**, L. Zhang, O.J. Vavasour, G.W.C. Baker, V.A. Shah, P.A. Mawby, and P.M. Gammon, " Design and Optimisation of Schottky Contact Integration in a 4H-SiC Trench MOSFET", *Materials Science Forum*, vol. 1004, pp. 808-813, 2020.

3. G.W.C. Baker, C. Chan, T. Dai, **A.B. Renz**, F. Li, V.A. Shah, P.A. Mawby, and P.M. Gammon, "Study of 4H-SiC Superjunction Schottky rectifiers with implanted p-pillars", *Materials Science Forum*, vol. 963, pp. 539-543, 2019.

List of oral presentations

1. **A. B. Renz**, V.A. Shah, Y. Bonyadi, F. Li, G.W.C. Baker, P.A. Mawby, and P.M. Gammon, "Surface effects of passivation within Mo/4H-SiC Schottky diodes through MOS analysis", oral presentation at *European Materials Research Society Fall Meeting 2018*, Warsaw, Poland.
2. **A.B. Renz,** V.A. Shah, O.J. Vavasour, Y. Bonyadi, G.W.C. Baker, F. Li, T. Dai, M. Walker, P.A. Mawby, and P.M. Gammon, "Development of high-quality gate oxide on 4H-SiC using atomic layer deposition, accepted for oral presentation at

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Abstract

The very nature of the wide bandgap semiconductor silicon carbide (SiC), namely its high critical electric field, thermal conductivity and stable native oxide, silicon dioxide (SiO_2), has enabled the design, fabrication and market penetration of a new generation of power devices, Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect transistors (MOSFETs), with blocking voltages from 600-1700V. Despite the successful commercial realisation of these devices, the surface of SiC and the interfaces it forms with metals (Schottky interface) and insulators (MOS interface), are still the source of reliability problems such as premature breakdown and decreased lifetime of gate oxides on SiC.

The focus of this thesis lies on the exploration of passivation approaches to the Schottky interface as well as the investigation of the quality of deposited gate oxides. Firstly, an electrical and physical analysis of the impact of a proposed phosphorous pentoxide (P_2O_5) treatment on planar and optimised 3.3 kV JBS diodes reveals a reduction of Schottky barrier height as well as leakage current, offering a possible path to overcome the basic trade-off between on-state and off-state performance of a diode.

The second part of the thesis focuses on atomic layer deposition (ALD) – deposited SiO_2 layers, where a post-deposition annealing (PDA) study reveals the performance improvement when a PDA in forming gas ambient at 1100°C is carried out. This process was then successfully transferred and validated on freestanding 3C-SiC material, which successfully demonstrated the general suitability of this material for power device applications.

List of Abbreviations

AFM	Atomic Force Microscopy
Al_2O_3	Aluminium oxide
ALD	Atomic layer deposition
BDEAS	Bis(diethylamino)silane
BPD	Basal plane dislocation
C_2H_4	Ethylene
C_3H_8	Propane
C-V	Capacitance-voltage
CVD	Chemical vapour deposition
DLTS	Deep-level transient spectroscopy
EDMR	Electrically detected magnetic resonance
EDX	Energy-dispersive x-ray analysis
e-mode	Enhancement-mode
ESR	Electron spin resonance
EV	Electric vehicle
FE	Field emission
FIB	Focussed ion beam
FWHM	Full-width-half-maximum
Ga_2O_3	Gallium oxide
GaAs	Gallium arsenide
GaN	Gallium nitride
GaP	Gallium phosphide
Ge	Germanium
H_2	Hydrogen

HCl_3Si	Trichlorosilane
HEMT	High electron mobility transistor
HVDC	High-voltage direct current
IGBT	Insulated-gate bipolar transistor
InAs	Indium arsenide
InP	Indium phosphide
InSb	Indium antimonide
JBS	Junction barrier Schottky
LED	Light emitting diode
LPCVD	Low pressure chemical vapour deposition
MOS	Metal-oxide-semiconductor
MOSCAP	Metal-oxide-semiconductor capacitor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPS	Merged PiN Schottky
N	Nitrogen
OBC	On-board charger
P_2O_5	Phosphorous pentoxide
P_b	Si dangling bond
P_{bC}	Carbon dangling bond
PDA	Post-deposition anneal
POA	Post-oxidation anneal
RMS	Root-mean square value
SBD	Schottky barrier diode
SBH	Schottky barrier height
SEM	Scanning electron microscopy

Si	Silicon
SiC	Silicon carbide
SiGe	Silicon germanium
SiH_4	Silane
SIMS	Secondary ion mass spectrometry
SiO_2	Silicon dioxide
SiP_2O_7	Silicon diphosphate
TDDB	Time-dependent dielectric breakdown
TE	Thermionic emission
TED	Threading edge dislocation
TEM	Transmission electron microscopy
TEOS	Tetraethyl orthosilicate
TFE	Thermionic field emission
TMA	Trimethylaluminium
ToA	Take-off angle
TSD	Threading screw dislocation
UPS	Uninterruptable power supply
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

List of Variables and Symbols

A	Device area
A	Effective Richardson's constant
BE	Binding energy
C_{FB}	Flatband capacitance

C_{IT}	Capacitance of interface traps
C_{OX}	Oxide capacitance
C_S	Semiconductor capacitance
dI/dt	Current fall/rise rate
D_{IT}	Density of interface trapped charge
D_{MC}	Mobile charge areal density
E_{00}	Tunneling energy of the semiconductor
E_C	Conduction band
E_{crit}	Critical electric field
$E_{SPECTR.}$	Measured energy of the detected/ejected electrons.
E_T	Trap level energy position
E_V	Valence band
$E_{X\text{-}ray}$	X-ray energy (h*υ)
G_M	Measured conductance
G_P	Parallel conductance
ħ	Reduced Planck's constant
I_{RR}	Reverse recovery current
J	Current density
J_R	Leakage current density
J_S	Saturation current
k	Boltzmann's constant
m^*	Tunnelling effective mass
m_0	Effective electron rest mass

N_D	Drift-region dopant concentration
N_F	Quantity of fixed charge
n_i	Intrinsic carrier concentration
N_{IT}	Number of interface trapped charge
N_M	Quantity of mobile oxide charge
N_{OT}	Number of oxide trapped charge
Q	Electron charge
Q_F	Fixed oxide charge
Q_{IT}	Interface trapped charge
Q_M	Mobile oxide charge
Q_{OT}	Oxide trapped charge
Q_R	Extracted charge
R_{ON}	On-resistance
$R_{ON,SP}$	Specific on-resistance
T	Absolute temperature
t_{OFF}	Off-time
t_{ON}	On-time
V	Applied bias, Voltage
V_B	Breakdown voltage
V_{BI}	Built-in potential
V_F	Forward voltage drop
V_{FB}	Flatband voltage
V_R	Reverse bias
W_g	Bandgap

ΔV_{FB}	Hysteresis voltage
η	Ideality factor
λ	Thermal conductivity
μ_n	Electron mobility
σ	Surface potential fluctuation
τ_{IT}	Time constant of the interface trap
$\phi^0_{B,n}$	Theoretical maximum metal-semiconductor barrier height without consideration of effects such as barrier height lowering
ϕ_{BN}	Barrier height
ϕ_M	Difference between vacuum level and Fermi level in the metal
ϕ_N	Potential difference between the conduction band level and Fermi level in the n-type doped semiconductor
ϕ_S	Difference between vacuum level and Fermi level in the semiconductor
χ_s	Semiconductor electron affinity
ω	AC measurement frequency

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Chapter 1: 1 Introduction

This thesis is focused on the surface of the wide bandgap semiconductor material silicon carbide (SiC) and the interfaces it forms with metals (Schottky interface) and insulators (MOS interface). In particular, it aims to provide insights into surface conditioning procedures and their impact on the quality of Schottky interfaces. Secondly, it aims to create a robust understanding on how to form good quality insulator/SiC interfaces by means of insulator deposition techniques. Post-deposition treatments of the deposited insulator, which have shown to produce high-quality interfaces on other materials such as silicon (Si), have been tailored to the SiC material. The most promising treatments were then further investigated to highlight one possible path to high quality interfaces on SiC. The progress made on these insulated layers will make possible transistors, metal-oxide-semiconductor field-effect-transistor (MOSFETs), that are more reliable and have fewer losses when they are switched. In combination with the improved Schottky diodes, this would lead to power electronic converter solutions with reduced losses and hence increased efficiency.

1.1 SEMICONDUCTOR APPLICATIONS OVERVIEW

Despite significant setbacks due to the two World Wars, the electronics technology has changed people’s lives across the globe during the twentieth century at an unprecedented extent and speed, with this trend continuing since the turn of the millennium. Today’s electronics applications cover a wide range, from low-power consumer electronics such as smart phones, up to high-voltage direct current (HVDC) grid level converters. Since all of these applications require different operating

conditions, the electronic device engineering has always played a critical role in the electronics hierarchy, covering device structure design, fabrication and choice of semiconductor materials. These semiconductor materials and their key parameters - bandgap energy, charge carrier mobility, saturation velocity, critical electric field and thermal conductivity - determine the device's performance in the applications.

For the past decades, Si has been the dominant semiconductor device shaping the semiconductor market through its availability on large wafer diameters with extremely low material defects and its reliable oxide, silicon dioxide (SiO_2), leaving only marginal market niches for other semiconductor materials such as germanium (Ge), gallium arsenide (GaAs), gallium nitride (GaN), and silicon carbide (SiC). As of 2018, 87 % of the devices within the power semiconductor market were still based on Si [1].

1.1.1 APPLICATION SPACE FOR OTHER SEMICONDUCTOR MATERIALS

The most influential semiconductor material parameter is the bandgap energy, since this correlates with most other parameters such as critical electric field, intrinsic carrier concentration, which directly dictate the suitability of a material for a defined application. Germanium, indium arsenide (InAs) and indium antimonide (InSb), all being narrow bandgap semiconductors, can mostly be found in low-power applications such as photodetectors in the infrared radiation detection, due to their ability to detect and emit photons in this spectrum. Opposite to this, wide band gap semiconductors such as SiC and GaN are suitable for high power applications, such as power converters for automotive applications and, in the case of silicon carbide, even for ultrahigh voltage applications (> 5 kV) such as traction, static var compensation and high-voltage direct

current (HVDC) [2-4]. The wide bandgap semiconductor material SiC will be the focus of this thesis.

1.1.2 THE USE OF WIDE BANDGAP SEMICONDUCTOR DEVICES

The very nature of the wide bandgap enables devices fabricated on wide bandgap semiconductor materials such as SiC and GaN to withstand much higher electric fields, on the order of ten times higher, than Si [5]. Their good thermal conductivity also allows the use of devices at higher temperature, such as at 100°C in the car engine bay. Given that wide bandgap semiconductor devices have a much higher critical electric field than conventional devices, electronic device designers have the chance to either block a significantly higher voltage for the same device dimensions or reducing the thickness of the device by the same ratio, allowing for the resistance to be scaled down. The combination of the advantages allows for the use in power conversion [4, 6], automotive converters [5, 7], ultra-high frequency and space applications [8-10].

The potential benefits of using power semiconductor devices in applications become obvious when the powertrain in electric vehicles (EVs) is regarded. A typical schematic of this can be seen in Fig. 1.1. It depicts the importance of power electronics devices, since there are multiple stages which need the conversion of electrical power, both in the form of DC/DC converters as well as DC/AC inverters. The most relevant of these conversion stages is, however, the main inverter stage, which converts DC currents and voltages from the battery-side side into AC power which is needed for the operation of the electrical machine, which in most cases is either an induction machine or a permanent magnet synchronous machine.

The converter or inverter topologies are based on the operation of power semiconductor devices, in particular three-terminal devices,

transistors, which have been developed on very mature silicon wafers over the past five decades. To this day, the vast majority of converters/inverts use silicon-based insulated-gate bipolar transistors (IGBTs) due to its excellent reliability and low price.

In recent years, a few manufacturers of EVs have switched from using Si IGBTs to using new silicon carbide-based MOSFETs in their main inverter, starting a possible transition away from Si-based transistors to SiC-based topologies for high power applications. This trend is accompanied by the uptake of GaN transistors in low voltage/power applications, such as on-board chargers (OBCs).

Due to the material properties of SiC, which will be explained in more detail later in this chapter, manufacturers were able to scale down the size and weight of the main inverter, e.g. the main inverter stage of a Tesla Model 3 2018 weighs about 4.8 kg, compared to 11 kg in a 2019 Nissan Leaf and 8.2 kg in a 2019 Jaguar I-Pace, both of which are using Si-IGBT-based inverters[11]. In addition to this, the Tesla has a power density which is 4.4 x higher than the Nissan Leaf. The efficiency was increased

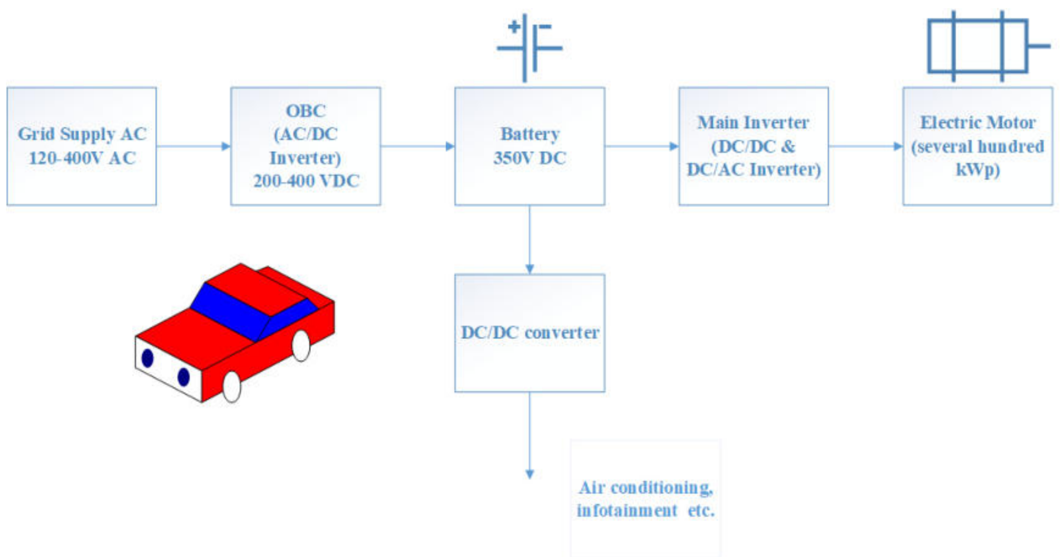

Figure 1.1 A schematic of a typical drivetrain in an electric vehicle with multiple inverter and converter stages.

up to 97% [11] using the SiC-based technology, too. Although this came at the expense of higher costs, it allowed for the manufacturing of an electrical vehicle with an extended range due to the use of wide bandgap semiconductor devices, e.g. a more efficient inverter stage and lower overall weight of the powertrain. Also, more typically, this allows for a reduction in the number of expensive and heavy batteries the car must carry for the same range. The lighter inverter and battery pack in turn make the car more efficient.

1.2 SEMICONDUCTOR ALLOYS AND COMPOUND SEMICONDUCTORS

The chemical composition of semiconductors is the most commonly used property to distinguish them. The vast majority of semiconductors comprise of a single chemical element, in most cases either silicon or germanium, located in group 14 of the periodic table. With Si representing the benchmark material in terms of its reliability and application relevance, Ge is a narrow bandgap material, especially used in infrared sensor applications.

The combination of two or more semiconductor elements in a solution or a compound is called an alloy[12].

Both silicon and germanium can form an alloy with each other, silicon germanium (SiGe), on which commercial products such as SiGe diodes are commercially available. Alloys can also be made with the two remaining group 14, or group IV, materials carbon and tin, to form IV-IV alloys, though most of these are unstable and near-impossible to prepare.

Often, compound semiconductors are formed when materials of different groups are used. III-V semiconductors, using elements from group 13 (e.g., Al, Ga, In) and 15 (e.g., N, P, As, Sb), include GaAs, indium phosphide (InP), gallium phosphide (GaP), and GaN, allowing bandgap engineering. From a foundational material (typically GaAs or InP), one can engineer an alloy with the desired bandgap and lattice constant (e.g., $In_{0.53}Ga_{0.47}As$, which lattice matches to InP but has a narrower bandgap). This flexibility in material properties and combinations, combined with a direct bandgap for most III-V materials, has led them to dominate in light emitting diode (LED) and photodiode applications. As a rule of thumb, the selection of materials from a lower position in the periodic table will result in a narrower bandgap and vice versa. II-VI semiconductors also exist but they occupy an even smaller niche than III-V materials and their properties will not be further discussed in this thesis.

Beyond group IV and analogous III-V and II-VI semiconductors, many other crystalline compound can be semiconducting and suitable for device fabrication. An example is gallium oxide (Ga_2O_3) – while conventionally considered an insulator, its bandgap of 4.8 eV still allows it to be used as a wide bandgap semiconductor when suitably doped.

Silicon carbide is a binary IV-IV compound semiconductor, similar to III-V semiconductors, and has a wide bandgap of 3.21 eV [13]. With its wide bandgap and related electrical parameters, such as a high critical electric field of 2-3 MV/cm, SiC is already responsible for significant improvements in the power electronics field from voltage ratings of 600 V and up.

1.3 REVIEW OF WIDE BANDGAP MATERIAL DEVICES

This brief overview of the current application space of wide bandgap devices will focus on the most industrially relevant materials: SiC, GaN and, to a lesser extent, diamond and Ga_2O_3. An overview of important material properties can be found in TABLE 1.1.

Table 1.1: The material properties of Si and selected wide bandgap semiconductors at 300 K [12, 14-16], where W_g – bandgap (eV), E_{crit}, critical electric field (MV/cm), n_i – intrinsic carrier concentration (cm^{-3}), λ – thermal conductivity (W/cm.K), elec. sat. velocity–electron saturation velocity ($cm.s^{-1}$),μ_n – electron mobility ($cm^2.V^{-1}.s^{-1}$)

Semiconductor Material	W_g (eV)	E_{crit} (MV/cm)	n_i (cm^{-3})	λ (W/cm.K)	Elec. Sat. Velocity ($10^7.cm.s^{-1}$)	μ_n ($cm^2.V^{-1}.s^{-1}$)
Si	1.12	0.2	1.5×10^{10}	1.5	1	1350
4H-SiC	3.26	2.8	8×10^{-9}	4.5	2	720-650
GaN	3.39	3.75-3.3	1.9×10^{-10}	1.3	2.5	2000-1000
Diamond	5.45	10	1.6×10^{-27}	20	2.7	3800
3C-SiC	2.36	1.4	1.5×10^{-1}	3.2	2	800
Ga_2O_3	4.85	8	$2.6 \times 10^{-9} – 1 \times 10^{-22}$	0.1-0.3	1.8-2.0	300

The material properties of silicon carbide, mean that devices such as Schottky barrier diodes (SBDs) and MOSFETs can be used at a much higher voltage level. Whereas commercial Si SBDs and MOSFETs are being employed at lower voltages, their SiC counterparts have penetrated the power device market at blocking voltages from 600 V to 1700 V over the past two decades [3], possibly extending this further up to 3300 V within the next five years. SBDs and MOSFETs rely on only a single charge carrier type for operation (typically electrons). This allows them to switch quickly and efficiently, unconstrained by minority carrier generation and recombination effects, which dominate in bipolar devices. Although this comes at the expense of higher conduction losses, this does not restrict their uptake in the market for automotive power devices, with blocking voltages at around 650°V.

Furthermore, SiC devices have been used in traction applications in the railway sector, uninterruptable power supplies (UPS) [2-4] and EV applications such as inverters, on-board chargers, DC-DC converters and DC rapid chargers, and they are also are at the brink of entering into AC drives and wind applications [7], where improvements in efficiency are needed. An example of this was shown in section 1.1.2. On a non-commercial level, ultra-high voltage (>10 kV) devices have been successfully demonstrated [17-19].

Factors which limit the further uptake of SiC devices are its higher cost per wafer compared to Si, its higher density of performance deteriorating material defects such as basal plane dislocations (BPDs), threading edge dislocations (TEDs), threading screw dislocations (TSDs) [13, 20], and issues with the reliability of the insulator/SiC interface, which lower the lifetime of MOS-based devices and reduce channel mobilities [21], hence increasing the specific on-resistance $R_{SP,ON}$ of the devices.

GaN power devices are currently utilising mainly lateral device architectures, offering good performance in high-frequency [22], gas sensors [23] motor drives [24] and rail traction drives[25], although always at considerably lower voltage (maximum 650-900 V) and power ratings than SiC. Lateral power GaN devices such as enhancement-mode (e-mode) high electron mobility transistors (HEMTs) and diodes are already commercially available up to 900 V[5], competing with Si IGBTs and SiC MOSFETs in automotive applications in this voltage range. The previously mentioned lower power ratings compared to SiC are due to the lateral device geometry: in a lateral device, the current flows through a smaller cross-sectional area, compared to large vertical devices, increasing on-state resistance and limiting the current carrying capability of these devices, so they are limited to applications up to a few kW [26]. GaN research has been ongoing into vertical GaN devices, using either freestanding GaN or GaN bulk substrates and, most importantly, using lower-cost GaN-on-Si substrates, which could successfully block voltages up to 1.2 kV [26]. For high-cost premium devices, GaN-on-SiC substrates are available in research areas and could potentially capitalise on the lower lattice mismatch between GaN and SiC and the higher thermal conductivity of SiC substrates [27]. Generally however, the limitations in material- layer structures unsuitable for vertical devices, high defect density from growth on mismatched substrates and limited wafer diameters - are still hampering the further development of GaN devices, since this is still significantly restricting their current, voltage and power ratings[26].

Amongst the mentioned wide bandgap semiconductors, 3C-SiC, further explained in chapter 2, diamond and Ga_2O_3 devices do mainly exist in niche research applications, where successful 3C-MOSFETs [28]

and diodes[29], quasi-vertical diamond SBDs [30, 31] and research-grade Ga_2O_3 diodes [15] have been shown. Ga_2O_3 devices suffer from the material's extremely low thermal conductivity and the challenges arising when trying to p-type dope material [32] , whereas diamond devices suffer from the absence of a reliable doping process. Hence, although these materials all offer potential power electronics advantages over Si, their poor material quality, high material cost or other engineering challenges hamper further development.

The results reported in this thesis aimed to develop a surface conditioning process of 4H-SiC Schottky diodes and a dielectric deposition process on SiC materials (3C and 4H) suitable for MOS devices.

1.4 THESIS OUTLINE

In the following chapter, the material properties and growth methods of SiC are introduced. Afterwards, it introduces the power device structures that are analysed in the thesis with a focus on their interfaces. It then ends with the electrical and physical characterisation methods.

Chapter 3 then delivers an investigation into the impact of a phosphorous pentoxide surface passivation treatment on the performance of planar SiC SBDs. After showing the static electrical results, a surface study employing AFM/SEM, TEM, XPS is carried out to investigate impacts on the device brought about by this treatment. The transfer of this process into 3.3 kV power structures will be presented in chapter 4, where the development of the cross-sectional structures, the electrical performance as well as an XPS investigation are shown. A double pulse switching test is carried out on the fabricated device structures, too.

Chapter 5 then delivers a post-deposition annealing study on ALD-deposited silicon dioxide layers, in which the impact of different temperatures, ambients and post-deposition anneals on electrical characteristics of MOSCAP structures is shown. Key electrical parameters of interest that are investigated are flatband voltage, hysteresis voltage and frequency dispersion. The surface bonding chemistry is again investigated by means of XPS. In the final results chapter, the aforementioned ALD deposition process is done on freestanding 3C-SiC material, where an investigation focuses on material properties first. An AFM and XRD study is followed by electrical characterisation of MOSCAPs using thermal oxides, LPCVD-deposited and ALD-deposited oxides.

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2 Silicon Carbide Properties, Growth, Characterisation and Devices

Throughout this thesis, the crystal structure, physical and electrical properties of silicon carbide will be frequently referred to. This chapter will deliver descriptions of the crystal structure of SiC, SiC epitaxial growth, epitaxial layer defects and the most widely used growth technique, chemical vapour deposition (CVD). The chapter will then introduce the power devices that are analysed in this thesis, the theory of their interfaces and the electrical and physical techniques used to characterise them.

2.1 SEMICONDUCTOR CRYSTAL STRUCTURES, SIC POLYTYPES

When crystals are formed between solid elements or compounds, they create regular lattice patterns. Single element semiconductors, such as Si, Ge, and diamond, mostly form diamond crystal structures. Compound semiconductors most frequently form diamond-like zincblende structures (e.g. GaAs, InGaAs, GaP), though wurtzite structures that resemble hexagonal close-packed crystal structures can also be found. The most relevant compound semiconductors, GaN and SiC, are predominantly a hexoganl crystal lattice, called wurtzite.

Although their chemical composition is identical, most semiconductor materials can exhibit different crystal structures, a phenomenon that is called polymorphism [2]. For a subgroup of polymorph crystals, the stacking sequence of the smallest repetitive cell, a unit cell, differs in one axis. This structural effect is called polytypism [3]. Silicon carbide's crystalline structure is unique in that, to this day, more than 200 polytypes

have been found [4-7], although only a few of these have been shown to be stable.

SiC only allows for a rigid 50:50 stoichiometry of silicon and carbon atoms. Each carbon atom bonds to four silicon atoms, and vice versa, forming two fundamental structural patterns that can be seen in Fig.2.1, from [8]. Si and C atoms are linked via covalent bonds and form a tetrahedron. The hexagonal structure, Fig. 2.1(a), can be found in most SiC polytypes. All hexagonal polytypes of SiC are called α-SiC.

Cubic SiC, or β-SiC, as depicted in Fig.2.1 (b), is referred to as zinc-blende pattern, which has the same diamond structure as Si and Ge.

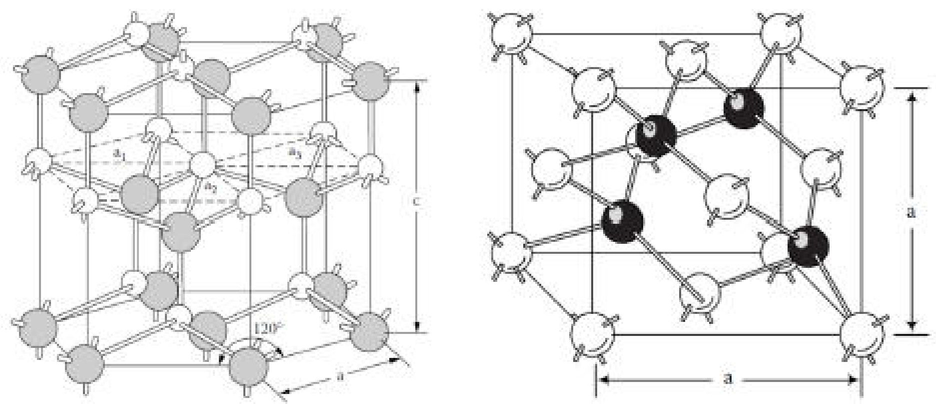


Figure 2.1 : Hexagonal (a) and cubic (b) SiC lattice, dark atoms represent Si and light atoms represent C atoms [7].

To differentiate between the different polytypes, their stacking sequence needs to be analysed. For simplification in this section, only the position of the Si atoms will be assessed, as the carbon atom aligns with it vertically in the c-plane, as seen in Figure 2.1a. For simplification, Fig. 2.2 can be observed [9]. Only three double-atomic layers denoted A, B and C exist in SiC and all polytypes can be formed when changing the

stacking sequence of these. The order in which the occupational sites repeat determines each polytype.

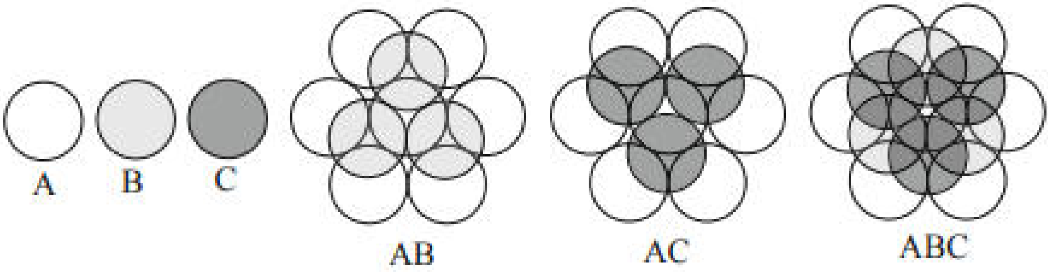


Figure 2.2: The stacking layer sequence in SiC depicting the three different occupation sites [8].

The stacking sequence of relevant polytypes of SiC is shown in Fig. 2.3, reproduced from [10]. Their labelling follows rules which are outlined in [11], where the first number refers to the number of layers needed to form a complete unit cell, H, C and R refer to hexagonal, cubic and rhombohedral lattice structures, respectively. The fundamental electrical properties of the introduced polytypes will be outlined in the next section.

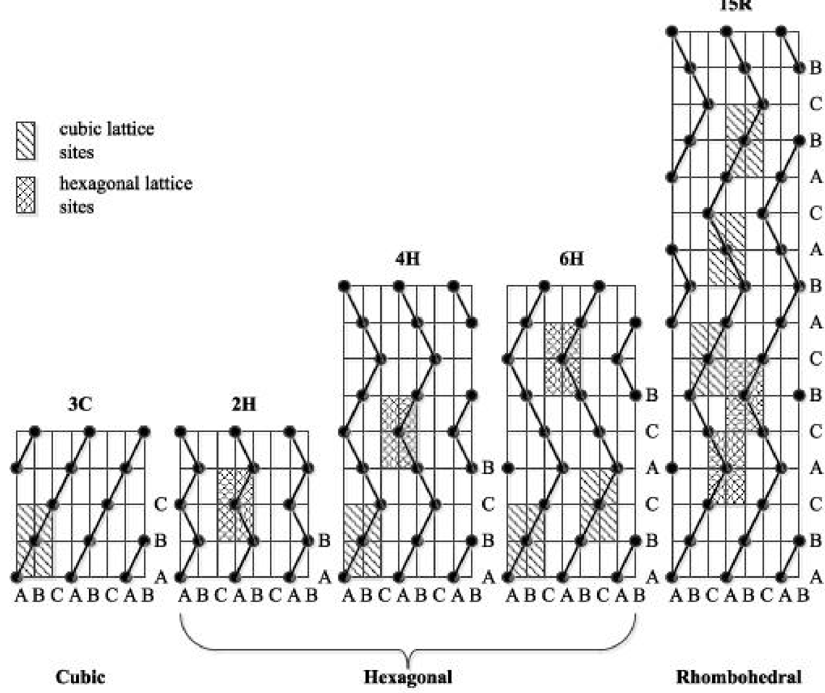


Figure 2.3: Stacking structure of selected SiC polytypes [9].

Table 2.1: A summary of the main electrical properties of Si, the most important polytypes of SiC and wurtzite GaN at 300 K [1]. Given the rarity of c-GaN and ubiquity of w-GaN, the wurtzite polytype is commonly referred to simply as ‘GaN’, and it can be assumed that the wurtzite polytype is being considered unless stated otherwise.

Properties	**Units**	**Si**	**4H-SiC**	**6H-SiC**	**3C-SiC**	**w-GaN**
Bandgap	(eV)	1.12	3.26	3.0	2.36	3.39
Critical Electric field	(MV/cm)	0.2	2.8	2.5	1.4	3.75-3.3
Electron Saturation Velocity	(cm/s)	1×10^7	2×10^7	2×10^7	2×10^7	2.5×10^7
Electron mobility	(cm^2/Vs)	1350	720-650	500	800	2000-1000
Hole mobility	(cm^2/Vs)	480	120	80	40	30
Intrinsic Carrier Concentration	(cm^{-3})	1.5×10^{10}	8×10^{-9}	10^{-5}	1.5×10^{-1}	1.9×10^{-10}
Thermal Conductivity.	(W/cm.K)	1.5	4.5	3-4	3.2	1.3

2.2 ELECTRICAL PROPERTIES

For the successful performance of power electronics devices, it is of paramount importance to consider the electrical properties of the material these devices are fabricated with. Key electrical parameters at 300 K can be found in Table 2.1. Their impact on device performance will be briefly described now. The bandgap of a material will determine how many carriers, at any given temperature, can cross from the valence band to the conduction band, impacting the intrinsic carrier concentration (n_i), which correlates with leakage current levels. The thermal conductivity governs maximum current rating via the thermal resistance between junction and die attach. On a circuit level, the device performance will be governed by the bulk mobility parameters (device resistance) and electron saturation velocity (switching).

For 4H-SiC, the extremely low intrinsic carrier concentration of approximately 8 x 10^{-9} cm^{-3} at 300 K (Table 2.1) make devices suitable to operate at much higher temperatures than Si. Since this parameter is 13 orders of magnitude higher for Si, a Si device compared to an identical SiC device will have higher leakage currents at a given operating temperature, resulting in higher losses and earlier device breakdown. This high temperature performance is also improved by 4H-SiC's thermal conductivity of 4.5 W/cm.K, approx. 3 times higher than for GaN and Si, which aids removal of heat generated by on-state and switching losses.

When comparing the three commercially relevant SiC polytypes, 4H-SiC (3.26 eV) has the highest bandgap compared to 6H-SiC (3.0 eV) and 3C-SiC (2.36 eV), offering about 3 three times the bandgap of Si.

Regarding the electron mobility, 3C-SiC (800 $cm^2/V.s$) and 4H-SiC (750-650 $cm^2/V.s$) outperform 6H-SiC (500 $cm^2/V.s$). In terms of hexagonal polytypes, 4H-SiC's hole mobility of 120 $cm^2/V.s$ is four times lower than in Si, although it still offers the highest hole mobility in the observed SiC polytypes, with 3C-SiC's hole mobility being as low as 40 $cm^2/V.s$ [12]. When comparing 4H-SiC to the other polytypes, its reasonably high mobility parameters, lowest intrinsic carrier concentration and widest bandgap all contribute to its dominance across all commercially available SiC products. Furthermore, its commercially available material quality is vastly superior with respect to 3C-SiC. Moreover, its similar mobility properties along the c- and a-axis (different from 6H-SiC, where the anisotropic mobility parameters are far more pronounced) make this polytype especially suitable for vertical power device structures [13].

The ability of 4H-SiC to withstand around 9x greater critical electric fields than Si means that, for the same device thickness, 4H-SiC devices can support a ten times higher voltage before impact ionisation progresses into avalanche breakdown. As a result, 4H-SiC can use much thinner layers with a higher doping compared to Si devices, decreasing on-state resistance without compromising blocking voltage capability. Fig. 2.4 introduces the SiC MOSFETs and compares them to their Si counterparts, where all the measurements were taken by Qinze Cao at Warwick University using a B1505 Parameter analyser on commercially available packaged devices of different suppliers. Measurements were provided with permission to be used in this thesis given by Peter Michael Gammon at Warwick University. There is a fundamental trade-off in unipolar devices (such as SBDs and MOSFETs) between specific on-state resistance and breakdown voltage, which can only be beaten by using a

bipolar device architecture or changing material. The exact description of the unipolar limit for 4H-SiC can be found in [14].

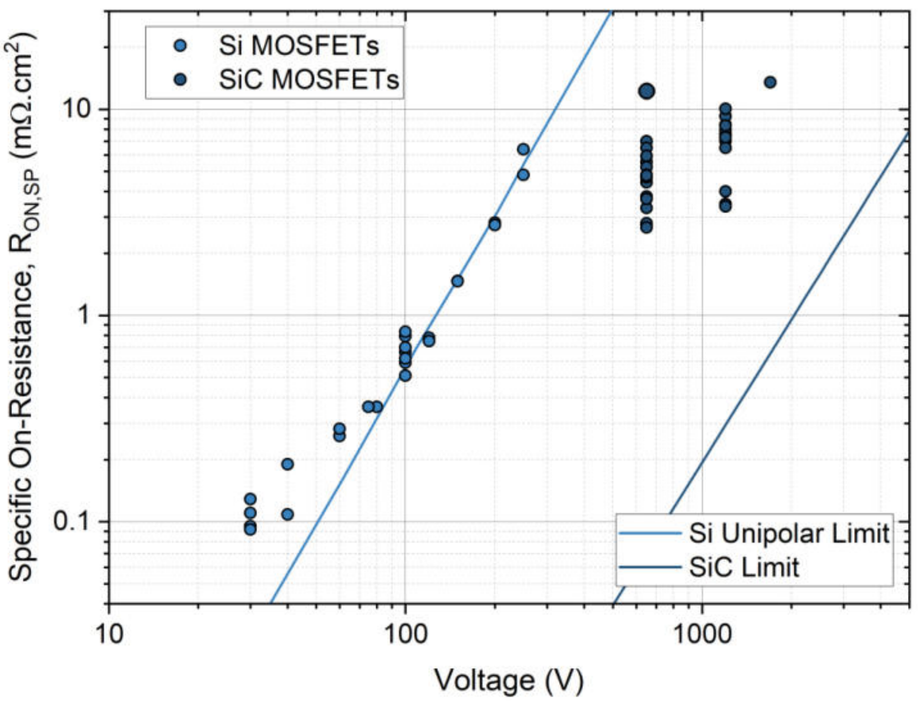


Figure 2.4: Unipolar limit comparison of devices which were fabricated on Silicon or Silicon carbide.

Fig. 2.4 illustrates that commercially available 4H-SiC metal-oxide semiconductor field-effect transistors (MOSFETs) could offer breakdown voltages which are ten times higher at the same specific on-resistance than for their Si counterparts (theoretical line in the figures). In addition to this figure, there is still one major barrier that exists in SiC device development which is the lack of devices utilising two carrier types (bipolar devices), such as PiN diodes, insulated-gate bipolar transistors (IGBTs) and thyristors, which are widely used in Si at higher breakdown voltages and higher current levels.

The absence of commercially available bipolar devices in 4H-SiC can be explained by considering the material challenges that arise when bipolar layers are grown and devices are fabricated on them.

Since heavily doped p-type exitaxial layers on highly doped n+-substrates, required in bipolar devices such as PiN diodes, have been shown to vary the lattice constant in SiC [15, 16] , additional stress is inducted near the p+/n- interface, which, especially for bigger wafer diameters, leads to an increase in wafer bow and/or the formation of additional basal plane dislocations (BPDs) [17].

Furthermore, the low carrier lifetime in bipolar SiC devices of about 1-2 μs [17], which determines the on-state and switching losses, is not long enough for sufficient conductivity modulation. Itis caused by the presence of point defects (explained in more detail in section 2.4) acting as recombination centres, finally reducing the maximum current density in bipolar SiC devices.

In addition to this, the forward voltage of bipolar SiC devices such as PiN diodes exhibits an increase (drift) of forward voltage drop in the conducting state, which is called ‘bipolar degradation’. This is caused by an expansion of a basal plane dislocation during carrier injection, causing both locally reduced carrier lifetimes and an increase in leakage current. Hence, the presence of these technological challenges hamper the uptake of bipolar 4H-SiC devices.

Having introduced the electrical parameters of SiC, a focus will now be set on the epitaxial growth and material weaknesses which hamper the further uptake of commercial 4H-SiC devices.

2.3 EPITAXIAL GROWTH OF 4H-SIC USING CVD

Since this thesis focuses on the interfaces of 4H-SiC and performance of power devices, the production of SiC boules via sublimation growth method and their dicing into substrates will not be further discussed here.

The first major process of relevance to the work herein is CVD, used by chip manufacturers for the growth of 4H-SiC epitaxial layers.

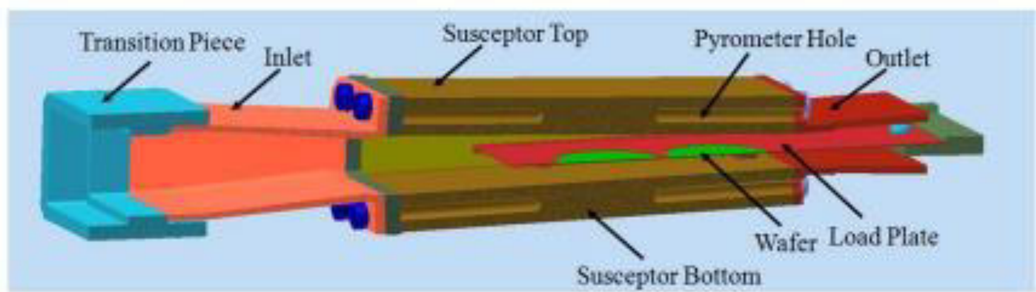


Figure 2.5: Schematic of a typical hot-wall vertical CVD reactor, where the substrate is located on the load plate at the centre of the reactor [13].

In Fig. 2.5 [18], the layout of a typical horizontal hot-wall CVD reactor is shown. Typical Si and carbon (C) precursor gases employed in this process are silane (SiH_4) and propane (C_3H_8) or ethylene (C_2H_4), respectively. These precursor gases are transported into the chamber by a carrier gas, usually hydrogen (H_2), where they decompose and the resulting subspecies are adsorbed onto the substrate surface. On the surface they have enough energy to find a preferential bonding site. To increase the growth rate in standard layers, Cl is added to the Si precursor, which prevents its problematic decomposition at low temperature[19, 20]. The SiC substrates are placed on a high temperature tolerant susceptor, which will be loaded into the chamber.

Layers are then typically grown at 1650°C [18], with pressure between 100-1000 mbar [21] at growth rates up to 100 μm/h, when using trichlorosilane (HCl_3Si) as Si precursor and C_2H_4 as C precursor [18].

Aluminium (Al) and nitrogen (N) are commonly employed as dopants in this system, where doping concentrations from 5×10^{14} cm^{-3} up to 1×10^{20} cm^{-3} can be achieved. For device applications, the process has to be optimised to precisely control layer thicknesses and doping levels across the entire wafer diameter (usually up to 6”).

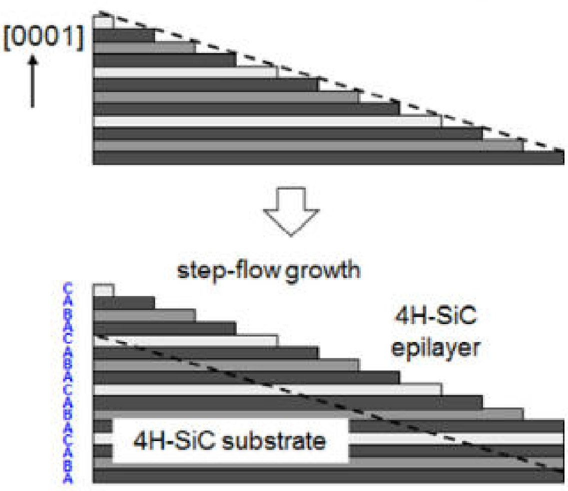


Figure 2.6: Schematic of the step flow growth on layers grown on a 4H-SiC substrate, from [22].

To achieve polytype control during the epitaxial layer growth, layers are grown on substrates that are cut at a 4° off-angle towards the (0001) plane, as shown in Fig 2.6 [22]. Here, homo-epitaxial growth can be achieved using step flow growth, where the stacking sequence of the substrate serves as a template for epitaxial layer growth [23].

Although the material quality of 4H-SiC layers has been improved significantly over the past decades, there are still relevant concentrations of material discontinuities in the crystal lattice, defects, in 4H-SiC epitaxial layers. The major types of defects in the epitaxial layers will be described next.

2.4 MATERIAL CHALLENGES IN SIC

Material quality is of the utmost importance when introducing new materials into the semiconductor industry since the presence of any defect has the potential to reduce the electrical performance of diodes and transistors that are fabricated on all of them. Generally, the crystal lattice discontinuities can be classified into zero- up to three-dimensional defects depending on their propagation through the lattice.

Defects that cause irreversible operational damage when located in the active cross-section of a device are called ‘killer defects’ [24].

Amongst these, micropipes were the most destructive type of defect in 4H-SiC until the early 2010s. They comprise of a screw with a hollow core, penetrating through the entire substrate into an epitaxial layer grown on top of this along the (0001) axis. The introduction of step-flow growth, as described in the previous chapter, helped to dissociate these into several, non ‘killer defect’-type, dislocations [25, 26]. The successful reduction of micropipes mean that nowadays commercial wafers have micropipe densities of 0.1 cm^{-2}, while their proliferation around the outer edge means they are virtually eradicated.

Major one-dimensional defects, which are currently dominant in commercial 4H-SiC layers, are threading screw dislocations (TSDs), threading edge dislocations (TEDs) and basal plane dislocations (BPDs), which all propagate from the substrate into the epitaxial layers. TSDs are at the centre of a spiral with the spiral step height of four Si-C bilayers and usually grow alongthe (0001) direction during boule growth [27]. BPDs, as well as TEDs, represent the addition of an extra half-plane into the hexagonal crystal stacking and only differ in terms of their propagation direction. The propagation of all three major dislocations from the substrate into the epitaxial layer can be seen in Fig. 2.7, which also shows

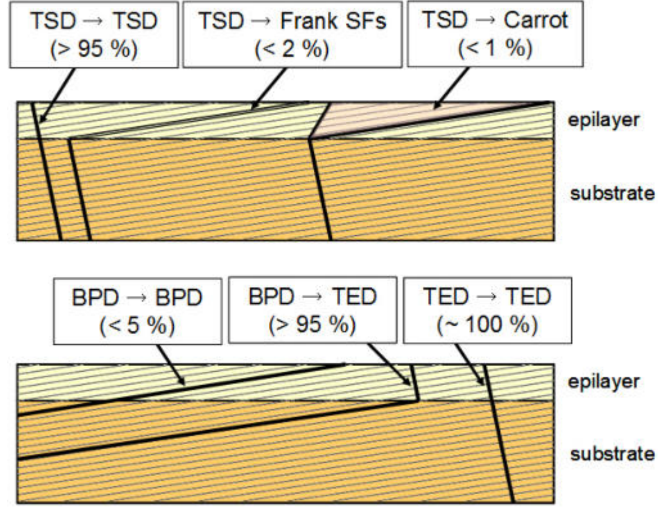


Figure 2.7: Schematic of the propagation of TEDs, TSDs and BPDs and conversion rate of these at the interface between substrate and epitaxial layer, from [22].

some ways they can morph when transitioning from the original wafer to the epitaxial layer. Regarding their impact on practical device performance, both TEDs and TSDs have been shown to increase the leakage in fabricated 4H-SiC SBDs, whilst a high density of BPDs has been shown to increase threshold voltage shift as well as reduce the bulk lifetime in any bipolar device structure. Whilst the TED and TSD density is approximately 2500-6000 cm^{-2} and 300-500 cm^{-2}, respectively, a common BPD density is between 0.1-1 cm^{-2} [24], after 99% of those in

the starting substrate are eradicated within the first ~ 1 micron of growth, known as a buffer region.

The most prominent 2-D and 3-D defects all deleteriously affect device performance, when located in the active area of the device. They include carrots, triangular defects, downfall particles and the aforementioned micropipes (Fig.2.8), which have common defect densities between 0.1-1 cm^{-2} [22]. Their presence increases leakage currents and although their creation is not fully understood yet, it is most likely related to major

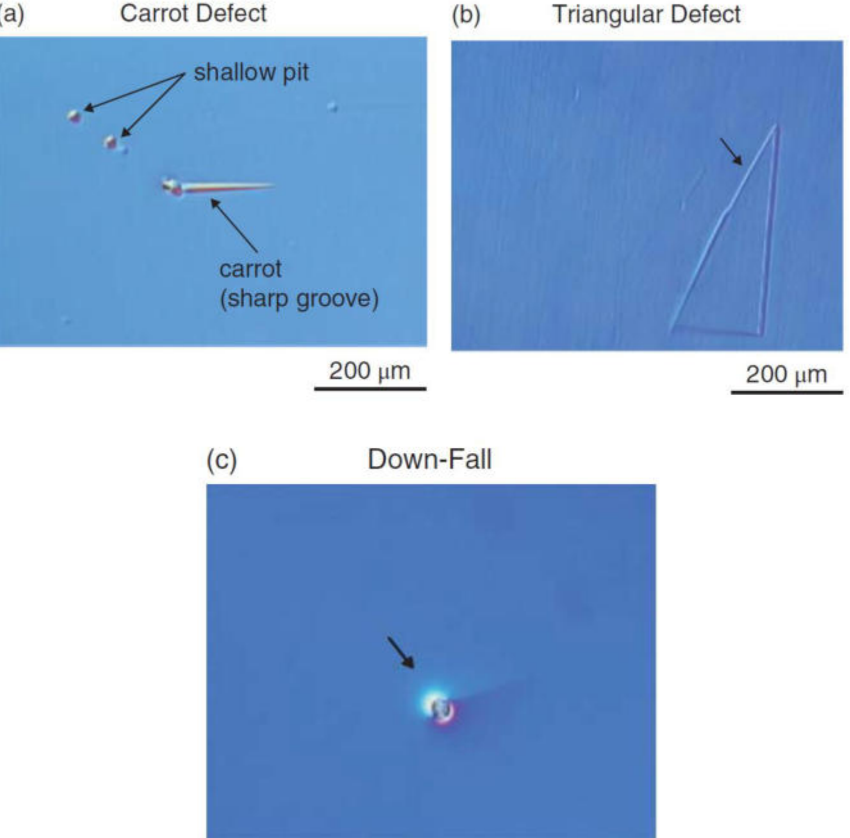


Figure 2.8: Microscopic images of the carrot defect, triangular defect and downfall defect in the epitaxial layers, from [22].

technological issues such as remaining debris from chamber changes, poor surface quality from substrates and non-optimised chamber growth conditions [22].

The last remaining class of 4H-SiC epitaxial defects are point defects, which are vacancies, interstitials, antisites or impurities in the crystal lattice, forming levels which can be deep or shallow. Their location in the upper half of the conduction band is known because conventional deep-level transient spectroscopy (DLTS) is done on n-type material, and vice

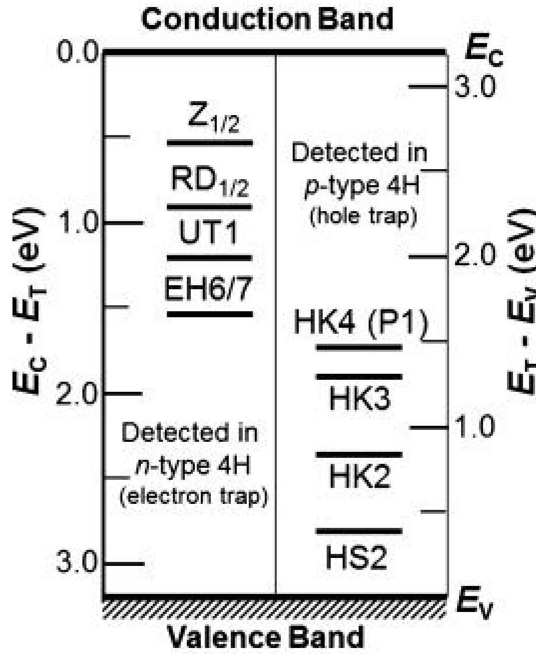


Figure 2.9: Major deep levels in 4H-SiC epitaxial layers, when they are grown 4° off-axis, from [22].

versa for p-type material. An overview of major deep levels in 4H-SiC can be seen in Fig. 2.9.

The major point defects in 4H-SiC epitaxial layers are the $Z_{1/2}$ centre and, to a lesser extent, the $EH_{6/7}$ centres, which typically have defect densities in the 10^{13} cm^{-3} order. The $Z_{1/2}$ centre has been identified to be the major lifetime killer in bulk 4H-SiC epilayers [28], since it is thought to act as a recombination centre close to the conduction band edge, increasing the importance of eradicating the defect, especially for bipolar applications in IGBTs and thyristors as well as the body diode of the SiC MOSFET. Both the $Z_{1/2}$ and $EH_{6/7}$ centres originate from carbon vacancies

within the lattice structure, differing in their respective charge states [29, 30].

Having introduced the major defects in 4H-SiC epilayers, introduced next are the different types of 4H-SiC device relevant to the investigations described in this thesis.

2.5 SIC DEVICES

To evaluate the use of a semiconductor device, some general performance indicators exist in a circuit. In the off-state, all power devices need to block a voltage up to a rated breakdown voltage (V_B) and keep the leakage current value I_R below a defined current level at V_B.

In the on-state, the forward voltage drop V_F must not be higher than a defined nominal current, hence on resistance (R_{ON}) must be minimised. During switching, devices must be able to switch between V_B and V_F in a time t_{ON}, and vice versa from V_F to V_B in a time t_{OFF}. Losses must be minimised during these transitions. In addition, these devices must be able to constantly operate at an operating temperature T. Furthermore, a certain device area A and device cost shall not be exceeded.

Within this parameter range, a trade-off and balance needs to be found between related parameters. For example, a change from unipolar to bipolar devices might reduce R_{ON}, and hence lowering conduction losses, but it will also increase t_{ON} and switching losses. Typically, the modification of one parameter will improve one performance indicator at the detriment of another, which raises the importance of device designs that are suited to their specific application. At first, the next subsections will introduce the different sorts of Schottky barrier diodes, with all described cross-sections shown in Fig. 2.10.

2.5.1 Schottky Barrier Diodr

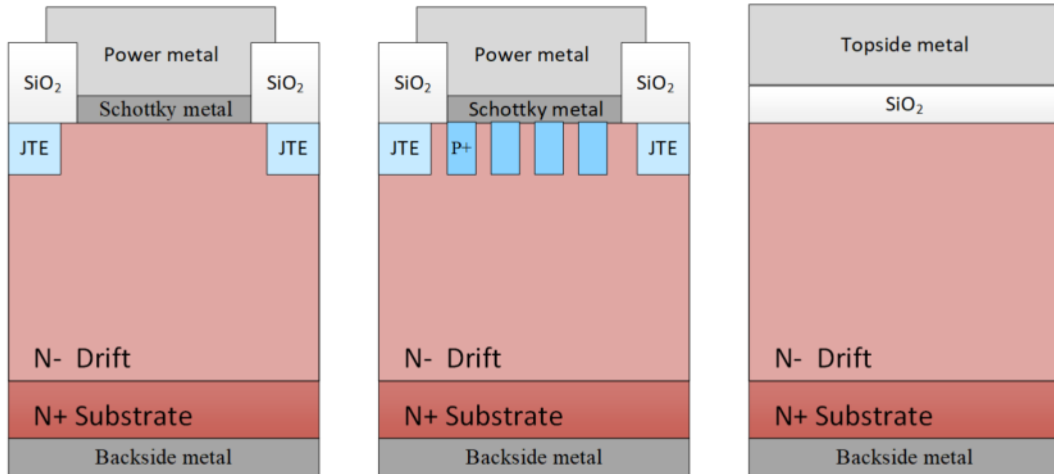


Figure 2.10: Cross-sectional view of the described device structures Schottky barrier diode (left), merged pin Schottky or junction barrier Schottky (middle) and metal-oxide-semiconductor capacitor (right).

As unipolar devices, SBDs only rely on majority carriers for their operations. This enables their use in fast-switching operations since no electron-hole recombination takes place. However, this also means that no conductivity modulation takes place, meaning that conduction losses will be higher for Schottky diodes compared to equivalently rated PiN diodes. This basic trade-off dictates the blocking voltage range at which these devices are employed in the power device market. Up to 200 V blocking voltage, most commercial Si diodes are Schottkys, above which PiN diodes are employed. SiC Schottky diodes are available in the blocking voltage range from 600-1700 V, some even at voltages up to 3300 V. This is at the low to medium blocking voltage end of SiC diodes, with SiC PiN diodes having been demonstrated that could block up to 27 kV[31].

The V_B of a SBD is directly dependent upon a thick lightly n-doped epitaxial region. Increasing V_B, and hence the drift region, therefore comes at the expense of an increase in $R_{ON,SP}$, which constitutes a basic trade-off in Schottky diode behaviour. Before the diode can be turned on,

a forward voltage (V_F) greater than the potential barrier at the Schottky interface must be overcome, and , the choice of Schottky contact metal (at the anode) with its individual work function is another fundamental design parameter in governing V_F. Schottky barrier diodes feature heavily throughout this thesis and their interfaces are being investigated in Chapter 3 and Chapter 4. The theory of the Schottky contacts will be introduced later in this Chapter.

2.5.2 Merged PiN Schottky and Junction barrier Schottky diodes

Merged PiN Schottky (MPS) diodes utilise a Schottky contact on a lightly doped n-region with intermittent p+ stripes. Usually implanted, if an ohmic contact can be formed to the P+ regions then the diode appears as a Schottky in parallel with a pin diode [32]. Since they are using both the characteristics of a Schottky and PiN diodes, their design is an attempt to benefit from the advantages of both unipolar and bipolar device action. Turning on first as a Schottky with low V_F, hole injection at voltages higher than the p-n junction built-in potential, reduces $R_{ON,SP}$. The p+ stripes also aid with the reduction of leakage current in the off-state as the P+- regions keep the peak electric field from the surface. The main design task for this device type is to balance the fraction of Schottky contact and PiN contact in the cell structure in the active area. A wide fraction of p+ will lead to a decrease of I_R whilst simultaneously increasing $R_{ON,SP}$ and vice versa [33].

A Junction barrier Schottky (JBS) diode is the same structure but no attempt is made to make an ohmic contact to the P-regions, instead, they are there purely to reduce the surface electric field in the off-state. The vast majority of commercial devices are JBS diodes.

2.5.3 Metal-oxide semiconductor capacitors

Metal-oxide-semiconductor capacitors (MOSCAPs) are probably the most widely used semiconductor test structure to investigate the quality of a dielectric-semiconductor interface, alongside the MOSFET itself. A MOSCAP is formed when a dielectric layer is grown or deposited on a semiconductor material, which is then topped with a metal layer. The impedance of the MOSCAP at variable DC voltage is then analysed to assess deviations from the 'ideal' CV-response. This can then be correlated to trap levels at or near the oxide-semiconductor interface, e.g. when a high amount of fixed charge is present in the oxide, a DC voltage shift can be seen which is proportional to the density of fixed charge.

Now that all device structures have been introduced, the theory behind the analysis of Schottky interfaces as well as oxide-semiconductor interfaces will be presented.

2.6 SCHOTTKY INTERFACE THEORY

When semiconductors and metals are combined, a potential barrier is formed, a Schottky barrier, named after Walter H. Schottky who introduced the mathematical relationships governing the interface in Germany in the 1930s[34]. A schematic overview of the energy levels at a metal-semiconductor interface can be seen in Fig. 2.10, both at t=0 (top) and at steady state (bottom).

For an electron to flow from the semiconductor into the metal, it must go over (or through) the potential barrier in this depletion region, named the built-in potential V_{BI} of a metal-semiconductor junction. According to Fig. 2.10, the relationship between V_{BI} and the Schottky barrier height $\Phi_{B,n}$ is as follows [33]:

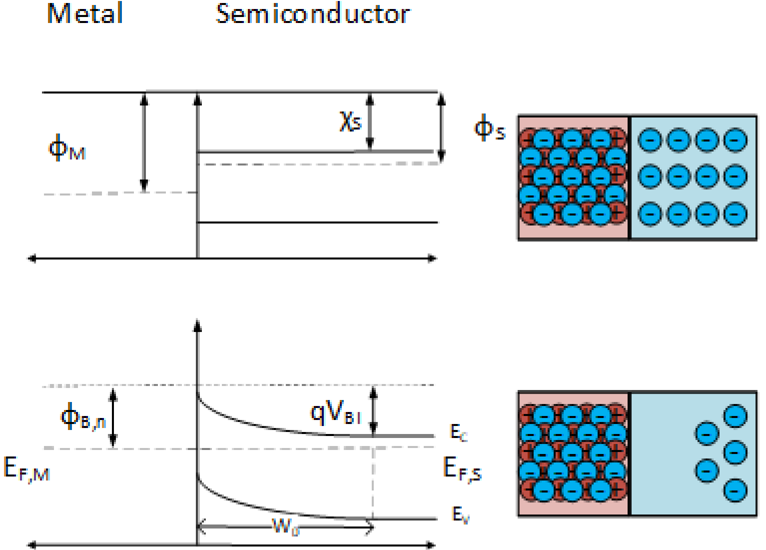


Figure 2.11: The Schottky metal-semiconductor interface involving a moderately lowly n-doped semiconductor. (Top) The interface instantly after connection at t=0, prior to a steady-state, and (bottom) after the formation of a depletion region, with χ_S – the semiconductor electron affinity, φ_S – Difference between vacuum level and Fermi level in the semiconductor, φ_M – Difference between vacuum level and Fermi level in the metal, $\varphi^0_{B,n}$ – theoretical maximum metal-semiconductor barrier height without consideration of effects such as barrier height lowering, E_C and E_V- conduction band and valence band, respectively, and φ_N – the potential difference between the conduction band level and Fermi level in the n-type doped semiconductor.

$$\Phi_{B,n} = qV_{BI} + \left(E_C - E_{F,S}\right) \quad (2.1)$$

where E_C is the conduction band energy and $E_{F,S}$ is the Fermi level in the semiconductor.

Also, the Schottky barrier height can be expressed differently:

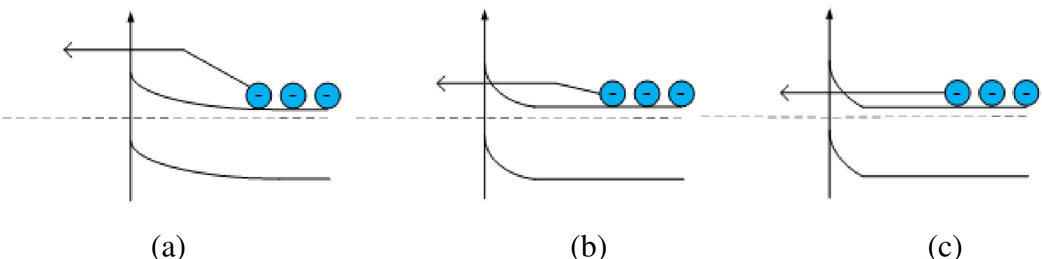
$$\Phi_{B,n} = \Phi_M - \chi_S \text{ (2.2)}$$

With χ_S being the semiconductor electron affinity and φ_M the difference between the vacuum level and the Fermi level in the metal. In the next section, the different current transport mechanisms will be demonstrated.

2.6.1 Current transport across the Schottky barrier

The current transport across the metal-semiconductor barrier in Schottky diodes relies almost entirely on majority carriers. When applying a voltage across the Schottky diode, a current flow across the metal-semiconductor interface results. The doping level in the semiconductor will determine the width of the depletion region W and hence the relevant current flow mechanism at the interface.

In Schottky diodes, thermionic emission (TE), thermionic field emission (TFE) and field emission (FE) are the major current transport mechanisms. Fig. 2.11 shows the relationship between doping levels and current transport mechanism, from a low doping level and thermionic emission at one end, to a relatively high doping level and field emission at the other end. Thermionic emission is the most common mechanism in Schottky contacts due to most diodes using lowly n-doped ($<1e^{16}$ cm^{-3})



(a) (b) (c)

Figure 2.12: Band diagram schematic of the three dominant current transport mechanisms (a) thermionic emission, (b) thermionic field emission and (c) field emission.

epitaxial layers. By applying a bias across the contact, the electrons see a drift decreasing the barrier and increasing their respective energy level,

enabling current flow over the Schottky barrier. When a reverse bias is applied, the energy barrier is too high to overcome, although a minority carrier leakage current is present, and its minor role in the transport is considered for completion.

In the forward conduction, the current flow from the semiconductor to the metal can be described with the following relationship [33, 35]:

$$J = A^{*}T^{2}e^{-\left(\frac{q\Phi_{B,n}}{kT}\right)}\left(e^{\frac{qV}{kT}} - 1\right) (2.3)$$

with J - current density, A*- effective Richardson's constant, T – absolute temperature, k – Boltzmann's constant, V – applied bias. When introducing the saturation current J_S covering the first factor, the equation can be re-written to

$$J = J_S\,(e^{\frac{qV}{kT}} - 1)(2.4)$$

where

$$J_S = A^{*}T^{2}e^{-\left(\frac{q\Phi_{B,n}}{kT}\right)}(2.5)$$

Equation 2.3, when rearranging with Eq. 2.5, can often be found in literature in a simplified version, being valid for voltage values greater than 3 kT/q in Equation 1.28 a in [36], which is the case throughout this thesis:

$$J = J_S\,e^{\frac{qV}{kT}}(2.6)$$

Fig. 2.11 (c) shows a completely different transport mechanism, where a highly-doped semiconductor results in a very narrow depletion region. As a result, electrons are able to quantum-mechanically tunnel

through the very narrow barrier, an effect that is named field emission. This effect is employed in ohmic contacts, where metals are deposited on highly doped semiconductors. In between those two current transport mechanisms is thermionic field emission, where the doping level in the semiconductor means that field emission occurs once the electrons have had a slight energy increase and hence do not have to move all the way over the barrier. The apparent conduction mechanism in a device can be calculated using the E_{00} tunneling energy of the semiconductor, which then needs to be compared to the thermal energy kT, using the following relationship[35]:

$$E_{00} = \left(\frac{q\hbar}{2}\right)\sqrt{\frac{N_D}{\epsilon_S m^*}} \quad (2.7)$$

where E_{00} – is the tunnelling energy of the semiconductor, $\hbar$ is the reduced Planck's constant and m^* is the tunnelling effective mass, which is approx. $0.77m_0$ with m_0 – effective electron rest mass [37]. Once this value has been calculated, TE is said to dominate when $E_{00} \leq 0.5$ kT, whereas FE will dominate when $E_{00} \geq 5$ kT [38].

2.6.2 Ideality factor

In Equation 2.3, the current flow across a Schottky junction is presented when only thermionic emission occurs. This is the most dominant mechanism in 4H-SiC SBDs or JBDs due to the low doping levels in their epitaxial layers. However, this does not take into account real imperfections at the Schottky contact such as the appearance of other mechanisms or contact inhomogeneities [39]. These will cause a deviation from the ideal on-state behaviour which can be plotted using Equation 2.3, causing a decrease in logarithmic slope during the on-state or other features such as double bumps. This is why an ideality factor η is

introduced into the equation 2.3 [40], shown in Equation 2.8, with the observed current being completely dominated by thermionic emission when the ideality factor is as closely to 1 as possible. Whilst also considering the impact of the image force phenomenon (image force lowering), the following equation can be derived [36]:

$$J = J_S\, e^{\frac{qV}{\eta kT}}\left(1 - e^{-\frac{qV}{kT}}\right) (2.8)$$

Which in literature is often being written in the form below, which is a scientifically robust approximation for V> 3 kT/q:

$$J = J_S\, (e^{\frac{qV}{\eta kT}} - 1) (2.9)$$

Whereas the same restrictions apply to this Eq. 2.8 and 2.9 as to equation 2.6[36].

Whenever Schottky interfaces were considered and modelled throughout the thesis, ideality factors and SBHs were calculated considering the mathematical relationships describing the current transport mechanisms in the on-state, which were outlined in this chapter.

2.7 METAL-OXIDE-SEMICONDUCTOR (MOS) INTERFACE THEORY

For characterisation of fabricated MOSCAPs, the underlying physical theory needs to be considered. MOSCAPs are used to extract information about the oxide-semiconductor interface and are widely used because they allow for complex analyses of charge behaviour within the oxide and at the interface whilst they only require a simplistic device geometry. The fabrication only involves the growth or deposition of an insulating layer followed by a metal layer on top of the insulator, and one the semiconductor backside. This relatively simple device structure then

allows for the extraction of charge quantities near the interface and in the insulator when variable DC voltages are applied, and impedances are detected at these varying voltage values. Since power MOSFETs employ the same interfaces, MOSCAPs have been and will be essential in the further reduction of charged states near the interface and an improvement of gate oxide lifetimes in 4H-SiC MOSFETs.

All diagrams and descriptions in these sections refer to n-type SiC, as used herein.

2.7.1 Ideal C-V MOSCAP response in 4H-SiC

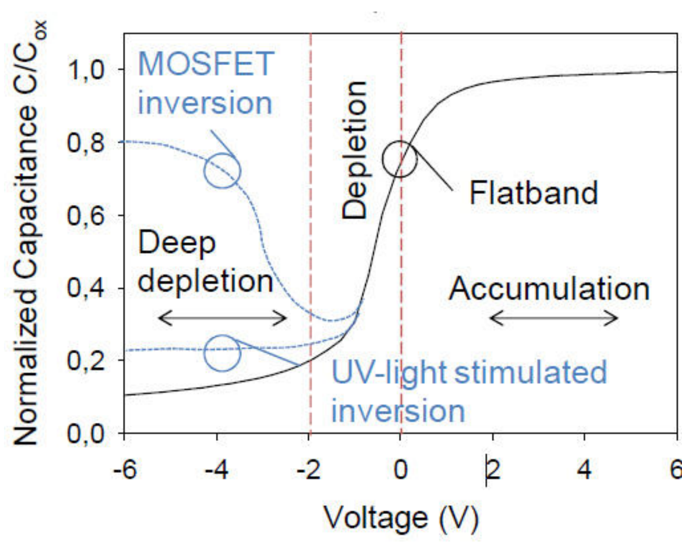


Figure 2.13: Schematic representation of an ideal C-V response of an n-type SiC MOSCAP (black), showing the accumulation, flatband and deep depletion section, from [33].

A significant part of the analysis of the interface and oxide quality stems from a comparison of the capacitance-voltage (C-V) curve of 4H-SiC MOSCAPs to the ideal C-V response. The C-V curve is comprised of DC voltage-dependant capacitance, measured by applying a small AC current, superimposed on the DC bias. An example of an ideal C-V response of an ideal n-type 4H-SiC MOSCAP can be seen in Fig. 2.12, from [41]. The different regimes will be briefly described in the next paragraphs, whereas the inversion regime will only be mentioned here

since it is not observed in SiC MOSCAPs under normal temperature and optical excitation operations. In the absence of source/drain regions (which have opposite doping polarity to the body), the inversion layer cannot be formed because the intrinsic minority carrier concentration and generation rate in SiC are too low to supply enough minority carriers for an inversion layer. In MOSFET structures, minority carriers are supplied from the source and/or drain regions. Under optical excitation and/or elevated temperature, there can be sufficient supply of minority carriers to form an inversion layer.

2.7.2 Accumulation regime

The application of a positive gate bias on an n-type MOSCAP will attract electrons in the semiconductor towards the oxide-semiconductor interface, as shown in Fig. 2.13. Energetically speaking, the bands in the

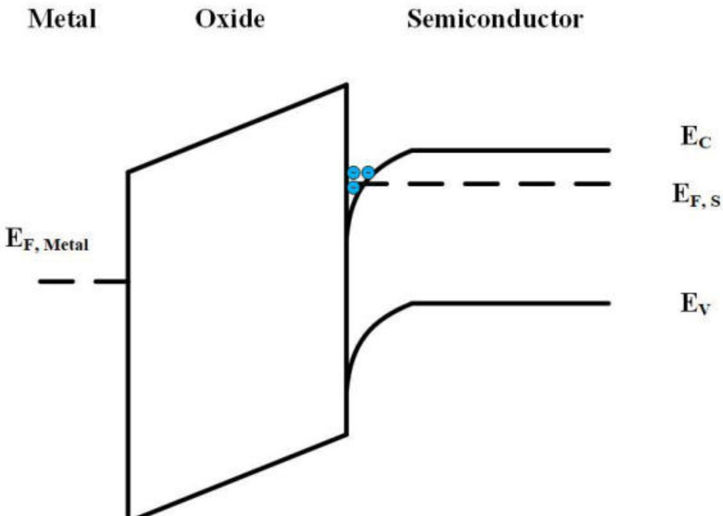


Figure 2.14: Band diagram of an n-type 4H-SiC MOSCAP in accumulation.

semiconductor bend down and make it more favourable for electrons to accumulate at the oxide-semiconductor interface in the conduction band. In the accumulation regime, the electric field drop will then mainly occur in the oxide and the entire capacitance can be regarded using the parallel plate capacitor analogy, as if the semiconductor were a metal. It is

assumed that the maximum capacitance in deep accumulation, once saturated, is the oxide capacitance, C_{OX}.

2.7.3 Depletion regime

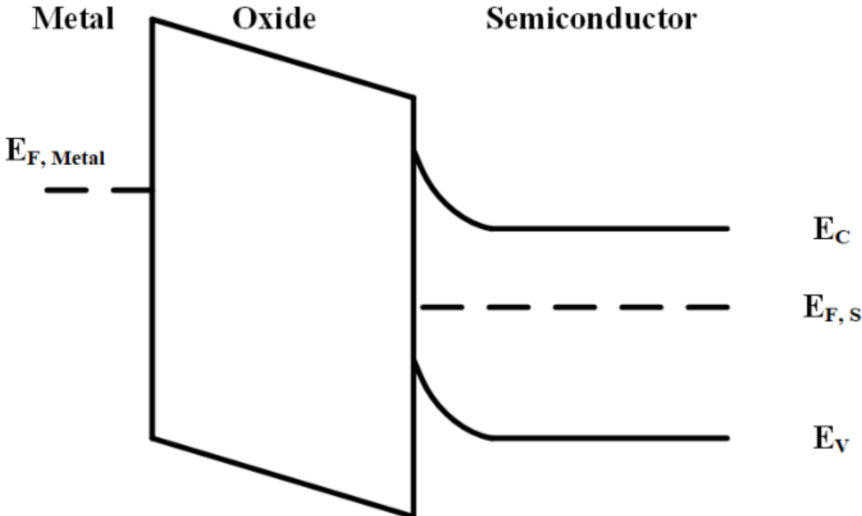


Figure 2.15: Band diagram of an n-type 4H-SiC MOSCAP in depletion.

When the gate bias is reduced from a strong positive bias to a negative bias, the band bending is reduced until the bands are bending into the opposite direction. Electrons are repulsed from the interface, forming a depletion region. This is similar to a parallel plate capacitor widening, causing a reduction of capacitance. Here, the concentration of dopants in the drift region affects the slope of capacitance (dC/dV). The schematic of the MOSCAP in deep depletion can be seen in Fig. 2.14.

2.7.3 Flatband regime

At the flatband point, no band bending occurs. The schematic at flatband regime can be seen in Fig. 2.15.

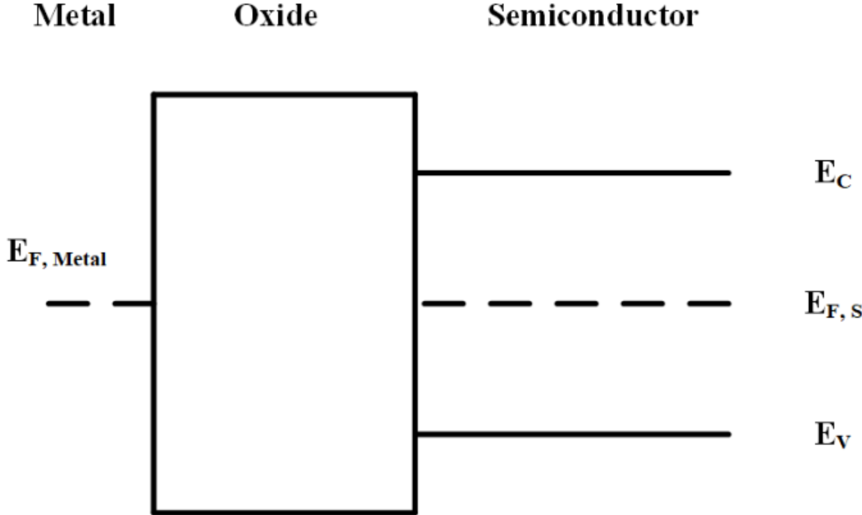


Figure 2.16: Band diagram of an n-type 4H-SiC MOSCAP in flatband mode.

In ideal structures such as the ones described by Fig. 2.15, the flatband voltage is determined by the work function difference between the metal and the semiconductor Φ_{MS}. The deviation of flatband voltage from this ideal value is caused by different charge types, which are explained in more detail in the section below, can be seen in the flatband voltage equation 2.10 [38]:

$$V_{FB} = \Phi_{MS} - \frac{Q_F}{C_{OX}} - \frac{Q_{IT}(\Phi_S)}{C_{OX}} - \frac{1}{C_{OX}}\int_0^{t_{OX}} \frac{x}{t_{OX}} \rho_m(x)dx - \int_0^{t_{OX}} \frac{x}{t_{OX}} \rho_{OT}(x)dx \quad (2.10)$$

With V_{FB} – Flatband voltage, Φ_{MS} – work function difference between metal and semiconductor, $Q_{F, IT, M, OT}$ – Fixed, interface trapped, mobile or oxide trapped charge, respectively, t_{OX} – thickness of the oxide, ρ (x) –

oxide charge per unit volume, $Q_{IT}(\Phi_S)$ – considering, that the interface trapped charge occupancy depends on the surface potential.

2.7.3 Trapped charge and its impact on C-V responses

Charge in the oxide and at the interface between oxide and semiconductor does often create deviations in the C-V response of 4H-SiC MOSCAPs such as the flatband voltage and increases leakage current levels, lowers channel mobilities in MOSFET structures and decrease the lifetime of MOS-based devices. To address these issues, the bulk of the analysis of 4H-SiC MOSCAPs focuses on obtaining information on the presence of charge quantities and to establish ways to reduce these quantities.

The presence of charge within the bulk of the oxide and at the oxide-semiconductor interface can be classified into four categories, according to Schroder [38] (Q in C, N in cm^{-2}, D in cm^{-2} eV^{-1}) :

1. Fixed oxide charge (Q_F, N_F).

2. Mobile oxide charge (Q_M, N_M).

3. Oxide trapped charge (Q_{OT}, N_{OT}).

4. Interface trapped charge (Q_{IT}, N_{IT}, D_{IT}).

The fixed oxide charge is covering charge that does not vary depending on the device operation and, when present, shifts the C-V curve in the 'x (voltage) axis', usually introduced by the oxide process. A key electrical parameter to give an indication of the presence of fixed oxide charge in the insulator is the flatband voltage V_{FB}. In an ideal MOSCAP, V_{FB} is

usually close to 0 V and mainly depending on work function differences, meaning that there are no fixed charge quantities present in the MOSCAP.

Mobile oxide charge originates from ionic impurities, mainly sodium, lithium, potassium and hydrogen, and have the electrical ability to diffuse through the entire insulating layer. When present, these ions have the biggest impact on high-temperature electrical behaviour causing a poor time-dependent dielectric breakdown (TDDB) performance. Once in the oxide, it cannot be eliminated but a reversible ion movement is possible. When devices are fabricated in a well-controlled clean room environment, their presence can be almost eliminated.

Oxide trapped charge originates from the presence of holes or electrons in the oxide and arguably the culprit in hysteresis and TDDB (alongside mobile ionic charge) and is often also described as 'near interface trap'. In Si-SiO_2 systems , unlike fixed oxide charge, it can often be eliminated when annealing below 500°C is being carried out [38].

Of the greatest relevance in SiO_2/4H-SiC systems is the presence of interface trapped charge, since it is electrically active and reacts with the semiconductor structure underneath. Interface trapped charge generally covers structural defects and oxidation induced defects as well as metal impurities in some instances. They are about two to three orders of magnitude higher in SiO2/4H-SiC systems than in Si systems and their presence is related to imperfections of the thermal oxidation process in SiC, which ends up with residual carbon, dangling bonds and oxidation induced defects at the interface. Interface-trapped charge is highly electrically active and located close to the conduction band edge [24]. They are the source of serious interface challenges in SiC, such as low electron channel mobility in SiC MOSFETs and reliability issues with

SiO_2 in SiC MOSFETs. Their extraction methods are described in section 2.8.2.

The next section will now cover the electrical and physical characterisation techniques which were used throughout the thesis.

2.8 ELECTRICAL CHARACTERISATION TECHNIQUES

Although the physical characterisation techniques introduced later can provide information on possible explanations of a device performance, the electrical characterisation of a semiconductor device is the backbone of semiconductor analysis, which is why they will be introduced first.

2.8.1 I-V analysis

The majority of on-state analysis of diodes described in this thesis were performed on an Agilent Technologies B1500 A Semiconductor Device Analyser, which was setup for vertical device measurements. Here, the conducting back stage was used as a backside contact. To extract a low

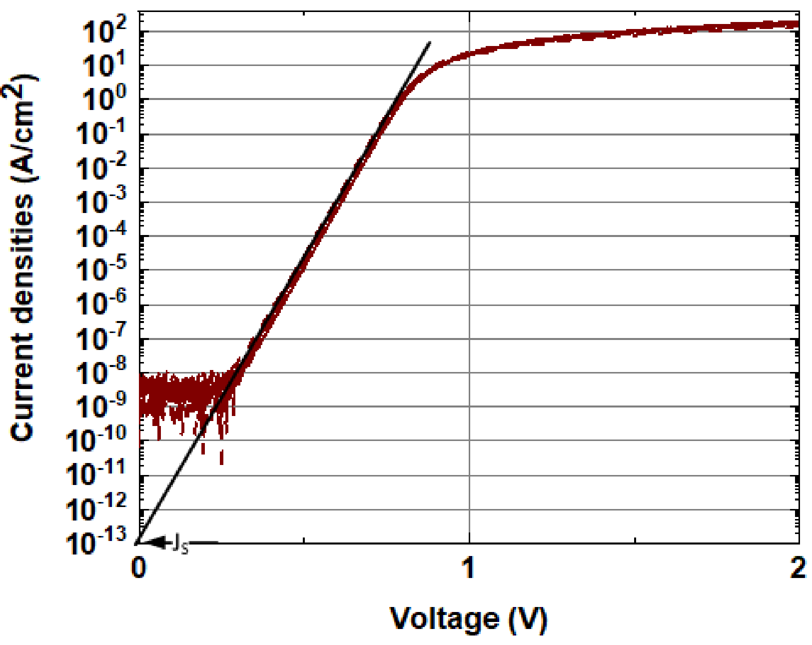


Figure 2.17: Logarithmic current trace of a typical n-type 4H-SiC SBDs in the on-state with J_S – Saturation current density and the ideality factor and SBH extraction method indicated.

voltage sweep to extract ideality factors, barrier heights and on-state resistances, a specified DC voltage is applied across the diode and its DC current will then be measured. This is then carried out over a specified voltage range, e.g. from 0 to 5 V, where the current is limited by the individual Source Measuring Unit (SMU), which was 100 mA in this instance. The voltage limit of these units was 200 V. In Fig. 2.16, a typical current trace of a 4H-SiC SBD can be seen, with the linear region in the logarithmic current range being dominated by the thermionic emission regime, when Eq. 2.3 and Eq. 2.5 can be rearranged to

$$J = J_S\left(e^{\frac{qV}{\eta kT}} - 1\right) \quad (2.8)$$

where J_S has been defined in Eq. 2.5. Fig. 2.14 shows that the saturation current density can also be modelled/read off at the intersection between the linear graph and the x-axis. Equation 2.5 can then be rearranged to extract the barrier height ϕ_{BN}. Once the barrier height has been extracted, Eq. 2.8 can then be rearranged to extract the ideality factor. For this method to be within reasonable scientific standards, the voltage resolution steps need to be as high as possible, which is why 1000 datapoints were taken in the on-state throughout the thesis to extract these parameters.

In the off-state, measurements were mainly used to extract leakage currents and device breakdown at higher voltage levels, with no modelling involved. The exact process conditions will be shown in the results Chapters. In the following paragraph, the C-V analysis methods will be explored.

2.8.2 C-V analysis

As outlined in section 2.7, the C-V analysis can be used to extract information on the density of interface states, D_{IT}, as well as quantity of

other charge types. In short, a DC bias is applied across a MOSCAP across a defined voltage range, creating a voltage sweep. Furthermore, a small AC signal is applied on top of this signal and the magnitude and phase are analysed to extract the capacitance and conductance at each defined voltage step. Throughout the thesis, capacitances were measured using a Keysight/Agilent E4980A LCR meter capable of measuring at frequencies from 20 Hz up to 2 MHz. In the first part of this section, the high-low as well as the conductance method will be introduced as means to extract the relevant charge densities. Figure 2.17 presents the equivalent circuit used to derive the equations for the high-low method.

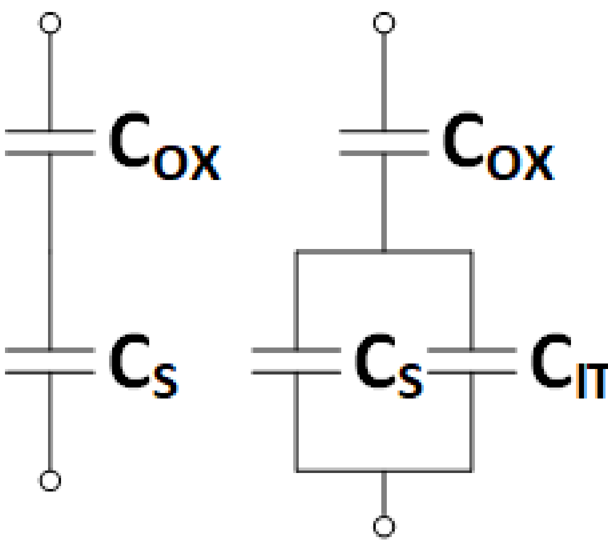


Figure 2.18: Equivalent circuit of the ideal MOSCAP (left) and the circuit used for the high-low technique.

The main assumption behind the application of this technique is that the interface states do follow the AC excitation and respond to measured low frequencies (≤ 1 kHz) whereas they do not respond at all at high frequencies (≥ 1 MHz). In other words, the high-low method considers the low capacitance to be the sum of MOSCAP capacitance plus capacitance of interface traps, whilst the high frequency is just MOSCAP capacitance. Based on the equivalent circuit in Fig. 2.17, the capacitance of low

frequency capacitance of the MOSCAP, C_{LF}, can be expressed by Equation 2.9 [24]:

$$C_{LF} = \frac{1}{\left(\frac{1}{C_{OX}}\right) + \left(\frac{1}{C_S + C_{IT}}\right)} (2.9)$$

with C_S- semiconductor capacitance (F), C_{OX} – oxide capacitance (F), C_{IT} – capacitance of interface traps (F). With $D_{IT} = C_{IT}/q^2$, Equation 2.9 can be rearranged to give the following mathematical relationship:

$$D_{IT} = 1/q^2 \left(\frac{C_{OX}C_{LF}}{C_{OX} - C_{LF}} - C_S\right) (2.10)$$

Assuming that C_{IT} can be ignored at high frequencies, the following total semiconductor capacitance at high frequencies is shown in Eq. 2.11, where C_{HF} is the high frequency capacitance of the MOSCAP.

$$C_S = \frac{C_{HF}C_{OX}}{C_{OX} - C_{HF}} (2.11)$$

This can then be inserted into equation 2.10.

$$D_{IT} = C_{OX}/q^2 \left(\frac{C_{OX}C_{LF}}{C_{OX} - C_{LF}} - \frac{\frac{C_{HF}}{C_{OX}}}{1 - \frac{C_{HF}}{C_{OX}}}\right) (2.12)$$

Once the densities of interface traps have been calculated, they have to be put in context to their respective position within the energy band diagram. According to Schroder [38], the surface potential can be calculated using an adapted Berglund equation when integrating around the flatband voltage, resulting in the following equation:

$$\varphi_S = \int_{V_{FB}}^{V_{GS}} \left(1 - \frac{C_{LF}}{C_{OX}}\right) d\,V_{GS} \quad (2.13)$$

The result obtained can then be converted into a real energy position below the conduction band edge, the exact derivation of this process can be found in [38].

In summary, the high-low method offers a convenient technique to extract interface trap level densities. It offers only a limited trap level range under the conduction band edge, which is usually presented at a trap level underneath the conduction band edge, E_C-E_T, of 0.2 eV – 0.6 eV.

This method shown to have certain disadvantages in SiC such as a higher time constant dispersion in SiC as opposed to Si, which shifts the surface potential towards the majority carrier band edge [42, 43]. The same reports also demonstrate that very fast interface states in SiO_2/4H-SiC which respond to frequencies up to 1 MHz, contradicting the general assumption of this technique. Furthermore, the calculation of surface potential in this technique shows a very wide distribution of surface potential and demonstrates a high dispersion of time constants, which causes an extension of the transition phase from high frequency to low frequency. Hence, the described effects can lead to an underestimation of interface traps in SiC. This technique has still been used widely in 4H-SiC since it was embedded into a comparison study and where these disadvantages can be assumed to be distributed evenly across observed the dataset, so that extracted trends are scientifically robust.

The two further methods, which are more widely used in the semiconductor characterisation field are the Terman method and the conductance method [24]. In the Terman method, the calculation of density of interface traps is based on the deviation/comparison of a

measured high-frequency to an ideal C-V curve, calculations using [44]. Since the assumption that interface states in 4H-SiC do have a time constant so they do not compare to high frequencies at all does not hold true in this context[38], this method is not usually used in 4H-SiC [24]. Amongst the Terman and conductance method, only the latter method has proven to show reliable results in 4H-SiC MOSCAPs. The conductance method generally starts by observing the ratio of the parallel conductance over the AC measurement frequency [24]:

$$\frac{G_P}{\omega} = \frac{\omega G_M C_{OX}^2}{G_M^2 + \omega^2 (C_{OX} - C_M)^2} \quad (2.14)$$

where G_P – parallel conductance, ω – AC measurement frequency, G_M – measured conductance. The second fundamental equation of this technique is shown in Eq. 2.15 below [45]:

$$\frac{G_P}{\omega} = \frac{q}{2} \frac{D_{IT}}{\omega \tau_{IT}} \frac{1}{\sqrt{2\pi\sigma^2}} \int_{\infty}^{\infty} \ln(1 + (\omega {\tau_{IT}}^2) e^{2\varphi_s})\, e^{-\frac{\varphi_S^2}{2\sigma^2}}\, d\varphi_S \quad (2.15)$$

with τ_{IT} being the time constant of the trap and σ the surface potential fluctuation. τ_{IT}, σ and D_{IT} in 2.15 must be fitted as a function of ω to the experimental equation in 2. 14.

The conductance method is a thorough and exact technique to extract the D_{IT} levels in 4H-SiC and is hence considered to be more suitable for this purpose than the Terman method, though not being able to accurately measure very fast interface states. In recent years, Yoshioka and Nakazawa also developed the C-Ψ method[43], which showed to accurately evaluate D_{IT} including very fast states generated during nitridation anneals [46], based on a comparison between quasi-static and theoretical capacitances[46] . However, the extensive data, time and

modelling effort required for both the conductance and C-Ψ method meant that they were not applied during the course of this thesis.

2.9 PHYSICAL CHARACTERISATION TECHNIQUES

2.9.1 Secondary Ion Mass Spectrometry

In the semiconductor industry, secondary ion mass spectrometry (SIMS) is a widely employed characterisation technique to determine the chemical composition of a sample. In the context of this thesis, its high sensitivity (detection limit ~10^{15} cm^{-3}) is used to collect information on lattice impurities, such as nitrogen (N), aluminium (Al), phosphorous (P), Si, C, and oxygen (O) concentrations at different sample depths, e.g. either at the Schottky or MOS interface. Its advantage over electrical measurement techniques is that it does not differentiate between electrically active and electrically inactive impurities, hence providing a more precise information on the physical presence of these impurities in the lattice. The simplified schematic of a SIMS machine can be seen in

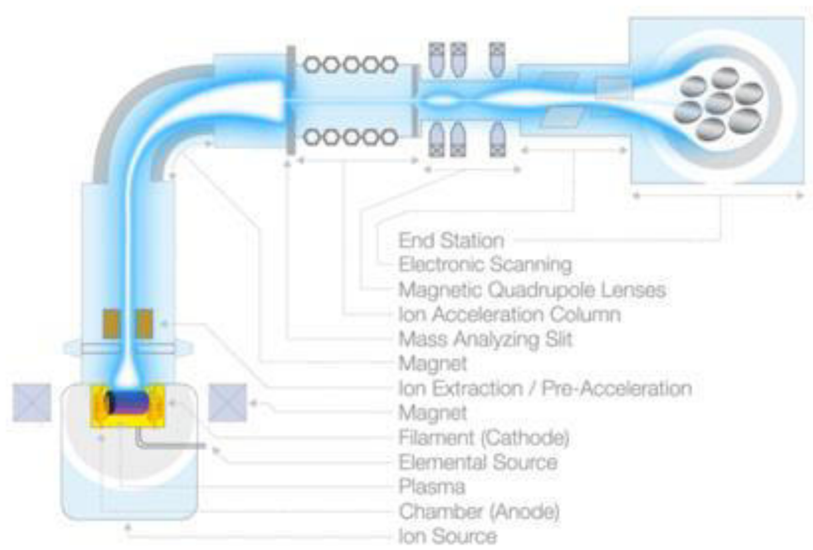


Figure 2.19: Simplified schematic of a SIMS rig [37].

Fig. 2.18 [47]. In a SIMS system, primary ions are deliberately accelerated and used to bombard the sample at such a high energy so they

forcefully eject atoms and ions from the sample structure which can then be detected. These measured ions will then be isolated and counted, resulting in a plot of impurity concentration over sample surface depth. The low detection limit/noise base for most dopants to be investigated in 4H-SiC layers such as N, P, Al is about 5×10^{15} cm^{-3} whilst for other elements such as hydrogen in MOS layers this can be relatively high, e.g. 1×10^{18} cm^{-3}. In this thesis, SIMS has been used to extract atomic concentrations of phosphorus at the Schottky interface as well as hydrogen and oxygen throughout the oxide as well as the interface between oxide and semiconductor in MOSCAPs.

2.9.2 Atomic Force Microscopy

Atomic Force Microscopy (AFM) can be employed to very accurately (resolution down to 0.1 nm) scan the surface topology of a semiconductor sample by scanning a sharp tip across the sample surface. An AFM rig comprises a low spring constant cantilever with a micro-machined contact tip, which follows and responds to variations in surface morphology, as well as a laser that is focused on the end of the cantilever and reflected to a four-quadrant photodetector which measures variations in the laser spot position as the cantilever is deflected. The results are then fed back to a piezoelectric stage, which manipulates the height to minimise the photodiode signal in a closed-loop control system. When both the lateral scanning control and the vertical height feedback control/measurement are merged, two-dimensional images of the surface morphology are created. In the course of this investigation, AFM was used to extract surface roughness values as well as to identify obvious surface decoration features.

2.9.3 Scanning Electron Microscopy

In scanning electron microscopy (SEM), a high energy electron gun is focused onto a small area on the sample surface. The electron beam excites 'secondary' electrons to be emitted from the sample and a detector uses a positively charged cage to attract and detect the secondary electrons. A simplified overview of this process can be seen in Fig. 2.19, from [48]. The build-up of the image can be observed when signals change due to the sample properties such as topography, roughness and density of a sample. Throughout this investigation, SEM is used to investigate the presence of surface decorations and comparing them to AFM densities of

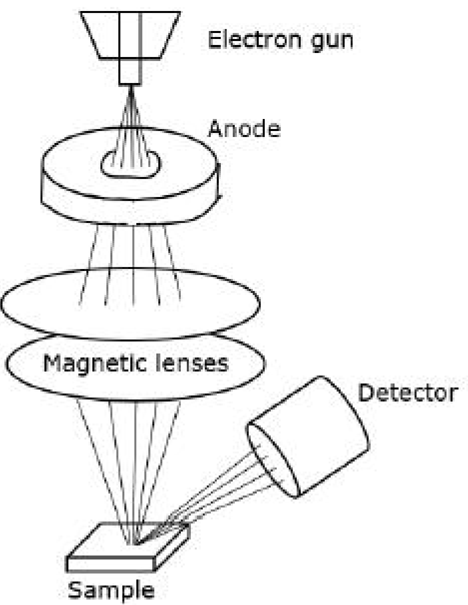


Figure 2.20: Simplified schematic of a scanning electron microscope, from rig [38].

those. In the physical analysis research of 4H-SiC, the ability of SEMs to image cross-sections of finalised device structures is often used.

2.9.4 Transmission electron microscopy

The working principle of transmission electron microscopes (TEM) is similar to that of an optical microscope, in which a sequence of lenses is used to magnify the image of the investigated section of the sample. The main advantage of using TEM lies within its extremely high resolution limits, which approach 0.08 nm [38]. The schematic of a typical TEM can be seen in Fig. 2.20 [38], which can be primarily operated in bright-field,

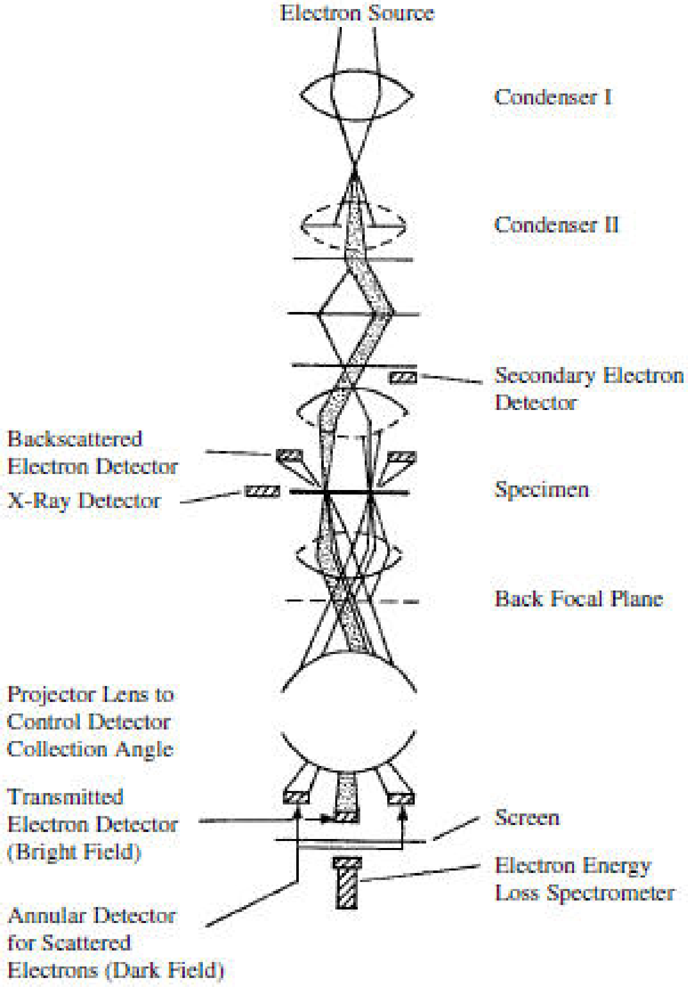


Figure 2.21: Simplified schematic of a transmission electron microscope, from [30].

dark-field and high-resolution imaging mode. The sample preparation is of paramount importance in TEM, since it requires the sample to be thinned for it to be transparent to the electron beam. In the centre of

Fig. 2.20, the electrons are then transmitted and scattered through the thin sample into the back focal plane, under which an image detector or fluorescent screen forms a high-resolution image of the sample.

The sample thinning is usually done using a grinding stage until a sample thickness of about 10 µm is reached. Then, ion milling (Ar) is used to further thin down the sample. For the purposes of this thesis, the focussed ion beam (FIB) technique was used for sample preparation and a JEOL TEM 2100+ system was used for imaging.

2.9.5 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is typically used to measure and characterise the bonding energy which is present in atomic bonds near or at the sample interface. Throughout this thesis, XPS is used to chemically characterise the atomic bonds at the device surfaces in an attempt to correlate the electrical device performance to the chemical bonds. In XPS, primary X-rays of an energy from 1 kV to 2 kV [38] cause the ejection of photoelectrons of the sample. The detected/analysed energy of the measured photoelectrons follow the fundamental relationship, outlined in Schroder [38]:

$$BE = E_{XRAY} - E_{SPECTR.} - q * Work\ function\ spectrometer \quad (2.16)$$

with BE – Binding energy, $E_{X\text{-ray}}$ – the x-ray energy (h*υ), $E_{SPECTR.}$ – measured energy of the detected/ejected electrons.

After having loaded the samples into the XPS chamber, a survey scan across a large energy range at low resolution is carried out to identify the elements in the sample. Emission of electrons from core electron shells form ‘fingerprint’ lines, characteristic to an individual element. Spectra from these core levels are then measured, using high energy resolution to scan the highest-intensity peak for each element of interest. The core

spectra are comprised of a number of components, each representing a different bonding environment, where bonding to an electronegative element like oxygen or fluorine increases binding energy and bonding to an electropositive element like molybdenum decreases binding energy (typically by a few eV). Due to well documented handbooks and binding energy databases, the measured elements and chemical shifts on components can then be identified[49].

The sample spot in XPS is generally approximately 1 mm in diameter, with the probing depth depending on sample density, x-ray energy and the angle at which the survey is done. Since an aluminium (Al) Kα x-ray source is used in this thesis, the probing depth throughout was approximately 10 nm, though the signal from deeper atoms will be attenuated more than surface atoms.

2.9.6 Physical characterisation methodology overview

The following table outlines where and how the aforementioned characterisation methods have been used in the course of this thesis:

Table 2.2: Overview of used characterisation techniques in the course of this thesis.

Characterisation method	**Destructive/ non-destructive?**	**Contracted/ carried out in-house ?**
Secondary Ion Mass Spectrometry	Destructive	Contracted
Atomic Force Microscopy	Non-destructive	In-house / Done by the author
Scanning Electron Microscopy	Non-destructive	In-house / Done by the author
Transmission Electron Microscopy	Destructive	In-house / Done by Yisong Han, Department of Physics at Warwick University
X-ray photoelectron spectroscopy	Destructive	In-house / Done by the author

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3 The improvement of Mo/4H-SiC Schottky diodes via a P_2O_5 surface treatment

3.1 INTRODUCTION

In this Chapter the application of surface treatments prior to metallisation of 4H-SiC Schottky diodes will be studied, with the aim of conditioning the metal/semiconductor interface to improve their electrical characteristics. A successful process is then proposed, which is taken forwards for the fabrication of optimised power diode device structures in Chapter 4. The results of this Chapter have been published in [1, 2].

Improvements to the SiC SBD have, in the main, focused on the choice of the Schottky contact metal, which governs the Schottky barrier height (SBH) at the metal/semiconductor interface [3-6]. The significant impact of the barrier height on the on-state performance can be emphasised by using the equation 3.1 to calculate the forward voltage drop in a thermionic emission dominated system, written in terms of the barrier height and the ideality factor η, according to [3]:

$$V_F = \eta * \frac{kT}{q} \ln\left(\frac{J_F}{AT^2}\right) + \eta\Phi_{B,n} + R_{ON}J_F \qquad (3.1)$$

with V_F – forward voltage drop across the Schottky junction (V), J_F – the total forward current density (A/cm^2) and R_{ON} - the specific on-resistance (Ω.cm^2). By considering this relationship it becomes evident that changing the Schottky contact (hence the barrier height through the choice of metal and its respective workfunction) has a direct influence on the forward voltage drop, hence the on-state power dissipation of the device. In addition to this, the quality of current conduction at the interface, resulting in an ideality factor, has a direct impact on the relationship, too,

e.g. a Schottky contact with current conduction described by an ideality factor close to 1 (considered ideal according to the thermionic emission theory) will show a lower voltage drop than a contact described by a higher ideality factor, hence resulting in lower on-state power dissipation (conduction losses).

Until recently, SiC suppliers have opted for titanium (Ti) and titanium-silicides over nickel (Ni) and nickel-silicides as the Schottky contact metal, resulting in a low SBH and hence minimal turn-on voltage, due to its lower work function compared to Ni (φ_{Ti} = 4.33 eV and φ_{Ni} = 5.04-5.35 eV [7]). However, in the last five years, there has been research and development of molybdenum (Mo) Schottky contacts [6, 8-10] which have a similar work function (φ_{Mo} = 4.36-4.95 eV [7]) but a significantly higher melting point. In particular, Infineon integrated molybdenum nitride (MoN) contacts [10] into their 6th generation of SiC SBDs [11, 12], which was reported to lower the SBH to 0.86 eV, resulting in even lower turn-on voltage at the expense of increased reverse leakage current [11]. Elsewhere however, the Mo/SiC interface was reported to have a barrier height as high as 1.28 eV by Bonyadi *et al.*[13], while in Latreche *et al.*[14] and Lee *et al.[15]* it is 1.01 eV, with a very low ideality factor over a wide temperature range. The authors have previously reported SBH values between 1.27 eV and 1.43 eV [1].

Surface passivation treatments prior to metal deposition have been shown to improve the electrical characteristics of the final diode [1, 14, 16]. In Lee *et al.* [13], prior to the deposition of Ni, a post-oxidation anneal (POA) in nitrous oxide (N_2O) ambient at 1000 C for 2 h, before the removal of the grown oxide, resulted in both a tighter distribution of ideality factors across the measured SBDs and a significant reduction of leakage current densities.

Similar passivation treatments, including annealing in hydrogen, nitrogen, nitrous oxide, or argon ambient, annealing in phosphorous-containing ambients as well as boron incorporations have been employed in metal-oxide-semiconductor (MOS) structures on SiC in an attempt to reduce the density of interface states near the silicon dioxide (SiO_2)/SiC interface [16-20]. Among these methods, annealing in N_2O ambient has been found to be the most effective technique [21]. However, recent reports in the impact of phosphorous pentoxide (P_2O_5) depositions as a surface passivation for SBDs and MOSFETs [1, 22-24] have shown an improvement both in leakage current densities for SBDs and in channel mobility for transistors. As this treatment also improved the on-state performance of the measured devices, the benefits of nitridation prior to metallization of SBDs were exceeded. Hence, it has been shown that pre-treatments of SBDs have the potential to minimise the disadvantages of using anode metals with low barrier height.

3.2 DEVICE FABRICATION AND EXPERIMENTAL PROCEDURE

Mo/SiC Schottky diodes were fabricated to analyse the effect of different passivation treatments on the turn-on and reverse leakage current levels. These were fabricated using highly n-type (nitrogen-doped), 4° off-axis 4H-SiC substrates supplied by Dow Corning, on which a lightly doped (1×10^{15} cm^{-3}) 35 µm epitaxial layer was grown. These starting wafers were diced into 14×14 mm^2 chips and cleaned using a standard RCA 1/ HF (10%)/ RCA 2/ HF (10%) process. Subsequently, one of three passivation routines were applied to the SiC samples:

- 1. The deposition of P_2O_5 in a tube furnace at 1000°C for 2 h, the samples having been mounted on a carrier wafer and placed in front of a silicon diphosphate (SiP_2O_7) source wafer (the P_2O_5 treatment).
- 2. Thermal oxidation in an Ar:O_2 (4 slm:1 slm) ambient at 1400° C for 4 h (henceforth referred to as the O_2 treatment).
- 3. Thermal oxidation in an Ar:N_2O (4 slm:1 slm) ambient at 1300°C for 4 h (the N_2O treatment). A fourth set of control samples was fabricated in parallel, which underwent no passivation treatment.

Next, all the treated samples were cleaned in dilute HF (10%) to remove the oxide layers before the individual active areas of Schottky diodes were defined and mesa-isolated by dry etch. For device insulation, a 1 μm thick SiO_2 layer was deposited by low pressure chemical vapor deposition (LPCVD) using tetraethyl orthosilicate (TEOS) as a precursor, covering the active areas before the contact formation. Ti(30 nm)/Ni (100 nm) ohmic contacts were then formed on the backside of the samples after a rapid thermal anneal at 1000°C for 2 min in Ar (5 slm) ambient. Schottky contacts were then formed by opening a window in the thick SiO_2 layer and evaporating 100 nm of Mo before annealing them at 500°C in Ar (5 slm) ambient. Finally, a 1 μm thick Al metal overlay was evaporated on top of the die, which serves as a field plate. A cross section of the fabricated final device structure can be found in Fig. 3.1, with the process flow being shown in Table 3.1.

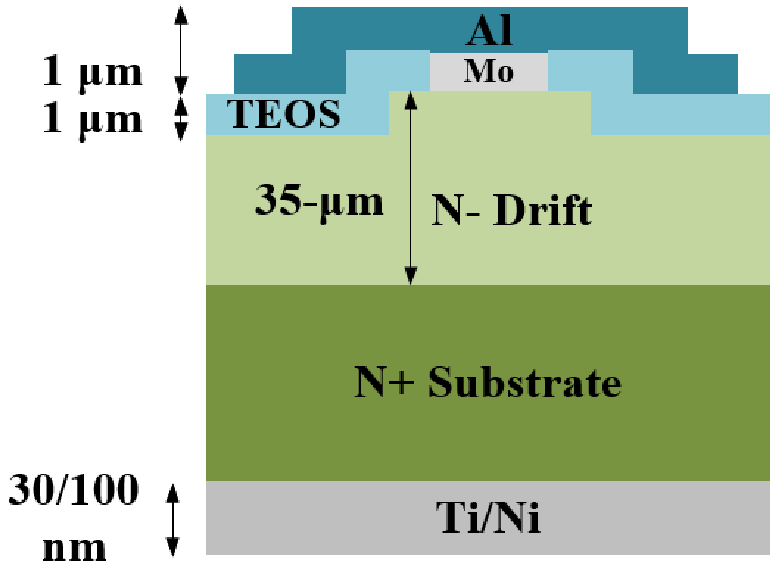
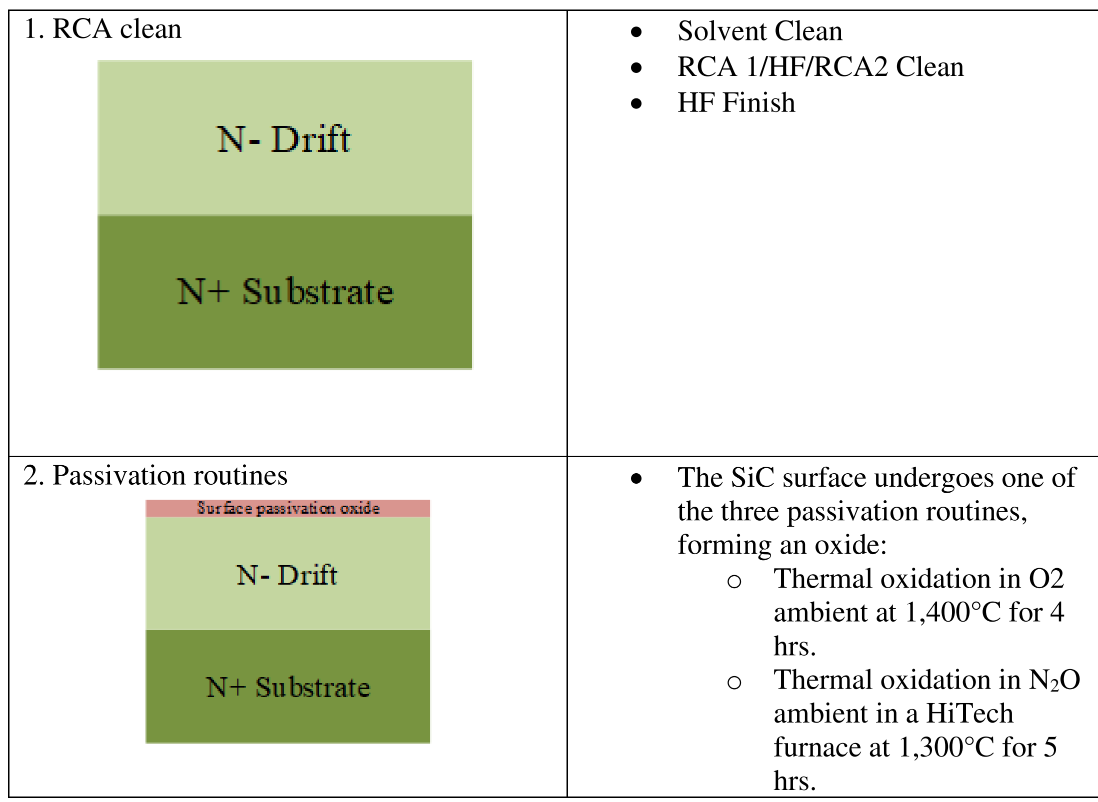


Figure 3.1 Cross-sectional view of the fabricated Schottky barrier diodes with Mo as the Schottky contact metal. The Schottky contact area is 4.39×10^{-4} cm^2.

Several chips have been fabricated across a number of different wafers from the batch. The results presented here were repeatable across the die from the same and different wafers.

Table 3.1: Process flow for the fabrication of the Schottky barrier diodes.



1. RCA clean N- Drift N+ Substrate	• Solvent Clean • RCA 1/HF/RCA2 Clean • HF Finish
2. Passivation routines Surface passivation oxide N- Drift N+ Substrate	• The SiC surface undergoes one of the three passivation routines, forming an oxide: ○ Thermal oxidation in O2 ambient at 1,400°C for 4 hrs. ○ Thermal oxidation in N_2O ambient in a HiTech furnace at 1,300°C for 5 hrs.

	○ P_2O_5 passivation using a silicon diphosphate 4" wafer at 1,000°C for 2 hrs.
3. Oxide removal/ subsequent field oxide layer formation and Schottky contact deposition Mo N- Drift N+ Substrate Ti/Ni	• Previously grown/deposited layers are removed in HF. • Field oxide layer is deposited to protect the surface. • Deposition of a backside Ti/Ni contact and ohmic contact anneal at 1,000°C for 2 minutes in Ar ambient (5 slm). • Photolithography is carried out to open up a window in the oxide • Removal of SiO2 in the process window using a CHF3:Ar dry etching recipe. • Deposition of 100nm Mo using an e-beam evaporation system. • Schottky contact anneal at 500°C.
4. Power metal deposition (final device structure in Figure 3.1)	• Photolithography • Deposition of a 1-2 μm thick Al power metal on top to form a field plate.

3.3 CURRENT-VOLTAGE (I-V)

The rectifying characteristics of all the diodes were characterized via I-V measurements at room temperature using a Keysight B1505A parameter analyser and a semiprobe semiautomatic probe station. On-state parameters were then extracted from the on-state characteristics, assuming that thermionic emission [4, 25] was the governing conduction mechanism at the Schottky interface. The ideality factor (η) and SBH were measured between leakage current densities of 1×10^{7} and 1×10^{3} A cm^{2}.

The saturation current density J_S from Equation 2.5 can then be extracted graphically, as described in Section 2.8.1. This is done by determining the intersection of the linear region of the logarithmic current density over voltage (logI – V) plot to the y-axis (V=0). The barrier height $\Phi_{B,n}$ can then be extracted from this equation, given that all other variables

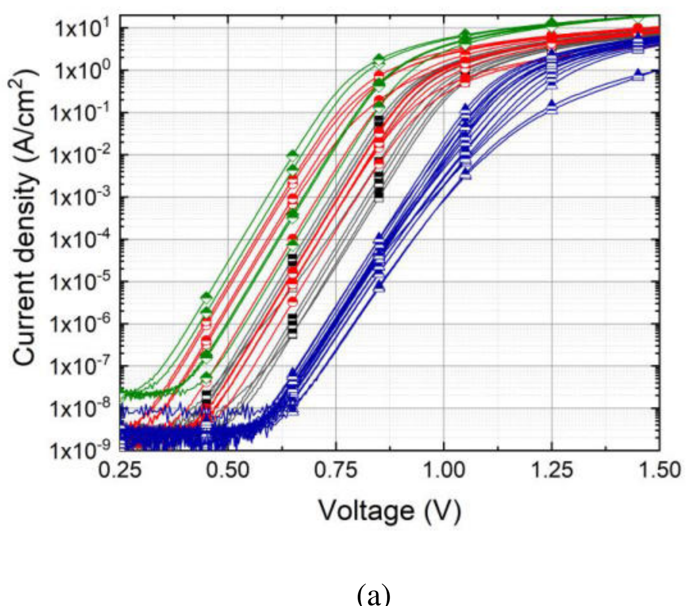
are material constants. In a second step, the ideality factor can then be extracted by rearranging equation 2.8, to

$$\ln(J) = \frac{qV}{\eta kT} + \ln(J_S) \qquad (3.2)$$

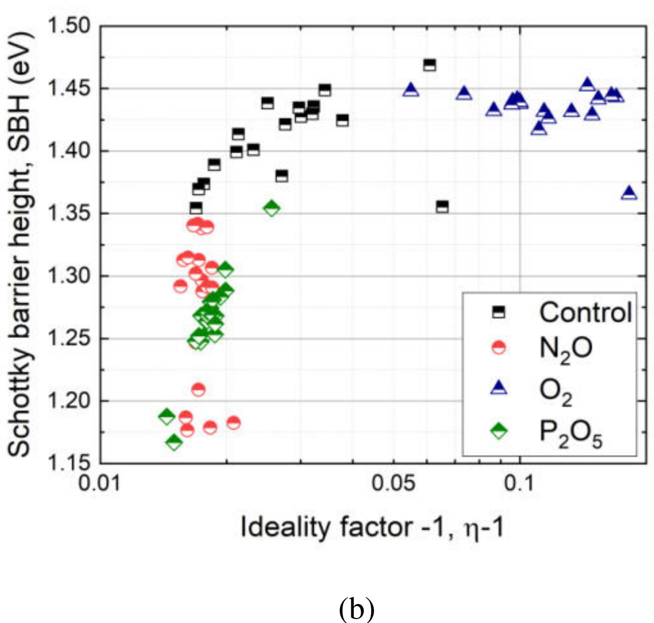
The ideality factor can then be easily rearranged, given that the other parameters are constants. The exact extraction of the data can be seen in the MATLAB code provided in Appendix A.

A typical set of on-state characteristics (at room temperature) for the Mo/SiC diodes are shown in Fig. 3.2(a), as well as their barrier heights and ideality factors (plotted as η-1) in Fig. 3.2(b) for at least 15 different SBDs of each type. All the diodes had very low values of η, confirming that thermionic emission is the dominant current transport mechanism.6 Without any surface treatment, the control samples had a relatively wide spread of SBH and η, which averaged at 1.41 eV and 1.03, respectively (Fig. 3.2). A summary of the extracted electrical parameters is shown in Table I.

From this baseline, the O_2 surface treatment appears to have worsened the electrical characteristics, resulting in a higher average SBH of 1.43 eV and η of 1.09, while there remains a wide spread of the results. On the contrary, the SBH was significantly lowered by applying the N_2O and



(a)



(b)

Figure 3.2 Typical on-state I-V characteristics (a) of the Schottky diodes, measured at 22 °C. SBH and ideality factors (b) for these diodes at room temperature as well.

P_2O_5 treatments, with average values of 1.28 eV and 1.27 eV, respectively. These diodes also had extremely low η, all below 1.02, and a tight, repeatable distribution.

Table 3.2: Summary of measured ideality factors, barrier heights, and reverse leakage currents of the as-grown and treated samples. All measurements were carried out at room temperature. Mean values are provided with standard deviations.

Sample	Schottky barrier height (eV)	Ideality factor	Reverse leakage current at -500 V ($A.cm^2$)
Control	1.38 ± 0.08	1.05 ± 0.09	1.47×10^{-2} $\pm 3.01 \times 10^{-2}$
O_2 treated	1.43 ± 0.04	1.09 ± 0.04	2.34×10^{-3} $\pm 3.56 \times 10^{-3}$
N_2O treated	1.28 ± 0.06	1.02 ± 0.01	4.07×10^{-3} $\pm 9.28 \times 10^{-3}$
P_2O_5 treated	1.27 ± 0.03	1.02 ± 0.01	2.12×10^{-5} $\pm 6.13 \times 10^{-5}$

Figure 3.3 shows the ideality factor and the SBH taken from 80 to 320 K, for a typical control diode and P_2O_5-treated diode. Both diodes follow typical trends, explained elsewhere [4, 5, 25] with η increasing and SBH decreasing at low temperatures. There is little difference in the ideality factor, which remains below 1.1 until 175 K for both diodes. However, it can be seen that the room temperature offset in the SBH of 0.10–0.13 eV is maintained across the temperature range.

The most significant outcome of this study is shown in Fig. 3.4, which summarizes the leakage current density (at V_R = 500 V) of at least 60

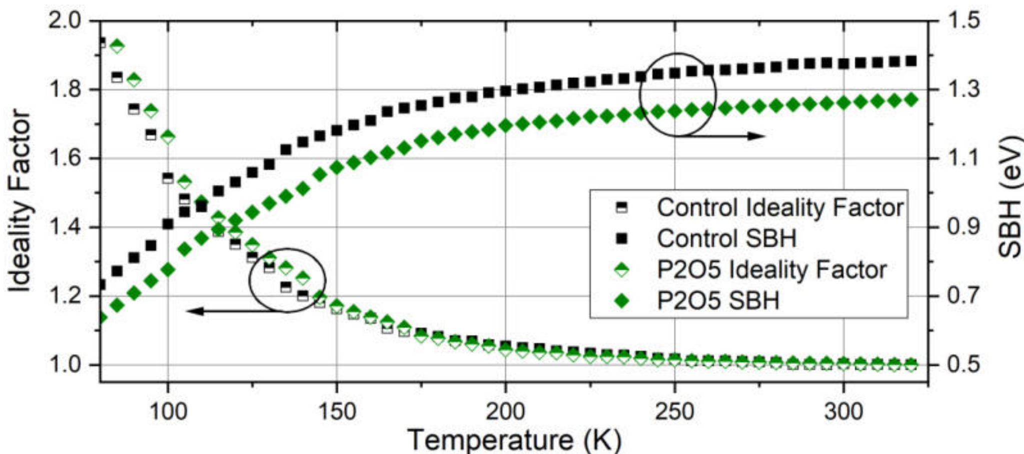


Figure 3.3 SBH and ideality factors for a typical control and P2O5-treated diode from 80 to 320 K.

diodes per treatment. Despite the reduction in SBH demonstrated in Fig.3.2 and Table 3.I for the P_2O_5-treated diodes, these can be seen to give the lowest leakage current levels, with a median value of $1{:}5 \times 10^6$ A cm^2, three orders of magnitude lower than the control diodes. This is contrary to the expectation that the reduced SBH (and hence a lower turn-on voltage) will result in an increased leakage, as happened when Infineon moved from Ti to Mo [11, 26].

In Bonyadi *et al.*[13], these Mo/SiC diodes were compared to Ni and Ti SiC diodes that underwent the same pre-treatments. These results showed that a P_2O_5-treated Mo/SiC diode had a SBH equivalent to Ti, but a leakage current lower than any Ni diode, thus combining the benefits of both low- and high-SBH metals. Furthermore, the Mo diodes were the only diodes to undergo any significant leakage current reduction after any

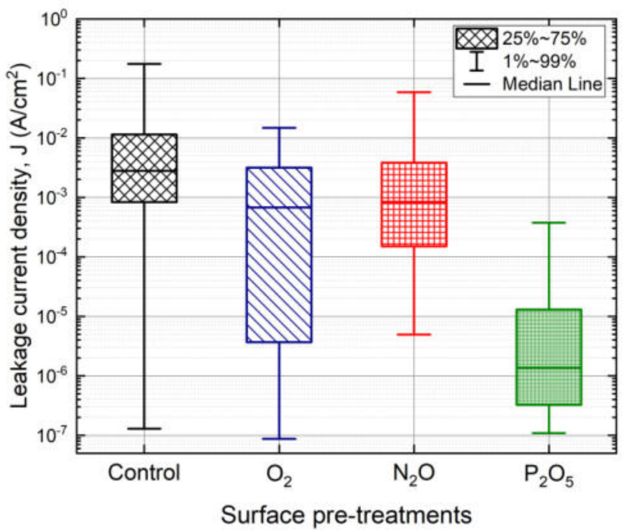


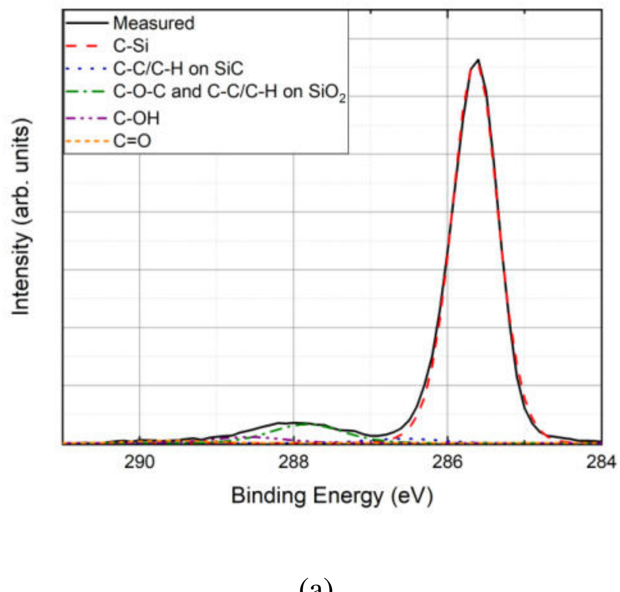
Figure 3.4: Diode leakage current characteristics at VR = 500 V, measured at 22°C. Median values are represented due to the logarithmic scale.

of the pre-treatments. To investigate the mechanisms by which the P_2O_5 treatment improves the diode characteristics, a series of physical analyses were carried out.

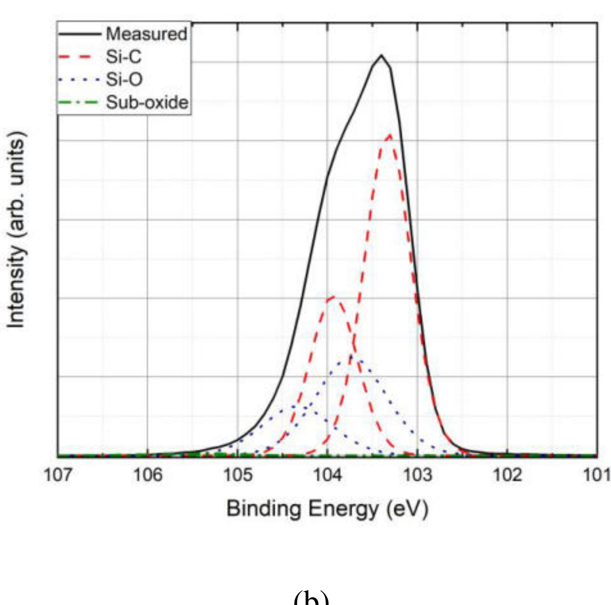
3.4 XPS AND SIMS STUDY

X-ray photoelectron spectroscopy (XPS) characterization was performed in order to investigate the physical and chemical properties of the SiC surface after removal of the previously grown or deposited oxides. Samples were prepared using the oxide growth and deposition procedures described above, with the oxides being removed in HF (10%) solution afterwards. The samples were then immediately loaded into a Kratos Axis Ultra DLD XPS system. The samples were illuminated with al Kα X-rays (1486.6 eV), the spectrometer work function was calibrated using polycrystalline Ag foil prior to the experiments, and the spectra were analysed at take-off angles (ToA) of 90 and 15, giving 3λ depths of 10 nm and, 3nm, respectively. High-resolution core spectra were taken for Si 2p,

C 1s, O 1s, P 2p, and N 1s, and the data were analysed using the CasaXPS software package, employing Shirley backgrounds and Voigt (Gaussian-Lorentzian) line shapes. The Si 2p and C 1s of the untreated sample spectra are shown in Figs. 3.5(a) and 3.5(b). All spectra are shown for a 90 ToA.



(a)



(b)

Figure 3.5: XPS data and fits for the (a) C 1s region, (b) Si 2p region without surface treatment.

Due to the presence of adventitious carbon in XPS, carbon clusters cannot be quantified directly from the XPS spectra. In order to analyze the effect of surface treatments on carbon clusters, the Si:C stoichiometry of the surface is extracted using the relative atomic concentration of SiC components in the C 1s and Si 2p spectra. An overview of the obtained Si:C ratios can be seen in Fig. 3.6.

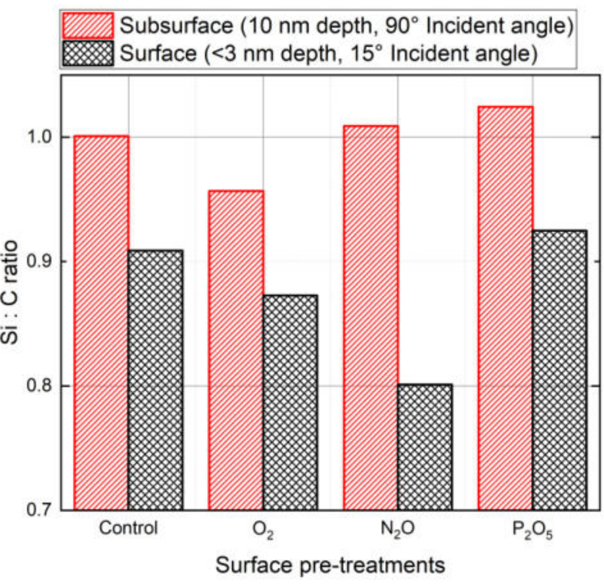


Figure 3.6: Si:C ratio of the investigated samples at different surface depth.

For the 90 ToA, the results were close to stoichiometric. The control sample showed stoichiometry closest to 1.0 and, consistent with the carbon cluster model, the O_2 treatment gave a 4.3% carbon-rich surface and the N_2O treatment restored stoichiometry. The P_2O_5 treatment gave a 2.4% silicon enrichment, showing clear evidence of a surface modification and indicating that silicon, or possibly SiO_2, may have a role in improved diode performance. For the 15°ToA, the O_2 and N_2O treatments gave carbon enrichments of 13% and 20%, while P_2O_5 gave the lowest carbon enrichment of 7.5%. The 15°ToA quantification was more significantly affected by adventitious carbon, which may have

influenced the analysis, but it is also more sensitive to the surface composition, suggesting that the surface may be more carbon-rich than the 10 nm below it. For both measurements, the P_2O_5 treatment has shown to combat carbon enrichment.

The P 2p spectrum of the P_2O_5-treated sample is shown in Fig. 3.7 and confirms the presence of phosphorus pentoxide following the P_2O_5 treatment [27-29]. This shows that traces of P_2O_5 can be found near the

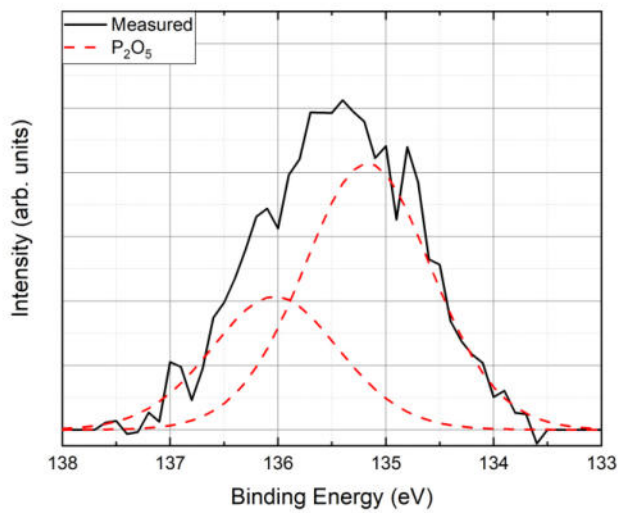


Figure 3.7: P 2p region showing a P_2O_5 peak for the P_2O_5-treated sample.

surface even after the removal of the oxide via HF. This peak was not observed for any of the other samples. Secondary ion mass spectrometry (SIMS) was used to further confirm the presence of phosphorus after the P_2O_5 treatment and metallization and to investigate its depth distribution. One sample was prepared using the P_2O_5 treatment and Mo deposition, as described above. SIMS was carried out using Si, C, and P+ matrix markers at a high resolution (1 nm) near the Mo/SiC interface (100–200 nm).

Figure 3.8 shows the SIMS spectra. Phosphorus concentrations of up to 1.5×10^{19} cm^{-3} could be detected at the Mo/ SiC interface.

This surface chemistry study has shown, using XPS, that a

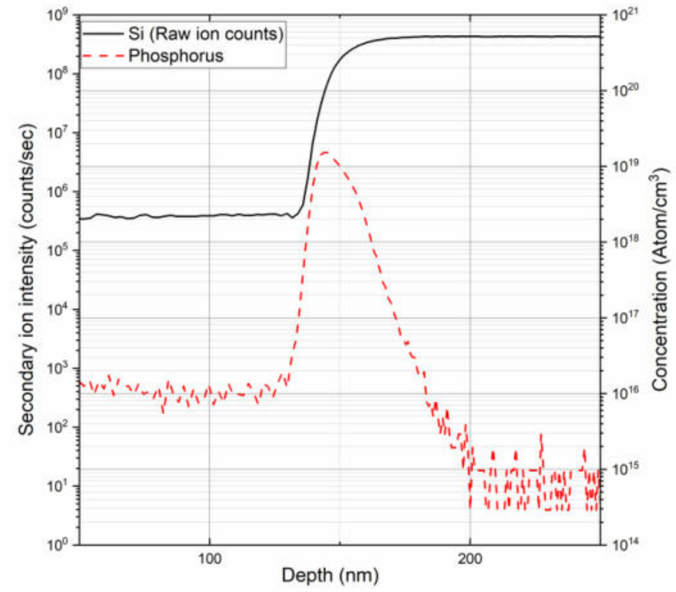


Figure 3.8: SIMS results for the P_2O_5-treated sample.

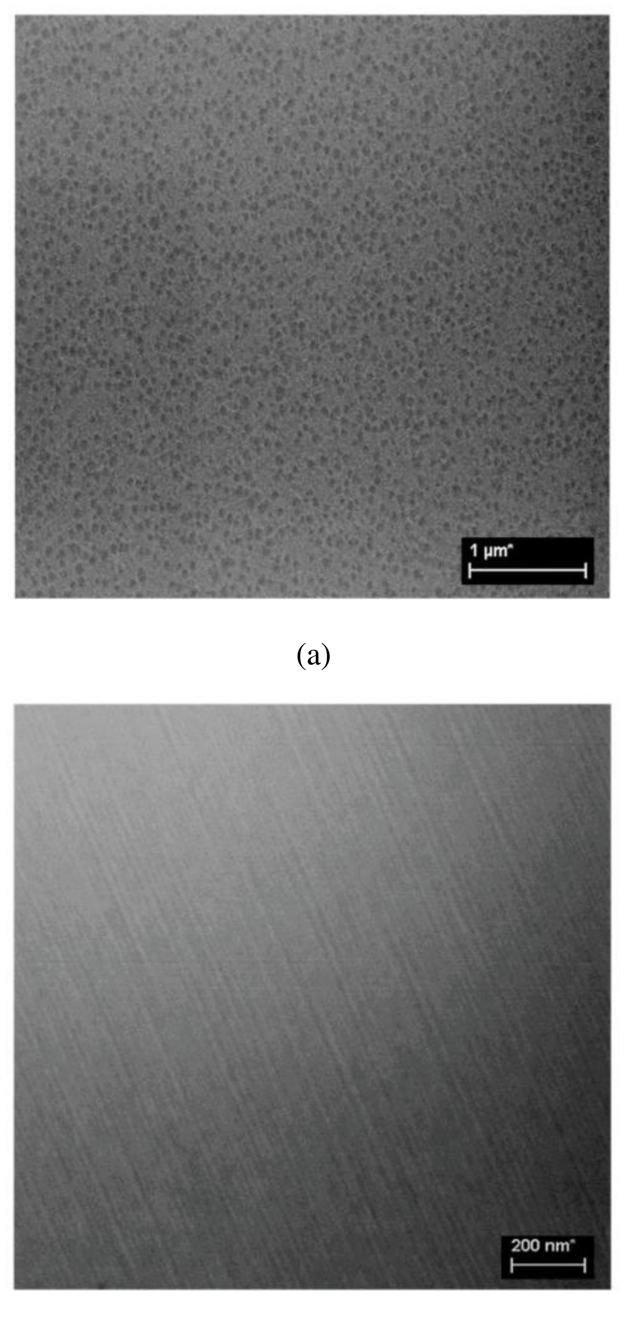
phosphorous deposition (P_2O_5) process in N_2 ambient does not lead to carbon enrichment at the interface, unlike the O_2 treatment and the N_2O treatment at a shallow probing depth. Furthermore, both XPS and SIMS results show that phosphorous remains are found after HF etching and post-metallisation.

3.5 SURFACE MORPHOLOGY STUDY USING AFM AND SEM

AFM and SEM images were taken for a P_2O_5-treated sample and an untreated control sample. A Bruker Icon AFM was used in a peakforce tapping mode. The probe tip was made of Si on a nitride lever. The scan area of the presented images is 5×5 μm^2. Four scans were taken for both samples across different positions on the chip with little difference between the regions. For the SEM investigation, the same samples were investigated in a Zeiss SUPRA 55-VP FEGSEM at an accelerating voltage of 15 kV. Two scans were taken for both samples, with representative images shown in Fig. 3.9.

As a result of the AFM images, RMS roughness values below 1 nm were measured for both samples, with average values of 351 pm for the control sample and 711 pm for the P_2O_5-treated sample. The P_2O_5-treated sample shows clear circular features with a density of approximately 5×10^9 cm^2, as shown in Fig. 3.10(a). Their size and shape vary across the sample, with widths between 70 and 200nm and depths ranging from 1 to 3 nm, although the measurable depth was limited by the AFM tip.

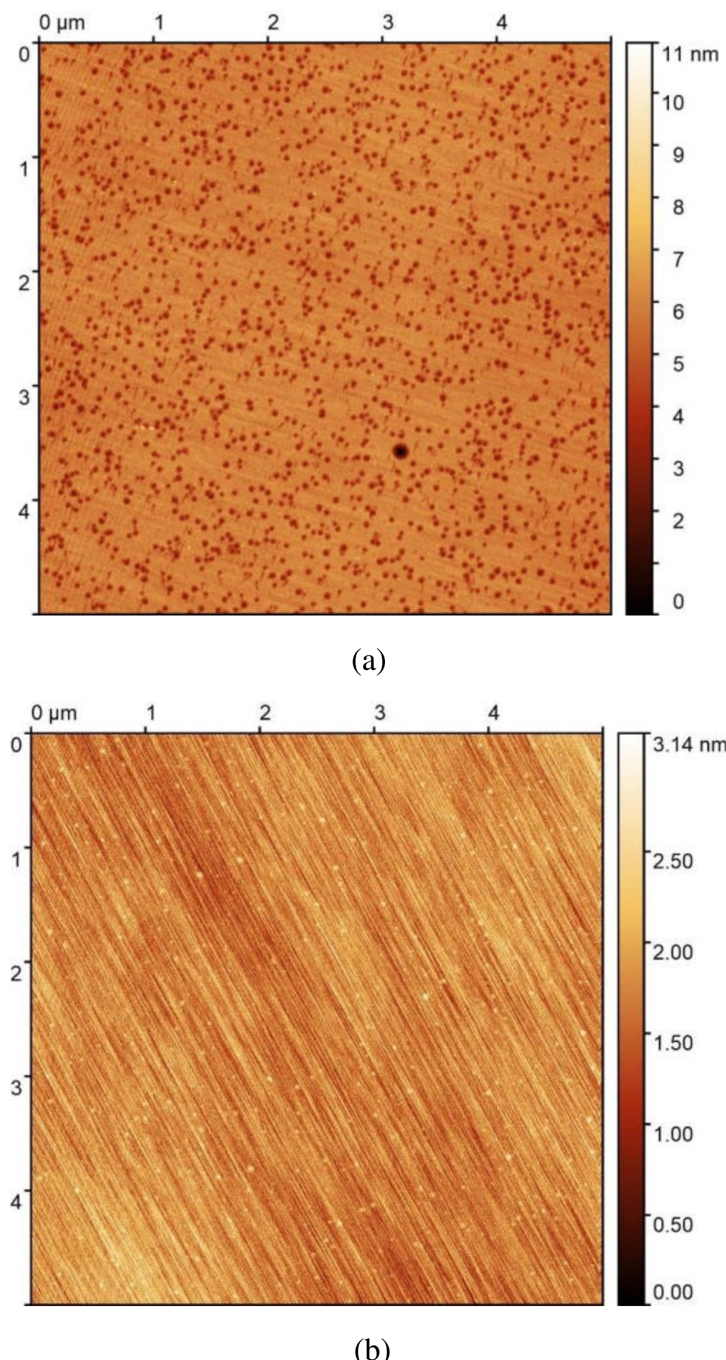
In the untreated sample, normal SiC surface steps are clearly visible, while the circular surface features of visible post-P_2O_5 treatment are also faintly visible, though not as deep pits, but rather very small peaks. The same surface features were not seen in the post-N_2O/O_2 treatment. The SEM showed the extent of these defects over a wider area. Figure 3.9 shows the P_2O_5-treated and control surfaces at 1 um and 200 nm fields of view, respectively.



(b)

Figure 3.9: SEM images of (a) a P_2O_5-treated sample and (b) an untreated control sample with a 1 µm and 200 nm scan size, respectively.

With the AFM micrographs, the difference between the control and P_2O_5-treated surfaces is visible. The P_2O_5-treated surface shows the same feature sizes and shapes as the AFM micrographs, with similar densities of 5.5 × 109 cm-2 and a slightly rougher surface. The surface morphology



(a)

(b)

Figure 3.10: AFM images of (a) a P_2O_5-treated sample and (b) an untreated control surface with a 5×5 µm^2 scan size.

study has shown that the P_2O_5 treatment has induced a high intensity of surface features, not seen in the control sample.

3.6 CROSS-SECTIONAL ANALYSIS USING TEM

Cross-sectional TEM specimens of the control and P_2O_5-treated Mo/SiC SBDs were prepared using a focused ion beam. The interface of these devices was observed in either a JEOL 2100 TEM or a JEOL ARM 2000F TEM. Energy-dispersive x-ray analysis (EDX) was performed in the JEOL ARM200F equipped with a 100 mm^2 Oxford Instruments windowless EDX detector. In places along the P_2O_5-treated interface, such as that shown in Fig. 3.11(a), features can be seen which propagate approximately 10 nm into the SiC. These are distributed nonuniformly across the observed interface, with region widths varying from 80 to 120 nm.

Initial EDX mapping results confirm that these are amorphous features with an increased oxygen concentration, which are most likely formed due to the deposition of oxygen and phosphorus during the P_2O_5 treatment, since no such features and oxygen concentrations were found in the untreated SiC sample. The oxide in these pits, therefore, remains after the HF dip that removed the P_2O_5 layer.

In contrary, the untreated control sample shows a uniform interface, with an interfacial region less than 2 nm thick.

3.7 DEFECT CHARACTERISATION USING SYNCHROTRON XRT

(a)

(b)

Figure 3.11: HRTEM images of the Mo/SiC interface of (a) the P_2O_5-treated and (b) the untreated control SBD and (c) EDX linescan through a Schottky diode sample that had undergone a more dilute HF dip (1ml HF:100ml H_2O) to further investigate the observed decorations .

To investigate a potential connection between the high density (5×10^9 cm^2) of surface defects and typical SiC defects—basal plane dislocations

(BPDs), threading edge dislocations (TEDs), and threading screw dislocations (TSDs)—in the underlying epitaxial layer and substrate, synchrotron x-ray topographs were taken from untreated and treated (all three surface treatments) samples that had previously undergone SEM and AFM analyses. The imaging was carried out at beamline 1-BM at Advanced Photon Source, Argonne National Laboratory, USA. To image all dislocations in the substrate and epitaxial layers, 11-2 0 reflections were recorded. For stacking fault detection, 10-10 and 10-11 reflections were recorded. Grazing incidence angle scans (resulting in a penetration depth of 35 μm) were also performed along the 11-28 plane to detect threading dislocations and BPDs in the epitaxial layer. A grazing scan of the untreated control sample revealed that no BPDs were observed except around a 3C inclusion, which indicates that they are all converted to TEDs during the epigrowth. No deflected dislocations were observed for the control sample. For the P_2O_5-treated sample, some BPDs were seen and this sample showed the highest density of TEDs measured across all samples. No stacking faults could be observed for any of the analysed samples. An overview of the measured defect densities of all investigated samples can be seen in Table 3.II. There is some significant difference between the values extracted, but it is expected that most of these differences come from the varying locations of the chips from across the wafer. All these bulk defect densities are on average 5 orders of magnitude lower than the measured surface feature density of 5×10^9 cm^2. This suggests that the observed features on AFM and SEM micrographs are not related to defects that originate in the bulk or epitaxy.

3.8 DISCUSSION

The electrical measurements of the P_2O_5-treated diodes revealed a reduction in the off-state leakage of the Mo/SiC SBDs of 2–3 orders of magnitude, compared to those that had not been treated. Furthermore, these devices had a SBH 0.11 eV lower than the untreated control samples, which appears to defy the logical leakage current vs turn-on voltage trade-off dictated by the Schottky barrier height. It is worth noting that the leakage of these Mo diodes is also lower than identical Ni/SiC diodes produced previously [13], despite a barrier height of .0.3 eV being lower. At the same time, both the ideality factor of the devices and the uniformity of the results were improved by the P_2O_5 treatment, suggesting an overall improvement in the homogeneity of the metal-semiconductor interface. AFM images, shown in Fig. 3.10, and TEM images, shown in

Table 3.3: Summary of measured defect densities of the as-grown and treated samples.

Sample	BPD (cm^{-3})	TED (cm^{-3})	TSD (cm^{-3})
Control	814	2378	1202
O_2 treated	3085	460	690
N_2O treated	1618	1790	1355
P_2O_5 treated	3045	12122	383

Fig. 3.11, revealed that the P_2O_5 treatment has a physical impact on the SiC surface, creating “nanopits” that are 3–10 nm deep and wide. Despite the wafer having undergone a HF dip to remove the oxide left on the

surface after the pre-treatments, SIMS analysis suggests that a significant quantity remained within the surface pits. Despite evidence of phosphorous at the surface from SIMS, it was not possible to identify phosphorous in the nanopits within the detection limit of EDX in the diodes, but when reducing the HF concentration in the post-deposition wet etch of separately fabricated diodes such as in Fig.3.11 (c), these could be detected, suggesting a means of controlling the content of both phosphorous and oxygen at the interface by varying the concentrations of the etchants.

The oxide-filled nanopits are believed to have the biggest impact on the electrical characteristics of the device. From synchrotron x-ray topography analysis, it is evident that their high density (5×10^9 cm^2) does not correlate with any identifiable bulk or epitaxial defects, which means that the nanopits observed here are different from other nanopits [30] that have been shown to be the source of a high leakage forming at the surface of threading dislocations. Regardless of their origin, the termination of the surface features, which are barely visible on the AFM scan of the control sample, has the effect of homogenizing the interface, given that current is prevented from passing through these areas. Any source of inhomogeneity at a Schottky interface causes a degradation of the diode's I-V characteristics, with dirt, defects, and grain boundaries all having been linked to an increase in the distribution of SBH at an interface, leading to a degradation of I-V characteristics [3-5]. The electrical results shown in Table 3.I confirm that the termination of these defective areas results in a set of diodes with minimal spread in SBH between devices.

It is proposed, therefore, that the oxide-terminated nanopits are a source of leakage within the control samples, yet they are terminated in the P_2O_5-treated diodes. The leakage may arise either by (1) being a region of low

SBH or (2) by simply being an imperfection, an area in which the electric field is higher locally than across the rest of the interface. If case 1 were true and areas of low SBH were being terminated, one might expect the average SBH of the P_2O_5-treated diodes, obtained by I-V analysis, to be greater than that of the untreated control samples. Contrary to this, the barrier height of the P_2O_5-treated diodes was, on average, 0.11 eV lower. However, this does not eliminate this possibility. SIMS and XPS analysis both showed that a significant amount of phosphorous ($>1 \times 10^{19}$ cm^{-3}) is present at the interface, left over from the removed P_2O_5 layer. Without any high temperature activation, only a small fraction of these phosphorous atoms will have become active dopants. Indeed, basic calculations relating N_D to the Fermi level position[31] confirm that an increase in active dopants from 1×10^{15} cm^{-3} in the control diodes to 7×10^{16} cm^{-3} in the P_2O_5 diodes would result in the Fermi level being 0.11 eV closer to the conduction band and hence the same reduction in barrier height. Despite the increase in doping, E_{00} calculations[31] confirm that the dominant conduction mechanism at 7×10^{16} cm^{-3} will remain thermionic emission and not thermionic field mission. This theory is supported by the very low ideality factors in the P_2O_5 diodes, which would not be the case if the doping was high enough for thermionic field emission to dominate. Therefore, the increase in subsurface doping, combined with the homogenization of the barrier height after the oxide termination of surface defects, could explain the reduction of the barrier, while simultaneously decreasing leakage.

In the case of the N_2O treatment, the leakage current was not improved, but the SBH and ideality factors were reduced. For the O_2 treatment, no improvement of the electrical characteristics was seen. Both of these treatments are different from the deposited P_2O_5 treatment, in that they

consume the top few nanometers of SiC while forming an oxide. XPS results confirm that, in the case of O_2, the stoichiometry of the SiC subsurface was poor, with carbon enrichment near the interface. However, N_2O restored the stoichiometry at the deep probing depth, but left a carbon-rich surface at a shallow probing depth. This is consistent with the carbon cluster model, where thermal oxidation treatments trap carbon beneath the oxide and, in turn, cause low channel mobility in SiC MOSFETs. In contrast, the P_2O_5 treatment retained a Si-rich interface, principally because the deposited layer does not consume the SiC but fills the previously described nanopits. However, the previously described n-type doping of the interface beneath the contact may have occurred in the N_2O sample, explaining its improved SBH and ideality factor.

Finally, these subtle changes in the contact subsurface can only occur because almost no silicide is formed after a Mo/SiC interface is annealed. This is due to the high melting temperature of Mo and has the result of preserving the monolayers of treated SiC beneath the interface, as seen in the TEM images of Fig. 3.11. This explains why the P_2O_5 treatment has no effect on other metals, such as Ti and Ni, which do form significant silicides at the interface. This leads to the question as to whether this treatment will work on other refractory metals, such as tungsten, niobium, and tantalum. Furthermore, this was a study performed on SiC wafers from one supplier, with 35 μm of epitaxy. Whether the P_2O_5 treatment will have the same beneficial effect on wafers from other suppliers, other epitaxy thicknesses, and at SiC interfaces with other refractory metals is still a work in progress.

3.9 CONCLUSION

A P_2O_5 surface passivation treatment prior to metallisation has demonstrated a significant improvement in the performance of Mo/SiC Schottky barrier diodes. The electrical characterization showed that P_2O_5-treated diodes have a leakage current two orders of magnitude lower than untreated control diodes, a reduction in the Schottky barrier height of 0.11 eV (and hence lower turn-on voltage), and a small improvement in the ideality factor. The P_2O_5 treatment appears to have two effects on the contact subsurface. First, the leakage is likely improved due to the formation of oxide-filled nanopits, witnessed in AFM and TEM scans, which terminate potential leakage paths from imperfections at the SiC surface and homogenise the interface. Second, the barrier is lowered due to a phosphorous-rich region below the contact, which increases the n-type doping and lowers the SBH. Finally, the enhancement of this sub-contact region is only possible because there is no silicide formed at the Mo/SiC interface, which would otherwise consume the top few nanometers of SiC (as in Ti and Ni). These results offer both increased performance of SiC SBDs and present opportunities to improve SBD performance and SiC surface passivation.

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4 3.3 kV SiC JBS diodes employing a P_2O_5 surface passivation treatment to improve electrical characteristics

In this chapter, fully optimised 3.3 kV JBS diodes are produced using the P_2O_5 surface treatment introduced in Chapter 3. Given the prior success of using the pre-treatment with Mo, this process is applied to other refractory metals, tungsten (W) and niobium (Nb) for the first time. The reasons for the enhancement are then investigated via XPS. Finally, the P_2O_5 treated Nb and Mo diodes are then developed into fully optimised JTE-terminated 3.3 kV JBS diodes to see how the P_2O_5 treatment affects leakage currents at high voltage, the device breakdown and the on-state.

The work presented in this Chapter has been published in [1].

4.1 INTRODUCTION

The introduction will also provide a brief of current developments in the selection of Schottky contact metal in commercial packages and research activities that look into modifications of the Schottky interface on 4H-SiC.

The SBH can be controlled by the choice of Schottky metal, leading to a trade-off between low forward voltage drop (V_F) and low reverse current (I_R). Titanium (Ti) has become the industry standard metal on SiC, as it results in a relatively low SBH (1.17 eV [2]), favouring V_F, and hence the on-state losses, over I_R. This is preferred over nickel (Ni), which results in a relatively high SBH (~1.35 eV [3]). Recently, the trend towards lower SBHs has been taken further, with a shift towards molybdenum (Mo) [4], and molybdenum nitride (MoN) [2, 5], the latter further reducing the SBH to 0.86 eV.

Attempts to further modulate the barrier height by varying the annealing temperatures have been undertaken in titanium (Ti) [6], tungsten (W) [7] and tungsten carbide (WC) [8, 9] as well as on Schottky diodes on more heavily doped epitaxial layers [10, 11]. Recently, the use of surface treatments prior to metal deposition has been shown to further influence this key trade-off between using different metals [4]. The use of a novel phosphorous pentoxide (P_2O_5) treatment, applied prior to metallisation, was shown in chapter 3 to highly dope the SiC subsurface to a depth of no more than 50 nm, lowering the SBH by an average of 0.11 eV, but yet it also reduced the I_R by an average of two orders of magnitude. The high-melting point of Mo is key to this, as it prevents the formation of silicides during the Schottky contact anneal, leaving the enhancement of the subsurface in place. For metals with lower melting points, such as Ti and Ni, which form silicides, the P_2O_5 enhancement has no effect.

4.2 DEVICE FABRICATION AND EXPERIMENTAL PROCEDURE

Two types of diodes were fabricated, shown in Fig. 4.1. Simple, small area (4.39×10^{-2} mm^2) mesa isolated Schottky diodes, without termination, were first produced to test the effects of the P_2O_5 treatment across various metal contacts. Then, fully optimised JBS diodes (active areas 1.56 mm^2 and 42.25 mm^2) were then produced such that the P_2O_5 treatment could be trialled on an industry standard process to high current and high reverse voltage. A novel hybrid termination design is shown in Fig.2 and was optimised for the 3.3 kV JBS diodes. This comprised of P+ floating rings comprising (75 μm total width, 200 nm depth, 3×10^{19} cm^{-3} box profile doping) and multiple floating JTE rings (75 μm total width, 500 nm depth, 2×10^{17} cm^{-3} box profile doping), both utilising Al+ implants at 500°C. These same two implants were used to form the P

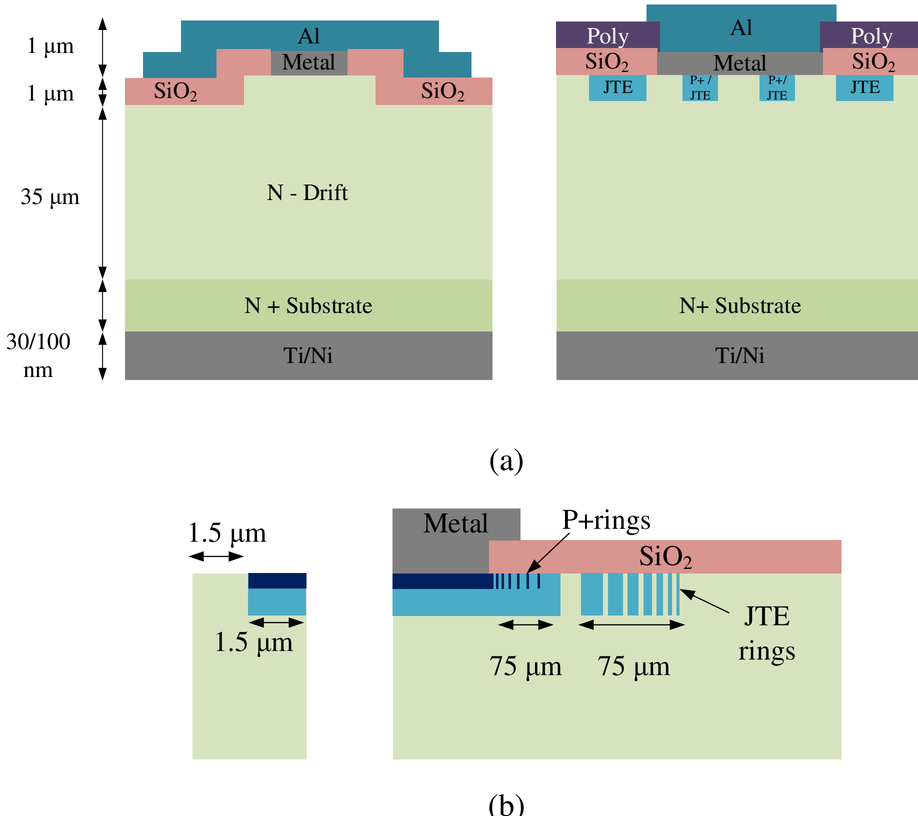


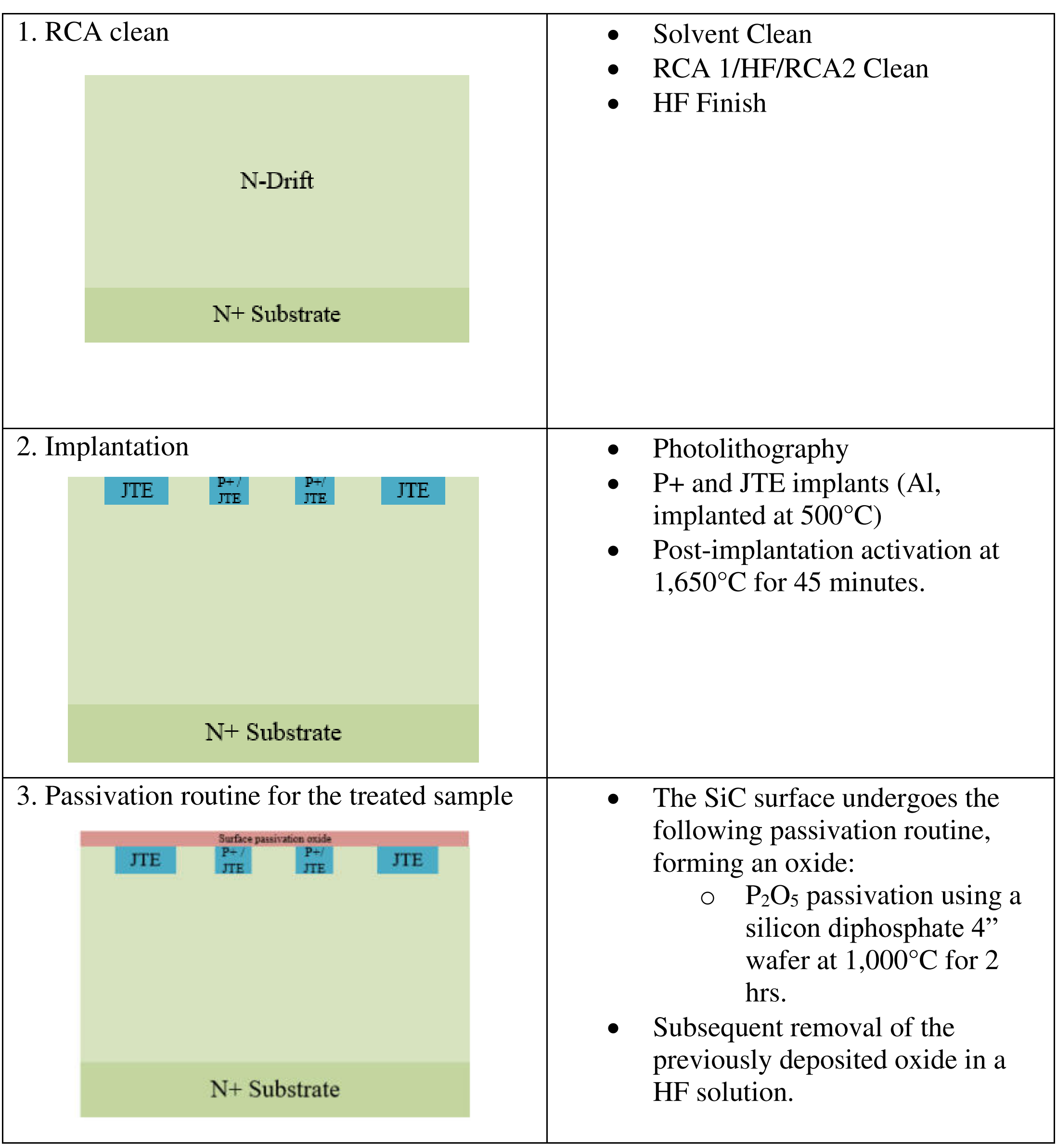
Figure 4.1 (a) left: Cross-section of the fabricated unterminated Schottky diodes and right: Cross-section of the fabricated 3.3 kV JBS diodes.

(b) Detailed JBS designs of left: The half-cell of the active area, using a shallow, highly doped p+ implant on top of the JTE implant; right: The hybrid termination consisting of P+ rings and multiple JTE rings. P+ ring widths are fixed at 3 μm (3, 3, 4, 6, 8, 11 μm gaps). JTE ring widths are 14, 11, 7, 5, 4 and 3 μm (3, 3, 4, 5, 7 and 9 μm gaps).

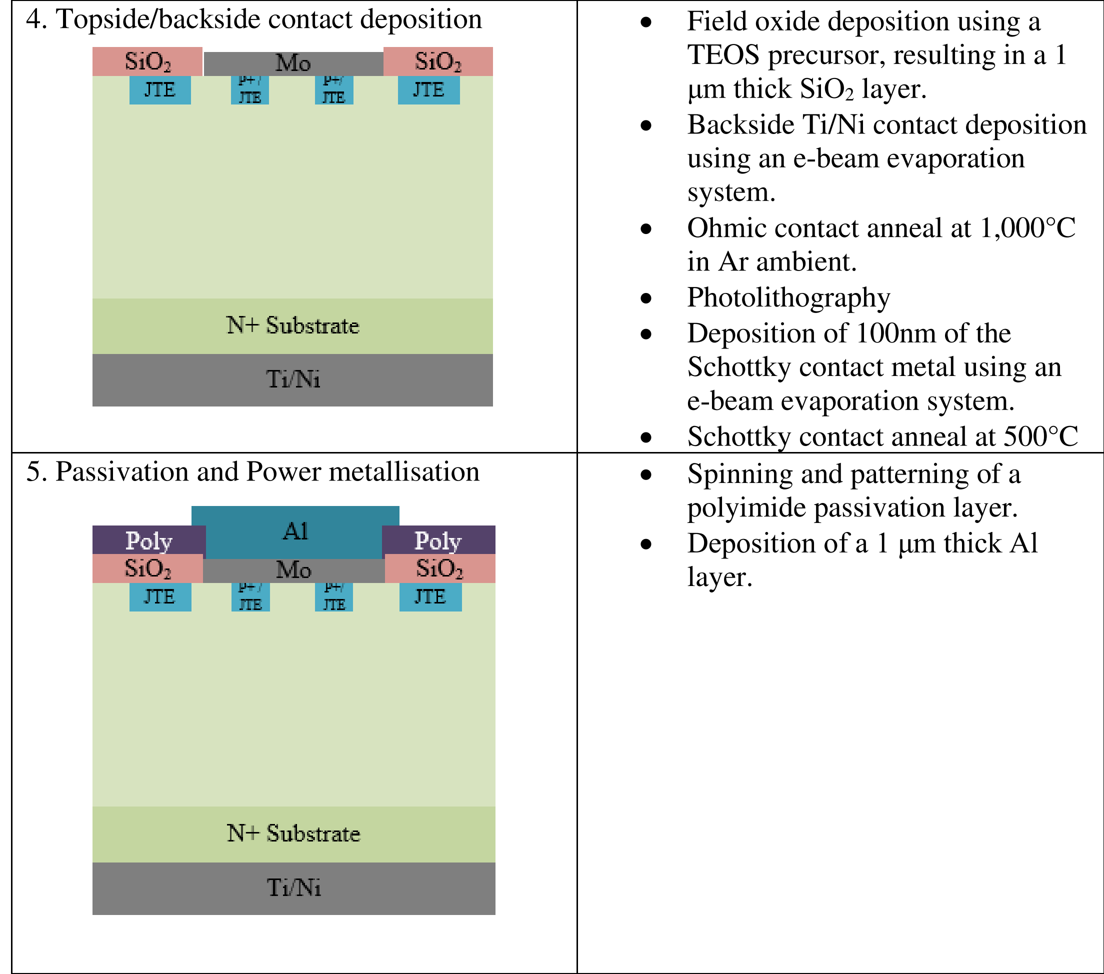
region in the active area, shown in Fig.4.1b (left), to shift the electric field away from the substrate. Both devices were fabricated on a 4×10^{15} cm^{-3} nitrogen-doped, 35 μm thick 4H-SiC drift region, which was grown on highly n- doped substrates. The wafers were laser-cut into 2cm × 2cm chips, before they were cleaned using a standard RCA 1/HF (10%)/ RCA 2/ HF (10%) process. After performing both p-implants in the JBS diodes, they underwent post-implantation activation at 1,650°C for 45 minutes, followed by a sacrificial oxidation step at 1,300°C for 2 hours in nitrous oxide ambient. Both the Schottky and JBS diodes then underwent the P_2O_5 deposition process at 1,000°C for 2 hrs in N_2 ambient, detailed in [4]. The P_2O_5 was then removed in dilute HF (10%) before a 1 μm thick field oxide

(silicon dioxide) was deposited. Ti (30 nm)/Ni (100 nm) ohmic contacts were then formed on the backside of the samples after an RTA at 1,000°C for 2 minutes in Ar (5 slm) ambient. In the next step, 100 nm thick Schottky contact metals (Mo, Nb or W) were deposited, then annealed at 500°C for 2 minutes. Finally, a 1 µm thick Al metal overlay was evaporated on top of the Schottky contact to serve as a field plate, and to aid wire-bonding for switching tests. The process flow for the fabrication of the devices can be shown in Table 4.1.

Table 4.1: Process flow for the fabrication of 3.3 kV 4H-SiC JBS devices.



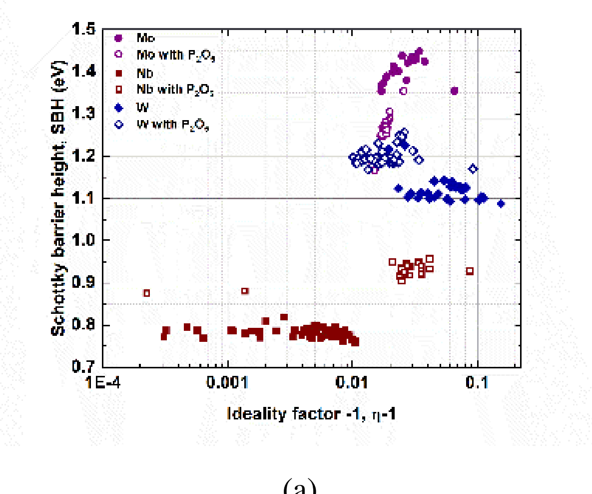
Step	Process details
1. RCA clean N-Drift N+ Substrate	• Solvent Clean • RCA 1/HF/RCA2 Clean • HF Finish
2. Implantation JTE P+/JTE P+/JTE JTE N+ Substrate	• Photolithography • P+ and JTE implants (Al, implanted at 500°C) • Post-implantation activation at 1,650°C for 45 minutes.
3. Passivation routine for the treated sample Surface passivation oxide JTE P+/JTE P+/JTE JTE N+ Substrate	• The SiC surface undergoes the following passivation routine, forming an oxide: ○ P_2O_5 passivation using a silicon diphosphate 4” wafer at 1,000°C for 2 hrs. • Subsequent removal of the previously deposited oxide in a HF solution.



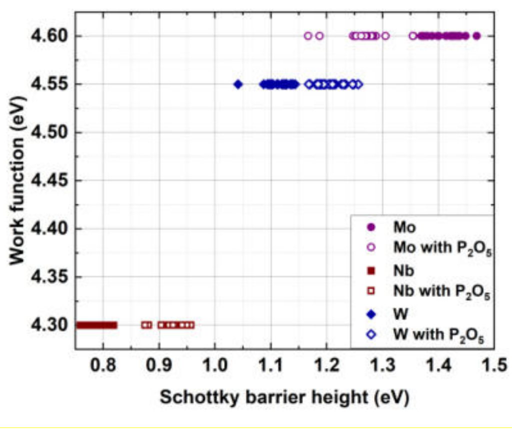
4. Topside/backside contact deposition	• Field oxide deposition using a TEOS precursor, resulting in a 1 µm thick SiO_2 layer. • Backside Ti/Ni contact deposition using an e-beam evaporation system. • Ohmic contact anneal at 1,000°C in Ar ambient. • Photolithography • Deposition of 100nm of the Schottky contact metal using an e-beam evaporation system. • Schottky contact anneal at 500°C
5. Passivation and Power metallisation	• Spinning and patterning of a polyimide passivation layer. • Deposition of a 1 µm thick Al layer.

4.3 SCHOTTKY DIODE ELECTRICAL RESULTS

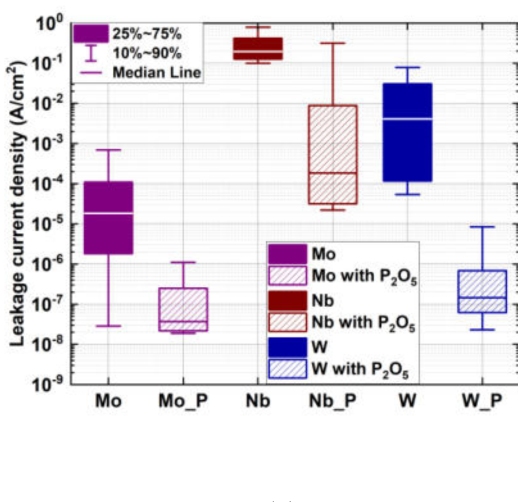
The rectifying characteristics of the unterminated W, Nb and Mo Schottky diodes were auto-probed at room temperature using a Keysight B1505A with a Semiprobe semi-automatic probe station. On-state parameters ideality factor (η) and SBH were extracted for at least 50 devices (Fig. 4.2 (a) and (b)), each under the assumption that thermionic emission (TE) is the governing transport mechanism. The work function values were extracted from [12]. The leakage current density (J_R) up to -200 V was measured for at least 100 of each of the devices, shown in (Fig. 4.2 (b)). Excellent rectifying characteristics appear across the entire dataset with a tight ideality factor distribution, shown in Table 4.1, with all datasets having a standard deviation of less than 0.04 A/cm^2.



(a)



(b)



(c)

Figure 4.2: (a) Ideality factors and work functions (b) over SBHs for the Schottky diodes, measured between 1×10^{-7} and 10 A cm^{-2}. (b) Leakage current densities of more than 100 devices each, measured at -200 V, for a device area of 4.39×10^{-4} cm^2.

The P_2O_5-treatment reduced the SBH of the Mo diodes to 1.26 eV, compared to 1.40 eV for the untreated Mo devices and a reduction in the median J_R of nearly 500×. Untreated Nb Schottky diodes have a very low average barrier height of 0.78 eV, which is increased using the P_2O_5 treatment to 0.93 eV, bringing about a reduction in the median J_R by three orders of magnitude. Similarly, the P_2O_5 treatment resulted in an increase in SBH from 1.12 to 1.20 eV for the W diodes, bringing about a reduction in leakage by over 4 orders of magnitude. Therefore, the P_2O_5 treatment has differing effects on the SBH, with the barrier height increasing for W and Nb, yet going down in Mo. However, it appears that it has a consistent

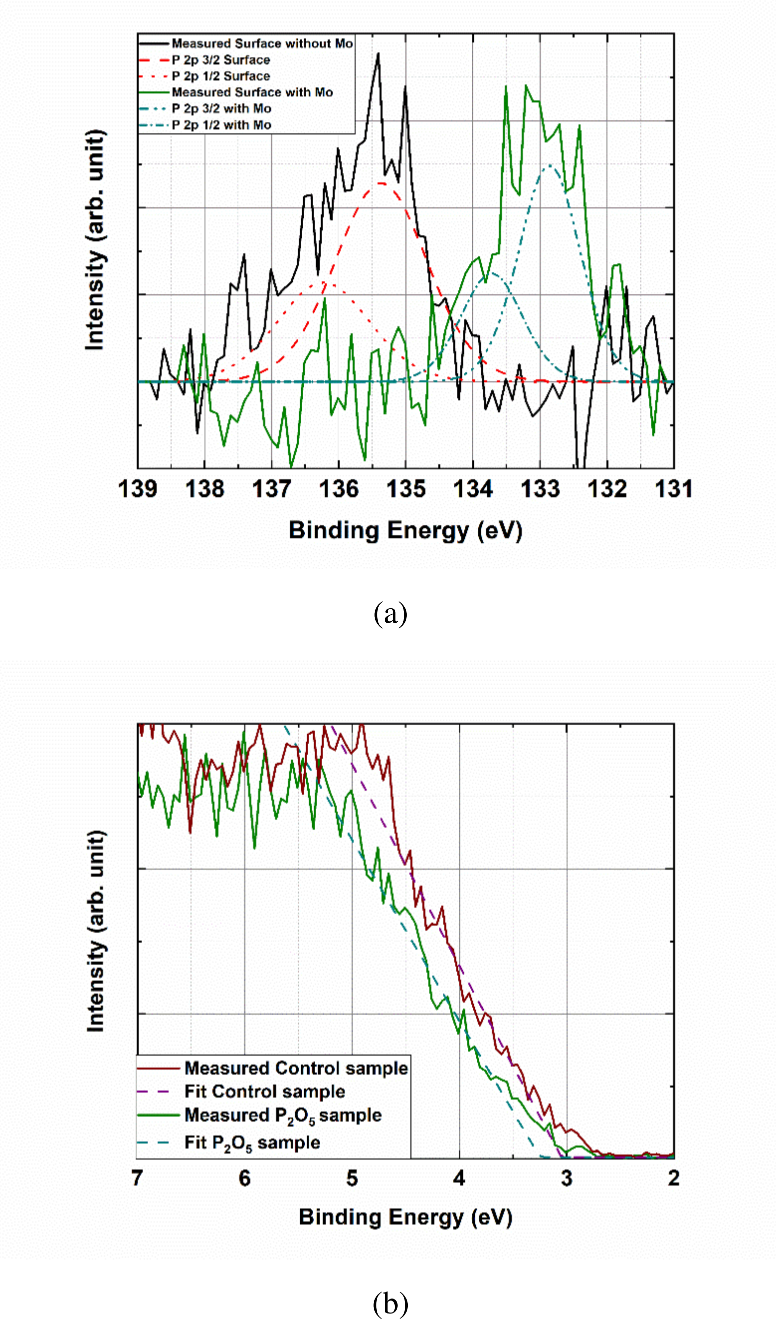
effect in lowering the leakage current. Given the magnitude of the leakage current reduction, and the fact that the Mo SBH actually reduced rather than increased, the reason for the leakage current reduction appear attributable to more than just the SBH. In [4], investigations into the interface showed that potential leakage paths were being filled by the P_2O_5 treatment, and that the SiC subsurface may have been doped by the phosphorous. To investigate further, information on the band structures of the Schottky diodes was sought via x-ray photoelectron spectroscopy (XPS).

4.4 SCHOTTKY DIODE XPS INVESTIGATION

Four samples were prepared for XPS analysis with and without the P_2O_5 treatment, both as a bare pre-metallised surface (2 samples) and fully fabricated Schottky diode with a Mo layer sufficiently thin (3-4 nm) to analyse the interface beneath it (2 samples). Core spectra were taken for Si 2p, C 1s, O 1s, P 2p and the valence band. The P 2p spectrum of Fig. 4.3

Table 4.2: Summary of measured barrier heights (average), ideality factors (average) and leakage current (median) measured at -200 V. Device area for leakage current measurements is 4.38×10^{-4} cm^2.

Contact metal/ treatment	**Schottky barrier height (eV)**	**Ideality factor**	**Reverse leakage current at -200 V (A.cm^2)**
Mo	1.409 ± 0.033	1.036 ± 0.035	1.835×10^{-5}
Mo + P	1.264 ± 0.036	1.013 ± 0.002	3.715×10^{-8}
Nb	0.782 ± 0.012	1.005 ± 0.003	0.195
Nb + P	0.928 ± 0.022	1.030 ± 0.017	1.850×10^{-4}
W	1.126 ± 0.035	1.063 ± 0.036	4.120×10^{-3}
W + P	1.200 ± 0.021	1.020 ± 0.014	1.460×10^{-7}



(a)

(b)

Figure 4.3:(a) P2p region showing a P2O5 peak for the P2O5-treated bare surface and for a Schottky sample with a 3-4nm Mo layer. (b) Valence band extraction for a measured control sample and P_2O_5-treated sample including fits.

(a) shows the chemical state of the phosphorus: The P_2O_5-treated surface received an HF oxide strip and no metal deposition and displays a P 2p 3/2 peak at 135.36 eV, indicating P_2O_5, whereas in the sample with the thin Mo/4H-SiC interface, it occurs at 132.86 eV. The bare P_2O_5-treated surface indicates that the phosphorus does not react with the SiC, but the

shift after Mo metal deposition indicates that a chemical reaction occurs between the P and the Mo. The similarity to previously-reported metal phosphate spectra [13, 14] suggests that a Mo phosphate complex is formed at the interface. However, the valence band spectra, shown in Fig.6, determined a Fermi level of 3.05 eV above the valence band edge for the untreated surface and 3.25 eV for the P_2O_5-treated sample. This extremely high Fermi level indicates that the phosphorus still acts as an n-type dopant at the surface, giving it a degenerately n-doped surface/interface

4.5 3.3 KV JBS DIODES – ELECTRICAL RESULTS

Fully optimised 1.56 mm^2 Nb and Mo JBS were measured up to 3.3 kV to investigate if the P_2O_5-treated diodes remained beneficial when subject to the high current and high electric fields of an industrially relevant power device structure. For benchmarking reasons, the results were compared to a Ni JBS diode of the same design. Firstly, the functionality of the termination design was tested by breakdown measurements of PiN diodes on the individual chips, eliminating the effect of barrier lowering on the leakage performance, hence showing best possible leakage performance. As Fig. 4.4 shows the devices were able to successfully block voltages higher than 3.6 kV without an occurrence of premature breakdown. Leakage currents exceeded a current level of 1×10^{-7} A only at voltages higher than 3 kV, proving the general applicability of the termination design irrespective of the surface treatment or Schottky contact metal.

Having successfully demonstrated the termination design using PiN diodes, the static characteristics of the JBS diodes could now be measured. Exponential on-state characteristics of small (active area of 1.56 mm^2)

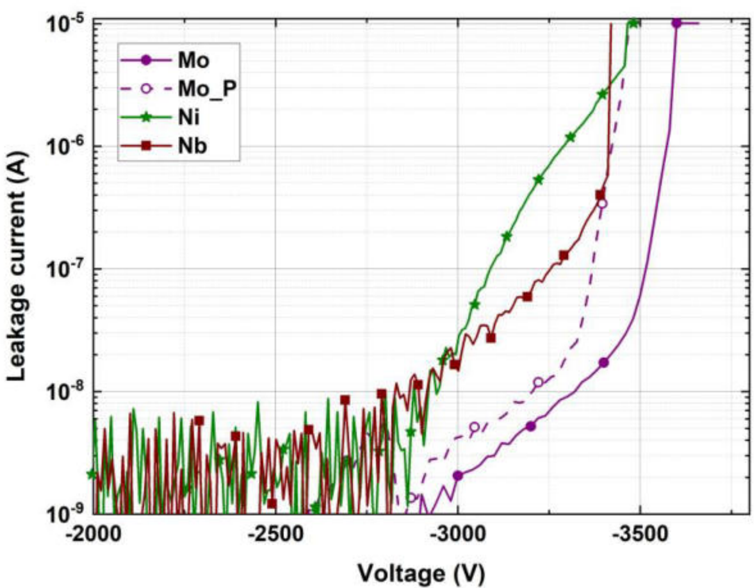


Figure 4.4: Leakage current measurement on PiN diodes (are is 1.56 mm^2) at room temperature, up to 3,700 V.

JBS diodes can be seen in Fig. 4.5, while all the results are summarized in Table 4.2. A reduction of barrier height due to P_2O_5 treatment is evident once more for the Mo devices, those with the treatment having an average SBH of 0.86 eV, 0.3 eV lower than the average untreated diode SBH. The treatment had a more minor effect on the Nb diodes, where the treated devices had an average SBH of 0.84 eV, an increase of 0.03 eV compared to the untreated devices. Fig. 4.5 (right) also shows the static on-characteristics of the large (active area of 42.25 mm^2) JBS diodes up to 5 A. The Nb and Mo diodes were fairly consistent, turning on after 0.5 V. A similar specific on-resistance ($R_{ON,SP}$) could be extracted across the entire dataset from 15 mΩ cm^2 (Mo,Ni) to 17 mΩ cm^2 (Mo + P_2O_5), to 18 mΩ cm^2 for the Nb devices. This is consistent with previously reported Ni 3.3 kV JBS diodes [15], which had a $R_{ON,SP}$ of 12 mΩ cm^2. These results showed that the impact of the P_2O_5 treatment on barrier height lowering/ increase, is consistent with the results in section. The high current results do not suggest a large advantage to using the treatment, but they show no

Table 4.3: Summary of measured barrier heights (average), ideality factors (average) and leakage current (typical)) measured at 1 µA for 1.56 mm^2 JBS diodes. $R_{ON,SP}$ for 42.25 mm^2 JBS diodes.

Contact metal/treatment	SBH (eV)	Ideality factor	V_R at 1 µA (V)	$R_{ON,SP}$ (mΩcm^2)
Mo	1.15 ± 0.03	1.03 ± 0.04	1720	15
Mo + P	0.86 ± 0.05	1.04 ± 0.01	3560	17
Nb	0.81 (typical)	1.07 (typical)	100	18
Nb + P	0.84 ± 0.06	1.02 ± 0.01	900	18
Ni	1.50 ± 0.04	1.04 ± 0.02	3300	15

detriment, which is important given the impact the treatment has on the off-state characteristics.

The off-state characteristics of selected 'average' 1.56 mm^2 JBS diodes are depicted in Fig. 4.6. Once the leakage current has exceeded the noise base of the equipment, barrier lowering can be seen which causes a steady increase in leakage with voltage in all shown devices. A general correlation can be seen between the SBH extracted from the on-state

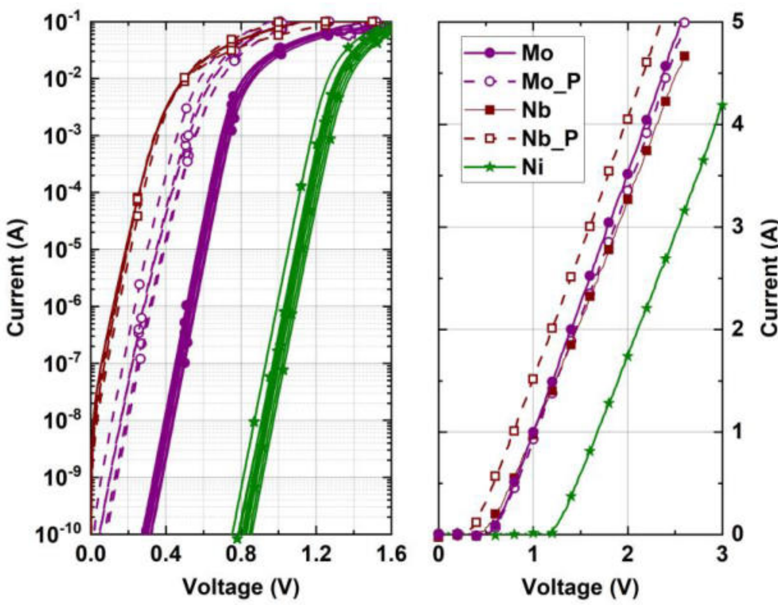


Figure 4.5: left, the exponential turn-on characteristics of the small JBS diodes (active area of 1.56 mm^2). These results were used for the extraction of barrier heights and ideality factors (extracted for current values between 1 × 10^{-7} and 10 A.cm^{-2}) at room temperature. Right, static on-state characteristics of the large JBS diodes (active area of 42.25 mm^2).

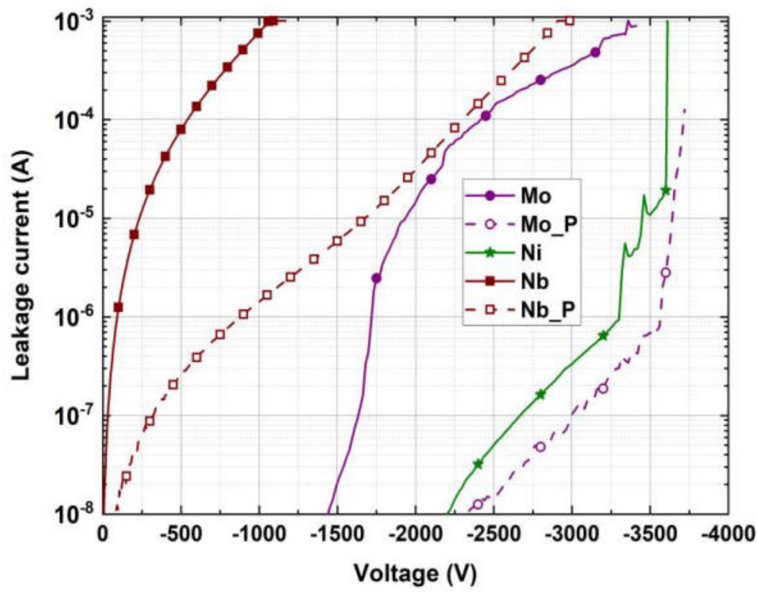


Figure 4.6: Leakage current measurements, up to 3800V. Measurements were carried out at room temperature. The device area is 1.56 mm^2.

characteristics and the breakdown voltage and leakage current profiles: Using a leakage currents of 1 μA as a limit, the Ni devices reach this at 3300 V, the untreated Mo device at 1720 V and the untreated Nb at just 100 V. However, the most significant outcome of these results is the impact of the P_2O_5 treatment, which boosts the Mo voltage to 3560 V, and the Nb to 900 V. These results suggest that the SBH formed by the Nb diodes is likely too small to be a realistic prospect for 3.3 kV diodes. However, the SBH of the Mo+P devices appears to be high enough to support the rated voltage, despite evidence that the Mo phosphate barrier may be lower than the pure Mo. This, we suggest, is due to the effects previously reported [4], that the P_2O_5 treatment terminates potential leakage paths at the SiC surface. This suggests that to utilize Mo as a contact metal in SiC, a P_2O_5 treatment is useful in order to minimize leakage and maximise breakdown voltage, actions that allow the scaling of the technology to large current ratings, without exceeding industry standard off-state leakage targets (typically 1mA at the rated voltage). Both the static on- and off-state results confirm the trends which could be

seen on unterminated device structures in the previous sections, proving the general applicability of the P_2O_5 treatment on optimised and multi-implanted power device structures.

4.6 DOUBLE PULSE SWITCHING TEST

The dynamic switching characteristics of the SiC JBS diodes were tested using a clamped inductive switching circuit ([16-20]). The circuit schematic of the test rig is shown in Fig. 4.7, whilst the final packaging prototype can be seen in Fig. 4.8. Since the leakage performance of the Nb JBS diodes was poor, this was only measured on the Mo (with and without P_2O_5 treatment) and the Ni JBS diodes. In the testing rig, the switching events are dominated by the low side transistor, which are then responded to by the high side JBS diode. The switching rate of the bottom side MOSFET events were varied by altering the gate resistance R_G, hence varying the RC time constant.

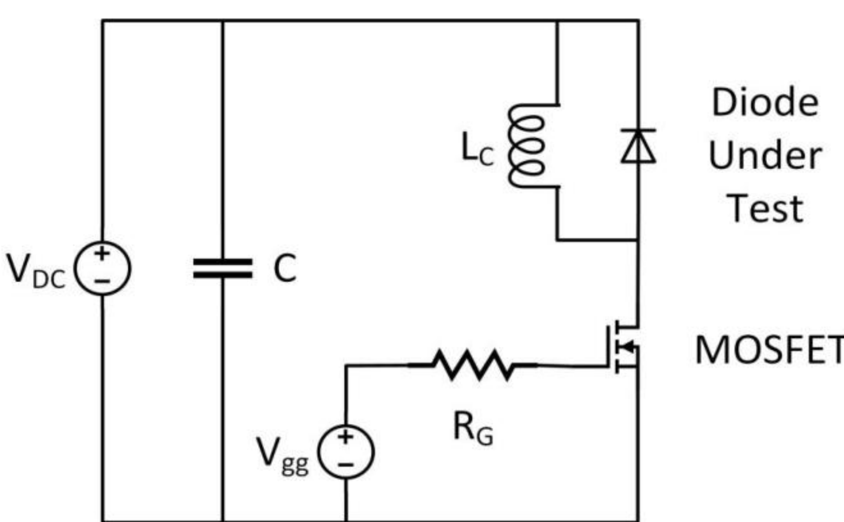


Figure 4.7: Circuit diagram of the clamped inductive switching rig with V_{DC} – DC power supply, R_G – gate resistor, I_G – gate current, L_C – Inductor.

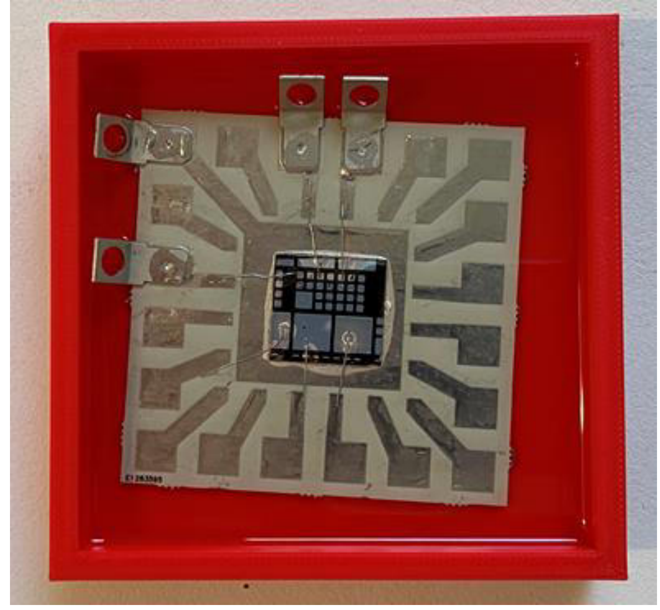


Figure 4.8: Chip prototype package for the double-pulse switching test. The substrate of the bare die was connected to the IMS board using conductive silver paste. The terminals were soldered onto the board after wire bonding. Then, the whole board was covered with silicone gel, after having been placed in a 3D-printed box.

A 1200V/20 A SiC MOSFET was used as a switching device. The commonly used double-pulse switching setup was implemented, in which the first pulse is used to charge the inductor, whilst the second pulse is deployed to record the turn-on and turn-off behaviour of both devices. For the purpose of this investigation, measurements were carried out at room temperature only, using a V_{DC} of 500 V and a gate resistance of 18 Ω. Measurements could not be carried out at rated voltage due to limitations of the electric rig, but are intended to serve as a precursor to verify the general switching characteristics of the design.

The same JBS diodes (active area of 1.56 mm^2) that had undergone static characterisation were used. To enable connection to the testing rig, each chip was placed on an insulated metal (IMS) board, where its 2 µm thick Al anode pad metal was bonded to the outer metal pads on the board, before the terminals were soldered to the board. To avoid arcing, the board was then placed in a 3D-printed package, which was filled with silicone

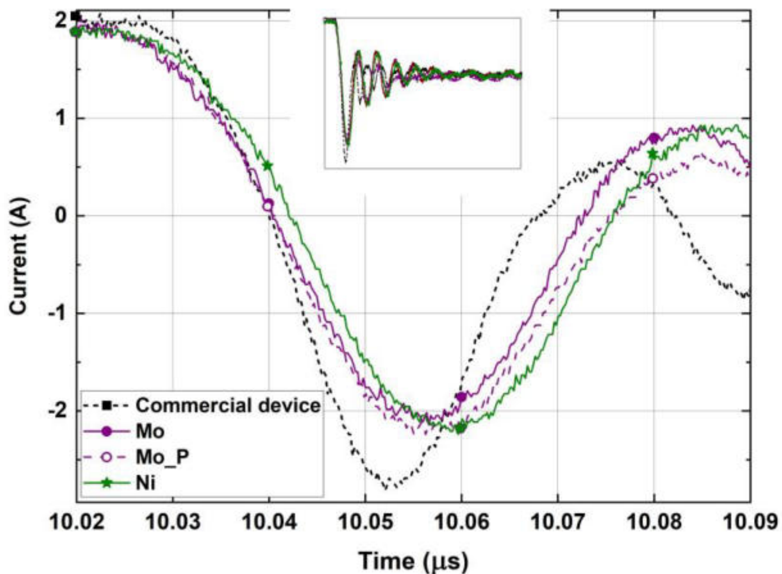


Figure 4.9 : Turn-off characteristic of the measured devices. Measurements were taken at room temperature using a V_{DC} of 500 V and R_G of 18 Ω. In the inset, the entire turn-off waveforms are shown.

gel and left to cure at room temperature overnight. Fig. 4.8 shows the final layout of the devices which were tested in the switching rig.

In Fig. 4.9, the turn-off characteristic of the JBS diodes at rated current (2 A) are shown. For the purposes of benchmarking, this was compared to a commercially available and already packaged 1200 V JBS diode (STPSC10HD12D) with a slightly higher current rating (10 A).

With the configuration, a moderate current fall rate (dI/dt) of approximately 150 A/µs could be achieved for the commercial device, which was about 40 A/µs faster than for any of the measured Mo diodes, with the Ni device showing the slowest response of all measured devices. For the commercial devices, this comes at the expense of a slightly higher reverse recovery current (I_{RR}) of 2.82 A. All the 3.3 kV JBS devices had I_{RR} values of approximately 2.2 A. The higher switching rates of the commercial device (probably due to a difference in package) in combination with the also increased reverse recovery current resulted in

similar extracted charge (Q_R) values of approximately 78 nC for all measured devices.

4.7 CONCLUSION

The application of a phosphorous pentoxide treatment consistently lowered leakage current levels Mo, W, and Nb SBDs, with the W devices showing the most significant reduction of four orders of magnitude. In the Mo devices, the treatment resulted in a lower Schottky barrier height, as extracted by the forward I-V characteristics. However, the same process increased the SBH of the W and Nb treated devices compared to the untreated devices. XPS analysis on the Schottky interface revealed the formation of a metal-phosphorous-oxygen complex at the Schottky interface. Put together, this suggests that the metal phosphate that forms with Mo has a lower work function than the original, resulting in the lower SBH, whereas in the W and Nb, the resulting phosphate has a higher work function greater than the original metal. XPS also revealed that the P_2O_5 treatment appears to heavily n-type dope the Schottky subsurface (<50 nm), given an increase in the valence band to fermi level offset to 3.25 eV.

For the fully realised 3.3 kV PiN diodes, the functionality of the hybrid termination was proven with breakdown voltages exceeding 3,500 V on all measured devices. The on-state of the JBS diodes was then characterised, where the same impact of the surface passivation treatment on barrier heights and ideality factors could be seen. All the large area devices had a $R_{SP, ON}$ between 15-17 mΩcm^2. Most significantly, off-state characterisation of the JBS diodes revealed a reduction in leakage current levels and the maximization of the breakdown voltage in the P_2O_5-treated samples, with the Mo treated device showing leakage currents below 1 x 10^{-6} A up to 3,560 V. The Nb devices had extreme leakage at low reverse

voltage, so only dynamic charactictics of the Mo and Ni devices were then measured using a clamped inductive switching circuit at room temperature. No difference was evident between the devices, their switching performance all similar to that of a commercial 1.7 kV diode, all devices having Q_R values of approximately 78 nC.

In summary, this chapter established that Mo appears to be an appropriate low work function metal that could be used to realise SiC JBS diodes rated at 3.3 kV and above with low on-state losses. However, through a combination of effects, namely manipulating the metal work function, doping the subsurface and terminating defects, a phosphorous pentoxide treatment is an essential step in minimising the off-state leakage, such that the optimal breakdown voltage can be reached. While P_2O_5 treatment also benefits the Nb and W diodes, the resulting SBHs are respectively too low (causing early onset leakage current) and too high (resulting in large on-state losses), compared to the P_2O_5 treated Mo devices.

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5 Development of High-Quality Gate Oxide on 4H-SiC Using Atomic Layer Deposition

A novel process to form a high quality gate oxide is proposed and explored in this chapter. Improvements in the reliability and quality of ALD-deposited SiO_2 layers on SiC are demonstrated, through the fabrication and characterisation of MOSCAPs, while a preliminary investigation on Al_2O_3-deposited layers is also included. The results of ALD-deposited SiO_2 layers with and without a range of post-deposition anneals (PDAs) are shown, demonstrating a high quantity of oxide charge and a poor interface quality for as-deposited samples, which is improved following PDA. The analysis of interface trapped charge, flatband voltage, hysteresis, frequency dispersion and a distribution of breakdown voltages of annealed samples are investigated as metrics of improvement following the PDA process. Results are benchmarked against a MOSCAP process using SiO_2 thermally grown in an N_2O ambient[1]. X-ray photoelectron spectroscopy (XPS) is used to investigate the physical and chemical properties of the interface and the reliability of the fabricated devices was studied using time-dependent dielectric breakdown (TDDB) measurements. These techniques demonstrate the benefits of ALD dielectrics, establishing a high-quality gate deposition process that could supersede thermal oxidation in MOS structures.

The work presented in this Chapter has been published in[2, 3].

5.1 INTRODUCTION

SiO_2 can be readily grown at standard temperatures between 1200°C and 1400°C [4, 5] on SiC surfaces using thermal oxidation, hence being the dominant gate oxide in SiC metal-oxide-semiconductor (MOS) based

devices. However, compared to the Si/SiO2 interface, the 4H-SiC/SiO_2 interface has a high density of interface traps (D_{IT}), which is a major cause of low channel mobility and threshold voltage instability in 4H-SiC MOSFETs.

The relationship between the density of interface traps and and channel mobility here can be seen when considering the dominant scattering and trapping processes in SiC MOSFETs:

Generally, electron mobility in the inversion channel is affected by several scattering mechanisms, which can be described by using Matthiesen's rule as shown in [6]:

$$\frac{1}{\mu_{inv}} = \frac{1}{\mu_C} + \frac{1}{\mu_P} + \frac{1}{\mu_I} \quad (5.1)$$

With μ_{inv} – inversion layer mobility, μ_C – charge carrier mobility contribution from Coulombic scattering, μ_P – phonon scattering and μ_I – charge carrier mobility contribution from scattering at the 4H-SiC/SiO_2 interface (roughness).

The term μ_C is a result from carrier-carrier electron scattering, resulting from both fixed charge states at the interface traps and further by considering more distant charged defects within the dielectric (SiO_2) or the semiconductor (4H-SiC). The second term μ_P describes the fraction that results from phonon scattering whereas the last term describes the scattering that stems from SiC/SiO_2 interface roughness in MOSFETs.

Due to their high density, interface traps are the most important trap type that affect the field-effect mobility in SiC. The field-effect mobility is the most widely used parameter to describe channel conduction in 4H-

SiC inversion layers, which can be experimentally determined using the following equation, according to [7, 8]:

$$\mu_{FE} = \frac{Lg_m}{WC_{OX}V_{DS}} \quad (5.2)$$

with μ_{FE} – field effect mobility, g_m – transconductance, L- gate length, W- gate width, C_{OX} – gate oxide capacitance and V_{DS} – gate-source voltage.

Interface traps are physically located in an electrically accessible charged state at the SiO_2/SiC interface, capturing and emitting electrons and holes at the interface. Physically, they can be described as either dangling bonds, Si clusters (Si-Si bonds) or carbon clusters (C-C bonds) or any other disorderly complex in the transition zone from semiconductor to dielectric.

The charged state of interface traps leads to a decrease in channel conductivity due to the increase in Coulomb scattering of electrons, hence lowering mobility.

The high D_{IT} is the result of residual carbon [9] which remains near the interface after thermal oxidation resulting in trap states with energy levels within the bandgap of SiC.

High-quality deposited dielectrics have attracted recent interest as a means to eliminate, or significantly reduce, the D_{IT} created during high-temperature thermal oxidation. With deposited dielectrics, substrate consumption and the amount of carbon released from the substrate is minimised, and thus the interface states inherent in thermal oxidation can be greatly reduced. Among several dielectric deposition techniques, atomic layer deposition (ALD) is widely used due to the quality of the

oxide, its superior uniformity, the precise control of thickness and process steps, and its low deposition temperature. The deposition of aluminium oxide (Al_2O_3) layers and their use as gate dielectrics in MOSCAP and MOSFET structures on 4H-SiC has been widely investigated [9-11] with fewer reports being made on the deposition of SiO_2 [12-14]. Promising interfacial properties of ALD-deposited Al_2O_3 layers on 4H-SiC were reported to result in high field-effect mobilities (μ_{FE}) of 64 cm^2/Vs [10]for purely ALD-deposited dielectrics and 258 cm^2/Vs [10] for a combination of thermal and ALD-deposited oxides in MOSFETs [9, 10]. Although both Al_2O_3 and SiO_2 ALD-deposited layers have shown promising electrical properties[15], there are still issues related to the bulk oxide and the oxide-SiC interface that need to be remedied; for instance, ALD-deposited layers can form porous oxides, causing problematic electric properties such as increased leakage current and premature dielectric breakdown. First investigations into the impact of 1100°C PDA in Argon (Ar) [14] and nitrous oxide (N_2O) [11, 12] ambients on deposited layers have reported improvements in the I-V and C-V performance of MOSCAPs, reducing both leakage currents and flatband voltages. Other high k- dielectric layers such as hafnium oxide (HfO_2), titanium oxide (TiO_2) or tantalum oxide (Ta_2O_5) have been investigated due to their very high permittivity values, which should, according to Gauss's law (product of permittivity and electric field normal to the dielectric/semiconductor interface has to be continuous [6]), theoretically reduce the electric field in the dielectric. However, due to their other material properties such as small barrier height at the interface between HfO_2/SiC, the presence of high tunnelling currents even at low electric fields made them unsuitable for SiC device applications. Since the increase of the permittivity does lead to an increase in oxide capacitance when the oxide thickness remains constant, the replacement of a dielectric with a dielectric that has a higher

permittivity will generally lead to an increase in switching losses, they are also generally considered less suitable for the many high-frequency, high power applications in silicon carbide.

5.2 DEVICE FABRICATION AND EXPERIMENTAL PROCEDURE

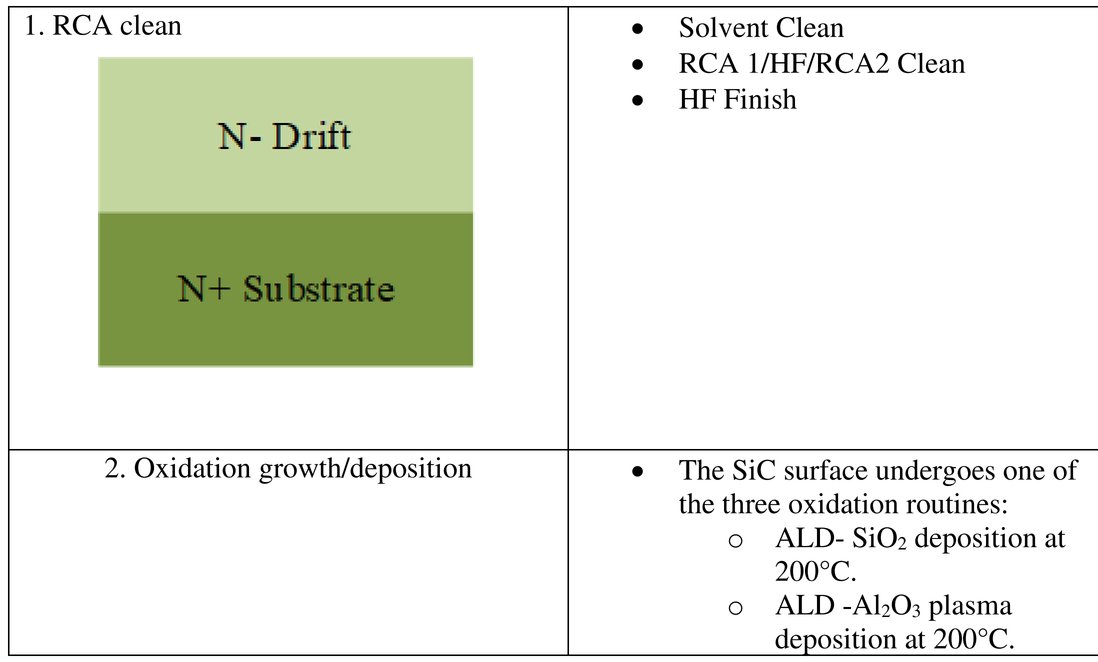
The 10 μm thick drift layers of 3-5 × 10^{15} cm^{-3} n-type doping were epitaxially grown in-house on 100 mm diameter, 4° off-axis, highly doped n-type 4H-SiC wafers. Growth was performed using a 30 μm/hr growth rate and N_2 as a dopant in an LPE ACiS M8 chemical vapour deposition (CVD) reactor. In parallel, commercial material with the same epitaxial layer thickness and the same n-type doping was used for verification purposes of the material. Surface roughness values of ~300 pm were obtained for both as-grown materials using atomic force microscopy (AFM).

After an initial RCA1/HF/RCA2/HF clean, 14 × 14 mm SiC chips underwent one of the three oxidation routines, resulting in approximately 30 nm thick oxides, which was confirmed using accumulation capacitance electrical measurements as well as AFM step height measurements::

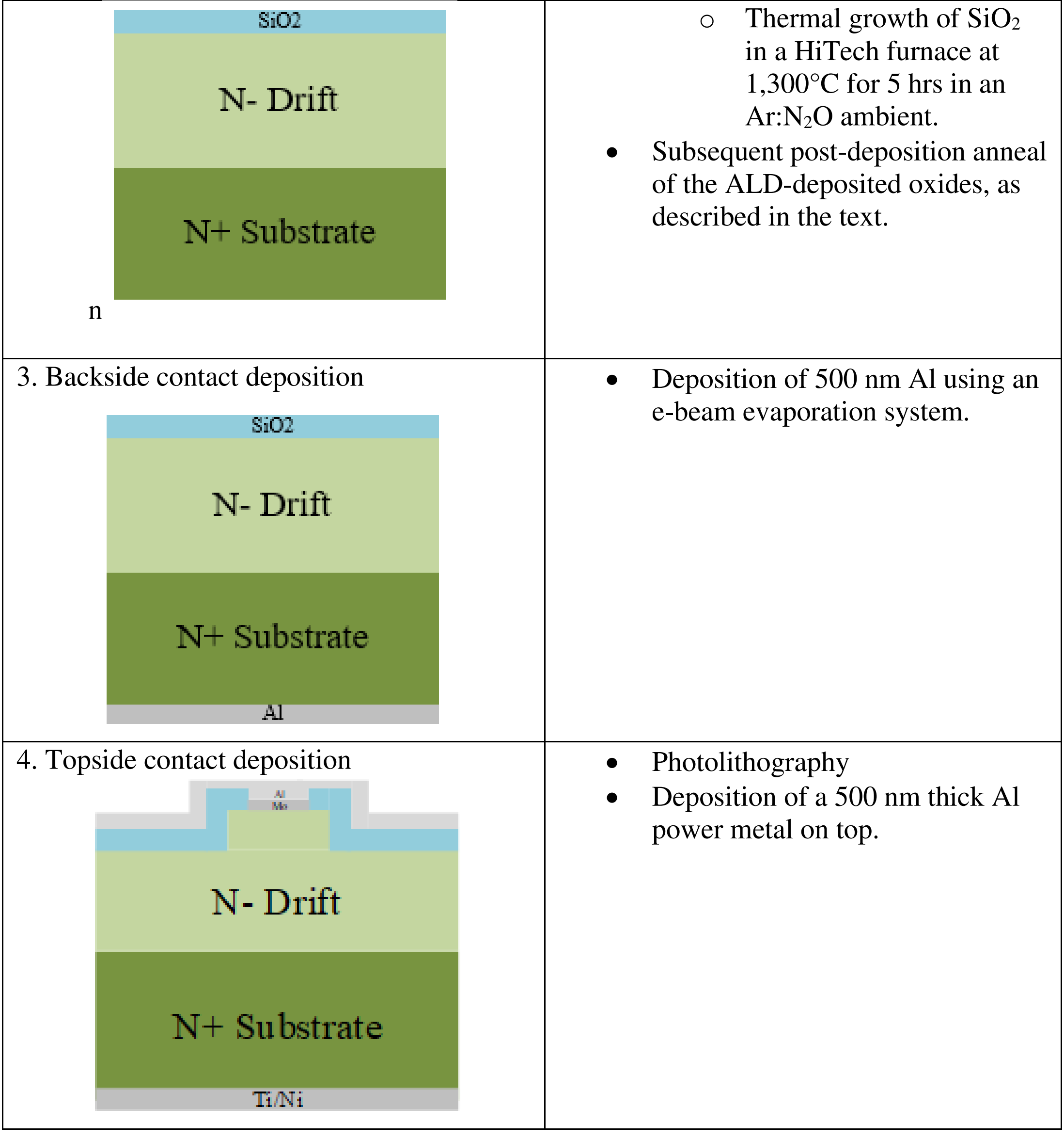
- 1: SiO_2 plasma deposition at 200°C using bis(diethylamino)silane (BDEAS) and O_2 plasma precursors in an Ultratech Fiji G2 Plasma-Enhanced ALD System.
- 2: Al_2O_3 plasma deposition at 200°C using trimethylaluminium (TMA) and O_2 plasma in the same ALD system.
- 3: Thermal growth of SiO_2 in a HiTech furnace at 1300°C for 5 hours in an Ar: N_2O (4 slm: 1slm) ambient.

Samples were then loaded into a high temperature anneal furnace and annealed at elevated temperatures for 1 hour in oxidising (N_2O), inert (Ar) or reducing (forming gas: H_2:N_2, 1:19) atmosphere at a gas flow rate of 5 slm. Subsequently, Al gate contacts (500 nm) were deposited and patterned using a wet etch. Finally, a 500 nm Al layer was deposited on the backside of the samples by electron beam evaporation, forming an ohmic contact, similar to [11, 16, 17]. Devices that were used for dielectric breakdown measurements had a protecting >1 μm thick SiO_2 layer deposited before gate oxide deposition via LPCVD. Here, the gate patterning was carried out by means of a lift off process using S1818 photoresist with a thickness of 1.8 μm. The schematic of the MOSCAPs' cross section is depicted in Fig. 5.1, with the second structure using a field oxide for passivation, isolation between devices and to aid wire bonding for the TDDB rig. The process flow can be found in Table 5.1.

Table 5.1: Process flow for the MOSCAP fabrication.

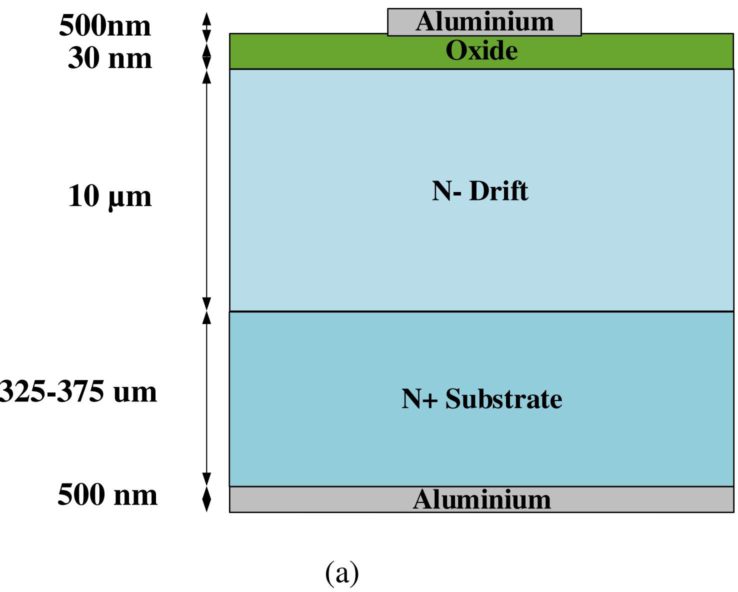


1. RCA clean	• Solvent Clean • RCA 1/HF/RCA2 Clean • HF Finish
2. Oxidation growth/deposition	• The SiC surface undergoes one of the three oxidation routines: o ALD- SiO_2 deposition at 200°C. o ALD -Al_2O_3 plasma deposition at 200°C.



n	○ Thermal growth of SiO_2 in a HiTech furnace at 1,300°C for 5 hrs in an $Ar{:}N_2O$ ambient. • Subsequent post-deposition anneal of the ALD-deposited oxides, as described in the text.
3. Backside contact deposition	• Deposition of 500 nm Al using an e-beam evaporation system.
4. Topside contact deposition	• Photolithography • Deposition of a 500 nm thick Al power metal on top.

Room temperature vertical C-V measurements were recorded using an Agilent E4980 precision LCR meter. The D_{IT} was then determined using the high-low method (1 MHz and 1 kHz), flatband voltage was extracted from a theoretical flatband capacitance (C_{FB}), hysteresis voltage was extracted for the same value and frequency dispersion in accumulation was extracted as an average percentage per decade increase in frequency. A custom-built TDDB testing rig was used for room temperature breakdown measurements, enabling simultaneous leakage current measurements of 32 devices. Devices were held at each



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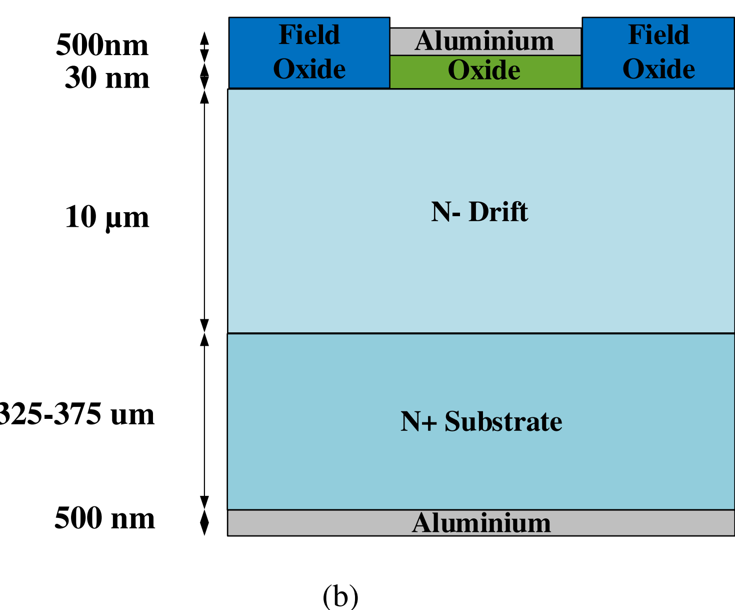

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Figure 5.1: Cross section schematic diagram of (a) fabricated MOSCAPs used for C-V analysis and (b) MOSCAPs used in the TDDB testing rig.

electric field for 1h before stressing them at the next higher voltage level. The breakdown current level was set at 1 µA.

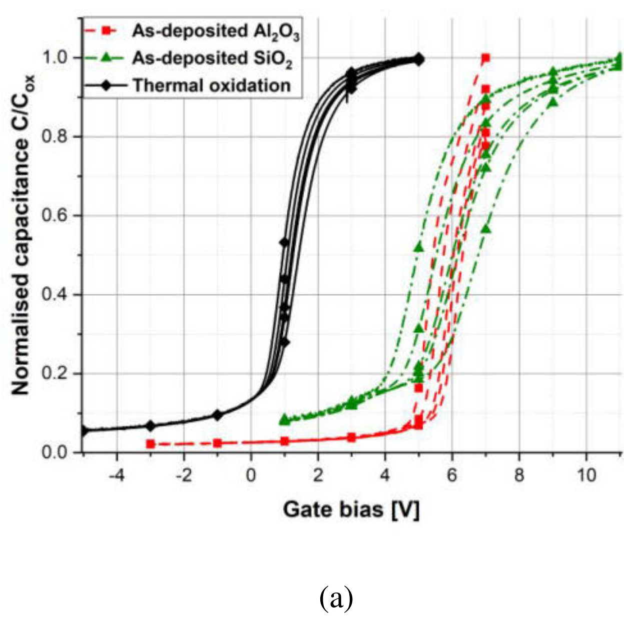
For XPS analysis of ALD-deposited samples, the oxide thickness was limited to 5 nm to ensure photoemission from the oxide, interface and substrate could be detected without exposing the interface to air or

inducing damage from sputtering. After deposition, the samples were then annealed prior to loading in the XPS chamber. This ensured the preservation of the same surface as for the fabricated MOSCAPs prior to loading in the XPS chamber. XPS was then performed using a Kratos AXIS Ultra DLD system, with the hybrid magnetic-electrostatic lens configured in electrostatic mode to enable the use of a charge neutraliser. Excitation was a monochromated aluminium Kα source (1486.6 eV) with a take off angle (ToA) of 90°. High-resolution core spectra were taken for Si 2p and C 1s. The ratio of the respective SiC components in the Si and C spectra were used to quantify the interface stoichiometry and any other elements were below 2% atomic concentration.

5.3 INITIAL C-V AND TDDB MEASUREMENTS

Room temperature C-V measurements at frequencies from 1 kHz to 1 MHz were taken from 16 devices utilising as-deposited Al_2O_3 and SiO_2 layers as gate dielectrics.

Fig. 5.2 shows normalized C-V responses as well as their respective interface trap densities. C-V responses from thermally oxidised devices are shown for comparison. Average flatband voltages of approximately 6 V (Al_2O_3) and 8.5 V (SiO_2) demonstrate the presence of negative charge in both ALD oxide layers and at the interface. These values are consistent with other reported MOSCAPs using as-deposited layer structures [11, 18]. Al_2O_3 MOSCAPs show the poorest response in accumulation mode, including the highest accumulation frequency dispersion of 23% (from 1 kHz to 1 MHz), suggesting that it is not fully accumulated, which could be due to fixed or slow charge. The capacitance of SiO_2-deposited devices



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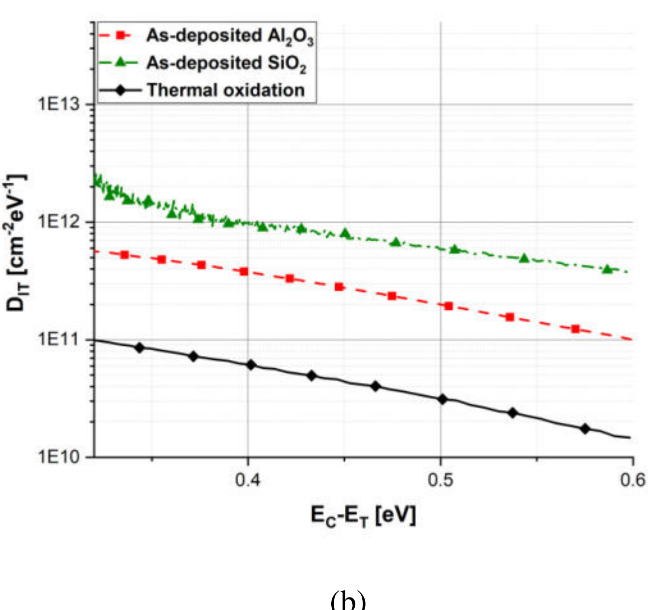

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Figure 5.2: (a) Representative C-V response of as-deposited layers and (b) their density of interface traps.

fully accumulates, with minimal frequency dispersion in accumulation. In depletion, the high density of interface traps causes a spread of C-V response, which is confirmed by the calculation of density of interface traps. Here, D_{IT} values, are approximately an order of magnitude higher than for thermally oxidised MOSCAPs. The relatively poor response of the as-deposited oxides is likely due to their reported porosity and

negative charge trapping effects [19, 20] resulting in high leakage currents and emphasising the need for further optimisation of the quality of these films through the use of PDAs. The results of a systematic PDA study on the ALD-deposited SiO2 layers, comprising the key C-V parameters, can be found in Table 5.1. The Al_2O_3 layers were not taken forward to this study, due to their high flatband voltage, lack of complete accumulation and high D_{it} , although the performance of these ALD- Al_2O_3 deposited

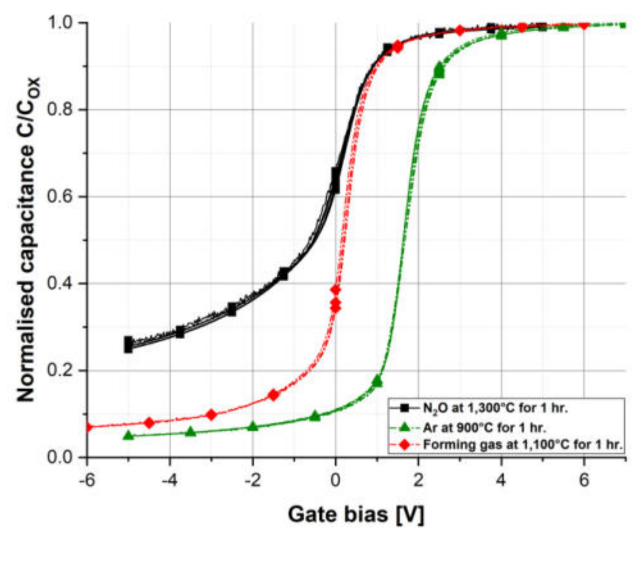
Table 5.2: Flatband voltage, hysteresis and frequency dispersion of the ALD SiO_2 MOSCAPs, after PDA. All values are given with standard deviations. 16 devices were measured for each annealing condition.

Ambient	Temp. [°C]	Flatband voltage [V]	Hysteresis [V]	Frequency dispersion [% dec^{-1}]
As-deposited	-	8.39 ± 1.016	0.19 ± 0.134	2.58 ± 1.54
N_2O	900	1.08 ± 0.11	0.18 ±0.008	0.13 ± 0.04
	1100	2.1 ± 0.13	0.28 ± 0.09	1.48 ± 1.79
	1300	0.49 ± 0.05	0.08 ±0.003	0.26 ± 0.15
Argon	900	0.73 ± 0.62	0.08 ± 0.009	0.04 ± 0.03
	1100	-1.28 ± 0.98	0.1 ± 0.03	2.81 ± 3.51
	1300	-1.21 ± 0.45	0.04 ± 0.02	0.11 ± 0.009
Forming Gas	900	7.86 ± 0.71	0.31 ± 0.09	0.68 ± 0.23
	1100	0.23 ± 0.13	0.08 ± 0.008	0.12 ± 0.05
	1300	0.4 ± 0.08	-	0.41 ± 0.37

layers could very likely have been improved by carrying out a post-deposition annealing, such as in [11]

All the PDA treatments have resulted in the reduction of the flatband voltage and hysteresis when compared to the as-deposited SiO_2 devices. This indicates a significant reduction of the density of trapped oxide charge both in the bulk oxide and near the SiO_2/4H-SiC interface when the oxide is exposed to high temperatures.

Of greatest significance from the PDA study is the forming gas anneal performed at 1100°C for 1 hour, highlighted in Table 5.I. This results in a significant improvement to flatband voltage, frequency dispersion, hysteresis and D_{IT} compared to the as deposited ALD SiO_2, and even the conventional thermally oxidized samples with a N_2O PDA. A V_{FB} of 0.23 V ± 0.13 V and D_{IT} of 2×10^{11} cm^{-2} eV^{-1} at E_C-E_T = 0.2 eV was achieved. This confirms previous investigations on forming gas-annealed thermal oxides [21], in which forming gas anneals above 1050°C before and after deposition reduced D_{IT} by one order of magnitude ($< 1 \times 10^{12}$ cm^{-2}). Argon annealing resulted in the widest distribution (Fig. 5.3b) of flatband voltage with an average of 0.73 V at 900 °C. The N_2O annealed samples generally show the tightest distribution at all three temperatures, with 1300 °C-annealed samples averaging a V_{FB} of 0.49 V. However, annealing at 1300 °C resulted in the growth of thick (>200 nm) thermal SiO_2, the result of the high oxidation rate of SiO_2 at these temperatures. This makes these devices unsuitable for gate oxide applications.



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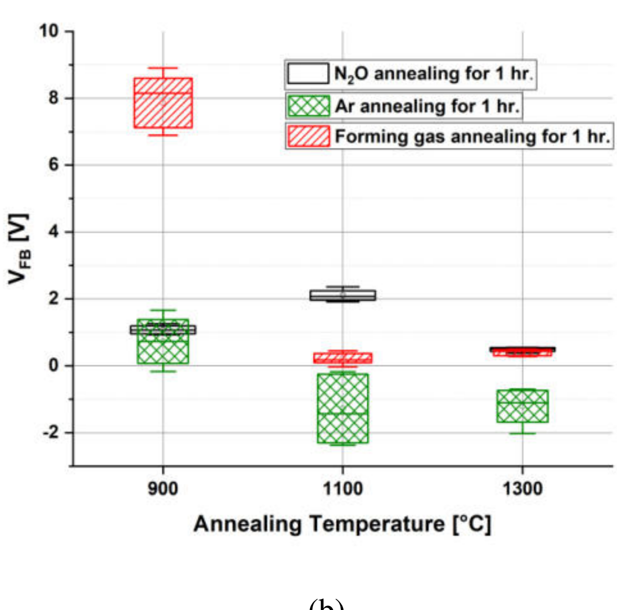


(b)

Figure 5.3: (a) Typical C-V response of best annealed samples for each ambient and (b) the distribution of flatband voltages after PDAs at different temperatures and ambients.

MOS capacitors with both thermally-grown and ALD-deposited oxides (as-deposited and forming gas annealed) underwent TDDB testing, and a breakdown distribution is shown in Fig. 5.4.

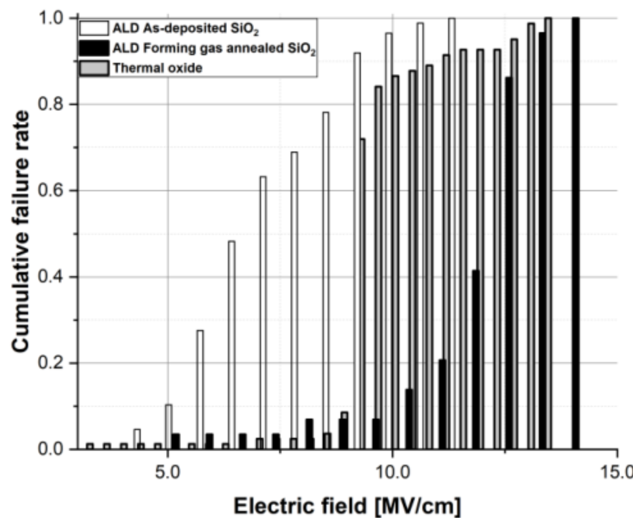


Figure 5.4: The breakdown distribution of MOSCAPs, measured at room temperature.

The measurement covered a wide electric field from to approximately 15 MV/cm. The obvious difference between the three distributions confirms that both the choice between thermal oxidation and ALD-deposition and choice of PDA process plays a major role in the reliability of the oxide layers. It can be seen that at least two breakdown mechanisms are recognizable from the failure distribution of the thermal oxides. When neglecting the first 6 premature devices up to 6.5 MV/cm, there is a sharp increase in device failures of thermally oxidized samples at breakdown fields <10 MV/cm. At breakdown fields higher than 10 MV/cm, the devices break down more gradually for this dataset. For the as-deposited layers, a first sharp increase can be seen at an electric field of 5 MV/cm. Between 5 MV/cm and 9 MV/cm, most devices break down linearly and only a few devices are still operating at breakdown voltages higher than 10 MV/cm. This can be attributed to the porosity of the ALD oxide. The forming gas annealed samples show the best breakdown distribution, with less than ten percent of devices having broken down at breakdown fields below 10 MV/cm. Once this electric field has been exceeded, the majority

of devices breakdown at an electric field of 12.5 MV/cm. Since the improvement was clearly correlated to the forming gas treatment, further investigations by means of XPS and SIMS and C-V measurements were made to understand the mechanism behind the improvement brought about by the forming gas anneal.

5.4 IN-DEPTH C-V INVESTIGATION OF THE SIO_2/4H-SIC INTERFACES

This part of the investigation focuses on the aforementioned forming gas PDA, but also includes the impact of PDAs in nitrogen (N_2) and argon (Ar) ambients to clearly distinguish the observed effect. For benchmarking reasons, a thermal oxidation in N_2O ambient was also included.

Room temperature vertical capacitance-voltage (C-V) measurements were recorded using an Agilent E4980A LCR meter, with the D_{IT} being calculated using the high-low method (1 MHz and 100 Hz). 100 Hz was chosen as the low frequency for the extraction of trap levels to keep a logarithmic frequency range from 10^2 to 10^6 Hz [8]. The surface potential was calculated using the Berglund integral [22], integrating around the flatband voltage [23]. The inaccuracies of this approach due to higher time constant dispersion in SiC as opposed to Si, shifting the surface potential towards the majority band edge, have been described in recent investigations [24, 25]. However, since this investigation is a comparative study of different anneals, an estimate of D_{IT} can be provided and general trends can be derived and, as problems such as underestimation of interface traps are considered to equally affect the whole sample set. An overview of results of at least 50 room temperature measurements per dataset are shown in Table 5.2. Representative C-V responses as well as

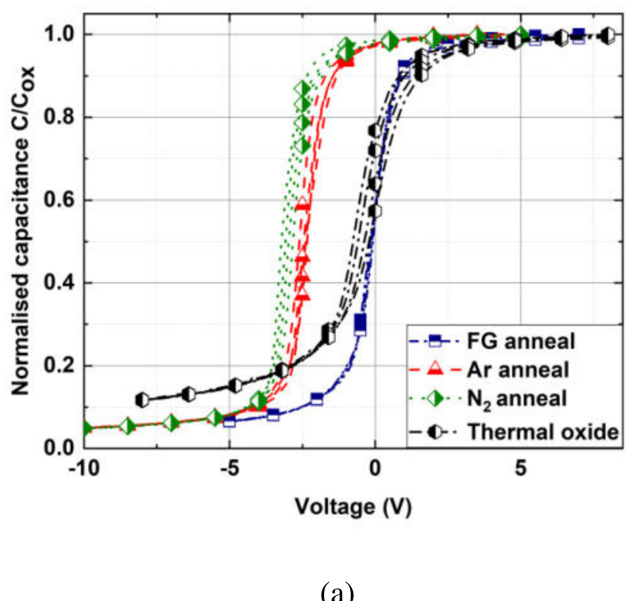
their associated D_{IT} profiles relative to the conduction band edge are shown in Fig. 5.5. The D_{IT} extracted from the sample which was grown in N_2O ambient is in agreement with other reports[1].

Table 5.3: Flatband voltage, hysteresis and frequency dispersion of the ALD SiO_2 MOSCAPs, after PDA. All values are given with standard deviations. 16 devices were measured for each annealing condition.

Sample	**Flatband voltage (V)**	**Hysteresis (V)**	**Frequency dispersion (%dec^{-1})**
ALD as-deposited	8.39 ± 1.02	0.19 ± 0.13	2.58 ± 1.54
ALD + FG	-0.29 ± 0.13	0.10 ± 0.08	0.33 ± 0.29
ALD + Ar	-2.72 ± 0.79	1.86 ± 0.18	0.31 ± 0.15
ALD + N2	-2.93 ± 0.12	2.83 ± 0.15	0.25 ± 0.11
Thermal oxide	0.61 ± 0.12	0.15 ± 0.01	0.40 ± 0.19

They are also very repeatable with the flatband volate and hysteresis both having tight distributions, averaging 0.61 V and 0.15 V, respectively.

Although the Ar and N_2 annealed ALD-deposited oxides both improved upon the as-deposited ALD sample's average flatband voltage of 8.4 V, their C-V responses are poor compared to the N2O oxidation process, with average flatband voltages decreasing to -2.72 V and -2.93 V, indicating the presence of positive charge at, or near, the interface. Furthermore, their high average hysteresis voltage values of 1.85 V and 2.83 V respectively indicate a significant quantity of positive mobile ions in the dielectric layer, which will be subject to further investigation later in this chapter. The most significant outcome of this study is that the forming gas annealed samples show the most promising performance of the dataset, with flatband voltages averaging -0.29 V and the hysteresis values averaging 0.10 V, as shown in Fig. 5.5.



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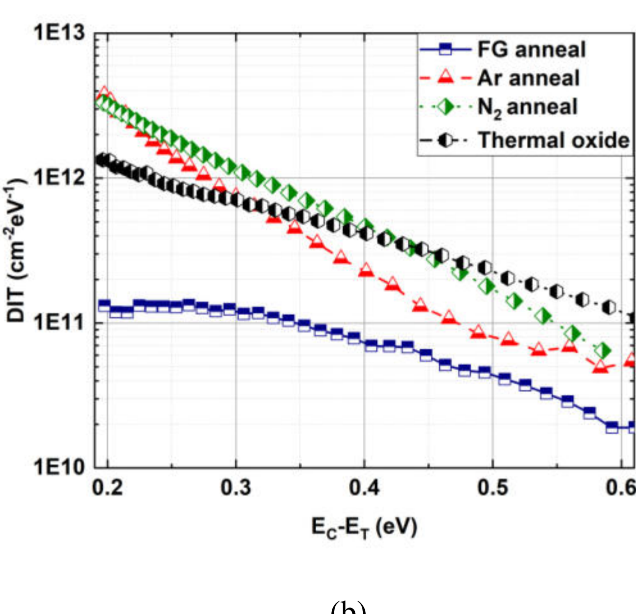

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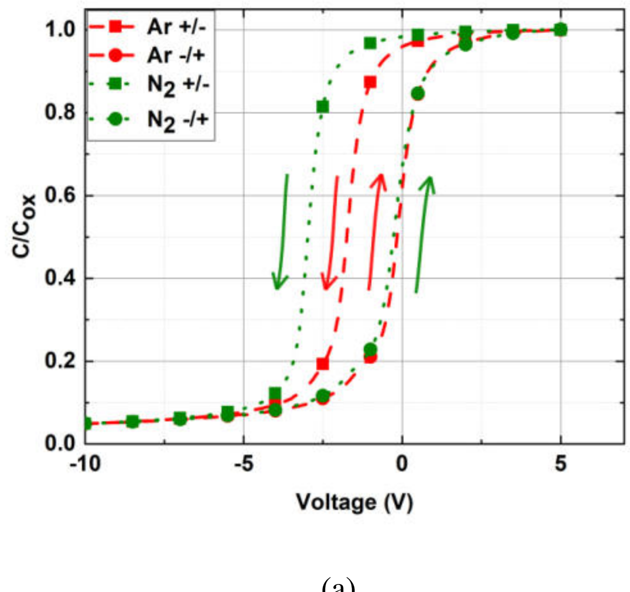
Figure 5.5: (a) Capacitance-voltage (1 kHz, 10 kHz, 100 kHz, 1 MHz), normalised to the oxide capacitance, of annealed ALD-deposited and thermally oxidised samples and (b) D_{IT} with respect to the energy trap level E_T below the conduction band level E_C.

The density of interface traps of the forming gas annealed samples is lower than the other datasets, with a D_{IT} of 2.12×10^{11} cm^{-2} eV^{-1} at E_C-E_T = 0.2 eV, an order of magnitude lower than the N_2O oxide growth process.

Of further significance is the deviation between forming gas and nitrogen annealed samples, with the D_{IT} of the N_2 samples being 6.6×10^{12} cm^{-2} eV^{-1} at E_C-E_T = 0.2 eV. This is a first indication of the possible impact of hydrogen on the electrical performance of the investigated MOSCAPs.

The existence of another charge phenomenon within the different MOSCAP oxide layers was quantified by analysing the hysteresis in their C-V responses. Representative responses of the Ar and N_2 annealed samples at 1 MHz are shown in Fig. 5.6 (a). They were first swept from accumulation into deep depletion, keeping the oxide electric field below 3 MV/cm. Afterwards, the same samples were swept “backwards”. The observed dependence on the sweep direction is an indication of positive mobile charge states near the interface which are spontaneously generated during the operation of the device, causing a counter-clockwise capacitance shift. The counter-clockwise hysteresis was observed in the FG-annealed and thermally oxidised samples as well. Investigations on thermally oxidised SiO_2/4H-SiC structures initially suggested extrinsic effects such as ions introduced by metallisation or through hydrogen related anneals as the cause for the counter-clockwise hysteresis behaviour[26-28]. This was later found out to be an intrinsic behaviour, in which mobile positive ions in the oxide are accelerated towards the bottom of the SiO_2/SiC interface with deteriorating consequences on its interface trap density, reliability and bias temperature instability in measured MOSFETs [29, 30]. The mobile charge areal density (D_{MC}) can then be calculated using the following relationship:

$$D_{MC} = \frac{(\Delta V_{FB} \times C_{OX})}{q} \quad (1)$$



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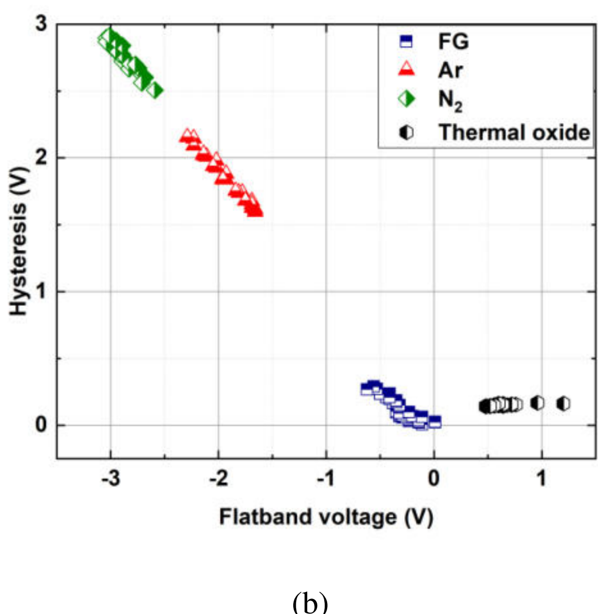


(b)

Figure 5.6: (a) Hysteresis C-V response of Ar and N2 annealed samples at 1 MHz. Samples were swept from accumulation to deep depletion and backwards. (b) Hysteresis voltage plotted over flatband voltage for 50 MOSCAPs per different sample.

where q is the electron charge (C), C_{OX} is the oxide capacitance per unit area (F cm^{-2}) and ΔV_{FB} is the hysteresis voltage (V). An overview of the density of mobile ion charge can be found in Table 5.3. The Ar and N_2

Table 5.4: Density of mobile charge states from 25 samples each with a device area of 1.257×10^{-3} cm^2. Values are average values provided with standard deviations.

Sample		Density of mobile charge states (cm^{-2})
ALD + FG		$1.13 \times 10^{10} \pm 5.84 \times 10^{9}$
ALD + Ar		$3.71 \times 10^{11} \pm 3.47 \times 10^{10}$
ALD + N_2		$5.63 \times 10^{11} \pm 2.28 \times 10^{10}$
Thermal oxide		$1.28 \times 10^{10} \pm 9.00 \times 10^{8}$

annealed MOSCAPs had the highest density of mobile ion charge, averaging 3.71×10^{11} cm^{-2} and 5.63×10^{11} cm^{-2}, respectively.

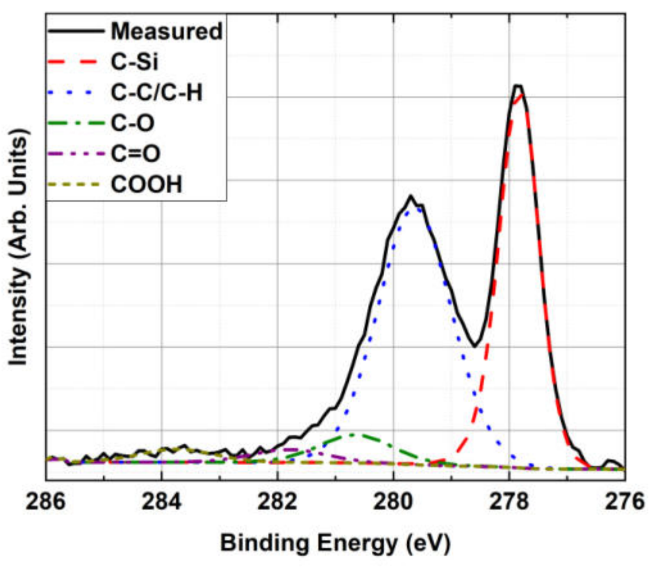
In contrast, the forming gas annealed MOSCAPs had a much reduced density of these, averaging 1.13×10^{10} cm^{-2}, a value very slightly lower than the average value for the N2O- oxidised MOSCAPs. The reduction in hysteresis voltage can also be seen in Fig. 5.6 (b), with the hysteresis voltage being the flatband voltage difference between the measurements. The outcome of the FG-annealed improvement also represents a reduction by more than an order of magnitude compared to previous reports of ALD- deposited SiO_2 [12], and a reduction by a factor of 4 when compared to reports on high-quality ALD-deposited Al_2O_3 [11, 19], which showed clockwise hysteresis, which were the result of slow states in the oxide.

5.5 SURFACE CHEMISTRY STUDY USING XPS AND SIMS

For a further investigation into the origin of the improvement brought about by the FG-anneal, XPS was performed using a Kratos Axis Ultra DLD system on ALD as-deposited, N_2-annealed and FG-annealed SiO_2-SiC samples to investigate interface stoichiometry. Direct quantification of carbon clusters is not possible due to adventitious carbon that appears at the same binding energy as carbon clusters. However, the stoichiometric ratio of Si-C in the Si 2p spectrum and C-Si in the C 1s

spectrum is used to investigate interface chemistry. The samples were illuminated with Al Kα X-rays (1486.6 eV) and the spectra were analysed at a take off angle (ToA) of 90°, giving a 3 λ depth of 10 nm. All investigated oxides were approximately 5 nm thick. High-resolution core spectra were taken for Si 2p, C 1s, O 1s and N 1s, and the data were analysed using the CasaXPS software package, employing Shirley backgrounds and Voigt (Gaussian-Lorentzian) lineshapes. XPS data and fits of the ALD as-deposited sample can be found in Fig. 5.7. Only marginally different spectra and fits were obtained for the other investigated samples. All three ALD samples showed a higher signal from Si-C in the Si 2p spectrum than the C-Si in the C 1s, implying Si enrichment at the surface. The as-deposited sample showed the least Si enrichment, with a C:Si ratio of 0.8, the N_2-annealed sample's ratio was 0.74 and the FG-annealed sample showed a marginal decrease to 0.72.

These C:Si ratios contrast sharply with those from thermal oxidation processes [31], where the C:Si ratio is higher than 1. However, N_2O processes have been shown to improve stoichiometry, bringing the C:Si ratio closer to 1, than for dry oxidation processes[31]. In thermal oxidation processes in N_2O ambient, N is assumed to passivate excess carbon, resulting in an overall less defective interface. In deposition processes, however, the C:Si ratio lower than 1 suggests that native Si and the Si precursor BDEAS bind to C, resulting in little-to-no residual carbon at the interface and excess Si dominating interface defect levels. In contrast to C defects, which are typically reduced only by nitridation, a wider range of Si passivation treatments exist, most prominently FG annealing [23]. The decrease in C:Si ratio with any anneal step, as well as a decrease in the Si-suboxide component, suggests that Si complexes, such as Si dimers



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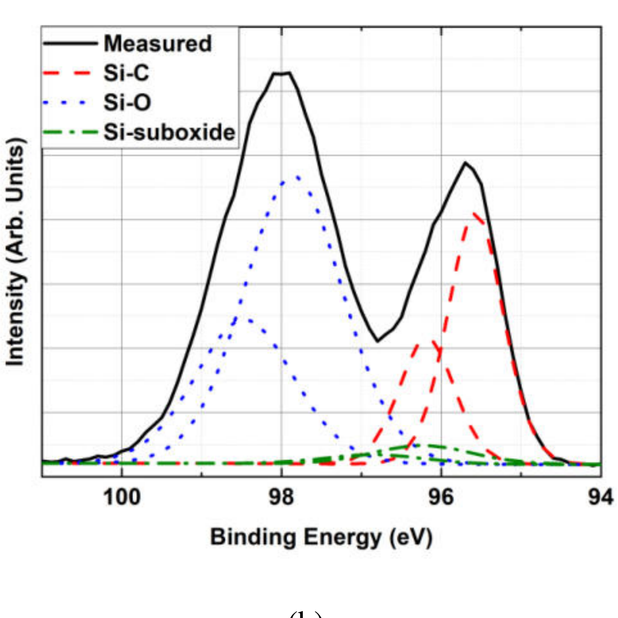


(b)

Figure 5.7: XPS data and fits for the (a) C 1s region and (b) Si 2p region of the ALD as-deposited sample.

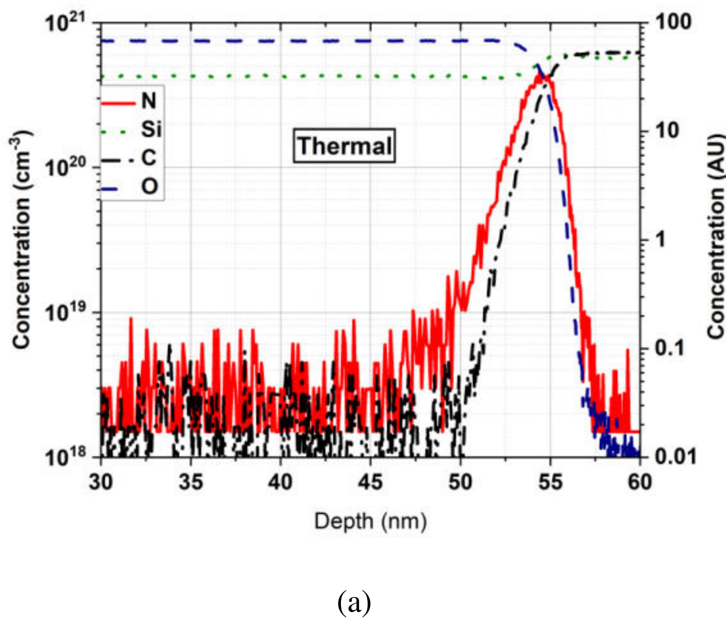
or Si_xO_y groups, are broken down into simple Si dangling bonds, which can be readily passivated with a FG anneal. When compared to work by Umeda *et al.* [32, 33] using electron spin resonance (ESR) and electrically detected magnetic resonance (EDMR) on thermally grown SiO_2/SiC, no signal for Si dangling bonds (P_b) was found, but that the carbon dangling bond (P_bc) signal is characterised in abundance. Here, although not a

direct comparison, we note that thermally grown oxides have a c-rich interface which would support an analogous larger $P_b c$ signal. This underlines the fundamental difference between the thermally grown and the deposited SiO_2/SiC interface.

Secondary ion mass spectrometry (SIMS) was performed to investigate the distribution of nitrogen and hydrogen located at the interfaces of the thermally-grown oxide and FG-annealed ALD-deposited oxide. Due to the complexity and background noise level of SIMS measurements in MOS structures, individual samples were prepared in parallel for each profile. H and N SIMS profiles from the thermal and the FG sample are shown in Fig. 4.8 and 4.9. In these, H and N are quantified with absolute values, with Si, C and O only quantified in arbitrary units. It should be noted that the detection limit for N in SiO_2 is 2×10^{18} cm^{-3}, and H in SiO_2 is 3×10^{19} cm^{-3}, shown on the graphs. As Table 5.4 and Fig 5.8 and 5.9 show, N appears at the interface for both samples, with similar observations for H. These increases in atomic concentration can also partly originate from measurement artefacts such as a residual atmospheric contamination on the surface before oxide growth/deposition, a change in ionisation efficiency as SIMS sputter through the interface, and charging/charge compensation changing near the interface. As such, comparisons are made based on the maximum concentration of N and H at the interface, with results shown in Table 5.4.

Table 5.5: SIMS results: peak interfacial concentration of H and N.

Sample	Peak H concentration (cm^{-3})	Peak N concentration (cm^{-3})
Thermal	3.50 x 10^{20}	4.48 x 10^{20}
ALD + FG	1.50 x 10^{21}	4.40 x 10^{19}



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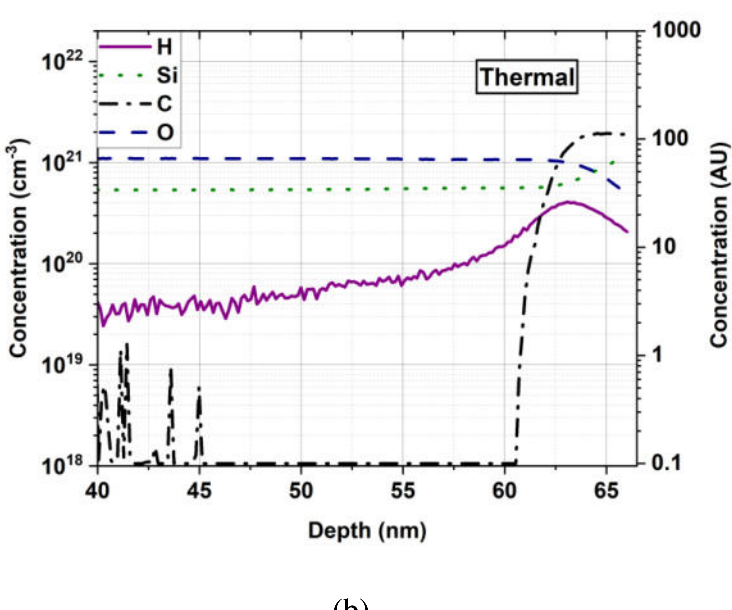
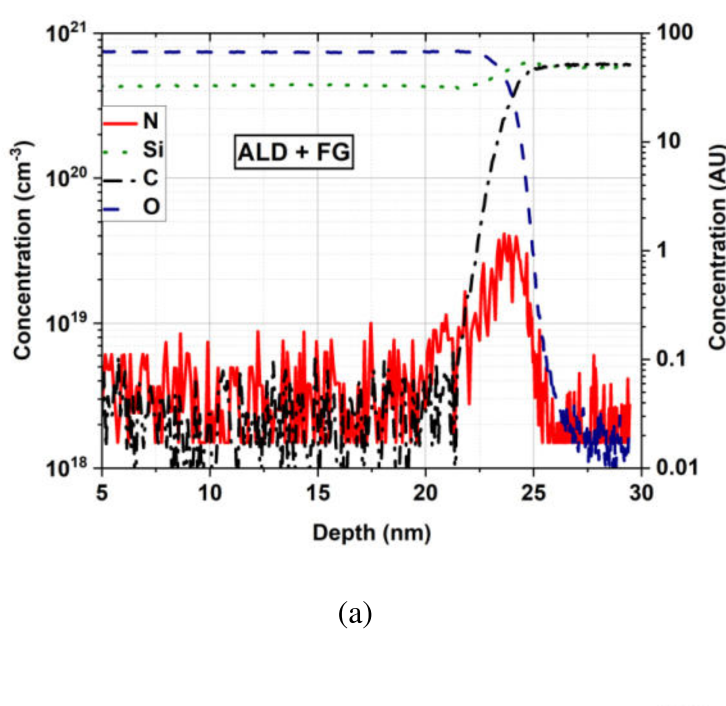


(b)

Figure 5.8: SIMS profiles of nitrogen (a) and hydrogen (b) in the thermally oxidised sample. The sample had a grown SiO_2 layer on top of the semiconductor, profiles are shown for the whole of the oxide and the first 5-10nm of the semiconductor. H and N are quantified with absolute values, Si, C and O with arbitrary units.

As one might expect, the thermally-grown oxide shows the highest peak nitrogen concentration, approximately an order of magnitude higher than the deposited oxide, and hydrogen concentration four times lower than ALD-FG oxide. The N profile for the thermal sample is similar to



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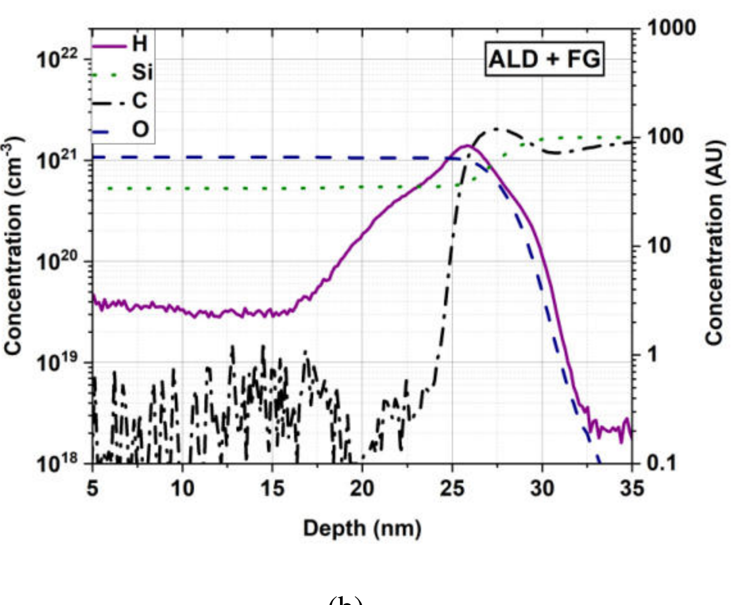

(b)

Figure 5.9: SIMS profiles of nitrogen (a) and hydrogen (b) in the FG-annealed ALD-deposited sample. The sample had a deposited SiO_2 layer on top of the semiconductor, profiles are shown for the whole of the oxide and the first 5-10nm of the semiconductor. H and N are quantified with absolute values, Si, C and O with arbitrary units.

fig. 5.8 (a), where the N levels fall below detection limits, hence both are localised to the interface rather than distributed through the oxide. Diametrically, the H peak concentration is four times lower within the thermally-grown oxide, than the ALD-FG sample. However, whilst H

levels are detected throughout the thermal oxide, they fall below detection limits in the ALD-FG sample, having implications on how this potential mobile charge can move. The results support the notion that the improvement in electrical performance of the ALD FG-annealed oxide layers can be down to the hydrogen passivation of Si dangling bonds at the oxide-semiconductor interface. The aforementioned theory of the hydrogen passivation effect is also backed up by theoretical descriptions [34, 35]in which hydrogen was found to have the potential to passivate traps near SiO_2/4H-SiC interfaces.

5.6 CONCLUSION

In summary, a high quality SiO2/SiC interface has been developed by annealing the ALD deposited SiO2 layer in forming gas for one hour at 1100° C. This has brought about improvements to the ALD layer in terms of flatband voltage (-0.29 ± 0.13 V), hysteresis (0.10 ± 0.08 V), D_{IT} (2.12×10^{11} cm^{-2} eV^{-1} at E_C-E_T = 0.2 eV) and positive mobile charge density near the interface of 1.13×10^{10} cm^{-2}. XPS analysis revealed a Si-rich interface for all ALD-deposited samples, with the FG having the most Si-rich interface with a C:Si ratio of 0.72. As Si-suboxide components were reduced as well, this suggests that the anneal breaks down Si complexes into Si dangling bonds, which can then be passivated. SIMS analysis demonstrated an increase in hydrogen concentration near the interface of the annealed sample when compared to a thermal sapmle, with a peak concentration of 1.50×10^{21} cm^{-3} being four times higher than for the thermal oxide, suggesting that the improvement in electrical performance is due to hydrogen passivation of trap states at the oxide-semiconductor interface. It is concluded that a more stoichiometric interface allows compositionally greater hydrogen passivation. Hence,

passivation in ALD-deposited SiO_2/4H-SiC becomes similar to the well-known thermal SiO_2/Si system, and is outlined here for the first time.

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6 Initial investigations into the MOS interface of freestanding 3C-SiC layers for device applications

This chapter reports on an initial investigation into the material quality and device suitability of a novel homo-epitaxial 3C-SiC growth process. The physical properties of the material are evaluated using atomic force microscopy (AFM) to extract the surface roughness and using high-resolution X-ray diffraction (XRD) to analyse the crystal quality. In addition, electrical properties are presented of SiO_2/3C-SiC MOSCAPs with comparisons made between conventional thermally formed oxides and those formed via atomic layer deposition (ALD). D_{IT}, flatband voltages and hysteresis voltages are extracted to test the suitability of this material for device applications.

The work presented in this Chapter has been published in [1].

6.1 INTRODUCTION

Due to its relatively low defect concentration, electronic quality and commercial availability, 4H-SiC is the most common SiC polytype for power electronics applications. Hence, mature unipolar 4H-SiC device structures such as Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) are commercially available and highly competitive in power converter applications (600-1700 V blocking voltage), potentially replacing Si PiN diodes and Si insulated-gate bipolar transistors (IGBTs).

Furthermore, SiC has the advantage over other wide bandgap semiconductors, whereby silicon dioxide (SiO_2) can be directly thermally

grown on the epilayer for the use as a gate oxide in metal-oxide-semiconductor (MOS) devices, offering compatibility with mature Si processing technology. However, the quality of reported 4H-SiC/SiO_2 interfaces has suffered from a higher density of interface traps (D_{IT}), as well as higher leakage current levels as a result of a smaller conduction band offset (2.7eV) compared to the Si/SiO_2 interface (3.2eV) [2].

In contrast to the hexagonal polytype 4H, silicon carbide's cubic polytype 3C offers the opportunity to be grown hetero-epitaxially on Si substrates, largely reducing material costs. Furthermore, the larger conduction band offset (3.7eV) at the 3C-SiC/SiO_2 interface theoretically enables MOS devices to have considerably lower leakage currents and D_{IT} levels than unipolar MOS devices fabricated on 4H-SiC.

The large mismatch in physical, thermal and crystallographic properties between 3C-SiC and the underlying Si substrate hampers the development of this material [3]. With the lattice mismatch and the difference in thermal expansion coefficient at deposition temperature being about 20 %[4], residual strain is created which enhances wafer bow and promotes the formation of dislocations, stacking faults, microtwins and other material defects[4] to allow strain relaxation.

The concept of pseudomorphic material is well known in the Si_{1-x-y} Ge_x C_y –on Si substrate material systems. In these, during growth, initial seed layers of these layers are deposited from the source material onto the substrate and thus thin layers which are defect free. These layers initially assume the in-plane lattice parameter of the substrate and the out-of plane lattice parameter is tetragonally distorted, hence they are fully strained layers. Upon increasing this thickness, the strain energy increases within

the layer and at a certain thickness dislocations will form to enable a strain relieving mechanism, referred to as the critical thickness.

However, the growth of 3C-SiC on Si is slightly different, in that the intial "seed" layer is replaced by a carbonisation. Here, a carbon precursor is injected at elevated temperatures and mixes with the silicon in the substrate, forming 2D nucleation of 3C-SiC phases, which laterally extend and join together with antiphase domain defects between them. Hence, ther is no initial homogeneous layer and defects are formed at the very onset of growth, so there is no point at which SiC material is fully strained, hence the terms "pseudomorphic" and " critical thickness" are not suitable in this context.

Even though high mobility (up to 228 $cm^2/V.s$) 3C-SiC MOSFETs have been reported in the past decade [5-7], in-depth studies of 3C-SiC MOS capacitors (MOSCAPs) still show high quantities of positive charge at, or near, the 3C-SiC/SiO_2 interface[8].

Homo-epitaxial growth of freestanding 3C-SiC will eliminate the lattice mismatch and the thermal expansion coefficient difference caused by heteroepitaxy of 3C-SiC on Si, which limits the epitaxial thickness and causes in built material stress, causing wafer bow and warp[9] . Other works to grow freestanding 3C-SiC [10] used sublimation growth on a chemical vapour deposition (CVD) grown 3C-SiC on Si template, with the Si template then melted in-situ. There, high quality free-standing (001), 20-90 µm thick layers with diameters of >10 mm were achieved, verified with x-ray diffraction (XRD) analysis. Other reports [11] demonstrated fabrication of free standing substrates of 300 µm thickness by growth of 3C-SiC grown on undulant Si templates, where the Si template was then chemically removed as the last step. In later works,

these were then subsequently used to grow a 40 µm thick epitaxial layer [12] by means of the sublimation epitaxy where layers showed local accumulation of stacking faults, resulting in the formation of different polytypes. Since CVD growth is more ubiquitious for active device formation a 3C-SiC homo-epitaxial CVD process with standard Si substrates would have more potential in a commerical process. Recently, a process using CVD epitaxy on standard large (100 mm) wafer diameter wafers has been reported [13], with high polytype uniformity and low defect densities.

6.2 DEVICE FABRICATION AND EXPERIMENTAL PROCEDURE

Homo-epitaxial 3C-SiC layers (on-axis) were grown using CVD on Si (100) substrates in a LPE ACiS M-10 hot-wall reactor. Initially, growth was carried out a temperature close to the melting point of Si (1400°C) to form a 90 µm highly doped 3C layer. By increasing the temperature further, the Si substrate melted and was removed, leaving the remaining freestanding SiC layer. This was used as a seed layer to homo-epitaxially grow at a temperature of 1640°C a further 150 µm of highly nitrogen-doped 3C. A final 10 µm n-type drift layer of doping (2 x 10^{16} cm^{-3}) was epitaxially grown. The exact process has been reported by Anzalone et al[14].

For benchmarking, 4H-SiC epitaxial layers were grown on 4 degrees off (0001) substrates using an LPE ACiS M8 reactor. The growth temperature was 1650°C, using a trichlorosilane (TCS) and ethylene (C_2H_4) mix in an H_2 ambient at a nominal growth rate of 30 µm/h. A 10 µm thick epilayer was intentionally doped during growth at 4 x 10 $^{15}cm^{-3}$

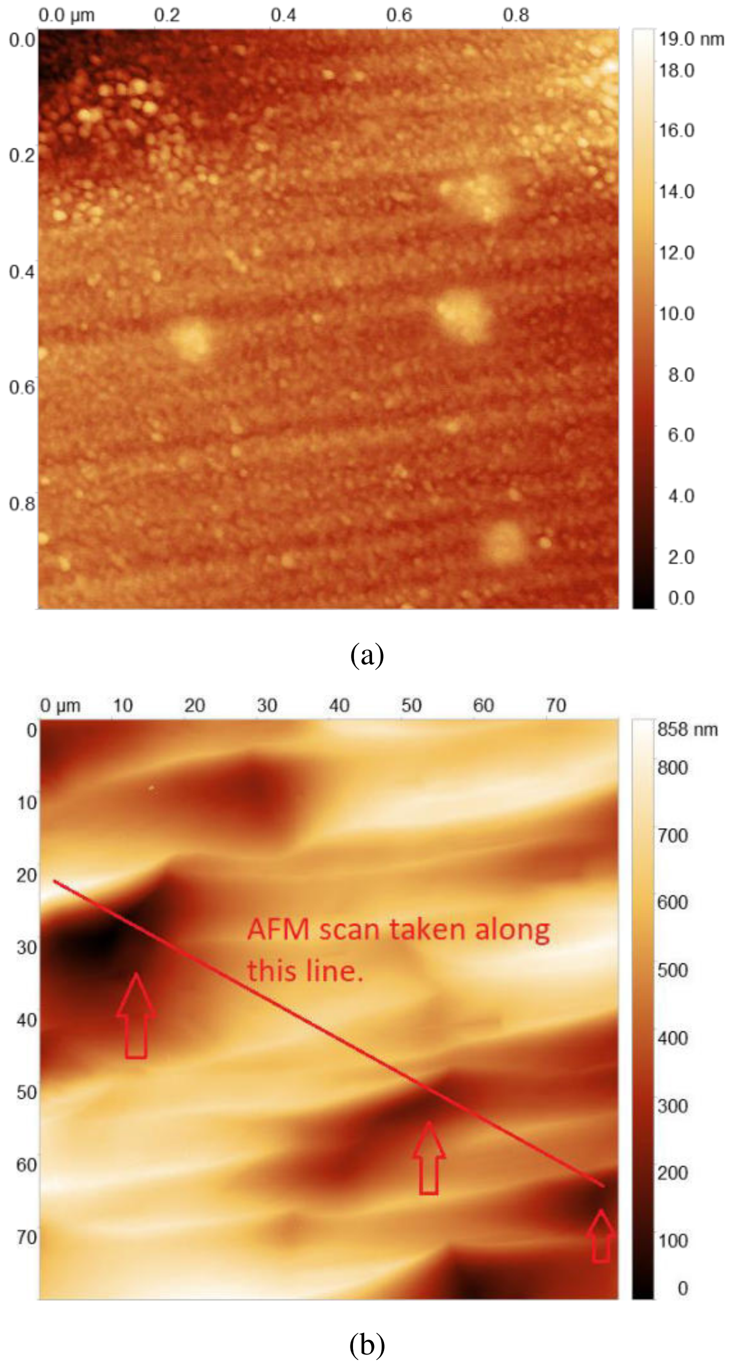
with nitrogen on a 1 x 10^{19} cm^{-3} highly N-doped substrate. Furthermore, 3C-on-Si material was provided by NOVASIC, which had an unintentionally doped (2 x10^{16} cm^{-3}) n-type 3C-SiC (100) 10 µm thick epitaxial layer which was grown on-axis on a 4-inch Si (100) substrate. MOS-devices, made with a thermal oxide have recently been reported, demonstrating the high quality of this material[15].

For roughness analysis, a Bruker Icon AFM was used in PeakForce Tapping mode to investigate the surface of the freestanding 3C-SiC material. The probe tip was made of Si on a nitride lever, with scan areas ranging from 1 µm x 1 µm to 80 µm x 80 µm. Extracted data were analysed using the Gwyddion software package. Here, the root-mean square (RMS) surface roughness is computed as square sum of absolute values of height data differences from the mean height over the entire scan area.

The crystal quality of two 3C-SiC wafers was analysed using XRD in a high resolution X-ray facility, consisting of two Panalytical X'Pert Pro MRDs, both equipped with a Cu Kα 1 hybrid monochromator as the incident beam optics and a receiving slit/analyser crystal in the diffracted beam optics.

6.3 SURFACE ROUGHNESS INVESTIGATION USING AFM

RMS roughness values for the freestanding 3C-samples increase exponentially with scan size from 1.62 nm (1 μm x 1 μm) in FIG. 6.1(a) to 163nm (80 μm x 80 μm) in FIG. 6.1(b), as FIG.6.2 (a) reveals. Whereas the RMS roughness value for the smallest size demonstrates a reasonable

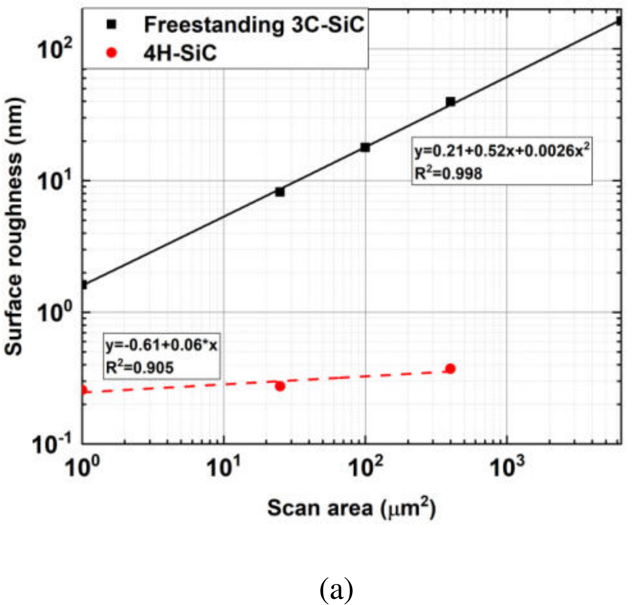


(a)

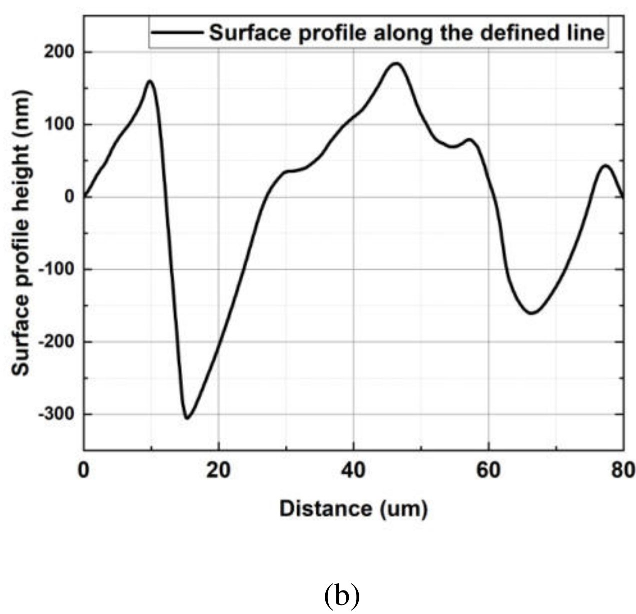
(b)

Figure 6.1: (a) Atomic force microscopy images of freestanding 3C-SiC samples with with 1μm x 1μm (a) and 80 μm x 80 μm (b) scan sizes.

range for device performance, the RMS values of bigger scan sizes will lead to a severe impact on key electrical parameters such as leakage current and reduce effective field mobility, hence increasing any specific on-resistance ($R_{SP,ON}$) values made from as-grown materials. The reason for the worsening of surface roughness can be seen in FIG.6.1 (b), where



(a)



(b)

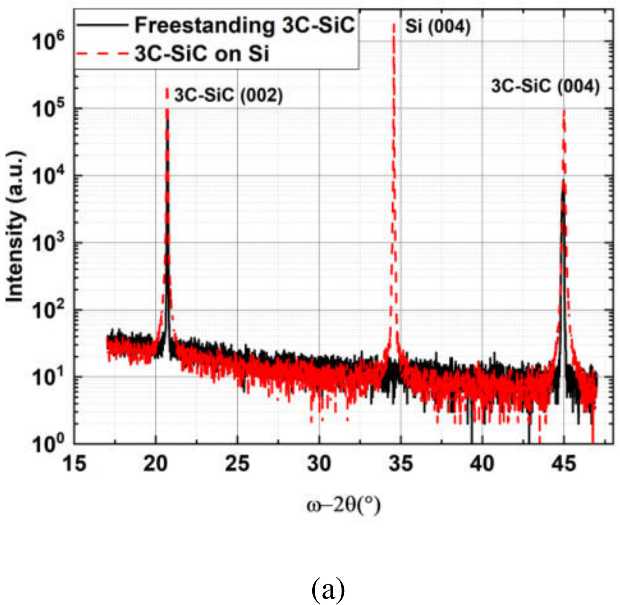
Figure 6.2: (a) Plot of surface roughness over scan area (c) with includes a 4H-SiC sample as well. The surface profile in image (b) was extracted the line in figure 6.1 (b), starting from the top left corner down to the bottom right corner.

the presence of large pits (35 μm width and and 100-450nm depth), with a density of 1.09 x 10^5 cm^{-2} is the cause of a sharp increase in surface roughness. The structural location of these pits resembles step bunching, a phenomenon widely reported for 4H-SiC with fewer reports for 3C-SiC[16]. They could also be phase boundary artifacts from protrusions during deposition of the initial 3C-SiC/seed. This can usually be reduced by process optimisation of the epitaxial growth or polishing. In comparison, the investigated 4H-SiC sample shows a smoother surface with no visible roughness and RMS values below 1 nm for all measured scan areas, revealing a significant difference in terms of surface quality when compared to the freestanding 3C-SiC sample.

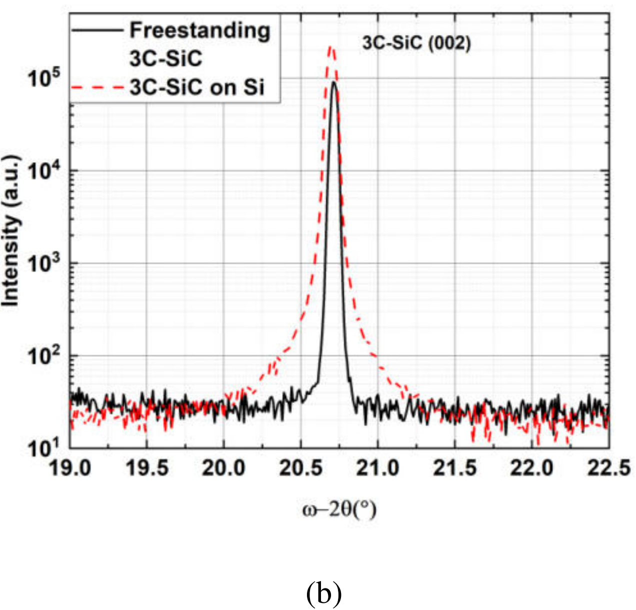
6.4 CRYSTAL QUALITY INVESTIGATION USING XRD

In FIG.6.3 (a), a ω-2θ curve is shown depicting a 3C-SiC (002) peak at 21°and a 3C-SiC (004) peak at 45° for both samples. A third Si (004) peak could be detected at 35° for the 3C-SiC on Si sample only.

Furthermore, the full width of half-maximum (FWHM) of the 3C-SiC (002) peak was extracted from the rocking curve in FIG.6.2 (b) for both samples. A high FWHM in the rocking curve of the 3C-SiC (002) peak has been shown [17] to be directly related to a high density of well-reported defects in 3C-SiC, such as stacking faults and micro-twins; a low



(a)



(b)

Figure 6.3: ω-2θ XRD scans (rocking curves) depicting (a) the full XRD spectrum and the (b) 3C-SiC (002) region for a freestanding 3C-SiC and a 3C-SiC on Si samples.

FWHM generally demonstrates a good average material quality [18]. The FWHM of the freestanding 3C-SiC is approximately 160 arcseconds lower than the FWHM of 210 arcseconds extracted for the 3C-SiC on Si sample. This is in good agreement with previous reports[14] and suggests promising material quality when compared to 3C-SiC on Si material.

6.5 ELECTRICAL RESULTS

For further investigations into the suitability of the previously described materials for device processing, electrical characteristics were extracted from MOS-devices. Oxides formed using ALD and thermal oxidation were considered. A FG post-deposition anneal (PDA) was carried out on ALD-deposited samples since this process has recently shown a big improvement in terms of electrical parameters and interface quality when compared to as-deposited ALD silicon dioxide and thermal oxide[19, 20].

All samples were cleaned with a solvent clean, followed by a HF(10%)/RCA1/HF(10%)/RCA2/HF(10%) process. SiO_2 was deposited on the ALD samples in an Ultratech Fiji G2 Plasma-Enhanced ALD system, with a substrate temperature of 200°C, bis(diethylamino)silane (BDEAS) as the Si precursor and O_2 plasma as a co-reagent. The deposited layer thickness was ≈ 30 nm (500 cycles). Again, 4H-SiC samples were used for benchmarking.

Following deposition, one set of samples (freestanding 3C-SiC, 3C-SiC on Si and 4H-SiC) was left as-deposited, and a second set of samples was loaded into a high-temperature anneal furnace, where they were annealed in forming gas (FG, 5% H_2 in 95% N_2) for 1 hr with a gas flow of 5 slm and a temperature of 1100 °C, as this process has been reported to improve the interface on 4H-SiC/SiO_2 MOSCAPs[19].

A third set of samples underwent thermal oxidation processes. The SiO_2 for the 4H-SiC samples were formed using a direct N_2O thermal

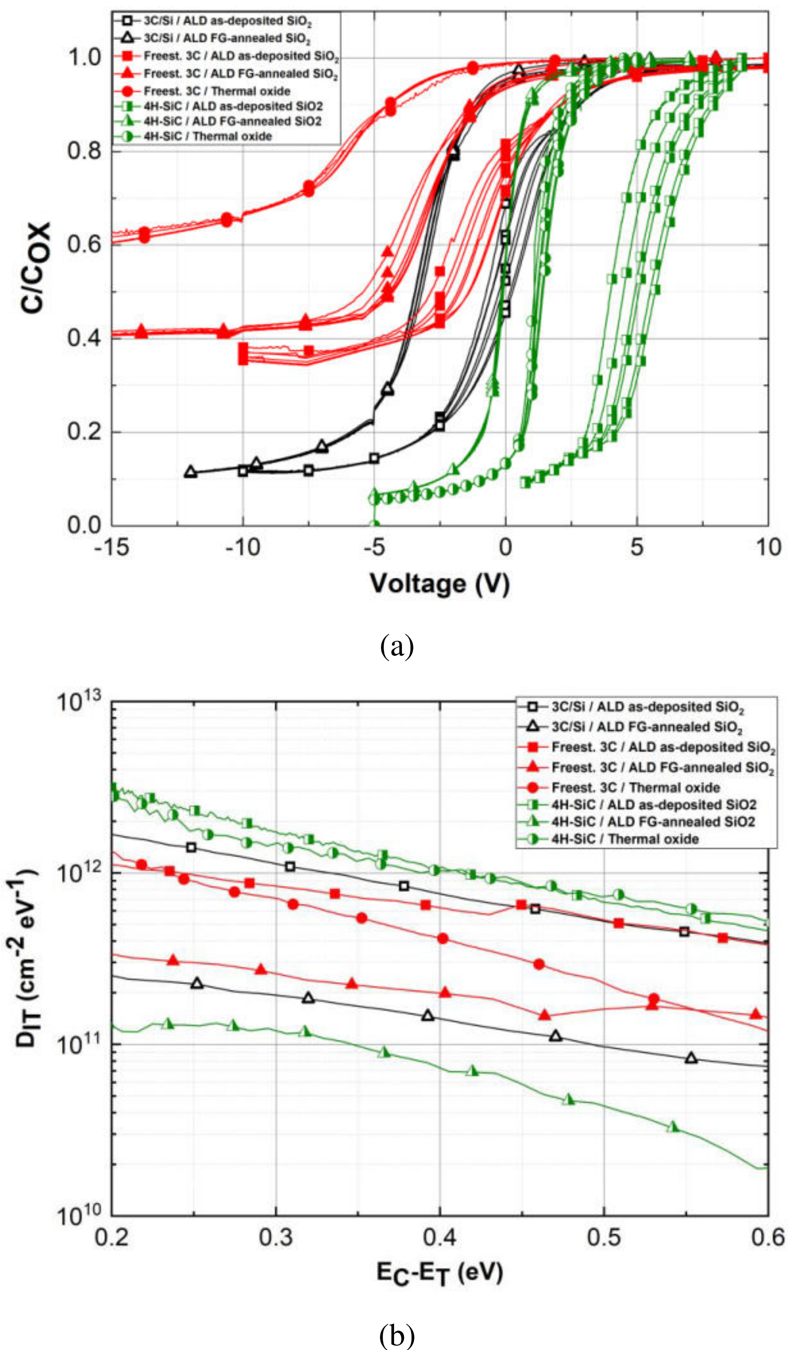
growth in a HiTech furnace at 1300 °C for 4 hours in an $Ar:N_2O$ (4 slm: 1 slm) ambient[21].

The freestanding 3C-SiC samples underwent a dry oxidation process in the same furnace at 1200°C for 10 minutes in an $Ar:O_2$ (4 slm: 1 slm) ambient followed by a post oxidation anneal at 1200 °C in an $Ar:N_2O$ (4 slm: 1 slm) ambient since this process has been proven to be highly reliable for 3C-on Si SiC MOSCAPs [15]. A dataset for thermal oxides on 3C-on Si was not included in this study but can be found in a study carried out by Li et al.[15]. Aluminium (Al) contacts were formed on top of the oxide layers using an Al wet etch and a 1 μm thick Al ohmic contact was deposited on the backside using electron beam evaporation. A process flow for the fabrication of the MOSCAPs can be found in Table 5.1.

Afterwards, room temperature vertical capacitance-voltage (C-V) measurements were recorded using an Agilent E4980A LCR meter and the D_{IT} was calculated using the high-low method (1 MHz and 1 kHz).

Key electric parameters such as flatband voltage (V_{FB}), hysteresis voltage and frequency dispersion in accumulation were then extracted and averaged from at least 16 devices per sample. Results are shown in TABLE 6.1 whereas characteristic C-V responses of the dataset are shown in FIG.6.4 (a) and their D_{IT} levels relative to the conduction band edge are represented in FIG.6.4 (b). For leakage current measurements, I-V measurements were carried out on the same MOSCAPs, with representative results being shown in FIG.6.5.

Generally, the as-deposited and FG-annealed devices which were fabricated on 3C-SiC on Si are very repeatable, with all electrical parameters having tight distributions. Here, flatband voltages and frequency dispersions of the as- deposited sample (3C-SiC on Si) show an



(a)

(b)

Figure 6.4: Normalised capacitance-voltage curves for each dataset (a) and the respective D_{IT} curves (b). The device area is 8.04 x 10^{-4} cm^2. For thermal and 4H-SiC oxides, the device area is 3.14 x 10^{-4} cm^2.

excellent performance, averaging 0.54 V and 0.07 % x dec^{-1}, respectively. This is already a significant improvement compared to reported 4H-SiC/ALD-deposited SiO_2 (as-deposited) interfaces utilising the same process, in which flatband voltages averaged at 8.63V and accumulation was not fully accomplished[20]. This suggests that positively charged

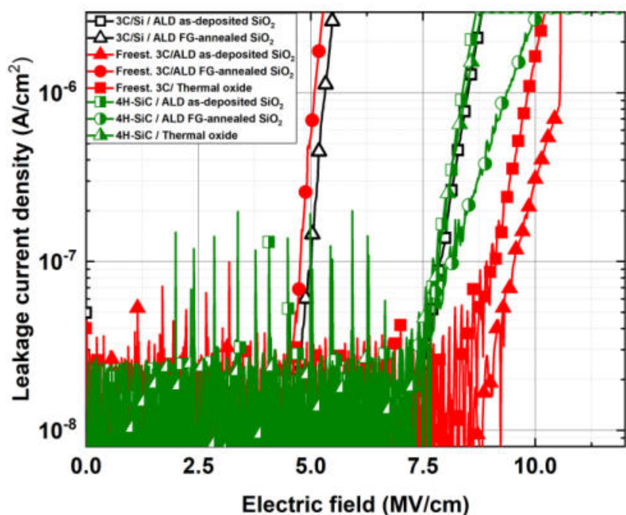


Figure 6.5: Leakage current measurements. The device area is 8.04 x 10^{-4} cm^2. For thermal and 4H-SiC oxides, the device area is 3.14 x 10^{-4} cm^2.

(donorlike) states near or at the 3C-SiC/SiO_2 interface[22] neutralised a significant quantity of negative charge, which is created during the ALD-deposition of SiO_2, leading to a low flatband voltage.

In comparison, the FG-anneal on 3C-SiC on Si samples reduced hysteresis voltage values, averaging 0.16 V, whilst shifting the C-V curve further away from the ideal response, with flatband voltages averaging -2.73 V. It also reduced the D_{IT} by roughly one order of magnitude to 2.8 x 10^{11} cm^{-2} eV^{-1} at E_C - E_T = 0.2 eV. As a side note, this is further confirmation that, on 3C-SiC on Si, MOSCAPs utilising deposited oxides can achieve similar D_{IT} levels as those using thermally grown oxides, as seen previously[15, 23]. The flatband voltage of thermal oxides on 4H-SiC averaged 0.61 V, with D_{IT} levels at 2 x 10^{12} cm^{-2} eV^{-1} at E_C - E_T = 0.2 eV. The best interface quality was shown in the FG-annealed 4H-SiC sample, with a D_{IT} levels at 1.5 x 10^{11} cm^{-2} eV^{-1} at E_C - E_T = 0.2 eV.

The most significant outcome of this investigation is the performance of both as-deposited and FG-annealed MOSCAPs on freestanding 3C-

Table 6.1: Summary of measured flatband voltage, hysteresis and frequency dispersion of 16 samples per category, with a device area of 8.04 x 10^{-4} cm^2. For thermal and 4H-SiC oxides, the device area was 3.14 x 10^{-4} cm^2.

Sample	**Flatband voltage (V)**	**Hysteresis voltage (V)**	**Frequency dispersion (% x dec^{-1})**
Freest. 3C-SiC as-dep.	-0.72 ± 1.14	1.49 ± 0.58	0.08 ± 0.05
Freest. 3C-SiC FG-anneal	-3.71 ± 0.42	2.26 ± 1.37	0.20 ± 0.09
Freest. 3C-SiC Thermal	-4.06 ± 0.23	0.15 ± 0.07	0.47 ± 0.40
3C-SiC/Si as-dep.	0.54 ± 0.13	1.02 ± 0.33	0.07 ± 0.04
3C-SiC/Si FG-anneal	-2.73 ± 0.18	0.16 ± 0.07	0.37 ± 1.14
4H-SiC as-dep.	8.39 ± 1.02	0.16 ± 0.13	2.58 ± 1.54
4H-SiC FG-anneal	-0.29 ± 0.13	0.10 ± 0.08	0.33 ± 0.29
4H-SiC Thermal	0.61 ± 0.12	0.15 ± 0.01	0.40 ± 0.19

SiC. The as-deposited samples show good flatband voltage and frequency dispersion distributions, averaging -0.72 V and 0.07 x dec^{-1}. D_{IT} levels of the devices are in the same range as for devices fabricated on 3C-SiC on Si, with a trap level of 2.8 x 10^{11} cm^{-2} eV^{-1} at E_C - E_T = 0.2 eV. Although the average hysteresis voltage value of 1.49 V indicates a high quantity of charge in the oxide and near the interface[24], this is a promising result which is confirmed by the excellent leakage current performance with samples reaching a current level of 1 x 10^{-9} A at an electric field higher than 10 MV/cm. The forming gas annealed samples on freestanding 3C-SiC follow a similar trend as for the 3C-SiC on Si dataset, with D_{IT} levels

being significantly reduced to 3.3 x 10^{11} cm^{-2} eV^{-1} at E_C - E_T = 0.2 eV, with trap levels being about an order of magnitude lower than for the thermal oxide on freestanding 3C-SiC. However, the hysteresis response is poor for the FG-annealed samples on freestanding 3C-SiC, averaging at 2.36 V, which warrants further investigation, though this is likely related to the presence of slow traps in the semiconductor due to the step bunching. Leakage levels reveal that the FG-annealed samples on both 3C-on-Si as well as well as the freestanding 3C-SiC suffer from a relatively poor leakage performance, with tunnelling beginning before an electric field of 5 MV/cm. The leakage current of the FG-annealed device on 4H-SiC shows lower leakage current levels (1 x 10^{-9} A at an electric field of about 10 MV/cm) than for the as-deposited and thermal oxides on 4H-SiC. This indicates that a high quality/chemical-mechanical polished surface might be able to lower the leakage current levels of the other two FG-annealed 3C-SiC samples.

6.6 CONCLUSION

In conclusion, a homo-epitaxial (freestanding) 3C-SiC growth process has been investigated in terms of its surface properties and crystalline quality and its suitability for device application has been established. AFM surface investigations show that the surface quality of the freestanding 3C material, without having undergone a polishing process, is promising at 163 nm RMS roughness for a scan size of 80 µm x 80 µm , but is not directly comparable to an optimised 4H-SiC homoepitaxy process on chemical-mechanical polished surface, measured at roughly 2 nm. It was shown this was caused by pits (35 µm width and 450 nm depth) with a density of 1.09 x 10^5 cm^{-2} which had formed during material growth. This undermined the generally good material uniformity seen at smaller scan sizes. XRD analysis revealed that freestanding 3C-SiC, with

a FWHM for the 3C-SiC (002) peak of 160 arcseconds, has a superior crystal quality with potentially lower densities than for 3C-on-Si material (210 arcseconds). C-V analysis then revealed similar trap levels for both 3C-SiC materials as well as 4H-SiC. The ALD deposited, FG annealed MOS capacitors on freestanding devices having a D_{IT} level of 3.3 x 10^{11} cm^{-2} eV^{-1} at E_C - E_T = 0.2 eV. Also, both the thermally oxidised and ALD as-deposited samples on freestanding 3C-SiC showed the lowest leakage current levels of the entire dataset, with both devices reaching still low leakage current levels of 1 x 10^{-9} A at electric fields above 10 MV/cm. Hence, the general competitiveness of homo-epitaxially grown 3C-SiC with 3C-on-Si as well as 4H-SiC material in terms of device quality was demonstrated, particularly given the scope for improving surface morphology and proving the suitability of the material thickness for wafer-scale processing.

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7 Conclusions and Future Work

7.1 INTRODUCTION

The work presented in this thesis spanned a number of investigations linked by their objectives to improve the interfaces made to wide bandgap semiconductor SiC. The investigations covered the Schottky interface, used in diode fabrication, and the MOS interface, as applied both to 4H-SiC and to 3C-SiC.

In this Chapter, the achievements of these investigations are summarised. It also contains suggestions for future research in the development of both surface passivation techniques on 4H-SiC SBDs and on the further development of ALD-deposited oxides.

7.2 SCHOTTKY DIODE CONCLUSIONS

A novel phosphorus pentoxide technique based on a deposition technique prior to metallisation was introduced and investigated on planar SBDs as well as fully optimised 3.3 kV JBS diodes.

On planar Mo/4H-SiC SBDs, the aforementioned treatment caused a reduction of leakage current by two orders of magnitude when compared to conventional, untreated devices. The ideality factor showed a slight improvement, too. The leakage is most likely improved because of the presence of oxide-filled nanopits near the surface which was witnessed in AFM, TEM and SEM images. These are seen to terminate leakage paths from imperfections at the SiC surface, homogenising the interface. At the same time, it is thought that the barrier is lowered due to a phosphorous-rich region below the contact, increasing the n-type doping and lowering

the SBH. It is believed that this effect is only possible in refractory metals such as Mo as almost no Mo-silicide forms.

In the next stage of the investigation, this process was applied to further refractory metals such as W and Nb. The reduction in leakage current was most significant in treated W/SiC diodes, which averaged four orders of magnitude lower than untreated tungsten devices. Although the effects on Mo could be repeated, the same process applied to W and Nb resulted in an increased SBH compared to untreated devices. XPS analysis of the interface revealed the presence of a metal-phosphorous-oxygen complex at the Schottky interface. It also revealed that the P_2O_5 appeared to have heavily n-type doped the Schottky subsurface, given an increase in the valence band to fermi level offset to 3.25 eV.

When fully optimised 3.3 kV JBS diodes were fabricated and characterised, the general functionality of the design and fabrication process was proven with breakdown voltages exceeding 3,500 V on all measured devices. The on-state of the JBS diodes was then characterised, where the same impact of the surface passivation treatment on barrier heights and ideality factors could be seen. Most significantly, off-state characterisation of the JBS diodes revealed a reduction in leakage current levels and the maximisation of the breakdown voltage in the P_2O_5-treated samples.

In summary, the P_2O_5 treatment can reduce off-state leakage substantially ensuring that a high breakdown voltage could be reached. This occurs via a combination of effects, namely manipulating the metal work function, doping the subsurface and terminating defects.

7.2.1 Schottky diode future work

For the phosphorous treatment used to produce low leakage SBDs, the deposition technique was carried out at 1000°C for 2 hrs, which was suggested by the source wafer supplier. In future work, both the deposition time and a post-deposition high-temperature anneal could be varied to investigate the effects of time and temperature on the phosphorous pentoxide-concentration at the interface. The analysis of post-deposition anneal temperatures will provide information on the electrical activation of phosphorous dopants at the interface. This would provide valuable information on whether the effects seen can be accentuated, and/or controlled such that the SBH and leakage can be fine-tuned to the needs of the application. In combination with SBDs to which these treatments are applied, a final picture of the impact of this treatment on the electrical performance could be delivered.

7.3 MOS INTERFACE CONCLUSIONS

Several post-deposition anneal studies on 4H-SiC MOSCAPs were carried out on ALD-deposited SiO_2. As a result, a high quality SiO_2/SiC interface was developed by carrying out a forming gas anneal for one hour at 1100°C after the ALD deposition. It was shown that this brought about vast improvements of the ALD layer in terms of flatband voltage, hysteresis, D_{IT} and positive mobile charge density. XPS-analysis revealed that a Si-rich interface could be found on these layers too, suggesting that the anneal breaks down Si complexes into Si dangling bonds, which could then be passivated.

In the last investigation, this process was then applied to a homo-epitaxially grown 3C-SiC epitaxial layer. The material was first investigated in terms of its surface properties and crystalline quality using

AFM and XRD. MOSCAPs were fabricated on this material and also on 4H-SiC MOSCAPs and 3C-on-Si MOSCAPs, and a similar level of traps on all the materials was seen. Both the thermally oxidised and ALD as-deposited samples on freestanding 3C-SiC showed the lowest leakage current levels of the entire dataset, exceeding electric fields of 10 MV/cm. This then showed the general competitiveness of homo-epitaxially grown 3C-SiC, particularly given the scope for improving surface morphology.

7.3.1 MOS Interface future work

To determine the full applicability of the developed gate oxides in MOSFET structures, later MOSFETs need to be fabricated and their channel mobility parameters extracted to validate this process even further. Also, the reliability of the deposited oxides needs to be compared to thermally grown oxides on 4H-SiC. A common technique to verify the reliability of the gate oxide is by carrying out time-dependent dielectric breakdown (TDDB) measurements, in which the devices are stressed at different voltages (constant voltage mode) or different current (constant current mode), to extract predictions on their lifetime in commercially packaged devices.

Appendix A MATLAB Code for barrier height and ideality factor extraction

A.1 AUTOMATIC DETERMINATION OF BARRIER HEIGHT

```
% Automated version of IVT_Differentiate.m if multiple files in the
% DataImport format can be specified.


clear all

ParameterSetup

load('\\doozer.ads.warwick.ac.uk\User64\u\u1691280\Desktop\Matlab\NoAl.mat'
)

Device = NoAl;

%%% Diode Area:
A=1;
areachoice = [0.000438898, 0.0014134553, 0.002836353667, 0.003963495];
%area = areachoice(A);
area = 1;

AA = 146;%112; %4HSiC Richardson's Constant (Same for 3C?)


NoVs = size(Device,1)-1; %"Size" tells you the size of the array
NoTs = size(Device,2)-1; %Hence NoVs means the number of voltages

%Create an array of voltages, currents and temps from the original data
    for j=1:NoVs
        VArray(j) = Device(j+1,1);
        for i=1:NoTs
            IArray(j,i) = Device(j+1,i+1);
        end
    end

    for i=1:NoTs
        TArray(i) = Device(1,i+1);
    end

    kTqArray=kb*TArray/q;

    Vint=VArray(2)-VArray(1); %Step size between voltages.

    % Isolate the useful data (i.e. ignore noise at low current and
    % resistance (V-IR) at high current
    IMin = 1e-7;
    IMax =1e-1;
    Vmin = 0.25;

    %Set the number of values that make up the differential calculations
```

```
    DiffWidth=25;

    OutputInSBH = zeros(NoVs,NoTs*3);
    Ioutput = zeros(NoVs,NoTs);
    nArray = zeros(NoVs,NoTs);
    SBH = zeros(NoVs,NoTs);
    VPrint = zeros(NoVs,NoTs);

    for i=1:NoTs %For every temperature
           nlow = 10000;
           SpecI = log(2e-8);
           SpecIComp = 10000;

        for j=0.5*(DiffWidth+1):(NoVs-(0.5*(DiffWidth-1))) %For every
voltage ignoring those that won't have the full diffwidth at the start and
end
            if VArray(j-(0.5*(DiffWidth-1)))>Vmin %Make sure V>VMin
                if IArray(j-(0.5*(DiffWidth-1)),i)>IMin %Make sure Imin< I
< Imax.
                    if IArray(j+(0.5*(DiffWidth-1)),i)<IMax
                        DiffTot=0;
                        for k=(j-(0.5*(DiffWidth-1))+1):(j+(0.5*(DiffWidth-
1)))
                            DiffTot = DiffTot + log(IArray(k,i)) -
log(IArray(k-1,i)); % Add all the delta Is
                        end
                        DiffArray(j,i) = DiffTot / (Vint*(DiffWidth-1));
%Divide these by the delta voltage

                        IS(j,i) = exp ( log(IArray(j,i)) - (DiffArray(j,i)
* VArray(j) ) ); %Extract IS at the x-axis


                        SBH(j,i) = - kTqArray(i) * log( IS(j,i) / (area *
AA * TArray(i) * TArray(i) ) );  %Convert IS into SBH


                        nArray(j,i)=1 /(kTqArray(i) * DiffArray(j,i) );
%Calculate Ideality via two methods (should be identical)
                        nArray2(j,i) = (VArray(j)) / ( kTqArray(i) * log(
(IArray(j,i) / IS(j,i)) + 1 ) );
                        Ioutput(j,i) = IArray(j+(0.5*(DiffWidth-1)),i);
                        VPrint(j,i)=VArray(j);



                        if abs(SpecI-log(IArray(j,i)))<SpecIComp
                            SpecIComp=abs(SpecI-log(IArray(j,i)));
                            Spec_n(i) = nArray(j,i); %Find the values ata
specific current

                            Spec_SBH(i) = SBH(j,i);
                            Spec_I0(i) = IS(j,i);
                        end

                        if nArray(j,i)> 10
                            nArray(j,i)=0;
                            Ioutput(j,i)=0;
                            VPrint(j,i)=0;
                        end
```

```
                        if nArray(j,i)< 1
                            nArray(j,i)=0;
                            Ioutput(j,i)=0;
                            VPrint(j,i)=0;
                        end



                        if nArray(j,i)<nlow
                            if nArray(j,i)>0.5
                            nlow = nArray(j,i); %Find the lowest ideality
for each Temp.
                            lowj = j;
                            VPrint(j,i)=0;
                            end
                        end


                    else
                        DiffArray(j,i)=0; %Reset the differential array
                    end
                else
                    DiffArray(j,i)=0;
                end
            else
                DiffArray(j,i)=0;
            end
        end

        Nons(i) = nnz(nArray(:,i));
        NoSBHs(i) = nnz(SBH(:,i));

        nAve(i) = sum(nArray(:,i))/Nons(i);
        SBHAve(i) = sum(SBH(:,i))/NoSBHs(i);
        nLowest(i) = nlow;
        SBHLowestn(i) = SBH(lowj,i);
        ISLowestn(i) = IS(lowj,i);
        JSLowestn(i) = IS(lowj,i)/area;

        OutputInSBH(:,i*4-3)=VPrint(:,i);
        OutputInSBH(:,i*4-2)=Ioutput(:,i);
        OutputInSBH(:,i*4-1)=nArray(:,i);
        OutputInSBH(:,i*4)=SBH(:,i);
%          OutputTemp(1,i*3-2)=TArray(i);
%          OutputTemp(1,i*3-1)=TArray(i);
%          OutputTemp(1,i*3)=TArray(i);
    end

    %OutputInSBH(~OutputInSBH)=nan;
    %nArray(~nArray)=nan;
    SBH(~SBH)=nan;
```

A.2 PARAMETER SETUP

```
%Constants
%clear
q=1.602176487E-19; % Charge Electron
kb=1.3806503E-23;  %Boltzmanns Constant
T=300;
kTq=kb*T/q;          %Thermal Energy
Beta = 1/kTq;        %Inverse Thermal Energy
e0=8.854e-14;        %Permittivity of Free Space
m0=9.1095e-31;       %Mass of Electron
h=6.626068e-27;      %Planck's Constant
hbar=h/(2*pi);       %Reduced Planck's Constant
h2=4.1357e-15;
hbar2=h2/(2*pi);

    %1 = Germanium
Ks(1) = 16.2;
Eg(1) = 0.661;
NC(1) = 1.98e15 * T^1.5;
NV(1) = 9.60e14 * T^1.5;
ND(1) = 5e14;
me(1) = 0.22*m0;

    %2 = SiC
Ks(2) = 10;          %Dielectrioc Constant
Eg(2) = 3.26;        %Bandgap
NC(2) = 3.25e15 * T^1.5;    % Density of states in the Conduction Band
NV(2) = 1.73e15 * T^1.5;    % Density of states in the Valence Band
ND(2) = 1.4E+15;            % Doping
me(2) = 0.37*m0;

    %3 = Si
Ks(3) = 11.9;
Eg(3) = 1.12;
NC(3) = 6.2e15 * T^1.5;
NV(3) = 3.5e15 * T^1.5;
ND(3) = 5e18;
me(3) = 0.36*m0;



%ND = logspace(16, 20, 17);

%HfO2
%x0   = 4e-6;
%KO   = 25;
%Area = 0.00453;
%C0   = KO*e0*Area/x0;
%C0   = 1.58e-9;

%SiO2
x0   = 5e-7;
KO   = 3.9;
Area = 0.000447938;
C0   = KO*e0*Area/x0;
mOx=0.41*m0;
```

```
es = e0*Ks;

for i=1:3 %Data for another programme...
    ni(i)    = sqrt(NC(i)*NV(i))*exp(-Eg(i)/(2*kTq));
    Ld(i)    = sqrt(Ks(i)*e0*kb*T/(2*q*q*ni(i)));
    PhiF(i)  = -kTq*log(ND(i)/ni(i));
    UF(i)    = PhiF(i)/kTq;
    PhiN(i)  = -kTq*log(NC(i)/ND(i));
    PhiNdegen(i) = kTq* ( log(ND(i)/NC(i)) + (ND(i)/NC(i))/sqrt(8) - (3/16
-sqrt(3)/9)*(ND(i)/NC(i))*(ND(i)/NC(i)) );
end
```