

## Investigations of Short Circuit Robustness of SiC IGBTs with Considerations on Physics Properties and Design

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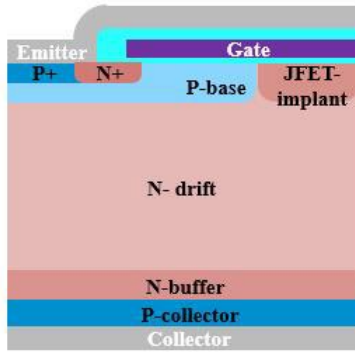
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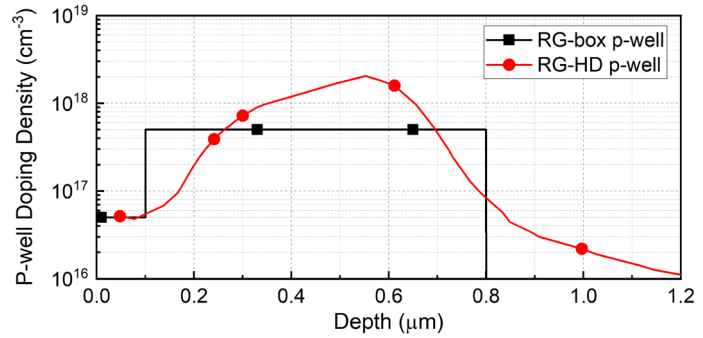
**Abstract.** The commercial success of silicon carbide (SiC) diodes and MOSFETs for the automotive industry has led many in the field to begin developing ultra-high voltage (UHV) SiC insulated gate bipolar transistors (IGBTs), rated from 6 kV to 30 kV, for future grid conversion applications. Despite this early interest, there has been little work conducted on the optimal layout for the SiC IGBT, most early work seeking to overcome difficulties in fabricating the devices without a P+ substrate. In this paper, numerical TCAD simulations are used to examine the link between the carrier lifetime of SiC IGBTs and their short circuit capability. For the planar devices, simulations show that increasing carrier lifetime from 1 to 10  $\mu$ s, has not only a profound effect reducing on-state losses, but also increases short circuit withstand time (SCWT) by 39%. Two retrograde p-well designs are also investigated, the optimal device for SCWT having a 100 nm channel region of  $5 \times 10^{16} \text{ cm}^{-3}$ , with this increasing to a peak value of  $2 \times 10^{18} \text{ cm}^{-3}$ , in a 700 nm region beneath the channel.

### Introduction

The electrical and thermal properties of silicon carbide (SiC) have made it an excellent candidate for high power applications. Ultra-high voltages (UHV) 4H-SiC devices rated at 10 kV and above are an attractive choice for HVDC converters, as to reduce the number of devices required in, for example, voltage-source converters [1, 2]. Despite the optimization to gain better on-state performance and lower switching losses, the short circuit robustness of SiC IGBTs needs improving. The impact of a number of the state-of-the-art IGBT developments to date are explored in a series of benchmarking simulations.



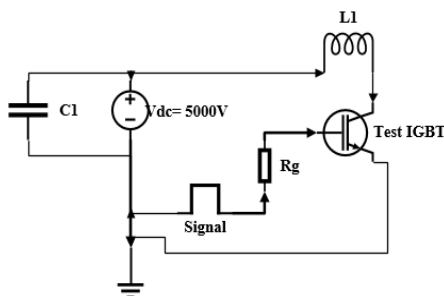
**Fig. 1** Planar SiC n-IGBT structure.



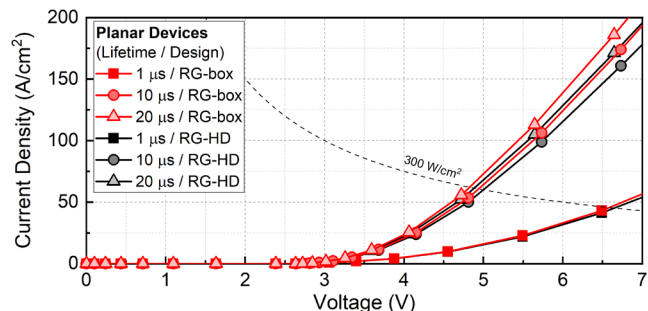
**Fig. 2** The p-well doping concentration of the retrograde planar devices, the RG-HD design coming from process simulation.

To begin, baseline 10 kV planar IGBT geometry has been implemented in the Sentaurus TCAD platform, its layout depicted in Fig.1. The baseline models are then adapted, with the p-well design and the impact of the lifetime  $\tau_n$ . For the baseline models, the anode side of the structure is a field-stop design with a 3  $\mu\text{m}$ ,  $1 \times 10^{19} \text{ cm}^{-3}$  p+ collector and a 1  $\mu\text{m}$ ,  $1 \times 10^{17} \text{ cm}^{-3}$  N-buffer. The cathode side employs a planar gate structure with an n-doped enhancement region. Due to the inherent poor SiC channel mobility, appropriate interface models are necessary and a realistic SiC/SiO<sub>2</sub> trap profile with increasing trap concentrations at the edges is employed [3]. This strongly affects the channel mobility due to scattering mechanisms at the interface (i.e., acoustic, surface roughness, coulomb scattering [4]). Retrograde p-well is historically proposed for the high-density Si-based CMOS technology with later studies reporting an improvement in the latching performance compared conventional p-well design [6]. Two retrograde (RG) p-well designs are compared, their doping profiles shown in Fig. 5. They both have a 0.1  $\mu\text{m}$  deep,  $5 \times 10^{16} \text{ cm}^{-3}$  channel region. Beneath this, the “RG-box” variant features a 0.7  $\mu\text{m}$ ,  $5 \times 10^{17} \text{ cm}^{-3}$  uniform box-profile doping. The second “RG-HD” variant features a higher doping, peaking at  $2 \times 10^{18} \text{ cm}^{-3}$ , which has been designed in the process simulator and verified experimentally. Both implementations are simulated with  $\tau_n$  set to 1  $\mu\text{s}$ , 10  $\mu\text{s}$  and 20  $\mu\text{s}$ .

Following analysis of the static characteristics, the short circuit robustness of the variants is investigated via a short-circuit switching simulation. In order to obtain informative results, the p-base current is isolated from the emitter current at the cathode side of the device by adding an additional separate base contact to monitor the current flow at the top of the device. Fig. 3 shows the short circuit test circuit, in which a 5000 V DC pulse is applied to the IGBTs’ collector for increasing duration until the device breaks down (via parasitic n+/p-base turn-on and eventual thermal runaway). The parasitic inductance (L1) for the test setup is 180 nH.



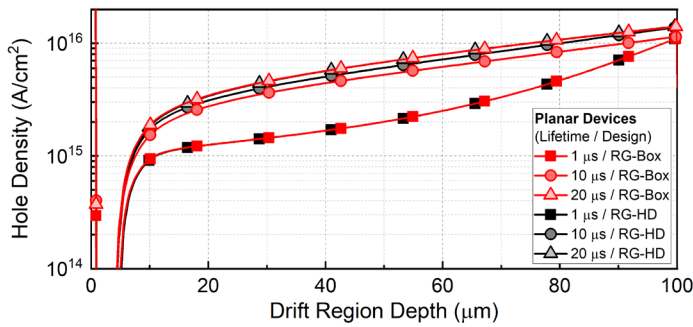
**Fig. 3** Short circuit test circuit for the 10 kV IGBT.



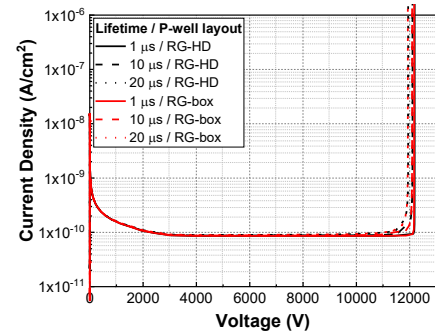
**Fig. 4** Simulated ON-state characteristics of the planar IGBTs at room temperature, with different lifetimes and p-well designs.

## Static Results

The forward conducting characteristics of the planar IGBT designs, are shown in Fig. 4; Fig. 5 shows their excess carrier density in the drift region at 100 A/cm<sup>2</sup>. As demonstrated experimentally [5, 6, 7], the on-state losses are heavily affected by the underlying carrier lifetime and the distribution of the charge. At  $\tau_n=10 \mu\text{s}$  the carrier density of the 100  $\mu\text{m}$  drift layer with a RG-box p-well approaches relative saturation. An  $R_{\text{ON,SP,DIFF}}$  of 12.2 m $\Omega\cdot\text{cm}^2$  is recorded, the  $V_{\text{ON}}$  is 5.6 V at 100 A/cm<sup>2</sup>, and the  $J_{\text{ON}}$  is 60 A/cm<sup>2</sup> at 300 W/cm<sup>2</sup>. The on-state characteristics are largely unaffected by the different retrograde p-well designs.



**Fig.5** Plasma distributions along the drift region at 100 A/cm<sup>2</sup>.

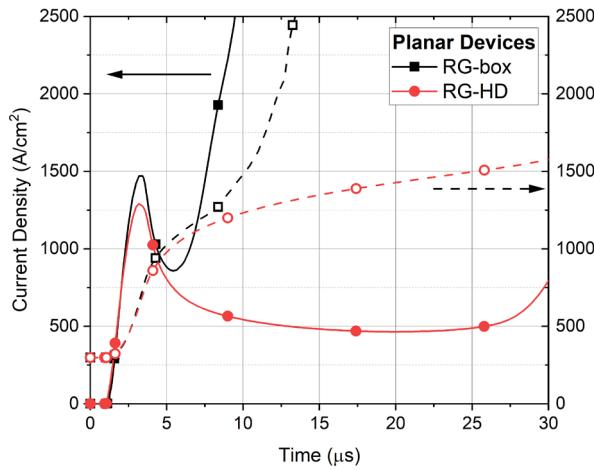


**Fig.6** Simulated OFF-state characteristics of the planar IGBTs at room temperature, with different lifetimes and p-well designs.

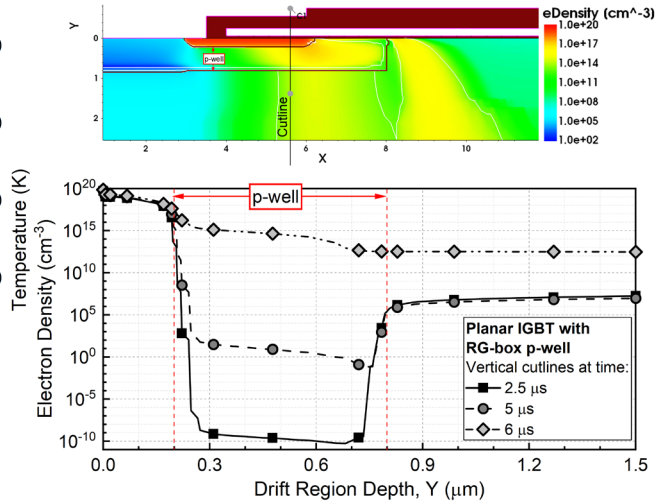
## Short circuit Robustness

### 1) Planar IGBT: Effect of p-well design

Short circuit switching simulations demonstrated the advantage of the RG-HD p-well design in withstanding a short circuit fault condition. Fig. 7 shows the transient characteristic under short-circuit conditions with the gate pulse left on until latch up and destruction. This occurred after 6  $\mu\text{s}$  for the RG-box p-well device whereas the optimised device lasted for over 25  $\mu\text{s}$ . The reason for this improvement in the RG-HD p-well design is due to its higher doping (Fig. 2) beneath the channel, which provides a low resistance path for hole current to the emitter. Fig. 8 shows the electron current density of the RG-box structure during this period. As minority carriers, in the p-well, the electron density is seen to exceed  $5 \times 10^{14} \text{ cm}^{-3}$  at  $t_{\text{SC}} = 6 \mu\text{s}$ , suggesting that the n+/p-base junction is forward biased and thus triggering the junction failure, with the device eventually failing due to thermal runaway.



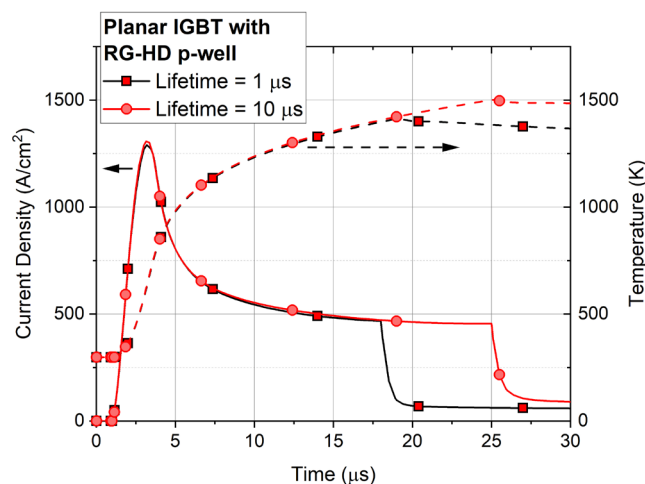
**Fig.7** Simulated Short circuit curves for both retrograde planar devices with  $\tau_{max,n}=1 \mu s$ .



**Fig.8** Top, the electron density of a planar RG-box p-well device at  $t_{sc} = 6 \mu s$ . The bottom plot shows the electron density at different time intervals  $t_{sc} = 2.5, 5$  and  $6 \mu s$  along the vertical cutline shown.

2) Planar IGBT: Effect of carrier lifetime

For the SiC IGBTs, like SiC MOSFETs [8,9], SRH generation is responsible for an increase in leakage current. Reducing carrier lifetime enhances the SRH generation in the depletion region of the p-base/n-drift junction, and the holes generated flow through the p-base/n-drift junction, leading to an increase in base leakage current. For the RG-HD p-well structure the lifetime effect is significant. From Fig. 9, an increase in  $\tau_n$  from  $1 \mu s$  to  $10 \mu s$  brought about an increase in the SCWT of 39% from  $18 \mu s$  to  $25 \mu s$ . This underlines that a lifetime enhancement procedure (e.g. via surface oxidation [10]) would benefit both ON-state performance and short-circuit capability. Similar to the concept of current saturation, the SRH generation rate reaches a minimum by  $\tau_n=10 \mu s$ , and no further improvement in the SCWT occurs above this value.



**Fig.9** Short circuit (last pass) curves for the RG-HD p-well IGBT device, with (a)  $\tau_{max,n}=1 \mu s$  and (b)  $\tau_{max,n}=10 \mu s$ .

## Summary

The static performance and short circuit robustness of 10 kV SiC IGBTs was investigated. The planar structure is with much improved short circuit robustness, in a similar fashion to silicon devices. However, in contrast to silicon bipolar devices, SiC IGBTs static and dynamic performance does benefit from lifetime enhancement. A highly doped retrograde p-well doping profile is necessary in order to improve on-state and short circuit robustness.

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