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FEM-based analysis of avalanche ruggedness of high voltage SiC Merged-PiN-Schottky and Junction-Barrier-Schottky diodes

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ABSTRACT

Through comprehensive experimental measurements and TCAD simulation, it is shown that the avalanche ruggedness of SiC MPS & JBS diodes outperforms that of closely rated Silicon PiN diodes taking advantage of the wide-bandgap properties of SiC which leads to a high ionization and activation energy given the strong covalent bonds. Although the MPS diode structure favours a high reverse blocking voltage with small leakage current and a high current conduction, the localise current crowding caused by the multiple P^+ implanted region leads to the avalanche breakdown at lower load currents than the SiC JBS diode. The results of Silvaco TCAD Finite Element modellings have a good agreement with the experimental measurements, indicating that SiC JBS diode can withstand the high junction temperature induced by avalanche in line with the calculated avalanche energy.

1. Introduction

Merged-PiN-Schottky (MPS) are bipolar SiC devices [1,2] that can be used for high frequency and medium voltage applications, for instance as output diodes in Power Factor Correction (PFC) circuit and as clamping diode in high voltage DC transmission. Clamping diodes can experience high voltages that they may lead to avalanche conduction and potentially failure, while undetected failures in grid-connected PFC circuits [3] may lead to overcurrent surges. Electrothermal ruggedness and avalanche ruggedness of SiC MPS diodes have been assessed [4–7] under Unclamped Inductive Switching (UIS) test, but with lack of comparison with other similarly rated power rectifiers. The intention of this work is to investigate the avalanche ruggedness of commercially available 4H- SiC MPS diodes through UIS tests in comparison with similarly rated Silicon PiN and SiC Junction Barrier Schottky (JBS) diode in Table 1 as in Fig. 1. Extensive experiments and Silvaco TCAD modelling are carried out to investigate the performance by UIS stressing, verifying the models by good matching.

2. UIS test measurements

The single event avalanche ruggedness of Silicon PiN, SiC JBS and SiC MPS diodes have been investigated through a wide range of UIS measurements. Table 1 includes the key parameters of the three diodes under test. All devices are fabricated in standard TO-220 packages. The UIS testing board is shown in Fig. 2 with a common, high voltage Silicon IGBT (IXBX55N300) acting as the power switch. The initial temperature of diodes before each UIS event is controlled from 25 °C to 175 °C via a temperature controller. A load inductor of 1.25 mH is charged to the peak avalanche current that is proportional to the length of the gate pulse (L_P), with pulse length of 80 μs & 160 μs, and proportional to the DC link voltage (V_{DC}) increased from 90 V to 360 V. When the IGBT switches off, the current flowing through the inductor starts to decrease while a counter Electromagnetic Force (EMF) will be induced to resist the abrupt change. The diode voltage rises to the breakdown voltage [7,8], triggering the avalanche current to flow through the diode. Unlike the power diodes which will suffer high electrothermal stress, the IGBT will stay in the safe region due to its much higher voltage/current ratings (3 kV & 55 A at 110 °C). The load current is initially set to a low value to ensure an initial avalanche energy lower than their failure limit. The pulse length and DC-link voltage are then gradually increased to apply more electrothermal stress on the device under test (DUT) until failure.

Figs. 3 and 4 show the UIS waveforms for diodes with different technologies with load current increased until device failure is achieved. Before the failure occurs, the avalanche duration increases with increase

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Table 1
Features of silicon PiN, 4H-SiC JBS & MPS diode.

	Silicon PiN	SiC JBS	SiC MPS
Model	DSI30-12A	C4D20120A	GC20MPS12220
Made	IXYS	CREE	GeneSiC
Voltage	1200 V	1200 V	1200 V
Current	30A at 130 °C	26A at 135 °C	30A at 135 °C
Leakage	40 μA	200 μA	10 μA

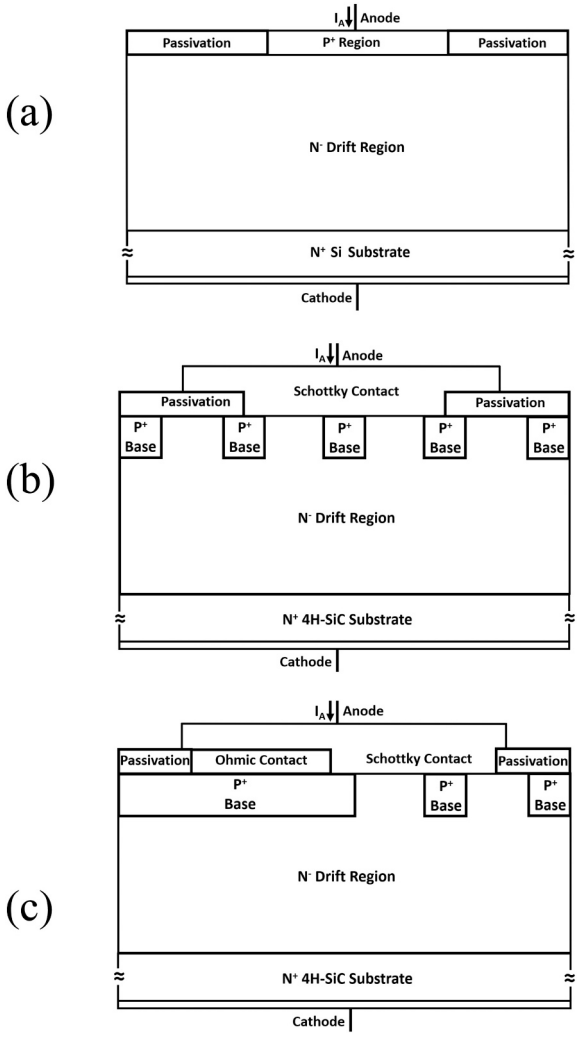

Fig. 1. Cross-sectional schematic of (a) Silicon PiN diode, (b) 4H-SiC JBS diode [8] and (c) 4H-SiC MPS diode [9].

of load current. It can also be seen in Fig. 4 that the higher effective breakdown voltage of Silicon PiN leads to the much lower diode current when failure occurs compared to that of the SiC devices even though all devices are rated at 1.2 kV. When the device failure is initiated, the diode fully conducts in the reverse conduction with increasing current levels exceeding the pre-set load current levels because of the avalanche multiplication effect together with the thermal runaway effect while the diode voltage immediately drops to zero as the blocking capability is lost. Silicon PiN diode failed at lower load current compared with the SiC JBS & SiC MPS while its recovery process, as in Fig. 4, has been skipped as the device cannot handle such high induced avalanche current. This is due to the excessively high induced voltage by the inductor. Figs. 5 and 6 emphasize the difference in avalanche ruggedness among the three different diodes at failure. It is seen that the SiC devices can sustain the avalanche conduction for a longer time than the Silicon

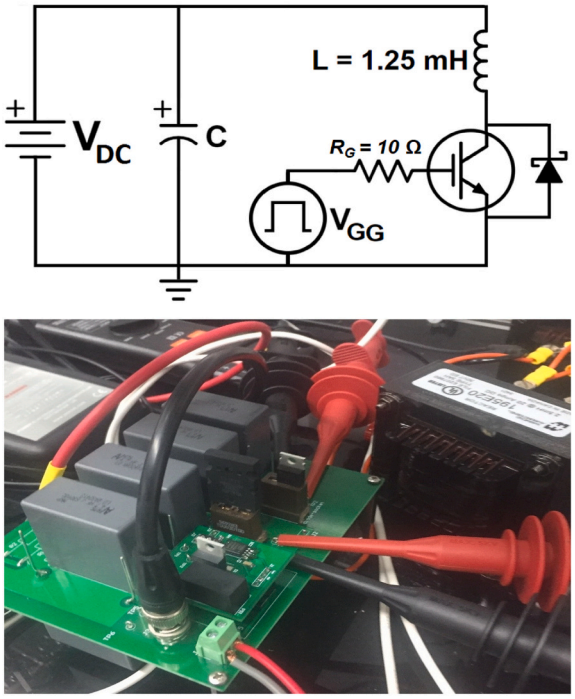

Fig. 2. The UIS test circuit schematic and the test board.

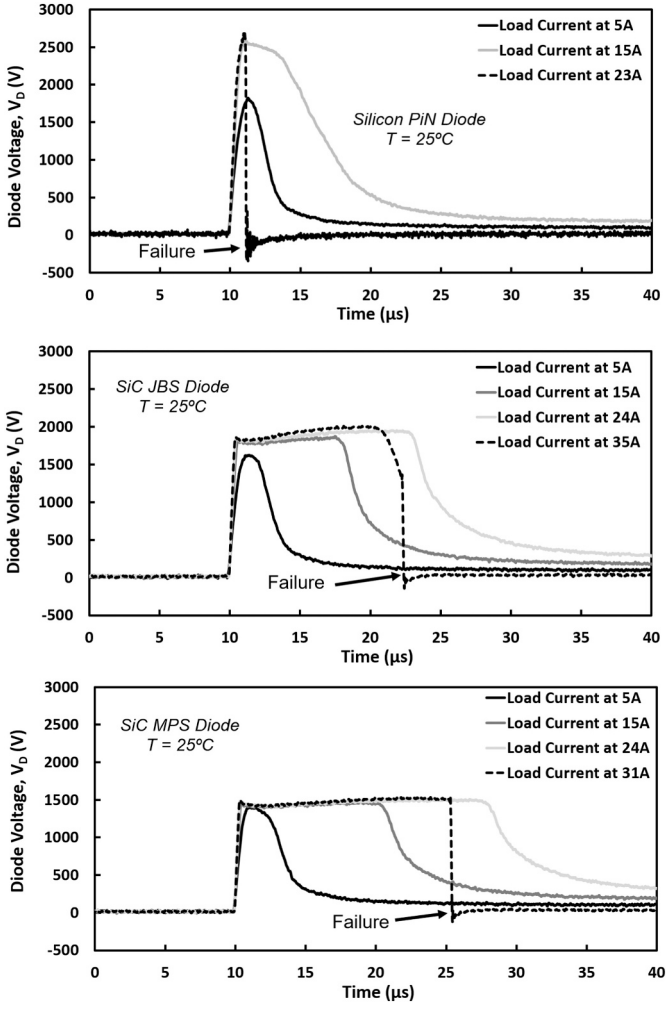

Fig. 3. UIS diode voltage at different Load currents for Silicon PiN, SiC JBS and SiC MPS diodes.

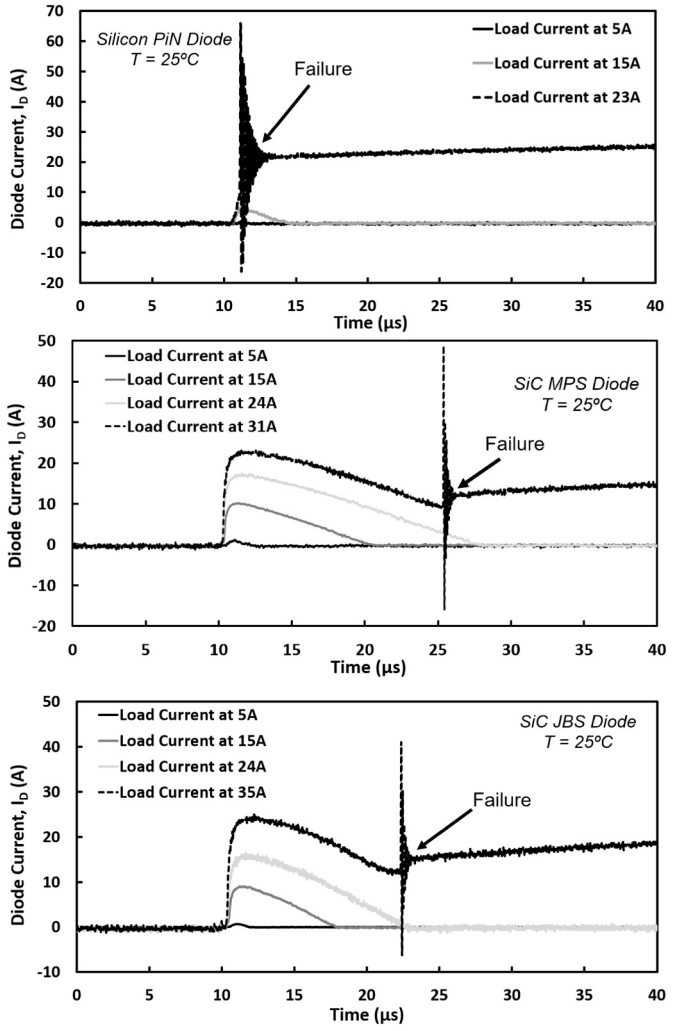

Fig. 4. UIS diode Current at different Load currents for Silicon PiN, SiC JBS and SiC MPS diodes.

device before the avalanche multiplication is triggered. At high temperatures, all devices are found to fail at lower currents with shorter recovery period. This can be explained by the fact that there is less headroom to dissipate power during the recovery process when the temperature is increased. The key failure mechanism in the Silicon PiN diode is non-reversible high voltage breakdown of the P—N junction between the N-drift and P-Anode. The failure mechanism in the SiC MPS is dominated by heat generation by UIS, while in the SiC JBS, it is a combination of heat and electric field.

The avalanche energy is an important parameter since the avalanche breakdown mechanism of power rectifiers takes place by increased dissipated energy at the junction of device, leading to temperature increase that destroys the metallizations of the device [6–8]. Figs. 5 and 6 provide a comparative illustration of the failure limit of the three devices under UIS at 25 °C and 175 °C, respectively. The critical avalanche energy is determined as the maximum value before failure during the single pulse UIS tests which is shown in Fig. 7 together with UIS energy density per die area, comparing the avalanche energy between different devices. It can be seen that the SiC JBS diode has the highest critical avalanche energy and the critical avalanche current, closely followed by the SiC MPS diode with significant at distance to Silicon PiN diode in all temperatures. The critical energy for all devices decreases as temperature rises as it is more difficult to dissipate the generated heat by UIS [10].

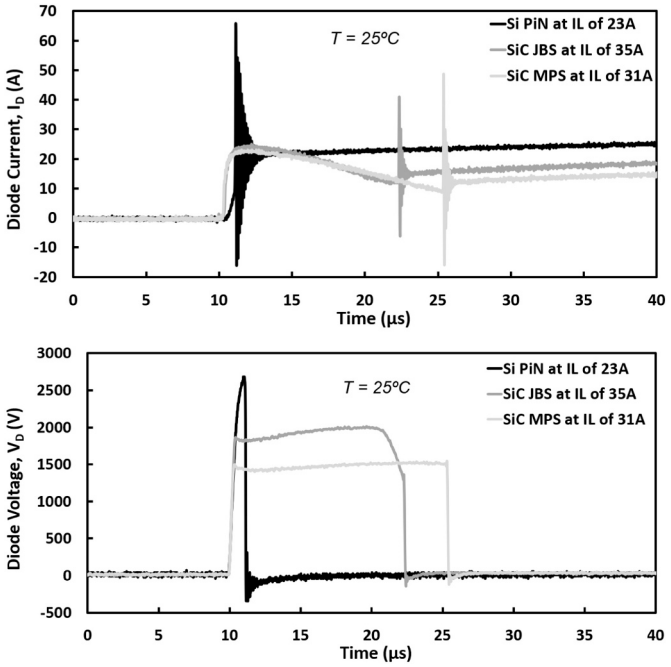

Fig. 5. The diode current and diode voltage of Silicon PiN, SiC JBS and SiC MPS diode when failure occurs at 25 °C.

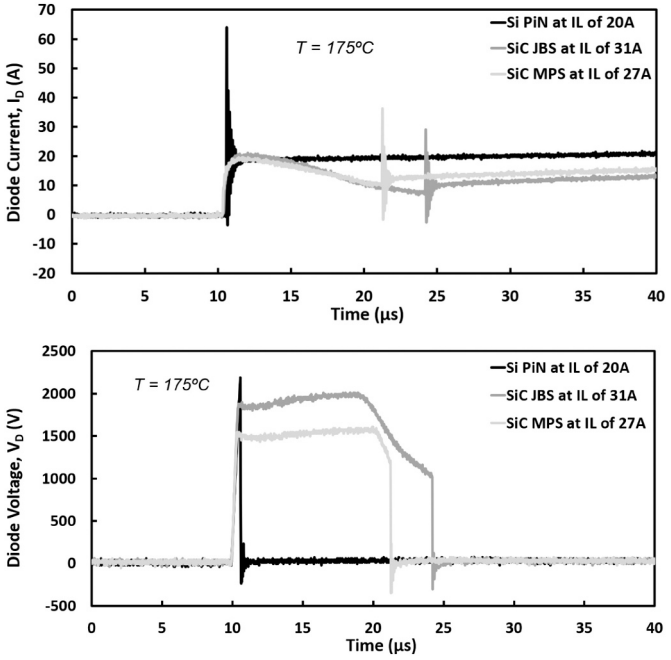

Fig. 6. The diode current and diode voltage of Silicon PiN, SiC JBS and SiC MPS diode when failure occurs at 175 °C.

3. TCAD simulation validation

Silvaco TCAD finite element models have been developed to further study the failure mechanisms of all three devices. The device structures shown in Fig. 1 are modelled in TCAD as shown in Figs. 8 to 10 together with the UIS waveforms at the point just before failure in all 3 devices. The avalanche voltage is shown to be almost flat during breakdown, inline with measurements seen in Fig. 3, while the load current and diode current are also plotted. TCAD simulations show that junction temperature is at peak at the end of the current fall, overlapped with voltage,

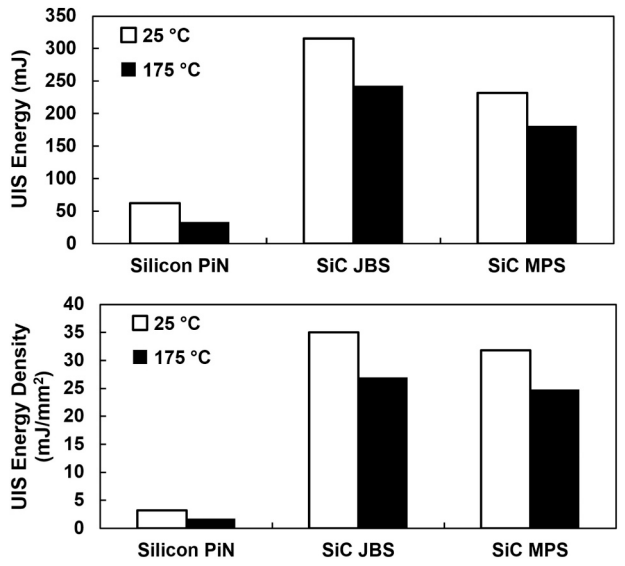

Fig. 7. Comparison of critical avalanche energy for Silicon PiN, SiC JBS & SiC MPS diode at different temperatures.

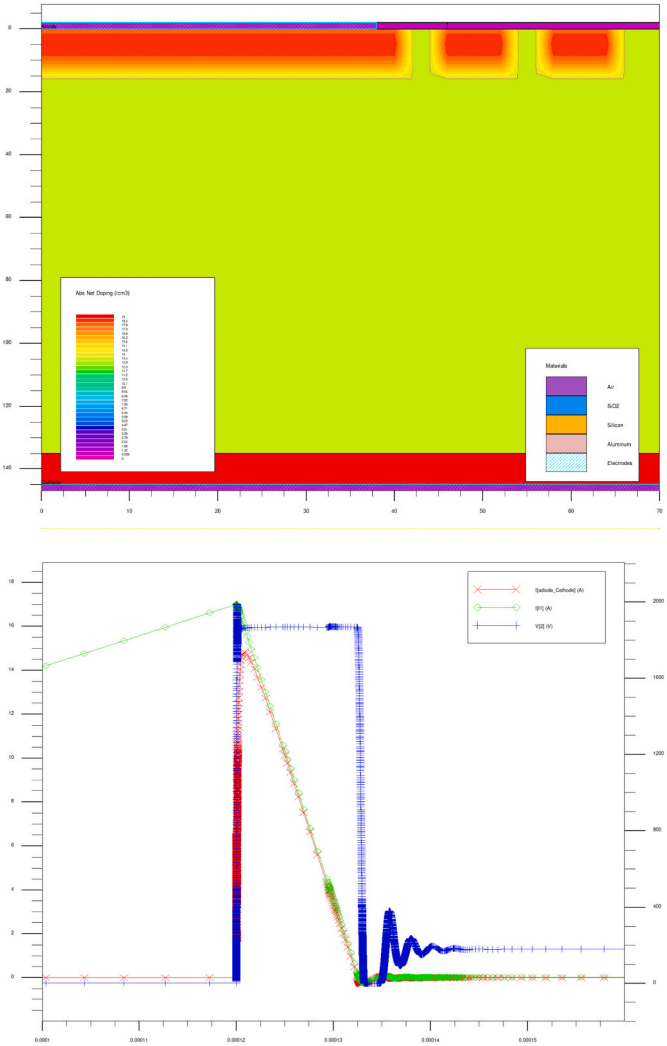

Fig. 8. Structure of the Silicon PiN diode in TCAD along with the current and voltage waveforms under UIS stress.

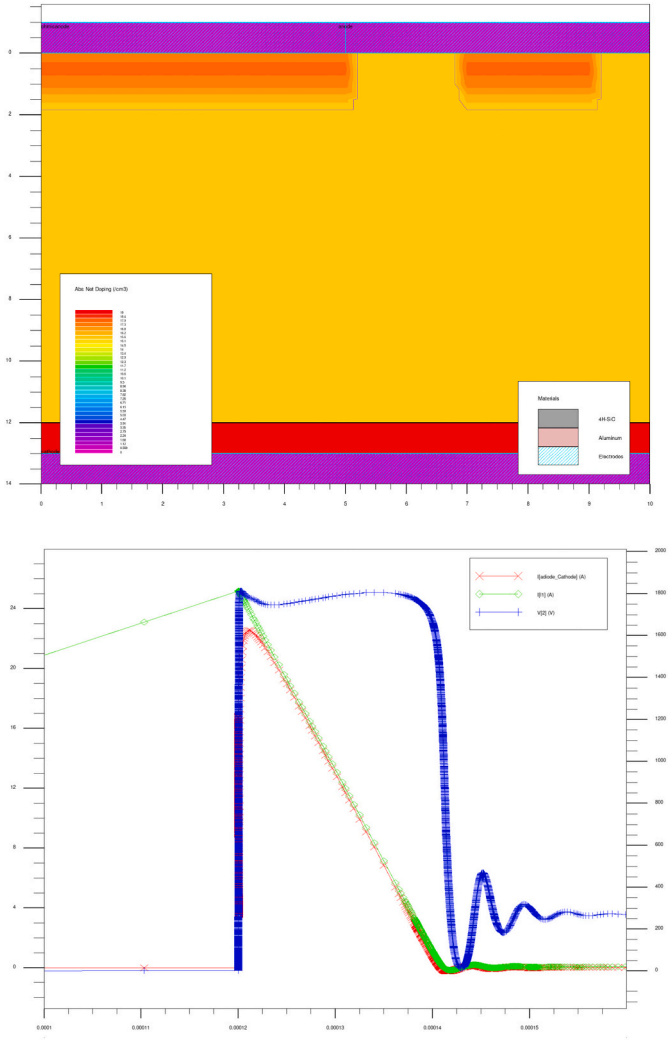

Fig. 9. Structure of the 4H-SiC MPS diode in TCAD and the current and voltage waveforms under UIS stress.

leading to maximum heat generation in just a few µs.

To enable analyzing the avalanche energy density of the devices, and to ensure that the Silvaco TCAD models developed are representative of the actual device, the failed devices have been CT-Scanned using a Nikon® XT H 225 ST CT-Scanner at the XTM Facility, Palaeobiology Research Group, University of Bristol and have been analyzed using the Dragonfly® software. The results of the scans, together with measurements of die sizes are included in Fig. 11. It can be seen that the Silicon PiN diode has the largest die, followed by the SiC JBS and MPS.

Fig. 12 provides a comparison of the IV characteristic of the devices based on the device datasheet and the TCAD model output. It can be seen that outputs of the developed models have good agreement with datasheet measurements with a small margin of error. This indicates that the structure of the model and its parameters are close to that of the actual device parameters.

Fig. 13 shows the results of modelled diode voltage by TCAD for all 3 devices during the UIS pulse before failure together with the experimental measurements at 25 °C, while Fig. 14 shows similar comparison of models and measurement results for inductor current.

The results of the simulations indicate that the models agree with the measurements for all devices. The measured diode voltage of the Silicon PiN diode is higher than that of the model output due to its higher effective breakdown voltage [11,12] than the values stated in the datasheet of the device. The CT scan of the three devices after failure

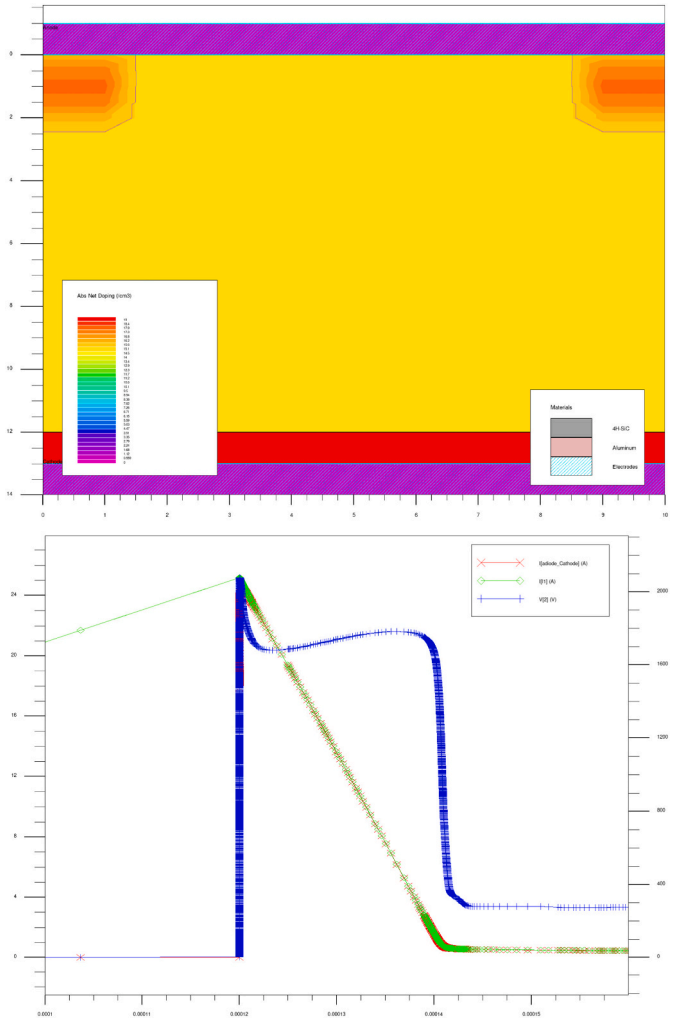

Fig. 10. Structure of the 4H-SiC JBS diode in TCAD and the current and voltage waveforms under UIS stress.

indicate that there are molten anode metallization caused by the elevated temperatures [6], leading to wear-out of the bond-wires. The devices have similar packaging though, and thus the impact of package degradation on the measured performance of the devices is not making an impact on the comparative analysis. The devices have also been subject to static and dynamic tests, the results of which can be found in [13].

4. TCAD simulation analysis

Figs. 15-23 show the TCAD simulation results of junction temperature, current density and electric field density of all three devices during different stages of the UIS stressing.

Fig. 15 demonstrates the current density of the Silicon PiN diode during different stages of UIS stressing. It can be seen that the current density is at its peak when the load current reaches its maximum, and the density is higher on the left side of the device as the actual P—N junction between the anode and the drift region is on the left, while on the right, as in Fig. 8, are the edge terminations to relieve the electric field density at the edges of the device. This results in the current to flow between the P—N junction terminals.

Fig. 16 demonstrates the lattice temperature of the device, where it can be seen that the device is at its hottest during UIS, and especially at the end of the UIS stress period, where the peak lattice temperature coincides with the peak current density, as expected.

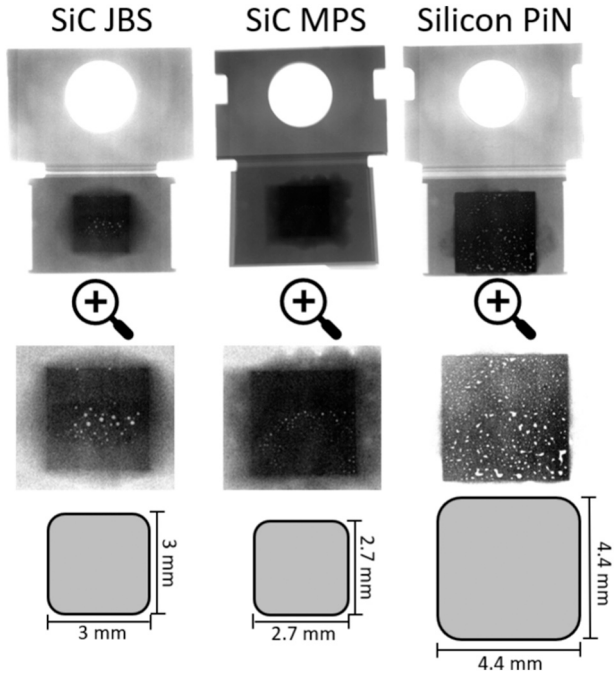

Fig. 11. CT scan of the Silicon PiN diode, SiC JBS and SiC MPS diodes to determine accurate die size.

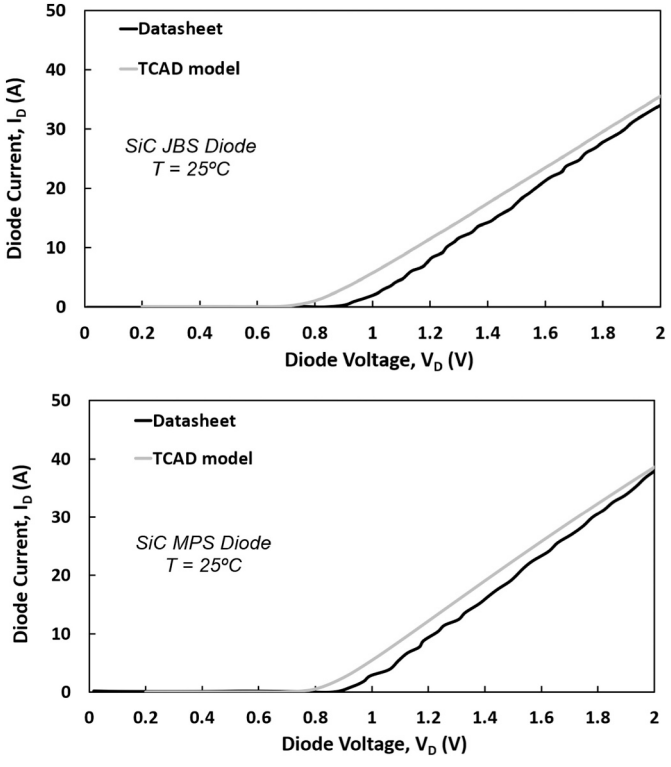

Fig. 12. TCAD Modelled and measured IV characteristic of Silicon PiN, SiC JBS and SiC MPS diode.

Fig. 17 demonstrates the electric field density at different stages of the UIS, where it can be seen that it is at its peak when the inductive induced voltages is applied to the diode. The edge terminations have alleviated the density of electric field, which in turn have increased the capability of the diode to withstand the high UIS voltage. The field density is drops as soon as the induced voltage is removed.

Fig. 18 demonstrates the current density of the SiC MPS diode during

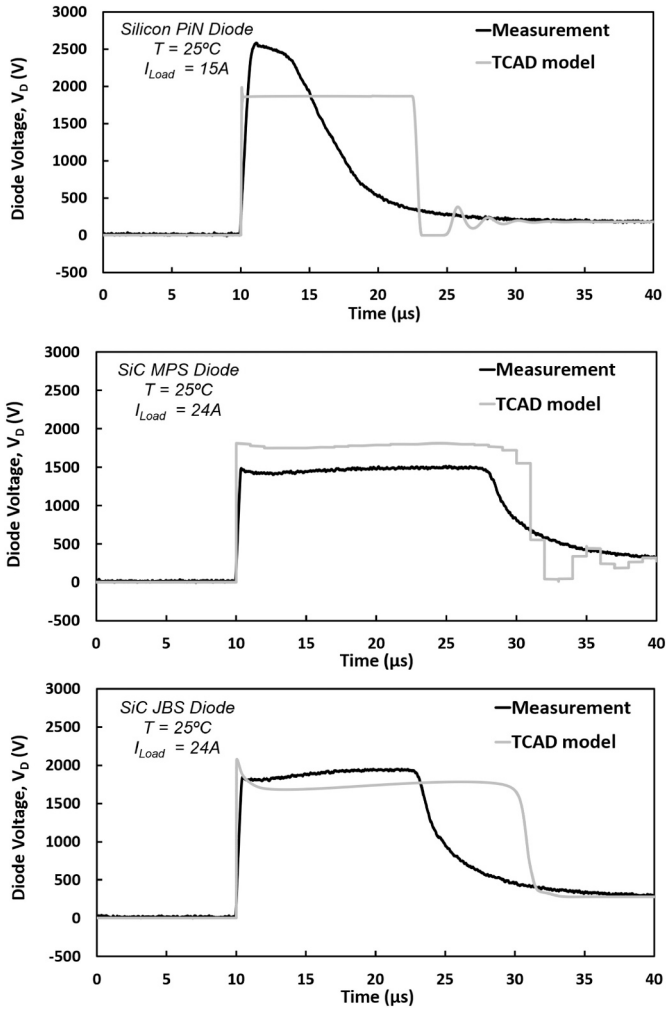

Fig. 13. TCAD Modelled and measured Diode Voltage of Silicon PiN, SiC JBS and SiC MPS diode.

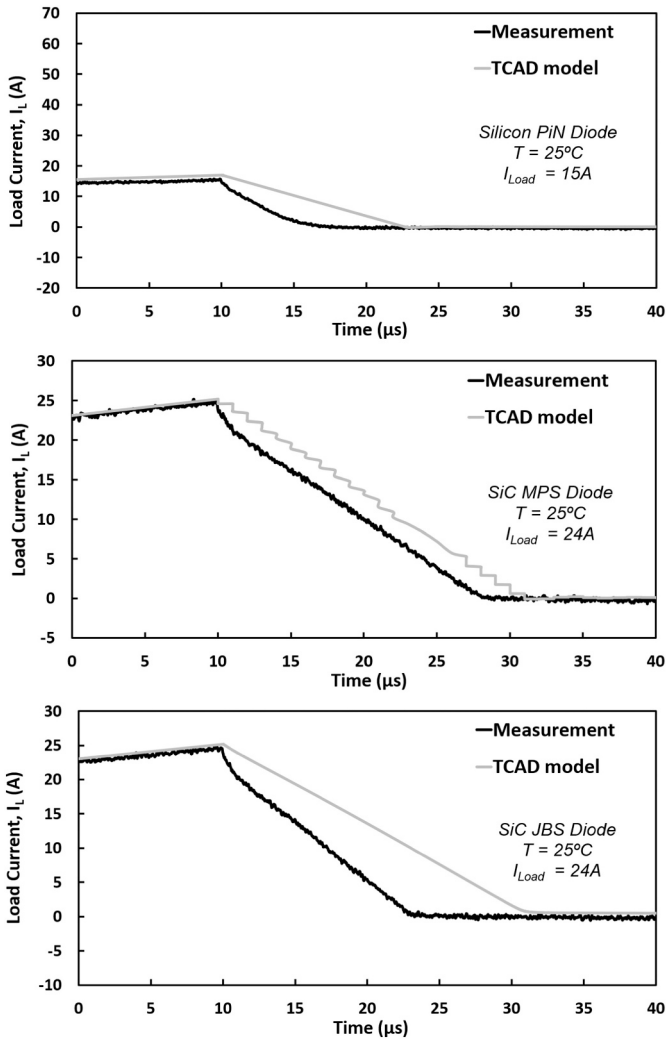

Fig. 14. TCAD model output and measured inductor current of Silicon PiN, SiC JBS and SiC MPS diodes.

avalanche, where it can be seen that the peak of the current density is happening between the two Schottky contacts and P-region, enabling taking advantage of both SBD and P regions for ambipolar conduction. The peak of the current coincides with the peak of UIS current.

Fig. 19 demonstrates the lattice temperature of the device at different UIS stages, indicating the maximum temperature coinciding with maximum current density, though with some delay once the full UIS heat has been generated. Fig. 20 indicates the electric field distribution of the 4H-SiC MPS diode during the UIS stress. It can be seen that the peak of electric field is on the P—N junctions, and presence of a secondary junction has alleviated the distribution of the electric field in the device, leading to its increased blocking capability. The peak of the electric field is the edges of the P—N junction, and coincides with the maximum applied UIS voltage, and it drops sharply as soon as the UIS voltage is removed.

Fig. 21 presents the distribution of current density in the SiC JBS diode. It can be seen that the P-regions, implemented as edge terminations, contribute to conduction while the Schottky contact is contributing most next to the P-terminations. These lead to uniform distribution of the current density between the two contacts, with significant density of current being located at the centre of the device.

Fig. 22 shows the lattice temperature of the SiC JBS during the UIS, where the temperature across the entire lattice has raised significantly immediately following dissipation of the UIS current, at the end of the UIS transient, leading to a uniform temperature rise across the device, though it drops significantly once the generated heat is removed.

Fig. 23 demonstrates the electric field density of the device where it can be seen that the peak electric field is at its peak during presence of the UIS voltage, and the peak field is on the P-terminations.

Overall, it can be observed that the junction temperature of SiC devices is higher than the Silicon device. This is in-line with the results of experiments because the critical avalanche energy is higher for SiC devices. The critical load current of SiC JBS diode is also the highest, followed by the SiC MPS diode and the Silicon PiN diode. It can also be seen that a high electric field is formed between the long P^+ region and the N^- drift region for the SiC MPS diode. It is shown that the electric field at the Schottky contact for SiC MPS diode is reduced as it is shielded by the closest P^+ region while SiC JBS diode experiences higher electric field.

The avalanche current of SiC JBS diode is more evenly distributed in the device active region when compared with that of SiC MPS diode and Silicon PiN diode. This is because the higher electric field in the middle of Schottky contacts lead to a more evenly distribution of avalanche current as it is diverted to two different edges of the P^+ region. In contrary, current crowding is observed in the case of SiC MPS diode due to the smaller electrical field formed at the Schottky contact.

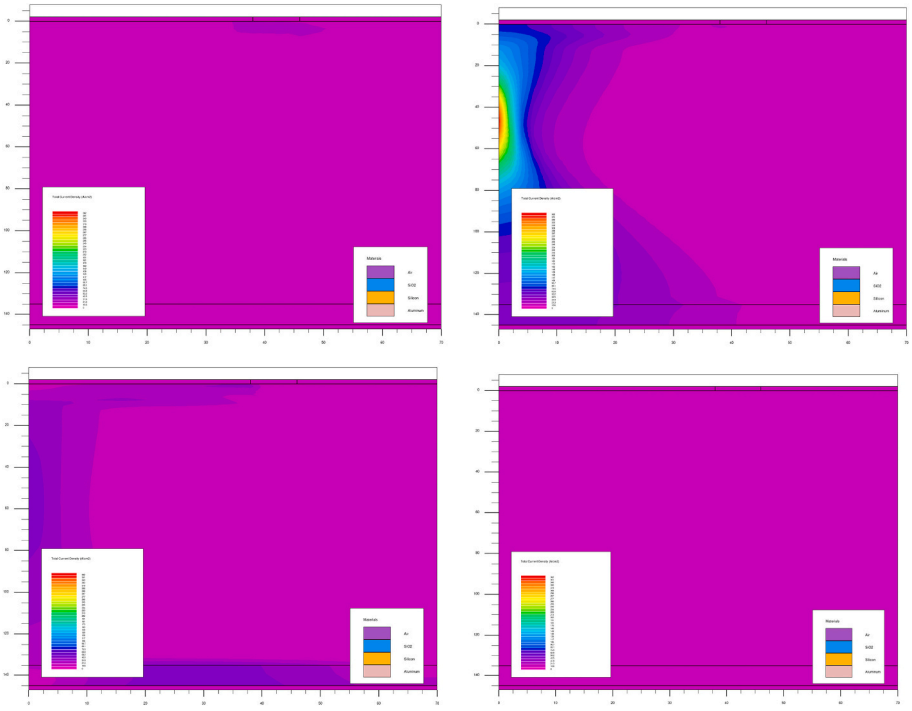

Fig. 15. TCAD simulation of current density for the Silicon PiN diode during stressing stages by UIS.

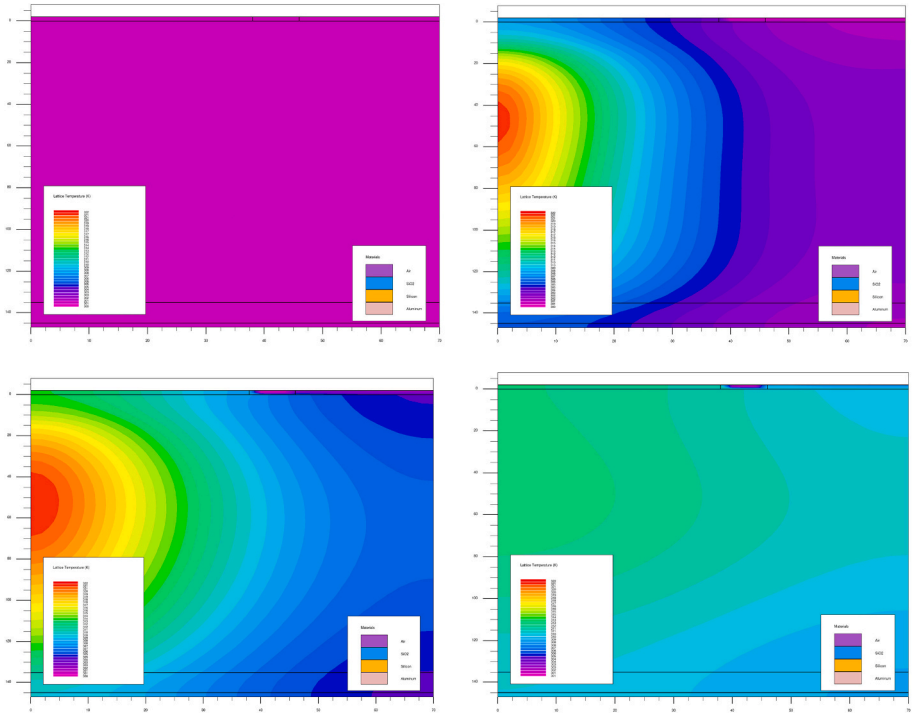

Fig. 16. TCAD simulation of lattice temperature for the Silicon PiN diode during stressing stages by UIS.

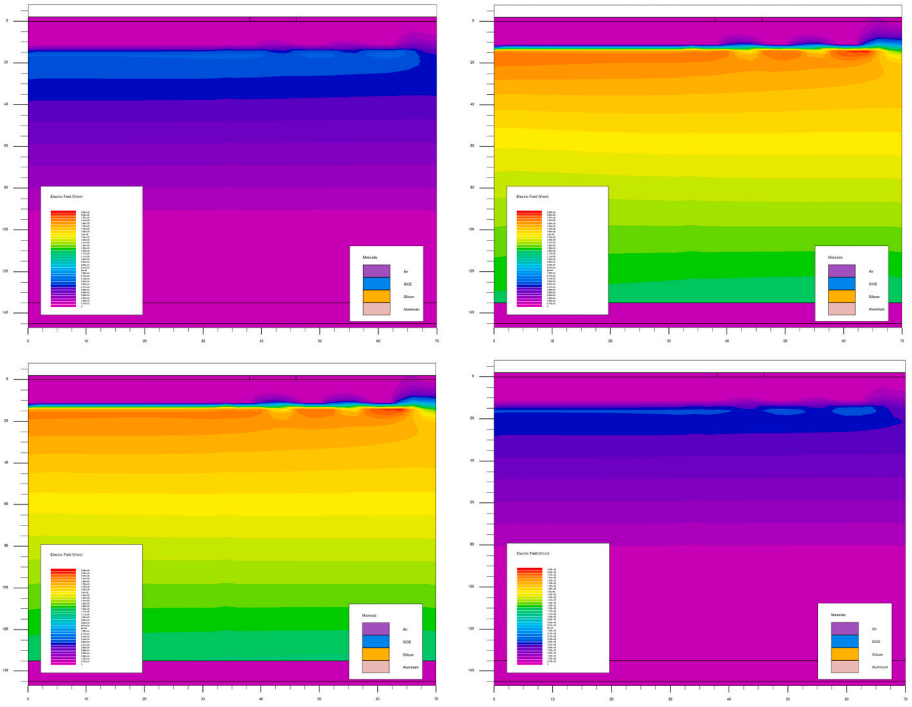

Fig. 17. TCAD simulation of electric field density for the Silicon PiN diode during stressing stages by UIS.

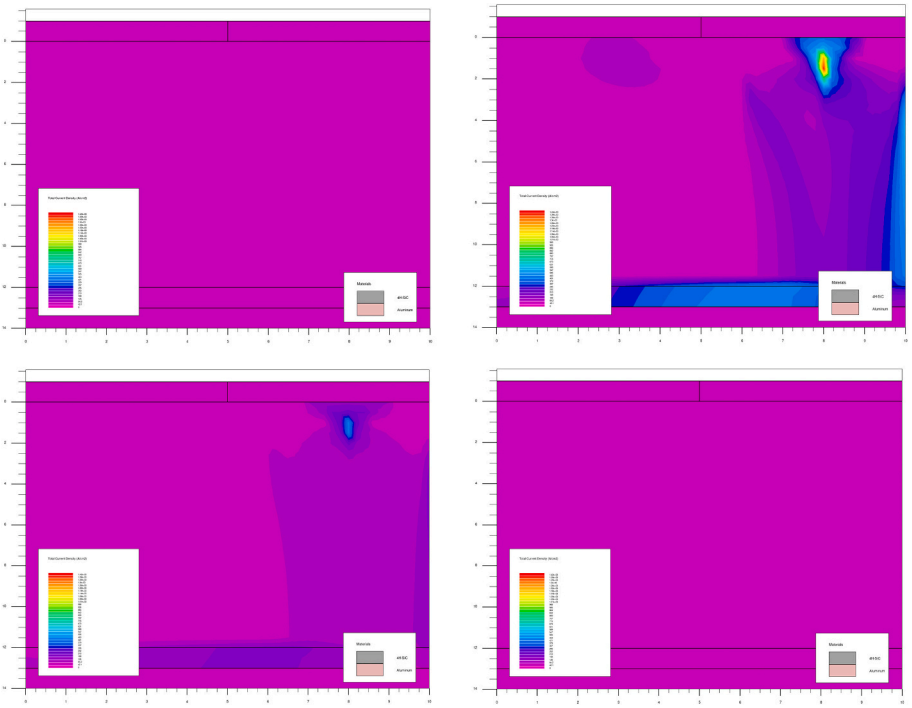

Fig. 18. TCAD simulations of the current density for the 4H-SiC MPS diode during stressing stages by UIS.

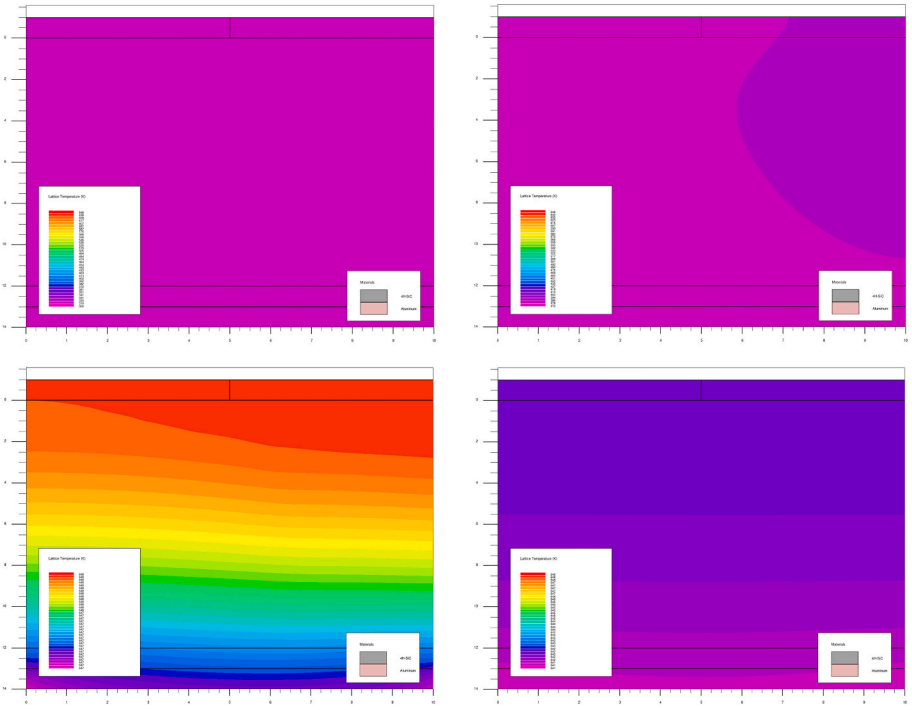

Fig. 19. TCAD simulation of lattice temperature for the 4H-SiC MPS diode during stressing stages by UIS.

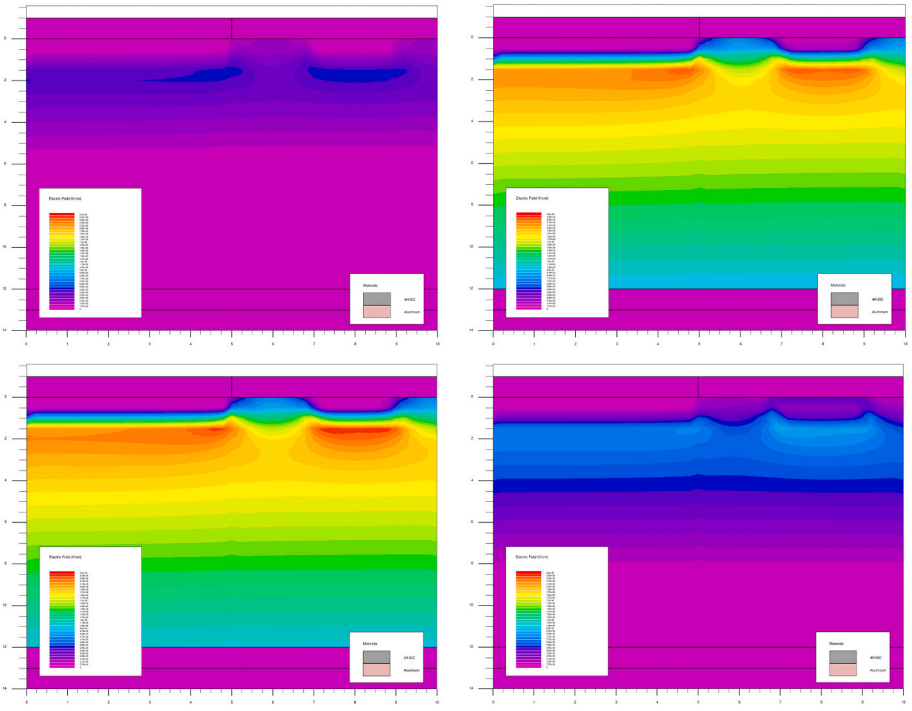

Fig. 20. TCAD simulations of electric field density for the 4H-SiC MPS diode during stressing stages by UIS.

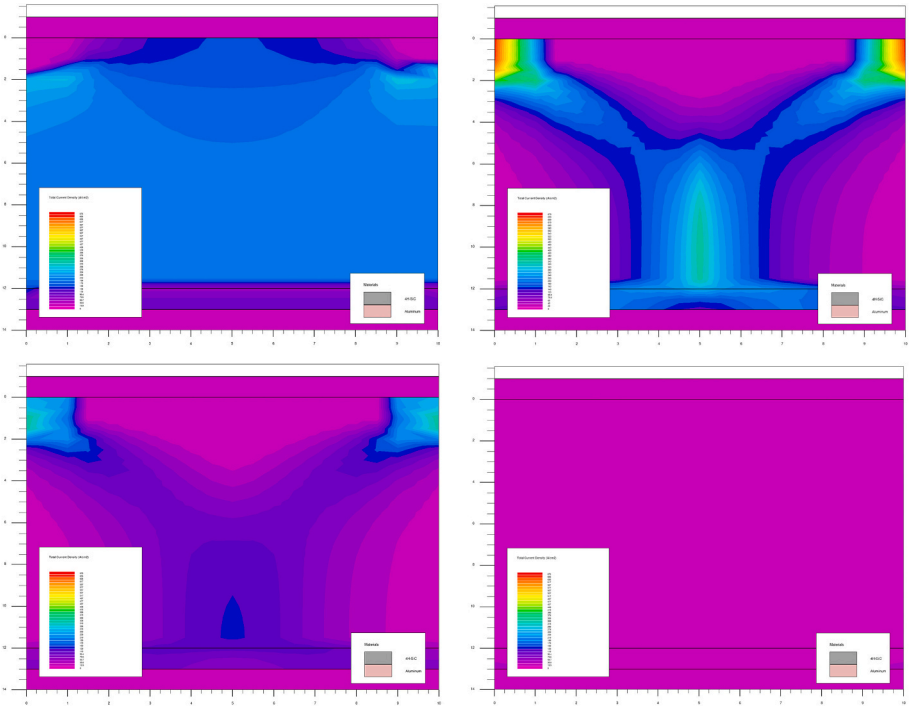

Fig. 21. TCAD simulation of the current density for the 4H-SiC JBS diode during stressing stages by UIS.

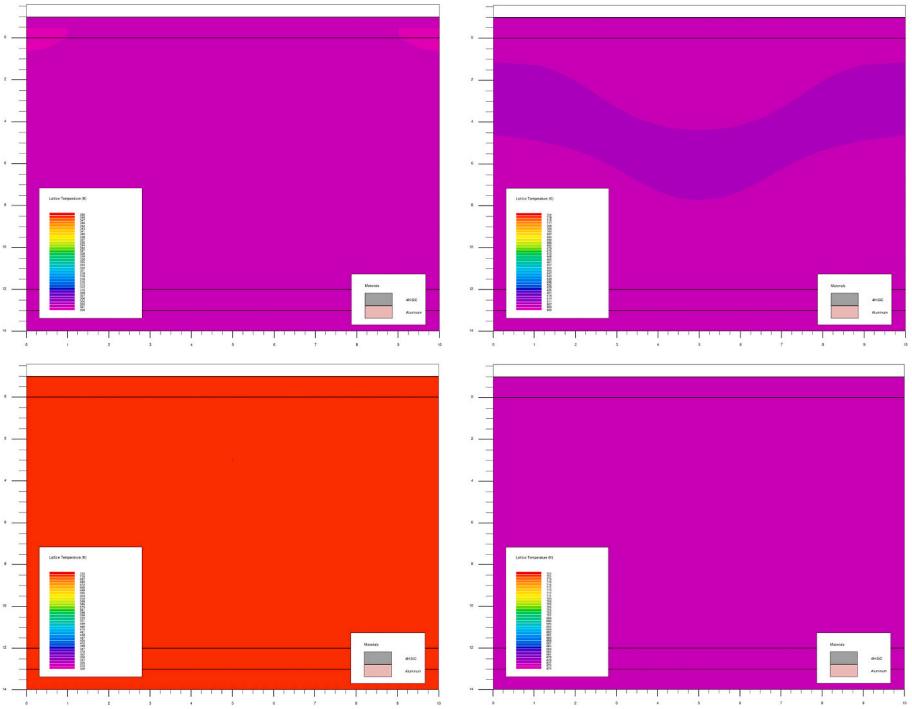

Fig. 22. TCAD simulation of lattice temperature for the 4H-SiC JBS diode during stressing stages by UIS.

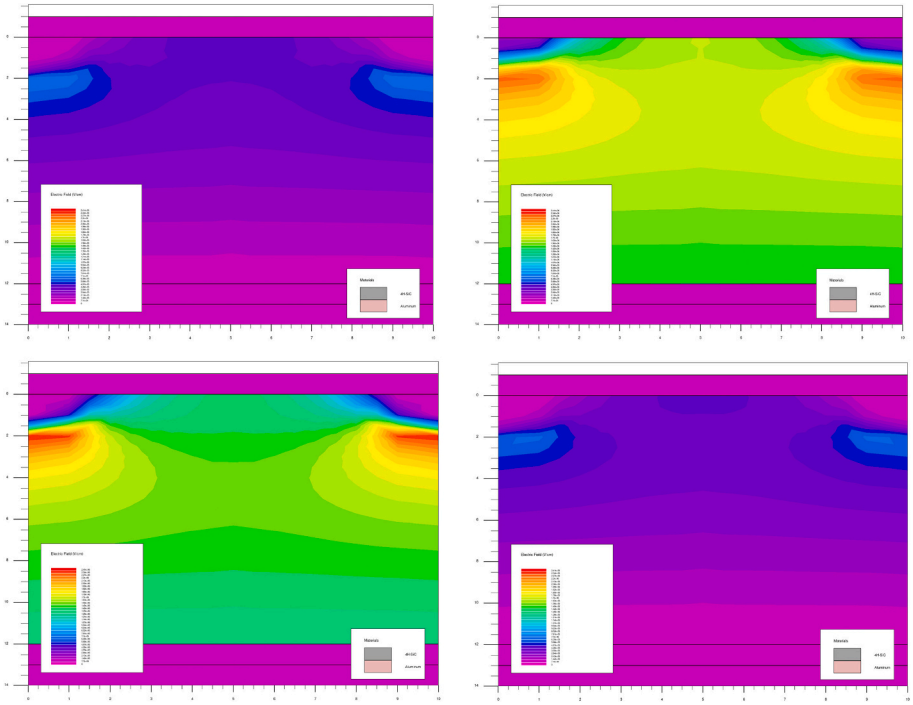

Fig. 23. TCAD simulation of the electric field density for the 4H-SiC JBS diode during stressing stages by UIS.

5. Conclusion

A wide range of UIS measurements and TCAD simulation shows that the avalanche ruggedness of SiC MPS & JBS diodes outperform that of the closely rated Silicon PiN diode. Both TCAD simulation and experimental results reveal that SiC JBS diode are able to withstand higher avalanche current than SiC MPS diode in different operation temperatures. Modelling results also indicate that SiC JBS diode can withstand the highest junction temperature in line with the calculated avalanche energy. TCAD models support the argument that the Silicon PiN diode has pre-maturely failed by extreme electric field at the junction due to the significant UIS voltage, while the failure mechanism in the 4H-SiC MPS & JBS diodes have been dominated by heat generation by UIS.

CRediT authorship contribution statement

Chengjun Shen: Conceptualization; Investigation; Writing - Original Draft.

Renze Yu: Investigation.

Saeed Jahdi: Conceptualization; Methodology; Writing - Review & Editing.

Phil Mellor: Writing - Review & Editing.

Sai Priya Munagala: Investigation.

Andrew Hopkins: Investigation.

Nick Simpson: Investigation.

Olayiwola Alatise: Methodology; Writing - Review & Editing.

Jose Angel Ortiz-Gonzalez: Methodology; Writing - Review & Editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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