Analyzing the Impact of Die Positions inside the Power Module on the Reliability of Solder Layers for Different Power Cycling Scenarios

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***Abstract*—Solder layers, used as bonding material inside the power module to attach the semiconductor die on Direct Bond Copper (DBC) substrate and DBC substrate on baseplate, are one of the regions most prone to failure. The failure usually occurs in the form of solder cracks and depends on various operating conditions, such as - maximum temperature, temperature swing, and heating time. The cracks generated inside the solder layers can eventually result in its delamination. Power modules are usually power cycled to estimate the failure sites and mechanisms. However, the failure mechanisms can vary depending on the frequency, amplitude, and range of the temperature in the Power Cycling Tests (PCT). In this study, we have used the Finite Element Method (FEM) in COMSOL Multiphysics to analyse the impact of the PCT on both die attach, and baseplate attach solder layers. Additionally, the effect of the degree of asymmetry in the die position on the reliability of both the solder layers are analysed. The FEA (Finite Element Analysis) results are analysed to have a better understanding about the aspects impacting the lifetime of the power module.**

***Index Terms*—Power module, finite element method, power cycling, solder, viscoplasticity, lifetime estimation**

I. Introduction

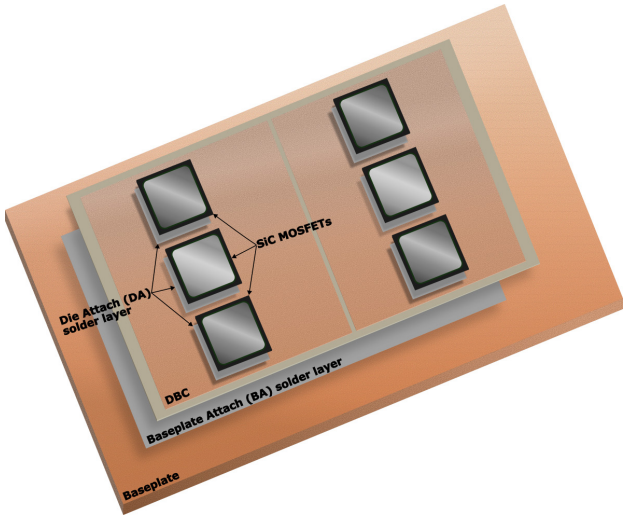
The automotive industry has undergone a significant transformation in recent years due to the increasing government policies favoring the adoption of Electric Vehicle (EV). It is projected that by 2040, 85% of new trucks sold in the United States, Europe, and China will be equipped with zero-emission powertrains [1]. The electric power-train, which is a crucial component of the EV comprises energy conversion stages like inverter [2] and dc/dc converter [3]. Inverter, which is the backbone of the electric powertrain constitutes around 45% of the total powertrain costs [4]. It is typically composed of different components and technologies, with power semiconductor devices such as diodes and Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) being the core components of the inverter. These devices are typically packaged in various configurations to provide electrical interconnections, thermal management, mechanical support, and protection from the environment [5]. Multi-chip power modules are the most common packaging type for power semiconductor devices [6].

Traditionally, Silicon (Si) Insulated-Gate Bipolar Transistor (IGBT) have been used inside the inverters. However, due to the proven benefits of Silicon Carbide (SiC) over Si, SiC MOSFETs are now fast replacing these Si IGBTs. SiC offers higher breakdown voltage, higher switching frequency, superior thermal conductivity, and can operate at higher junction temperature [7]. Due to these superior material properties, SiC based power modules tend to be more compact compared to Si based power modules of the same power rating. Despite the advantages of compactness in SiC-based power modules, their reliability remains a significant challenge. Previous research, such as the work presented in [8], has used the physics-based approach to study the reliability aspects of these modules by comparing them with Si IGBT and SiC MOSFET modules. However, most physics-based studies have introduced symmetry to reduce computational time.

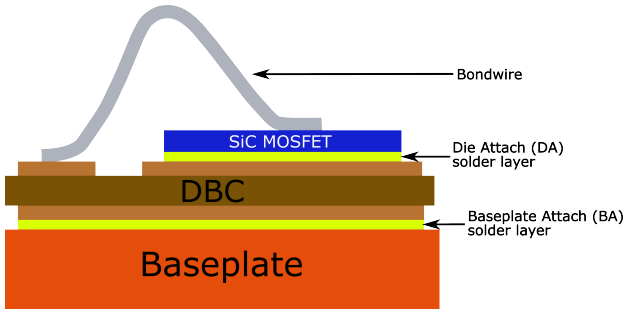
In this study, we conducted a thermo-mechanical analysis on the power module using the Finite Element Method (FEM). A 3D model of the power module was designed and analyzed using COMSOL Multiphysics. The effect of the die position and its population during different power cycling tests was analyzed using these 3D models. This paper is organized in the following manner. In Section II, different structures of power modules analyzed in this study have been discussed. Section III explains setting up the FEM model in COMSOL Multiphysics. In Section IV, the results are discussed with final conclusions given in Section V.

II. Structure of Power Module

Figure 1 shows the typical structure of a power semiconductor module. The configuration of the SiC MOSFETs on the Direct Bond Copper (DBC) varies depending on the



(a) 3D explosion view of the structure of power module (bondwires not shown).



(b) Cross-section of the power module.

Fig. 1: Conventional power module employing SiC MOSFETs, and solder layers.

topology being utilized. Multiple SiC MOSFETs are typically soldered onto the DBC in different configurations. To enhance the power capacity of the module, several dies are often connected in parallel, as shown in Figure 1a. The position and population of the dies on the DBC can result in different thermo-mechanical stresses for different Die Attach (DA) solder layers, leading to different lifetimes.

This paper investigates three different configurations of the power module in order to estimate the lifetime of the DA solder layer, depending on the die's position and population on the DBC. The first configuration, as shown in Figure 2a, features a single SiC MOSFET placed symmetrically at the center of the DBC. In the second configuration, as shown in Figure 2b, the SiC MOSFET is moved closer to the corner of the DBC. In the last configuration, as shown in Figure 2c, three SiC MOSFETs are located near one edge of the DBC. The dimensions of different materials used inside the power module are listed in Table I, with dimensions of the die and DA taken from [8]. It is important to note that the term DA refers to the solder layer present between the SiC MOSFET die and the DBC, while the term Baseplate Attach (BA) refers to the solder layer between the DBC and the baseplate.

TABLE I: Dimension of the power module.

Items	Length (mm)	Breadth (mm)	Thickness (mm)	Material
Semiconductor Die	3.36	3.1	0.18	SiC
Die attach solder	3.36	3.1	0.12	SAC305
DBC (Top layer)	10	10	0.3	Copper (Cu)
DBC (Substrate)	11	11	0.63	Al_2O_3
DBC (Bottom layer)	10	10	0.3	Copper (Cu)
Substrate attach solder	10	10	0.12	SAC305
Base Plate	15	15	1	Copper (Cu)

III. Finite Element Modelling

TABLE II: Properties of the materials [8].

Parameters	SiC	Copper (Cu)	Al_2O_3	SAC305
Coeff. of Thermal Expansion (10^{-6}/K)	3.4	17	6.5	23
Heat Capacity (J/(kg×K))	690	385	730	150
Density (kg/m^3)	3216	8960	3260	7380
Thermal Conductivity (W/(m×K))	370	400	35	50
Young's Modulus (GPa)	501	110	400	40
Poisson's Ratio	0.45	0.35	0.22	0.4

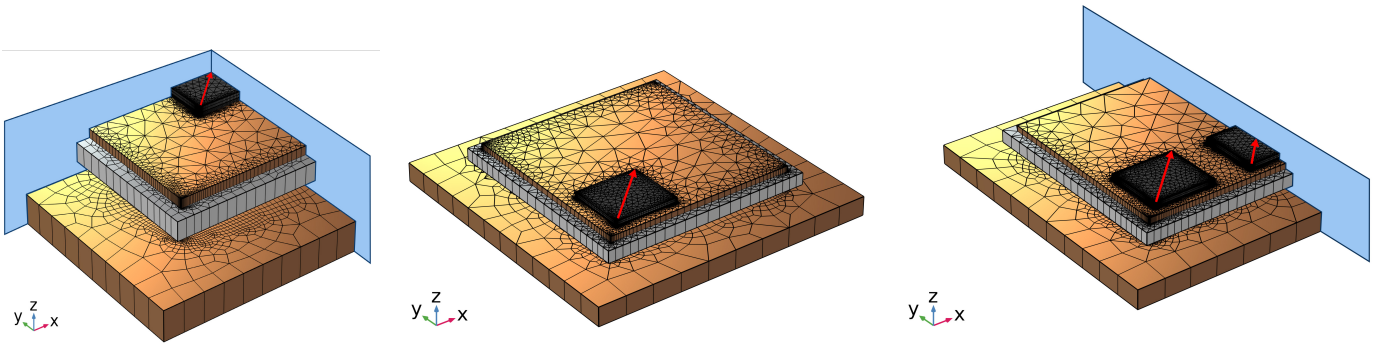
The use of Power Cycling Test (PCT) is a highly effective and accurate method for analyzing the reliability and lifetime of power modules and devices. However, it can be challenging to apply PCT in practice for testing expensive devices since the method requires numerous samples, which can be time-consuming and costly. To address this challenge, many researchers and companies use the FEM as a preliminary approach to simulation. FEM enables the calculation of stress and strain, which are difficult to measure in actual experiments, making it a valuable tool for predicting the reliability of power modules. Reliable simulation results obtained from FEM can also serve as an essential reference for developing more advanced packaging structures. Therefore, in this paper, we mainly use FEM with COMSOL Multiphysics to analyze the reliability of the solder layer in the SiC power model under PCT and investigate the impact of the degree of asymmetric die position on it.

A. Modelling

This section provides a detailed step-by-step modeling procedure for FEM, including boundary conditions, meshing, and parameter selection for the physical model.

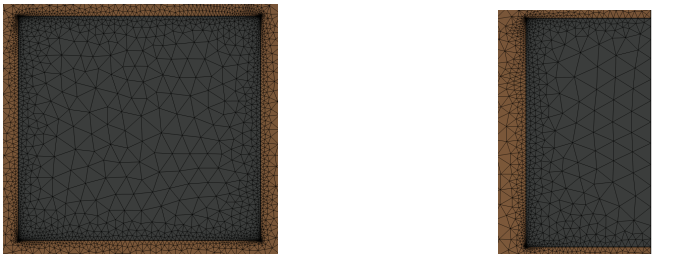
To reduce model size and computational time, symmetry has been used wherever possible. Quarter symmetry has been used for symmetric placement, as shown in Figure 2a. The blue planes in the figure represent the symmetrical boundaries in the yz- and xz-planes. Similarly, half symmetry has been used for the full module condition, as shown in Figure 2c. No symmetry condition has been used for asymmetric placement.

The quality of the mesh used for discretizing the model plays a crucial role in obtaining accurate approximate solutions to the problem. To ensure accuracy, a finer mesh is required



(a) Symmetric placement. (b) Asymmetric placement. (c) Full module.

Fig. 2: FEM models with their mesh elements (symmetrical boundary conditions defined in blue planes).



(a) Full module (Die 1). (b) Full module (Die 2).

Fig. 3: Mesh elements distribution on die and DA solder layers.

in regions where higher stresses are typically concentrated, such as at the edges and corners of the solder layer. A mesh sensitivity analysis has been performed using symmetrically placed models, by varying the number of elements and the element ratio at the edges of the DA layer. The final mesh has been selected based on the criteria of minimum standard deviation in the cycles to failure in the DA solder layer. For a complete model of the die and DA layer, this resulted in 94 elements at one edge with element ratio of 15 and maximum element size of 0.3 mm. The elements on the edges are symmetrically distributed, ensuring that a higher mesh concentration is achieved on each die corner. Figure 2 shows the meshing in different configurations, indicating that the regions around the edges and corners of different layers are finely meshed. It also shows the diagonal lines along which results like viscoplastic strain have been plotted. These diagonal lines do not include corners so as to exclude any singularity in the plots. Figure 3 focuses more on the meshing on and around the die and DA layer. In Figure 3b, which shows the second die of the full module, 94 symmetrically distributed mesh elements are found on the complete edge, while the remaining edges contain 47 mesh elements due to the presence of a symmetrical plane on the right side.

To perform the thermo-mechanical analysis, the heat transfer in solids and solid mechanics physics have been utilized

TABLE III: Anand model parameters for SAC305 solder [8].

Definition	Parameters	Values
Pre-exponential factor	A (s^{-1})	4.1×10^6
$\frac{\text{Activation energy}}{\text{Boltzmann's constant}}$	Q/R (K)	9460
Stress multiplier	ξ (1)	1.5
Strain rate sensitivity of stress	m (1)	0.303
Initial deformation resistance	s_0 (MPa)	12.41
Hardening coefficient	h_0 (MPa)	1378.95
Hardening sensitivity	a (1)	1.3
Deformation resistance sensitivity	η (1)	0.07
Deformation resistance saturation value	s (MPa)	13.79

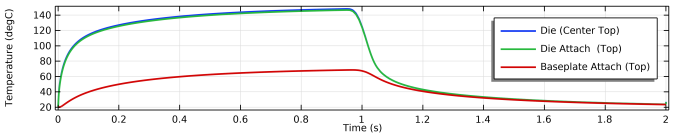
to generate thermal expansion multiphysics. The thermo-mechanical properties of the materials used in the study are listed in Table II. Specific parameters have also been required for each physical model. For the solid mechanics interface, all materials have been considered to be elastic, except for the solder which has been chosen to be viscoplastic. The Anand model has been employed to model the viscoplasticity of the solder layer, which takes into account both time-independent and time-dependent strain effects. This model assumes that the plastic flow occurs at all nonzero stress values and does not necessitate explicit yield conditions. The parameters used in the Anand model for SAC305 solder have been listed in Table III. The boundary conditions in the heat transfer in solid physics have been defined as follows: symmetry boundary condition has been defined in the symmetric planes shown in Figures 2a and 2c; the entire die volume has been defined as a homogeneous heat source; the bottom surface of the baseplate has been defined as a convective heat flux emulating a water-cooled heat sink with a plate length of 0.5 m, coolant velocity of 3 m/s, and coolant temperature of 293.15 K; remaining boundaries have been set as thermally insulated with an initial temperature of 293.15 K. The solid mechanics

TABLE IV: Volume averaged heat source values (W/m^3).

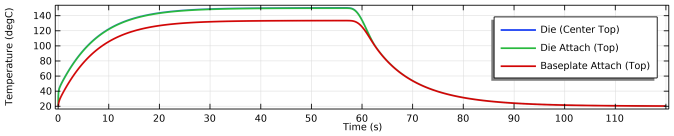
Case	Fast PCT	Slow PCT
Symmetric placement	90	16
Asymmetric placement	75	16
Full Module (Die 1 & 2)	62.2	8.1

TABLE V: Morrow model parameters for SAC305 solder [8].

Parameters	Values
Fatigue energy coefficient (W_f)	5.5×10^7 (J/m^3)
Fatigue energy exponent (m)	-0.69



(a) Fast PCT.



(b) Slow PCT.

Fig. 4: Temperature cycling in the asymmetric case during fast and slow PCT respectively.

boundary conditions have been defined as follows: the bottom surface of the baseplate has been fixed, and the remaining boundaries have been set free to move.

Two different power cycling tests are studied here, fast PCT and slow PCT. In case of the fast PCT, heating and cooling time are set to 1 sec each, while in the slow PCT, heating and cooling time are set to 60 sec each. Volume averaged heat source values, given in Table IV, are taken such that similar temperature cycling is achieved in all cases.

The study analyses the lifetime of the DA solder layers by using a fatigue node and fatigue study inside COMSOL Multiphysics. To estimate the number of cycles to failure, different lifetime model options are provided in the fatigue node. In this study, Morrow's lifetime model has been employed, which uses viscoplastic dissipation density within the solder layer. Morrow's fatigue model has been described using (1).

$$\Delta W_{vp} = W_f'(N_f)^m \tag{1}$$

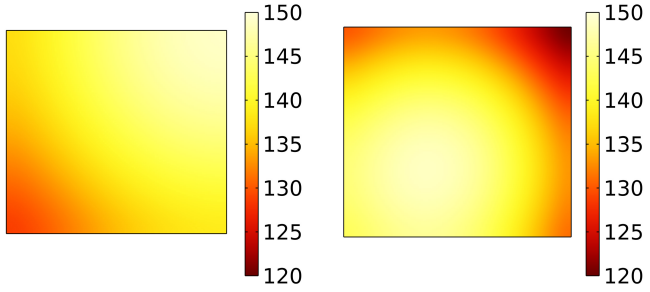
where, ΔW_{vp} represents the viscoplastic dissipated energy density during one cycle, N_f denotes the number of cycles to failure, and W_f' and m are the material constants. The material constants used in this study are mentioned Table V.

IV. Results and Analysis

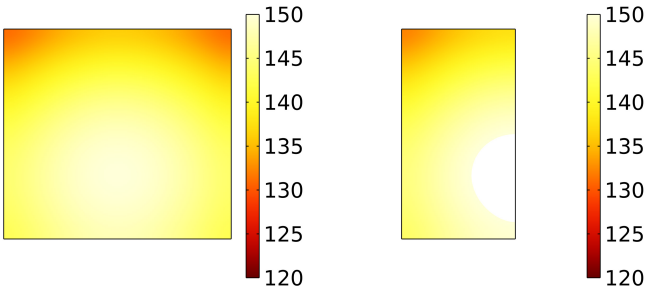
A. Thermal Performance

Figure 4 shows the temperature cycling of the die, DA, and BA solder layers during both fast and slow PCTs. It can be observed that, in both cases, the temperature of the DA solder layer closely follows that of the die. However, for the BA solder layer, temperature cycling is higher during slow PCT as compared to the fast PCT. This can result in higher levels of thermo-mechanical stress in the BA solder layer during slow PCT.

Figure 5 presents the temperature distribution in the solder layer of the DA during fast PCT under various placement

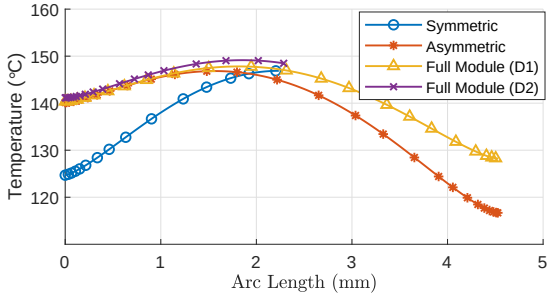


(a) Symmetric placement. (b) Asymmetric placement.

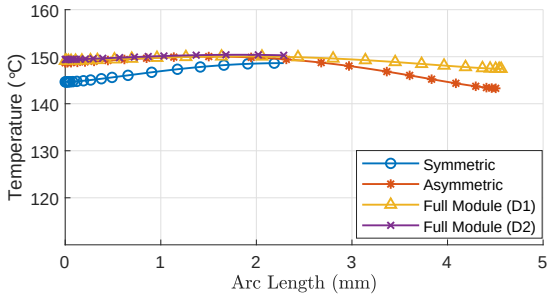


(c) Full module (Die 1). (d) Full Module (Die 2).

Fig. 5: Temperature distribution in DA solder layer surface at maximum temperature point during fast PCT (Scale in °C).

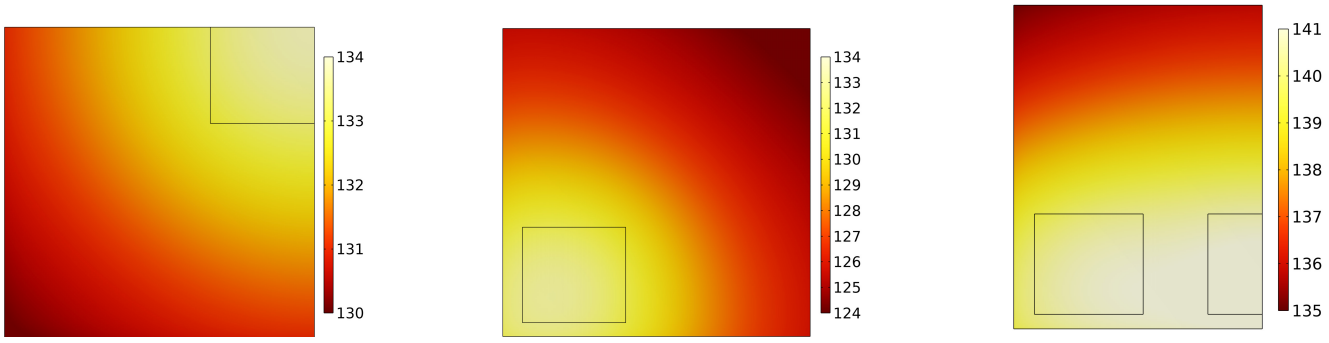


(a) Fast PCT.



(b) Slow PCT.

Fig. 6: Temperature along the diagonal line in the DA solder layer during fast and slow PCT.



(a) Symmetric placement. (b) Asymmetric placement. (c) Full module.

Fig. 7: Temperature distribution in BA solder layer surface at maximum temperature point during slow PCT (Scale in ^{o}C).

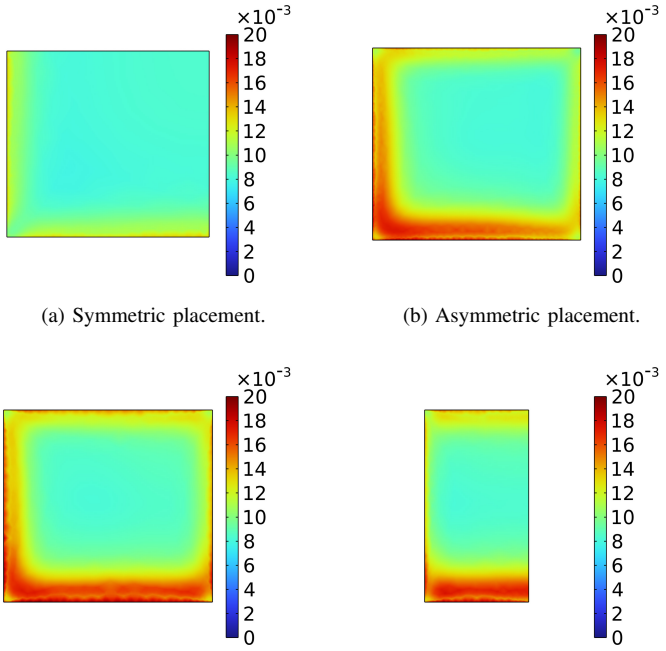
scenarios. In the case of symmetric placement, as shown in Figure 5a, the temperature at the center of the die was observed to be higher than that at the corners and edges. This is because the heat from the DA layer spreads in all directions inside the DBC, resulting in a lower temperature in the regions closer to the edges. In the asymmetric placement scenario, as depicted in Figure 5b, the heat in the DA layer near one corner of the DBC finds less area to spread than that in the opposite corner. This also holds for the regions closer to the edges and those farther away from them, resulting in a higher temperature in the region near the corner and edges of the DBC. For full modules, shown in Figures 5c and 5d, the temperature of the corner die DA layer increases in the region closer to the middle die. This is because the heat-spreading area is reduced due to the placement of the 2nd die.

Figure 6 shows the temperature along the diagonal in the DA layer during fast and slow PCT, respectively. It can be seen that the temperature gradient along the diagonal is higher in fast PCT with a higher temperature in the region near the corner of the DBC, except in the symmetric condition. However, temperature along the diagonal during slow PCT is more uniform and closer to the die temperature. This is because during slow PCT, the module reaches the steady state with DA and BA solder layers temperature closer to the die temperature.

Figure 7 shows the temperature distribution in the BA solder layer during slow PCT. From the figures, it can be observed that the temperature distribution in the BA solder layer depends on the location of the die. Additionally, it has been observed that the maximum temperature also varies depending on the location of the die on DBC . The temperature distribution in BA solder layer during fast PCT has not been shown due to smaller cycling as shown in Figure 4b.

B. Thermo-mechanical Performance

As described in the preceding section, the temperature distribution in the DA and BA solder layers varies depending on the placement and the number of dies, which results in variations in the magnitude of the thermo-mechanical loading in different regions of the solder layers during both fast and slow PCT. In this section, thermo-mechanical performance of the DA and the BA solder layers has been discussed.



(a) Symmetric placement. (b) Asymmetric placement.

(c) Full module (Die 1). (d) Full Module (Die 2).

Fig. 8: Accumulated viscoplastic strain in DA solder layer after one cycle during fast PCT.

1) DA Solder Layer: Figure 8 shows the accumulated viscoplastic strain in the DA solder layer after one cycle during fast PCT. As seen in the figure, the accumulated viscoplastic strain is the least for symmetric placement and the highest for the corner die (die 1) of the full module. Further analysis in Figures 8b-8d reveals that regions of the DA solder layer closer to the corner and edges of DBC undergo significant strain when compared to other regions. Similar observations are seen in Figure 9, which presents the accumulated viscoplastic strain along the diagonal in the DA solder layer. Additionally, it

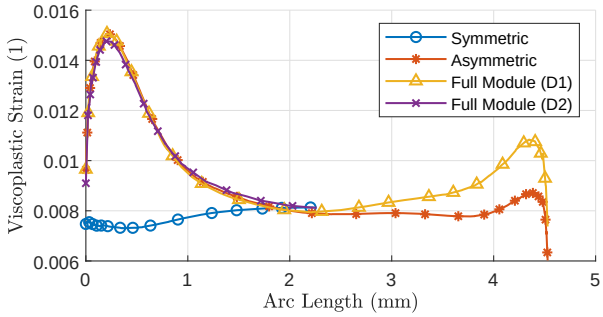


Fig. 9: Accumulated viscoplastic strain along the diagonal line in DA solder layer after one cycle during fast PCT.

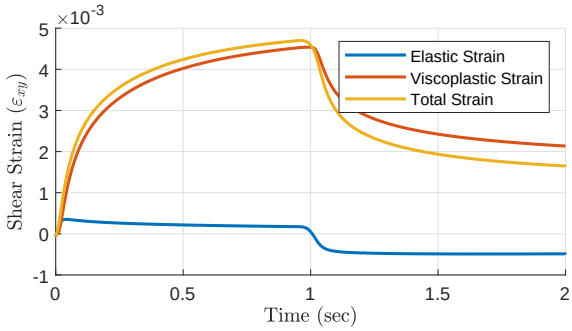
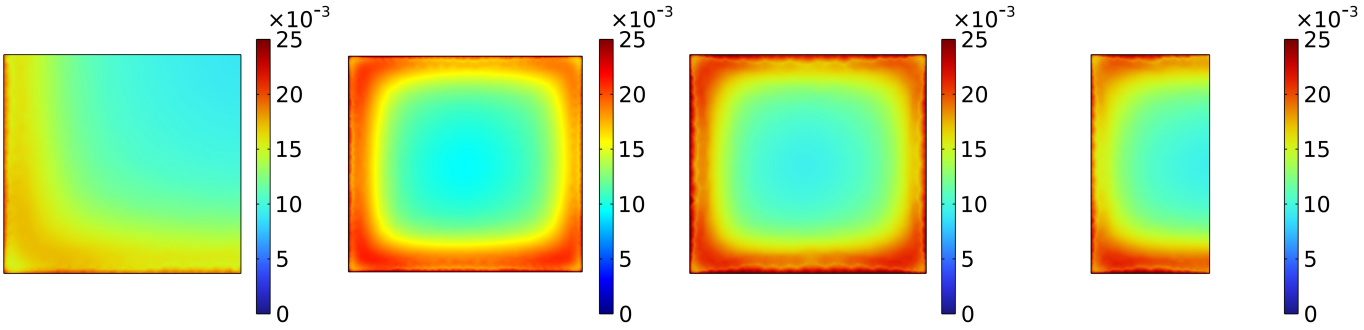


Fig. 10: Strain history at the maximum strained point during fast PCT inside DA in asymmetric placement case.



(a) Symmetric placement. (b) Asymmetric placement. (c) Full module (Die 1). (d) Full Module (Die 2).

Fig. 11: Accumulated viscoplastic strain in DA solder layer after one cycle during slow PCT.

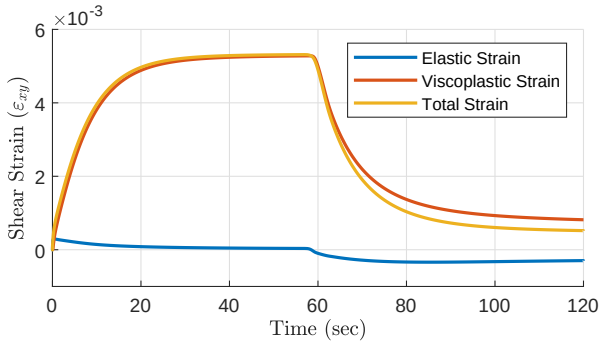
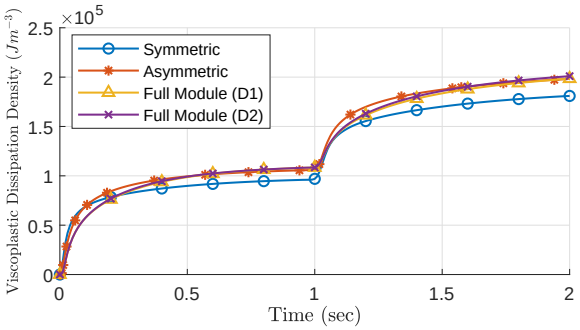


Fig. 12: Strain history at the maximum strained point during slow PCT inside DA in asymmetric placement case.

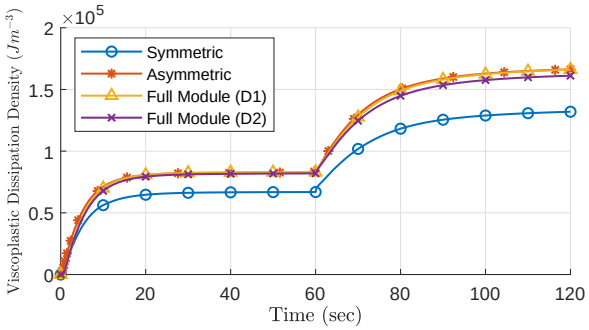
can be observed that the presence of the second die in the full module leads to an increase in viscoplastic strain in the nearby corner of die 1. It is important to note that the sharp corners and change in material can result in singularity in these regions, which tends to have very high values. Therefore, corners of the DA layer were avoided in this diagonal so as to exclude these singularity points. Figure 10 showcases the shear strain components in the asymmetric placement case, calculated at the maximum viscoplastic strain point along the diagonal line in the DA layer. It is worth noting that the elastic strain only dominates at lower temperatures, while the viscoplastic strain, consisting of both rate-independent plastic and rate-dependent creep strain, is the primary strain component during cycling.

Figure 11 shows the accumulated viscoplastic strain in the DA layer after one cycle during slow PCT. When compared with the fast PCT, accumulated viscoplastic strain is found to be higher in slow PCT with uniform distribution along the edges of the DA solder layer. However, it should be noted that one cycle in the slow PCT is 60 times longer than that in fast PCT. Therefore, the time dependent component of the inelastic strain will be higher in one cycle during slow PCT. Figure 12 shows the strain history at the maximum strained point in the diagonal of the DA during slow PCT. When compared with Figure 10, the viscoplastic strain is found to be higher and closer to the total strain in case of slow PCT.

Figure 13 illustrates the volume-averaged viscoplastic dissipation density ΔW_{vp} in one cycle during both fast and slow PCT. During the fast PCT, as shown in Figure 13a, ΔW_{vp} is observed to be minimum in the symmetric placement case, while it is almost equal in the remaining cases. It has also been observed in all the cases, as shown in Figure 13b, that ΔW_{vp} in one cycle is lower in the case of slow PCT when compared to the fast PCT. Therefore, the viscoplastic dissipation density when used with Morrow's lifetime model in (1), results in higher number of cyles to failure in slow PCT than in fast

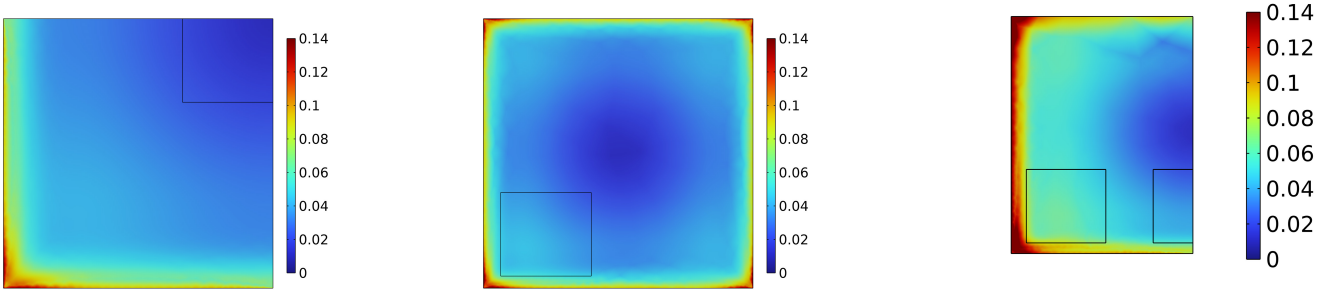


(a) Fast PCT.



(b) Slow PCT.

Fig. 13: Volume averaged viscoplastic dissipation density in the DA solder layer during fast and slow PCT respectively.



(a) Symmetric placement. (b) Asymmetric placement. (c) Full module.

Fig. 14: Accumulated viscoplastic strain in BA solder layer after one cycle during slow PCT.

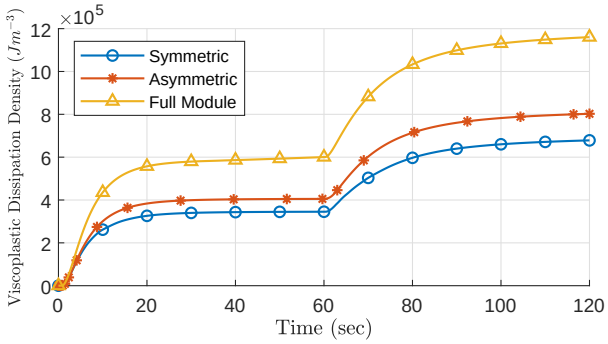


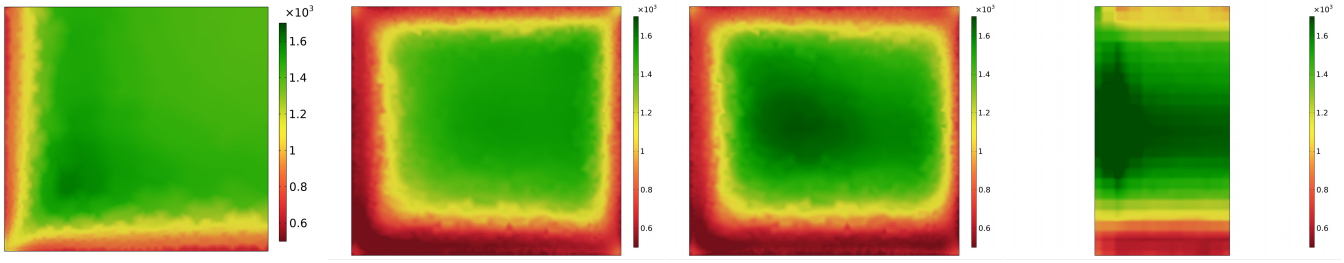
Fig. 15: Volume averaged viscoplastic dissipation density in the BA solder layer during slow PCT.

PCT.

2) BA Solder Layer: In the previous section, Figure 4b and 7 show that the BA solder layer goes through significant temperature cycling during slow PCT. This shows that the thermal load applied on the BA cannot be neglected. Figure 14 shows the distribution of the accumulated viscoplastic strain in one cycle during the slow PCT. When compared with the fast PCT, viscoplastic strain in the BA layer was found to be much higher during the slow PCT. It can also be observed from the figures that the corners are the most affected areas in the symmetric and the asymmetric placement cases. While in the case of the full module, the entire edge near the corner die is found to be highly strained. On comparing the viscoplastic dissipation density in Figure 15 it can be observed that it gets affected by both the placement and the quantity of the dies. The full module with three semiconductor dies accumulates the most viscoplastic dissipation density while the symmetric case, which has a die located farthest from the edges and corners has the least. The viscoplastic dissipation density in the BA layer during fast PCT was found to be much smaller in number, which is the reason why it is not shown in this paper.

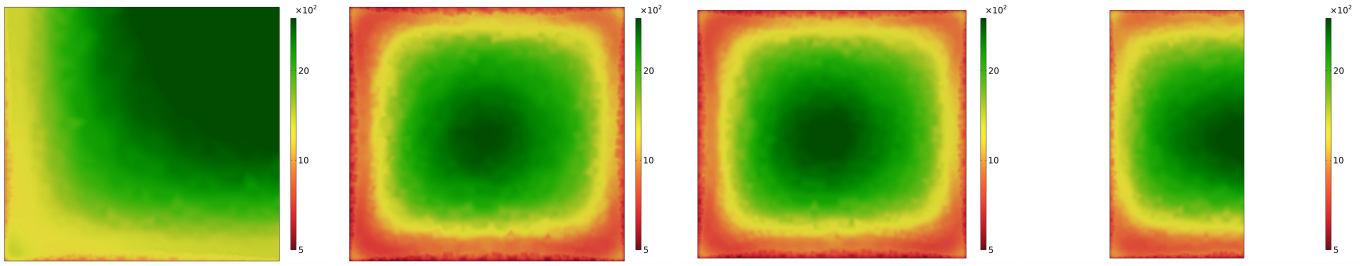
C. Cycles to Failure

Figure 16 shows the number of cycles to failure in the DA solder layer during fast PCT, which reveals lower levels in the number of cycles to failure near the edges and corners of the device. These areas also exhibit high accumulated viscoplastic strain. The placement of the die on the DBC plays a significant role in the DA lifetime. Comparison of the cycles to failure in symmetric and asymmetric placements, as shown in Figures 16a and 16b, demonstrates that the asymmetric placement results in a lower number of cycles to failure in the region closer to the corner of the DBC. However, the presence of a second die does not appear to have any significant effect on



(a) Symmetric placement. (b) Asymmetric placement. (c) Full module (Die 1). (d) Full Module (Die 2).

Fig. 16: Number of cycles to failure in DA solder layer during fast PCT.



(a) Symmetric placement. (b) Asymmetric placement. (c) Full module (Die 1). (d) Full Module (Die 2).

Fig. 17: Number of cycles to failure in DA solder layer during slow PCT.

the cycles to failure in this area. Figures 16c and 16d illustrate the cycles to failure in the full module, showing that die 1 (the corner die) experiences similar values in the region nearer to the corner of the DBC as in the asymmetric placement. However, the region in die 1 near die 2 shows reduced cycles to failure.

Figure 17 shows the number of cycles to failure in the DA layer during slow PCT. The lower number of cycles to failure is more uniformly spread around the edges when compared with the fast PCT. Furthermore, it can be observed that the DA solder layer during slow PCT exhibits a higher number of cycles to failure as compared with that during fast PCT. This finding is consistent with Figure 13, which shows a lower viscoplastic dissipation density in the case of slow PCT, resulting in higher cycles to failure. The figure highlights the significant role of the die placement on the DA lifetime.

V. Conclusion

This paper presents a comparative analysis of the effect of semiconductor die position and die numbers on the durability of the DA solder layers. The results show that the position of the die on the DBC has a significant effect on the lifetime of the DA layer, with the regions near the corner of the DBC experiencing a lower number of cycles to failure. The study used Anand's viscoplastic model to model the viscoplastic strain, which is the sum of the time-independent plastic and time-dependent creep strain, and employed FEM analysis. The viscoplastic dissipation density was then used in the Morrow's lifetime model to estimate the number of cycles to failure in the DA layer.

The thermal analysis revealed that the heat distribution varies with the position of the die on the DBC, with regions of the die closer to the corner of the DBC experiencing higher temperatures than other regions. Furthermore, the temperature gradient on the die surface is higher in the fast PCT compared to the slow PCT. This results in a non-uniform distribution of the viscoplastic strain and, consequently, non-uniform distribution of the cycles to failure in the DA layer. On the other hand, the temperature distribution in the slow PCT is more uniform, resulting in uniform distribution of the viscoplastic strain and cycles to failure in the DA layer.

The study also found that the viscoplastic dissipation density in one cycle is lower in the slow PCT, leading to higher cycles to failure when compared to the fast PCT. Additionally for all the cases, there was a significant increase in viscoplastic dissipation density in the BA solder layer during the slow PCT when compared to the fast PCT.

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