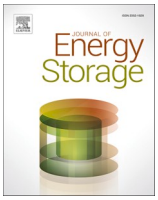
Journal of Energy Storage 66 (2023) 107424

Contents lists available at ScienceDirect

Journal of Energy Storage

journal homepage: www.elsevier.com/locate/est



Research papers

A new method to perform lithium-ion battery pack fault diagnostics – Part 3: Adaptation for fast charging

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ARTICLE INFO

Keywords:
Li-ion batteries
eVTOL
Electric aircraft
Fault diagnosis
Incremental capacity
Fast charging

ABSTRACT

Electric Vertical Take-Off and Landing (eVTOL) aircraft are expected to become ubiquitous in the future Urban Air Mobility (UAM) landscape. Several eVTOL aircraft propelled using Lithium-ion batteries are under development. However, despite the early spotlight, the manufacturers need to ensure safe long-term operation of the vehicles including strict checks on battery-related hazards. On the other hand, fast charging of eVTOL batteries is crucial to enable multiple flights per day and justify the economics of UAM. This work is aimed at contextualising battery safety for eVTOL through the modification of a battery fault diagnosis algorithm for fast charging. The algorithm was developed in Parts 1 and 2 of the paper to use the charging cycle data for detecting disconnection faults but tested only for low charging currents. This paper adapts the algorithm for fast charging through a novel technique termed as Partial Incremental Capacity (PIC). The PIC method was developed using experiments at single cell and supercell level before integrating it into the algorithm. Finally, the fault detection ability of the adapted algorithm was validated using a real-life eVTOL battery module. Thus, the updated version of the algorithm facilitates fault diagnosis while charging fast, making it ideal for implementation in eVTOL.

1. Introduction

The year 2021 witnessed major developments in electric aviation, particularly in the Urban Air Mobility (UAM) landscape. The UAM industry received investments in excess of $12 billion, with more than 6000 pre-orders placed for Electric Vertical Take-off and Landing (eVTOL) vehicles [1]. Several eVTOL manufacturers have emerged with battery-propelled vehicles at different stages of development and certification and expect to commence operations this decade [2,3]. Being at a nascent stage, the industry needs to match the safety standards of civil aviation by addressing the safety issues associated with Lithium-ion batteries [4–6]. Moreover, from an operational perspective, these aircraft will be required to make multiple short-haul journeys daily, thus making fast charging imperative to their success [7]. While both these issues are common with the automotive industry, the specifics of UAM offer unique advantages. For instance, UAM standards currently under development are expected to deliver a uniform consensus on the design and implementation of charging infrastructure [8,9]. This could create opportunities to systematise the use the charging phase for collecting battery data and identifying battery health metrics related to performance as well as safety.

This work aims to exploit the uniqueness of the UAM ecosystem to address battery safety while also respecting the requirement for fast charging. The paper is the third in a three-paper series presenting a novel battery fault diagnosis algorithm. The algorithm will be deployed to diagnose faults in the battery during the charging phase before each flight. Considering a disconnection fault, Part 1 covered the working principle of the algorithm as well as experimental testing of the algorithm at complexity level-1, i.e. under steady conditions. In Part 2, the cell-to-cell transferability of the algorithm was proven using a module composed of a new cell type. Moreover, the testing was extended to complexity level-2 by introducing a variation in State Of Charge (SOC) range and temperature during different charging cycles of the battery. Conducting experimental tests using a lab-based module and a real-life aerospace module composed of 88 cells, the algorithm was found to effectively diagnose faults under steady conditions in Part 1. The tests conducted in Part 2 revealed that the algorithm performance is optimal when the module is maintained at a constant temperature during different charge cycles. Nevertheless, several strategies were identified to overcome this limitation and hence, it should not be a major obstacle

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https://doi.org/10.1016/j.est.2023.107424
Received 18 January 2023; Received in revised form 21 March 2023; Accepted 11 April 2023

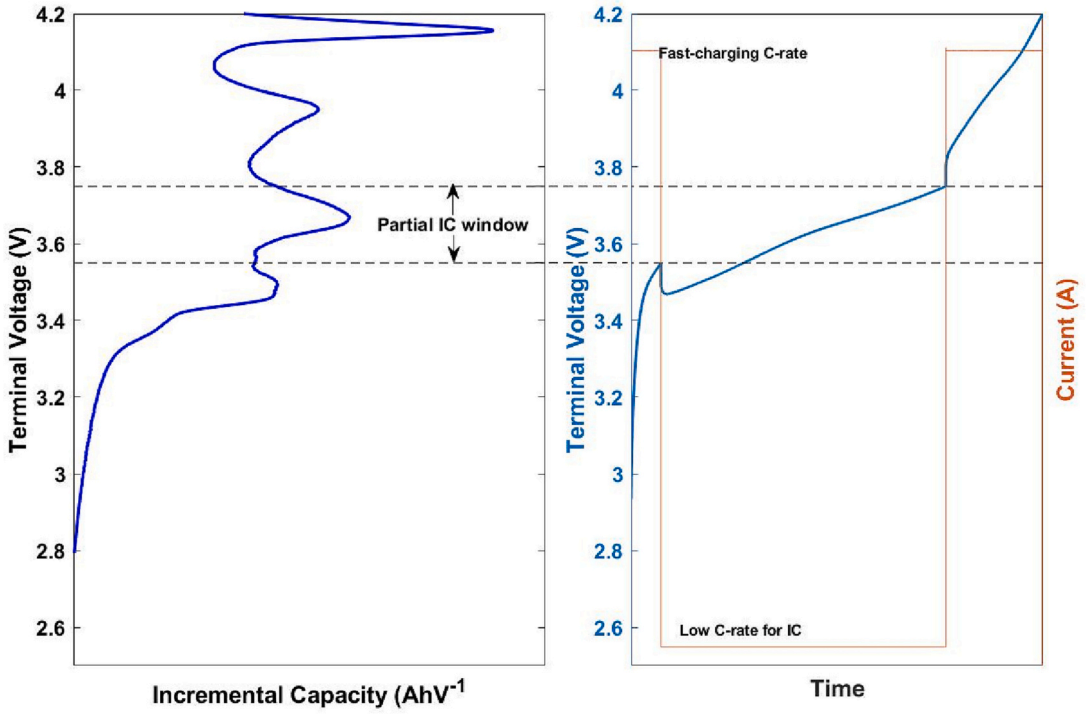

Fig. 1. Schematic representing the proposed Partial IC technique using two different C-rates.

in implementing the algorithm.

While the results provided useful insights into the working and applicability of the algorithm, the experiments in Parts 1 and 2 were conducted using a maximum C-rate of C/3, i.e. current that would charge the battery in 3 h. Such a long charging time might not suit the operational requirements of the UAM industry. Therefore, in this paper, the algorithm was extended to complexity level-3, which includes current that could charge the battery to more than 80 % SOC in less than 1 h. As shown in Parts 1 and 2, Incremental Capacity (IC) analysis is a crucial component of the algorithm. IC is a well-known technique in electrochemistry. It is used in battery research to relate electrode-level phenomena with cell-level measurements [10–18]. However, a key limitation of IC analysis is the requirement of cycling the cells at C-rates as low as C/25, which are unrealistic for real-life implementation. At higher C-rates, IC curves undergo significant loss of extractable features [19,20], which could limit the ability of the algorithm to detect faults. In addition, while IC analyses with C-rates as high as C/3 have been reported for the evaluation of State Of Health (SOH) [21,22], most of the studies were limited to single cell level with a handful of studies at module or pack level [23–25].

This paper addresses the C-rate limitation of IC analysis, and hence the fault diagnosis algorithm, through a novel method termed as "Partial IC (PIC)". The method involves switching the charging current during fast-charging to a lower C-rate that is suitable for partial extraction of IC features, i.e. specific features at known terminal voltage values. This is followed by rapid restoration of the higher C-rate. Thus, the PIC method allows for a compromise between charging time and quality of the extracted IC metrics. The paper describes the development of the PIC method at single cell level followed by implementation at supercell and module levels to assess its viability for fault diagnosis. Finally, the PIC method is integrated into the algorithm and validated experimentally using a real-life battery module. The findings are expected to uphold the relevance of the presented algorithm for real-life implementation in eVTOL batteries.

2. The proposed Partial IC methodology

A typical IC curve with four distinct IC peaks is shown in Fig. 1. Each peak in IC curve exists in a specific voltage range. Therefore, it was hypothesised that considering a predefined window during a charging process and reducing the C-rate to a lower value only over this window would enable capturing the IC features while achieving an acceptable charging time. This proposed method is termed *Partial IC* (PIC) and represented schematically through the voltage v/s time plot in Fig. 1. Selecting a particular peak for implementing PIC, the voltages corresponding to the two minima occurring before and after the peak would be determined experimentally as the voltage window. In a real-world charge scenario, the charging current will be switched from fast charge protocol to low C-rate at the start of this predefined voltage window. As soon as the voltage window pertaining to the selected IC peak is covered, the current will be switched back to the fast charge protocol.

Two methods were considered for performing the C-rate switching: (i) raw method and (ii) Direct Current Resistance or Internal Resistance (DCR or IR) compensation method. The raw method involved a direct C-rate reduction upon reaching the identified voltage window. While being simple to implement, it may not offer an optimal compromise between charge duration and quality of the data for ICA. This is because the reduction in current dependent component of the overpotential would cause a drop in the cell voltage. Thus, the charging at the lower C-rate would begin at a voltage less than the identified start point of the selected voltage window. Consequently, the lower C-rate would prevail for a wider voltage window than expected and increase the overall charging time. To overcome this limitation, the DCR-compensation method was introduced. In this method, it was assumed that the overpotential is proportional to the applied current. The C-rate switch was conducted at a higher voltage than the absolute start point of the voltage window. The new voltage for performing the C-rate switch was estimated using the overpotential, which was calculated using DCR available from high power pulse test (HPP). This method is expected to reduce the time spent charging at lower C-rate that would in turn reduce the overall charge duration. For detailed explanation of the method used

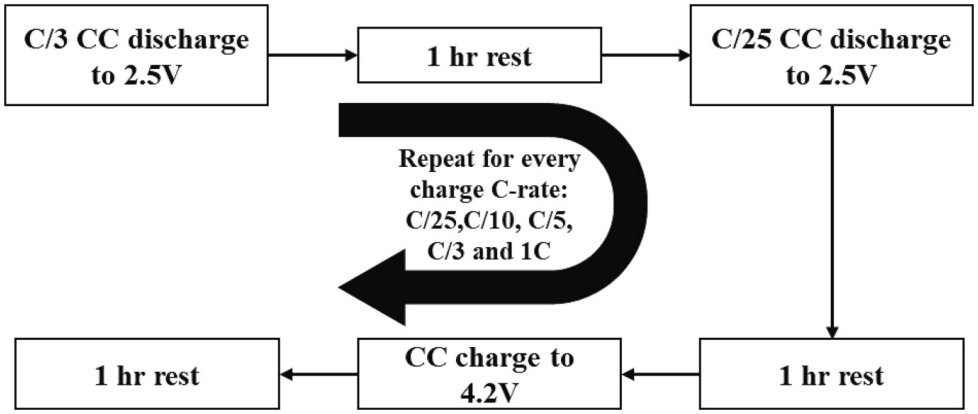

Fig. 2. Employed test profile for CC charge at various C-rates.

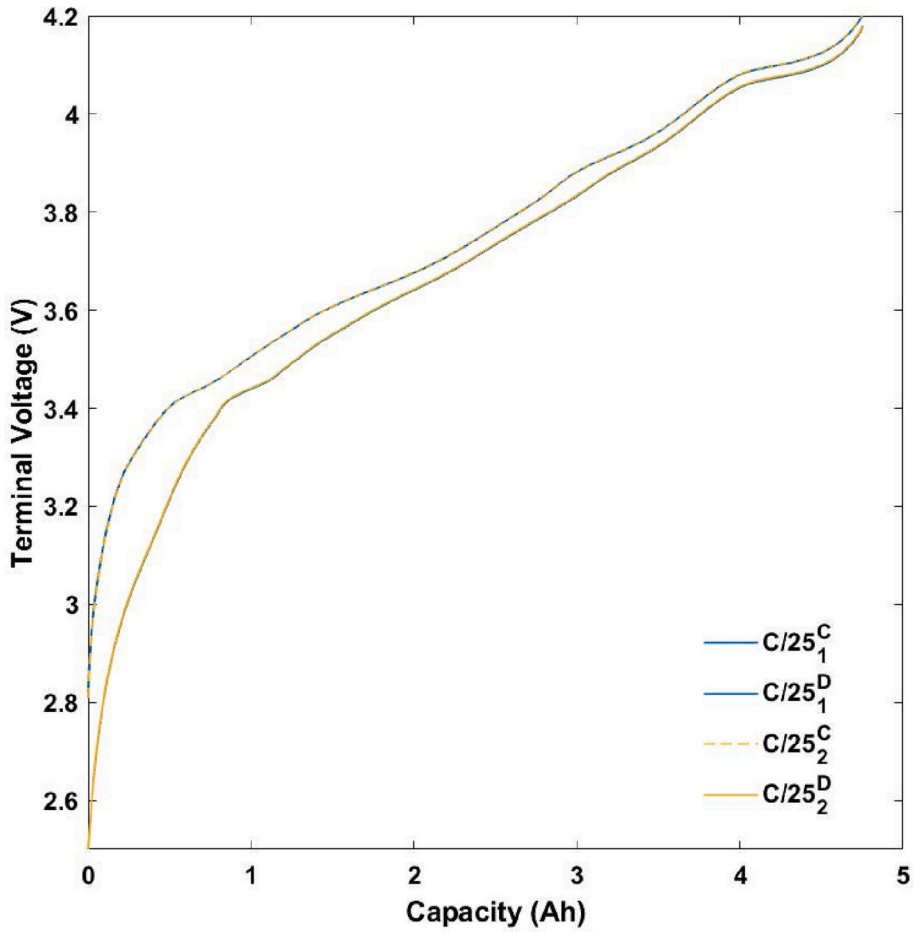

Fig. 3. Voltage v/s capacity curves for single cells corresponding to C/25 charge and discharge.

to perform IC analysis and extract IC features, the readers are referred to Part 1.

In Parts 1 and 2, a disconnection fault was used to validate the algorithm performance. It is intuitive that even at a high C-rate, a disconnection fault would produce a significant change in IC signature and could be captured using the fault diagnosis algorithm. However, to be globally applicable, the algorithm is expected to detect a broader array of faults. Previous results have indicated that compared to the disconnection defect considered in this work, milder fault conditions such as overcharge [26] and overtemperature [27] produce finer changes in IC features. These changes were observable at C-rates in the range of C/5 to C/3 but would be lost as higher rates are utilised. Therefore, using the PIC method during fast-charging would enable tracking such minor changes, thus allowing the algorithm to capture a broader range of faults while charging the battery within acceptable time. Moreover, analysis of fine changes in the IC signature was shown to facilitate battery state estimation and prognostics [16,17,28]. Thus, the PIC method is a step towards expanding the algorithm beyond fault diagnosis towards a holistic battery monitoring approach.

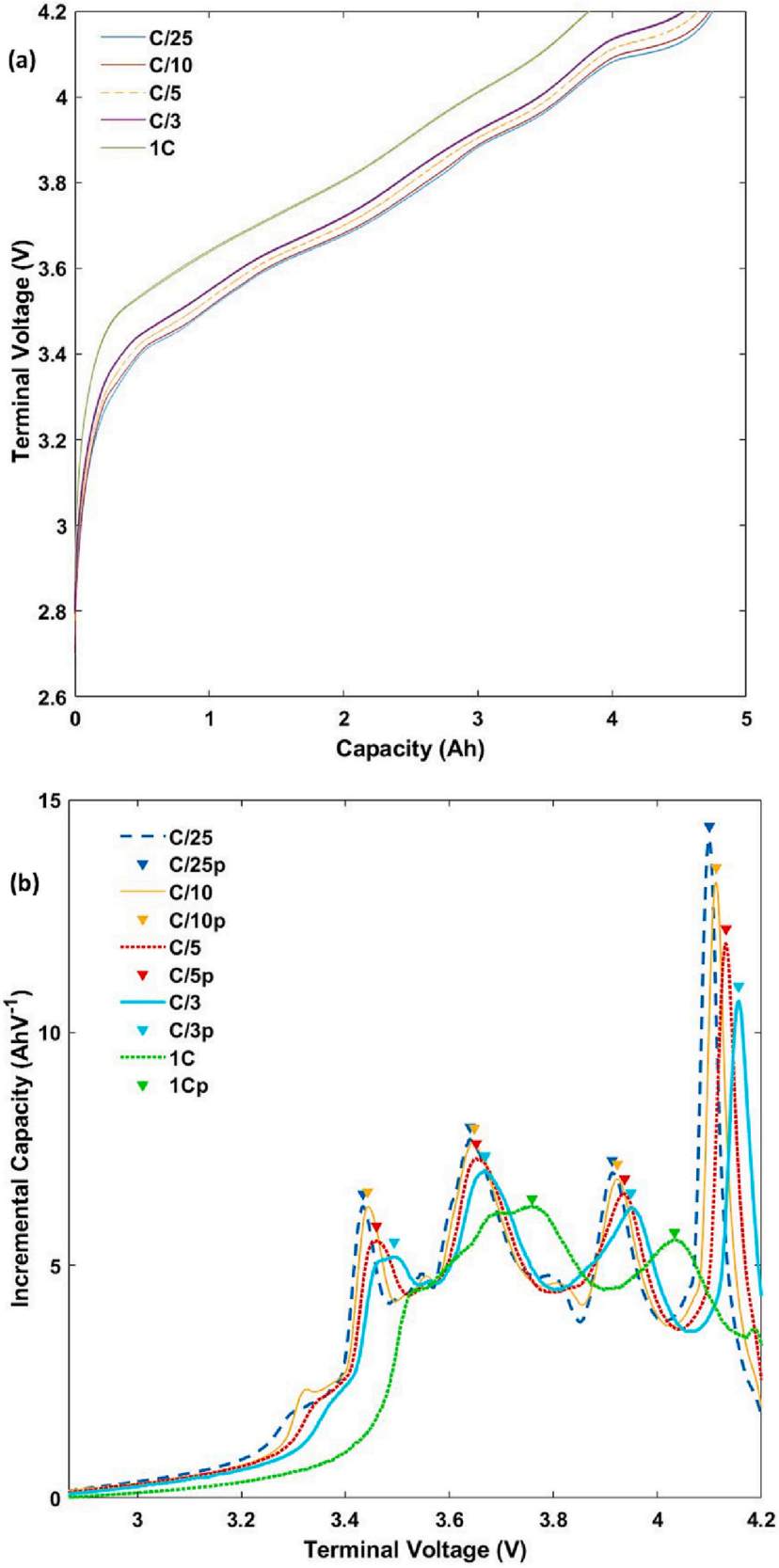

Fig. 4. (a) Voltage v/s capacity curves and (b) Single cell incremental capacity plot corresponding to charge segments at various C-rates for single cells.

Table 1
Characteristics of single cell corresponding to various C-rates.

C-rate	Charge capacity (Ah)	Charge energy (Wh)	IC peak intensity (Ah/V)	IC peak location (V)	Charging time (hours)
C/25	4.75	17.79	7.694	3.640	23.75
C/10	4.73	17.72	7.623	3.645	9.45
C/5	4.64	17.46	7.302	3.652	4.84
C/3	4.53	17.12	7.021	3.668	2.84
1C	3.83	14.53	6.271	3.756	0.80

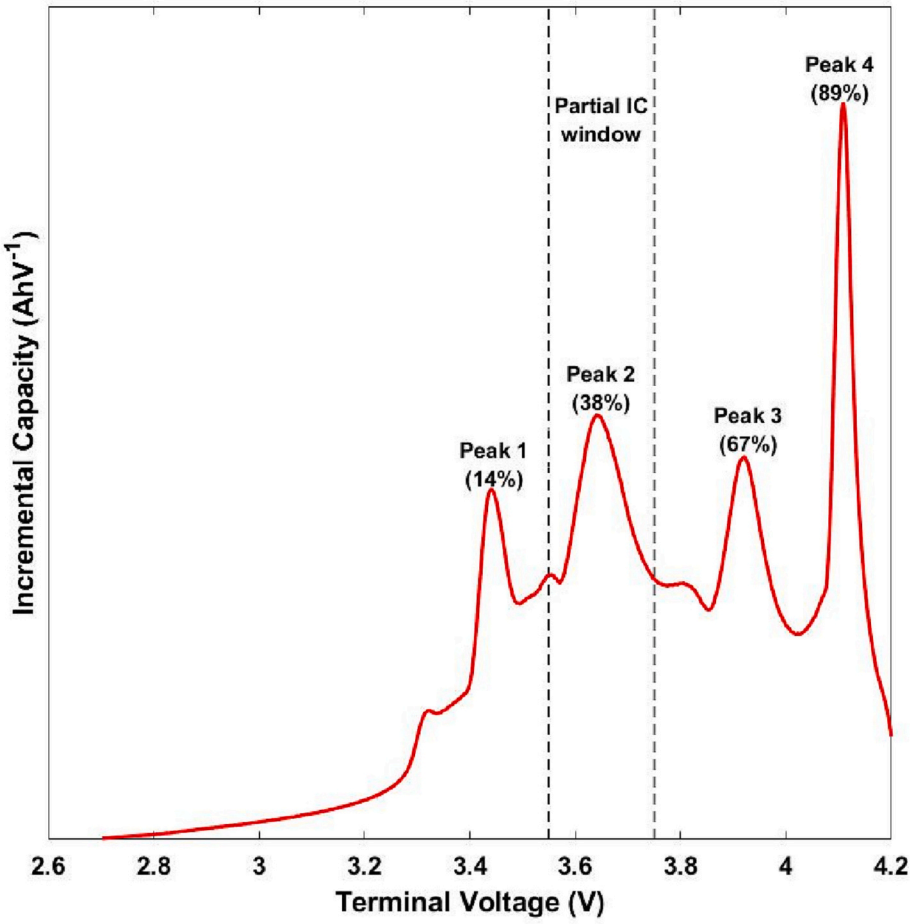

Fig. 5. Peak selection for partial IC based on SOC corresponding to each peak.

3. Experimental methodology

Samsung INR21700 48X and 40T cells, tested extensively in Parts 1 and 2 were used in this work. Initial testing using 48X cells was conducted at two Device Under Test (DUT) levels i.e. single cell and supercell, to understand the influence of C-rate on IC features. Based on these results, the PIC method was developed and implemented at both DUT levels, followed by assessment of the PIC method for fault diagnosis at supercell level. The fault detection capability of the PIC method was further assessed at module level, for both 48X as well as 40T modules. Finally, the PIC method was integrated into the algorithm and tested using a real-life battery module. The procedures corresponding to each test are discussed below. For details of the test setup and equipment, readers are referred to Pats 1 and 2.

3.1. Standard cycling

For implementation of ICA during the charge regime, individual cells as well as the 8P supercell were cycled at 5 different C-rates: C/25, C/10, C/5, C/3 and 1C. Fig. 2 shows a schematic of the employed testing procedure. A constant current (CC) regime was employed until the upper voltage limit of 4.2 V was reached. Before every charge cycle, the cell was discharged at the manufacturer recommended C-rate of C/3 in a CC regime till the lower cut-off voltage of 2.5 V was reached. Following the C/3 discharge, the cells (and supercell) were further discharged at C/25 till the lower cut-off voltage to ensure the same beginning of charge state for every charge cycle. During these tests, the current, voltage and temperature data were recorded at a constant frequency of 1 Hz. The collected data was analysed using MATLAB 2021B.

The OCV v/s SOC plot is used to understand the thermodynamic voltage evolution of a cell against its SOC. Given that conducting a GITT test is time consuming, a pseudo OCV plot was considered instead. This is plotted as the average of charge and discharge voltage v/s SOC plots at a very low C-rate [29]. The discharge and charge curves corresponding to a C-rate of C/25 are shown in Fig. 3 for 2 48X cells. The curves from the 2 different cells overlap precisely. The cell terminal voltage showed a steep rise to approximately 3.4 V, accumulating less than 10 % of the total capacity during this regime. In the region corresponding to the

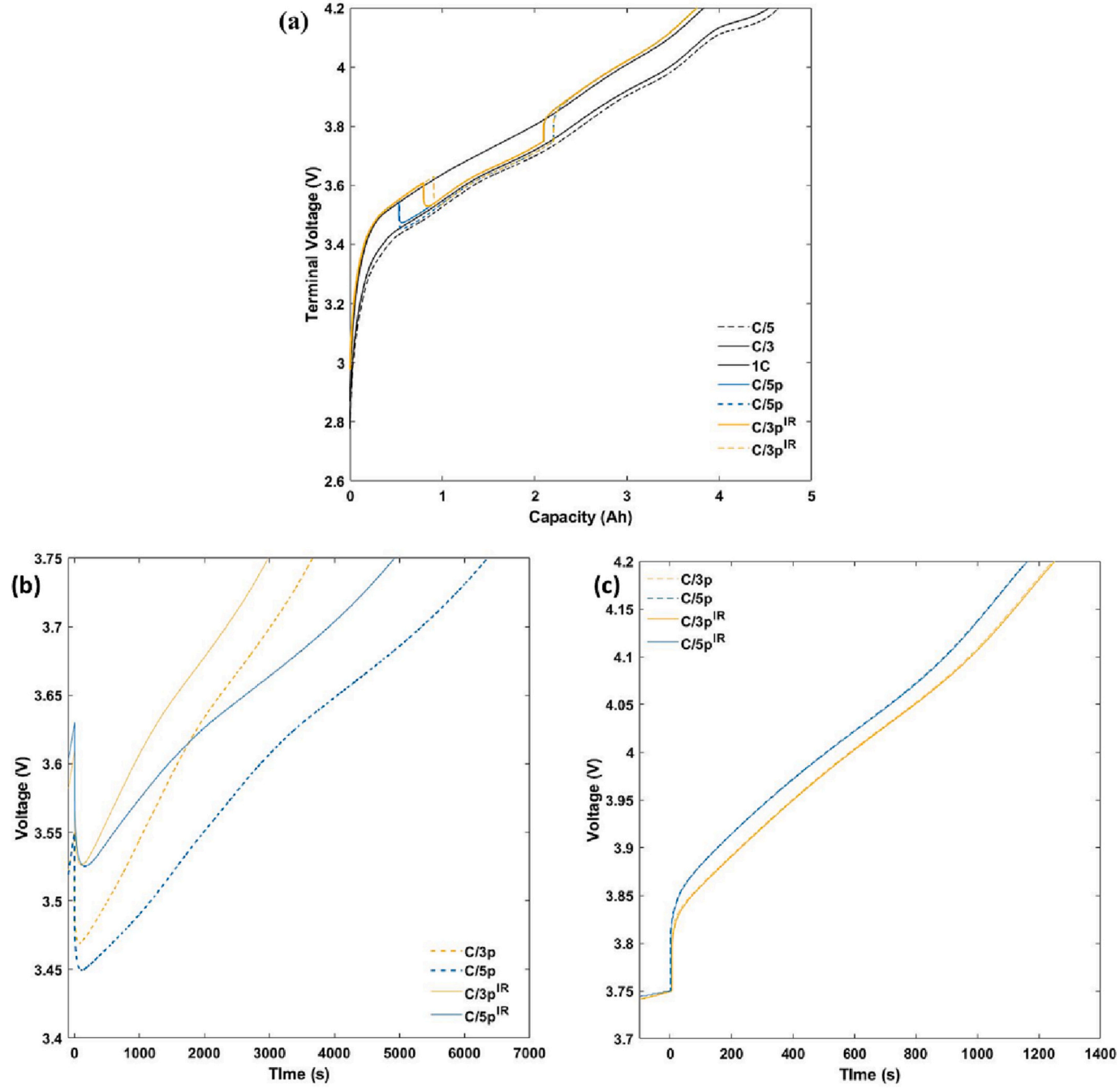

Fig. 6. (a) Voltage v/s capacity plot corresponding to partial IC experiments for single cell; (b) and (c): Voltage v/s time plot corresponding to C-rate switches during partial IC experiments for single cell. Note: Curves for constant current charging are also shown for reference.

Table 2
Characteristics of single cell corresponding to partial IC at C/3 and C/5. Note: Characteristics for CC charge segments are listed for comparison.

C-rate	Charge capacity (Ah)	Charge energy (Wh)	Charging time (hours)	Maximum temperature (°C)
C/5	4.64	17.46	4.84	28.9
C/3	4.53	17.12	2.84	30.3
1C	3.83	14.53	0.80	31.4
C/5 raw	3.76	14.09	2.19	31.1
C/3 raw	3.78	14.21	1.45	31.1
C/5 DCRC	3.75	14.11	1.87	31.7
C/3 DCRC	3.75	14.15	1.33	32.1

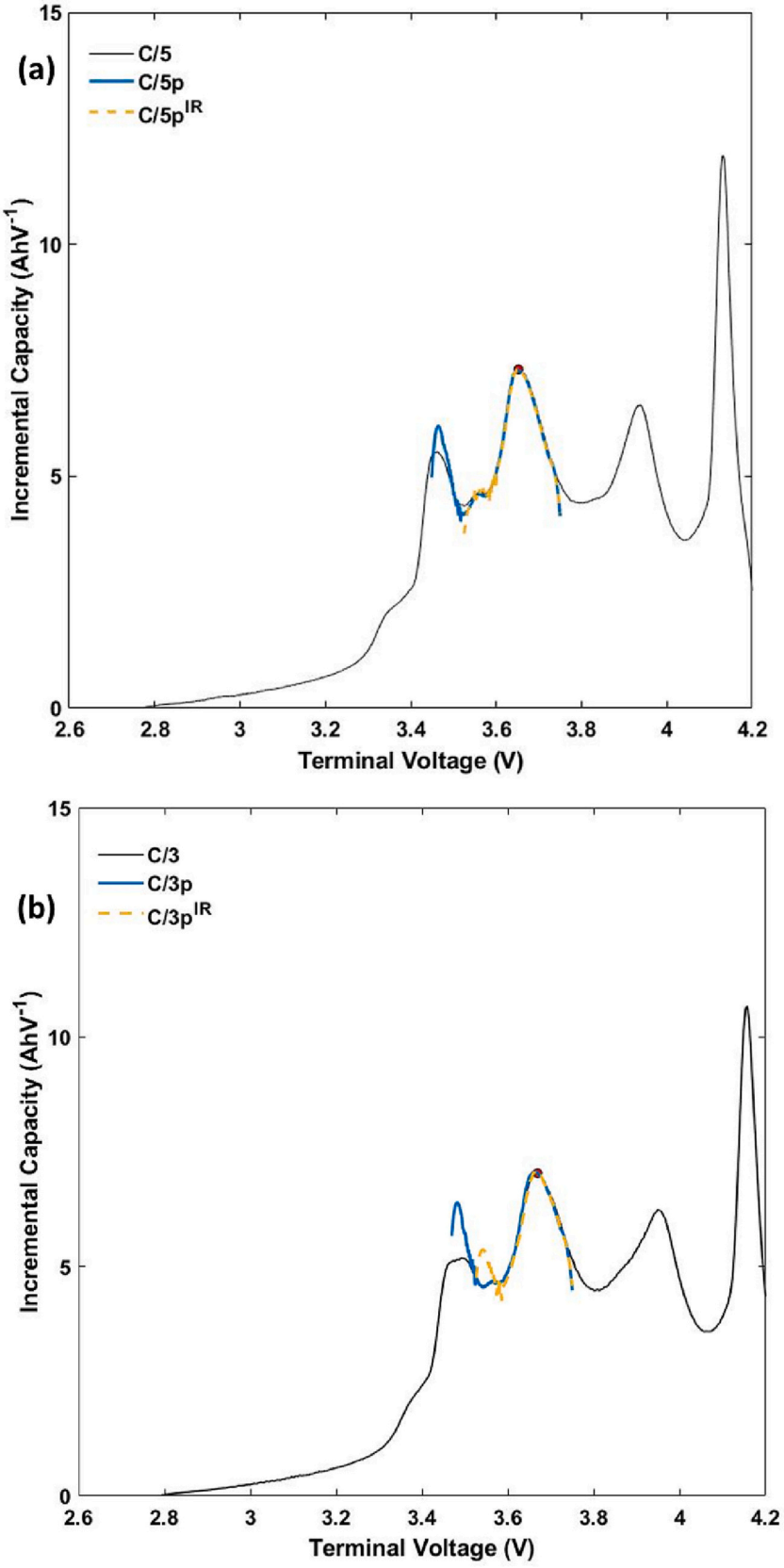

Fig. 7. Partial IC curves for single cell at (a) C/5 and (b) C/3. Note: IR indicates IR or DCR-compensated PIC.

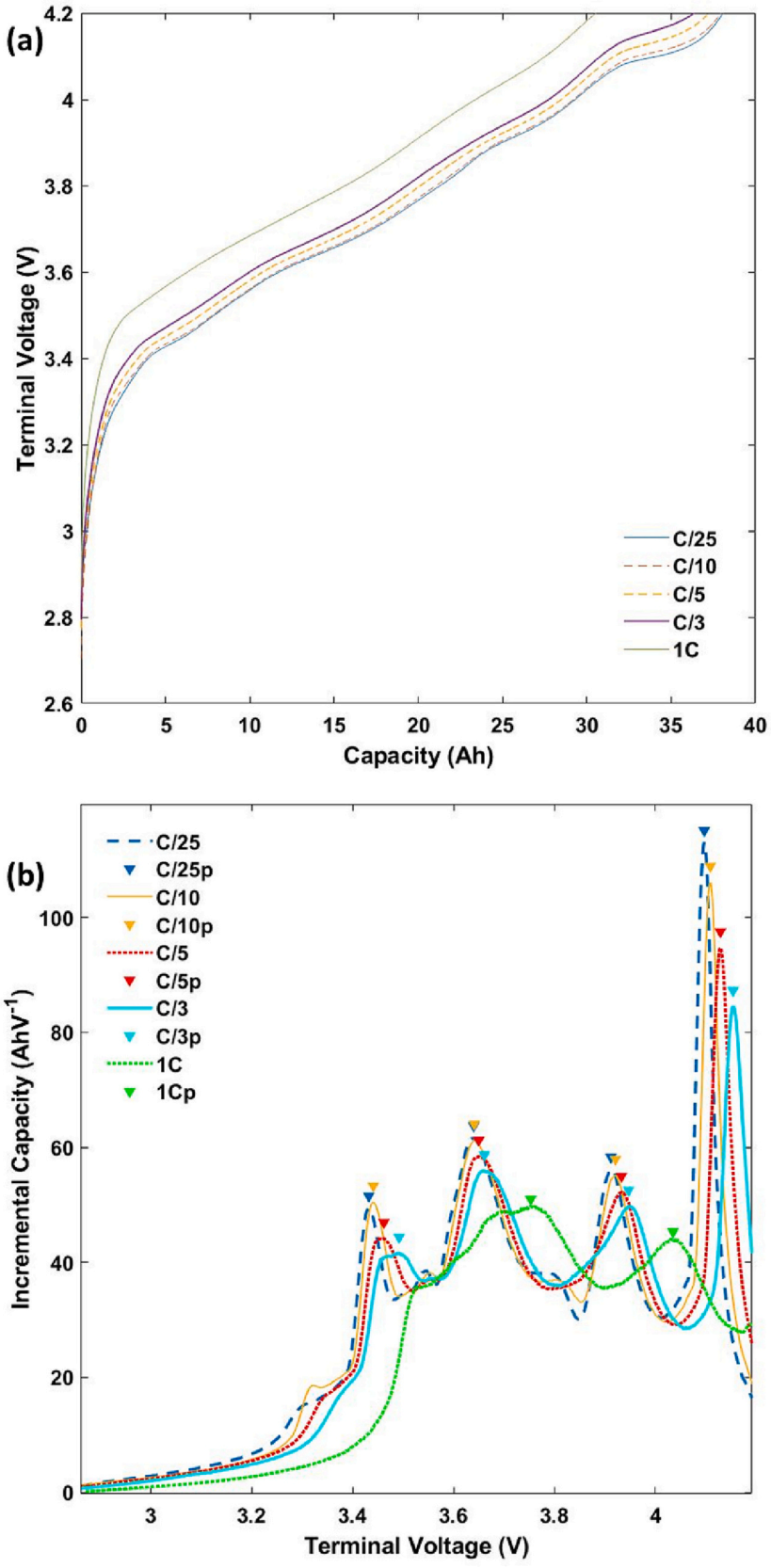

Fig. 8. (a) Voltage v/s capacity curves and (b) IC plots corresponding to charge cycles at various C-rates for 8P supercell.

Table 3
Characteristics of 8P supercells corresponding to various C-rates. Note: values from single cell tests are scaled up and represented in brackets.

C-rate	Charge capacity (Ah)	Charge energy (Wh)	IC peak location (V)	IC peak intensity (Ah/V)	Charging time (hours)	Maximum cell temperature (°C)
C/25	38.07 (38.00)	142.45 (142.29)	3.640	61.631	23.79	27.1
C/10	37.96 (37.82)	142.18 (141.76)	3.641	61.248	9.88	27.7
C/5	37.22 (37.13)	139.94 (139.65)	3.650	58.432	4.83	28.7
C/3	36.36 (36.26)	137.12 (136.93)	3.661	55.911	2.84	29.5
1C	30.52 (30.65)	115.82 (116.26)	3.753	49.711	0.79	31.6

upper voltage limit, 80 % of the cell capacity is accumulated upon charging the cell to 4 V. This is noteworthy as in real-life applications, battery packs are charged only up to 80–90 % of the maximum capacity during a fast-charging process. Given the low C-rate, the curve was able to capture transitions in the slope of the voltage, which pertain to different chemical reactions and phase transitions occurring at the electrode level during the charge/discharge process.

The CC charging data collected at different C-rates was used to produce IC curves. The IC peaks were analysed and voltage windows were identified to establish the current scheme for PIC. Following this, the developed PIC method was implemented at single cell and supercell level to assess its feasibility. Furthermore a supercell with a disconnection fault was charged using the PIC method to assess the ability of the PIC technique to capture faults. The disconnection fault was simulated by removing one cell from the 8P supercell.

3.2. PIC at module level

The proposed PIC technique was implemented for in-house modules having an 11s8p configuration. Modules assembled using 48X as well as 40T cells were tested to prove the PIC method for both cells. During the tests, the voltage of each 8P supercell was monitored using a Circuit Monitoring Board (CMB) and communicated to the cycler via a Controller Area Network (CAN) bus. To initiate the C-rate switch to the lower current, the highest supercell voltage logged using the CMB was used as the trigger. Similarly, at the end of the PIC window, the lowest supercell voltage was used to trigger the C-rate switch back to the fast charge regime. This ensured that requisite voltage window was covered at the lower C-rate for each supercell, thus safeguarding against supercell-to-supercell variation. Hence, degradation or defects causing voltage imbalance between the supercells will not prevent the Partial IC method from extracting the required IC metrics.

3.3. Fault diagnosis algorithm assessment using real-life battery module

Similar to the testing conducted for complexity levels 1 and 2 in Parts 1 and 2, the fault diagnosis algorithm was validated after integrating the developed PIC charging strategy for an aerospace module composed of 48X cells. The PIC charging strategy was implemented to charge the module before and after fault introduction in the two phases of testing, as outlined in Part 1. Three test cases were considered: DF1, DF2 and DF3 with one, two and three faulty supercells in the module respectively (DF: disconnection fault). Each faulty supercell had one cell physically disconnected. The supercell metrics, i.e. DCR and IC peaks were evaluated from the charging data and the fault parameters were calculated using the algorithm. Finally, the performance of the algorithm at complexity level-3 was compared to level-1 and 2 results.

4. Results

4.1. Single cell

The terminal voltage v/s capacity curves for all the considered C-rates are shown in Fig. 4(a). The plot consists of data corresponding to two repeats. The overlap between the data from the two different cells indicates consistency in the manufacturing process of the cells. Compared to the lower C-rates, a slight observable departure between the curves corresponding to the two cells occurs at 1C, which indicates the difference in their internal resistance. Moreover, the curves for 1C are distinct from the other C-rates due to the higher overpotential. As the C-rate increases, the transitions in voltage slope, captured at low C-rates, are lost. Moreover, a maximum temperature of 31.6 °C was observed during 1C charging. This is significantly higher than the 29.5 °C observed at the next fastest C-rate of C/3. For all the remaining C-rates, the maximum temperature was below 29 °C compared to the chamber set point of 26 °C. The IC-curves obtained from the CC charge cycles are plotted in Fig. 4(b). Four distinct peaks are observable with a few minor features. As the C-rate increased, there is a visible loss of features. Subtle transitions observed in the curves corresponding to C/25 and C/10 at approximately 3.3 V and 3.75 V are lost at higher C-rates. Nevertheless, the peak definition at C-rates of C/3 and C/5 was qualitatively comparable to lower C-rates. For each C-rate, the peaks were identified using identical parameters in the MATALB findpeaks function and are marked in Fig. 4(b). All the major peaks were recognisable till a C-rate of C/3. This reconciled with previous studies where IC analysis at similar C-rates were used for battery state estimation [21,22]. The IC curve at 1C is the most distinguishable. While showing a unique rightward shift due to the higher overpotential, the peak pattern shared across all the lower C-rates was lost. Without altering the peak identification parameters, only Peaks 2 and 3 were identified. Moreover, both the peaks showed a significant rightward shift.

Table 1 lists the metrics obtained from CC charging of single cells at different C-rates. As expected, the charge capacity and energy reduce with increasing C-rate. Charging times pertaining to each charge cycle are also listed and in agreement with the expected values as per the C-rate values based on nominal cell capacity. The data corresponding to 1C, which is most relevant to fast charging applications, indicates that only 81 % of the cell capacity was accumulated during the CC charge. The IC peak intensity and location corresponding to Peak 2, also listed in the table, quantitatively indicate the rightward shift and intensity reduction with increasing C-rate. Based on the qualitative and quantitative analysis, it is evident that up to C/3, the IC curves maintained similarity with the recommended C-rate for IC analysis, i.e. C/25. However, the curve at 1C showed a significant departure and hence is not directly usable for useful IC feature extraction.

4.1.1. Partial IC development

The 4 major peaks were compared based on the accumulated capacity as shown in Fig. 5. This is crucial from application perspective, as real-life charging may neither starts at 0 % SOC nor charges to the full 100 % SOC in every charging operation. Therefore, for the considered cell, peaks 1 and peaks 4 occurring at approximately 14 % and 89 % SOC were deemed unsuitable for consistent implementation of PIC. Among the remaining peaks, only Peak 2 was considered in this work.

To maximise the probability of capturing the IC Peak 2, which occurs at a voltage of 3.7 V, a wide voltage window of 3.55–3.75 V was selected for the purpose of PIC, also shown in Fig. 5. For the raw PIC, the C-rate was switched to C/3 or C/5 at a voltage of 3.55 V. For the DCR-compensated PIC, DCR values corresponding to an SOC of 20–40 % were evaluated using Hyper Pulse Power (HPP) tests. The HPP test result indicated an average DCR value of 24.92 mΩ. Therefore, the voltage for C-rate switching was offset using this value as per Eq. (1).

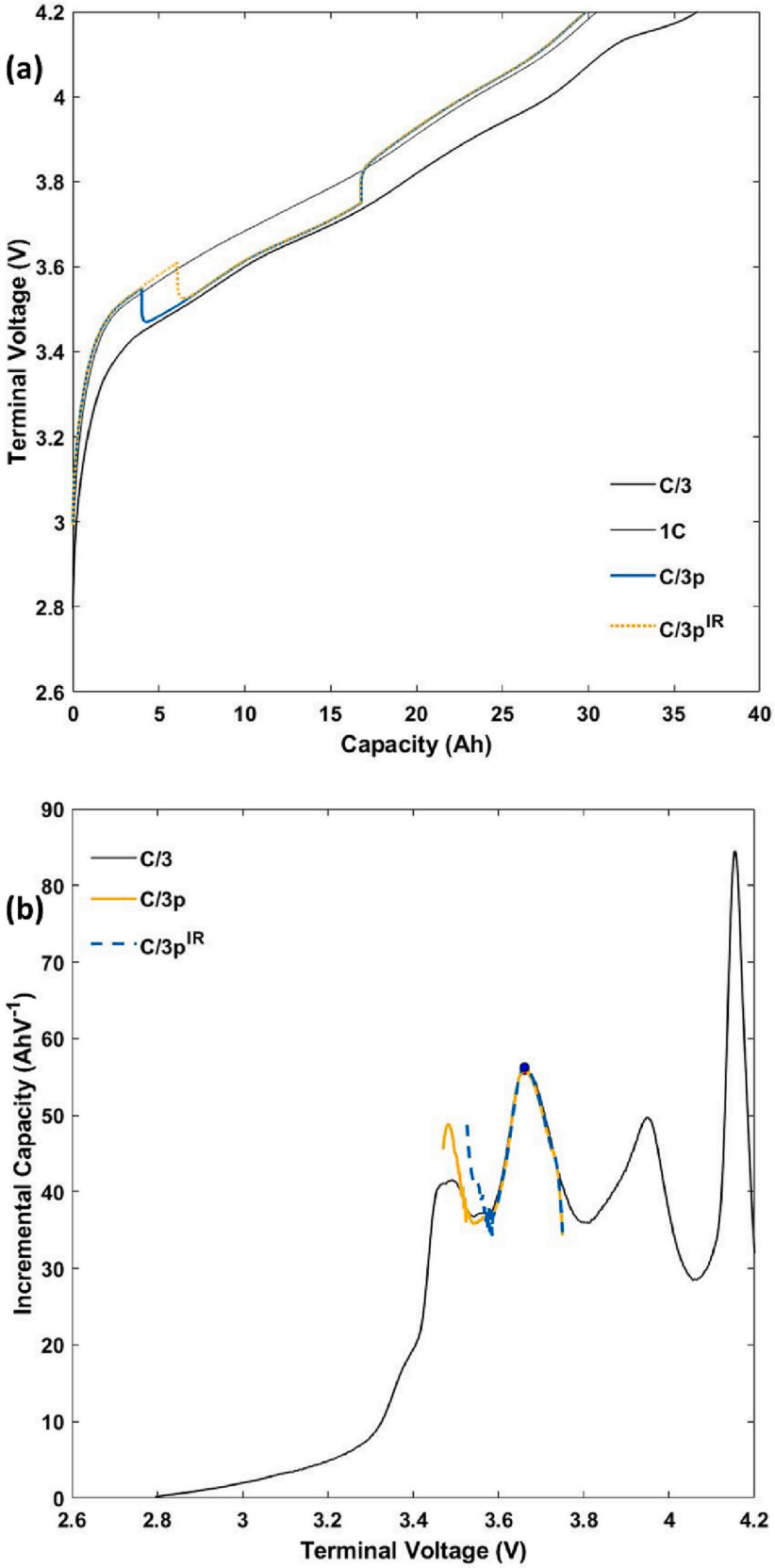

Fig. 9. (a) Voltage v/s capacity curves and (b) IC plots corresponding to partial IC based charge cycles for 8P supercell. Note: Curves for constant current charging are also shown for reference.

Table 4
Characteristics of 8P supercells corresponding to partial IC at C/3. Note: Characteristics for CC charge segments are listed for comparison.

C-rate	Charge capacity (Ah)	Charge energy (Wh)	IC peak location (V)	IC peak intensity (Ah/V)	Charging time (hours)	Maximum temperature (°C)
C/3	36.36	137.12	3.661	55.911	2.84	29.5
1C	30.52	115.82	3.753	49.711	0.79	31.6
C/3 raw	29.90	112.50	3.661	56.039	1.44	31.8
C/3 DCRC	29.85	112.56	3.661	56.257	1.33	31.8

$$V_{switch} = V_{lower} + R_{DC}\cdot(A_{1C} - A_{C-rate}) \quad (1)$$

where V_{switch} is the voltage at which the C-rate was changed, V_{lower} is the lower voltage limit for the selected voltage window (=3.55), R_{DC} is the calculated DCR, A_{1C} is the current corresponding to 1C and $A_{C\text{-}rate}$ is the current for the C-rate.

The resultant values for C-rate switching for C/5 and C/3 were 3.65 V and 3.63 V respectively. Applying a buffer, the switch was performed at 3.63 and 3.61 V. It is noteworthy that even in an aged state of the cell, the DCR-compensated method will allow for precise tracking of the IC peak. This is because the cell impedance would increase with the degradation of the cell. Therefore, upon reducing the C-rate, the voltage of an aged cell would drop to a lower value compared to the pristine state of the cell, thus covering the required voltage window at the lower C-rate.

4.1.2. Partial IC results

The resulting voltage v/s capacity curves for both the PIC methods are shown in Fig. 6(a). Upon reducing the C-rate, there was an immediate voltage drop due to the reduction in current dependent overpotential. To compare the voltage trends for different cases, the voltage was plotted against time, as shown in Fig. 6(b) and (c). For the raw PIC at both C-rates, the voltage dropped for approximately 2 min to 3.47 V (C/3) and 3.45 V (C/5). This was followed by a consistent rise. On the other hand, the DCR-compensated experiments resulted in voltage drops to approximately 3.53 for both C-rates. These are below the target voltage window of 3.55–3.75 V and hence considered suitable for IC analysis corresponding to peak 2.

Table 2 shows the capacity, overall charge duration and temperature evaluated from the data pertaining to PIC charging schemes. The constant current charge data for both C-rates are also listed for comparison. The capacity and energy for all the PIC charging cases were lower than the 1C CC charge. This was attributed to an anomaly in cycling method: the C/25 discharge step was not performed before the PIC charging, which resulted in different starting SOC. However, the energy and capacity were both within 3 % as compared with 1C CC charging. Therefore, the difference was considered negligible. In terms of charging time, raw PIC showed an increase of 83 min and 39 min for C-rates of C/5 and C/3 respectively compared with 1C CC charging time of 48 min. On the other hand, the DCR- compensated PIC had charging times 64 min (C/5) and 32 min (C/3) greater than 1C charging time. Therefore, the DCR-compensation resulted in a reduced charging time with respect to raw PIC and is therefore better suited for commercial applications. For the raw PIC, there was an increase in temperature compared to CC charge at both C-rates. Nevertheless, despite the longer charge duration allowing for greater heat generation, the measured rise was slightly lower than the 1C CC charge. On the other hand, the DCR-compensated PIC resulted in a temperature rise greater than the 1C charge. This could be due to the higher voltage at which the C-rate was reduced, thus allowing the 1C current to prevail for longer during the initial phase of charging.

The IC curves corresponding to the PIC region for raw PIC as well as DCR-compensated PIC at C/5 are plotted in Fig. 7(a). Similarly, the IC plots for C/3 are plotted in Fig. 7 (b). The IC plots for CC charging at these C-rates are also plotted for comparison.

For each C-rate, two important observations could be made. Firstly, for the raw PIC curve, it is noticeable that the Peak 1 showed an increase in peak intensity compared to CC charging. Secondly, there was noise in the IC plots which was not observed during CC charging. A plausible explanation behind this was the drop in voltage observed for a few minutes after the C-rate was changed. However, the higher intensity of Peak 1 or the observed noise did not affect the peak identification.

For both the C-rates, the peaks were obtainable using the same peak identification parameters in MATLAB. For each case, the difference in peak intensity compared to CC charging was less than 4 %. This indicates that the considered PIC strategies for both the C-rates are applicable for extracting useful IC features while charging the battery in less than 50 % time compared to CC charging. Compared to a C-rate of 1C, the PIC strategies resulted in added time, however the additional time could be accommodated in commercial applications via improved management or could be implemented as a periodic diagnostic test instead of performing it for every charge cycle.

4.2. 8P supercell

Similar to the single cell level experiments, the 8P supercell was also charged at 5 different C-rates. The voltage v/s capacity plots are shown in Fig. 8(a). Fig. 8(b) shows the IC plots obtained at each C-rate for the 8P supercell. The supercell data replicated the single cell IC plots, with similar features located at identical voltages. Moreover, the evolution of peaks with increasing C-rates was also identical to single cell, with major alterations observed at 1C. Similar to single cell data, the peaks for C/5 and C/3 were identifiable using the same parameters as C/25. The only anomaly was the higher peak intensity at C/10 compared to C/25, however the difference was negligible.

The supercell data evaluated from the charge cycles are listed in Table 3. The capacity and energy decreased with increasing C-rate. In addition, the single cell capacity and energy data were scaled by a factor of 8 and compared with the supercell data. The difference between the cell and supercell level metrics was within 0.5 %, which could be attributed to cell-to-cell variability. As expected, the maximum temperature with respect to ambient conditions increased with C-rates and showed a maximum value of 31.6 °C at 1C, while the temperature did not exceed 30 °C for other C-rates, as listed in Table 3.

4.2.1. Partial IC development at supercell level

The PIC strategies trialled at single cell level were employed to the supercell. Only the higher C-rate of C/3 was considered, with both raw and DCR-compensated PIC strategies. The resultant voltage v/s capacity plots are shown in Fig. 9(a). As for the single cell, the supercell voltage dropped for approximately 2 min to 3.47 V (raw PIC) and 3.53 V (DCR-compensated PIC). The IC curves corresponding to the PIC region for raw PIC as well as DCR-compensated PIC are plotted with C/3 CC charge curve in Fig. 9(b). The noise was again observed for both the PIC strategies. The error in peak intensity compared to CC charging was less than 1 % while the peak locations were identical. This confirmed that the PIC strategy was applicable for performing IC analysis at the supercell level.

The resulting metrics are listed in Table 4. Both charge capacity and energy were less than the C/3 charge. Compared to the 1C CC charge, there was a drop, potentially because of different starting SOCs, but the values were within 3 %. Unlike the single cell PIC trend, the raw as well as DCR-compensated PIC showed a higher maximum temperature compared to the 1C CC charge. However, the observed difference was negligible and within the accuracy of the thermocouple. Between the

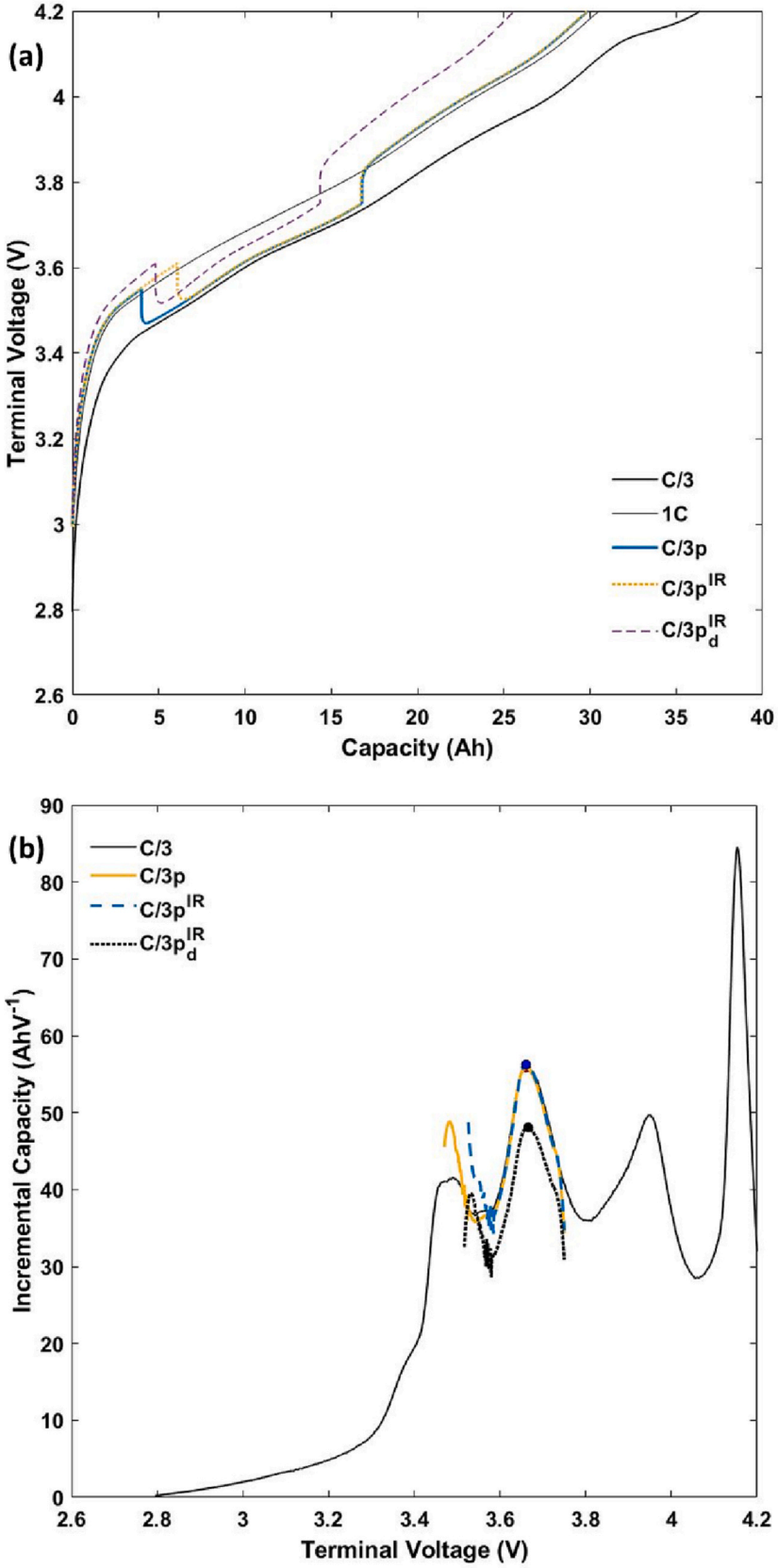

Fig. 10. (a) Voltage v/s capacity plot and (b) IC curves at C/3 corresponding to partial IC experiments for 8P supercell with and without faults. Note: subscript d indicates a supercell with disconnection fault; Curves for constant current charging are also shown for reference.

Table 5
Characteristics of supercells corresponding to C/3 partial IC. Note: d denotes supercell with a disconnection fault.

C-rate	Charge capacity (Ah)	Charge energy (Wh)	IC peak location (V)	IC peak intensity (Ah/V)	Charging time (hours)	Maximum temperature (°C)
C/3 DCRC	29.85	112.56	3.661	56.039	1.33	31.8
C/3 DCRC-d	25.61	96.66	3.666	48.091	1.16	32.1

two PIC strategies, the DCR compensated PIC resulted in a greater reduction in charging time.

4.3. Fault detection using Partial IC

4.3.1. Implementation of Partial IC technique

The DCR-compensated PIC strategy at C/3 was employed to the supercell with a disconnection defect. The resulting voltage v/s capacity curve is shown in Fig. 10(a). The lower capacity of the supercell resulted in early termination of the charging process. Moreover, the C-rate switch also occurred earlier, i.e. at a lower capacity. The IC curve for the defective supercell in the PIC region is shown in Fig. 10(b) with the PIC curves for the fully functional supercell. The curve showed a clear drop in IC values. This drop intensified in the region corresponding to the peak. The noise observed in the previously presented PIC data was also observed for the defective supercell.

The obtained charging metrics are listed in Table 5. The charge capacity for the defective supercell was 16 % less compared to fully functional supercell. Moreover, a higher maximum temperature was recorded. This was because the current was applied as per the nominal C-rate of the supercell. As the supercell had only 7 functional cells, the effective C-rate was higher than C/3 causing greater Ohmic heating. The IC peak intensity showed a drop of approximately 13 % alongside an increase of a few mV in the peak voltage. This difference in peak intensity was deemed to be significant enough to be differentiated from signal noise. Therefore, the PIC technique can be implemented at supercell level to detect disconnection faults in a supercell. The results are encouraging in that the method could detect the absence of one out of the eight cells in the supercell. Thus, it is reasonable to assume that a greater number of faulty cells should be detectable.

4.3.2. Investigation of noise in PIC data

To confirm the initially speculated dependence of the observed noise on the overpotential drop due to C-rate switch, an additional experiment was performed. In this experiment, the PIC segment was repeated at the supercell level with a rest period of 2 min between the initial 1C charge and the C/3 charge in the PIC window. This rest period would allow the voltages to relax before the low C-rate charging commenced. The resulting voltage v/s capacity plots and PIC curves are shown in Fig. 11 (a) and (b). The noise in the IC curves was eradicated while maintaining the peak intensity within 0.5 % compared to the initially obtained curves. In addition, the figure also shows a drop in the peak intensity corresponding to Peak 1. In Part 2, experiments conducted at the module level showed a similar drop in the IC curves pertaining to charging cycles that started at mid-SOC points and were speculated to be caused by prolonged relaxation before charging. The direct correlation between the reduction in peak intensity and the rest period before the commencement of charging at C/3, observable in the figure, confirms the speculation. Thus, the additional rest period successfully removed the noise in the PIC data.

4.3.3. Limitation of Partial IC

In the previous sub-section, a disconnection fault with one faulty cell in a supercell of 8 was simulated. The location of the IC peak remained within the PIC window despite the higher effective C-rate. While this is crucial to detect the disconnection fault, the peak could get pushed beyond the considered voltage window. This would result in failure of the presented method in detecting the fault. Such a scenario could occur when the number of simultaneously failed cells in a parallel-connected supercell is high enough to increase the C-rate significantly. Therefore, an experiment using a single cell was undertaken to identify the number of cells, the simultaneous failure of which would render the PIC method unusable. The failure of 4 and 5 cells in an 8P supercell was simulated by scaling the current of C/3 (selected for PIC) to the effective value a cell would be exposed to upon these many cells failing. This calculation indicated that 4 failed cells would result in a current of 3.2A ($8/4 \times C/3$), while 5 cells would cause 4.3A ($8/3 \times C/3$) to flow. A CC charge was conducted for these C-rates using the single cell. The resultant IC plots are shown in Fig. 12. For both the cases, the identified peaks using the same algorithm were found to lie within the selected voltage window for partial IC. This indicated that in the event of a simultaneous failure of 4 or even 5 cells in the supercell, the proposed PIC method would detect the fault. For a failure of 6 cells, the current at single cell level exceeds 1C. From Table 1, the voltage corresponding to the IC peak at 1C was found to lie beyond the considered voltage window. Therefore, the PIC algorithm will fail when six cells fail simultaneously. However, the BMS is expected to intervene in such drastic situations via obvious indications such as significant voltage imbalance across the pack.

4.4. Validation test with 11s8p module

The voltage v/s capacity curves for each supercell during the module-level PIC charging of 48X and 40 T supercells are shown in Fig. 13(a) and (b). Using Eq. (1) a C-rate switching voltage of 3.585 V was calculated for the 40 T cells. As this cell has a lower impedance compared to 48X, the overpotential correction was lower. The faulty supercells for both modules had the lowest beginning of charge voltage as it reached the cut-off earlier in the preceding discharge segment. The higher C-rate for this supercell is apparent from the greater slope of the charge curve. Contrary to the supercell level results, the charging of each supercell terminated simultaneously irrespective of the defect as the charging of the entire module was globally controlled. In addition, despite the presence of a defective supercell, the PIC segment lasted longer taking approximately 90 min to charge the module. This is because the C-rate switching was controlled such that the PIC voltage window corresponding to each supercell occurs at the lower C-rate of C/3, thus resulting in a longer PIC segment. The finally obtained IC curves from the lower C-rate segment are shown in Fig. 13(c) and (d). As evident from the figure, in both modules the IC peak corresponding to the faulty supercells showed a difference greater than 12 % compared to the average peak value for all the functional supercells. Thus, the PIC method was useful for identifying supercell having a single disconnection fault for both the modules, while charging them in 90 min.

4.5. Fault diagnosis for real-life battery module

The supercell voltage and temperature profile during the PIC charging regime corresponding to DF1 are shown in Fig. 14. The module was charged in less than 90 min. The internal temperature measured in the inter-cell pockets had maximum and minimum values of 45 °C and 42 °C respectively. The observed variation is comparable to the readings in Parts 1 and 2. On the other hand, while the temperature on the side cells at the edge of the module were all within 1 °C, the readings were 15 °C below the internal temperature because of their greater heat dissipation rates. The higher temperature compared to low C-rate cycling was attributed to the increased C-rate. Compared to DF1, the maximum temperature was within 1 °C for DF2 and DF3 tests.

The obtained fault parameters from the PIC charging strategy for

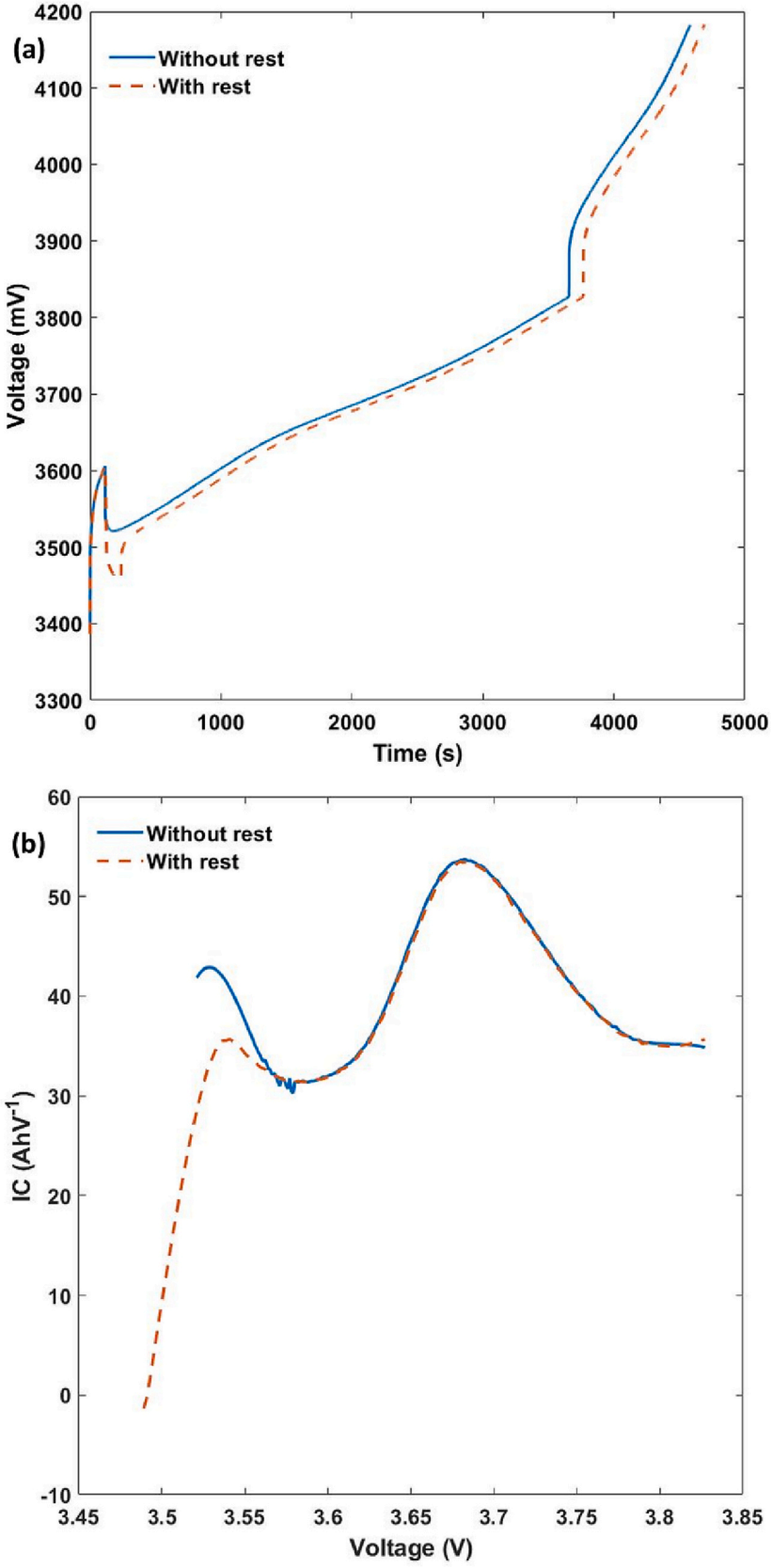

Fig. 11. (a) Voltage and (b) IC curves corresponding to PIC charging strategy with and without rest period after initial fast charging segment.

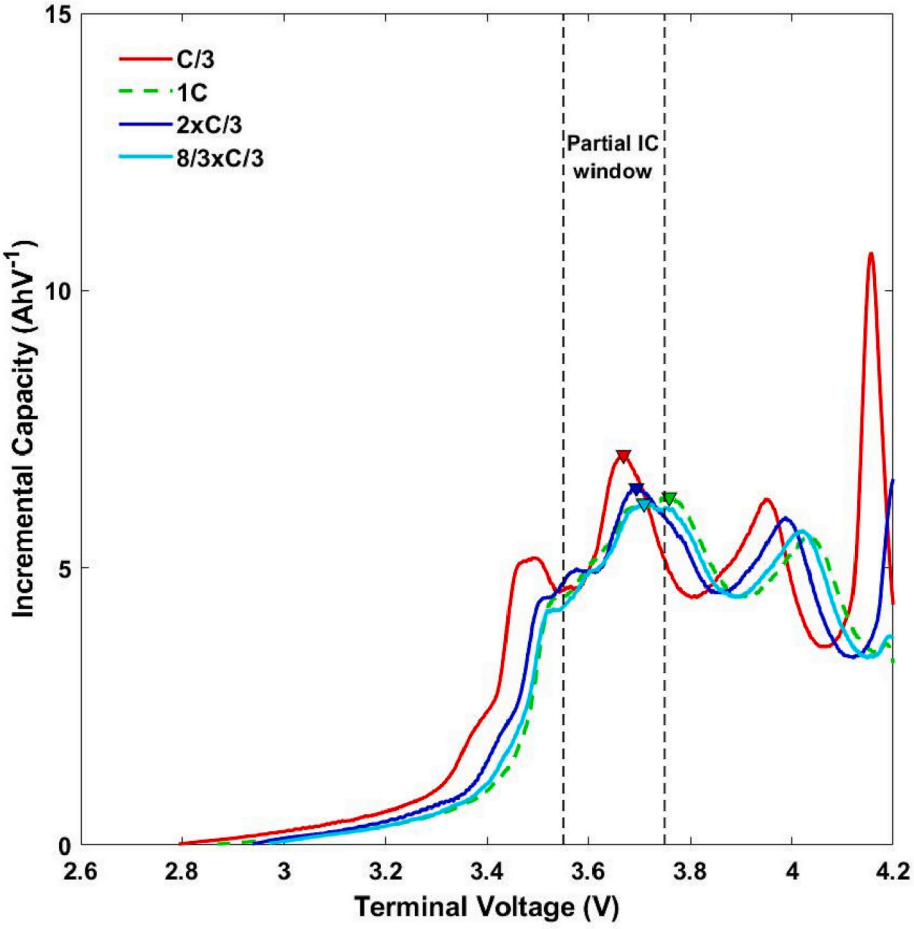

Fig. 12. IC peak recognition conducted for single cell at C-rates corresponding to failure of 4 and 5 cells. Note: IC curves for C/3 and 1C are shown for reference.

each supercell are shown in Fig. 15. The plot indicates that the supercells with the disconnection fault were identified successfully by the algorithm in each test case. On the other hand, a maximum fault parameter value of 11.5 was noted, which is acceptable with respect to level-1 results. Therefore, while charging the module faster compared to levels 1 and 2, the PIC technique enabled adequate functionality of the algorithm.

The fault parameter values obtained across Level-1 and Level-3 for the battery module tests are listed in Table 6. The minimum fault parameter for faulty supercells across all the tests was approximately twice the maximum and four times the average obtained for unfaulty supercells. This indicates a low probability of false alarms while providing a wide window for selecting an appropriate fault threshold.

The PIC technique was developed using a CC charge cycle in this work. However, fast charging typically occurs using modified current profiles developed to minimise battery degradation [30]. It is important to assess the feasibility of merging such fast-charging profiles with the PIC strategy. For instance, Fig. 16 shows the current profile for PIC implementation during a 1.3 kW Constant Power (CP) charge cycle for the battery module. The PIC phase involves a CC charge to enable IC implementation, while the CP charge segments have a constantly reducing current. Similar profiles, such as the UAM-specific ultrafast charging profile developed by Liu et al. [31], will be merged with PIC technique in future work to further reduce charging time as well as battery degradation.

5. Future considerations

The fault diagnosis algorithm was developed using multi-level experimental testing and validated across three levels of complexity to understand its applicability for real-life aerospace battery packs. To carry this work forward, the research presented in this three-paper series will be expanded through (a) incremental experimental tests to improve the confidence in results thus far and (b) inclusion of novel aspects to improve applicability and transferability.

The incremental component of future work will focus on performing further tests to assess the algorithm. This would involve tests subjecting the algorithm to various combinations of external conditions encountered thus far. For instance, fast charging considered in level-3 will be combined with partial charging conditions from level-2. Moreover, a broader range of defects will be considered as every defect may not produce a change as significant as the disconnection faults considered in this work. These include faults such as overvoltage and overtemperature occurring locally in certain cells in the module, which may produce smaller changes in the battery metrics calculated by the algorithm. Similarly, detection of Li plating will also be considered by using ICA as demonstrated by Anseán et al. [32] as well as post charge voltage analysis as shown by Somasundaran et al. [33]. Furthermore, the expected SOH and cell chemistry agnostic nature of the algorithm will be assessed using aged cells as well as different cell chemistry.

In addition, it is well understood from level-2 tests that additional redundancy is required in the algorithm in certain conditions where battery data may not remain comparable between consecutive charge cycles. This could be overcome by adding a model component to produce expected values of battery metrics for comparison. Exploiting the abundant memory available in the on-ground charger, the battery model parameters could be parametrised after every charge cycle, thus updating it to the aged state of the battery, a limitation often cited for

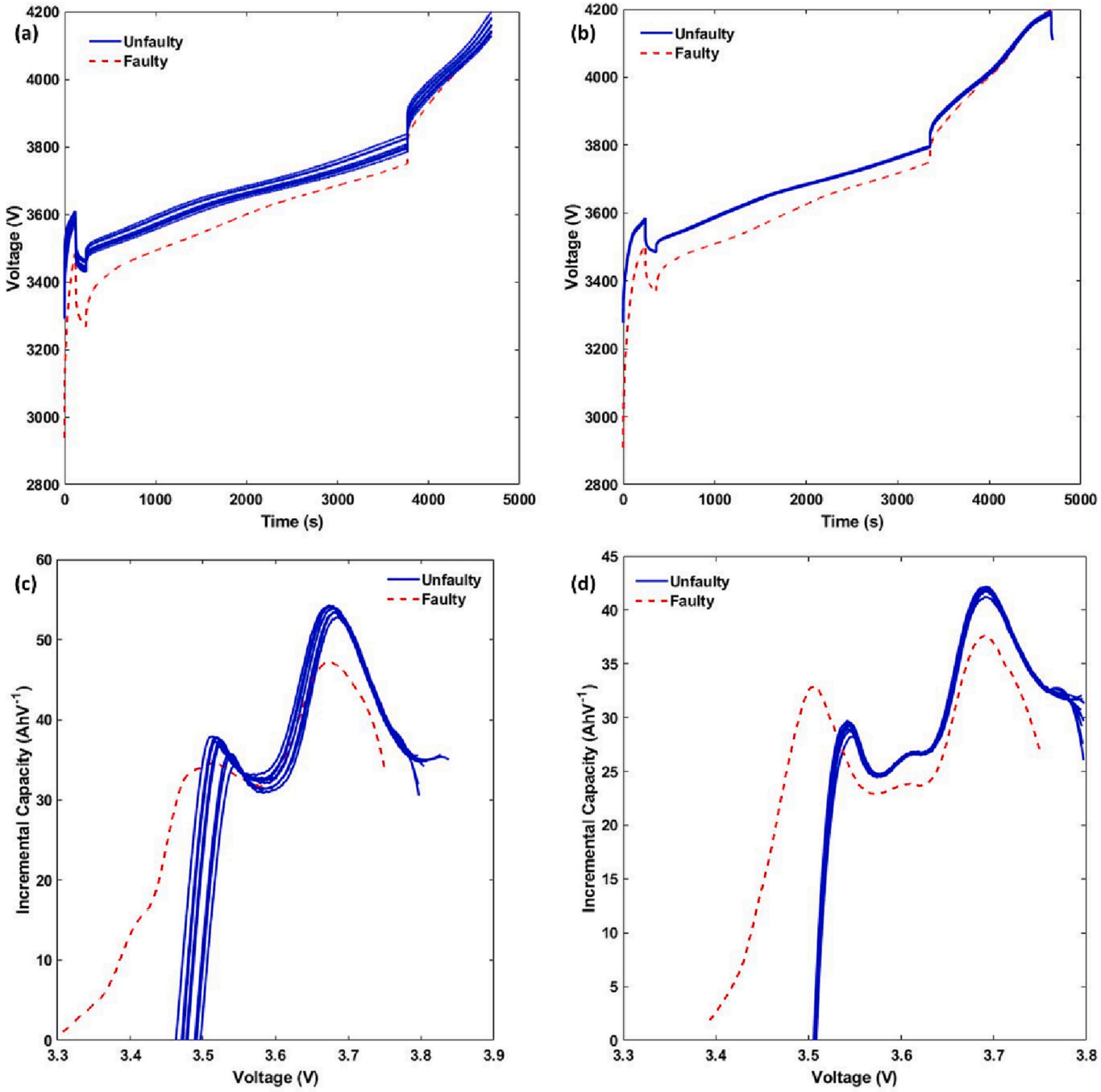

Fig. 13. Supercell data from validation test of the PIC algorithm at 11s8p level: Voltage v/s capacity and IC curves for PIC charge segment corresponding to 48X ((a) and (c)) and 40 T ((b) and (d)) cells.

model-based approaches [34]. Furthermore, Machine Learning (ML) techniques would be ideal for developing correlations corresponding to ideal battery performance from the data collected during numerous charging cycles and highlight the presence of a fault upon severe divergence from the learnt battery behaviour. The ML model could work in isolation or clubbed with a battery model. Incorporating such smart functionalities is expected to improve the robustness as well as cell-to-cell transferability of the algorithm, thus potentially reducing the experimental effort required to test and tune it as per different external conditions. Finally, the IC component of the algorithm is usable for analysis of electrode-level degradation phenomenon. Thus, further exploitation of the fine IC metrics obtained via PIC method over the lifetime of the battery would open the door for fault prognosis and pave the way to identify optimised battery operation for long-term durability at high-performance levels.

6. Conclusions

In this work, a novel technique called Partial Incremental Capacity (PIC) was presented. The PIC technique allows for collection of IC features, available only at a lower C-rate, during fast-charging by switching to a lower charge current in a specific voltage range. The technique was developed through experimental testing at single-cell and supercell levels and proven at the module level using an in-house module. The PIC technique was incorporated into a battery fault diagnosis algorithm focusing on disconnection faults and the performance of the algorithm

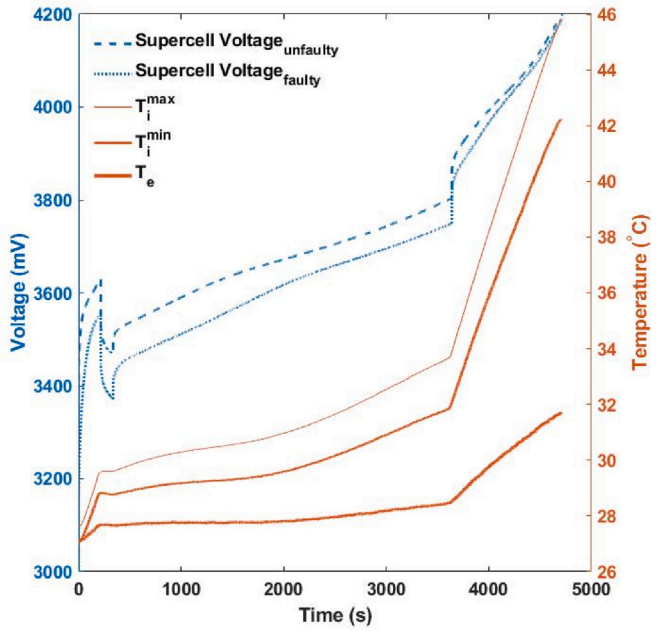

Fig. 14. Supercell voltage and temperature evolution in battery module during the PIC charge. Note: T_i represents inter-cell pocket temperature; T_e represents cell surface temperature on the edge of the module.

was validated through experimental testing using a real-life aerospace battery module. Thus, the fault diagnosis algorithm, developed and tested in Parts 1 and 2 for diagnosing disconnection faults using lower currents previously, was imparted with the ability to perform its task during fast-charging and minimises vehicle downtime in actual application. While this work was limited to the implementation of the PIC technique for a constant current charge scheme, more realistic charging profiles with a dynamic current/power profile will be considered in the future.

This paper series presented the development and validation journey of the battery fault diagnosis algorithm intended to work by exploiting data collected during the charging of electric aircraft. Advancing through three levels of development, the algorithm's viability for real-life implementation was improved. The algorithm was extensively tested using a real-life battery module, a step that was recognised as a gap in current literature. This was further highlighted by the importance of thermal management being realised as a crucial component for the algorithm, a limitation that ideal laboratory testing would have missed. The work presented thus far was limited to a disconnection fault. In the future, the algorithm will be extended to a broader range of battery faults to make it globally applicable. The SOH-independent and cell-agnostic nature of the algorithm will be confirmed through appropriate test conditions and specimens. The PIC technique would serve as an important enabler towards this vision. Moreover, opportunities have been identified to incorporate aspects of battery modelling and machine learning to exploit the available memory and computational power in an on-ground charger. The addition of such capabilities will improve the cell-to-cell transferability as well as reduce the experimentation burden, thus enhancing its overall industrial acceptance.

CRediT authorship contribution statement

Conceptualisation, A.S. and A.B.; methodology, A.S. and A.L.; validation, A.S. and A.L.; formal analysis, A.S. and A.L.; investigation, A.S., A.L. and Y.L.; resources, A.B. and D.W.; writing—original draft preparation, A.S. and A.L.; writing—review and editing, A.B. and D.W.; project administration, A.B. and D.W.; funding acquisition, A.B. and D.W. All authors have read and agreed to the published version of the manuscript.

Table 6
Statistical analysis and comparison of algorithm performance for the battery module across Level-1 and 3. Note: values crucial for indicating algorithm performance are underlined.

	Minimum (faulty)	Maximum (unfaulty)	Average (unfaulty)
Level-1	29.15	14.46	7.13
Level-3	28.65	11.52	6.46

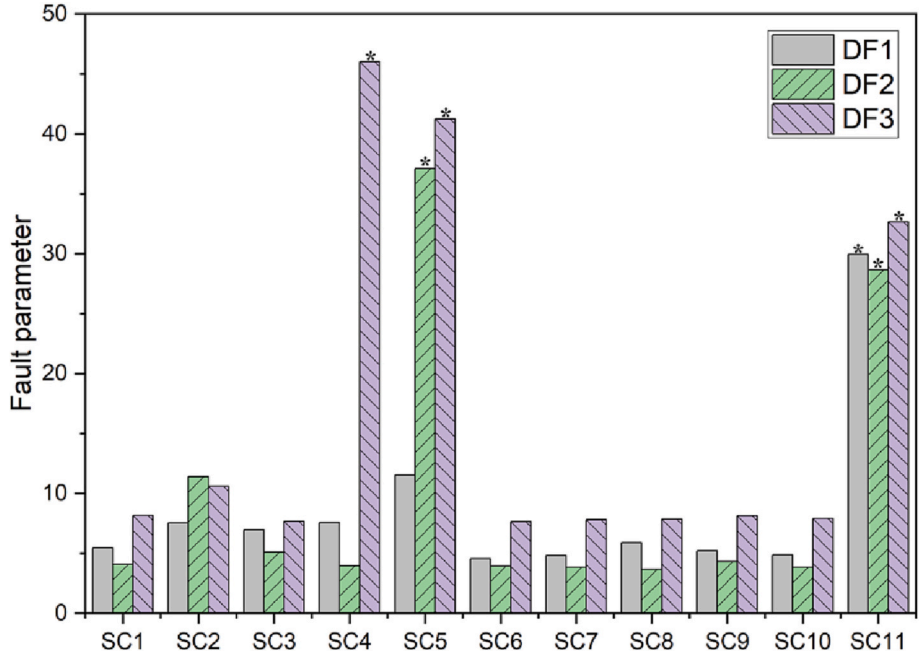

Fig. 15. Fault parameters obtained upon implementing the algorithm for the battery module data corresponding to PIC charging strategy. Note: Faulty supercells are denoted with *.

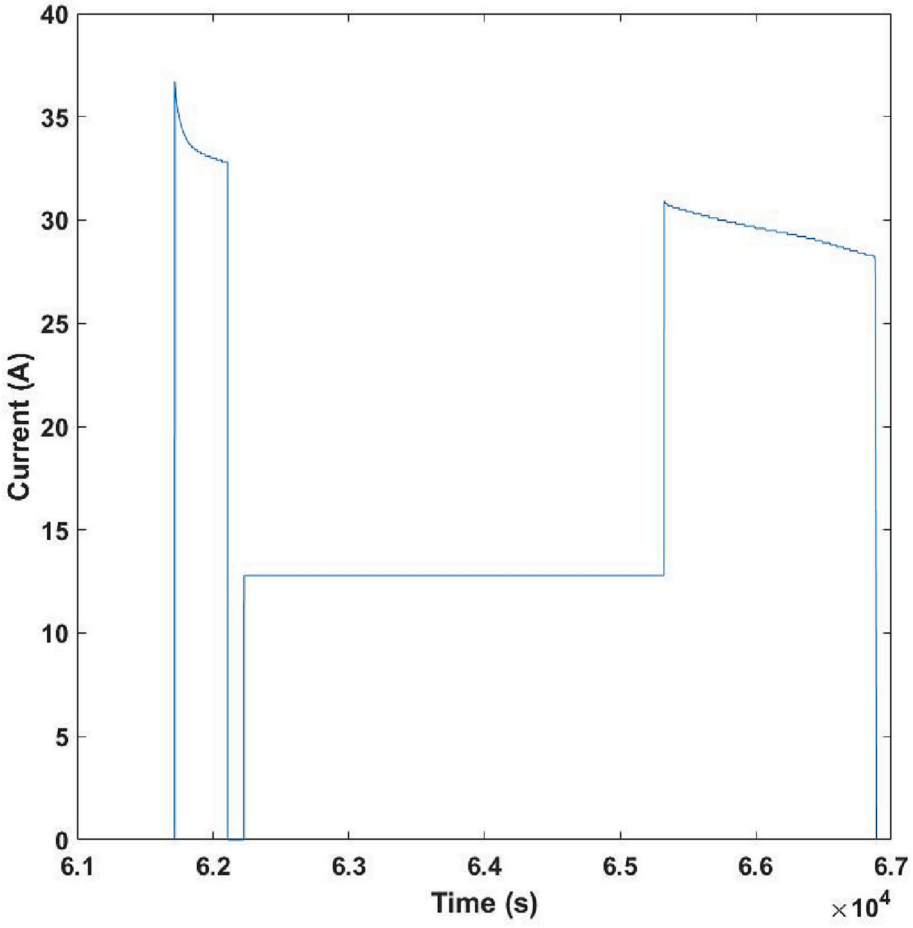

Fig. 16. Current profile implemented for PIC during a CP charge cycle for the battery module.

Funding

This research was supported by Aerospace Technology Institute (ATI) project called AEDD (IDEATE 63277).

Declaration of competing interest

There do not exist any conflicts of interest associated with this publication and the financial support received for this research could not have influenced its outcome.

Data availability

The data was generated as part of an ongoing project with an industrial partner and will be available in the future.

Acknowledgement

The authors would like to express their gratitude towards the research team and staff at WMG and Vertical Aerospace for their support and feedback.

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