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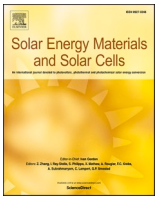

Exploring hafnium oxide's potential for passivating contacts for silicon solar cells

A. Wratten [a], S.L. Pain [a], A. Yadav [a], E. Khorani [a], T. Niewelt [a,b,c], L. Black [d], G. Bartholazzi [d], D. Walker [e], N.E. Grant [a], J.D. Murphy [a,*]

[a] School of Engineering, University of Warwick, Coventry, CV4 7AL, UK
[b] Fraunhofer Institute for Solar Energy Systems ISE, Heidenhofstraße 2, 79110, Freiburg, Germany
[c] Laboratory for Photovoltaic Energy Conversion, University of Freiburg, Emmy-Noether-Straße 2, 79110, Freiburg, Germany
[d] School of Engineering, The Australian National University, 2600, Canberra, Australia
[e] Department of Physics, University of Warwick, Coventry, CV4 7AL, UK

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ABSTRACT

We investigate the potential of ultra-thin HfO_2 films grown by atomic layer deposition for passivating contacts to silicon focusing on variations in film thickness and post-deposition annealing temperature. A peak in passivation quality – as assessed by carrier lifetime measurements – is reported for 2.2 nm thick films annealed at 475 °C, for which a surface recombination velocity <1 cm/s is determined. For films <2.2 nm thick, there is a marked decrease in passivation quality. X-ray diffraction highlights a change from crystallised monoclinic to amorphous HfO_2 as film thickness decreases from 12 nm to 2.2 nm. Kelvin probe results indicate that as-deposited 2.2–12 nm films have similar effective work functions, although the work function of 1 nm films is considerably lower. Upon post-deposition annealing in vacuum, all films exhibit a reduction in effective work function at temperatures coincident with the onset of passivation in air-annealed samples. An initial investigation into the contact resistivity in a passivating contact structure utilizing HfO_2 reveals a strong post-deposition annealing temperature dependence, with the lowest resistance achieved below 375 °C, followed by a decrease in performance as temperature increases towards the optimal temperature for passivation (475 °C). Limitations of the contact structure used are discussed.

1. Introduction

Many cell architectures that currently dominate the commercial silicon PV market are limited by recombination losses due to direct metal/Si interfaces at the electrode. However, the development of passivating contacts/interlayers between the Si and metal over recent years has helped to mitigate these losses, preventing recombination in the contacted region without significant reduction in contact conductance [1–5]. Such interlayer structures are referred to as passivating contacts.

The most promising passivating contact structures for silicon solar cells thus far have been amorphous silicon (a-Si) heterojunction (HJT), tunnel oxide passivated contact (TOPCon), and polysilicon on oxide (POLO) architectures [1,6,7]. Where dielectric films have been used, existing literature has focused on SiO_2 and Al_2O_3 due to their established performance as passivating layers, and their respective positive and negative fixed charges [8–12]. In the case of SiO_2, pinholes that are produced at high temperatures enable the material to be utilised for both electron and hole extraction [13,14]. However, the band off-sets of SiO_2 indicate favourability for electron transport over hole transport, which, amongst other factors, enables SiO_2 to have higher performance as an electron-selective layer than as a hole-selective layer [15]. There is considerable interest in developing hole-selective contacts that can match the performance of existing electron-selective contacts [16].

Hafnium oxide (HfO_2) is a dielectric material with existing application in transistors and capacitors [17,18], and has shown promise in recent years as a passivation layer for silicon photovoltaics [19–22]. Our previous work demonstrated that HfO_2 passivating films perform particularly well at ultra-thin thicknesses, below 3 nm, outperforming Al_2O_3 layers of a similar thickness [23]. This is especially useful for passivating contacts, as dielectric layers inherently have high resistance and so must be kept very thin to facilitate charge carrier transport

* Corresponding author.
E-mail address: john.d.murphy@warwick.ac.uk (J.D. Murphy).

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mechanisms [15]. The mechanisms involved for charge carrier transport are still under debate, but the two main hypotheses are quantum tunnelling and/or pinholes [24]. We have previously demonstrated that, under certain conditions, pinholes can exist in HfO_2 films [25], and hence at this stage both mechanisms could be possible. The probability of charge carrier tunnelling is inversely related to the film thickness [26]:

$$P_t = \exp\left(\frac{-2}{\hbar} t \cdot \sqrt{2m^* \cdot q \cdot \Delta\varphi_b}\right) \quad (1)$$

where $\hbar$ is the reduced Planck's constant, m^* is the tunnelling charge effective mass, q is the charge on an electron, t is film thickness and $\Delta\varphi_b$ is the potential barrier height at the interface. Consequently, the thinner the film, the higher the probability of charge carrier tunnelling and hence the higher the current which can be extracted.

Interestingly, HfO_2 films can be either positive or negatively charged. There is currently no consensus on the mechanisms that determine charge polarity, though there have been some suggestions that the choice of precursor or annealing ambient may have an impact [27,28]. Table 1 provides a review of existing literature where HfO_2 fixed charge is reported, alongside the deposition technique, post-deposition treatment, and measurement approach used. The charge of a dielectric layer plays an important role in determining the selectivity of a passivating contact. Specifically, the direction of band bending of the electronic bands at the interface is strongly dictated by the charge polarity and density. Since the charge polarity and density in HfO_2 can potentially be tuned, it may lend itself to applications in both electron- and hole-selective contacts. Literature has shown that whilst the ratio of band off-sets for negatively charged HfO_2 indicates electron favourability, the potential barrier for hole transport is lower than in both Al_2O_3 and SiO_2 [15].

Table 1 also provides an overview of the passivation quality achieved to date with HfO_2-based films. From Table 1 and it can be seen that HfO_2 is a promising passivation layer for *n*-type silicon, with SRVs of <10 cm/s possible for HfO_2 grown by thermal and plasma-enhanced ALD. There is little information published on HfO_2 surface recombination current density prefactors (J_{0s}), though our recent investigations achieve single-side values of 28.4 fA/cm^2 and 14 fA/cm^2 for 12 nm and 2.2 nm HfO_2 films, respectively [19,23].

This paper further investigates the passivation characteristics of negatively charged ultra-thin HfO_2 layers, focusing of thickness dependence, through photoconductance decay carrier lifetime, X-ray diffraction (XRD), and Kelvin probe measurements. This is followed by an initial study into an Au/Si(*n*-type)HfO_2/Al contact structure, containing a negatively charged HfO_2 layer, through the expanded Cox and Strack method (ECSM [37–40]). Potential limitations within the contact

Table 1
Review of reported HfO_2 fixed charge, including deposition, post-deposition, and measurement variables. Surface recombination velocities calculated at an excess carrier density of 1×10^{15} cm^{-3}, for wafers with resistivities of 1-5 Ωcm, are also included. Based on the relationship between SRV and J_{0s} described in Ref. [29], J_{0s} values are also approximated for studies using substrates of a fixed resistivity. Where J_{0s} values were reported by the authors, rather than determined herein, these values are italicised [30,31,32,34].

Reference	Precursor	Substrate	Deposition	Ambient	Measurement	Polarity	Magnitude (q/cm^2)	SRV (cm/s)	Approx. J_{0s} (fA/cm^2)
[30]	TEMAH[a]	*n*-type FZ*	Plasma (O_2)	N_2	CV[1]	Positive	10^{12}	-	-
[30]	TEMAH	*n*-type FZ	Plasma (O_2)	N_2	CV	Negative	10^{12}	38.9	168
[31]	TEMAH	*n*-type FZ	Thermal (H_2O)	N_2	CV	Positive	10^{12}	20	115
[28]	TEMAH	*n*-type FZ	Thermal (H_2O)	N_2	CV	Negative	$< 10^{11}$	7	40
[28]	TEMAH	*n*-type FZ	Thermal (H_2O)	H_2	CV	Positive	10^{12}	5	29
[28]	TEMAH	*n*-type FZ	Thermal (H_2O)	None	CV	Negative	10^{12}	29	167
[22]	TEMAH	*p*-type FZ	Thermal (H_2O)	H_2/N_2	Corona/CV	Positive	10^{11}	9.9	6
[22]	TEMAH	*n*-type FZ	Thermal (H_2O)	H_2/N_2				3.3	7
[21]	TEMAH	*n*-type FZ	Thermal (H_2O)	Air	CV	Positive	10^{12}	1.2	-
[32]	$HfCl_4$[b]	*n*-type FZ	Thermal (H_2O)	None	CV	Positive	10^{12}	76	-
[33]	$HfCl_4$	*n*-type Cz[†]	Thermal	N_2	KP[2]/COCOS[3]	Negative	10^{11}	-	-
[27]	$HfCl_4$	*p*-type	Thermal (H_2O)	H_2/N_2	CV	Negative	10^{12}	-	-
[27]	TDEAH[c]	*p*-type	Thermal (H_2O)	H_2/N_2	CV	Positive	10^{11}	-	-
[34]	TMHf[d]	*n*-type FZ	Thermal (H_2O)	N_2	CV	Negative	10^{12}	24	110
[34]	TMHf	*p*-type FZ	Thermal (H_2O)	N_2	CV	Negative	10^{12}	55	78
[35]	TDMAH[e]	*n*-type Cz	Thermal (H_2O)	-	COCOS	Negative	10^{11}	11	20
[35]	TDMAH	*n*-type FZ	Thermal (H_2O)	-	-	-	10^{11}	7.7	32
[19]	TDMAH	*n*-type Cz	Plasma (O_2)	Air	Corona	Negative	10^{12}	6.6	*28*
[23]	TDMAH	*n*-type Cz	Plasma (O_2)	Air	Corona	Negative	10^{12}	2.5	*14*
[36]	TDMAH	*p*-type Cz	Plasma (O_2)	Air	-	-	-	101	*393*
This work	TDMAH	*n*-type Cz	Plasma (O_2)	Air	-	-	-	0.6	*3*

(a) tetrakis(ethylmethylamido)hafnium, (b) hafnium tetrachloride, (c) tetrakis(diethylamido)hafnium, (d) trimethylhafnium, (e) tetrakis(dimethylamido)hafnium
* Float zone, [†]Czochralski
[1] Capacitance-Voltage, [2]Kelvin probe, [3]Corona Oxide Characterization Of Semiconductor method

structure and the HfO_2 layer itself are discussed.

2. Methodology

2.1. Dielectric layer deposition

5 cm × 5 cm samples were fabricated from 150 μm thick, 5 Ωcm, *n*-type or *p*-type Cz-Si (100) wafers herein referred to as *n*Si and *p*Si, respectively. These samples were first cleaned with an established process [41], involving 10 min in each of the following solutions heated to 80 °C: RCA1 (DI H_2O, NH_4OH (30%), and H_2O_2 (30%) in a 5:1:1 ratio), tetramethylammonium hydroxide (TMAH (25%)), and RCA2 (DI H_2O, HCl (37%), and H_2O_2 (30%) in a 5:1:1 ratio). The majority of wafers used were chemically etched, except those used for subsequent XRD measurements, for which mirror polished substrates were used, and the cleaning process omitted the TMAH etch. Before each cleaning and etching step, a DI water rinse and 60 s HF (1%) dip were conducted. The cleaning process was concluded with submersion in either a 1% HF/1% HCl solution (for XRD, Kelvin probe measurements, and lifetime measurements) or 2% HF solution (otherwise) until the samples became hydrophobic (approximately 10 s). No water rinse was performed prior to film deposition.

HfO_2 films were grown *via* plasma-enhanced ALD (PE-ALD) using a Veeco Fiji G2 system, with tetrakis(dimethylamido)hafnium (TDMAH) and O_2 plasma as the precursor and co-reactant, respectively. Argon was used as the inert purge gas. While various other precursors and deposition conditions have been shown to produce HfO_2 films [21,27,35,42] we chose to investigate films deposited with one specific deposition recipe for consistency across our studies. The TDMAH precursor, heated to 75 °C, was pulsed into the chamber for 0.25 s, followed by a 6 s pulse of O_2 plasma at 300 W. A 5 s purge was conducted before and after each step. The growth rate, for a deposition temperature of 200 °C, is approximately 1 Å/cycle (as reported by the supplier [43], and verified in previous work [23]). Film thicknesses corresponding to 10, 25, 50 and 100 cycles of HfO_2 were confirmed in our prior work to be ~1, 2.2, 3.3 and 12 nm, respectively, using x-ray photoelectron spectroscopy and x-ray reflectivity [23,25]. Intermediary thicknesses were estimated by interpolating from these thicknesses. The samples were then either left as-deposited, or annealed *ex situ* in air in a quartz tube furnace for 30 min. A variety of sample structures were used in this investigation. These structures are presented schematically in Fig. 1.

2.2. Film characterisation

Photoconductance decay charge carrier lifetime measurements of double-sided samples (Fig. 1(a)) were performed at room temperature, using a Sinton Instruments WCT-120PL lifetime tester (software version 5.74). The measurements were conducted in transient (short flash) mode and averaged over five flashes.

Film crystallinity was investigated using grazing incidence X-ray diffraction (GI-XRD). These measurements require using thicker, mirror polished Si wafers, as depicted in Fig. 1(b). Measurements were conducted using a 3rd generation Malvern Panalytical Empyrean XRD Diffractometer, with multicore optics (iCore), and a Pixcel3D detector, under Cu $K_{\alpha 1/2}$ radiation. An incidence angle of 0.5° was used for all measurements. 2θ measurements were taken in a range of 15°–70°, with a step size of 0.02–0.03°.

Kelvin probe data were acquired from single-sided HfO_2 samples (Fig. 1(c)) using an ultra-high vacuum UHV Kelvin probe (KP Technology) with an uncoated stainless-steel tip, which was calibrated at 4.4 eV. Films were measured under high vacuum (10^{-8} mbar), both at room temperature and as a function of temperature during *in situ* activation annealing, with a temperature ramp rate of ~3 °C/min. Annealing temperature and ramp rate were controlled manually. For this experiment, CPD measurements were taken at elevated temperature. Surface photovoltage (SPV) measurements were made at room temperature, prior to and following annealing. SPV was measured under white-light illumination with an intensity of ~0.25 Suns using the same system. For all other experiments in this work, measurements were at room temperature.

IV measurements were made using a Wentworth probe station with an Agilent B1500A Parameter Analyser. Fig. 1(d) and (e) show the sample structures considered. The resultant IV data were analysed using the ECSM [37–40]. In the standard Cox and Strack approach the total resistance (R_T) is defined as

$$R_T = R_C + R_S + R_0 \tag{2}$$

where R_C is the contact resistance, R_S is the spreading resistance within the substrate, and R_0 is the residual resistance from the full coverage rear contact, which is presumed negligible. The contact resistivity, ρ_c, can then be extracted from the following equation:

$$R_C = \frac{\rho_c}{\pi\left(d^2/4\right)} \tag{3}$$

where d is the diameter of the contact. For diode structures (*i.e.*, Schottky contacts), it is also necessary to apply Cheung's method [44]:

$$\frac{d(V)}{d(\ln I)} = R_T I + \frac{nq}{kT} \tag{4}$$

such that the contact resistivity is then the gradient of the plot of $R_T - R_S$ by the inverse contact area, given by $\frac{1}{\pi\left(d^2/4\right)}$.

2.3. Contact fabrication and process development

Photolithography was performed using an AZ2035 photoresist (MicroChemicals), spin-coated at 5000 rpm for 50 s, and soft baked at 110 °C for 60 s. Samples were then exposed to UV light through a photomask consisting of rows of circles, which varied in size from 1.4 to 2.4 mm in diameter. UV exposure was conducted using a Suss MicroTec BA8 Gen3 mask aligner in hard-contact mode, with an equivalent dose of 120 mJ/cm^2. This was then followed by a hard bake at 110 °C for 90 s, and development in an MF-319 (MICROPOSIT) solution for 35 s.

200 nm thick Al or 100 nm thick Au metal contacts were deposited using a Scientific Vacuum Systems Ltd electron-beam (e-beam) evaporation system. The exposed Si was etched *in situ* using an integrated ion beam gun to remove any native oxide before the deposition of the full-

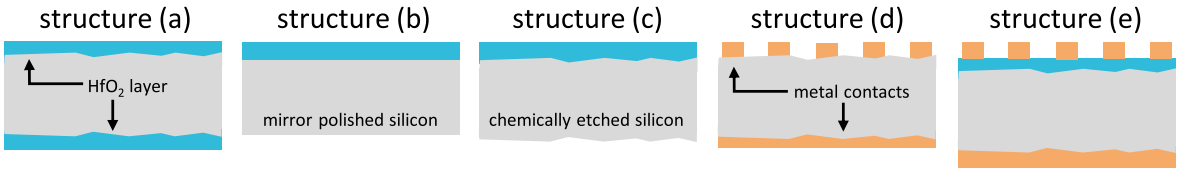

Fig. 1. Schematics of the various sample structures considered in this paper. These schematics are designed as visual aids and are not to scale. (a) Double-sided HfO_2 films on chemically etched *n*-type Si for lifetime measurements. (b) Single-sided HfO_2 on mirror polished Si for XRD measurements. (c) Single-sided HfO_2 on chemically etched *n*-type Si for Kelvin probe measurements. (d) Full area rear metal contacts and patterned front metal contacts for optimisation of the rear contact structure. (e) A completed sample with full area rear metal contact, front side HfO_2 layer, and patterned front metal contact.

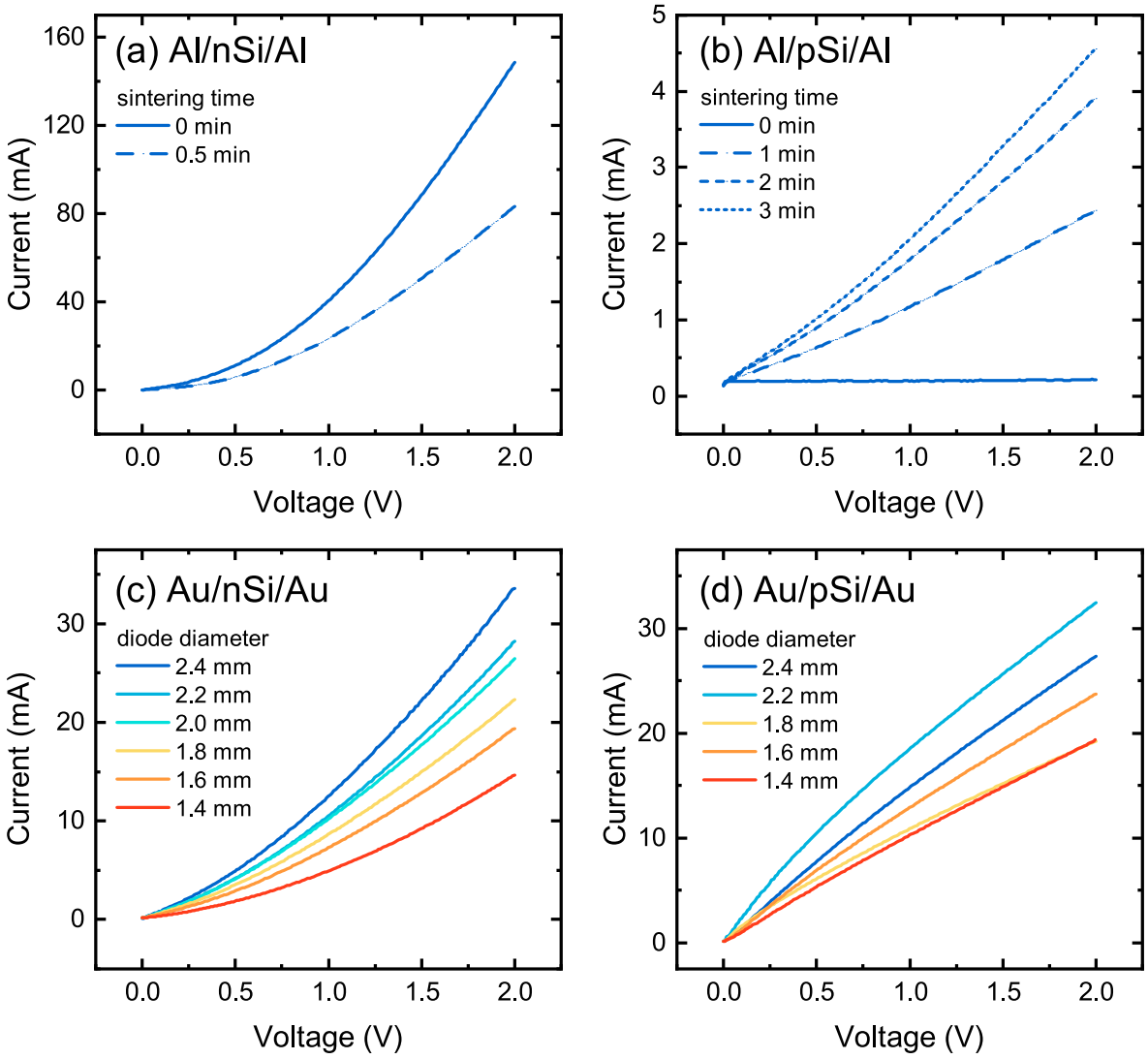

Fig. 2. Current-voltage characteristics of various direct metal-Si contact structures (corresponding to structure (d) in Fig. 1), with full area rear contacts and mm-scale circular front contacts. (a) Al/*n*Si/Al, with a 2.4 mm diameter front contact, before and after a 30 s sintering step at 400 °C in air. (b) Al/*p*Si/Al, with a 2.4 mm diameter front contact, after successive sintering steps. (c) Au/*n*Si/Au, un-sintered, for various front diode sizes. (d) Au/*p*Si/Au, un-sintered, for various front diode sizes.

area rear contact. Metal lift-off was then performed by leaving samples in dimethyl sulfoxide (DMSO) overnight.

The current-voltage (IV) characteristics of direct metal-Si contacts for structures depicted in Fig. 1(d), for *n*- and *p*-type wafers with Al and Au can be seen in Fig. 2. Fig. 2(a) shows the IV curve of an *n*-type substrate with a full-area Al rear contact and 2.4 mm diameter Al front contact (labelled Al/*n*Si/Al). The initial IV data show that the resistance is not constant and varies with voltage and current, indicating a non-ohmic contact. Sintering for 30 s at 400 °C begins to straighten the curve but results in a reduced current. The equivalent structure on *p*-type Si (Al/*p*Si/Al) initially produces a negligible current flow after deposition, implying an inefficient contact structure. This can be improved significantly through sintering, as demonstrated in Fig. 2(b); however, the absolute current values are still substantially lower than the Al/*n*Si/Al structure and deviate from ideal ohmic behaviour.

Using Au as contact metal results in similar current values for both *n*- and *p*-type samples, being higher than achieved for the Al/*p*Si/Al structure, but lower than the Al/*n*Si/Al structure, as seen in Fig. 2(c) and (d). Having direct metal-Si rear contacts that behave similarly for both wafer types is beneficial when making comparisons between the effectiveness of different metal-dielectric-Si front contacts, as the effects of the rear contact can be considered consistent throughout. The IV curves are also relatively ohmic, though not completely ideal. It is possible that a thin oxide grew on the exposed Si surface during the lithography process, although other factors like surface roughness and contamination could also play a part. This would not be an issue with the completed structure due to the inclusion of the HfO_2 layer. Importantly, not requiring a sintering step reduces the processing complexity and thermal budget of the sample development. Based upon these results, all sample structures considered in the rest of this work include a full area Au rear contact.

3. Results and discussion

3.1. Characteristics of ultra-thin HfO_2 films

In order to demonstrate the effectiveness of ultra-thin HfO_2 films as passivation layers, Fig. 3(a) shows the effective lifetime curves of samples with HfO_2 layers grown with different numbers of ALD cycles (hence thicknesses), deposited on *n*-type Si samples, and annealed for 30 min at 475 °C, structured as in Fig. 1(a). Fig. 3(b) shows effective lifetime values, and corresponding single-side J_{0s} values, for each of

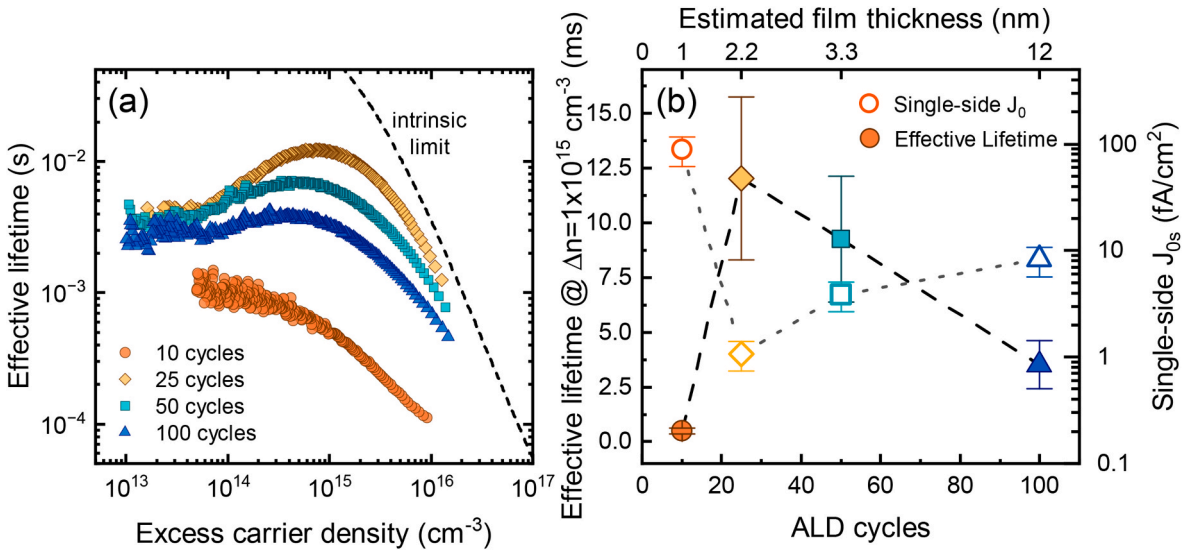

Fig. 3. (a) Effective lifetime curves for different HfO_2 films (10–100 cycles, corresponding to 1–12 nm estimated thickness), deposited via PE-ALD, on 150 μm 5 Ωcm *n*-type Cz-Si (100) wafers, annealed in air at 475 °C for 30 min. The intrinsic lifetime limit of Niewelt et al. [46] is also plotted. (b) Effective lifetimes extracted at an excess carrier density of 1×10^{15} cm^{-3} and single-side J_{0s} values for each film thickness in (a). Error bars correspond to the relative variation in measured values experienced between samples.

these samples, extracted at an excess carrier density of 10^{15} cm^{-3}. A clear trend can be seen, with the effective lifetime increasing as film thickness decreases from approximately 12 nm to 2.2 nm. However, the passivation level then rapidly decreases for thinner films, with the effective lifetime dropping by an order of magnitude. These results are in line with our previous investigations, which found that passivation quality peaks at a HfO_2 film thickness between 2.2 and 3.3 nm, achieving surface recombination values (SRVs) as low as 2.5 cm/s [23]. We have previously demonstrated that this change in passivation quality with film thickness is related to differences in levels of chemical and field-effect passivation [23], with 2.2–3.3 nm thick HfO_2 layers having higher levels of fixed charge and of chemical passivation (hence lower D_{it}) than films outside this thickness window. The effective lifetimes determined here for ~2.2 nm (25 cycles) of HfO_2 correspond to an SRV of 0.6 cm/s (single-side J_{0s} of ~1.1 fA/cm^2), the lowest SRV to date, and competitive with more conventional Al_2O_3 passivation [45].

Fig. 4 shows a comparison between the annealing temperature dependence of effective lifetimes for 'thin' and 'thick' HfO_2 films, with estimated thicknesses of 1 nm (10 cycles) and 12 nm (100 cycles), respectively. Notably, the impact of annealing temperature on effective lifetime remains consistent, regardless of film thickness, with optimal results found around 450 °C [19,23]. This implies a promising outlook on the application of HfO_2 films in passivating contacts fabricated with lower temperature processing – if effective diode structures can be produced using 1–2.2 nm thick HfO_2 layers, annealed at 450 °C. With 100 cycles HfO_2, we have previously demonstrated that good passivation is achieved with samples that have been annealed 450–475 °C, above the temperature required for the transition from amorphous to crystalline monoclinic HfO_2 [19]. To ascertain whether this crystallinity is a prerequisite for good passivation, each HfO_2 film thickness was characterised by XRD.

All films for XRD analysis were annealed at 475 °C, which is above the crystallisation temperature window previously observed for 100 ALD cycles of HfO_2 [19]. For 50–100 cycles of HfO_2 annealed at this

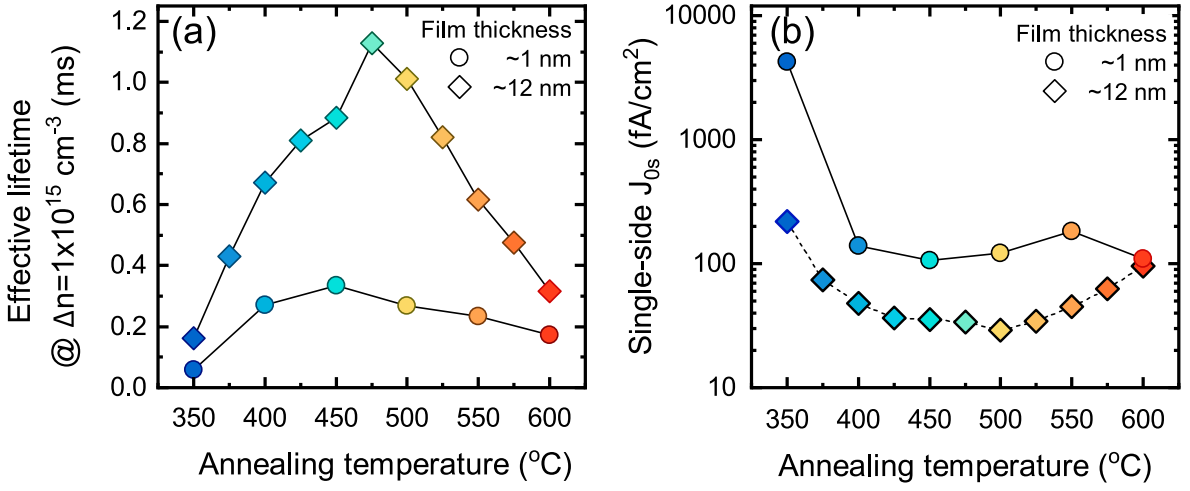

Fig. 4. (a) Effective lifetimes and (b) single-sided J_{0s} values extracted at an excess carrier density of 1×10^{15} cm^{-3} of HfO_2 films deposited via PE-ALD, on 150 μm 5 Ωcm *n*-type Cz-Si (100) wafers, annealed in air for 30 min at temperatures ranging from 350 to 600 °C. A comparison is made between 'thick' (~12 nm/100 cycles) and 'thin' (~1 nm/10 cycles) HfO_2 films. Effective lifetime data have been previously published in Refs. [19,23]. A discussion on extracting J_{0s} from the region around 1×10^{15} cm^{-3} can be found in Ref. [47].

temperature, the peaks present correspond to monoclinic HfO_2 [48], consistent with our prior work [19]. The main diffraction peaks corresponding to the monoclinic phase occur at 2θ = 15–45°, but with decreasing cycle number (and layer thickness), these peaks become broader and less distinct. By 25 cycles of HfO_2, no clear peaks are evident in this region. Instead, there is a low intensity 'hump' between 2θ = 25–35°, the position of which coincides with a similar feature observed for amorphous ALD-grown HfO_2, which we have previously published [19]. The features seen in the 2θ range of 50°—60° can be attributed to the (311) plane of the underlying c-Si (100) substrate [49]. Note that although no overlayer peaks could be detected with this set-up for ~1 nm (10 cycles) this does not mean that no HfO_2 is present on the surface, as the presence of HfO_2 has been verified *via* XPS [23].

The change in the XRD pattern for ~2.2 nm (25 cycles) of HfO_2 could indicate that the films are now amorphous, However, an alternative explanation may be that the GI-XRD is not sufficiently sensitive for characterisation of such ultra-thin films. Indeed, there are reports of HfO_2 thin films (<4 nm) appearing amorphous by XRD yet being determined as crystalline by other approaches [50]. In order to verify the XRD results obtained, HfO_2 samples were subjected to HF etching. Amorphous HfO_2 etches very quickly in dilute HF, whereas crystalline HfO_2 is resistant to HF etching [25,51]. Immersing 1 nm (10 cycles) HfO_2 in dilute (1%) HF for just 5 s is sufficient to remove the HfO_2 film completely, as verified *via* XPS and is associated with a loss of passivation [36], providing further evidence for a lack of crystallinity at this thickness. In order to evaluate the film crystallinity further, effective lifetime measurements were made for samples of each thickness following immersion in HF. The resulting effective lifetime values were used as an indication of film crystallinity – amorphous films etch quickly, resulting in considerable decreases in passivation, whilst crystalline films etch very slowly (if at all), with passivation level remaining stable. The results of this experiment are shown in Fig. 6.

As expected, passivation is lost for the ~1 nm films after just 5 s in dilute HF, whilst the ~12 nm samples are relatively stable (after an initial minor decrease in passivation). For the ~2.2 nm films the passivation takes roughly 3 times longer to be lost than in the ~1 nm case. When the difference in film thickness is considered, this suggests a similar etch rate for both sample types. The fact that the passivation is lost for these samples suggests that they have been fully etched and are therefore amorphous, which is in keeping with the results observed in Fig. 5. The passivation from the 12 nm films appears to stabilise after an initial decrease, whilst the ~3.3 nm samples show intermediary behaviour. As effective lifetimes can still be measured after 25 s, this suggests that the films have not been fully etched and are therefore more likely to be either fully crystallised or a mixture of amorphous and crystallised regions. ~2.2 and ~3.3 nm thick HfO_2 films having intermediary behaviour between that of ~1 and ~12 nm films is in keeping with the results presented in Fig. 3 (b). Good passivation is observed with films that do not appear fully crystalline, suggesting that the crystallisation of HfO_2 is not absolutely necessary for good passivation quality to be achieved.

Kelvin probe measurements can be used to determine the work function of a material [52], which is important when considering factors like conductivity and charge carrier tunnelling probability. For complex structures including dielectrics, the measured result is a combination of the semiconductor work function, the potential across the space charge region, and the potential across the dielectric layer, thus we instead refer to this as an 'effective' work function (EWF) [53]. This EWF contains information about the charge in the dielectric layer.

EWFs of the as-deposited films were measured, as shown in Fig. 7(a), with the EWFs for ~2.2–12 nm thick HfO_2 (5.1–5.25 eV) in good agreement irrespective of film thickness. There is a considerable decrease in EWF for ~1 nm (10 cycles) HfO_2, which has a measured EWF of 4.6 eV. The difference in EWF between ~1 nm and thicker films correlates with our previous findings, whereby similar fixed charge levels (which influence EWF) were observed for films >2 nm (20 cycles)

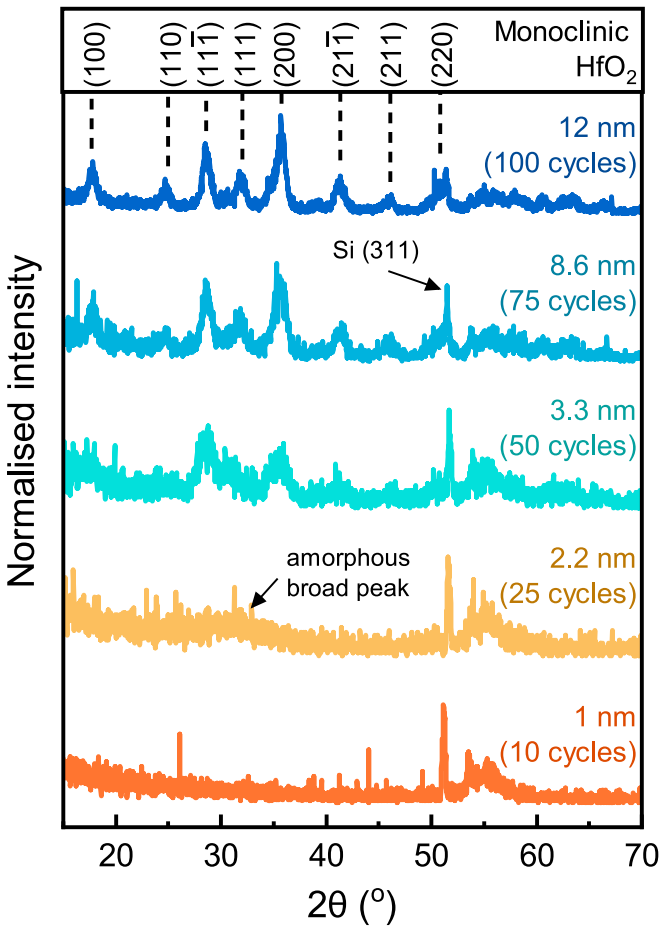

Fig. 5. GI-XRD measurements, using Cu $K_{\alpha 1/2}$, taken from polished silicon wafers coated with 10-100 cycles (corresponding to ~1–12 nm) of HfO_2 grown by ALD and annealed in air for 30 min at 475 °C. The main crystallographic planes present are labelled at the top. Patterns are vertically offset for clarity. To allow comparison, all patterns have been normalised to their most intense peak (generally the Si (311)). The sharp peak at 2θ = 26° in the 10 cycles HfO_2 pattern is thought to be an artefact, amplified by the normalisation process.

thick, while there was a considerable difference in fixed charge observed for ~1 nm (10 cycles) HfO_2 [23]. Following characterisation of the EWF at room temperature, samples were annealed *in situ* under vacuum at temperatures 25–500 °C. In all cases, EWF values remained relatively stable (within 0.1 eV) until ~300 °C. At annealing temperatures ≥300 °C, there is a marked, monotonic decrease in EWF for films ~2.2–12 nm (25–100 cycles) thick. For films ~1 nm (10 cycles) thick, there is a similar (albeit smaller) decrease from ~375 °C. For all films, EWF saturates with annealing at 400–500 °C, at which point all films studied have similar EWF (4.4–4.6 eV). The EWF values observed in this vacuum annealing experiment are of a similar order to our previous measurements conducted in air ambient, which also observed a considerable change in EWF at annealing temperatures 350–450 °C [19]. Our previous work found an increase in EWF at annealing temperatures ~350–450 °C, whereas here we observe a decrease in EWF. This differing behaviour could be ascribed to the different annealing ambients used in each case (air ambient and vacuum, respectively).

In addition to EWF as a function of vacuum annealing temperature, SPV was determined prior to, and following vacuum annealing. At all film thicknesses, negative SPV was measured suggesting the presence of negative charge, in line with our previous work [19,23]. There is a notable decrease in SPV magnitude (becoming less negative) for ~2.2–12 nm thick films (25–100 cycles) following vacuum annealing, although the trend is reversed for ~1 nm (10 cycles) HfO_2. SPV can

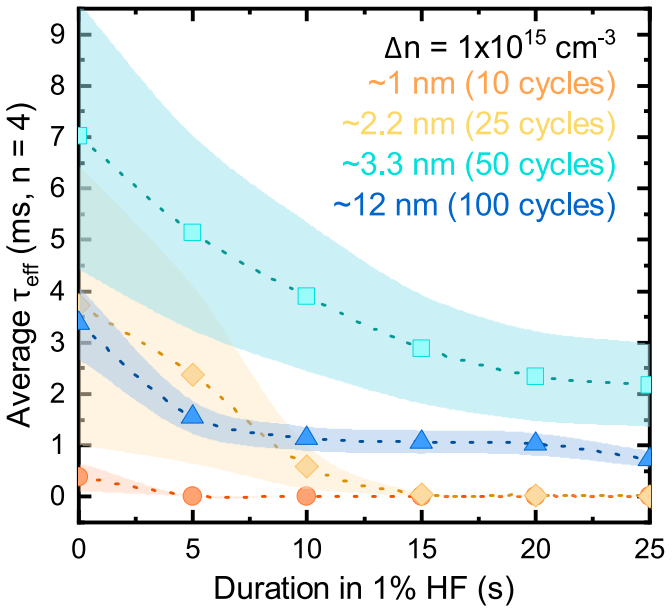

Fig. 6. Effective lifetime measurements for 150 μm 5 Ωcm *n*-type Si coated with 1 nm (10 cycles), 2.2 nm (25 cycles), 3.3 nm (50 cycles) and 12 nm (100 cycles) of HfO_2 annealed at 475 °C as a function of 1% HF immersion duration. Each data point corresponds to the average effective lifetime measured for four samples, and the error bands correspond to the experienced variation for samples of that thickness.

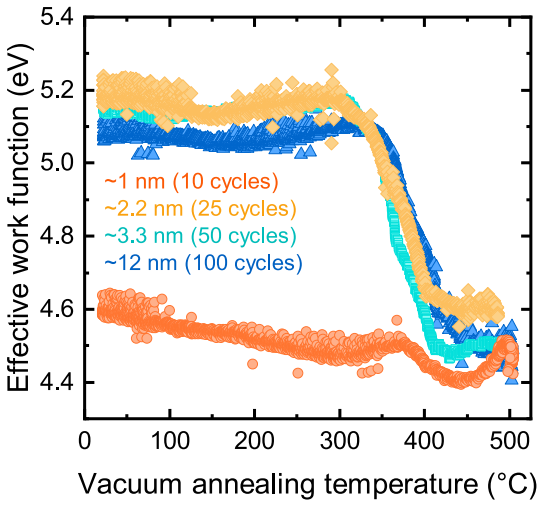

Fig. 7. Kelvin probe data acquired during *in situ* vacuum annealing of HfO_2 films with different thicknesses. Sample structure for these experiments can be seen in Fig. 1(c). Effective work function is measured as a function of increasing temperature for silicon wafers coated with 10-100 cycles (corresponding to ~1–12 nm) of HfO_2.

indicate the quantity of charge present, but results can be highly variable and dependent on both material properties and surface preparation effects [33,54,55]. It should be noted that the vacuum annealing step may influence passivation quality, as suggested by the reduction in SPV, as well as the film crystallinity. Several reports indicate that HfO_2 films annealed under vacuum need temperatures of 500 °C to crystallise [56–58] rather than the 300 °C crystallisation temperature observed elsewhere [22,35,42].

3.2. Contact optimisation

To maximise c-Si solar cell efficiency, the recombination current density at the surface (J_{0s}) needs to be minimised [12]. Good passivating contacts/interlayers feature J_{0s} values of ≪10 fA/cm^2 [12,59]. However, for passivating contacts, J_{0s} is not the only metric under consideration, as contact resistivity (ρ_c) must also be minimised for competitive cell efficiencies [12]. Although ~2.2 nm (25 cycles) HfO_2 gave the most promising passivation, the HfO_2 should be kept as thin as possible to maximise charge carrier transport, according to Equation (1). Prior computational studies show that contact resistivity for HfO_2 is only competitive as a hole selective contact when the films are ≤1.4 nm thick [15]. Thus ~1 nm (10 cycles) HfO_2 was used as a starting point for passivating contact experiments.

Fig. 8 compares Al and Au front contacts on top of ~1 nm (10 cycles) of as-deposited HfO_2, for *n*- and *p*-type Si substrates, with full area Au rear contacts. A depiction of this sample structure can be seen in Fig. 1 (e). In all cases, the front contacts remained un-sintered, to avoid damaging the Au rear contacts.

The samples with the strongest diode response were the *n*- and *p*-type Au/Si/HfO_2/Al structures, in Fig. 8(a) and (b) respectively. The *n*-type variant resulted in higher absolute current values than the *p*-type counterpart and had a clearer relation between current and contact size, with smaller diodes resulting in reduced current, as is necessary for the application of the ECSM. However, the shape of these diode curves is not ideal, with a considerable increase in current below the forward threshold voltage (at approximately 1.5 V), indicating non-negligible shunting. This shunt could possibly be a result of the e-beam evaporation process, whereby the Al may be driven down to the Si surface, creating a direct Al-*n*Si contact.

In the case of both *n*- and *p*-type substrates, the current values for the Au/Si/HfO_2/Au samples are lower than their Au/Si/HfO_2/Al counterparts, though both still produce a clear relation between current and contact size, as seen in Fig. 8(c) and (d). Again, the absolute current is higher in the *n*-type variant than the *p*-type. The shunt resistance is also less apparent in these structures, though this is difficult to determine due to the shape of the IV curves. In the case of the Au/*p*Si/HfO_2/Au sample structure (Fig. 8(d)), there is no consistent threshold voltage across the different contact sizes. Based upon these results, and the higher quality passivation for *n*-type substrates than *p*-type (see Table 1), it appears that HfO_2 is more suitable as an electron-selective contact. HfO_2 grown under our conditions on *p*-type substrates currently passivates less well than on *n*-type substrates, but this process has not yet been fully optimised. Hence, further investigations herein focus on the use of *n*-type substrates with an Au/Si/HfO_2/Al sample structure. However, a recent investigation found that HfO_2 has potential to be an effective hole selective contact on *p*-type substrates under certain conditions [15]. Optimising HfO_2 passivation on *p*-type silicon and the exploration of its charge carrier selectivity was beyond the scope of this work, but is an avenue for potential future exploration.

3.3. Variations of the HfO_2 layer

Fig. 9(a) shows various IV measurements for different contact sizes, taken on a sample with a ~1 nm (10 cycle) as-deposited HfO_2 layer. Six different contact sizes were considered, with three measurements taken for each contact size. In general, the samples show an approximate diode response, with current decreasing as contact size decreases, which is the required behaviour to apply the ECSM. However, the shunting is notably below the forward threshold voltage at 1.5 V, which thus complicates the analysis. This shunt appears to be more pronounced for larger contact sizes but has a negligible impact on the reverse bias measurements. Additionally, the results are relatively inconsistent between contacts of the same geometry, with some contacts producing considerably different IV curve characteristics, for example the blue curve in Fig. 9(a). Overall, these data are not ideal for the application of the ECSM.

It is still possible to extract contact resistivity values through the ECSM by selecting consistent IV data across the six different contact

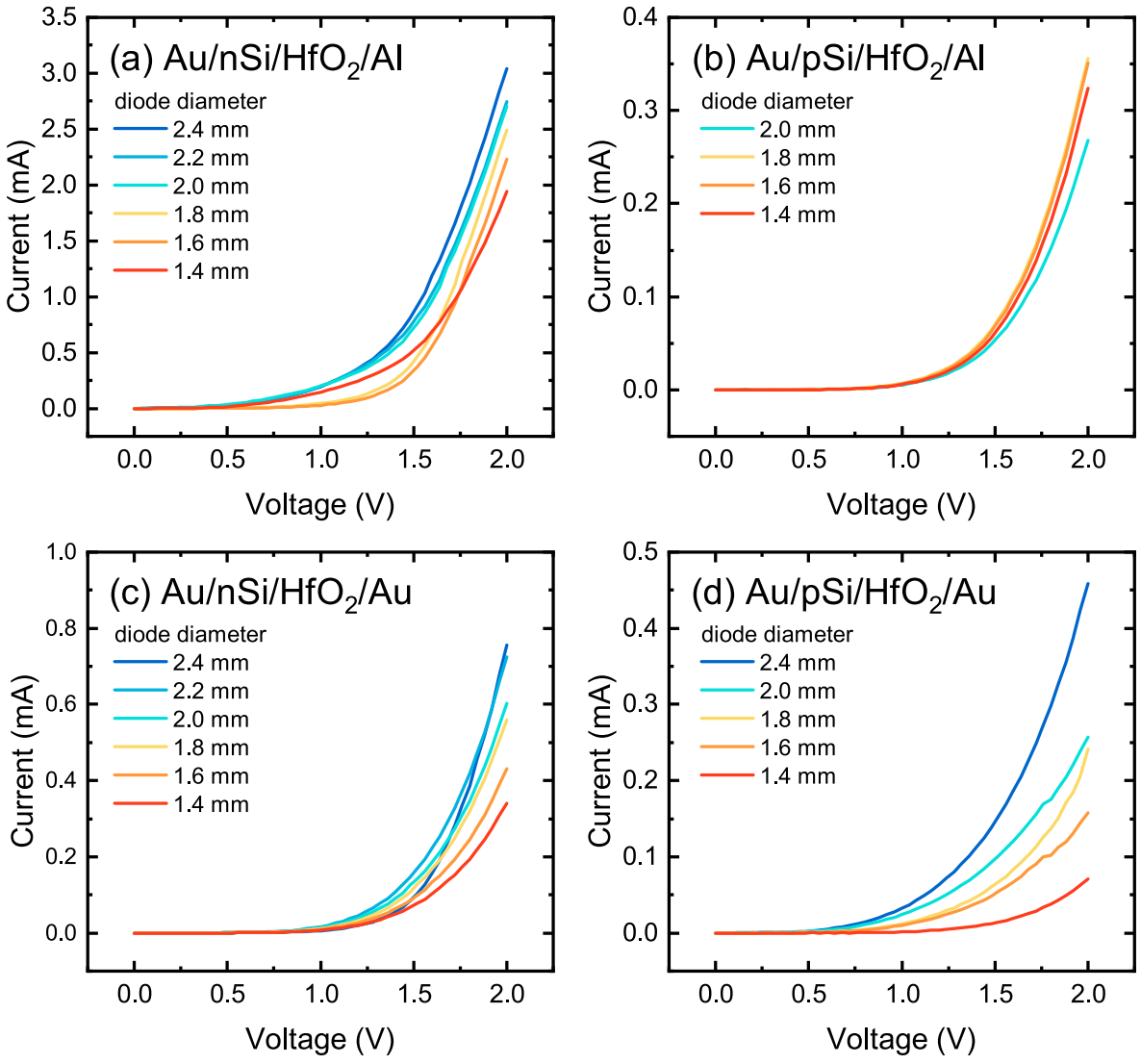

Fig. 8. Current-voltage characteristics of various metal-HfO_2-Si contact structures (corresponding to structure (e) in Fig. 1), with 1 nm (10 cycles) of as-deposited HfO_2, full area Au rear contacts and mm-scale circular metallic front contacts on 5 Ωcm Si. Sample structures include: (a) Au/*n*Si/HfO_2/Al, (b) Au/*p*Si/HfO_2/Al, (c) Au/*n*Si/HfO_2/Au, and (d) Au/*p*Si/HfO_2/Au.

sizes; however, these values should be considered as an estimate rather than a precise result. The result of these calculations for varying HfO_2 film thickness can be seen in Fig. 9(b). Contact resistivity values are determined to be in the order of 1 Ωcm^2 which, at first glance, would suggest poor performance from the HfO_2 sample structures. However, the difference between 0 cycles of HfO_2 – *i.e.,* Al directly on Si (structure d in Fig. 1) – and 10 cycles of HfO_2 (structure e in Fig. 1) is only 100–300 $m\Omega cm^2$. This indicates that the limiting factor in these measurements is more likely related to the metal contacts rather than the HfO_2 layer itself. Potential contributing factors have been highlighted previously in this manuscript (e.g., contact fabrication *via* electron-beam deposition, metal electrode thickness, surface quality prior to contact fabrication). As the focus of this study was on the HfO_2 layer alone, these factors are not yet optimised, but will be the focus of further investigations. Achieving a contact resistivity 100 $m\Omega cm^2$ is often considered a benchmark, as this is considered a maximum contact resistivity a full area contact structure can have where no significant power conversion efficiency (PCE) losses occur [1,15]. The potential of the HfO_2 layer may become more apparent if included in a better performing contact structure.

The contact resistivity increases substantially with thicker HfO_2 layers, with the value at ~2 nm (20 cycles) an order of magnitude higher than at ~1 nm (10 cycles). By ~3 nm (30 cycles) current values were indistinguishable from the measurement noise of the experimental setup, and so even an approximation of contact resistivity was not possible. These results suggest that ultra-thin (<2 nm) as-deposited HfO_2 films show some promise as interlayers in contact structures, though more investigation into the surrounding contact structure is required. Although our prior work demonstrated that pinholes could be induced in HfO_2 [25], the observed relationship between film thickness and contact resistivity suggests that in this structure, charge transport is principally *via* charge carrier tunnelling, rather than *via* pinholes, based on Equation (1).

Fig. 10 shows a plot of conductance (defined as the reciprocal of resistance), calculated above the forward threshold voltage, against the annealing temperature of a ~1 nm (10 cycle) HfO_2 layer (before contact deposition), with each colour representing a different contact size. Since the contact resistivity values extracted from these data through the ECSM cannot be reported to a high degree of accuracy, it was necessary to use a different metric to compare between samples that resulted in similar levels of performance.

Lower temperature anneals result in higher conductance, with a peak in performance occurring between 275 and 325 °C. After annealing at higher temperatures there is a downward shift in the data,

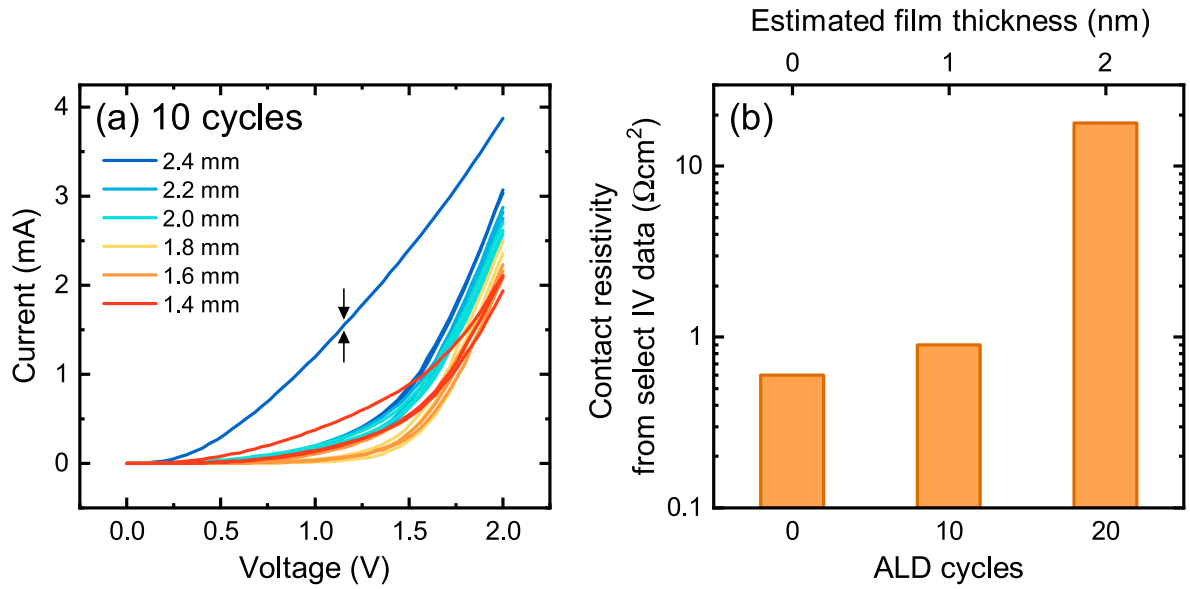

Fig. 9. (a) Repeated current-voltage measurements, with various metal front contact diameters, for an Au/*n*Si/HfO_2/Al contact structure (Fig. 1(e)), with 1 nm (10 cycles) of as-deposited HfO_2 (no activation anneal). The arrows highlight an example of IV characteristics that do not fit the typical diode response. (b) Approximate contact resistivity measurements, calculated from applying the ECSM to select IV data. These values are intended as a guide.

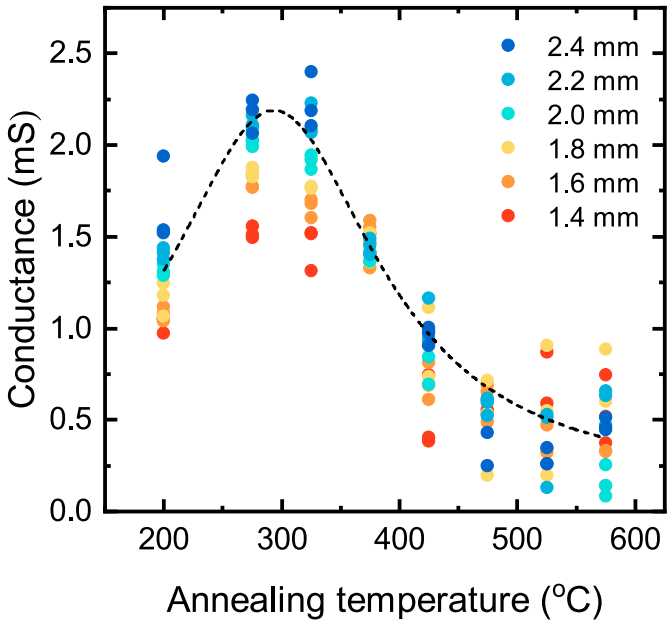

Fig. 10. A comparison between sample conductance (1/R) and HfO_2 annealing temperature, for an Au/*n*Si/HfO_2/Al sample structure (Fig. 1(e)), with ~1 nm (10 cycles) of HfO_2 on 5 Ωcm Si. Different metal front contact diameters are represented by different coloured data points. The dashed line provides a guide for the eye.

corresponding to an increase in resistance, which then plateaus around 475 °C. This shift in resistance is unlikely related to crystallisation of the material, despite the temperature range aligning with the previously determined crystallisation region for thicker HfO_2 films [19], as these ultra-thin films (~1 nm) appear to remain amorphous at these temperatures, demonstrated through the XRD results in Fig. 5 and etching results in Fig. 6.

Additionally, the lower temperature samples show a clear relation between resistance and contact size, with larger contacts resulting in higher conductance. This trend is lost for samples annealed above 375 °C, indicating that more complex mechanisms of carrier transport may become involved for samples annealed in this higher temperature range. The loss of a current to contact size dependence is seen in all contact structures considered in Fig. 8, once the HfO_2 layer is annealed at temperatures above 375 °C. From these data, it can be concluded that samples annealed at lower temperatures, (<375 °C) create better performing contact structures than those annealed at higher temperatures. This conflicts with the passivating performance of HfO_2 films, in which it has been shown that higher annealing temperatures (~450 °C) are necessary for high quality passivation [19].

4. Conclusion

We have studied the thickness dependence of HfO_2 films, highlighting a peak in passivation performance around 2.2 nm thick, for films annealed at 475 °C. XRD measurements suggest that although 12 nm HfO_2 films annealed at 475 °C have a crystallised monoclinic structure, with decreasing film thickness films stay more amorphous. The lack of crystallinity observed for thin films annealed at this temperature, in conjunction with the good passivation performance, contradicts prior reports suggesting that HfO_2 passivation may rely on a crystallised film [19]. Kelvin probe measurements demonstrate a difference in EWF for ~1 nm (10 cycles) and ~2.2–12 nm (25–100 cycles) films prior to annealing, although following vacuum annealing there is closer agreement between the values. Through KP measurements we also observe a strong change in EWF at annealing temperatures coincident with the onset of passivation.

Alongside the material characterisation of HfO_2, we have conducted a preliminary study into the application of thin HfO_2 layers in passivating contact structures. Using a simple contact resistance measurement architecture and low-temperature processing we found the best performance with an Au/*n*Si/HfO_2/Al sample structure. The thickness dependence of contact resistivity was estimated using the ECSM, though the non-ideal IV characteristics of these samples limits the accuracy of this approach. Apparent shunting may be due to metal implantation from the high energy e-beam process, resulting in a one-directional shunt.

The annealing temperature dependence of contact resistance of the Au/*n*Si/HfO_2/Al samples is investigated through conductance measurements, and we find that resistance is lowest for samples annealed below 375 °C. For annealing at higher temperatures, the resistance

increases and the relation between current values and contact size is lost, indicating a change in carrier transport mechanisms. This shift in performance is consistent with the crystallisation region of HfO_2, however, as demonstrated by XRD, the ultra-thin HfO_2 layers should remain amorphous. This suggests that there are other factors influencing the material within this temperature region, perhaps including a change in dielectric charge. Unfortunately, the temperature dependence of the sample contact performance and passivation work in opposing directions, as passivation has been shown to peak around 475 °C, which is significantly higher than the optimal temperature range for the contact performance.

HfO_2 has been established to have excellent passivation, particularly at the sub-10 nm scale, which would make it a promising candidate for applications in passivating contact structures. This work provides a preliminary exploration of the topic, highlighting changes in performance resulting from HfO_2 film thickness and annealing temperature. Further work to optimise the contact structure to achieve ideal diode performance is required, and this may require increasing the complexity of the contact architecture and thermal budget.

Access to data statement

Data underpinning figures in this paper can be freely downloaded from https://wrap.warwick.ac.uk/75493. Requests for additional data should be made directly to the corresponding author.

CRediT authorship contribution statement

A. Wratten: Methodology, Investigation, Conceptualization, Formal analysis, Validation, Visualization, Writing – original draft. **S.L. Pain:** Investigation, Validation, Visualization, Writing – original draft. **A. Yadav:** Investigation, Writing – review & editing. **E. Khorani:** Investigation, Writing – review & editing. **T. Niewelt:** Conceptualization, Writing – review & editing. **L. Black:** Supervision, Investigation, Writing – review & editing. **G. Bartholazzi:** Investigation, Writing – review & editing. **D. Walker:** Investigation, Writing – review & editing. **N.E. Grant:** Supervision, Conceptualization, Writing – review & editing. **J.D. Murphy:** Conceptualization, Funding acquisition, Project administration, Resources, Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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