Measurements and Review of Failure Mechanisms and Reliability Constraints of 4H-SiC Power MOSFETs Under Short Circuit Events

Renze Yu, *Graduate Student Member, IEEE,* Saeed Jahdi, *Senior Member, IEEE,* Olayiwola Alatise, *Senior Member, IEEE,* Jose Ortiz-Gonzalez, *Member, IEEE,* Sai Priya Munagala, Nick Simpson, *Member, IEEE,* and Phil Mellor, *Member, IEEE*

***Abstract*—The reliability of the SiC MOSFET has always been a factor hindering the device application, especially under high voltage and high current conditions, such as in the short circuit events. This paper experimentally reviews the failure mechanisms caused by destructive short circuit impulses, and investigates the degradation patterns of key electrical parameters under repetitive short circuit events. The impact of test parameters on the short circuit reliability of SiC MOSFET has been analyzed. Approaches to characterize the electrical-thermal-mechanical stress during the short circuit period and advanced test methods are highlighted. Finally, the constraints from the standpoint of both manufacturers and users have been presented, including comparison of current SiC MOSFET devices, reliability evaluation of parallel SiC MOSFET devices, reliability improvement of the chip, performance improvement of protection circuits, and reliability assessment of SiC MOSFET devices under application-representative stress.**

***Index Terms*—Device Degradation, Failure Mechanism, Modeling, Reliability, SiC MOSFET, Short Circuit**

I. Introduction

COMPARED with Silicon (Si), wide-bandgap semiconductors such as Silicon Carbide (SiC) have better properties like higher breakdown field, higher thermal conductivity, and higher electron mobility. The wider bandgap of SiC offers a higher operating temperature. A higher breakdown field is advantageous to reduce the chip size, capacitance, and on-state resistance (R_{on}). Higher thermal conductivity contributes to better heat dissipation and less thermal resistance. Higher electron mobility is conducive to higher switching capability and higher current density. Thus, power electronic systems using SiC devices have become more compact, more efficient, and more lightweight in contrast with Si Insulated Gate Bipolar Transistor (IGBT) counterparts, and SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices are the most popular one among all SiC devices [1]–[4].

R. Yu, S. Jahdi, S. P. Munagala, N. Simpson and P. Mellor, are with the Electrical Energy Management Group, School of Electrical, Electronics and Mechanical Engineering, University of Bristol, Bristol BS8 1UB, U.K. (e-mail: renze.yu@bristol.ac.uk, saeed.jahdi@bristol.ac.uk, priya.munagala@bristol.ac.uk, nick.simpson@bristol.ac.uk, p.h.mellor@bristol.ac.uk)

O. Alatise and J. O. Gonzalez are with are School of Engineering, University of Warwick, Coventry CV4 7AL, U.K. (e-mail: O.Alatise@warwick.ac.uk, J.A.Ortiz-Gonzalez@warwick.ac.uk)

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Although SiC MOSFETs outperform Si counterparts under several circumstances, the reliability of SiC MOSFET devices is not very desirable, especially under extreme conditions. The instant, simultaneous high voltage and high current will cause larger and more concentrated electrical-thermal stress to a smaller die, which might be beyond the capability of the device and result in destructive failure [5]. On the other hand, the gate oxide of SiC MOSFET is another reliability concern compared with Si IGBT [6], [7]. First, the defect density in the SiC/SiO_2 interface is approximately two orders of magnitude higher than that of Si/SiO_2 interface, which strongly affects the overall performance of the device. Second, the lower energy band offset between SiC/SiO_2 interface and higher temperature dependency of the barrier height are also responsible for the instability of the gate oxide. Tunnelling and injection of carriers into the gate oxide will result in higher leakage current. Finally, the gate oxide of the SiC MOSFET device is deigned thinner to obtain acceptable threshold voltage (V_{th}), which means that the gate oxide suffers from higher electrical-thermal-mechanical stress under the same operating conditions [8], [9].

Short circuit is one of the worst working conditions for power devices. It happens when the load is shorted by the false trigger of the gate driver or the error in control strategy. Large power dissipation in this short period induces rapid temperature rise and has the possibility to destroy the device instantly. In industry, power devices are required to be able to withstand the short circuit fault for at least 10 μs before the protection circuit operates [10], [11]. This is not a problem for Si IGBT devices, but it is a challenge for SiC MOSFET devices. It has been reported that the typical short circuit withstand time (SCWT) for commercial SiC MOSFET devices is within 2-7 μs, and it is even shorter at elevated temperatures and voltages [12], [13]. Therefore, it is significant to investigate the failure mechanism under short circuit events so as to know the weakest location inside the device. Also, it is important to figure out the impact of test conditions on device reliability to provide reference for device application and protection.

Furthermore, it is possible that the device survives after one short circuit impulse, but suffers from repeated short circuit events throughout its operation time. In this case, the electrical parameters will degrade and the performance of the SiC MOSFET device will deteriorate over time. In order to further evaluate the health status and calculate the lifetime

of the SiC MOSFET device, knowing how and why these parameters change in the long run is meaningful.

Except for short circuit tests, many researchers have established simulation models to analyze the internal device behaviour during the short circuit period. For example, a Technology Computer Aided Design (TCAD) model was built to simulate the current distribution inside the device [14]. An analytical thermal model depending on temperature and drift region thickness was proposed in [15]. In [16], an electrical-thermal model was presented to simulate the failure mechanism in the short circuit event. A multiphysics model was proposed in [17] to reveal the thermal-mechanical stress of the chip in the transient period. Recently, advanced online test methods have also been proposed to inspect the surface morphology and health status of SiC MOSFET devices [18], [19], which are useful tools to analyze the device failure mechanism and monitor the long-term reliability under the short circuit conditions.

Although existing literature provides valuable references for the short circuit reliability research of SiC MOSFET, a comprehensive summary of the current work from failure mechanism, degradation pattern, effect of test condition, to modeling method is still missing. Hence, the paper is written aimed at four purposes: (1) To summarize different failure and degradation mechanisms of SiC MOSFET devices under different test conditions, (2) To illustrate the latest methods to reproduce the short circuit behaviour of the SiC MOSFET devices, (3) To highlight issues on chip technology, short circuit protection, lifetime prediction of SiC MOSFET devices, (4) To propose meaningful feedback to manufacturers and users about the short circuit reliability research. Contents of the paper are arranged as follows: Section II introduces different failure modes in destructive short circuit conditions. Section III focuses on the degradation of electrical parameters and related mechanisms. The impact of test conditions on device reliability is analyzed in Section IV. Section V describes how to characterize the short circuit performance of SiC MOSFET devices during the short circuit. Five perspectives for future research are put forward in Section VI, and Section VII concludes the paper.

II. Analysis of Failure Modes under Destructive Short Circuit Events

To gain better knowledge of the short circuit reliability SiC MOSFET and optimize the device thereafter, it is necessary to conduct in-depth research on the failure mechanism to know why the device fails, how the failure is reflected and where the fragile part is.

A. Typical Short Circuit Characteristics

Typical short circuit waveforms of voltage and current are shown in Fig. 1. The short circuit event can be divided into four phases:

(1) The short circuit fault starts at t_0, and the dc-link voltage is directly applied on the conducting SiC MOSFET device. Because of the low resistance in the main circuit, the current increases rapidly, and the device shifts from the cutoff region to the saturation region. The dc-link voltage has a small voltage drop induced by stray inductance in the circuit but recovers quickly. The short circuit current reaches the peak (I_{peak}) at t_1. The huge instant power causes a large temperature rise inside the SiC MOSFET chip.

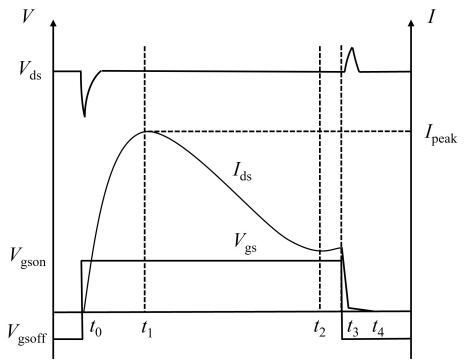

Fig. 1. Typical current and voltage waveforms for a SiC MOSFET device under short circuit event.

(2) The device still works in saturation region between t_1 to t_2. The voltage on the device remains unchanged as the dc-link voltage and the temperature continues to increase in this period, leading to the increase of acoustic scattering and surface roughness scattering, which brings about the negative temperature coefficient of carrier mobility [20]. The drain-source current (I_{ds}) begins to decrease and exhibits a negative slope.

(3) As the temperature continues to increase from t_2 to t_3, more thermal carriers will be activated and leakage current can be generated. If the decreasing rate of the channel current is slower than the increasing rate of the leakage current caused by thermal excitation, the current slope changes to positive, and I_{ds} increases again. Also, the high temperature and high electric field are likely to induce the injection of carriers into the gate oxide, increasing the gate leakage current and decreasing the gate voltage (V_{gs}). If the device is overheat, the device will no longer be controllable and thermal runaway failure will happen.

(4) The short circuit fault is removed when the negative gate bias is applied at t_3. From t_3 to t_4, the short circuit current reduces quickly, but there might be a current tail that occurs at the end of the short circuit event, which is the aforementioned leakage current caused by thermal excitation. The device can be safely turned off on the condition that the short circuit energy does not exceed the safe operating area (SOA).

B. Failure modes 1: Thermal Runaway Failure

Thermal runaway failure tends to happen under high drain-source voltage (V_{ds}) conditions, where a steep temperature rise inside the SiC MOSFET chip is induced within only a few μs [21]–[24]. When thermal runaway failure is triggered, a change in the current slope and a tail current are often observed [21], [25]–[29]. This is caused by the generation of carriers in the drift region induced by the high temperature. Large amounts of electrons and holes are generated because of the high voltage and high

temperature during the short circuit. The electrons and holes will increase the current density, further increasing the chip temperature and forming positive feedback. Eventually, the device fails due to thermal runaway. Another mechanism leading to thermal runaway is the latch-up of the parasitic NPN transistor (N-drift/P-well/N^+-channel region) inside the MOSFET [8], [10], [30], [31]. This will happen when the current flowing through the P-well region is large enough to activate the parasitic Bipolar Junction Transistor (BJT). The current is generated by the high electric field across the P-well/N-drift region and high temperature. Once this current is large enough and the parasitic BJT becomes uncontrollable, thermal runaway will happen. Eventually, the temperature is so high to melt the Al and is able to form a hot spot or burnt area on the chip. Typical waveforms under this failure mechanism are illustrated in Fig. 2. Under V_{ds} of 600 V and after 9 μs of short circuit stress, negative V_{gs} is applied to turn off the device, but a large leakage current can still be seen. Combined with the high V_{ds}, the temperature inside the device keeps increasing and more electron-hole pairs are generated, which in turn increases the current and temperature. In the end, thermal runaway failure happens in 4-5 μs after turn-off. The surface of the chip after failure is shown in Fig. 3. The device has been exploded in the experiment, and the Al on the chip surface was totally melt.

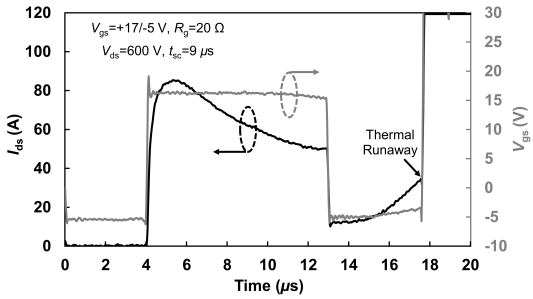

Fig. 2. Typical current and voltage waveforms under thermal runaway failure.

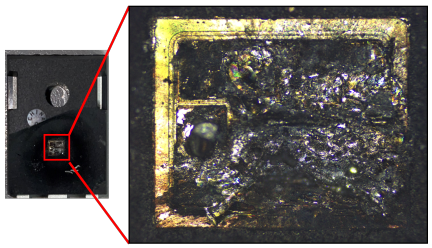

Fig. 3. Exploded device and surface of the SiC MOSFET chip under thermal runaway failure.

C. Failure Modes 2: Gate Destruction

Different from the failure mode caused by the rapid temperature rise, gate failure is more likely to happen under lower temperature and longer time duration (t_{sc}) occasions, which means the device is heated up at a lower speed, and the final temperature is not high enough to induce the massive generation of electron-hole pairs to cause thermal runaway [26], [28], [32].

Gate destruction is reflected by the malfunction of the gate oxide. The failure mode is the sudden short circuit between the gate and source electrodes. Typical waveforms causing gate destruction is plotted in Fig. 4. In this condition, the device is short-circuited for 30 μs under V_{ds} of 300 V . After the device is switched off by a negative V_{gs} for 6 μs, the gate and source electrodes are short-circuited. Compared with the previous situation, V_{ds} is much lower and t_{sc} is increased by twofold. In [33], post failure analysis by Scanning Electron Eicroscope (SEM) and Focused Ion Beam (FIB) found out that the SiO_2 between the gate and source electrodes has cracked after gate destruction. Silicon particles and deformation of Al material were observed near the gate oxide. In [34], the composition of elements was detected using Energy Dispersive Spectrometer (EDS) after the device failed. A notable increase of Al (71.58% in atomic scale) was found near the gate oxide crack. A thermal-mechanical model was further built to simulate the chip temperature and oxide stress in the short circuit period. The failure mechanism can be explained as follow: At the beginning of the short circuit impulse, the temperature inside the device began to increase. The stress between the Al and gate oxide increased because of the increasing temperature difference. After several microseconds, the maximum stress of oxide reached above the strength limit of the SiO_2, and caused the rupture of the gate oxide. However, the temperature at this moment was not high enough to melt the Al, it kept increasing until exceeding the melting point of Al. The molten Al gradually sept into the crack and led to the short circuit of the gate in a short period of time. Since it takes time to cause crack and fully short circuit the gate oxide, this kind of failure often happens in long-time short circuit events [23], [35].

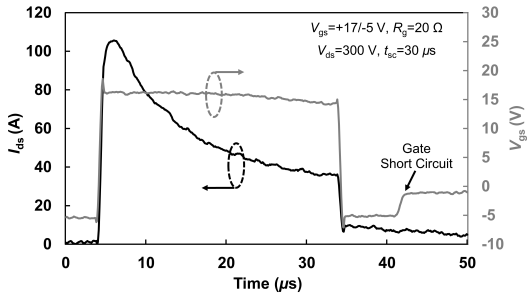

Fig. 4. Typical current and voltage waveforms under gate failure.

Two failure mechanisms of SiC MOSFET in the short circuit event are more straightforwardly demonstrated in Fig. 5. To summarize, when the junction temperature (T_j) rises relatively quickly to a high value during the short circuit, a large number of carriers will be generated. The positive feedback between the generated current and increasing temperature will eventually cause the thermal runaway of the chip. The critical value for this failure is T_{RWF}. However, if T_j rises at a slower speed with a longer time, there will be enough time to accumulate thermal-mechanical stress. Once the temperature is high enough (T_{GF}) to melt the Al, the molten Al will infiltrate

into the ruptured oxide and cause the short circuit of the gate.

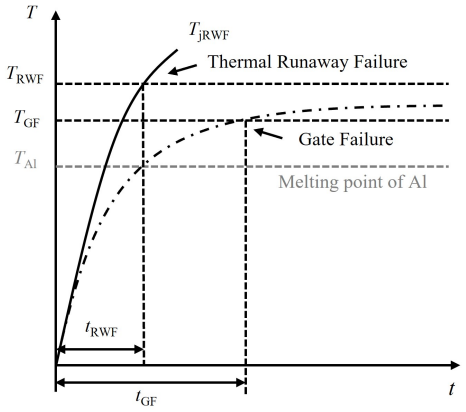

Fig. 5. Summary of failure mechanisms of the SiC MOSFET under different short circuit conditions [26].

III. Degradation of SiC MOSFET in Repetitive Short Circuit Conditions

Repetitive short circuit events are more likely to happen compared with single, destructive short circuit impulse because the action of the short circuit protection circuit will protect the device from instant failure. Under repetitive short circuit events, the short circuit energy is not high enough to cause the direct failure, but the electrical-thermal-mechanical stress will cause the gradual degradation of the chip, which affects the electrical performance and long-term reliability of the device. Thus, it is meaningful to investigate the degradation of chip parameters in order to provide information for health monitoring and reliability assessment of SiC MOSFET devices.

A. Static Parameters

1) V_{th}: Most reliability issues in SiC MOSFET can be explained by the vulnerable gate oxide and unstable V_{th} [7]. Compared with Si IGBT, the gate oxide in SiC MOSFET is much thinner to ensure a low V_{th} and transconductance [36]. Hence, its gate oxide suffers from higher stress compared with Si counterparts. Besides, the gate oxide in SiC MOSFET is of poor quality due to the presence of carbon atoms and manufacturing technology. High-density defects take part in the trapping near the SiC/SiO_2 interface and result in the parameter drift over time [37], [38]. The relationship between V_{th} and interface charge is expressed in Eq. 1 in [39]:

$$V_{th} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}} \quad (1)$$

where ε_S is the dielectric constant of SiC material, k is the Boltzmann's constant, T is the lattice temperature, N_A denotes the doping concentration in the P-region, n_i represents the intrinsic carrier concentration, C_{ox} is the gate oxide capacitance, Q_{ox} is the accumulated charges in the gate oxide, and q is the electronic charge. It can be deduced that the capture of positive charges leads to the decrease in V_{th}, and the capture of negative charges leads to the increase in V_{th}. In [40], two different changing trends of V_{th} were observed: Under the test condition at V_{gs}=20 V and V_{ds}=600 V, an increase in V_{th} happened when t_{sc} was 3.3 μs, a change from negative to positive variation of V_{th} was seen when t_{sc} was 2 μs; and a complete negative change was observed when t_{sc} was shortened to 0.8 μs. A similar phenomenon was also observed in [41]. V_{th} decreased until t_{sc} reached 4 μs and after that, V_{th} shifted positively with short circuit time. This was explained by the competition of different mechanisms as stated in [37]. At the beginning of the short circuit event, the intrinsic electrical potential in the JFET region was lower than the gate oxide. Holes generated from impact ionization can gain enough energy from the electric field and overcome the SiC/SiO_2 barrier, causing a negative V_{th} bias. When t_{sc} was prolonged, the effect of impact ionization was mitigated, and high energy electrons that were able to overcome the barrier became dominated, which led to the increase of V_{th}. When t_{sc} was long enough, thermally activated electrons became absolutely dominant and presented a pure positive change in V_{th}. It should be mentioned that the occurrence of V_{th} turn around depends on the accumulated charge state in the oxide [42]. There is also a chance that the shift of V_{th} gradually recovers once the electrical stress is removed on the condition that there is no permanent destruction of gate oxide [43].

2) R_{on} and I_{ds}: For SiC MOSFET, R_{on} is mainly constituted of source contact resistance (R_{cs}), channel resistance (R_{ch}), accumulation resistance (R_a), drift region resistance (R_{epi}), N^+ substrate resistance (R_{sub}) and drain contact resistance (R_{con}). Although R_{on} is mostly decided by R_{ch} and R_{epi}, the change of R_{on} is mostly influenced by the change of V_{th}, and only R_{ch} and R_a are related to V_{th}. The dependency of R_{ch}, R_a and I_{ds} on V_{th} is shown in Eq. 2-Eq. 4 in [44].

$$R_{ch} = \frac{L_{ch}}{W_{ch}}\mu_n C_{ox}\left(V_{gs} - V_{th}\right) \quad (2)$$

$$R_a = \frac{L_a}{W_a \mu_{na} C_{ox}\left(V_{gs} - V_{th}\right)} \quad (3)$$

$$I_{ds} = \frac{W_{ch}\mu_n C_{ox}}{L_{ch}}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right] \quad (4)$$

where L_{ch} is the length of the channel, W_{ch} is the width of the channel, μ_n is the mobility of electrons in the channel, L_a is the length of the accumulation area, W_a is the width of the accumulation area, and μ_{na} is the mobility of electrons in the accumulation area. The injected high-energy electrons caused by high temperature and high electric field lead to the positive shift in V_{th}, which increases the R_{ch}, R_a and overall R_{on}. Moreover, the increase of R_{on} could also be caused by the deterioration of the Al metallization layer or the packaging of the device (such as the lift-off of bond-wire), as reported in [27], [45].

3) I_{gss}: Gate leakage current (I_{gss}) can be used to evaluate the degradation of the gate oxide. In repetitive short circuit tests, if I_{gss} is minor and stable, then the gate oxide is healthy. If I_{gss} increases sharply with short circuit cycles, then the gate oxide has suffered from irreversible degradation. The

degradation of the gate oxide are attributed to two main mechanisms. One is related to the electrical-related factor, which is cumulative-carrier-induced electric breakdown: the accumulation of carrier injection is speculated to lead to the increase in I_{gss}. Once the accumulated carrier reaches a certain amount or they are close enough to form a great local electric field, the gate oxide will break down [9], [46], [47]. The other failure mechanism is caused by the thermal-mechanical stress, which is associated with the conductive path as a result of the oxide crack and Al infiltration and is similar to the singular short circuit failure [48], [49]. In practice, the large I_{gss} will increase the voltage drop shared by gate resistance (R_g) and reduce the V_{gs} that is actually applied on the chip, which will increase the R_{on} and reduce the switching speed of the SiC MOSFET device. Typical I_{gss} and V_{gs} degradation patterns with the progress of repetitive stress are shown in Fig. 6.

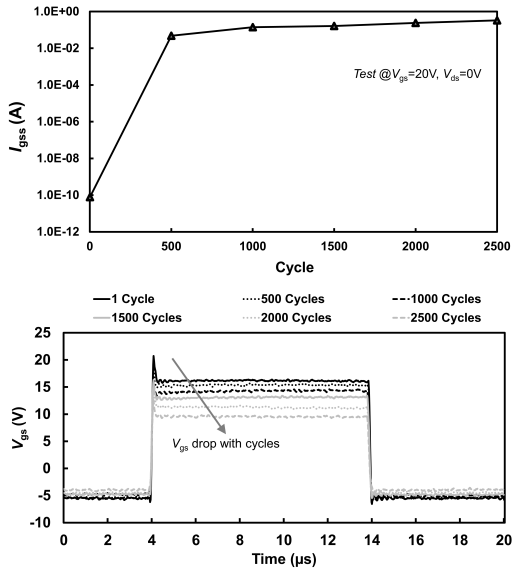

Fig. 6. Degradation of the gate oxide (a) I_{gss}, (b) V_{gs}.

It should be mentioned that the gradual increase in I_{gss} could also happen during the singular short circuit impulse [21], [35], [50], [51]. The underlying mechanism was assumed to be caused by Fowler-Nordheim (FN) tunnelling effect and Schottky emission in [25], but according to the model fitting and experimental measurements, the FN tunnelling effect would overestimate the results under the simulated condition. The generation of I_{gss} comes from the Schottky emission effect, in which carriers could gain enough thermal energy to overcome the SiC/SiO_2 barrier and be injected into the dielectric layer [50]. Besides, I_{gss} increases and the oxide degrades faster with the increase in the applied V_{gs} and V_{ds} as reported in [9], [52], [53].

B. Dynamic Parameters

1) Switching time: According to [54], the dynamic performance of the SiC MOSFET is closely linked to static parameters, such as V_{th}, and so far most studies focus on revealing the degradation of static parameters of SiC MOSFET, and neglect the influence on dynamic behaviour. Since the SiC MOSFET device often works at switching states, it is meaningful to study the influence of repetitive short circuit events on the switching behaviour.

In [55], the charge pumping test was performed on a planar SiC MOSFET with short circuit impulses of 1000 times, and there was a positive shift in the C_g-V_g curve. The results indicated that the JFET region was not degraded, but the channel at the gate-oxide interface was severely degenerated. These were caused by the hot electrons injection and the generation of extra traps, which acted as negative charges and led to the positive drift of V_{th}. To analyze the connection between static performances and dynamic parameters, expressions of the turn-on time (t_{on}) are shown in Eq. 5-Eq. 9 in [54].

$$t_d = R_g C_{iss} \ln\left(\frac{V_{gs}}{V_{gs} - V_{th}}\right) \tag{5}$$

$$t_{ri} = R_g C_{iss} \ln\left(\frac{V_{gs}\mu_n C_{ox} W_{ch}}{V_{gs}\mu_n C_{ox} Z - L_{ch}\sqrt{I_{ds}} - V_{th}\mu_n C_{ox} W_{ch}}\right) \tag{6}$$

$$t_{fv} = \frac{R_g C_{gd}}{\left(V_{gs} - V_{gp}\right)}\left(V_{ds} - I_{ds} R_{on}\right) \tag{7}$$

$$V_{gp} = V_{th} + \sqrt{\frac{J_c W_{ch} L_{ch}}{2\mu_n C_{ox}}} \tag{8}$$

$$t_{on} = t_d + t_{ri} + t_{fv} \tag{9}$$

where t_d is the turn-on delay time, C_{iss} is the input capacitance, t_{ri} is the current rise time, C_{gd} is the gate-drain capacitance, and t_{fv} is the voltage fall time, J_c is the current density, and V_{gp} is the miller plateau voltage. Thus, the increase in V_{th} led to a increase in t_d and t_{ri}, corresponding to $t_{d(on)}$ in [55]. Although there was an increase in V_{gp}, t_{fv} hardly changed, corresponding to t_r. The combined effect of $t_{d(on)}$ and t_r finally led to an increase in t_{on}.

Similarly, the turn-off switching time (t_{off}) can be written as Eq. 10-Eq. 13 in [54]:

$$t_s = R_g C_{iss} \ln\left(\frac{V_{gs}}{V_{gp}}\right) \tag{10}$$

$$t_{rv} = R_g C_{gs} \frac{(V_{ds} - V_{on})}{V_{gp}} \tag{11}$$

$$t_{fi} = R_g C_{iss} \ln\left(\frac{V_{gp}}{V_{th}}\right) \tag{12}$$

$$t_{off} = t_s + t_{rv} + t_{fi} \tag{13}$$

where t_s is the storage time, t_{rv} is the voltage rise time, V_{on} is the voltage drop of the device under conduction mode, and t_{fi} is the current fall time. The increase in V_{gp} led to decrease in t_s, corresponding to the $t_{d(off)}$ in [55]. t_{rv} and t_{fi} also decreased, leading to the reduction in t_f and overall t_{off}.

2) Switching speed: Turn-off/on speed can be reflected by voltage and current switching rates, namely dv/dt and di/dt. The voltage and current switching rates could be written in Eq. 14 and Eq. 15 in [56], [57]. It could be found out that switching rates for a specific device are dependent on V_{gs}, V_{th}, and V_{gp}. Thus, the degradation of static parameters will cause the degradation of dv/dt and di/dt.

$$\frac{dV_{ds}}{dt} = \frac{V_{gs} - V_{gp}}{R_g \cdot C_{gd}(V_{ds})} \tag{14}$$

$$\frac{dI_{ds}}{dt} = \frac{\mu_n W_{ch} C_{ox}\left(V_{gs}\left(1 - e^{\frac{-t}{C_{iss}R_g}}\right) - V_{th}\right)V_{gs}}{L_{ch}C_{iss}R_g e^{\frac{t}{C_{iss}R_g}}} \tag{15}$$

The only reported degradation of dv/dt and di/dt under short circuit event was in [58]. However, the fluctuation was rather large. In order to avoid the random error in data processing, dv/dt and di/dt during turn-off period was differentiated, and the peak absolute value was extracted as the degrading indicator. The refined data for symmetrical and asymmetrical trench SiC MOSFET devices are shown in Fig 7. It could be seen that for both symmetrical and asymmetrical trench devices, |dv/dt| and |di/dt| increase with the decrease in V_{th} at first. When the gate oxides begin to degrade after 100 cycles (obvious increase in I_{gss} in the measurement), both |dv/dt| and |di/dt| are decreased, and the reduced V_{gs} instead of V_{th} becomes the dominate reason.

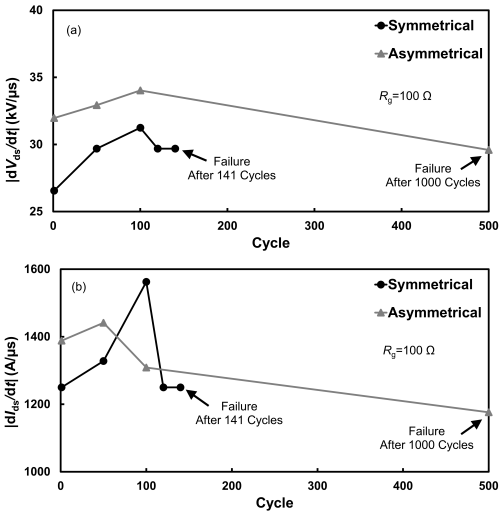

Fig. 7. Turn-off switching rates of symmetrical and asymmetrical trench devices.

Similar to the turn-off transient, the decreased V_{th} is the responsible reason for the degradation of turn-on |dv/dt| and |di/dt|, which is shown in Fig 18. Once the oxide is severely degraded with large I_{gss}, the switching speed will be reduced. In contrast with turn-off |dv/dt| and |di/dt|, turn-on |dv/dt| and |di/dt| are lower and have milder degradation trend.

3) Switching energy: Due to the increase in t_{on} and the decrease of t_{off}, the turn-on switching energy (E_{on}) and the turn-off switching energy (E_{off}) were calculated to be increasing and decreasing as the short circuit experiments

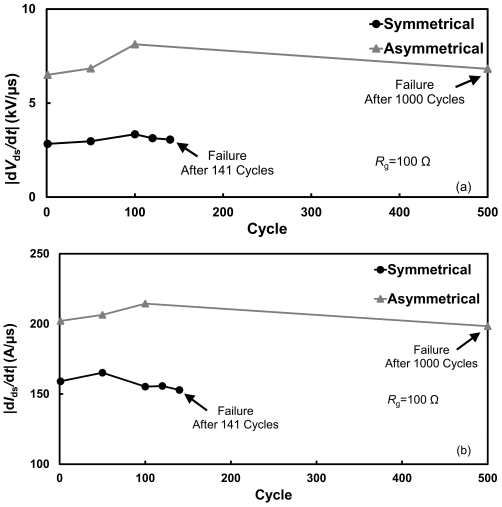

Fig. 8. Turn-on switching rates of symmetrical and asymmetrical trench devices.

proceeded [55]. However, it should be mentioned that E_{on} and E_{off} depend on the combined effect of switching time, oscillation, and dynamic R_{on}. It is hard to tell which parameter has the most significant impact on E_{on} and E_{off} variation. Thus, mathematical models should be built in the future to fully understand the impact of repetitive short circuit events on the degradation of dynamic performances. Also, the effect of different short circuit test conditions on the variation of E_{on} and E_{off} should be investigated.

IV. Effects of Test Conditions on Short Circuit Reliability of SiC MOSFET

A. V_{ds}

In applications such as electric vehicles, V_{ds} may change to adjust the output voltage. Thus, investigating the short circuit performance of the device under different V_{ds} is of significance. In [30], researchers investigated the influence of V_{ds} on the failure mechanism of SiC MOSFET. It has been observed that the large current density caused by the high electric field and high temperature finally led to the thermal runaway failure under high V_{ds} condition (48-63% of the breakdown voltage). For medium V_{ds} (36-47% of the breakdown voltage), the inability to turn off the channel current was the reason for device failure. By applying a lower negative V_{gs}, the failure of the SiC MOSFET device can be avoided. The gate-source resistance was low after the low V_{ds} experiment (24-31% of the breakdown voltage), and gate failure was observed. Similar patterns have been reported and verified by the test results of planar, shield-planar, and trench SiC MOSFETs, which are summarized in Fig. 9 [35]. Based on simulations and post-failure analysis performed under similar conditions in [23], [34], T_j rose to a high value in a very short time under high V_{ds} condition, which was enough to instantly cause the thermal runaway failure. However, lower V_{ds} reduced the rising speed of temperature, thereby providing adequate time for gate oxide rupture and Al infiltration, leading to the gate malfunction.

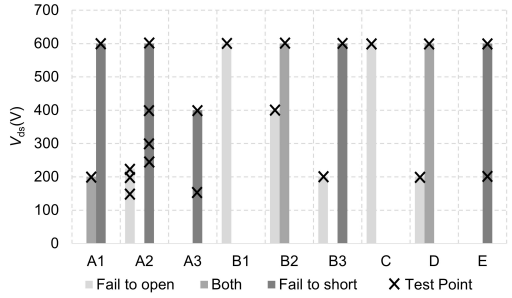

Fig. 9. Statistical results of failure modes under different V_{ds} for different devices (results from [35] - re-adapted for visualisation.)

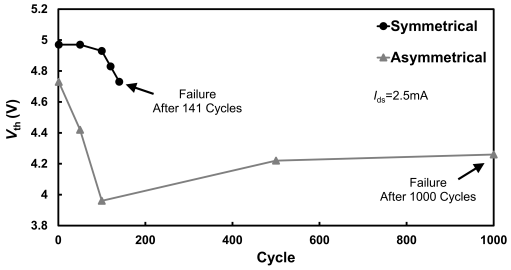

Fig. 10. Negative drift of V_{th} by applying negative V_{gs} during the turn-off intervals between short circuit impulses.

B. V_{gs}

V_{gs} affects R_{on}, thereby influencing I_{peak}, T_j and SCWT [59]. According to results in [21], [60], [61], SCWT increased with the decrease in V_{gs} due to lower I_{peak} and lower T_j. Also, it has been reported in [21], higher positive V_{gs} could induce gate short circuit failure under V_{ds}=600 V test, while low positive V_{gs} caused the thermal runaway failure instead. Similar results was also observed in [12]. However, compared with the effect of V_{gs}, the failure mechanism is more determined by the magnitude of V_{ds} [12], [30]. Furthermore, it has been reported that the value of V_{gs} affects the drift direction of V_{th} [62]. With V_{gs} of 10 V and V_{ds} of 400 V, V_{th} decreased with the progress of repetitive tests. However, with V_{gs} of 20 V and V_{ds} of 400 V, V_{th} increased instead. The interesting finding was explained to be caused by the different electric field directions in the oxide layer under different V_{gs}, which determined the type of injected carriers.

For commercial SiC MOSFET devices, a moderate negative V_{gs} is preferred to safely turn off the device [63], [64], which holds in short circuit events. According to test results in [65], for both planar and trench devices, if turn-off V_{gs} changes from 0 V to -5 V, SCWT can be increased by 0.5 μs and 1 μs, respectively. This phenomenon is because a more negative V_{gs} can suppress the current density and lower the lattice temperature, proven by simulation results in [24], [66]. In [67], researchers discovered that after the device was turned-off in the short circuit event, the residual high temperature combined with negative V_{gs} could provide enough energy for holes to inject and accumulate within the gate oxide, and mitigate the shift of parameters compared with the condition of the applied V_{gs} of 0 V. In [58], similar phenomena was also reported, but different from the positive V_{th} shift in most papers, radical negative drifts for both symmetrical and asymmetrical trench SiC MOSFETs were observed, as shown in Fig 21. The reason behind was because of the negative V_{gs} between short circuit intervals. The residual high temperature right after the short circuit caused energized holes to overcome the barrier and inject into the gate oxide, which not only counteracted but also outweighed the effect of injected electrons. Nevertheless, it should be noted that if negative V_{gs} exceeds the recommended value in the datasheet, the short circuit reliability of the SiC MOSFET will be reduced.

C. R_g

Although R_g affects the switching speed, current and voltage oscillation of the SiC MOSFET device, its variation seems to have a minor impact on short circuit current within a reasonable range, as is shown in Fig. 11. With lower R_g, the current rises faster at first, leading to the increase of T_j correspondingly. After reaching its peak, the mobility of carriers begins to decrease because of the negative temperature coefficient, which increases the R_{on} and lowers the short circuit current. The smaller the R_g, the higher the I_{peak} is and the earlier the current drops. However, the critical short circuit energy (E_{sc}) and SCWT seem irrelevant with R_g, verified by both test and simulation in [60], [68], [69].

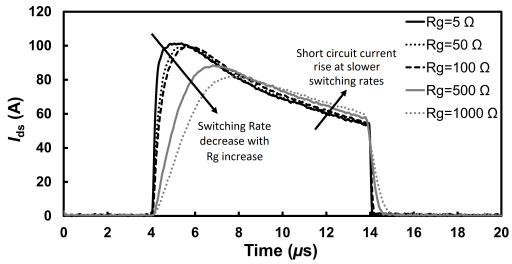

Fig. 11. Effect of R_g on short circuit current.

D. Case Temperature

SiC MOSFET devices often work in conditions where the temperature is higher than the room temperature. Thus, the influence of temperature on device reliability should be considered. According to test results shown in Fig. 12, higher ambient temperature increases the current rising speed but lowers the short circuit current after reaching I_{peak} for planar, symmetrical and asymmetrical trench SiC MOSFETs, which is related to the negative temperature coefficient of V_{th} and positive temperature coefficient of R_{on}.

The contribution of temperature on device robustness seemed dependent on the device manufacturer [21], [31]. SCWT was less relevant to temperature for devices from Wolfspeed, but it decreased significantly with the temperature increase for Rohm devices under same test conditions. E_{sc} decreased with the increase in temperature for both devices. In [70], the effect of temperature on repetitive short circuit reliability was investigated and an interesting trend was

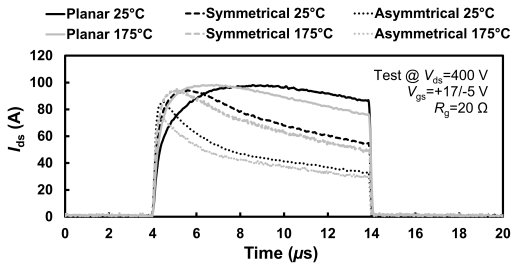

Fig. 12. Effect of temperature on short circuit current.

discovered: the repetition cycle was higher for devices with higher case temperature. The difference phenomena between destructive and degraded tests under given test condition was caused by t_{sc}. In destructive short circuit tests, t_{sc} lasted until the devices fail, which was relatively longer than the time in repetitive tests. With the increase in case temperature, the gap between the initial temperature and the critical failure temperature shown in Fig. 5 was decreased and less energy/heat was needed for thermal runaway failure or gate failure. Hence, SCWT is reduced for some devices. For repetitive experiments with shorter t_{sc} of 2.2 μs, T_j was not high enough to cause any immediate failure. According to the thermal model in [70], devices with lower initial temperature had higher temperature swing, leading to higher mechanical stress between Al and SiO_2 caused by coefficient of thermal expansion (CTE) mismatch. Thus, it took less cycles for the gate oxide to be ruptured.

V. Modeling and Characterization of SiC MOSFET during Short Circuit

To reproduce the internal behavior of SiC MOSFET during the short circuit event, different characterization methods have been developed, which are suitable for investigating the device performance from different aspects.

A. TCAD Model

TCAD is a useful tool to reveal the internal behaviour of the SiC MOSFET cell during the short circuit process. In [71], an electrical-thermal model of a planar SiC MOSFET was built and verified. The distribution of the drain current and temperature in the single pulse test was revealed. The channel region was observed to have the highest impact ionization rate and the electric field. By manually setting the carriers near the gate oxide, the degradation of the device in repetitive tests can be simulated. Based on energy-dispersive X-ray spectroscopy images, simulation models for planar and trench SiC MOSFET devices considering the coupling of the electrical, thermal, and mechanical field were developed to investigate the gate failure mechanism in [23]. For planar devices, the electric field inside the gate oxide was lower than the breakdown electric field of SiO_2, indicating the gate failure of the device was not caused by insulation breakdown. The temperature profile showed that the temperature on the source surface exceeded the melting point of Al, and could lead to the deformation of electrodes. The distribution of the maximum mechanical stress was consistent with the region of crack in practice. As for trench devices, the simulated electric field was also proven not to be the root cause of device failure. Similarly, the surface temperature at the source would result in the melt of the electrode metal. The tensile stress near the trench wall could induce the formation and stretch of the crack, leading to the gate short circuit eventually. In [22], the TCAD model was improved to be a three-dimensional one. Both thermal runaway failure and gate destruction failure can be reproduced by setting different conditions. According to simulated results, the high current density near the gate channel resulted in the NPN transistor latch-up in high voltage conditions, while the concentrated mechanical stress in the gate interlayer caused the gate failure in low voltage conditions. Although using TCAD models can achieve comprehensive results, the method requires detailed device information, such as dimension, doping concentration, material properties, and physical models, etc. Besides, it takes lots of time and computing resources to calculate a TCAD model. The higher accuracy, the more computationally demanding it is.

B. Behavioral Model

The behavioural model is a feasible way to simplify the model. Considering the equations of power semiconductors, a behavioural model was built in [31]. The results roughly demonstrated the changing trend of temperature and current in the short circuit duration, but its accuracy should be improved further. Taking the thermally generated current, parasitic NPN transistor, and the effect of mobility degradation into account, a mathematical model was proposed to simulate the electrical behaviour of SiC MOSFET device in [72]. The model can precisely predict the performance of the device under high current and high voltage conditions, which was in good agreement with waveforms in SPICE software. Combined with the Cauer thermal network, T_j can be estimated. Based on tested short circuit waveforms and heat dissipation equations, a behavioural model was proposed to estimate T_j in [73]. To ensure high accuracy estimation, the temperature dependency of thermal conductivity and specific heat capacity of chip materials was considered. The uneven distribution of current in the JFET region and the latent heat of Al melting were taken into account as well. Similar to TCAD models, the device degradation can be simulated by considering the effect of interface trap accumulation. In [74], the impact of carrier scattering on channel mobility and the contribution of gate bias and temperature were considered, where the Coulombic scattering was set to be related to the interface state. Simulation results were proved to be in good agreement with the experiments under various conditions.

C. Thermal Network Model

Thermal network models predict the thermal behaviours of power devices. By calculating the power loss under specific working conditions and taking the device packaging into account, the temperature distribution of each layer can be accurately predicted [75]. Compared

with complex TCAD models, thermal network models have advantages of time-saving and higher computation efficiency. However, most studies have focused on the module or system-level temperature estimation under normal operating conditions [76], [77], and few studies have paid attention to the temperature change and distribution inside the chip using the thermal network model. In [78], a 5-layer Cauer thermal network model was built according to parameters provided by the datasheet. Although the effect of temperature on material parameters were considered, the temperature was still underestimated since the chip was taken as a whole. In order to avoid such errors, the chip was treated as an uneven heat source and a chip-level thermal network model was proposed in [79]. Based on heat distribution results in the TCAD model, the chip was divided into 9 RC units. The temperature dependency of thermal resistance and thermal capacitance of chip material was considered. In contrast with TCAD results, the chip-level thermal network can not only assure similar accuracy but also reduce the computational time to a great extent. In [80], a similar chip-level thermal network model was proposed independent of the TCAD model. Based on the chip structure and dimension, the power dissipation was calculated in PLECS through current, mobility, and V_{th} equations. Taking into the temperature dependency of electrical and thermal parameters into account, the effect of V_{gs} and V_{ds} on lattice temperature was revealed. Although basic information of the chip was still needed, this method greatly reduces the computational complexity, and can obtain reliable results quickly.

D. Advanced Measurement

Except for simulation models, some researchers have applied advanced test methods to observe the performance of SiC MOSFETs during the short circuit transient in real-time. In [81], a dynamic platform was built to evaluate the thermal behaviour and to extract electrical parameters of the device during the short circuit event. By importing test data into MATLAB, T_{j} was calculated based on heat diffusion equations. By applying different t_{sc} and processing data at the end of the short circuit event instantly, device parameters such as V_{th}, average channel mobility could be obtained at different temperatures. The accuracy of the results was verified by comparing the chip surface roughness with the estimated temperature that may potentially induce the melt of Al. In [82], a novel method was proposed to observe the failure process of the SiC MOSFET chip during the short circuit transient. A SiC MOSFET device was specially made without packaging, and a high-speed camera was used to record the fast dynamic process. The starting point of Al melting, the complete liquid phase of Al, the change of electrode roughness, and the re-solidification of Al can be seen from the reflection of dark and bright regions, which were intuitive.

VI. Outlook

Although the failure and degradation mechanisms and characterization methods have been summarized, there are still some points worth studying in order to improve the reliability of the SiC MOSFET device, evaluate and monitor the health status of the device under application conditions.

A. Reliability Comparison of SiC MOSFETs from Different Manufactures and with Different Structures

The reliability of SiC MOSFET devices is of importance to the safe operation of the power system. It would be helpful for engineers to select devices if there is sufficient information about the reliability of the device. Therefore, it is necessary to compare the robustness and reliability of SiC devices from different companies or with different structures.

The comparison of the short circuit robustness of SiC MOSFETs was made in [45]. It was reported that SiC MOSFETs with similar current ratings from different manufacturers had notable differences in the short circuit test at V_{ds} of 600 V: SCWT was 13 μs and 5 μs, and E_{sc} density was 2.4 J/cm^2 and 0.9 J/cm^2 for two tested devices, respectively. In [31], the short circuit performance of commercial SiC MOSFETs from Wolfspeed and Rohm was tested under various electrical-thermal conditions. Results showed that the 2$^{\mathrm{nd}}$ generation SiC MOSFETs from Wolfspeed withstood the lowest E_{sc} and had the lowest SCWT under different case temperatures and dc-link voltages, while the devices from Rohm had the highest reliability. Besides, the reliability of Wolfspeed products seemed to be less sensitive to different temperatures. In recent years, researchers have done experiments on SiC MOSFETs from Wolfspeed, Rohm and STMicroelectronics with different device technology [52]. Key indicators such as SCWT, current density and E_{sc} have been comprehensively compared to reveal the reliability among 5 devices. In this paper, the robustness of 7 commercial SiC MOSFETs from different vendors was compared at different temperatures to reflect the short circuit robustness with the latest chip technology. All devices have the same voltage rating and similar current rating. Details of 7 devices are listed in Table I. The devices were tested at V_{ds} of 600 V, V_{gs} of +17/-5 V. SCWT and E_{sc} were compared at 25°C and 175°C, shown in Fig. 13 and Fig. 14. It can be discovered that at room temperature, Device B shows the lowest reliability, whose SCWT is only 5 μs. Device A, F and G have similar reliability, and their SCWT is 9 μs. Device C, and D also exhibit high robustness, and they can withstand the short circuit impulse up to 11-12 μs. The highest reliability among all devices belongs to Device E, which did not even fail after 19 μs. The robustness at higher temperature is slightly different. Device B still has the lowest robustness, and its SCWT seems irrelevant with temperature. SCWT for Device A, F and G show slight dependency on temperature, and is 8, 7 and 8 μs, respectively, decreasing by 1-2 μs. For rest devices, their reliability also exhibit temperature dependency more or less, but Device C and E can still withstand the short circuit stress over 10 μs. E_{sc} comparison of these devices can be found in Fig. 14. The devices with higher SCWT also have higher E_{sc}, and E_{sc} at 175°C is always lower than the energy at 175°C, which is because of the lowered SCWT and lowered short circuit current at high temperature.

To further quantify the device reliability, SCWT and E_{sc} density were calculated based on chip area and plotted in

TABLE I
KEY PARAMETERS OF SIC MOSFETS

Vendor	Voltage Rating (V)	Current Rating (A)	R_{on} (mΩ)	C_{iss} (pF)	Chip Area (mm^2)
A	1200	18	160	606	5.79
B	1200	19	160	724	3.21
C	1200	22	160	870	5.50
D	1200	20	189	650	6.44
E	1200	22	160	1200	24.52
F	1200	17	160	398	5.76
G	1200	19	140	454	3.61

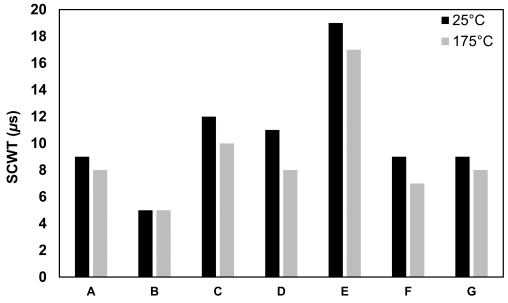

Fig. 13. SCWT comparison of devices from different manufacturers.

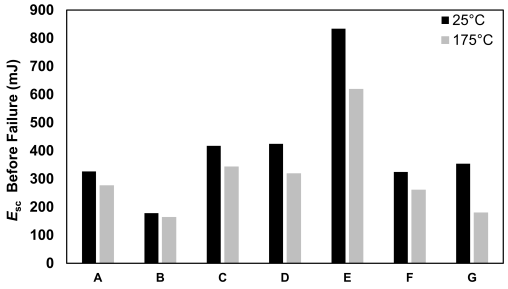

Fig. 14. E_{sc} comparison of devices from different manufacturers.

Fig. 15 and Fig. 16. From Fig. 15, it can be seen that Device C and G have high SCWT density at both temperatures. The SCWT density of Device D and F show high dependence on temperature, while Device A and B exhibit little dependence. Although Device E has the highest SCWT in the test, its SCWT density is the lowest. The good short circuit performance is at the expense of large chip area, which will lead to slow dynamic performance. Even though Device C and G still have high SCWT density, they also have relatively high E_{sc} density compared with other devices, as can be seen from Fig. 16. E_{sc} density is very stable for Device A and B at both 25°C and 175°C. Not surprisingly, Device E has the lowest energy density, which totally gives credit to its large area. It can be concluded that Device C and G have achieved the best balance among short circuit performance, temperature stability, and chip area.

The robustness of SiC MOSFET with different structures was also investigated in Table II. There is no conclusion as

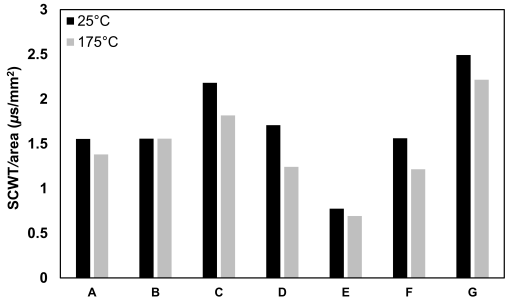

Fig. 15. Comparison of normalized SCWT of devices from different manufacturers.

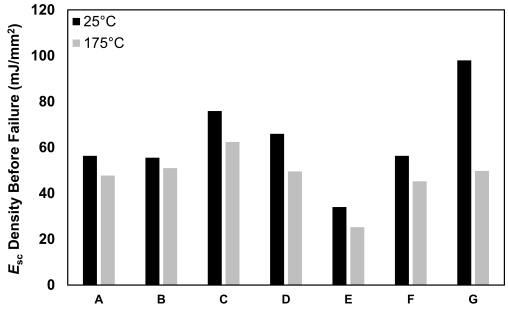

Fig. 16. E_{sc} density comparison of devices from different manufacturers.

to which structure is more reliable because the short circuit performance of devices with different structures was dependent on multiple factors such as the thickness and quality of the oxide, chip size, doping concentration, manufacturer, etc, excluding from chip structure. In [83], [84], the trench SiC MOSFETs exhibited shorter SCWT compared with the planar SiC MOSFETs with similar power ratings. The reason behind this was attributed to the bigger chip area of the planar device, which reduced the current density and heat density. However, similar SCWT was found in a 1200 V planar SiC MOSFET and a 650 V rated symmetrical trench device at various V_{ds} in [30], and a 650 V-rated symmetrical trench device was found more reliable than a 900 V planar device in [14]. The reliability of planar and asymmetrical trench SiC MOSFETs, symmetrical and asymmetrical trench SiC MOSFETs was studied in [23], [32] with matching SCWT under different V_{ds}. However, the failure mechanisms are regardless of the chip structure and is more related to the test conditions: thermal runaway failure is prone to happen under high V_{ds} while gate failure tends to happen under low V_{ds} for planar, symmetrical and asymmetrical trench SiC MOSFETs [22]–[24], [30].

The comparison of short circuit reliability under repetitive stress is also important, but most studies have focused on the planar SiC MOSFETs [40], [53], [55], [62], [67], [71], [85]. Test conditions such as t_{sc} [40], the magnitude of positive V_{gs} [62], and the off-state negative V_{gs} after the short circuit event [67] were found to have impacts on the device degradation and the drift of V_{th}. In [62], it was found that the degradation of V_{th} of planar SiC MOSFET was more obvious than symmetrical trench SiC MOSFET because the

TABLE II
AN OVERVIEW OF RELIABILITY COMPARISON OF SiC MOSFETs UNDER SINGULAR SHORT CIRCUIT EXPERIMENT

Source	Device Type	Experiment Condition	Test Results/Reliability	Failure Mechanism/Conclusion
[21]	1200 V Planar SiC MOSFETs	V_{gs}=15-19/-5 V, V_{ds}=400-800 V, T=25-150°C	SCWT and failure mode depend on test conditions	(1) V_{gs} was a key factor to cause gate dielectric breakdown. (2) High DC bus voltage was responsible for thermal runaway failure. (3) Case temperature had a minor impact on the ruggedness of selected devices.
[30]	1200 V Planar, 650 V Symmetrical trench SiC MOSFETs	V_{gs}=18/-5 V for Planar SiC MOSFET, V_{gs}=15/-4 V for Symmetrical trench SiC MOSFET, V_{ds}=400/600/800 V, T=25°C	Planar: SCWT=19.5/9/5.8 μs at V_{ds}=400/600/800 V Symmetrical trench: SCWT=20.4/8.6/5.7 μs at V_{ds}=400/600/800 V	For both devices: (1) High DC bus voltage was likely to cause thermal runaway failure. (2) Medium DC bus voltage was likely to re-open the MOS channel after turn-off. (3) Low DC bus voltage would result in gate oxide failure. (4) No significant difference in failure mechanisms between two types of devices.
[22]	1200 V Symmetrical trench SiC MOSFETs	V_{gs}=15/-4 V, V_{ds}=400/800 V, T=25°C	V_{ds}=400 V, SCWT=20.4 μs V_{ds}=800 V, SCWT=5.7 μs	(1) At 400 V, the devices failed because of the conductive path between poly gate and source aluminium. (2) At 800 V, thermal runaway happened due to high current density near the gate and the activation of parasitic BJT.
[23]	1200 V Planar, Asymmetrical trench SiC MOSFETs	V_{gs}=18/-5 V for Planar SiC MOSFET, V_{gs}=15/-5 V for Asymmetrical trench SiC MOSFET, V_{ds}=400/800 V, T=25°C	Planar: SCWT=16/5 μs at V_{ds}=400/800 V Asymmetrical trench: SCWT=15/5 μs at V_{ds}=400/800 V	For both devices: (1) At 400 V, the high von Mises stress in the gate oxide led to the fracture. (2) At 800 V, the high temperature caused the activation of parasitic BJT.
[24]	1200 V Symmetrical trench SiC MOSFETs	V_{gs}=15/-4 V, V_{ds}=400/800 V, T=25°C	Device 1: SCWT=15/10 μs at V_{ds}=400/800 V Device 2: SCWT=32/4 μs at V_{ds}=400/800 V	For both devices: (1) At 400 V, the devices failed due to SiO_2 rapture. (2) At 800 V, the devices failed due to thermal runaway.
[32]	1200 V Symmetrical, Asymmetrical trench SiC MOSFETs	V_{gs}=18/-5 V for Symmetrical trench device, V_{gs}=15/-5 V for Asymmetrical trench device, V_{ds}=400/600/800 V T=25°C	Symmetrical trench: SCWT=15/8/5.2 μs at V_{ds}=400/600/800 V Asymmetrical trench: SCWT=15/8.5/5.8 μs at V_{ds}=400/600/800 V	(1) Thermal runaway failure for all Symmetrical trench SiC MOSFETs. Gate failure for Asymmetrical trench SiC MOSFETs at V_{ds}=400/600 V. Thermal runaway failure at V_{ds}=800 V. (2) No obvious disparity of short circuit reliability between two types of devices.
[35]	9 different 1200 V Planar, Symmetrical trench SiC MOSFETs	V_{gs} is within safe operating range for all SiC MOSFETs, V_{ds}=150-600 V, T=25°C	Gate fail-to-open, thermal runaway failure, and drain-source short circuit were observed at different test conditions for various devices.	Each device had its own behaviour during the test under the same test condition, depending on chip size, doping, chip topology, etc.
[41], [84]	650 V Planar, Symmetrical trench SiC MOSFETs	V_{gs}=15,18,20/-3.8 V, V_{ds}=200-350 V, T=25°C	SCWT and failure mode depend on test conditions.	Planar SiC MOSFET was more robust than trench SiC MOSFET because of higher current and heat density of trench structure.
[14]	Planar, Symmetrical trench SiC MOSFETs	V_{gs}=15/0 V, V_{ds}=300 V, T=25°C	900 V Planar: SCWT=14 μs 650 V Symmetrical trench: SCWT=19 μs	Thermal runaway for Planar MOSFET. Gate oxide breakdown for trench MOSFET due to large current and impact ionization rate were generated at the gate trench corner.

degradation happened in the channel region for the planar device, while the degradation happened at the trench corner for the trench device. In [86], the reliability of planar and trench devices was compared. Results showed that the long-term reliability of planar devices was five times higher in contrast with trench devices.

The repetitive short circuit reliability of planar, symmetrical, and asymmetrical trench SiC MOSFETs was also compared at different temperatures by authors [87]. The same test conditions (V_{ds}=400 V, V_{gs}=+17/-5 V, t_{sc}=10 μs) were applied on three types of devices with similar power rating. The increase in I_{gss} shown Fig. 17 clearly showed the reliability difference among three structures. At both 25°C and 175°C temperatures, I_{gss} of planar devices had almost no degradation after 5000 cycles. After tens of cycles, symmetrical trench devices showed large increase in I_{gss} at both temperatures, indicating the oxide had suffered from irreversible damage. For asymmetrical trench SiC MOSFETs, the large I_{gss} ramp occurred after 500 cycles at room temperature. The gate and source electrodes were short-circuited after 500 cycles as well at elevated temperature. I_{gss} could not be measured anymore.

Taking the case at 25°C for example, the current density distribution at the peak points and temperature distribution at the end of the short circuit impulse of three devices in TCAD simulation were revealed in Fig. 18. The effectiveness of the model has been validated in [87]. From Fig. 18(a), it can be discovered that planar and symmetrical trench SiC MOSFETs have symmetrical current distribution, while the current flows in the left side for asymmetrical trench SiC MOSFET due to its special structure to protect the gate oxide and reduce chip area. For all three types of devices under test, the channel region has the highest current density. Compared with trench SiC MOSFETs, the current density in the channel is smaller for planar SiC MOSFET which is due to its larger chip area. In Fig. 18(b), the highest temperature locates under the gate region for three types of SiC MOSFETs. The asymmetrical trench device has the highest temperature, while the planar device has the lowest temperature.

Overall, short circuit robustness and reliability for the commercial SiC MOSFET devices should keep up with the device technology. Systematic comparisons and summaries would provide valuable reference for device selection and technology improvement.

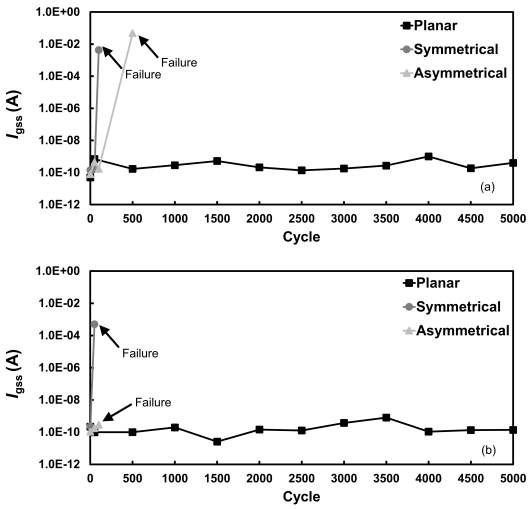

Fig. 17. Reliability comparison of planar, symmetrical, asymmetrical trench SiC MOSFET devices under repetitive short circuit tests. (a) 25°C, (b) 175°C.

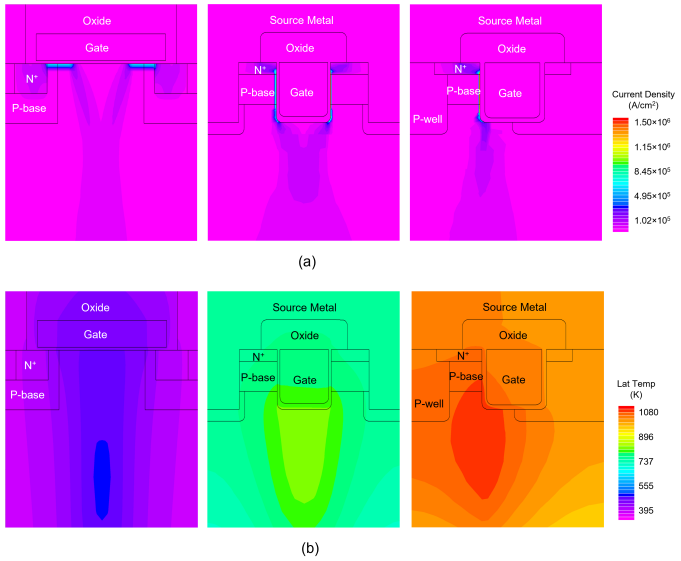

Fig. 18. Internal performance of planar, symmetrical, and asymmetrical SiC MOSFETs during short circuit event [87]. (a) current density distribution at the peak point, (b) temperature distribution at the end of the test.

B. Short Circuit Reliability of Parallel SiC MOSFETs and Multi-chip SiC Module

Since discrete SiC MOSFET device is unable to carry high current, parallel SiC MOSFET devices and SiC power modules are more commonly used in practice. Ideally, each parallel chip is supposed to share same current in the parallel configuration. However, the uneven distribution of intrinsic parameters such as V_{th} and R_{on}, and external parameters such as parasitic inductance, R_g, and T_j among chips will lead to the uneven distribution of current and energy during the short circuit impulse, which will further affect the T_j of the chips. Since the transient energy is large and the temperature can easily reach a high value, the failure of the chip may directly happen if the worst condition is considered. If the chips suffer from multiple short circuit events, then they will mutually affect until failure and each chip may have different degrees of degradation. Both conditions will greatly lower the reliability of the power electronic systems. Besides, it has been reported in [78] that due to the reduced resistance and inductance in the parallel configuration, the total short circuit current of parallel chips is larger than that of the single chip. Thus, the reliability and current distribution among parallel SiC MOSFET chips needs to be discussed.

In [88], the short circuit performance of SiC MOSFETs with different V_{th} were compared. It has been found out that the device with lower V_{th} had higher I_{peak}. Except for the spread in V_{th}, the effects of case temperature and R_g difference were also discussed in [78], [89]. Test results under

different case temperatures and R_g are shown in Fig 19 and Fig 20. The results show that the device with high initial temperature rises faster. After reaching its peak, the current begins to fall, and the higher case temperature difference between parallel devices, the greater difference in the current dropping phase. As for the influence of R_g mismatch, the difference in current distribution is not significant. The device with lower R_g operates faster and has higher I_{peak} at first. The device with higher R_g has slightly lower R_{on} and higher current in the current dropping phase. This is because the fast rising current also increases T_j, which reduces the mobility of carriers and increase the R_{on} after reaching I_{peak}.

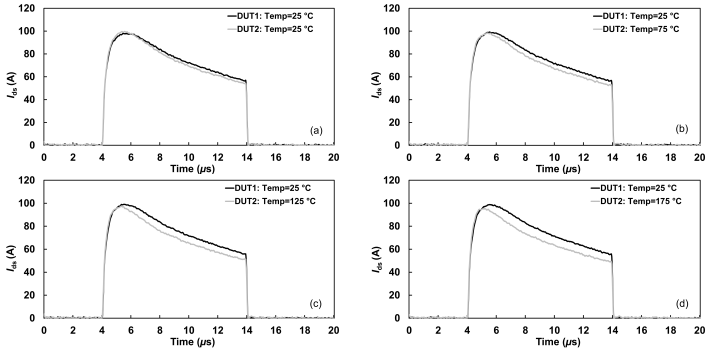

Fig. 19. Influence of temperature on short circuit current between parallel devices. (a) 25°C and 25°C, (b) 25°C and 75°C, (c) 25°C and 125°C, (d) 25°C and 175°C.

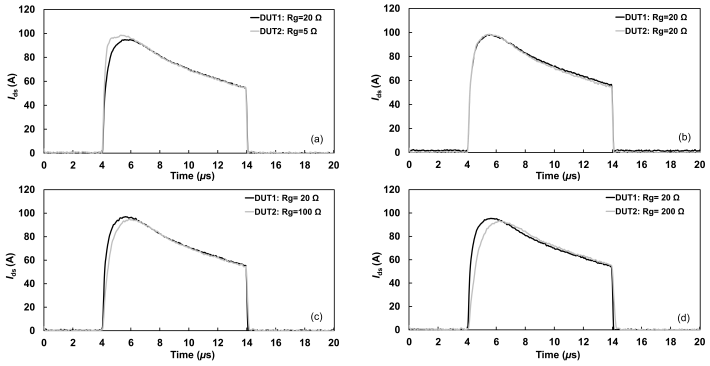

Fig. 20. Influence of R_g on short circuit current between parallel devices. (a) 20 Ω and 5 Ω, (b) 20 Ω and 20 Ω, (c) 20 Ω and 100 Ω, (d) 20 Ω and 200 Ω.

With regard to power modules, a 1.2 kV/300 A SiC power module from Wolfspeed and a 1.2 kV/180 A SiC power module from Rohm were tested and compared in [90] under same conditions. The 1.2 kV/300 A module can only withstand 1.9 μs while the 1.2 kV/180 A module can withstand 7.2 μs short circuit impulse under V_{ds} of 800 V at 25°C. On one hand, the notable difference in SCWT may be caused by the difference in device technology. On the other hand, it is reasonable to infer that the most fragile chip directly determined the short circuit reliability of the whole module and there were huge spreads of parameters in the Wolfspeed module that lowered the overall reliability. To ensure the consistency of the chip performance and improve the reliability of the module, SiC MOSFET chips should be carefully selected. A screening strategy to balance the offset of static parameters to avoid difference in short circuit performance was proposed in [91]. The deviation in short circuit current and short circuit energy can be significantly decreased by appropriately screening the transfer characteristics.

Furthermore, due to higher saturation carrier drift rate and smaller internal capacitance, SiC MOSFET devices switch faster and are easily affected by parasitic inductance. Thus, the difference in switching speed between parallel devices affects the short circuit reliability to a great extent. The imbalance ratio of main circuit stray inductance on short circuit performance SiC MOSFET device was briefly discussed in [92]. Although researchers drew the conclusion that under the ratio of 1.5, parallel devices exhibited minor difference, it should be noted that compared with the ratio of 1, the short circuit energy between devices was completely different. The impact of different inductance mismatch on short circuit behaviour was more thoroughly clarified in [93]. Results indicated that the inductance mismatch in the gate-source path and the quasi-source path contributed to the current and energy imbalance most because of the feedback of V_{gs}. The difference in drain inductance, gate inductance, and auxiliary inductance had minor effects on the short circuit performance. The difference between the gate-source inductance and the quasi-source inductance may promote each other's effect and further exacerbate the short circuit performance.

Although researchers have figured out the influence of parameter mismatch on the short circuit performance of parallel devices, repetitive short circuit tests should be carried out to see how parallel devices and power modules degrade in the long run. It is important to know the degradation relationship and reliability among parallel chips. Except for the consistency of chip parameters, special attention needs to be paid to the conformity of packaging parameters. Advanced mathematical models could be built to better guide the design of the packaging of multi-chip modules.

C. Chip Optimization

To improve the short circuit reliability of SiC MOSFET devices, many research work has been trying to optimize the device structure. Methodologies to improve the ruggedness of SiC MOSFET devices can be divided into the following three types: (1) by selecting different gate dielectric materials [21], [34], (2) by redesigning the thickness of the gate oxide and changing V_{gs} correspondingly to reduce the saturation current of the device [66], [94], [95], (3) by restructuring the chip topology (changing doping profiles, adopting different structures, etc) [96]–[101].

(1) Selection of gate material: Based on the failure mechanisms discussed above, the rupture of the gate oxide and the melting Al induced by the high thermal-mechanical stress are responsible for the gate destruction for all types of SiC MOSFET devices. Thus, the researchers proposed to alleviate the thermal-mechanical stress by reasonably designing the thickness of the gate structure [34] or mitigating the CTE mismatch among the poly-silicon, gate interlayer dielectric, and source metal layer [21]. Nevertheless, since the work function difference between metal and semiconductor, the

thickness of gate dielectric, and the doping in the chip topology have a significant impact on the electrical behaviour of the device [54], the selection of the materials in the gate structure is crucial and needs to be further investigated. The feasibility of the manufacturing process should be concerned.

(2) Redesign of the gate structure: Some researchers also proposed to improve the robustness of the SiC MOSFET device by thickening the gate oxide. Even though the peak short circuit current was reduced and SCWT was increased in [66], the increase in R_{on} is disadvantageous to the efficiency of the power system. In [94], a constant gate charge scaling method was presented to reduce the current of SiC MOSFET only in the saturation region. By reducing the thickness of gate oxide and the applied V_{gs} simultaneously, the short circuit current can be suppressed in the simulation, while the R_{on} in the linear region was unchanged. Although the method was alleged to be suitable for different chip structures, the method would greatly diminish the linear region of SiC MOSFET and reduce the operational V_{ds} window.

Another way to reduce the saturation current was put forward in [95]. The thickness of the gate oxide was decreased together with the reduction in channel mobility to ensure acceptable V_{th} for a planar SiC MOSFET. To avoid gate oxide breakdown, the allowable applied positive V_{gs} range was shrunk. This approach was validated to improve the short circuit robustness significantly, but it should be noted that the gate driver should be carefully designed when the gate oxide is thinned because the reduced V_{gs} operating window will be susceptible to problems such as crosstalk, and gate voltage overshoot/oscillation. The long-term gate reliability should also be further investigated in the future.

(3) Chip structure modification: In [96], ways to reduce the saturation current were discussed. By increasing V_{th}, decreasing V_{gs}, and the channel width to channel length ratio, the saturation current can be lowered. The reduction in source doping, channel width, gate bias, and the increase in channel doping were simulated to be effective to increase the SCWT in varying degrees, but these methods would also lead to the increase of R_{on}. Among all the methods, the reduction in source doping was found to achieve the best trade-off.

In [97], the structure of the planar SiC MOSFET was optimized with a deeper P-well region by utilizing channeling implantation. The extended P region was able to generate a larger depletion region at low V_{gs} and in the short circuit condition, which would increase the R_{on} and lower the current in the JFET region, thereby improving the short circuit robustness. However, at high V_{gs} of 20 V, the effective width of JFET region was sufficient to conduct high current, which is advantageous to reduce R_{on} in the forward conduction mode. The improved design reduced I_{peak} and prolonged the SCWT by 2.7 times and 4 times, respectively, in V_{ds}=800 V and V_{gs}=20 V short circuit test. Although the output characteristics and blocking capability of the new structure were proved to be less affected, the dynamic performance needs further testing. A structure to achieve better temperature performance of channel resistance in the planar SiC MOSFET was presented in [98]. By dividing the N^+ region into two separate regions and inserting a low-doped region as shown in Fig. 21(a), SCWT can be slightly increased. R_{on} performed more stable with the change of temperature, and the dynamic characteristics were verified as well.

In [99], a trench SiC MOSFET device with deep P^+ shielded regions and current spreading layers was proposed as shown in Fig. 21(b). Current spreading layers (CSL) were adopted to provide a better pinch-off effect and reduced saturation current, and P^+ shielded regions can lower the electrical stress of the gate oxide. The optimized structure was proved to have lower R_{on} in the linear region and lower T_j compared with a gate bottom P^+ shielded trench structure and a double trench SiC MOSFET. The short circuit robustness of a structure with similar principles was investigated in [100]. The structure was shown in Fig. 21(c), optimized with additional P^+ regions in the N^+ regions and N-base regions next to the gate oxide in the P-base regions. In [101], the robustness of a lateral SiC MOSFET was improved by arranging a heavily doped N region and a lightly doped P region next to the gate channel to lower the saturation current. The method achieved a 24% decrease in saturation current and a doubled SCWT.

Overall, the mainstream chip optimization methods to improve the short circuit robustness focus on increasing the strength of the gate dielectric or reducing the saturation current by adjusting the chip structure. Most studies have provided only simulation results. The feasibility to make actual chips based on these methods, the cost, and the actual performance of the chips should be investigated further.

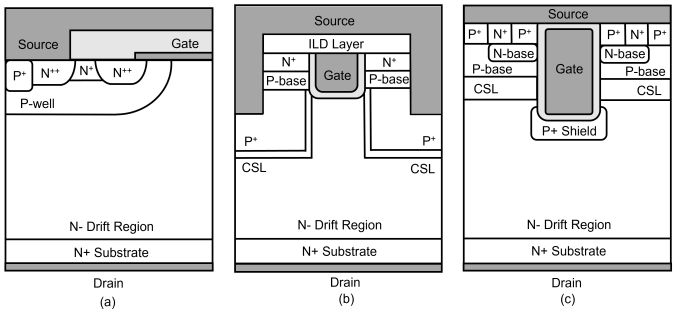

Fig. 21. Novel chip structures to improve the short circuit robustness of SiC MOSFETs reported in [98]–[100].

D. Protection Design of Gate Driver

In contrast with the Si IGBT devices, SCWT for SiC MOSFET devices is much shorter, which proposes a new challenge to the short circuit protection. Based on results in [102], to assure the long time reliability of SiC MOSFET, the short circuit fault was supposed to be identified and removed within 3 μs. Thus, a reliable gate driver is required to detect the short circuit fault sensitively, act rapidly and accurately, and can adapt to different working conditions. Researchers have developed short circuit protection circuits by detecting V_{gs}, desaturation voltage, source parasitic inductance induced voltage spike or the current rising rate [103]–[106]. However, these methods have their advantages and disadvantages. For instance, by detecting V_{gs} and current changing rate, the protection circuit

can achieve good transient performance, but the detection and control circuits are complex. The desaturation method can avoid this shortcoming, but the accuracy is easily affected by temperature and other noises in the circuit, so are the parasitic inductance detection method. Recently, smaller short circuit protection circuits using digital parts such as 350 nm Bipolar-CMOS-DMOS have been developed to better meet the special needs of short circuit protection for SiC devices, which will not cause a significant increase in the weight and volume of the whole system [107].

Furthermore, auxiliary circuits have been studied. In [108], [109], the researchers proposed to add another depleted-mode Si MOSFET in series with the source electrode of SiC MOSFET to improve the performance of the gate driver. The circuit was called BaSIC(DMM), and its principle was to induce the Si MOSFET to work within the saturated region during the short circuit event, thereby reducing effective V_{gs} and short circuit current. I_{peak} can be reduced by 46% and SCWT can be increased by 65% for a C2M0280120D SiC MOSFET with one series Si MOSFET in a single short circuit event. Short circuit cycles can be enhanced by 15 times in the repetitive test. However, there was still a 17% and 20% increase in R_{on} and switching energy of the device, generating extra loss and heat. In [110], researchers optimized the circuit and investigated the influence of different Si MOSFET products on short circuit current at various temperatures and V_{gs}. SCWT for a C2M0160120 SiC MOSFET was able to extend from 7.9 μs to over 10 μs in the short circuit event with V_{ds} of 800 V and V_{gs} of 20 V at room temperature, meeting the standard in industry [111], and there was only a 3.6% increase in R_{on}. In [112], the circuit was verified to ensure good dynamic performance, and had the potential to be commercial. However, the availability, performance and cost of the method should be more comprehensively evaluated for multi-chip SiC power modules. Moreover, the effect of chip aging on the protection accuracy and sensitivity should also be studied in the future.

E. SOA and Reliability Assessment of SiC MOSFET Under Practical Conditions

In practice, it is important to adjust the electrical stress to ensure the device work in the SOA. Based on two failure modes of SiC MOSFET, the criterion to identify thermal runaway failure and gate destruction was proposed in [90]. The fundamental idea was that if either kind of failure happened, then the specific current, voltage, and SCWT were chosen to be the short circuit SOA to that corresponding failure mode. Otherwise, the stress would be increased until reaching the limit. I_{ds} was used to determine the thermal runaway failure boundary and I_{gss} was used to define the gate failure boundary. Although the effectiveness of the method was proven under different V_{ds}, the influence of factors such as temperature and device degradation on short circuit SOA was not considered. According to [113], short circuit SOA was decreased after short circuit tests. Thus, the conception of "repetitive critical energy" was proposed to describe the short circuit SOA in [48], below which the device can suffer from short circuit impluses multiple times and excessive temperature inside the chip can be avoided. Otherwise, the device would degrade rather quickly under a rather high temperature.

On the other hand, the performance and the reliability of the device is strongly influenced by working conditions [114]. Thus, the reliability evaluation on SiC MOSFET will be more valuable if the impact of actual operating states is taken into account. In [78], the impact of Bias Temperature Instability (BTI) on short circuit performance for planar and trench SiC MOSFET was firstly reported. According to test results, the increasing stress time will continuously lower the short circuit current for both planar and trench SiC MOSFETs. Furthermore, the effect of positive and negative BTI tests on short circuit current is clarified in this paper. Four brand new trench SiC MOSFETs were applied with V_{gs} of -36 V, -24 V, 24 V, and 36 V for 1000 s. After the stress, short circuit stress with V_{ds} of 400 V and V_{gs} of +17/-5 V was applied to the devices. Experimental results are shown in Fig. 22. It can be discovered that after BTI tests, all devices experienced V_{th} and R_{on} drift, and the greater the gate stress, the more pronounced the drift is. Besides, the negative V_{gs} tends to decrease the V_{th} and increase the short circuit current while the impact of the positive V_{gs} acts the opposite.

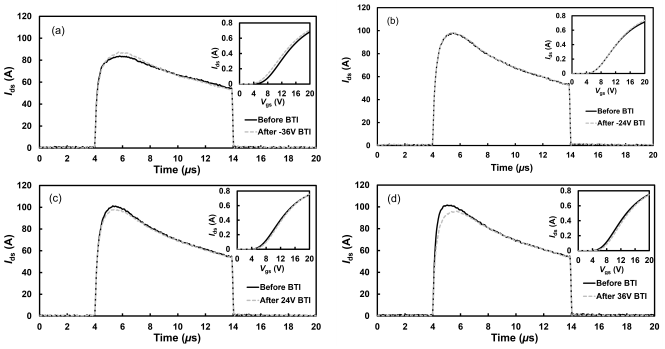

Fig. 22. Influence of negative and positive BTI on short circuit performance. (a) V_{gs}=-36 V, (b) V_{gs}=-24 V, (c) V_{gs}=24 V, (d) V_{gs}=36 V.

Except for the BTI stress, the device also suffers from alternative temperature fluctuation due to frequent turn-on/off, change in case temperature under working conditions. It is important for engineers to develop the overhaul and maintenance plan based on the lifetime of power devices in case of unexpected failure. However, it is a complex subject since it is difficult to reproduce the actual stress and calculate the accurate lifetime. So far, many researchers have conducted different types of accelerated tests from different aspects to induce specific types of failure and plenty of lifetime models have been proposed to improve the accuracy [115]–[118], but the impact of unexpected events, such as short circuit, on lifetime prediction is barely considered. On one hand, the device suffers from alternating electrical and thermal stress, the aging of electrical parameters is inevitable [44], [119]. On the other hand, the occurrence of the short circuit events impacts the power cycling performance in turn, and the effect of short circuit events on the accelerating failure and lifetime reduction should be taken into account. In [120], the short

circuit performance of 1.2 kV SiC MOSFETs was tested under different degradation levels. Test results revealed that the parameter degradation induced by the packaging damage barely affected the short circuit reliability, but the deterioration of the gate oxide after power cycling had a huge impact on the device, and SCWT was reduced after the power cycling test. In [121], [122], mixed experiments were firstly carried out to figure out the impact of repetitive short circuit events on the remaining lifetime of the SiC MOSFET device. Different cycles of short circuit events were applied to SiC MOSFETs after same cycles of power cycling tests. Results showed that with the increase in short circuit cycles, there was a decrease in I_{ds}, V_{gs}, and short circuit energy. Besides, devices under mixed experiments dissipated larger power and induced a higher T_j fluctuation compared with devices that only suffered from power cycling tests. The lifetime deduced as a function of tested short circuit energy and initial short circuit energy was proposed to calibrate current lifetime models. In order to gain more convincing results for lifetime prediction, the mutual effect of power cycling and short circuit events should be thoroughly investigated. Acceleration factors such as temperature, V_{gs} and V_{ds} should be considered in the model to precisely evaluate the device reliability under actual working conditions.

VII. Conclusion

This paper has experimentally reviewed the latest trends on short circuit reliability research of SiC MOSFET devices including the recently released generation of SiC devices and different gate structures. The emphasis is given on four topics including failure mechanism, degradation pattern, influencing factors, and characterization methods to better understand the state-of-art SiC MOSFET devices. Concerning problems in testing, connection, optimization, protection, and evaluation of SiC MOSFETs under short circuit condition have been pointed out. The following conclusions can be drawn:

(1) The failure mechanisms of the SiC MOSFET under singular short circuit event can be divided into two categories: thermal runaway failure and gate destruction. The positive feedback between the sharp temperature rise and carrier generation will eventually cause the thermal runaway failure. The large thermal-mechanical stress and the infiltration of melting Al into the gate oxide crack is the root cause of gate failure. Compared with the thermal runaway failure, the temperature causing the gate failure is lower and the time is longer.

(2) Repetitive short circuit events bring about the degradation of static and dynamic parameters of SiC MOSFETs. The defects in the oxide and the accumulation of charges caused by high electric field and temperature are main reasons. The injection of electrons into the oxide leads to the positive shift of V_{th}, thereby increasing R_{on}, t_{on}, and E_{on}, while the I_{ds}, t_{off} and E_{off} will be decreased. It is noted that the increase of I_{gss} is not only dependent on injected charges but also related to the health status of the oxide.

(3) Test conditions have a notable impact on the short circuit reliability of SiC MOSFET. High V_{ds} is more likely to cause thermal runaway failure, while there is a higher probability to cause gate failure under low V_{ds} conditions. As for the effect of temperature, the device with lower initial temperature tends to have longer SCWT in destructive short circuit events. The reliability for devices in repetitive tests under different temperatures may depend on test conditions and manufacturers.

(4) Several characterization methods have been proposed to reproduce the device behaviour during the short circuit impulse. The TCAD model is the most instinctive and informative way to reveal internal electrical-thermal behavior and verify the degradation/failure mechanism, through which important indicators such as current density, electric field, impact ionization rate, temperature distribution, etc, can be obtained. Recently, the effect of mechanical stress is taken into account and two-dimensional TCAD models have been improved to be three-dimensional ones. However, to build an accurate TCAD model, the chip dimension must be known, and the material properties, doping concentration, and physical models should be carefully selected. Hence, it is hard to develop the model if the chip structure is unknown, and it can also be time-consuming to calculate the finite element model. Compared with the TCAD model, the behavior model can reproduce the voltage, current, power, and T_j during the short circuit transient more easily by considering semiconductor physics and heat dissipation equations, but it is difficult to illustrate internal behaviors. The thermal network model is a simple and quick way to estimate the overall T_j based on the generated power. Depending on whether the chip is considered as a whole or the chip is divided into different layers, different accuracy can be achieved, and basic information on the chip size is essential. As for the advanced measurement methods, the devices are often specially treated and test platforms are customized. Specific instruments such as the optical microscope and high-speed camera might be required to make it possible for monitoring the chip behaviour in real-time during the short circuit transient.

(5) Despite plenty of simulations and tests, the research on short circuit reliability of SiC MOSFET is still not comprehensive. Comparisons on the short circuit reliability of state-of-art SiC MOSFETs need updating to provide useful information to engineers and applications. Approaches to improve the short circuit robustness of devices, short circuit protection performance, and short circuit reliability among parallel devices should be further studied. The reliability assessment of SiC MOSFET under application conditions still has a long way to go.

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Renze Yu received the B.S. and M.Eng. degrees from the China University of Mining and Technology, Xuzhou, China, and Chongqing University, Chongqing, China, in 2018 and 2021, respectively, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical engineering with Electrical Energy Management Group Laboratory, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K.

His research interests include the performance and reliability analysis of wide-bandgap power semiconductor devices, including silicon carbide and gallium nitride devices in power electronics applications.

Saeed Jahdi (Senior Member, IEEE) received the Ph.D. degree in power electronics from the University of Warwick in Coventry, Coventry, U.K., in 2016. He is an Assistant Professor of power electronics with Electrical Energy Management Group, University of Bristol, Bristol, U.K. Formerly, he was with the HVDC Center of Excellence of General Electric, General Electric (GE) Grid Solutions, Stafford, U.K., as a Power Electronics Engineer and Line-Coordinator on several onshore and offshore VSC-HVDC projects in the U.K., Germany, Sweden, France, and Italy. He is also a Chartered Engineer with the U.K. IET. His research interests include wide-bandgap power semiconductor devices in power electronics.

Dr. Jahdi was a recipient of the GE's competitive Early-Career Engineering Award in 2018 for contribution to the success of these flagship HVDC projects by GE, and the 2021 outstanding paper award for the IEEE Transactions on Industrial Electronics.

Olayiwola Alatise received the B.Eng. (first class Hons.) degree in electrical/electronic engineering and the Ph.D. degree in microelectronics and semiconductors from Newcastle University, Newcastle upon Tyne, U.K., in 2005 and 2008, respectively.

He is currently a Professor and Royal Society Industry Fellow in power electronics with the University of Warwick, Coventry, U.K. He has led several research projects in power electronics and is currently working on industrial projects with major automotive OEMs. In 2004 and 2005, he joined ATMEL North Tyneside where he worked on the process integration of the 130-nm CMOS technology node. In June 2008, he joined the Innovation R&D Department, NXP Semiconductors, as Development Engineer where he designed, processed, and qualified discrete power trench MOSFETs for automotive applications and switched-mode power supplies. In November 2010, he joined the University of Warwick and has been a Professor in electrical engineering, since 2019. He has the authored or coauthored more than 130 journal/conference publications and supervised 11 PhDs in Power Electronic devices.

Prof. Alatise was a recipient of the 2021 best paper award in the IEEE Transactions in Industrial Electronics and 2023 best paper award at CIRED. He was an Associate Editor for the IEEE Journal of Emerging and Selected Topics in Power Electronics, a Chartered Engineer, and Fellow of the IET.

Jose Ortiz-Gonzalez received the B.Eng. degree in electrical engineering from the University of Vigo, Vigo, Spain, in 2009, and the Ph.D. degree in power electronics from the University of Warwick, Coventry, U.K., in 2017.

Since 2013, he has been with the School of Engineering, University of Warwick, Coventry, U.K. He was a Senior Research Fellow in power electronics in January 2018. Since August 2019, he has been an Assistant Professor in power electronics. He has authored or coauthored more than 40 publications in journals and international conferences. His research interests include electrothermal characterization of power devices, reliability, and condition monitoring.

Sai Priya Munagala received the B.Tech, M.Sc and PhD degrees in 2012, 2015 and 2020 from Jawaharlal Nehru Technological University, India, Technische Universität Darmstadt, Germany and the University of Birmingham, UK respectively.

Dr Munagala is currently a research associate in the Electrical Energy Management Group at the University of Bristol, UK. Her research is on post processing of additively manufactured alloys to improve the performance of electrical machines . Her interests include high temperature materials, fabrication of advanced materials, recycling of materials, metal additive manufacturing and material characterisation.'

Nick Simpson received the B.Eng. and Ph.D. degrees in electrical engineering from the University of Bristol, Bristol, U.K., in 2009 and 2014, respectively.

Dr Simpson is currently Associate Professor of Advanced Electrical Machine Design and a member of the Electrical Energy Management Group within the Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. His research focuses on performance improvement of electrical machines through advanced multi-physics design and manufacturing techniques, with a particular interest in additive manufacturing of active components.

Phil Mellor received the B.Eng. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, University of Liverpool, Liverpool, U.K., in 1978 and 1981, respectively.

Prof. Mellor is currently a Professor of electrical engineering with the Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. Prior to this, he held academic posts with the University of Liverpool, from 1986 to 1990, and the University of Sheffield, Sheffield, U.K., from 1990 to 2000. His research interests include high-efficiency electric drives and actuation and generation systems for application in more electric aircraft and hybrid electric vehicles.