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Design and Investigation of a Metamorphic InAs Channel Inset InP HEMT for Cryogenic Low-Noise Amplifiers

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ABSTRACT This work proposes a 100 nm metamorphic InP HEMT with an InAs channel inset for cryogenic environment millimetre wave applications. The usage of an ultra-thin 2 nm barrier layer, unique composite channel topology and III-V material selection provides superior electron confinement in the channel, enhancing 2DEG concentration and mobility, thereby improving the speed of the proposed device. We achieve a unity current gain frequency (f_T) of 248.9 GHz and a maximum oscillation frequency (f_{MAX}) of 523.9 GHz with a current gain of 67.7 dB at 0.1 GHz, 298 K. A f_T/f_{MAX} of 5.02 GHz/10.01 GHz is achieved at 90 K. Off-state leakage current is in the nanoampere range with minimum noise figure (NF_{MIN}) of only 0.09 dB at 10 GHz, 90 K. We compare the DC, RF, noise and parasitic characteristics of the proposed device with other composite channel InP HEMTs proposed in latest works and showcase performance improvements in all domains. The performance achieved by using an InAs insert specifically is also justified, with InGaAs-InAs-InGaAs channel HEMTs providing 1.4 times better f_T and f_{MAX} with only half the NF_{MIN} of their InGaAs-InP-InGaAs channel counterparts. The proposed composite channel device showcases anomalous trends in electron scattering rate and electron mobility with impurity concentration and temperature variation. A novel frequency-and-temperature dependent small signal model has been put forth which accounts for these atypical cryogenic trends to accurately predict the behavior of the device under varying RF and temperature conditions.

INDEX TERMS Composite channel FETs, Cryogenic electronics, high electron mobility transistors (HEMTs), Low Noise Amplifiers (LNAs), Millimetre wave applications, Ultrathin Barrier

I. INTRODUCTION

Traditional silicon-based devices encounter performance limitations when operating in cryogenic environments, primarily due to heightened sensitivity to defects, impurity scattering, reduced carrier mobility, and thermal expansion mismatch [1]. To surmount the limitations faced by silicon devices at cryogenic temperatures, we use III-V materials which exhibit superior mobility and diminished impurity scattering, owing to lower extrinsic doping requirements [2]. The higher bandgap of III-V materials at the heterointerfaces enables superior electron confinement, enhancing carrier mobility. When designing a III-V heterostructure device, however, various III-V combinations can be considered for the formation of a HEMT [3], [4].

InP and GaAs have been selected for our proposed device due to their inherent material characteristics that

facilitate optimal cryogenic performance. InP and GaAs possess relatively narrow bandgap energies of 1.35 eV and 1.42 eV respectively, in contrast to GaN's 3.39 eV bandgap [5]. This reduced bandgap allows for more accessible electron excitation at cryogenic temperatures, where thermal energy for electron excitation is substantially diminished [6]. Notably, InP exhibits relatively low thermal generation rates compared to other III-V materials, resulting in a significant decrease in the thermal generation of electron-hole pairs at cryogenic temperatures [7]. This characteristic contributes to maintaining lower noise levels and improving the overall signal-to-noise ratio in cryogenic devices [8]. Furthermore, InP exhibits excellent material stability under extreme low-temperature conditions, demonstrating minimal degradation in performance and reliability [9], [10]. For a typical FET device, the improvement of cutoff frequency and the reduction of noise

and parasitics go hand in hand as given by the Fukui equation [11] (1), (2).

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{GS} + C_{GD})(1 + \frac{R_S + R_D}{R_{DS}}) + g_m C_{GD}(R_S + R_D)} \quad (1)$$

$$NF_{MIN} = 10 \log(1 + 2\pi K_f f C_{GS} \sqrt{\frac{R_G + R_S}{g_m}}) \quad (2)$$

In composite channel FETs however, due to anomalous electron mobility and non-linear impact ionization behavior as proposed by Pozdnyakov's impurity dependent rate scattering and angle model [12] the Fukui model is inapplicable, particularly at cryogenic temperatures.

In composite channel HEMTs at cryogenic temperatures it is found that the HEMT layer topology that provides maximum cutoff frequency and the topology that provides minimized noise are different from one another, violating Fukui's model.

RF specialized InP HEMTs are being proposed to meet an acute industry demand for devices with high f_T , f_{MAX} and acceptable noise characteristics. 5G & 6G applications [13],[14], millimetre wave applications [15],[16], imaging applications [17], cryogenic applications [18]-[20], MMIC [21] and several emerging use cases [22] necessitate the usage of InP HEMTs for RF applications.

In this work, we design a composite channel HEMT and explain the tradeoff between gain optimization and noise optimization. The movement restriction and flow control of electrons within the composite channel are analyzed.

The bandgaps present on either side of the 2-dimensional-electron-gas (2DEG) and their effect on confining the majority charge carriers as they flow through the device is analyzed. The HEMT consequently proposed by utilizing our optimization supersede existing composite channel HEMTs in terms of RF, DC and noise characteristics. In Fig. 1, we compare our proposed HEMT with existing HEMTs [23]-[27] for LNA applications. Since f_T is proportional to L_G^{-2} , $f_T \cdot L_G^2$ is a constant for a given FET device [28]. Hence, comparing $f_T \cdot L_G^2$ allows one to compare the RF performance of FETs with different L_G values.

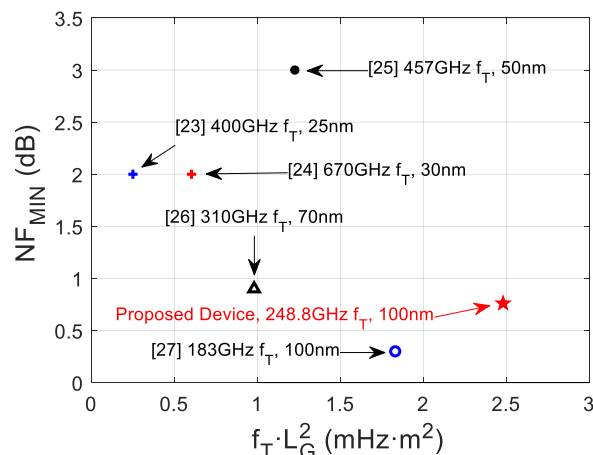


FIGURE 1. Comparison of simulation results of the proposed HEMT with measured data of recently suggested HEMTs for LNA applications.

II. DEVICE STRUCTURE AND SIMULATION ENVIRONMENT

The usage of a 2 nm ultrathin barrier layer and a channel inset in the proposed HEMT has been shown in the structure diagram Fig. 2. An $\text{In}_{0.08}\text{Ga}_{0.92}\text{As}$ passivation layer has been used to improve the noise performance of the device and an InP layer has been used as etch stop.

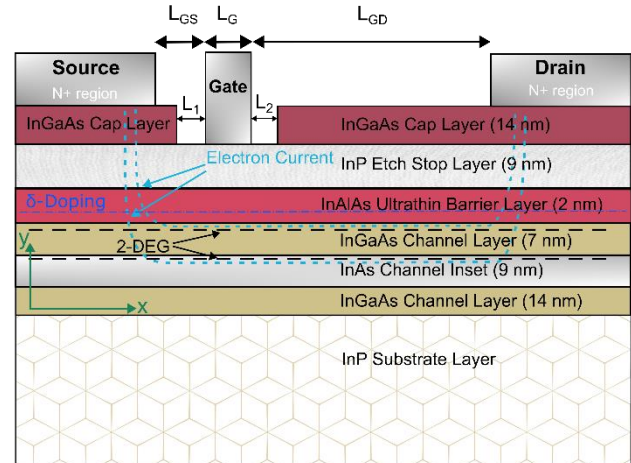


FIGURE 2. Structural diagram of the proposed HEMT.

TABLE 1. Optimized x-axis dimensions with 100 nm L_G .

Lateral Dimension	Optimized Value (nm)
L_{GS}	170 nm
L_G	100 nm
L_{GD}	530 nm
L_1	50 nm
L_2	50 nm

A. Ultra-thin barrier layer

When barrier thickness is reduced to the scale of the electron wavelength, quantum confinement effects dominate. Electrons in the 2-DEG are confined within the quantum well formed by the 2nm thin barrier layer and the heterojunction interface. Due to the reduced thickness, the quantum well potential energy profile becomes steeper, creating a stronger potential energy barrier, confining the electrons in the lateral direction to a narrow region near the heterojunction interface.

Electrons in the 2-DEG channel exhibit a wave-like nature and are subject to the principle of minimum energy. When the barrier layer is thin, the energy levels of the electrons become quantized within the quantum well. The electrons tend to occupy the lowest energy states available within the well, which correspond to the region near the heterojunction interface [29]. This energy minimization behavior further confines the electrons to a narrow region near the interface. Electrons on either side of the heterojunction occupy energy levels corresponding to an array of potential wells. Assuming the mass of an electron travelling within this array of potential wells to be m^* , in a well of width L_z in the Z direction satisfies the free particle Schrodinger equation (3)

$$-\frac{\hbar^2}{2m^*} \frac{d^2\psi}{dz^2} = E\psi \quad (3)$$

with eigenvalues (4),

$$E_n = \frac{\hbar}{2m^*} \left(\frac{n\pi}{L_z}\right)^2 = \left(\frac{\hbar^2 \pi^2}{2m^* L_z}\right) n^2 \quad (4)$$

with eigenfunctions (5),

$$\psi_n = A \sin(n\pi z/L_z) \quad (5)$$

where z is the perpendicular distance from the heterointerface, ψ denotes the amplitude of the charge carrier's wave motion, m^* denotes the mass of the charge carrier, L_z is the width of the well within which electrons travel and n denotes the n th energy band from the heterointerface. The farther away an electron propagates from the heterointerface, the more excited it is (higher value of n in (4) and (5)). This causes it to vibrate away from well-defined planar wells in the 2DEG [30]. The movement of electrons perpendicular to the planar 2DEG region causes a loss in mobility within the 2DEG as the net velocity of the carriers is distributed across three dimensions instead of two [31]. If we create our material interfaces to be 1 nm – 2 nm in thickness, electrons are forced to occupy the low energy states near the heterojunction of the barrier-channel interface as higher energy states are physically absent. The effects of an ultrathin barrier layer help improve the electron current density of the upper 2DEG region from 1.94×10^8 A/cm² to 2.08×10^8 A/cm².

B. InAs Channel Inset

Due to the channel inset, two heterointerfaces are formed within the channel, resulting in two 2DEG (two-dimensional electron gas) regions. This is shown in Fig 3. where peak electron current density is observed in three regions- 3.96×10^8 A/cm² in the ultrathin barrier, 2.08×10^8 A/cm² in the upper InGaAs-InAs channel inset heterointerface and 1.94×10^8 A/cm² in the lower InAs-InGaAs channel inset heterointerface. This results in a “net” 2DEG electron current density of 4.02×10^8 A/cm² exceeding the 2.55×10^8 A/cm² electron current density observed in the single channel HEMT with the same dimensions. This results in improved f_T and f_{MAX} in the inset

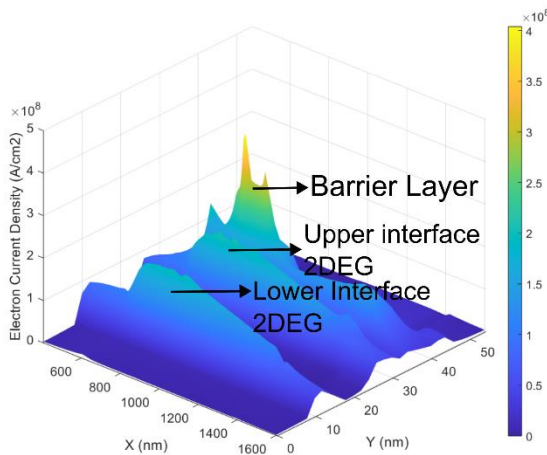


FIGURE 3. Electron current density within the device at the Barrier Layer and each of the two 2DEG regions.

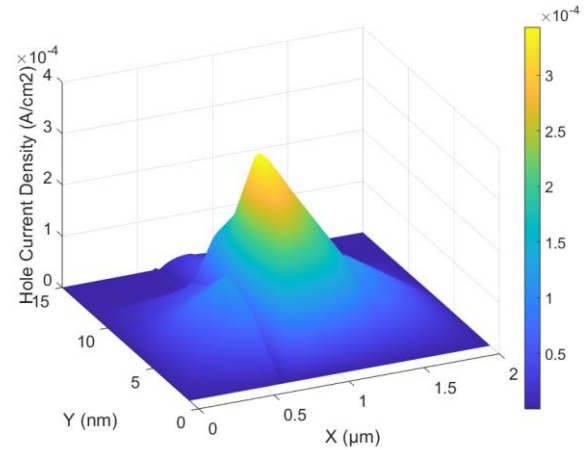


FIGURE 4. Peak hole current generation is observed underneath the gate at the second 2DEG region.

channel HEMT compared to the single-channel HEMT. Fig. 4 depicts the hole current generation in the device which was seen in the second 2DEG region alone.

C. Electrical and mathematical models

To accurately model charge carrier behavior, electron mobility at cryogenic temperatures was simulated using the Caughey-Thomas model while trap generation and recombination were simulated using the Shockley-Read-Hall model. The Caughey-Thomas mobility model is an empirical mobility model used for semiconductors. It was specifically used as it incorporates scattering mechanisms such as lattice scattering, impurity scattering, and surface scattering, all while being applicable at a wide temperature range (6) [32].

$$\mu_n(E) = \mu_{n0} \sqrt{\frac{1}{1 + \left(\frac{\mu_{n0} E}{v_{sat}}\right)^2}} \quad (6)$$

where μ_{n0} is low-field electron mobility, E is the electric field, and v_{sat} is the electron saturation velocity. The electron saturation velocity is defined as 2×10^7 cm/s, which is obtained by linear interpolation from InAs and GaAs. Impact ionization and Band-Gap-Narrowing (BGN) models were used while employing Fermi-Dirac statistics instead of Boltzmann statistics due to the presence of high doping concentration.

D. Simulation Environment

1) Low Temperature Simulations

The intrinsic carrier concentration decreases with a decrease in temperature. In quasi-neutral regions, the minority carrier concentration can cause underflow. To avoid computational underflow in low temperature simulations, 160-bit precision computing is enabled in the ATLAS engine. Further, cryogenic material-specific models are enabled which help in achieving more accurate results at cryogenic temperatures.

2) Impurity scattering

Lattice sites are several thousand times heavier than the charge carriers that travel through the device. Impurity scattering is consequently elastic in nature. For the energy distribution of simulated charge carriers to match the true charge carrier distribution, certain energy dissipation mechanisms are employed for carriers within the lattice. The Ridley impurity scattering model is implemented in the TCAD simulation. The scattering rate is calculated by the ATLAS engine upon enabling the RIDLEY flag.

Additionally, phonon scattering is computed by the ATLAS engine based on an energy dependent model stated as follows:

Deformation potential H' is computed as:

$$H' = E \frac{dy}{dr} \quad (7)$$

Where dy/dr is the deformation of the lattice due to phonons and E is the tensor that describes the shift in the electron band per unit deformation.

3) Lattice trap handling

Trap charges and corresponding trap carrier transitions that occur throughout the device were modelled using the Shockley-Read-Hall recombination model as shown in (8)

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUPO \left[n + n_{ie} \exp\left(\frac{ETRAP}{kT_L}\right) \right] + TAUNON \left[p + n_{ie} \exp\left(\frac{ETRAP}{kT_L}\right) \right]} \quad (8)$$

Within this model, the ETRAP parameter handles trap charges and corresponding trap energy levels. Additionally, to enable electron trap modelling and hole trap modelling, DEVDEG.E and DEVDEG.H flags have been enabled in the Silvaco TCAD simulation tool.

4) Mobility modelling

To perform accurate low-field mobility modelling, the ANALYTIC and ARORA models are enabled. In this manner, when a lattice temperature is specified, temperature dependent parametric values are evaluated locally at each point in the device. When lattice heating is not enabled, the model employs a constant global temperature within the device. With lattice heating, the thermal generation caused by impurity scattering is accounted for by the simulator.

III. RESULTS AND DISCUSSION

A. DC performance

The $I_{DS}-V_{GS}$ curve at 298 K is shown in Fig 5(a). The threshold voltage for which the device transitions from OFF to ON is negative, making it a depletion type device. The variation in these characteristics with a decrease in temperature is due to reduced thermal noise, which lowers the lattice scattering resulting in improved carrier transport efficiency. These trends are apparent in Figs. 5(b) and 5(c).

Fig. 5(d) shows that the value of saturation-drain current reduces with temperature. I_{DS} values at 300 K and 100 K are compared for the same biasing.

For low electric fields in the barrier, gate leakage is dominated by trap-assisted tunneling (TAT) and Poole-Frenkel (PF) emission. Donor-like traps concurrently exist on the HEMT surface and the 2-DEG in the channel originates from the ionization of the donor-like traps. The leakage current density from the channel to the gate is modelled as trap-assisted tunneling current and has a similar form to that of thermionic emission (9) [33].

$$J_{TAT} = J_0 \left\{ \exp\left[\frac{q(V_{GS}-V_0)}{\eta kT}\right] - 1 \right\} \quad (9)$$

where, J_0 , V_0 , and η are parameters used to fit the experimental data, q is the fundamental electronic charge, k is the Boltzmann constant, and T is temperature. Poole-Frenkel emission describes emission from traps by thermal activation but with a lowered trap depth induced by Coulomb interaction. The leakage current density due to this effect is termed Poole-Frenkel leakage and can be expressed as [33]:

$$J_{PF} = C_{PF} E \exp\left[-\frac{q(\phi_t - \sqrt{qE/\pi\epsilon_0\epsilon_S})}{kT}\right] \quad (10)$$

where C_{PF} is a constant, E is the electric field across the barrier, ϕ_t is the barrier height for the electron emission from the trap state, ϵ_0 is the permittivity of vacuum, and ϵ_S is the relative permittivity of AlGaN at high frequencies. For high barrier electric field, Fowler-Nordheim tunneling dominates leakage effects. At higher electric fields, electrons in the gate may tunnel through a rounded triangular barrier. Such leakage is modelled as Fowler-Nordheim tunneling current density (11) [33].

$$J_{FN} = AE^2 \exp\left(-\frac{8\pi\sqrt{2m_e}(q\phi_b)^3}{3q\hbar E}\right) \quad (11)$$

where ϕ_b is the Schottky barrier height. The net gate leakage current that is valid for a range of barrier electric fields can be expressed as (12).

$$J_G = J_{TAT} + J_{PF} + J_{FN} \quad (12)$$

The total gate leakage current in the 90 K – 150 K temperature range for the proposed device is shown in Fig. 5(e). The leakage current is observed to be in the sub-nanoampere range. A transient analysis of the proposed device was performed and is shown in Fig. 5(f). A minimum rise time and fall time of 3.1 ps was achieved corresponding to a driver switching time of 3 ps.

B. AC and Noise performance

As the operating frequency of the proposed HEMT is increased, several changes occur in transit time, parasitics and impedances within the device which manifest as a reduction in gain with an increase in frequency. As operating frequency increases, the time available for the carriers to travel through the device from the source to the drain decreases. This results in reduced gain as the carriers have less time to contribute to the output current. Parasitic capacitances associated with various device regions and

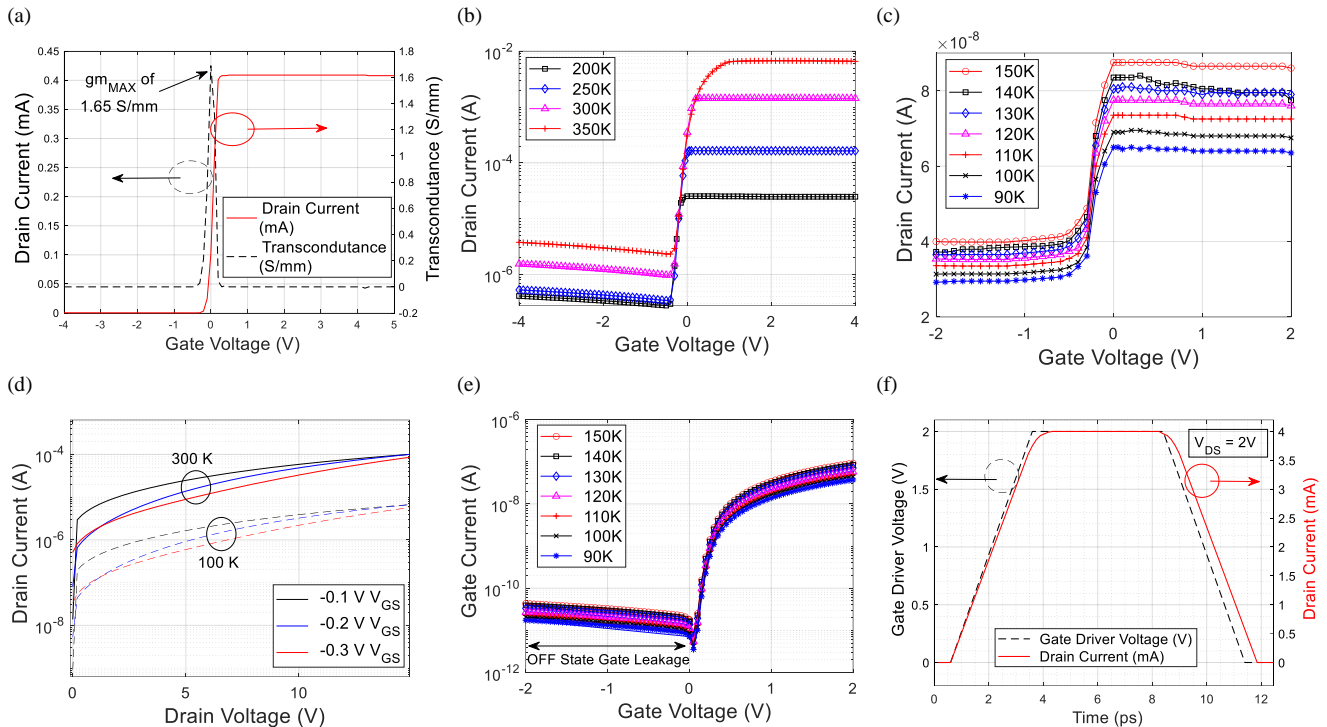


FIGURE 5. (a) I_{DS} - V_{GS} of proposed HEMT at 298 K. Peak transconductance g_{mMAX} of 1.65 S/mm is observed. The solid curve shows the drain current in mA and corresponds to the left y-axis. The dashed curve shows transconductance in S/mm and corresponds to the right y-axis. (b) I_{DS} - V_{DS} curve of proposed HEMT in 350 K-200 K range for a device width of 500 μ m. (c) I_{DS} - V_{GS} curve of proposed HEMT in 150K-90K range. (d) I_{DS} - V_{DS} curve of proposed HEMT at 300 K and 100 K. Black, blue and red lines denote V_{GS} biasing of -0.1V, -0.2V, -0.3V, respectively. Solid lines indicate behavior at 300 K and dashed lines indicate behavior at 100 K (e) Gate leakage characteristics: I_{GS} - V_{GS} curve of proposed HEMT in 150 K-90 K range. (f) Transient Analysis of the proposed HEMT. A minimum rise time and fall time of 3.1 ps was achieved corresponding to a driver switching time of 3 ps. The dashed curve shows gate driver voltage in V and corresponds to the left y-axis. The solid curve shows drain current in mA and corresponds to the right y-axis.

interconnects become more significant at higher frequencies.

The parasitic capacitances act as low-pass filters, attenuating the high-frequency components of the input signal. The roll-off of gain at 20 dB/dec rate is seen in our device across a range of temperatures seen in Figs. 6(a) to 6(d).

It is seen that f_{MAX} has a larger dependency on parasitic components than f_T . As parasitic components vary with temperature, f_{MAX} shows a larger temperature dependency than f_T , as is shown by the data in Table 2.

TABLE 2. Variation of f_T and f_{MAX} of the proposed HEMT with temperature

Temperature (K)	f_T (GHz)	f_{MAX} (GHz)
350	248.3	665.3
300	247.2	526.0
250	231.5	365.1
200	196.0	214.4
150	168	152
140	150	134
130	116	103
120	72.7	67.7
110	30.1	29.7
100	10.00	19.98
90	5.02	10.01

Noise must be reduced in an LNA to preserve the integrity of weak signals. By minimizing unwanted noise

contributions, the LNA can enhance the signal-to-noise ratio, enabling accurate and reliable amplification of low-level signals without distortion or degradation.

The variation of NF_{MIN} (minimum noise figure) and G_N (noise conductance) in the cryogenic (90 K – 150 K) temperature range is shown in Fig. 6(e) and Fig. 6(g). The variation of NF_{MIN} and G_N in the 200 K – 350 K temperature range is shown in Fig. 6(f) and Fig. 6(h). T_{min} (minimum noise temperature) of the proposed HEMT in the cryogenic operation range has been computed using the Pospieszalski Noise Model [34]. The Pospieszalski Noise Model equation is given in (13).

$$T_{min} = \frac{f}{f_T} \sqrt{r_{gs}g_{ds}T_gT_d + \left(\frac{f_T}{f}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2} + 2\left(\frac{f_T}{f}\right) r_{gs}g_{ds}T_d \quad (13)$$

where, r_{gs} , g_{gs} , T_g and T_d are small signal model parameters that are explained in section IV. The computed T_{min} lies between 6 K and 10 K at an ambient temperature of 90 K-110 K as shown in Fig. 6(i).

C. Material Selection for Channel Inset

Device performance using different composite channel materials has been analyzed. Using an InGaAs-InAs-InGaAs composite channel provided higher f_T and f_{MAX} than a full InGaAs channel as seen in Fig. 7(a) but displayed

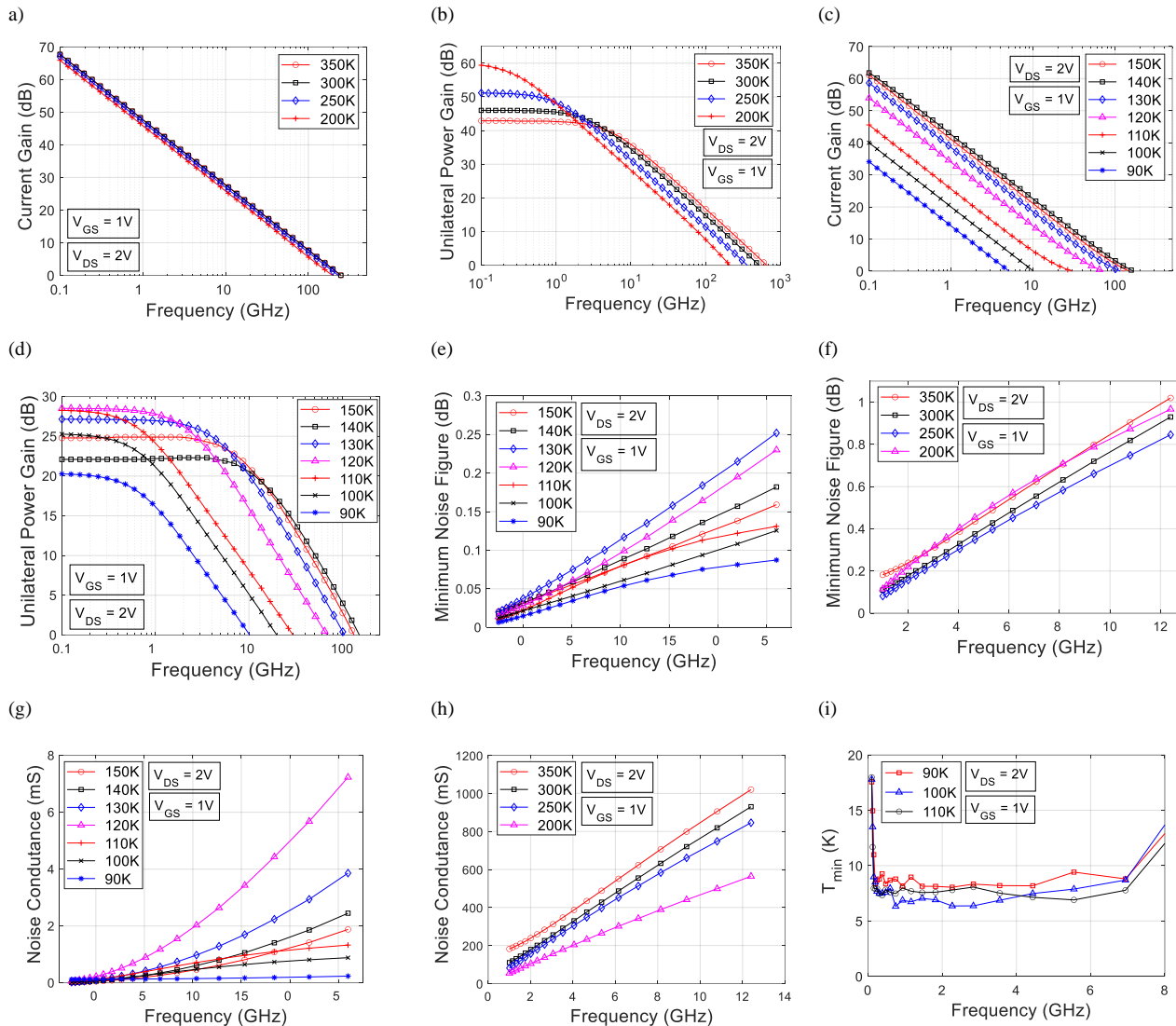


FIGURE 6. (a) Current Gain vs Frequency curve of proposed HEMT in 350 K-200 K range. (b) Unilateral Power Gain vs Frequency curve of proposed HEMT in 150 K-90 K range. (c) Current Gain vs Frequency curve of proposed HEMT in 150 K-90 K range. (d) Unilateral Power Gain vs Frequency curve of proposed HEMT in 150 K-90 K range. (e) Minimum Noise Figure vs Frequency curve of proposed HEMT in 150 K-90 K range. (f) Minimum Noise Figure vs Frequency curve of proposed HEMT in 350 K-200 K range. (g) Noise Conductance vs Frequency curve of proposed HEMT in 150 K-90 K range. (h) Noise Conductance vs Frequency curve of proposed HEMT in 350 K-200 K range. (i) Minimum Noise Temperature vs Frequency curve of proposed HEMT in 110 K-90 K range.

marginally higher NF_{MIN} as well due to the increased number of heterointerfaces in a composite channel. This is observed in Fig. 7(b). An InGaAs-InP-InGaAs composite channel, however, showed much worse performance than the InGaAs-InAs-InGaAs composite channel and full InGaAs channel, showcasing lower f_T and f_{MAX} and about twice the NF_{MIN} of the other two channel types as tabulated in Table 3.

The InGaAs-InAs-InGaAs composite channel structure, with its varying bandgaps, offers a higher cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) due to improved electron confinement and transport. However, the presence of heterojunction interfaces and interface imperfections in the composite channel can introduce additional noise sources, affecting noise parameters such as NF_{MIN} and G_N (noise conductance).

Table 3. Variation of f_T , f_{MAX} and NF_{MIN} with channel composition.

Channel composition	f_T (GHz)	f_{MAX} (GHz)	NF_{MIN} at 10 GHz (dB)
InGaAs-InAs-InGaAs	248.9	523.9	0.764
InGaAs-InP-InGaAs	181.8	202.6	1.584
InGaAs	241.5	449.4	0.725

D. Non-linear parameter variation and optimization challenges

For inset channel devices, it is found that f_T , f_{MAX} , noise and other parameters do not vary predictably with variation in doping concentration. This is due to anomalous noise behavior attributed to impurity deionization. Noise often increases due to increased impurity concentration, and several works have been devoted to the investigation of electron scattering by impurity ions in semiconductors.

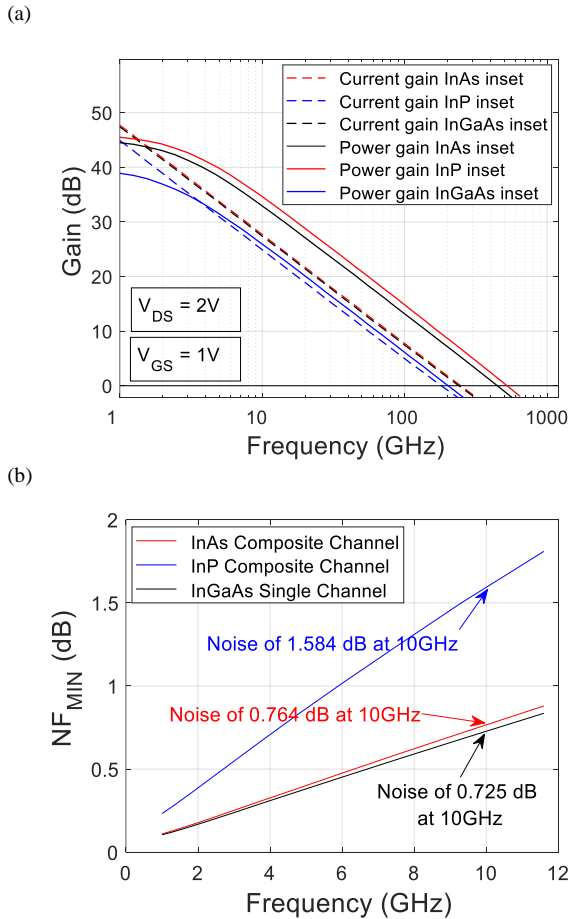


FIGURE 7 (a). Variation of Unilateral Power Gain (dB) and Current Gain (dB) with frequency for different channel inset materials. The dashed curves represent current gain while the solid curves represent power gain. **(b).** Variation of NF_{MIN} with frequency for different channel inset materials.

Following Fukui's equations (1) and (2), the optimized device structures for AC gain performance and AC noise are expected to be the same. However, due to channel inset effects and impurity scattering, they differ from one another, causing a performance trade-off between gain and noise in the device dimension optimization process.

Pozdnyakov's scattering rate model and polar scattering angle model can be used to determine electron mobility characteristics while accommodating the effects of ionized impurities at various concentrations. Pozdnyakov's scattering rate model models are given in (14) to (17) and Pozdnyakov's angle scattering models are given in (18) and (19) [12].

$$W_j = W_j^{aa} + W_j^{ab} + W_j^{bb} \quad (14)$$

$$W_j^{aa} = 4\pi a^2 n_j I_{aa} \left(\frac{2E(1+\eta E)}{m_d(1+2\eta E)^2} \right)^{\frac{1}{2}} \frac{\Xi_{a,j}^2}{1+f_a} \quad (15)$$

$$W_j^{ab} = 8\pi ab n_j I_{ab} \left(\frac{2E(1+\eta E)}{m_d(1+2\eta E)^2} \right)^{\frac{1}{2}} \times \frac{\Xi_{a,j} \Xi_{b,j}}{f_a - f_b} \ln \left(\frac{1+f_a}{1+f_b} \right) \quad (16)$$

$$W_j^{bb} = 4\pi b^2 n_j I_{bb} \left(\frac{2E(1+\eta E)}{m_d(1+2\eta E)^2} \right)^{\frac{1}{2}} \frac{\Xi_{b,j}^2}{1+f_b} \quad (17)$$

where W_j is the scattering rate of electrons by the j -th kind ionized impurities. 'a' and 'b' are the radii of the III-V material's constituent elements. W_j^{aa} denotes scattering between particles of radius 'a', W_j^{ab} denotes scattering between particles of radius 'a' and 'b', and W_j^{bb} denotes scattering between particles of radius 'b'. $\Xi_{a,j}$ and $\Xi_{b,j}$ are two functions such that $\Xi(0) = 1$ and $\Xi(k \rightarrow \infty) \rightarrow 0$ are true where k is the distance between particles 'a' and 'b'.

m_d is the density-of-state electron effective mass and η is the non-parabolicity parameter. ' f_a ' and ' f_b ' denote the collision frequency of particles 'a' and 'b' respectively.

$$\cos(\theta_\rho^{aa}) = 1 - 2 \frac{1-\rho}{1+\rho f_a} \quad (18)$$

$$\cos(\theta_\rho^{bb}) = 1 - 2 \frac{1-\rho}{1+\rho f_b} \quad (19)$$

where θ_ρ^{aa} denotes the scattering angle after collision with a radius 'a' particle and θ_ρ^{bb} denotes the scattering angle after collision with a radius 'b' particle. ρ is the effective charge density while ' f_a ' and ' f_b ' denote the collision frequency of particles 'a' and 'b' respectively.

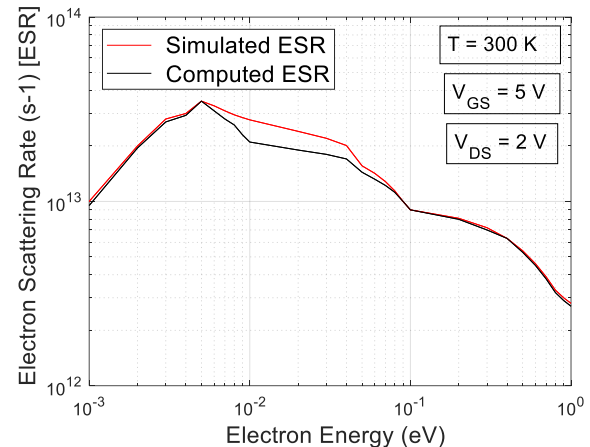


FIGURE 8. Electron Scattering Rate (ESR) variation with Electron Energy. The ESR variation obtained from TCAD simulation was found to match the mathematically computed ESR after accounting for impurity scattering effects within the device.

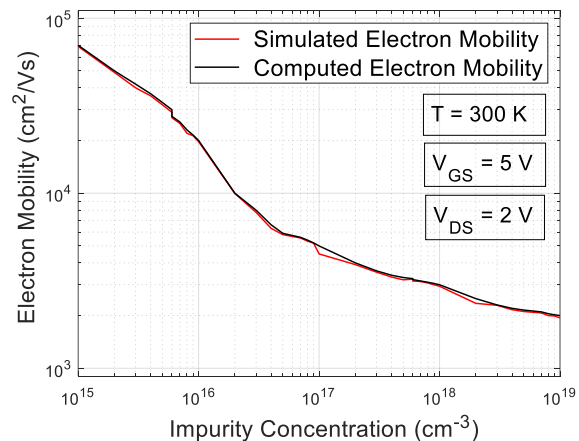


FIGURE 9. Variation of Electron Mobility in the proposed HEMT was found to match the mathematically obtained Electron Mobility only after accounting for impurity scattering effects within the device.

Applying Pozdnyakov's model to our composite channel HEMT in Fig 8, we observe that the modelled variation of electron scattering rate with impurity concentration matches the simulated electron scattering rate, with low error between the mathematically computed data and the data obtained upon TCAD simulation using ATLAS In Fig 9, we observe the non-linear variation in electron mobility as a consequence of impurity scattering.

IV. SMALL SIGNAL MODELLING AND CIRCUIT INTEGRATION

A. Intrinsic FET model creation using Y parameters

Small signal models help a circuit design engineer easily understand the characteristics and behavior of the device being modelled. Small signal models are used to simplify the analysis of electronic circuits by linearizing nonlinear components. They enable the study of circuit behavior around a bias point, making it easier to analyze and design amplifiers and other signal processing systems.

The S parameter model represents the scattering parameters of a device or circuit. It describes the relationship between incident and reflected waves at the ports, enabling analysis of signal transmission, reflection, and impedance matching in microwave systems. The Y parameter model on the other hand represents the admittance parameters of a two-port network.

The proposed HEMT device can be reduced to an intrinsic FET model using either the S parameter model or using the Y parameter model. The extraction of equivalent circuit parameters using S-parameters, however, is an ill-conditioned problem as there are too many unknowns and not enough equations [34]. Typically, optimization-based techniques are used to solve this problem. However, these procedures may lead to element values with no physical meaning and moreover, the results obtained are deeply influenced by the optimization method chosen. This leads us to use the Y parameter model equations (20)-(23) instead for equivalent circuit parameter extraction [35]-[38].

$$Y_{11} = \frac{j\omega C_{gs}}{1+j\omega C_{gs}R_i} + \frac{j\omega C_{gd}}{1+j\omega C_{gd}R_{gd}} \quad (20)$$

$$Y_{12} = -\frac{j\omega C_{gd}}{1+j\omega C_{gd}R_{gd}} \quad (21)$$

$$Y_{21} = \frac{g_m e^{-j\omega\tau}}{1+j\omega C_{gs}R_i} - \frac{j\omega C_{gd}}{1+j\omega C_{gd}R_{gd}} \quad (22)$$

$$Y_{22} = \frac{j\omega C_{gd}}{1+j\omega C_{gd}R_{gd}} + j\omega C_{ds} + \frac{1}{R_{ds}} \quad (23)$$

Using (20)-(23), we can solve for each of the equivalent circuit parameters (ECPs) in the equations (24) to (30):

$$R_{gd} = -Re\left(\frac{1}{Y_{12}}\right) \quad (24)$$

$$R_i = Re\left(\frac{1}{Y_{11}+Y_{12}}\right) \quad (25)$$

$$C_{gd} = \frac{1}{\omega Im\left(\frac{1}{Y_{12}}\right)} \quad (26)$$

$$C_{gs} = -\frac{1}{\omega Im\left(\frac{1}{Y_{11}+Y_{12}}\right)} \quad (27)$$

$$C_{SD} = \frac{Im(Y_{12}+Y_{22})}{\omega} \quad (28)$$

$$g_m = \left| \frac{(Y_{21}-Y_{12})(Y_{11}+Y_{12})}{Im(Y_{11}+Y_{12})} \right| \quad (29)$$

$$\tau = -\frac{Phase\{(Y_{21}-Y_{12})[1+j\frac{Re(Y_{11}+Y_{12})}{Im(Y_{11}+Y_{12})}]\}}{\omega} \quad (30)$$

B. Proposed Temperature and Frequency dependent Intrinsic FET model

Notice that the Y parameters used in this model are not temperature dependent. A critical problem with existing small signal models is that they are not suitable for deep-space or cryogenic applications as these parameters vary with temperature and do not show consistent trends. Using the anomalous electron mobility modelling procedure that was introduced in the device performance section, the effect of ionized impurities creating inconsistent trends at cryogenic temperatures can be modelled accurately. The equivalent circuit parameters obtained can be used to design the intrinsic FET model represented in Fig. 10.

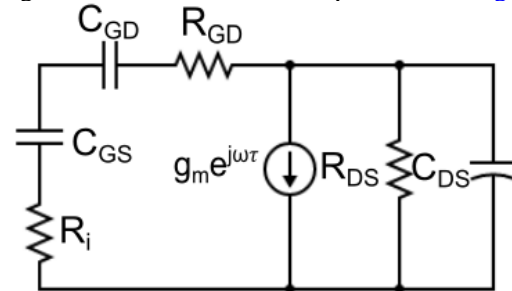
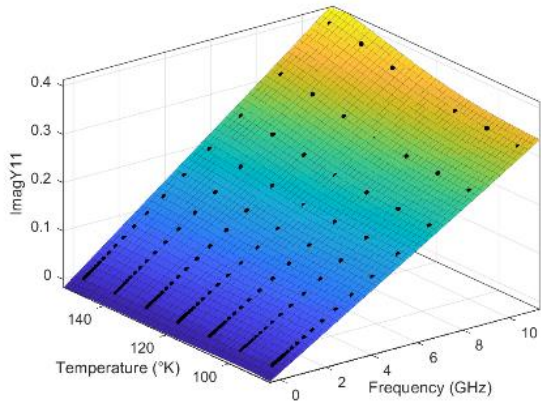


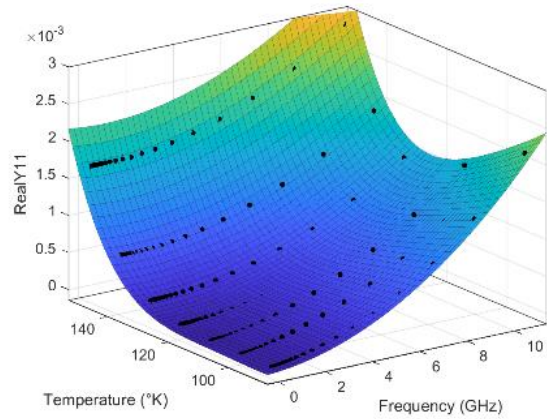
FIGURE 10. Intrinsic FET model using equivalent circuit parameters.

The model being proposed is a temperature dependent Y parameter model and hence, a temperature dependent intrinsic FET model. This proposed model allows one to predict the performance of the device at any intermediate temperature between the simulated data points. Temperature-dependent parameter modeling is vital in designing deep space devices due to the extreme temperature variations encountered. It allows accurate prediction of device performance by accounting for thermal effects on parameters such as resistances, capacitances, and transconductances. The proposed model facilitates proper characterization of the device's behavior over a useful temperature range. The proposed model uses high degree polynomial regression to fit any inconsistent or cyclical trends that are observed in the Y parameter model. The model was fitted to the data using 4th order polynomial regression.

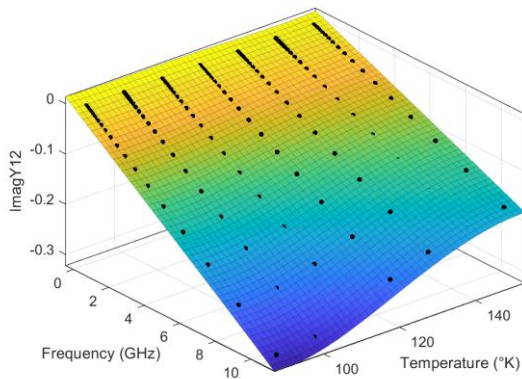
The temperature-dependent equivalent circuit parameter model $Y_{ij}(\theta)$ represents Y_{ij} as a function of temperature. The proposed models, along with corresponding regression characteristics: sum of squares of errors (SSE), R-square, adjusted R-square and Root Mean Squared Error (RMSE) are shown in Figs. 11(a) to (h). The sum of squares error (SSE) is the difference between the observed and predicted values. Lower values of SSE indicate a more accurate



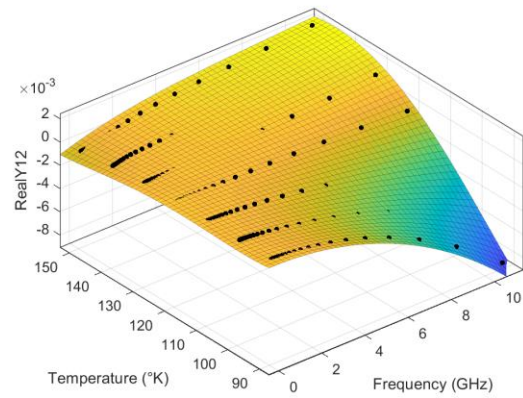
(a) SSE: $8.741e-05$ R-square: 0.9999 Adjusted R-square: 0.9999 RMSE: 0.00079



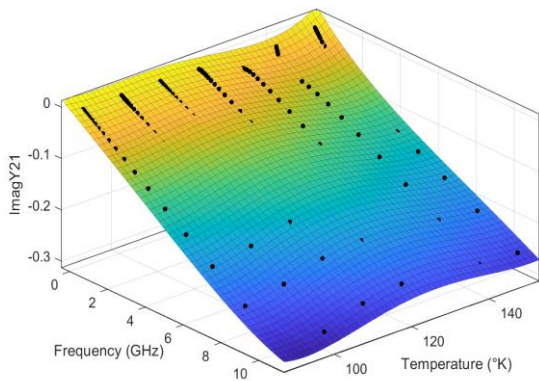
(b) SSE: $4.844e-08$ R-square: 0.9993 Adjusted R-square: 0.9992 RMSE: $1.867e-05$.



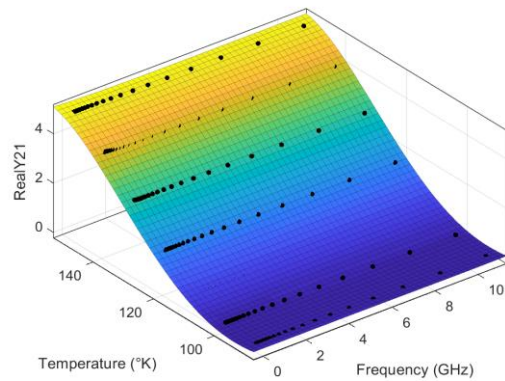
(c) SSE: $2.332e-06$ R-square: 0.9897 Adjusted R-square: 0.9886 RMSE: 0.0001295



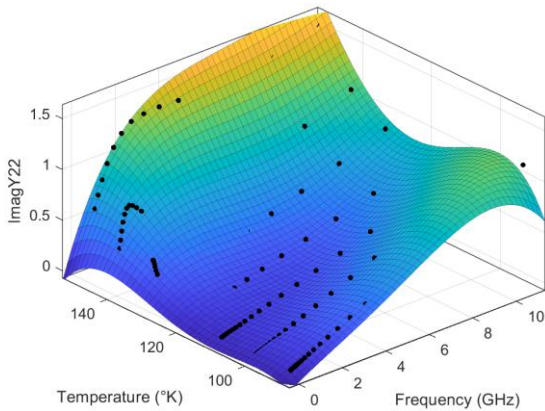
(d) SSE: $5.905e-05$ R-square: 0.9999 Adjusted R-square: 0.9999 RMSE: 0.0006518.



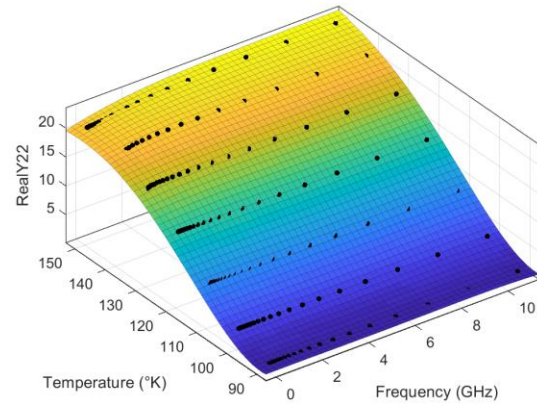
(e) SSE: 0.004584 R-square: 0.9939 Adjusted R-square: 0.9933 RMSE: 0.005743.



(f) SSE: 0.09077 R-square: 0.9998 Adjusted R-square: 0.9998 RMSE: 0.02555.



(g) SSE: 2.308 R-square: 0.9997 Adjusted R-square: 0.9997 RMSE: 0.1289.



(h) SSE: 1.808 R-square: 0.9153 Adjusted R-square: 0.9068 RMSE: 0.1141

FIGURE 11. Proposed Y-parameter models as a function of Temperature and Frequency obtained using 4th order polynomial regression (a). $\text{Im}(Y_{11}(f, \theta))$ (b). $\text{Re}(Y_{11}(f, \theta))$ (c). $\text{Im}(Y_{12}(f, \theta))$ (d). $\text{Re}(Y_{12}(f, \theta))$ (e). $\text{Im}(Y_{21}(f, \theta))$ (f). $\text{Re}(Y_{21}(f, \theta))$ (g). $\text{Im}(Y_{22}(f, \theta))$ (h). $\text{Re}(Y_{22}(f, \theta))$.

regression fit. R-square and adjusted R-square are measures that provide information about the goodness of fit of a model. RMSE is another performance indicator of a regression model. It measures the average difference between values predicted by a model and the actual values. The ECP values obtained using the proposed temperature-and-frequency dependent Y-parameter model are obtained in (31) to (38) as follows:

$$R_{gd} = -\text{Re}\left(\frac{1}{Y_{12}(\theta)}\right) \quad (31)$$

$$R_i = \text{Re}\left(\frac{1}{Y_{11}(\theta)+Y_{12}(\theta)}\right) \quad (32)$$

$$R_{ds} = \frac{1}{\text{Re}(Y_{12}(\theta)+Y_{22}(\theta))} \quad (33)$$

$$C_{gd} = \frac{1}{\omega \text{Im}\left(\frac{1}{Y_{12}(\theta)}\right)} \quad (34)$$

$$C_{gs} = -\frac{1}{\omega \text{Im}\left(\frac{1}{Y_{11}(\theta)+Y_{12}(\theta)}\right)} \quad (35)$$

$$C_{SD} = \frac{\text{Im}(Y_{12}(\theta)+Y_{22}(\theta))}{\omega} \quad (36)$$

$$g_m = \left| \frac{(Y_{21}(\theta)-Y_{12}(\theta))(Y_{11}(\theta)+Y_{12}(\theta))}{\text{Im}(Y_{11}(\theta)+Y_{12}(\theta))} \right| \quad (37)$$

$$\tau = -\frac{\text{Phase}\{(Y_{21}(\theta)-Y_{12}(\theta))[1+j\frac{\text{Re}(Y_{11}(\theta)+Y_{12}(\theta))}{\text{Im}(Y_{11}(\theta)+Y_{12}(\theta))}\}}{\omega} \quad (38)$$

The equation for parameter variation for the specific HEMT designed is as follows,

$$Y_{ij} = p_{00} + p_{10}f + p_{01}\theta + p_{20}f^2 + p_{11}f\theta + p_{02}\theta^2 + p_{30}f^3 + p_{21}f^2\theta + p_{12}f\theta^2 + p_{03}\theta^3 + p_{40}f^4 + p_{31}f^3\theta + p_{22}f^2\theta^2 + p_{13}f\theta^3 + p_{04}\theta^4 \quad (39)$$

where f is the frequency in Hertz, θ is the temperature in degrees kelvin and the coefficients p_{xy} are given in Table 4, Table 5 and Table 6. The coefficients p_{xy} are used to determine the Y parameter equations $\text{Real}(Y_{11})$, $\text{Imag}(Y_{11})$, $\text{Real}(Y_{12})$, $\text{Imag}(Y_{12})$, $\text{Real}(Y_{21})$, $\text{Imag}(Y_{21})$, $\text{Real}(Y_{22})$ and $\text{Imag}(Y_{22})$ as functions of temperature and frequency.

Table 7 demonstrates the variance of ECP values with temperature as determined by the proposed model. The observed trends in R_{GD} , R_i , R_{DS} , C_{GD} , C_{GS} and C_{DS} display a close correspondence to the expected trends, with resistive parameters dropping steadily with a reduction in temperature and capacitive trends displaying varying behavior.

TABLE 4. Coefficient values of p_{00} , p_{10} , p_{01} , p_{20} , p_{11} with 95% confidence bounds.

Parameter/ Coefficient	p_{00}	p_{10}	p_{01}	p_{20}	p_{11}
Real(Y11)	1.40E-04	1.92E-04	7.84E-05	9.30E-05	-8.04E-05
Imag(Y11)	7.72E-02	9.49E-02	6.61E-03	-1.58E-04	8.09E-03
Real(Y12)	-6.26E-05	-2.36E-04	5.07E-04	-7.33E-05	8.10E-04
Imag(Y12)	-5.37E-02	-6.63E-02	1.48E-02	3.42E-05	1.78E-02
Real(Y21)	1.56E+00	1.42E-03	2.24E+00	1.08E-02	-1.52E-02
Imag(Y21)	-5.32E-02	-5.73E-02	-1.60E-02	-1.25E-03	8.71E-03
Real(Y22)	1.33E+01	-3.42E-02	9.67E+00	-1.86E-01	2.47E-01
Imag(Y22)	1.56E-01	1.68E-02	2.84E-01	-4.16E-02	-8.13E-02

TABLE 5. Coefficient values of p_{02} , p_{30} , p_{21} , p_{12} , p_{03} with 95% confidence bounds.

Parameter/ Coefficient	p_{02}	p_{30}	p_{21}	p_{12}	p_{03}
Real(Y11)	2.36E-04	-3.32E-06	-3.93E-06	1.08E-05	1.95E-04
Imag(Y11)	3.94E-03	-8.43E-05	-3.89E-05	1.58E-03	-3.96E-04
Real(Y12)	-2.35E-04	2.91E-05	8.94E-05	5.50E-05	-1.09E-04
Imag(Y12)	-2.12E-03	7.98E-05	-2.02E-04	2.07E-05	-1.95E-03
Real(Y21)	5.81E-01	-7.97E-03	1.12E-02	-9.59E-02	-2.76E-01
Imag(Y21)	-2.42E-02	-2.20E-03	5.56E-03	-1.03E-02	4.32E-03
Real(Y22)	-1.69E+00	1.31E-01	-2.29E-01	2.56E-01	-1.27E+00
Imag(Y22)	3.94E-01	9.38E-02	-1.56E-01	1.87E-01	1.04E-04

TABLE 6. Coefficient values of p_{40} , p_{13} , p_{22} , p_{13} , p_{04} with 95% confidence bounds.

Parameter/ Coefficient	p_{40}	p_{31}	p_{22}	p_{13}	p_{04}
Real(Y11)	8.23E-07	-2.09E-06	1.48E-05	6.77E-06	5.26E-05
Imag(Y11)	7.03E-05	2.48E-05	-5.46E-06	-5.07E-04	-1.12E-03
Real(Y12)	-4.53E-06	2.75E-05	-1.59E-04	-5.17E-05	8.84E-05
Imag(Y12)	-3.57E-05	5.74E-05	-6.59E-05	-2.42E-03	9.36E-04
Real(Y21)	1.51E-03	-2.29E-03	2.16E-03	-7.64E-06	-8.23E-02
Imag(Y21)	4.38E-04	-1.60E-03	3.34E-03	-2.75E-03	6.09E-03
Real(Y22)	-2.32E-02	4.60E-02	-6.08E-02	6.16E-02	3.83E-01
Imag(Y22)	-1.91E-02	4.36E-02	-6.93E-02	6.85E-02	-7.01E-02

TABLE 7. The obtained ECP values using our proposed intrinsic FET model at 350K, 300K, 250K, 200K, 150K and 100K at 1 GHz.

ECP/ Temperature	350K	300K	250K	200K	150K	100K
$R_{GD} (\Omega.mm)$	7.48	5.59	4.15	1.14	0.78	0.57
$R_i (\Omega.mm)$	5.89	4.22	3.76	2.63	1.95	1.11
$R_{DS} (\Omega.mm)$	12.0	10.1	8.72	4.82	2.55	1.26
$C_{GD} (fF/mm)$	10.08	11.09	13.14	23.71	46.93	90.71
$C_{GS} (fF/mm)$	126.6	121.3	113.4	102.9	61.2	2.06
$C_{DS} (fF/mm)$	304.5	299.3	286.6	273.9	201.1	130.5

C. Comparison of estimated ECP values with extracted ECP values

To test the accuracy of the ECP values obtained using the Y parameter model, the ECP values estimated using the Y parameter model at different temperatures have been compared with the actual ECP values extracted using TCAD simulation.

The estimated capacitance ECPs are obtained between 1 GHz and 10 GHz using (24) – (26) for 19 different

frequencies. The simulated capacitance ECPs are obtained by solving drift-diffusion equations and obtaining the corresponding charge and potential profiles to estimate capacitance between the electrodes.

A comparative analysis of the estimated ECP capacitance values with extracted ECP capacitance values at 300 K, 200 K and 100 K are presented in Figs.12(a) to (i). The gate-source capacitance (C_{GS}) and source-drain capacitance (C_{SD}) were observed to drop off at cryogenic temperatures due to the shrinking of the depletion region at the source and drain terminals. The gate-drain capacitance (C_{GD}) on the other hand was found to increase with a decrease in temperature owing to reduced carrier concentration at the gate Schottky contact. With fewer carriers in the channel region, the electrostatic influence of the gate electrode on the carriers becomes more pronounced, leading to an increase in gate-drain capacitance.

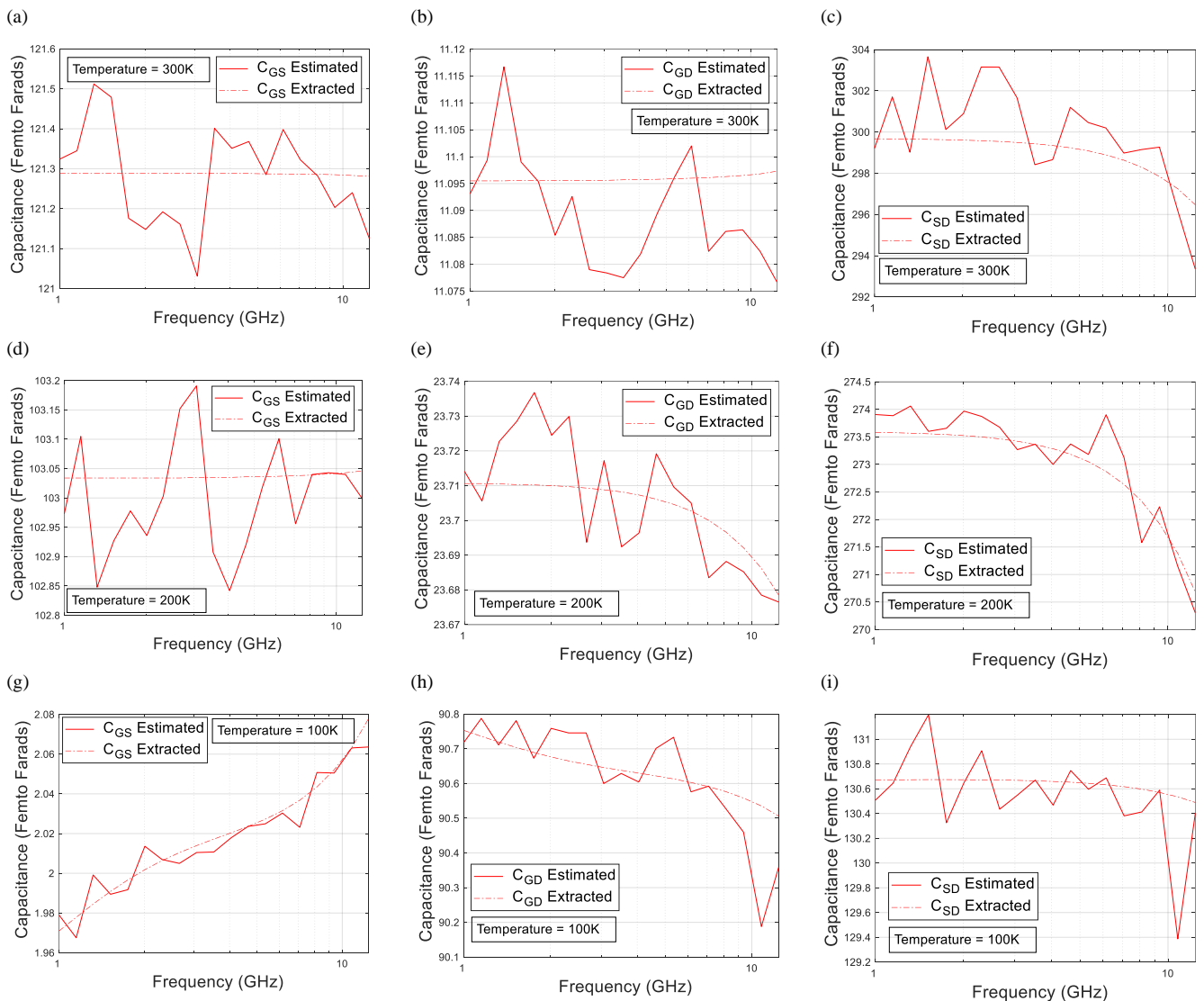


FIGURE 12 (a) Comparison of estimated and extracted C_{GS} at 300 K. (b) Comparison of estimated and extracted C_{GD} at 300 K. (c) Comparison of estimated and extracted C_{SD} at 300 K. (d) Comparison of estimated and extracted C_{GS} at 200 K. (e) Comparison of estimated and extracted C_{GD} at 200 K. (f) Comparison of estimated and extracted C_{SD} at 100 K. (g) Comparison of estimated and extracted C_{GS} at 200 K. (h) Comparison of estimated and extracted C_{GD} at 100 K. (i) Comparison of estimated and extracted C_{SD} at 100 K.

D. Device Interfacing and Circuit Integration

The proposed InP HEMT device and the associated model can be made to interact with other electronic components in an integrated circuit to achieve multiple functions.

The proposed device's fast switching speed and high amplification can be used to realize the switching components S_i and operational amplifiers OP_i . The performance of multimodal generalization and differentiation associative memory circuits proposed in [39] and bionic emotion modules proposed in [40] can be enhanced using the proposed HEMT device. The circuit can be realized using HEMT, which has been shown using a simplified HEMT structure in Fig. 13.

Further, due to the good cryogenic performance of the device, these circuits can be used to realize associative memory and bionic emotion modules in deep-space environments. The proposed InP HEMT can also be integrated into monolithic integrated circuits to realize amplifiers, mixers and multipliers [41] operating in the millimetre wave and early terahertz band range for deep-space applications.

V. FABRICATION PROCESS

InP HEMT devices are commonly fabricated using 3-inch InP wafers. The main processing steps in InP HEMT fabrication are mesa etching, metal contact establishment, passivation and pad metallization. The step-by-step fabrication procedure is explained and shown in Fig. 14.

A. Mesa Etching: Electrical isolation of the HEMT from other devices on the InP wafer is done by wet etching of the InGaAs, InAs and InAlAs layers using a $H_2O_2:H_3PO_4:H_2O$ (1:1:25) solution. The InP etch stop layer is etched separately using a $HCl:H_2O$ (3:2) solution. For forming gate recess structures using wet etching, citric acid/ H_2O_2 [42] or phosphoric acid/ H_2O_2 [43] is used. A substrate temperature of 200 C – 600 C is used in the InP HEMT fabrication process, although lower temperatures within this band are preferred to reduce the possibility of fluorine contamination [42]. Limiting substrate temperature within 250 C and 300 C allows for desirable wet etching of the InP HEMT but also considerably reduces fluorine contamination effects.

B. Source and Drain contact formation: Source and drain contacts of InP HEMTs are typically formed using metal amalgams such as AuGeNi [44], TiMoTiPtAu [45], NiGeAuGeNi [46], TiPtAu [47], NiGeAu/Ge/NiAu [48], NiGeAu [49] and AuGeNiAu [50]. The DC and RF performance of InP HEMTs can be considerably improved upon annealing treatments during contact formation. For InP devices, buried platinum annealing treatment is done in nitrogen-rich environments at a temperature of 250 C – 600

C. The required process time varies between 30 s and 15 mins depending on the dimensions of the device involved [51].

C. Gate contact establishment: Gate electrodes are typically formed using metal amalgamations of Ti, Pt, Au, Ge, Ni and Mo [52]-[53]. The parasitics associated with the gate stem of an InP HEMT are considerably lowered with a gate stem height of over 0.25 μ m. Two step or three step gate recess processes are employed to fabricate InP FETs with gate lengths less than 50 nm. The usage of multiple gate recess steps allows the fabrication of InP HEMTs with gate-channel distances up to 4 nm when compared to conventional gate recess processes. Due to thermal reactions between the gate metal and the semiconductor surface, 'gate sinking' takes place which is a major gate fabrication challenge. An electron beam lithographic process is generally used to recess the gate to a depth beneath the surface of the device. For gate lengths of 30 nm and below, fullerene introduced nano-composite beam fabrication techniques are employed [54].

D. Passivation and Doping: Passivation of InP HEMTs is performed using the plasma enhanced chemical vapor deposition process. Si_3N_4 is mainly used for surface passivation because of its low permittivity. A temperature of less than 300 C is generally used to passivate Si_3N_4 . Passivation using low permittivity materials can be used to reduce parasitic capacitance but also worsens the cut-off frequency of the device. Doping within an InP device can be performed using four different doping procedures. Single side Si-planar doping [55] and single side Si- δ -doping [56] is typically used above the channel region, double side Si-planar-doping [57] is used below the channel region and double-sided Si- δ -doping [45] can be used both above and below the channel region.

Double sided doping techniques can minimize the effects of impact ionization within the channel and consequently minimize kink effects observed in the output characteristics. The epitaxial growth process of a δ -doped structure such as that in the proposed HEMT devices differs from standard growth procedures. The creation of a δ -doped layer requires a lower substrate temperature in order to reduce surface segregation reactions of silicon atoms in the InAlAs layer.

E. Pad metallization: The passivation layer is first removed in the pad metallization regions using Si_3N_4 by reactive ion etching or using aluminium oxide. The pad metal stack is subsequently deposited by electron beam evaporation.

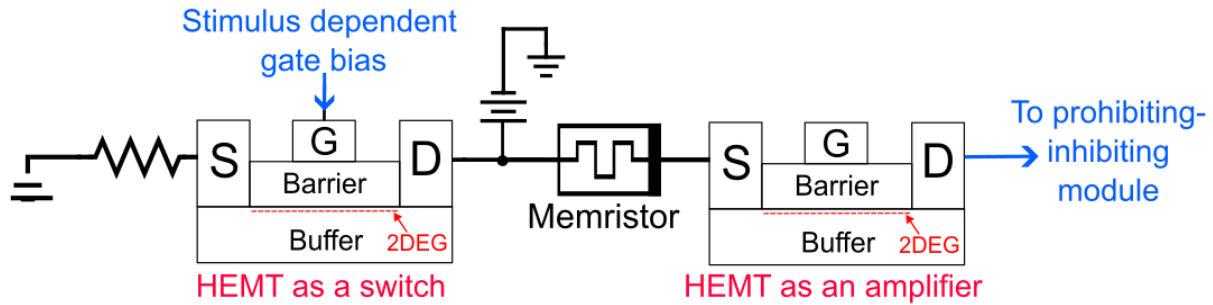


FIGURE 13. Integration of the proposed HEMT device in the logical judgement module of a bionic emotion module.

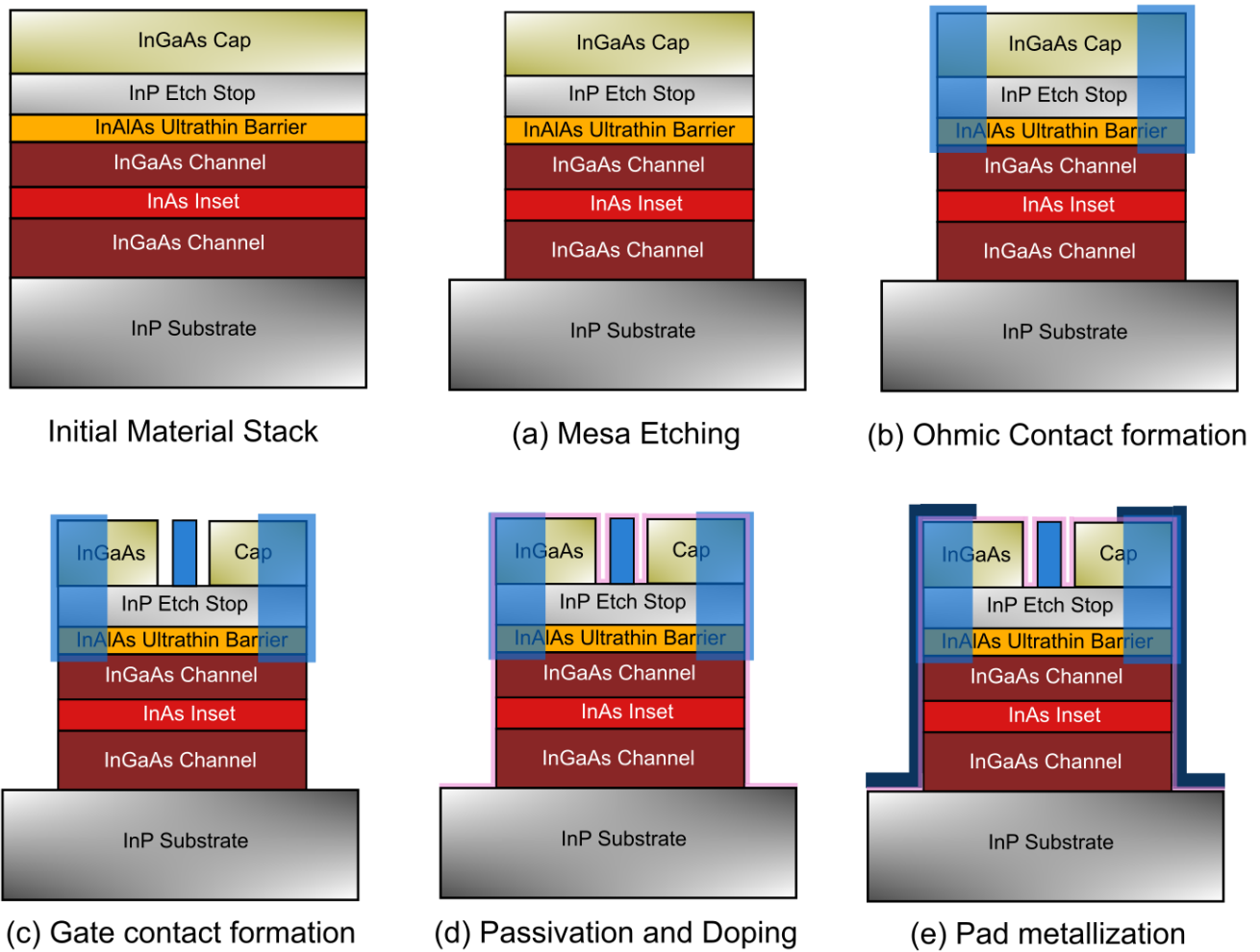


FIGURE 14. Step-by-step fabrication procedure of the proposed InP HEMT (a) Mesa Etching (b) Ohmic contact formation (c) Gate contact formation (d) Passivation and doping, and (e) Pad metallization.

VI. CONCLUSION

In our work, we have designed a novel metamorphic InP HEMT for cryogenic applications which exhibits f_T/f_{MAX} figures of 247.2 GHz/ 526.0 GHz at 298 K, 168 GHz/ 152 GHz at 150 K and 5.02 GHz/ 10.01 GHz at 90 K. We subsequently proposed a small signal model which accurately predicts ECPs within 0.1% of the empirically extracted ECPs. The unique structural topology and material selection in our work was presented and justified with the performance incentives of each design decision

such as the ultrathin barrier layer and composite channel explicitly explained. This device was designed in response to address the acute demand for devices with high f_T/f_{MAX} , and favorable noise characteristics across a wide temperature range in the context of deep-space and cryogenic applications. The performance characteristics of the proposed device indicate that is well suited for LNA, sensors and detectors, radio astronomy, quantum computers and other cryogenic RF applications.

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