WARWICK
THE UNIVERSITY OF WARWICK

Benchmarking the Robustness performance of SiC cascode JFETS against contemporary devices using simulations and experimental measurements

by

Sunday Nereus Akor Agbo

A thesis submitted in partial fulfilment of the requirements for the degree of
Doctor of Philosophy in Engineering

University of Warwick, School of Engineering
January 2023

Table of Contents

Acknowledgements

First, I would like to thank my supervisor Olayiwola Alatise for his immense patience and support throughout my thesis. Also, many thanks to my second supervisor Jose Ortiz-Gonzalez for helping me with a fresh perspective in times of doubt. You both believed in me and provided invaluable guidance over the course of my research. Thanks for believing in me.

I would also like to acknowledge the support from everybody in the Power Electronics Applications and Technology in Energy Research (PEATER) group. Everyone was always approachable, and ready to help and collaborate which made my research a lot easier. To Simon Mendy, Robert Wu, Erfan Bashar, Guy Baker, Benjamin Renz, Kyrylo Melnyk, and Nikolaos Iosifidis, I am very appreciative of your expertise, input, and friendship as well.

I am immensely thankful to my parents and siblings for their support, love, and understanding through the whole process. Finally, I would like to thank Jenifer, Douglas, Henry, Sylvia, Will, Linda, and Nazia, you all always made it a priority to check on me throughout the stressful period of my research.

Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has not been submitted for a degree at any other University. All the work described in this thesis was carried out by the author or under his direction except where specifically stated.

Parts of this thesis have been published by the author during the period of study in the school of Engineering at the University of Warwick from February 2019 until December 2022. They are given in full detail in the Publication List section.

Sunday N. A. Agbo

January 2023

List of Published Work

I. S. N. Agbo, J. Ortiz-Gonzalez, R. Wu, and O. Alatise, "Characterisation of Unclamped Inductive Switching in SiC Cascode JFETs," in The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020), 2021-01-01 2021: Institution of Engineering and Technology, doi: 10.1049/icp.2021.1114.

II. S. N. Agbo, J. Ortiz-Gonzalez, and O. Alatise, "Performance of SiC cascode JFETs under single and repetitive avalanche pulses," Microelectronics Reliability, vol. 110, p. 113644, 2020, doi: 10.1016/j.microrel.2020.113644.

III. S. N. Agbo, J. Ortiz Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "UIS performance and ruggedness of stand-alone and cascode SiC JFETs," Microelectronics Reliability, vol. 114, p. 113803, 2020/11/01/ 2020, doi: https://doi.org/10.1016/j.microrel.2020.113803.

IV. S. N. Agbo, E. Bashar, R. Wu, S. Mendy, J. O. Gonzalez, and O. Alatise, "Simulations and Measurements of Failure Modes in SiC Cascode JFETs under Short Circuit Conditions," in 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), 2021-11-02 2021: IEEE, doi: 10.1109/compel52922.2021.9646031.

V. J. Ortiz Gonzalez, R. Wu, S. N. Agbo, and O. Alatise, "Robustness and reliability review of Si and SiC FET devices for more-electric-aircraft applications," Microelectronics Reliability, vol. 100-101, p. 113324, 2019/09/01/ 2019, doi: https://doi.org/10.1016/j.microrel.2019.06.016.

VI. E. Bashar et al., "Comparison of Short Circuit Failure Modes in SiC Planar MOSFETs, SiC Trench MOSFETs and SiC Cascode JFETs," in 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2021-11-07 2021: IEEE, doi: 10.1109/wipda49284.2021.9645092.

VII. R. Wu et al., "Measurement and simulation of short circuit current sharing under parallel connection: SiC MOSFETs and SiC Cascode JFETs," Microelectronics Reliability, p. 114271, 2021-10-01 2021, doi: 10.1016/j.microrel.2021.114271.

VIII. R. Wu, S. Mendy, N. Agbo, J. O. Gonzalez, S. Jahdi, and O. Alatise, "Performance of Parallel Connected SiC MOSFETs under Short Circuits Conditions," Energies, vol. 14, no. 20, p. 6834, 2021-10-19 2021, doi: 10.3390/en14206834.

IX. E. Bashar et al., "A Review of Short Circuit Performance in 650 V Power Devices: SiC MOSFETs, Silicon Super-junction MOSFETs, SiC Cascode JFETs, Silicon MOSFETs and Silicon IGBTs," in PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 10-12 May 2022 2022, pp. 1-8, doi: 10.30420/565822162.

X. O. Alatise et al., "A Comparison of the Short Circuit Performance of 650 V SiC Planar MOSFETs, Trench MOSFETs and Cascode JFETs," IET Conference Proceedings, pp. 335-339

XI. J. Ortiz Gonzalez, A. Deb, E. Bashar, S. N. Agbo, S. Jahdi, and O. Alatise, "Benchmarking the robustness of Si and SiC MOSFETs: Unclamped inductive switching and short-circuit performance," Microelectronics Reliability, vol. 138, p. 114719, 2022/11/01/ 2022, doi: https://doi.org/10.1016/j.microrel.2022.114719.

XII. S. Mendy, N. S. Agbo, J. O. Gonzalez, and O. Alatise, "Influence of the SiC JFET Gate Impedance on the Off-State Voltage Balance in Cascode Configuration," in 2022 IEEE Workshop on Wide Bandgap Power Devices and Applications in Europe (WiPDA Europe), 18-20 Sept. 2022 2022, pp. 1-6, doi: 10.1109/WiPDAEurope55971.2022.9936268.

Abstract

This thesis provides the first comprehensive benchmarking exercise of SiC Cascode JFETs against similarly rated SiC Planar MOSFETs, Trench MOSFETs and other devices. Experimental measurements of short circuits in single and parallel devices, single and repetitive unclamped inductive switching as well as double pulse tests are used together with finite element simulations throughout the thesis. Power device robustness measures how well a device can sustain shocks during anomalous operation. These operating conditions are high voltages that exceed the device breakdown (avalanche conduction), or simultaneous high current and voltage through the device (Short circuit conduction). The silicon Carbide (SiC) cascode JFET is an electronic switch that combines two power devices, a low voltage silicon (Si) MOSFET and a high voltage SiC JFET operating as a single switch. This configuration avoids the challenges of reduced gate oxide reliability in SiC MOSFETs, and negative turn-on Voltage for JFETs. However, the robustness of SiC cascode JFETs have not been examined as extensively as conventional devices. Hence, this thesis investigates the robustness of SiC cascode JFETs as well as the failure modes during such operation and benchmarks the performance against conventional devices.

Analysis of avalanche robustness in SiC Cascode JFETs indicated a peculiar style of failure at high temperatures characterised by a soft failure (delayed turn-off, change of current slope, and dip in voltage), and an eventual catastrophic failure. This failure is different from other devices analysed which demonstrated a single catastrophic failure. The results show that the gate resistance of the SiC JFET plays a crucial role during avalanche mode conduction. Finite element simulations confirm this observation.

The Short circuit (SC) robustness analysis of the SiC Cascode JFET demonstrated invariability with temperature. In contrast, benchmarked devices show a SC correlation with temperature. The short circuit operation also revealed the Cascode JFET fails with a drain-source short while the gate-source junction is still functional. Also revealed is the crucial role of increasing JFET gate resistance in reducing short circuit robustness. The SC robustness is also analysed for parallel connected devices. The analysis demonstrates the parameters with the largest impact on SC current shared between paralleled devices. Variation in the embedded JFET gate resistance within the cascode JFET presents with the highest impact as confirmed by finite element simulation, while interface charges and the doping of the CSL region present with the largest impact in SiC MOSFETs.

Abbreviations

C_{GS} – Gate-drain capacitance

C_{DS} – Drain-source capacitance

C_{GS} – Gate-source capacitance

DC – Direct current

D_{it} – Density of interface states

D_n, D_p – Diffusion coefficients

DUT – Device under test

E – Electric Field

E_{max} – Maximum electric field

E_C, E_V – Conduction, Valence band energy

E_{AV} – Avalanche energy

E_{SC} – Short circuit energy

E_G – Energy bandgap

ε_s – Dielectric constant

GaN – Gallium Nitride

I_{AV} – Avalanche current

I_D – Drain current

I_{GS} – Gate source current

I_L – Load current

I_{SC} – Short circuit current

J – Total current density

J_n, J_p – Electron, Hole current density

k – Boltzmann's constant

L_{DC} – DC source parasitic inductance

L_D – Drain parasitic Inductance

L_S – Source parasitic inductance

κ – Thermal Conductivity

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

n, p – Electron, Hole density

n_i – Intrinsic carrier concentration

N_C, N_V – Conduction, Valence density of states

q – Electronic charge

R_{Drift} – Drift Resistance

$R_{DS(ON)}$ – Drain to source on-state resistance

R_G – Gate resistance

R_{GS} – Gate-source resistance

$R_{G,JFET}$ – JFET gate resistance(Cascode structure)

R_{ON} – On-state resistance

$R_{ON,sp}$ – Specific on-state resistance

R_{th} – Thermal Resistance

Si – Silicon

SiC – Silicon Carbide

SCSOA – Short circuit safe operating area

SCWT – Short circuit withstand time

SOA – Safe operating area

t_{AV} – Time in avalanche

T_{CASE} – Case temperature

T_J – Junction temperature

$T_{J(max)}$ – Maximum junction temperature

t_{ON} – ON time

t_{PULSE} – Pulse width time

t_{SC} – Short circuit withstand time

TCAD – Technology computer-aided design

μ - Carrier mobility

μ_n – Electron mobility

μ_p – Hole mobility

UIS – Unclamped Inductive Switching

V – Electrostatic potential

$V_{BR(DSS)}$ – Manufacturer's rated breakdown voltage

v_{sat} – Saturation drift velocity

V_{DD} – Input voltage

V_{DS} – Drain-source voltage

$V_{GS(th)}$, V_{th} – Threshold voltage

V_{GS} – Gate-source voltage

WBG – Wide bandgap

ZTC – Zero temperature coefficient

List of Figures

List of Tables

Chapter 1. Introduction

1.1. Background

Over the past decade there has been a steady increase in the demand for Wide bandgap (WBG) power electronic devices. These are electronic devices made from semiconductors with a relatively wider bandgap than silicon (Si), e.g., Silicon Carbide (SiC), Gallium Nitride (GaN), Diamond etc. This increase in demand is directly corelated to a coordinated effort at tackling the issue of global warming i.e., reduce global emissions of greenhouse gasses and achieve net zero emissions. Within the UK, the energy supply sector is one of the major contributing sectors to the total amount of emissions.

The UK's department for Business, Energy & Industrial Strategy estimated a total of 23.6% of the total CO_2 emissions within the country in 2021 was from the supply of energy. With the increasing demand in energy consumption, the emission from this sector can be improved by switching fuel sources, developing more efficient energy solutions, and behavioural changes. Currently, renewable energy sources accounts for 39.7% of the total energy generated in the UK. Efficient solutions that reduce waste of energy through the transmission, conversion, consumption on the demand side is also highly desirable [1].

Another key sector contributing heavily to the global emissions is transport. This includes emissions from road transport, aviation, railways, and shipping etc . In 2021, the transport sector accounted for an estimated 31.5% of CO_2 emissions within the UK which is the highest among the various sectors. To mitigate the emissions from this sector, there has been an increase in the demand for electric vehicles (EV) and various charging infrastructure, electric trains, and other renewable powered transport alternatives. Sales of EVs accounted for 5.6% of the total auto market in 2022 with a projected exponential increase in demand over the coming years [2]. At the end of November 2022, the number of EV charging point are reported to be 36752 across the UK. This is a 33% rise from the amount of charging stations in November 2021 [3].

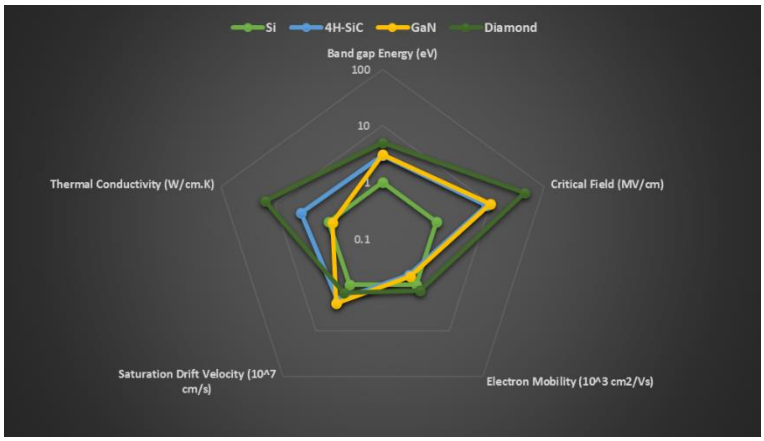


Figure 1.1 Semiconductor material properties

The increase in the demand for WBG devices is because possess superior material properties. Figure 1.1 shows the superiority of WBG semiconductor materials properties. This means they can withstand higher operational temperatures, switching frequencies, power densities, and breakdown voltages than their Si counterparts. These superior properties also mean lower switching and conduction losses which lead to improved efficiency in the system. All these superior metrics translate into decreased weight, size, and space taken up by power electronic systems (i.e., converter, magnetics, heatsinks, passive components etc).

Consequently, there has been an increased need for more robust and reliable WBG devices. The processing and fabrication of WBG devices compared to traditionally deployed Si based power electronics are still far from mature and hence require more research into new methods and standards for accessing and qualifying their robustness and reliability.

Over the last couple of years, SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have seen the most improvement among all the WBG power devices. As such, the robustness and reliability of SiC MOSFETs has seen a lot of research, improvement, and standardisation. One of the main reliability concerns of SiC MOSFETs is the poor quality oxide interface. GaN High Electron Mobility Transistors (HEMTs) have also been explored recently for applications requiring high switching frequencies. These GaN devices are relatively more expensive to fabricate and are not suitable for high density applications because of their lateral structures. SiC Junction Field Effect Transistors (JFETs) garnered a lot of interest at the onset of WBG research and development but was later abandoned due to the negative voltage required to turn-on the devices (Depletion Mode device), as well as the improvements in SiC MOSFETs. Recently there has been a resurgence in the adoption of SiC JFETs because of the realisation of an improved structure design. The current structure is a completely vertical single channel device in contrast to old 2-channel JFETs. Also, its implementation in certain applications like Solid Sate circuit breakers (SSCB), and the

Cascode Circuit. The Cascode circuit converts the JFET from negative voltage device (depletion mode) to a positive voltage (enhancement mode). There have been various studies into the switching and operation of the SiC Cascode JFET while demonstrating its superior or comparable performance to SiC MOSFETs, Si IGBT, Si Superjuction structures as demonstrated in the second chapter of the thesis and previous studies [4]. However, there is still very limited research into the robustness of this device constraining the widespread adoption.

Robustness in this context is the resilience of power device against single event and/or anomalous conditions like cosmic-ray incidents, short-circuits and robustness under avalanche conduction. Studying the robustness is important for determining the ability of power devices to withstand electrothermal stress and subsequently it is used to define the device operating limits. This thesis focusses on the latter two robustness metrics. Robustness under avalanche conduction is analysed by unclamped inductive switching (UIS). Applications that require high switching frequencies with inductive loads such as motor drive applications require power devices with good avalanche robustness. Also, a short circuit withstand time (SCWT) long enough for the short circuit fault detection to activate is required for power devices in all power systems.

1.2. Aims and Objectives

This work aims to evaluate the robustness concerns preventing the adoption of the SiC cascode JFET as a viable alternative for WBG power system applications. This thesis will be focused on using experimental measurements and finite element analysis (FEA) models to comprehensively investigate and analyse the robustness performance and possible failure mechanisms of the SiC Cascode JFET. Also, the results and performance are benchmarked against other power device technologies with similar rating. In particular:

1. Accurate High Voltage SiC JFET and LV Si MOSFET FEA models for use in analysing the device physics were developed.
2. The complete operation of the SiC cascode JFET is described.
3. The avalanche ruggedness of the SiC Cascode JFET, stand-alone SiC JFET, and SiC Trench MOSFET are compared. The effects of gate voltage and avalanche current are assessed. Also analysed is the failure using FEA simulations, and the performance under repetitive avalanche pulses.
4. Analysis of the influence of circuit and device parasitic parameters on short circuit robustness of Single SiC cascode JFETs. Same is done for Trench and Planar SiC MOSFETs. FEA simulations are also performed to analyse the devices.

5. Analysis of the short circuit robustness of parallel connected SiC cascode JFETs as well as SiC Planar and Trench MOSFETs for comparison. The impact of circuit and device parasitic parameters is investigated for all three technologies.

This work focuses specifically on cascode devices with blocking voltages between 600 V and 1200 V which can find use in applications such as, electric vehicles, power supplies, and solar inverters.

1.3. Key Contributions

The contributions of this thesis can be highlighted as follows,

Improved understanding of failure modes in SiC Cascode JFETs under Unclamped Inductive Switching: In this thesis section, the avalanche ruggedness of SiC Cascode JFETs is investigated alongside similarly rated SiC Planar MOSFETs, Trench MOSFETs, silicon super-junction MOSFETs and silicon MOSFETs. An unclamped inductive switching test rig was used to increase the avalanche current until failure was observed. This was done with different initial junction temperatures. While the MOSFETs failed in the conventional mode with a rise in the avalanche current and sudden drop in the drain-source voltage (indicating a short circuit), the Cascode JFET failed without a sudden short circuit. Interestingly, it appeared as though the peak avalanche current and energy of the Cascode JFET increased with initial junction temperature because the device survived relatively much larger avalanche currents without catastrophic failure. The voltage waveforms of the Cascode showed an anomalous and prolonged dip during avalanche. Subsequent failure analysis on the Cascode JFET showed that the low voltage silicon MOSFET was still operational and capable of voltage blocking with an oxide that retained its insulating properties while the JFET was shorted. Finite element models of Cascode JFETs in avalanche later showed that increased gate leakage of the JFET PN junction gate during avalanche caused a JFET gate-drain short with the LV MOSFET bypassed. This caused the Cascode JFET to go into linear mode during avalanche as indicated by the anomalous drain voltage behaviour. The results of this study were presented in the European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) 2020 and published as a journal paper in microelectronics reliability.

Improved Understanding of failure modes in SiC Cascode JFETs under Short Circuits: In this thesis section, SiC Cascode JFETs were benchmarked against SiC MOSFETs in terms of short circuit withstand time. 650 V SiC Planar MOSFETs, Trench MOSFETs, Cascode JFETs, Silicon SJ MOSFETs and silicon MOSFETs were tested at 400 V drain source voltage (60% of rated voltage) at 25C, 75C and 150C. The short circuit duration was increased until the devices

failed. The results showed the SiC Cascode JFETs exhibited reduced short circuit withstand time (SCWT) compared to the SiC Trench MOSFETs and the silicon devices. The SCWT in Cascode JFETs was largely temperature invariant. SiC Cascode JFETs were observed to fail in drain-source shorts with gate-source terminals still functional and capable of blocking the rated gate voltage. The SiC MOSFETs that were tested alongside the cascode JFETs in the same short circuit test rig showed a different failure mode. The failure of the SiC MOSFETs was a gate oxide failure with the drain source still capable of blocking voltages. The Cascode JFET was able to avoid this failure mode for two reasons (i) the gate oxide is that of a low voltage (LV) silicon MOSFET and is therefore more reliable with lower fixed oxide and interface trap charges and (ii) the short circuit current bypassed the LV silicon MOSFET and instead flowed through the JFET gate thereby resulting in a gate-drain short of the JFET. The results of this study were presented in the Workshop on Control and Modelling for Power Electronics (COMPEL) 2021.

Short circuit performance of parallel connected SIC JFETs: In this section of the thesis, key device and circuit parameters that influence current sharing during short circuit conduction between parallel connected 1200 V rated SiC cascode JFETs were studied and contrasted with similar studies for Trench, and Planar SiC MOSFETs of the same voltage rating. The analysis was done at 400 V (33% of rated voltage) which is much lower than the device rated voltage to remove the risk of failure, while varying threshold Voltage, gate voltage, gate resistance, case temperature, and parasitic inductance (simulation only) between parallel devices. The current shared between parallel cascode JFETs was not affected by a spread in threshold voltages. Conversely, the tests showed significant disparity in the current shared between parallel SiC MOSFETs due to a variation in threshold voltage. Finite element models of SiC MOSFETs showed that the density of interface charges, and the current spreading layer (CSL) doping which cause a spread in the threshold voltage were the most important factors impacting the performance of parallel connected devices during short circuit conduction. The parasitic resistance within the JFET gate loop greatly influenced the short circuit current shared by parallel cascode JFETs as demonstrated by finite element analysis of cascode JFETs. Results from this study were presented in the European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) 2021.

1.4. Thesis Outline

This thesis comprises of 6 chapters in total. The first is a general introduction to the research topic and the research aims and objectives.

Chapter 2, this Chapter introduced the cascode power device with a summary of the various cascode topologies. A Finite Element Analysis (FEA) modelling overview is also presented with considerations for modelling a power device cell. Next, a description of the various steps taken to model the SiC cascode JFET in this work is detailed with Static characteristics and transient Switching results from the model compared to typical experimental results. The chapter concludes with an analysis of the JFET cascode switching transient.

Chapter 3 presented an extensive review of the literature and the theory guiding the behaviour of devices during unclamped inductive switching (UIS). Next, the failure modes and peculiarities of SiC Cascode JFETs under single and repetitive UIS pulses are characterised and benchmarked against other SIC power devices of similar power ratings. The FEA model developed in chapter 2 is used to investigate the failure behaviour of the various devices during UIS with the results and conclusions also presented.

Chapter 4, This chapter evaluates the performance of commercially available SiC Cascode JFETs under short circuit conditions in comparison with comparatively rated silicon and SiC power devices. Hence, Short circuit measurements are performed on SiC Cascode JFETs, SiC Planar MOSFETs, SiC Trench MOSFETs, silicon MOSFETs, silicon super-junction MOSFETs. FEA simulations are used to understand the failure modes of SiC Cascode JFETs under short circuit conditions.

Chapter 5, here the short circuit performance of parallel connected devices with various parameter variations are presented. The investigations were done experimentally for SiC Planar, Trench MOSFETs and SiC Cascode JFETs, subsequently FEA mixed mode simulations (SILVACO) were used to investigate the short circuit physics respectively whilst exploring the effects of parameter variation on parallel short circuit performance.

Chapter 6 concludes the thesis with recommendation for further research provided.

References

[1] (2022). *UK ENERGY IN BRIEF*. [Online] Available: https://assets.publishing.service.gov.uk/government/uploads/system/uploads/attachment_data/file/1094025/UK_Energy_in_Brief_2022.pdf

[2] IEA, "Global EV Outlook 2022," 2022. [Online]. Available: https://www.iea.org/reports/global-ev-outlook-2022

[3] Zap-Map. "EV Charging Statistics 2022." https://www.zap-map.com/statistics/ (accessed.

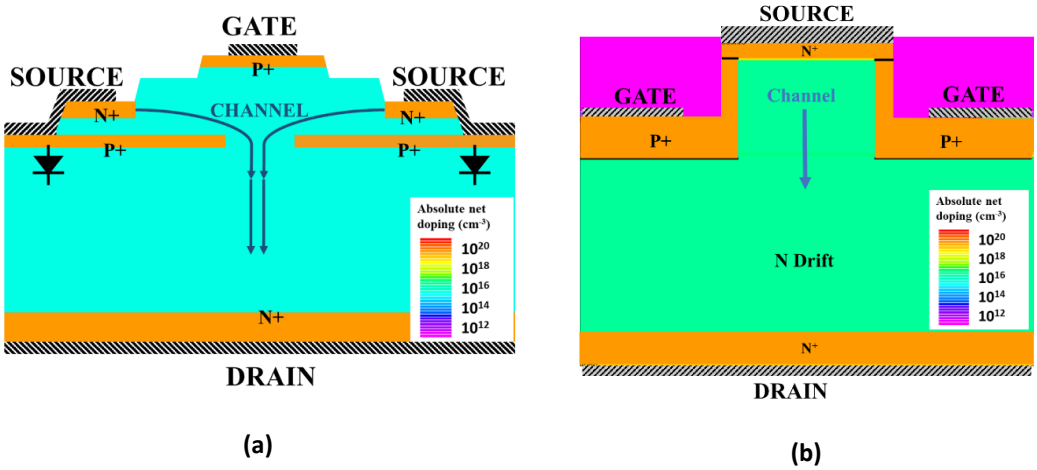
[4] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," *IEEE Transactions on Industrial Electronics,* vol. 67, no. 9, pp. 7375-7385, 2020, doi: 10.1109/TIE.2019.2945299.

Chapter 2. SiC Cascode JFET Modelling

2.1. Introduction to Cascode

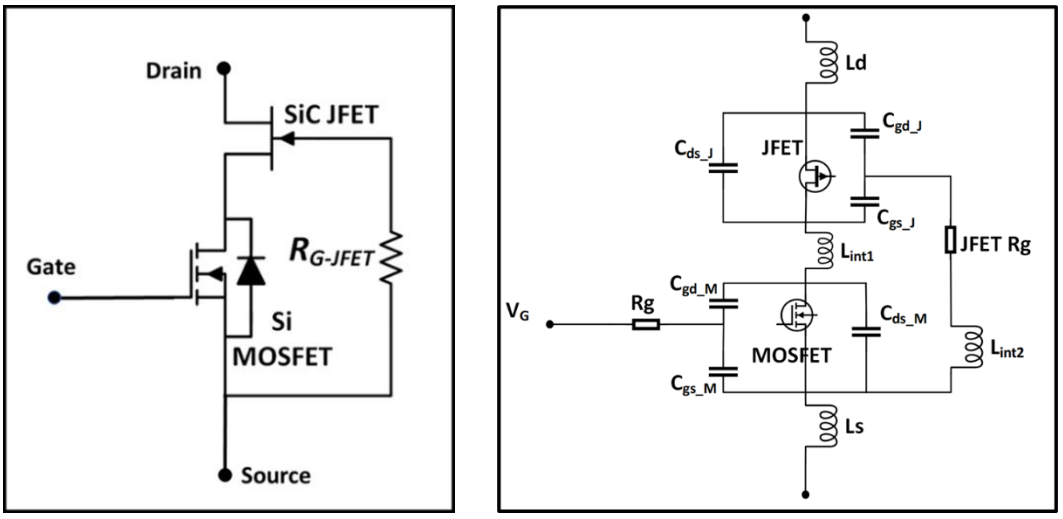
The Cascode device configuration is a promising device technology that combines the gate oxide reliability of silicon MOSFETs with the fast switching properties of SiC MOSFETs [1, 2]. The cascode is formed by connecting a low voltage (LV) silicon MOSFET between the gate-source terminals of a High Voltage (HV) power device. This is achieved using normally-on WBG devices (e.g., GaN HEMT, SiC JFET), so that the normally-on operation of the device is converted into normally-off operation. For this configuration to be achieved, the LV MOSFET breakdown voltage must be larger than the magnitude of the HV device pinch-off voltage.

This thesis is focused on the Cascode configuration with the SiC JFET as the HV device. There are two types of stand-alone SiC JFET structures. Figure 2.1 shows both device structures. The 2-channel SiC JFET pictured in Figure 2.1(a) was previously manufactured by SiCED[3-5]. It was the favoured structure in SiC JFET applications until recently with the fabrication of the vertical channel JFET by UnitedSiC pictured in Figure 2.1(b)[6, 7]. The 2-channel JFET was previously preferred in power electronic applications because it possessed a parasitic body diode, however the channel resistance is much larger leading to higher on-state resistance. Alternatively, the vertical channel JFET does not possess a parasitic body diode and uses its Gate-Drain PN junction for blocking voltage. However, it has a much lower channel resistance and is easier to fabricate (it does not have a buried P+ region). The vertical channel JFET can be designed as a normally-on and normally-off device, while the horizontal channel JFET can only be normally-on. Figure 2.2 shows the internal configuration of the SiC JFET cascode structure including the internal parasitic, while Figure 2.3 shows the two possible packaging configurations used for the SiC Cascode JFET. The side by side cascode package pictured in Figure 2.3(a) employs a bond wire for connecting the source of the HV SiC JFET to the drain of the LV Si MOSFET, while the stack configuration shown in Figure 2.3(b) directly bonds the drain of the LV MOSFET to the Source pad of the HV SiC JFET using solder paste. The stack configuration eradicates L_{int1}: the parasitic inductance between LV MOSFET drain and HV JFET source pictured in Figure 2.2(b). However, it couples the thermal performance of both devices together which is not ideal.



(a) (b)

Figure 2.1 Cell structure of (a) 2-channel JFET (b) Vertical channel JFET



(a) (b)

Figure 2.2 (a) Simple Internal structure of the SiC Cascode JFET (b) Internal structure with the various parasitic.

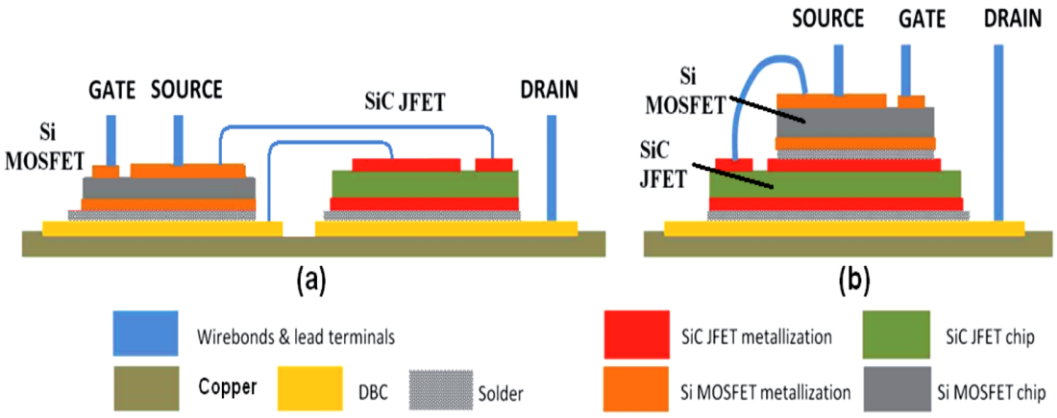


Figure 2.3 (a) Side-by-side co-package configuration, and (b) stack configuration of the SiC Cascode device replicated from [8]

Another device that utilises the cascode configuration is the GaN High electron mobility transistor (HEMT). Figure 2.4 shows the structure of the GaN HEMT. The GaN HEMT is a lateral heterojunction structure which conducts current by means of a lateral channel called the two-dimension electron gas (2DEG). This channel is formed at the interface between the AlGaN barrier and GaN layer as shown in Figure 2.4. The GaN HEMT is very attractive for high frequency operation because of the high switching speed and high mobility of the channel but is limited in high voltage applications. This is a constraint resulting from increasing the gate-drain lateral distance responsible for blocking voltage. An increase in the distance leads to substantial increase in the on-state resistance[9].

The material properties and consequently the expected performance of GaN devices has been touted to be superior to SiC is most applications. Table 2-1 shows the material properties of GaN and SiC with various key material metrics. GaN can withstand approximately 1.4x the critical electric field of SiC, which should allow it to operate at higher voltages with lower leakage currents. Also, GaN is better suited for High frequency operations. SiC is only superior to GaN with respect to thermal conductivity and melting point which makes it better suited to high temperature applications.

However, vertical structures are more easily realised with SiC in comparison to GaN. For vertical structures, the trade-off between increased voltage and device on-state resistance is greatly reduced. This makes SiC cascode JFETs and other SiC vertical structures preferable to GaN structures for high voltage and power dense applications. It is worth mentioning that a Vertical GaN fin JFET with a GaN substrate capable of blocking 650-1200 V has recently become available from NexGen Power Systems [10-15]. The device has shown good switching and robustness performances. It is however still curtailed by the availability and cost of GaN substrates in comparison to SiC and Si. Currently 200 mm SiC wafers are available in comparison to GaN (100mm).

Another key bottleneck of GaN is the maturity of the fabrication process. GaN deposition is typically achieved through the MOCVD epitaxy process on lattice-mismatched carriers such as silicon, SiC, diamond, or sapphire (heteroepitaxy). This triggers film stress and crystal imperfections, which predominantly leads to device instabilities and occasionally to catastrophic failures[16-18].The lattice mismatch in GaN structures grown by heteroepitaxy is therefore undesirable. In contrast, SiC structures can be grown on SiC substrates (homoepitaxy) resulting in more reliable power devices. Recent studies of the amount of crystal imperfections (defect densities) in SiC report approximately 10^3 cm^{-2}, while reports for GaN indicate 10^3-10^5 cm^{-2} for GaN-on-GaN structures, and 10^8-10^9 cm^{-2} for heteroepitaxial GaN [15].

Table 2-1. Comparison of SiC and GaN material properties

Material property	4H-SiC[19]	GaN[20]
Band gap Energy, E_g (eV)	3.26	3.39
Critical Field, E_C (MV/cm) ⊥c, ‖c	2.2,2.5	3.0
Electron Mobility, μ_n (cm^2/Vs) ⊥c,‖c	1000,1200	1000
Hole Mobility, μ_p (cm^2/Vs)	120	850
Relative Dielectric Constant (ε_r) ⊥c, ‖c	9.76,10.32	9.0
Intrinsic Carrier Concentration, (n_i)	5.0×10^{-9}	1.6×10^{-10}
Saturation Drift Velocity, V_{sat} (cm/s)	2.2×10^7	2.5×10^7
Thermal Conductivity, λ_{th} (W/cm.K)	4.9	2.3
Melting Point (K)	3100	2773

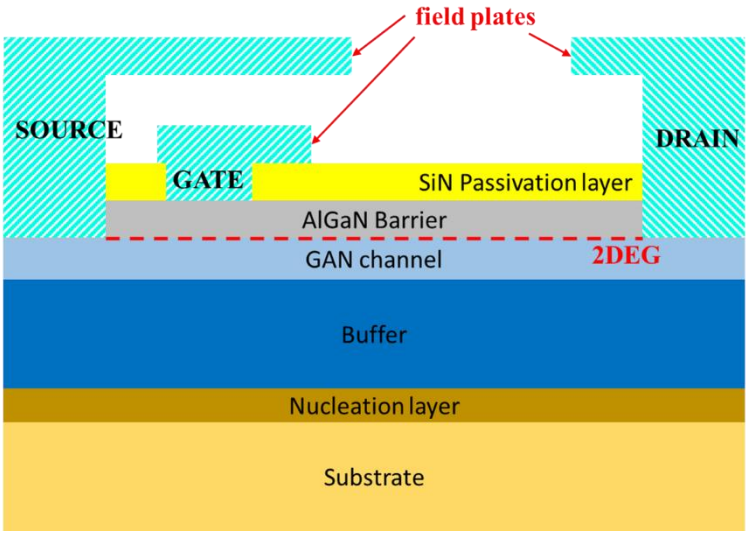


Figure 2.4 Cell structure of a GaN HEMT (Not drawn to scale)

Studies of robustness in GaN HEMTs have shown these devices possess no avalanche robustness [21-31], and have very poor short circuit robustness when compared to other Si and SiC power devices[32-36]. Unclamped inductive switching (UIS) tests of stand-alone GaN HEMTs showed they dissipate very minimal energy. Also, the devices were shown to withstand the surge energy through capacitive charging[23]. The devices failed when the peak resonant VDS is equal to the device's dynamic breakdown voltage coupled with very low peak currents. The dynamic breakdown voltage for each device is characteristically larger than its static breakdown voltage and varies with changes in resonance duration. Failure analysis of GaN HEMTs after failure in UIS were attributed to high electric fields. A correlation is demonstrated between failure spots from SEM imaging and peak electric fields from FEA

analysis. Cascode GaN HEMTS in UIS have also been extensively studied showing distinct differences compared to stand-alone GaN HEMTs[37, 38]. The dynamic breakdown voltage in this case is lower than its static breakdown voltage, and the UIS characteristics indicate two different failure modes. The first is a cascode GaN HEMT drain to source short with the Si MOSFET still operational indicating a GaN HEMT gate to drain short. In the second mode, UIS test of the DUTs after failure show the cascode GaN HEMT functions as a standalone Si MOSFET with an avalanche voltage equal to the MOSFET breakdown voltage (~35 V). This indicates a GaN HEMT drain to source short coupled with the gate to drain in an open circuit. Failure analysis indicate failure is due to buffer trapping in the GaN HEMT.

Analysis of 650 V GaN HEMTs under short circuit stress show excellent short circuit robustness for bus voltages up to 300 V (0.46 times the device breakdown voltage) and a gate voltage at the recommended maximum drive voltage. Short circuit withstand time (SCWT) greater than 10 µs were recorded. Above 300 V, the short circuit robustness reduces drastically with typical SCWT less than 1µs[34]. These two styles of failure at low voltage and high voltage after analysis show failure spots at different areas of the chip. Hence, there are two distinct causes of failure during short circuit. First, the failure at low voltage is cause by the melting of metals at high temperatures in wide areas of the chip close to external contact. Conversely, the failure at high voltage is attributed to a localised hot spot below the source field plate at the edge of the gate field plate where the power density and the temperature exceed the GaN/AlGaN failure limit[36].

2.2. Performance and advantages of SiC Cascode JFETs

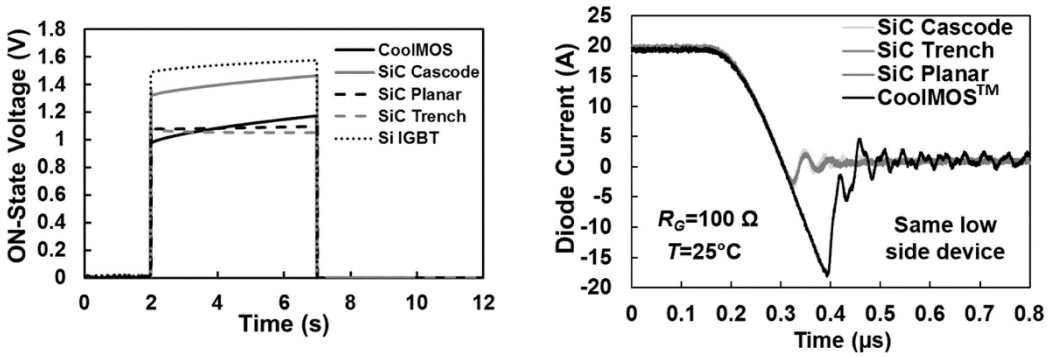
Improved energy conversion efficiency is widely cited as a benefit of SiC devices along with high temperature operation and fast switching rates. SiC MOSFETs are now an established power device technology competing with silicon MOSFETs and IGBTs in the 650 V to 1200 V application space[39]. SiC MOSFETs are well known for good avalanche performance in comparison with silicon MOSFETs and IGBTs [40-48]. This is due to the wide bandgap and high critical electric field characteristics of SiC which means more energy is required to generate electron-hole pairs through impact ionization [47]. SiC has a higher electric field and therefore a reduced rate of impact ionization. Although SiC MOSFETs have smaller active areas and higher junction-to-case transient thermal impedance, they are nevertheless very rugged under single and repetitive avalanche cycling.

However, SiC MOSFET devices continue to have reliability challenges regarding the performance of the gate oxide under short circuits [49, 50], threshold voltage shift from bias temperature instability [51-54] and time dependent dielectric breakdown [55].

SiC Stand-alone SiC JFETs have negative threshold voltages and therefore operate in depletion mode with excess gate currents [56]. Since this is not suitable for traditional power electronics applications that use normally-off devices with low leakage currents, SiC JFETs were not widely accepted by the industry.

The cascode is attractive because it avoids the problems in the stand alone JFET by using the LV Si MOSFET for switching, thereby operating in enhancement mode (normally-off). Also, the SiC Cascode JFET avoids the problem of increased interface trap density and fixed oxide traps in SiC/SiO_2 MOS interfaces. SiC MOSFETs have been reported to have reduced gate oxide reliability compared to silicon MOSFETs and IGBTs [57-61].

Another key advantage of the SiC Cascode JFET reported in previous literatures includes the reliability of the body diode because it uses the body diode of the low voltage Si MOSFET. This is more reliable than the SiC MOSFET body diode which is prone to bipolar degradation. The SiC cascode JFET also faces low losses during 3rd quadrant operation (also called reverse conduction) [39, 62, 63]. This is key to improving switching losses in applications with inductive loads. Applications such as synchronous dc-dc converters and inverters where the power transistor operates in the third quadrant benefit from this advantage. Figure 2.5 shows the comparison of the SiC cascode JFET body diode with other technologies as reported in literature.



(a) (b)

Figure 2.5 3rd quadrant performance of the Cascode reproduced from literature [39] (a) Forward voltage of body diodes (b) reverse recovery current in the body diodes

To further illustrate the competitiveness of the SiC Cascode JFET, the performance of the SiC cascode was measured and benchmarked against SiC MOSFETs of similar current ratings and targeted towards the 650 V voltage class and presented in this section. The datasheet references for the comparison are SiC cascode JFET (UJ3C065080K3S, 31 A), SiC trench MOSFET (SCT3060AL, 39 A), and SiC Planar MOSFET (C3M0065090D, 36 A). All switching measurements were taken from a clamped inductive switching test circuit (Figure 2.18) where the device under test (DUT) switches an inductive load using a SiC Schottky diode as

the free-wheeling diode. The SiC cascode JFET exhibits the best performance at the lowest external gate resistance (R_G). Figure 2.6(a) shows the turn-on di/dt, and Figure 2.6(b) shows the measured turn-off dV/dt for the three different SiC technologies evaluated. All references to gate resistance in this work are of external gate resistance except stated otherwise.

The total switching energy and specific ON-state resistance has been measured for these SiC device technologies to ascertain how the SiC Cascode JFET performs compared with SiC planar and Trench MOSFETs. Figure 2.7 shows the measured total switching energy at different temperatures where it is evident that the SiC Cascode JFET is the best performing device [39, 64].

The specific ON-state resistances have been calculated by static ON-state measurements of the forward voltage. The results are shown in Figure 2.8 for the SiC Cascode JFET, SiC Planar MOSFET and SiC Trench MOSFET. The SiC Cascode JFET exhibits the lowest specific ON-state resistance compared to the other SiC technologies.

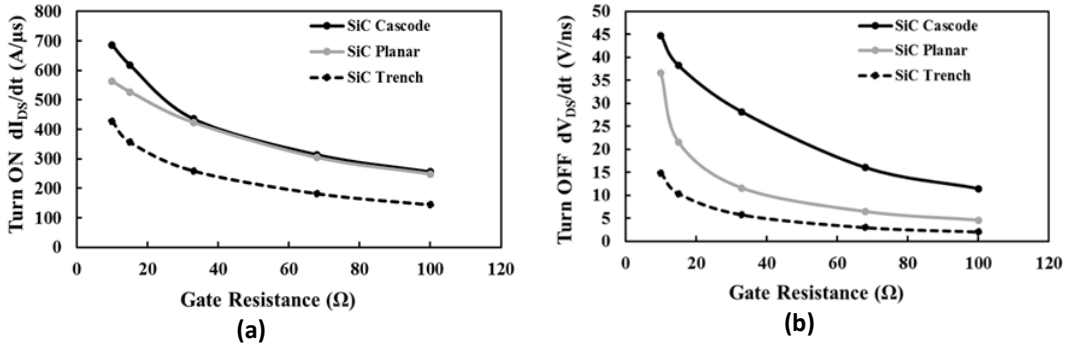


Figure 2.6(a) Measured turn-on dI/dt vs Gate resistance for different SiC technologies (b) Measured turn-off dV/dt vs gate resistance for different SiC technologies.

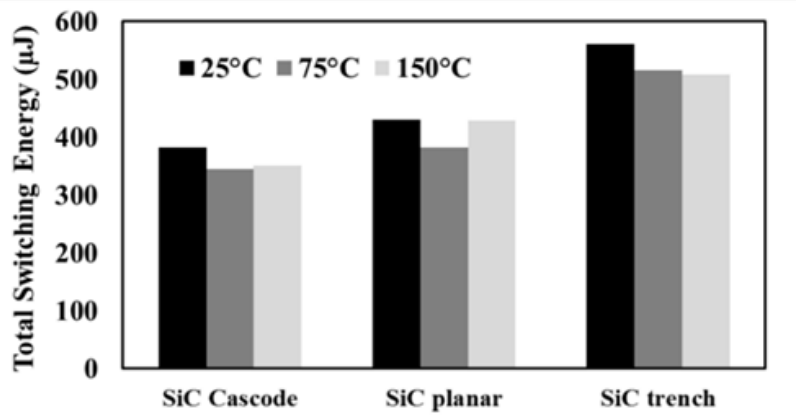


Figure 2.7 Total Switching Energy of the SiC devices at different temperatures.

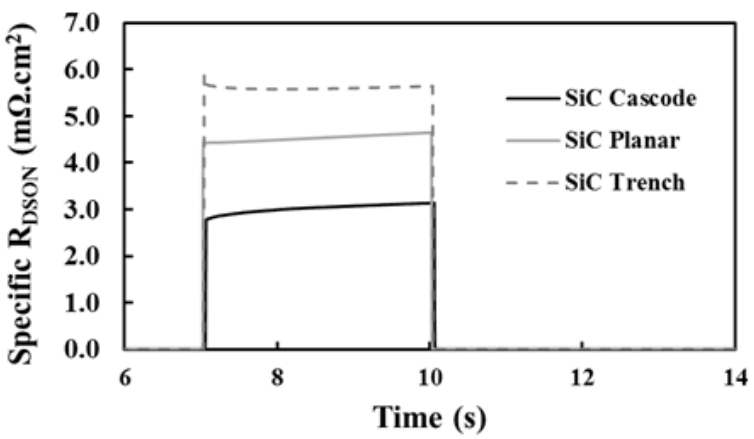
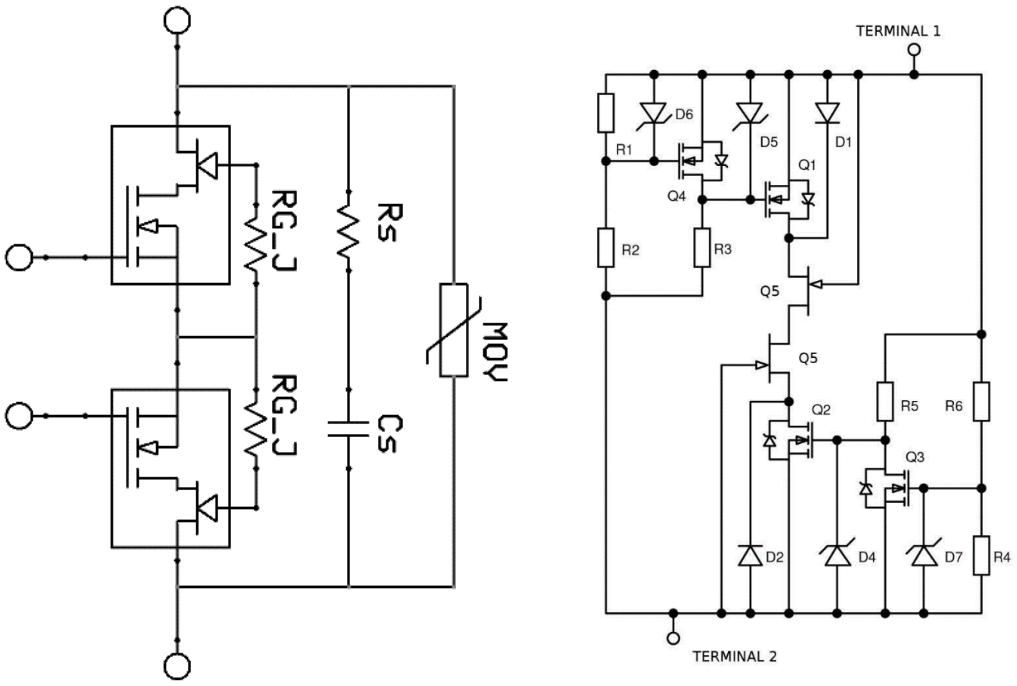


Figure 2.8 Specific ON-state resistance of the different SiC device technologies

2.3. Applications of Cascode JFET



(a) **(b)**

Figure 2.9 (a) Circuit architecture of a solid-state circuit breaker (b) Two-terminal self-biasing circuit breaker concept[65]

A wide variety of applications for the cascode have been reported in literature, these especially include applications that require fast turn-off[64-67]. Some of the applications recommended by the manufacturer include solid state circuit breakers, electric vehicle charging, Photovoltaic (PV) inverters, switched-mode power supplies, Industrial power supplies, Telecom and server power, power factor correction modules, motor drives, and induction heating. Figure 2.9 shows the circuit architecture of two circuit breaker concepts as an example employing the cascode.

Another application that has seen increasing interest is the construction of the “super cascode”[1, 68-70]. This concept employs extra SiC JFETs in series making the cascode capable of switching much higher voltages (up to 10 kV). Figure 2.10 shows the internal structure of the SiC super cascode and module prototype.

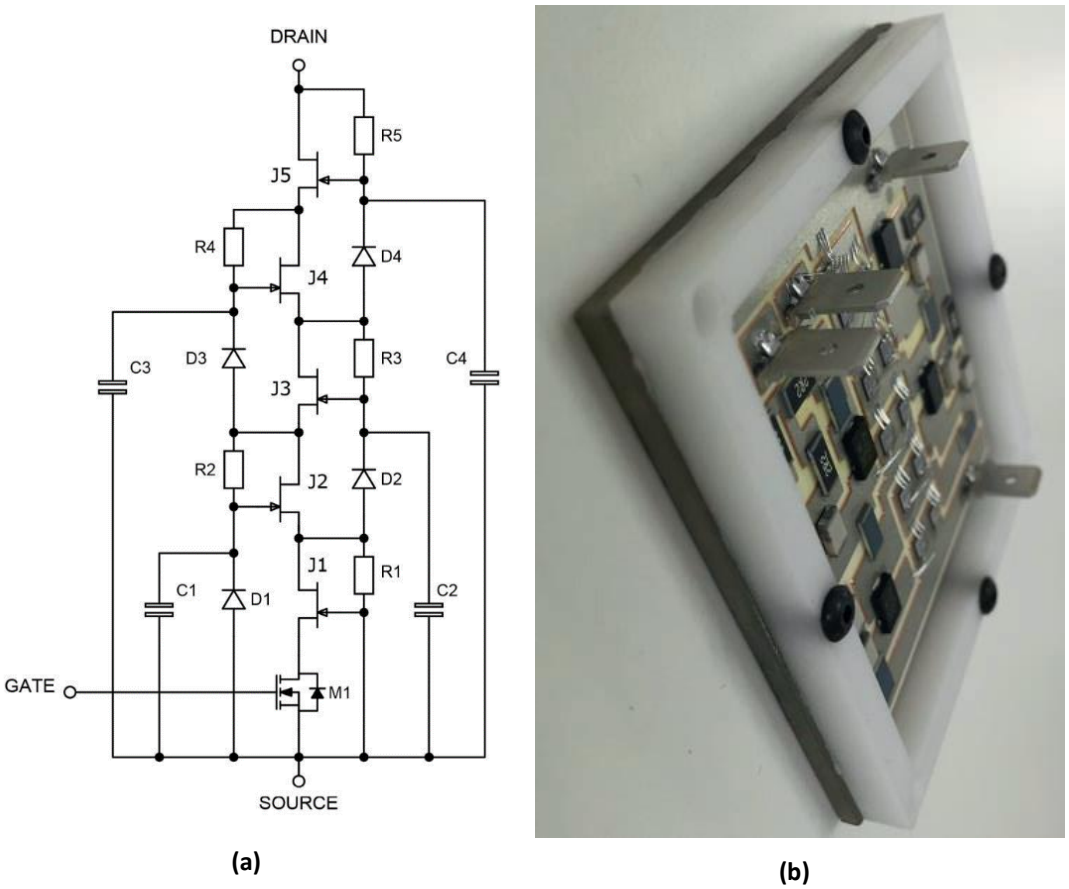


Figure 2.10 (a) super cascode circuit (b) super cascode module prototype[1]

2.4. Challenges of SiC Cascode JFET

The main factors mitigating widespread incorporation of SiC Cascode JFET in power electronic applications are possible problems when using Cascode JFETs in very high-voltage switching circuits resulting from significant difference between the MOSFET capacitance C_{DS_M} and that of the JFET capacitance C_{DS_J} [71]. Improper selection of the LV MOSFET with the correct capacitance causes instability during switching. Another important factor is limited research into the device robustness and failure mechanisms under various operating conditions.

As SiC cascode JFETs are gaining popularity in different applications [64, 72, 73], reliability and robustness studies are fundamental for increasing their adoption. Hence, it has become necessary to understand the robustness and failure mechanisms under various operating conditions, e.g., avalanche robustness and short circuit robustness.

In SiC MOSFETs, various studies have shown that the gate terminal is the failure point under SC conditions. This results from thermally generated carriers tunnelling through the gate oxide thereby causing permanent damage [74-78]. Also, the latch up of the parasitic BJT in SiC MOSFET is the reported failure mechanism in Avalanche [79].

In SiC Cascode JFETs, since a LV silicon MOSFET is used, the failure mode is different. The performance of SiC Cascode JFETs under SC conditions were evaluated previously [80, 81], with the trade-off between the short circuit withstand time SCWT and specific on-resistance demonstrated. Considering unclamped inductive switching (UIS), previous studies indicated the key role of the gate leakage current of the JFET during UIS conditions coupled with peculiar turn-off behaviour [8, 82, 83]. However, more studies need to be carried out to fully evaluate and understand the various failure modes and potential failure points in the SiC Cascode JFETs.

2.5. Fundamentals of Finite element modelling (FEM)

Characterising semiconductor device robustness leads to an increase in current and thermal runway. As a result, this requires precise modelling of the electrical and thermal behaviour within the semiconductor by the FEM simulator. The FEM simulator used in this research is the SILVACO ATLAS platform. The framework for the semiconductor electrical behaviours in ATLAS consists of fundamental equations which link together the electrostatic potential and the carrier densities within the simulation domain (represented by the finite element grid). These equations consist of Poisson's equation, the continuity equations, and the transport equations. In conjunction with the electrical equations, the thermal behaviour and self-

heating effects are simulated by solving the lattice heat flow equations in ATLAS. The equations to be solved consist of heat source/generation equations, heat flux equation, and boundary equations. These equations are then discretised for use in the simulation domain. This section summarises the fundamental model equations, material physical models, and the heat flow equations. The focus will be on the models necessary for FEA simulation of the SiC Cascode JFET.

- ## Energy Band Gap

The bandgap energy E_G is the difference in energy between the conduction band, E_C and valence band, E_V. The default Band gap model in ATLAS is the universal band gap energy shown in Eq. 2.1, this can be changed to account for required parameters and complexity. The parameters $E_G(300)$, α, and β can be specified on the MATERIAL statement in ATLAS with EG300, EGALPHA, and EGBETA respectively dependent on the material for simulation.

$$E_G(T_L) = E_G(0) - \frac{\alpha {T_L}^2}{T_L + \beta} = E(300) + \alpha\left(\frac{300^2}{300 + \beta} - \frac{{T_L}^2}{T_L + \beta}\right)$$

Eq. 2.1

- ## Fermi Statistics

Defining the carrier concentration in semiconductors is done by the Fermi-Dirac distributions and a parabolic density of states. The equations guiding this relationship are presented in Eq. 2.2 and Eq. 2.3.

$$n = N_c F_{1/2}\left(\frac{E_f - E_c}{kT}\right)$$

Eq. 2.2

$$p = N_v F_{1/2}\left(\frac{E_v - E_f}{kT}\right)$$

Eq. 2.3

Where the N_C and N_V are the density of states in the conduction and valence bands respectively, $F_{½}$ is referred to as the Fermi-Dirac integral of order ½, E_f is the fermi level, E_C and E_V are the conduction and valence band energy respectively, k is the Boltzmann's constant, and T is the temperature.

- ## Intrinsic Carrier Concentration (n_i)

The intrinsic carrier concentration is controlled by the thermal generation of electron hole pairs across the energy band gap of a semiconductor. The intrinsic carrier concentration can be determined from the energy band gap (E_G)[84].

$$n_i = \sqrt{np} = \sqrt{N_c N_v} \cdot e^{-\frac{E_G}{2KT}}$$

Eq. 2.4

- Carrier mobility (μ_n and μ_p)

Mobility describes the various processes responsible for scattering during electrical transport. These processes cause carriers to lose momentum. They include lattice vibrations (phonons), impurity ions, other carriers, surfaces, and other material imperfections.

The simplest way to model the mobility is with a constant mobility throughout the cell structure for a given material. The actual mobility is not constant because of the previously mentioned processes. This is accounted for by modelling its dependence on electric field, carrier concentration, temperature, and proximity to interfaces etc.

Four key division aid proper modelling of the mobility: (i) The mobility at low electric -field, (ii) Mobility at high electric field, (iii) Mobility within the semiconductor bulk regions and (iv) inversion layers.

The mobility at low electric field represents the mobility of carriers near equilibrium. In ATLAS, the low-field mobility can be modelled in five different ways. First, using constant carrier mobility values(MUN and MUP). The next option is using a look-up table (CONMOB). For more accuracy, the mobility can be modelled by an analytic model (ANALYTIC, ARORA, or MASETTI). The fourth possibility is a carrier-carrier scattering (CCSMOB, CONWELL, or BROOKS). The last option is the unified low-field mobility model (KLAASSEN).The model used in this work is the analytic (ANALYTIC) low-field mobility. It is based on the Caughey and Thomas doping dependent mobility[85] in Eq. 2.5 with added temperature dependence. The model is selected using the MODEL statement in ATLAS, and the parameters can be specified using the MOBILITY statement for improved accuracy.

$$\mu = \frac{\mu_{max} - \mu_{min}}{1 + (N/N_{ref})^{\alpha}} + \mu_{min}$$

Eq. 2.5

where N is doping concentration.

The mobility at high electric fields is accounted for by a saturation in carrier velocity. Increasing electric field magnitude causes carriers to gain more energy. This increases the probability of various scattering phenomena and consequently a saturation in the carrier velocity coupled with a reduction in effective mobility. This modelled in ATLAS using the parallel field dependent model (FLDMOB) based on the Caughey and Thomas field dependent mobility in Eq. 2.6. Similar to the low-field mobility, the parameters can be specified in the MOBILITY statement.

$$\mu = \mu_0 \left(\frac{1}{1 + \left(\frac{\mu_0 E}{V_{sat}} \right)^{\beta}} \right)^{\frac{1}{\beta}}$$

Eq. 2.6

Where μ_0 is the low-field carrier mobility, V_{sat} is the saturation velocity, and E is parallel electric field.

Another crucial mobility model used in this work is the Lombardi Model (CVT)[86] presented in Eq. 2.7. This is essential for increased mobility accuracy within the inversion layer of MOSFET structures. It accounts for various mobility degradation phenomena within the inversion layer, i.e., the carrier mobility limited by scattering with surface acoustic phonons (μ_{ac}), the carrier mobility in bulk semiconductor (μ_b), and the carrier mobility limited by surface roughness scattering (μ_{sr}). This model can also be modified to account for the effects of coulomb scattering by setting ALTCVT.N and ALTCVT.P on the MOBILITY statement for electron and hole mobility respectively. The JFET is not limited by surface roughness (μ_{sr}), this can be accounted for by adding ^ALT.SR.N to the statement.

$$\frac{1}{\mu_T} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}}$$

Eq. 2.7

- Poisson's Equation

Poisson's equation is derived from relating the electrostatic potential to the space charge density using their relationship with Electric field as shown below,

$$\nabla \cdot \vec{E} = -\frac{\rho}{\varepsilon}$$

Eq. 2.8

$$\vec{E} = -\nabla \Psi$$

Eq. 2.9

Where E is the electric field, Ψ the electrostatic potential, ε the semiconductor dielectric constant, and ρ represents the local space charge density consisting of electrons and holes concentration, ionised impurities, and possible traps.

Combining these two equations gives the poison's equation in Eq. 2.10,

$$\varepsilon \nabla^2 \Psi = -\rho$$

Eq. 2.10

- Carrier continuity equations

The change in the electron and hole densities due to the transport, generation, and recombination processes are modelled by the continuity and transport equations. The continuity equations are given in Eq. 2.11 and Eq. 2.12.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \vec{J}_n + G_n - R_n$$

Eq. 2.11

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \vec{J}_p + G_p - R_p$$

Eq. 2.12

Where n and p represent the carrier concentration (electron and hole respectively), J_n and J_p represent the carrier current density, G_n and G_p are the carrier generation rates, R_n and R_p are the carrier recombination rates, and q is the magnitude of charge.

To further model the components of the continuity equations(i.e., carrier current density, carrier generation, and carrier recombination), the transport equations are used. The models are derived from approximations of the Boltzmann transport equation. This approximation results in various forms of the transport models. The simplest transport model called the drift-diffusion model expresses the current densities with respect to the Quasi Fermi levels (Φ_n and Φ_p),

$$\vec{J}_n = -q\mu_n n\nabla\Phi_n$$

Eq. 2.13

$$\vec{J}_p = -q\mu_p n\nabla\Phi_p$$

Eq. 2.14

Where μ_p and μ_n are the hole and electron mobilities, and q is the electronic charge.

The relationship between the Quasi Fermi levels and the carrier concentration is given by,

$$\Phi_n = \Psi - \frac{KT_L}{q}\ln\frac{n}{n_i}$$

Eq. 2.15

$$\Phi_p = \Psi + \frac{KT_L}{q}\ln\frac{p}{n_i}$$

Eq. 2.16

Where n_i is the effective intrinsic carrier concentration, K the Boltzmann constant, and T_L is the lattice temperature.

The conventional form of the drift diffusion equation presented in Eq. 2.17 and Eq. 2.18 is obtained by rearranging Eq. 2.8 to Eq. 2.16,

$$\vec{J}_n = -q\mu_n n\nabla\Phi_n = -q\mu_n n\nabla\left(\Psi - \frac{KT_L}{q}\ln\frac{n}{n_i}\right) = q\mu_n n(-\nabla\Psi) + q\mu_n\frac{KT_L}{q}n\nabla\left(\ln\frac{n}{n_i}\right)$$

$$\vec{J}_n = q\mu_n n\vec{E}_n + \mathbf{q}D_n\nabla\mathbf{n}$$

Eq. 2.17

$$\vec{J}_p = q\mu_p p\vec{E}_p - \mathbf{q}D_p\nabla\mathbf{p}$$

Eq. 2.18

Where D = μ*KT_L/q, represents the carrier diffusion coefficients.

Carrier recombination

Carrier recombination is one of the mechanisms in control of restoring equilibrium within the semiconductor material after a perturbation to the thermal equilibrium. This return to equilibrium conditions is regulated by several simultaneous processes:[84]

a) recombination occurring due to an electron dropping directly from the conduction band into the valence band,

b) recombination occurring due to an electron dropping from the conduction band and a hole dropping from the valence band to a recombination level located within the energy band gap, and

c) recombination occurring due to electrons and holes in the conduction and the valence band respectively dropping into surface traps.

The rate of recovery is regulated by the minority carrier lifetime. During recombination, the energy of the carriers is dissipated by one of several mechanisms: (1) the emission of a photon (referred to as radiative recombination); (2) the distribution of the energy into the lattice in the form of phonons (referred to as multi-phonon recombination); and (3) the transmission of the energy to a third particle, which can be either an electron or a hole (referred to as Auger recombination)

In ATLAS, the recombination model is selected with the MODEL statement.

The Shockley Read Hall (SRH)[87, 88] formulation in Eq. 2.19 models the phonon transition in the semiconductors. The model can be further expanded to include dependence of carrier lifetimes on impurity concentration, total doping, and temperature.

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left[n + n_i e^{\left(\frac{E_{TRAP}}{KT_L}\right)}\right] + \tau_n\left[p + n_i e^{\left(\frac{E_{TRAP}}{KT_L}\right)}\right]}$$

Eq. 2.19

Where τ_n and τ_p are the minority carrier lifetimes of electrons and holes respectively.

Auger recombination (AUGER) is described by Eq. 2.20.

$$R_{Auger} = C_n\left(pn^2 - nn_i^2\right) + C_p\left(np^2 - pn_i^2\right)$$

Eq. 2.20

where C_n and C_p are Auger coefficients and are dependent on the type of material to be simulated. The coefficients can be defined using the MATERIAL statement in ATLAS.

Carrier generation (Impact ionization)

The generation of carriers in Poisson's basic equations is represented as impact ionisation. Understanding impact ionisation is important for accurate modelling of semiconductor devices breakdown. This is especially useful for high power and high voltage class power electronics. The impact ionisation mechanism is described by Eq. 2.21. This process requires carriers to gain enough energy to be ionized between collision which is provided by high electric fields.

$$G = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q}$$

Eq. 2.21

G is the local generation rate of electron-hole pairs, α_n and α_p are the ionization coefficient for electrons and holes, and J_n and J_p are the carrier current densities. Defining the impact ionization model in use for SILVACO ATLAS simulations is achieved with the IMPACT statement. The α_n and α_p are described using the equations below,

$$\alpha_n = A_N e^{\left[-\left(\frac{B_N}{E}\right)^{BETA_N}\right]}$$

Eq. 2.22

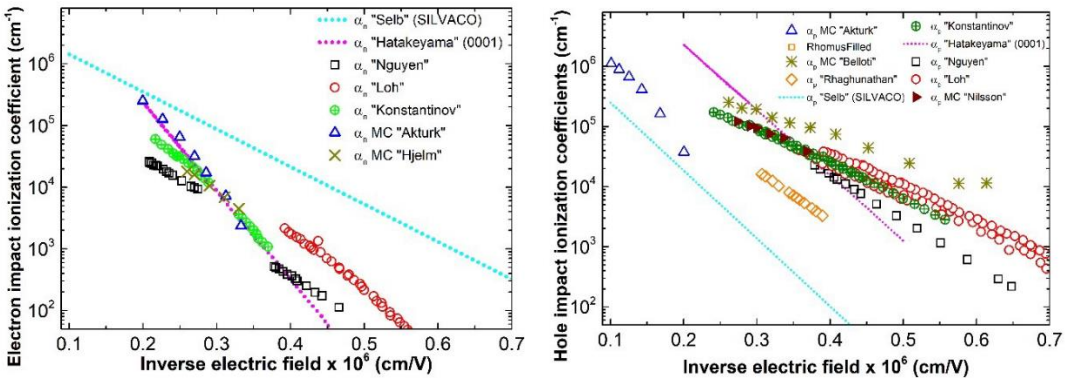
$$\alpha_p = A_P e^{\left[-\left(\frac{B_P}{E}\right)^{BETA_P}\right]}$$

Eq. 2.23

Where E is the electric field perpendicular to current flow at a point within the structure. A_N, A_P, B_N, B_P, $BETA_N$, and $BETA_P$ are fitting parameters. All model parameters to be used are also defined on the IMPACT statement. The parameter values used within this thesis are given in Table 2-2. These were extracted from the Loh model for impact ionisation in 4H-SiC[89]. For comparison, Figure 2.11 shows this model and various other SiC models reported in literature and their influence on the impact ionisation coefficients in relation to electric field. The default parameters in SILVACO ATLAS are for impact ionisation in Si and are used as a reference in the figure.

Table 2-2 Impact ionisation coefficients for 4H-SiC[89]

Variable	Values	ATLAS units
AN1	2.78 x 10^6	cm^{-1}
AN2	2.78 x 10^6	cm^{-1}
AP1	3.51 x 10^6	cm^{-1}
AP2	3.51 x 10^6	cm^{-1}
BN1	1.05 x 10^7	V/cm
BN2	1.05 x 10^7	V/cm
BP1	1.03 x 10^7	V/cm
BP2	1.03 x 10^7	V/cm
BETAN	1.37	-
BETAP	1.09	-



(a) **(b)**

Figure 2.11 Relationship of impact ionisation coefficient with electric field for SiC reproduced from literature [89-99].

- Thermal Model

The thermal properties are defined in ATLAS with the MATERIAL statement. This statement solves the heat flow equation of Eq. 2.24 together with the electrical equations as mentioned earlier.

$$C_\rho \left(\frac{\partial T_L}{\partial t}\right) = \nabla(\kappa \nabla T_L) + H$$

Eq. 2.24

Where C_ρ is the heat capacitance per unit volume, κ is the thermal conductivity., H is the heat generation, T_L is the local lattice temperature.

The heat source can be split in three parts. The first is Joule heating, this results from flow of current. The next is generation and recombination heat as a results of carrier generation and recombination. The last is called Thompson and Peltier heating. This results from a change in thermoelectric power.

The electron and hole current densities are modified as in Eq. 2.25 and Eq. 2.26 to account for effects of variation in lattice temperature within the device cell.

$$\vec{J}_n = -q\mu_n n(\nabla\Phi_n + \mathbf{P}_n\nabla\mathbf{T}_L)$$

Eq. 2.25

$$\vec{J}_p = -q\mu_p p\left(\nabla\Phi_p + \mathbf{P}_p\nabla\mathbf{T}_L\right)$$

Eq. 2.26

Where P_n and P_p are the absolute thermoelectric powers for electrons and holes.

The Heat capacity is modelled in ATLAS by polynomial model in Eq. 2.27. Model parameters for the polynomial model used in this thesis are presented in Table 2-3.

$$c(T) = A_c + B_c T + C_c T^2 + D_c T^{-2}$$

Eq. 2.27

Table 2-3 SiC thermal capacitance constants [100, 101]

Variable	ATLAS notation	SiC	ATLAS units
A_c	HC.A	0.676	J/cm^{3}K
B_c	HC.B	6.565 x 10^{-3}	J/cm^{3}K^2
C_c	HC.C	-3.697 x 10^{-7}	J/cm^{3}K^3
D_c	HC.D	6.852 x 10^{-10}	JK/cm^3

The thermal conductivity can be specified by four models on ATLAS. The constant model, the power model, the polynomial model, and the reciprocal model. The model used for this thesis is the polynomial model presented in Eq. 2.28. The polynomial model parameters for the simulations in this work were modified according to previous literature and are presented in Table 2-4.

$$\kappa(T) = \frac{1}{A_\kappa + B_\kappa T + C_\kappa T^2}$$

Eq. 2.28

Table 2-4 SiC thermal conductivity constants [100]

Variable	ATLAS notation	SiC	ATLAS units
A_k	TC.A	-0.171	cm·K/W
B_k	TC.B	1.488 x 10^{-3}	cm/W
C_k	TC.C	0	Cm/W·K

For device thermal simulations to run successfully, a thermal boundary conditions (approximating a heat sink as a lumped thermal resistance or conductance) must be specified. This is done using the THERMCONTACT statement. Including the thermcontact statement adds Eq. 2.29 to the heat flow equation. ALPHA is the thermal conductance of the boundary in W/(cm^{2}K), T_L is the lattice temperature, and T_B is the starting temperature of the boundary (heatsink/ambient).

$$\overrightarrow{J_{tot}^{u}} \cdot \vec{s} = ALPHA(T_L - T_B)$$

Eq. 2.29

2.6. Finite Element Modelling (FEM) of SiC Cascode JFETs

The steps in modelling the SiC JFET and other structures investigated in this thesis are demonstrated in the flow chart in Figure 2.12. In the subsequent sections the model strategy is demonstrated with static characterisation of the FE model.

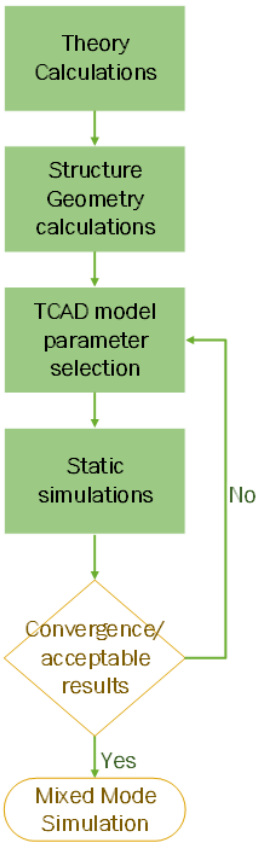


Figure 2.12 Flow chart of FEA modelling strategy

- ### Structure Geometry and Mesh

Pinch-off or JFET Threshold Voltage, (V_{TH_J})

The pinch off Voltage is the voltage require to close the channel of the JFET. Eq. 2.30 is the equation for determining the pinch-off voltage. This is derived from the depletion width equation with the assumption that the channel is completely depleted (pinched-off). This is used to design the desired channel width.

$$V_{TH\_J} = \Psi_{bi} - \Psi_p$$

Eq. 2.30

$$\Psi_p = \frac{qN_D a^2}{2\varepsilon}$$

Eq. 2.31

Where Ψ_p is the pinch-off potential, a is half the channel width, N_D is the donor concentration.

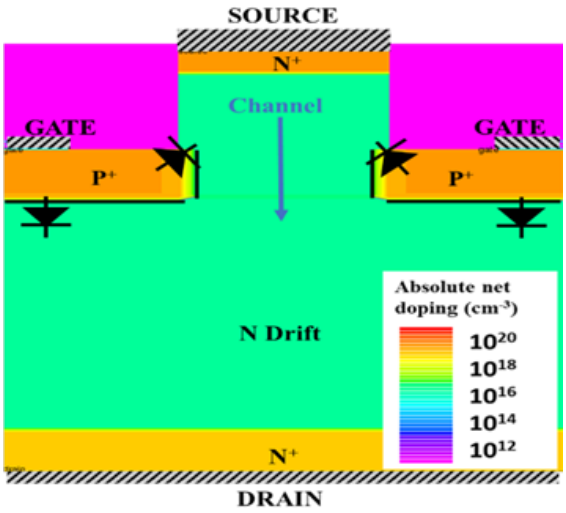
Breakdown

The breakdown of the JFET is regulated by the gate-drain P-N junction. This theoretical width of the JFET drift to achieve the desired breakdown is controlled by the simple breakdown equation.

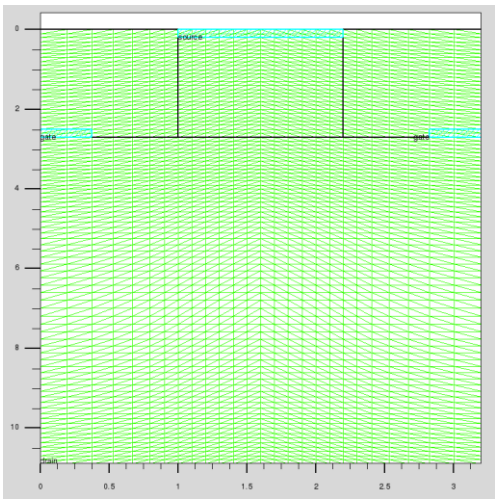
$$V_{BD} = \frac{E_C \cdot W_D}{2}$$

Eq. 2.32

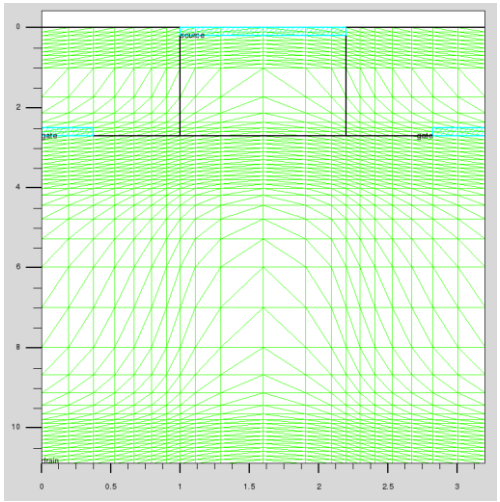
Structure and Mesh



(a)



(b)



(c)

Figure 2.13 SiC JFET structure with different mesh strategies (b) Tight Mesh (C) Loose Mesh.

Figure 2.13(a) shows the geometry of the JFET simulated in ATLAS. The geometry used is based on the SiC JFET from UnitedSiC [102]. The main difference is the absence of a P+ doped side wall in the channel. This P+ doping has a proportional effect on the parasitic capacitance,

C_{DS} of the JFET, and impacts the breakdown voltage of the gate-source junction. It also aids the reduction of drain Induced barrier lowering (DIBL) by increasing the channel length.

The device mesh is pictured in Figure 2.13(b) and (c). With the simplicity of the JFET structure, the mesh could be tight without too much consequence to simulation time while increasing accuracy. Figure 2.13(c) is a loose mesh strategy compared to the tight mesh density in Figure 2.13(b). Figure 2.14 shows the difference in breakdown voltage (V_{BR}) resulting from both mesh strategies. The loose mesh has a V_{BR} 23 V higher than the tighter mesh. Another difference is the smoothness of the curve for the tighter mesh showing improved accuracy.

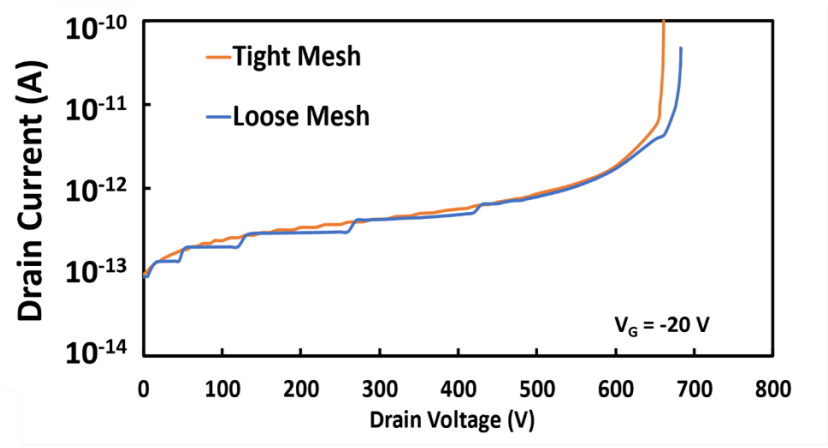
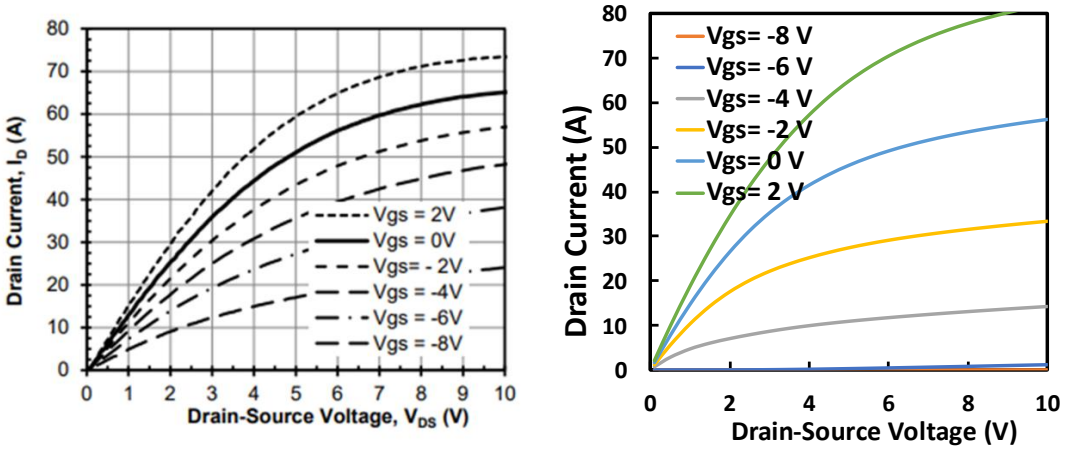


Figure 2.14 SiC JFET static breakdown Simulation.

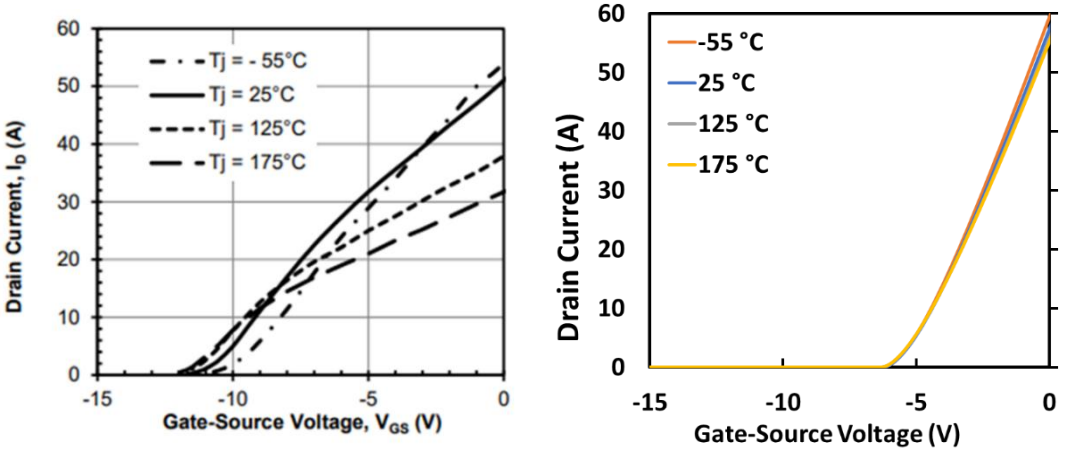
- Static characteristics

Figure 2.15 to Figure 2.17 presents the datasheet (UJ3N065080K3S) and ATLAS simulated static characteristics of the stand-alone vertical SiC JFET used to implement the cascode device. Figure 2.15 and Figure 2.16 show the output and transfer characteristics respectively, and Figure 2.17 shows the device capacitances. From the plots of the capacitance in Figure 2.17, the simulated JFET structure has zero drain-source capacitance, C_{ds} unlike the case of the datasheet. Hence, the curve of C_{OSS} and C_{RSS} are the same. Also, the threshold voltage of the simulated structure in Figure 2.16 is higher than the typical threshold voltage from the datasheet (The threshold voltage from the JFET simulation is extracted at 20 mA like the datasheet). The differences between the simulated characteristics and datasheet values are attributed to three key reasons. First, the slight differences in the implemented SiC JFET structure stated previously. Secondly, the inexact doping concentration used compared to that of the manufacturers. Finally, the adoption of a uniform doping profile in comparison to gaussian-like profiles characteristic to real devices structures. However, the structure used was considered sufficient for the requirements of this work.



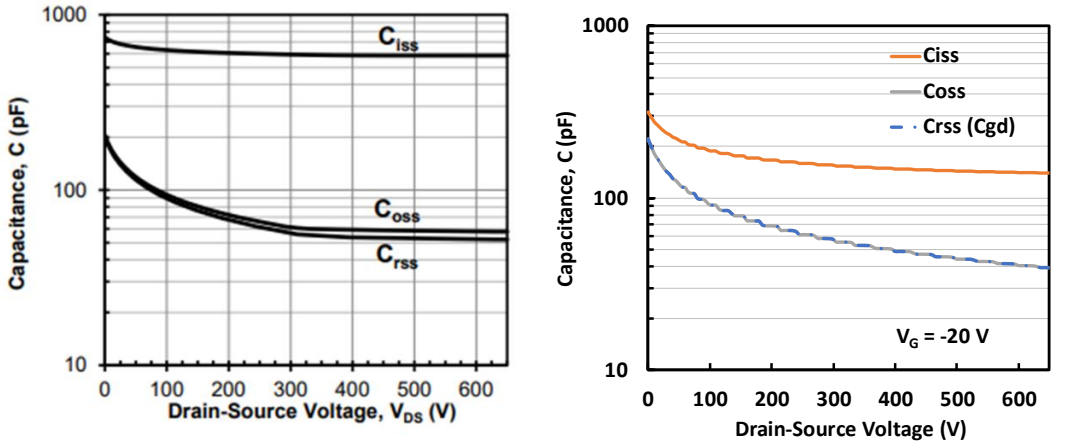
(a) (b)

Figure 2.15 Output characteristics of SiC stand-alone JFET (a) Datasheet (b) Simulated



(a) (b)

Figure 2.16 Transfer characteristics of SiC stand-alone JFET (a) Datasheet (b) Simulated



(a) (b)

Figure 2.17 SiC stand-alone JFET capacitances (a) Datasheet (b) Simulated.

- Mixed mode simulation (Double pulse test)

The cascode switching process was evaluated using the well-known double pulse test. Figure 2.18(a) shows a typical schematic of double pulse test circuit using a cascode JFET as the device under test (DUT) while Figure 2.18(b) shows the gate pulse sequence and typical characteristics during double pulse switching. Pictured in Figure 2.19 is the experimental setup for performing the double pulse tests. The plots of both turn-on and turn-off switching process and all the various stages in the SiC Cascode JFET are described in this section.

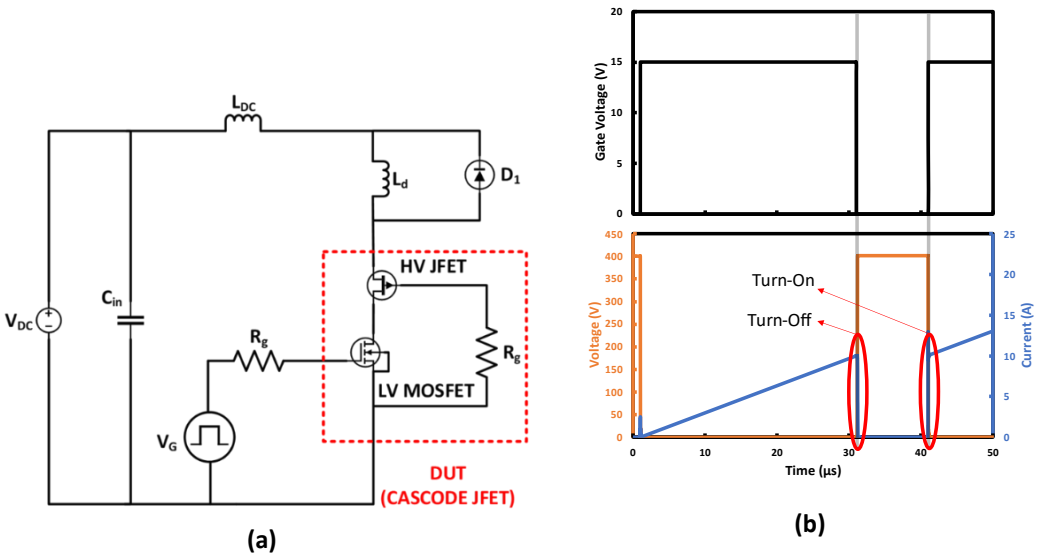
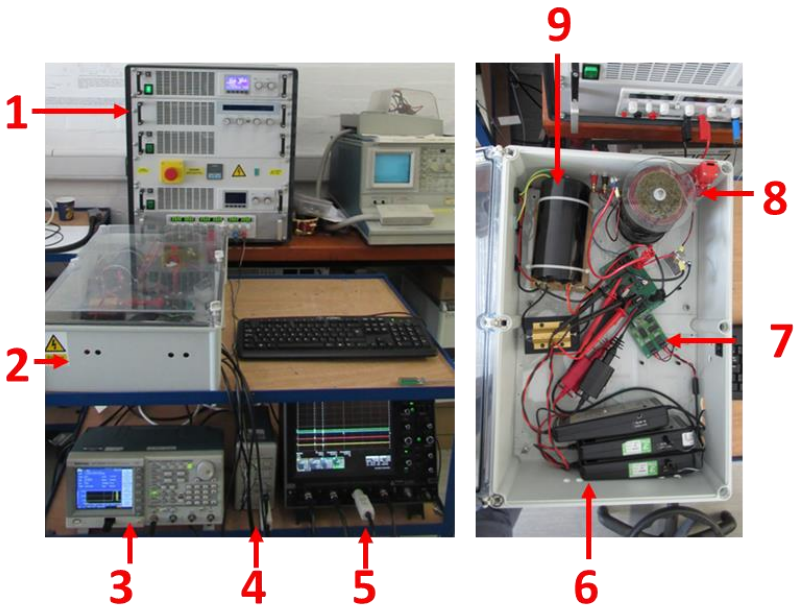


Figure 2.18 (a) Double pulse test circuit (b) Typical characteristics of a double pulse test

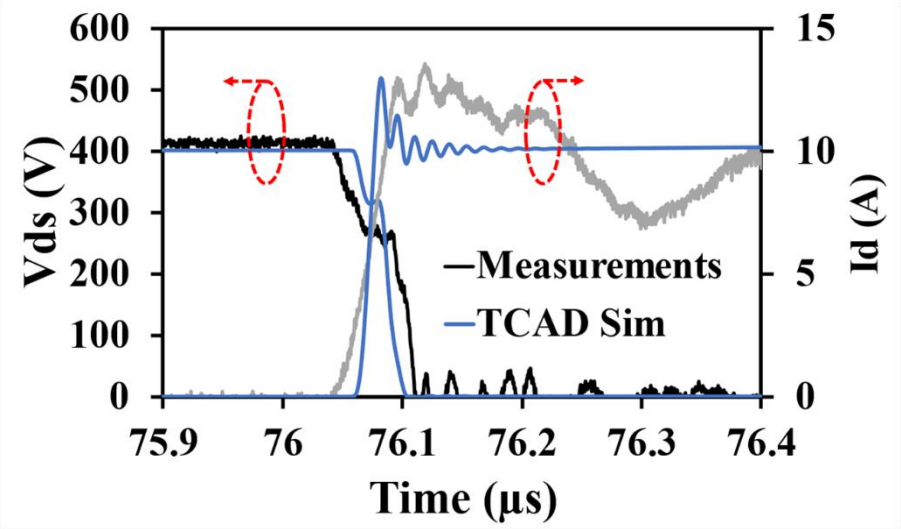


(1) DC Power supply, (2) Test Enclosure, (3) Function generator, (4) Current Probe Amplifier, (5) Oscilloscope, (6) Differential Voltage Probes, (7) Gate Driver, (8) Inductor, (9) DC Link capacitor

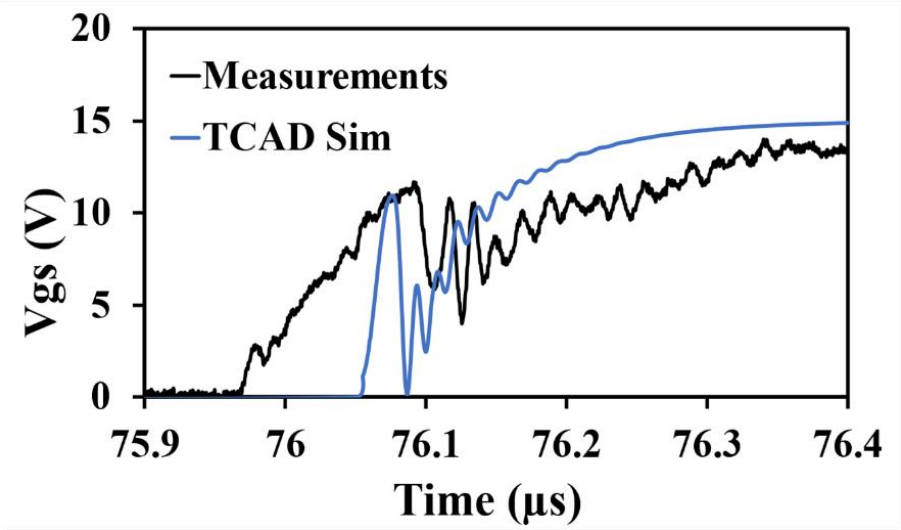
Figure 2.19 Double pulse test experimental setup

Turn-on

The cascode turn-on process was characterised using mixed mode simulations in ATLAS and compared with the experimental results. This is shown in Figure 2.20. Figure 2.21 demonstrates a simplified and exaggerated version of the switching process to ease description of the various stages of switching and the contributing parasitics.



(a)



(b)

Figure 2.20 Experimental measurement and simulated turn-on transient in SiC cascode JFETs (a) Cascode drain-source voltage and drain current (b) Gate-source Voltage

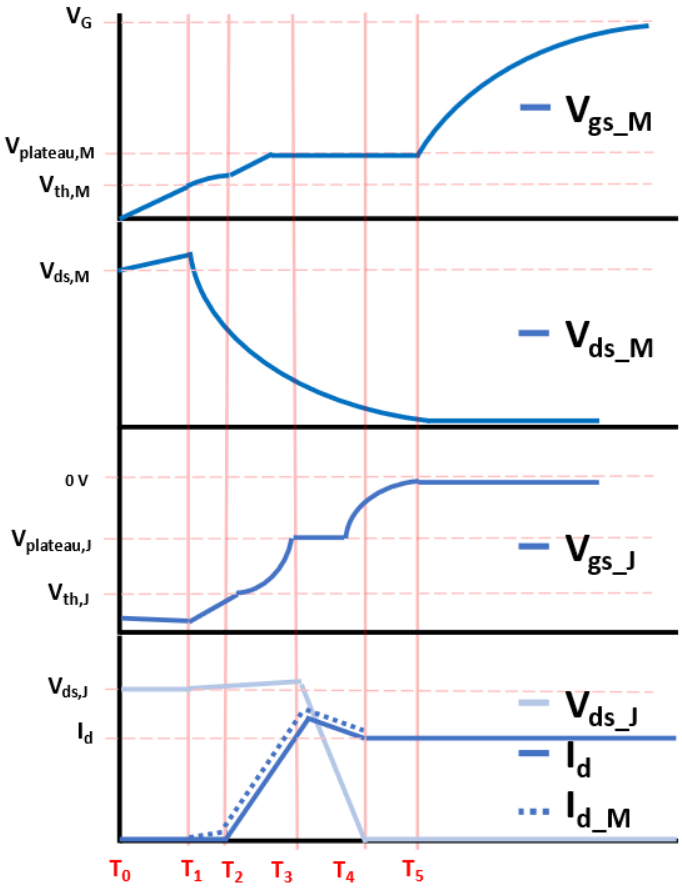


Figure 2.21 Turn-on transitions in a SiC Cascode JFET

Stage 1 ($T_0 - T_1$)

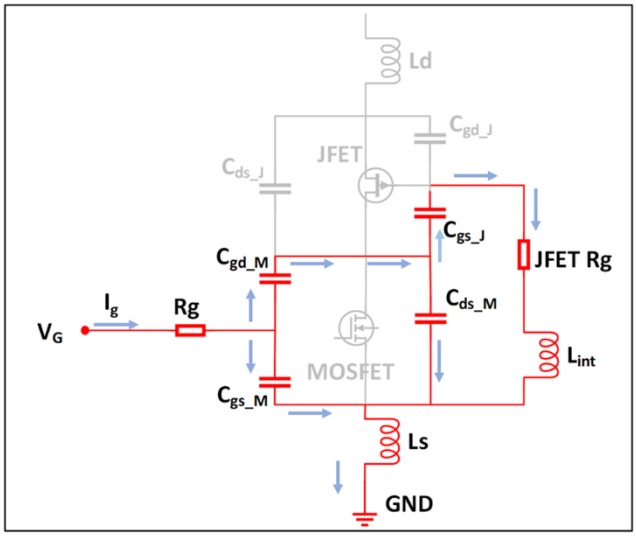


Figure 2.22 Equivalent circuit of SiC Cascode JFET during Stage 1 of turn-on.

At the start of the turn-on transient, C_{gs_M} charges and C_{gd_M} discharges. The two capacitances coupled together with R_g regulate the exponential rise in V_{gs_M}. V_{gs_M} rises to V_{th_M} during this stage. C_{ds_M} charges slightly, characterised by a slight increase in V_{ds_M}. Also, the increase in V_{ds_M} causes C_{gs_J} to discharge, characterized by a small decrease in V_{gs_J}.

Stage 2 ($T_1 - T_2$)

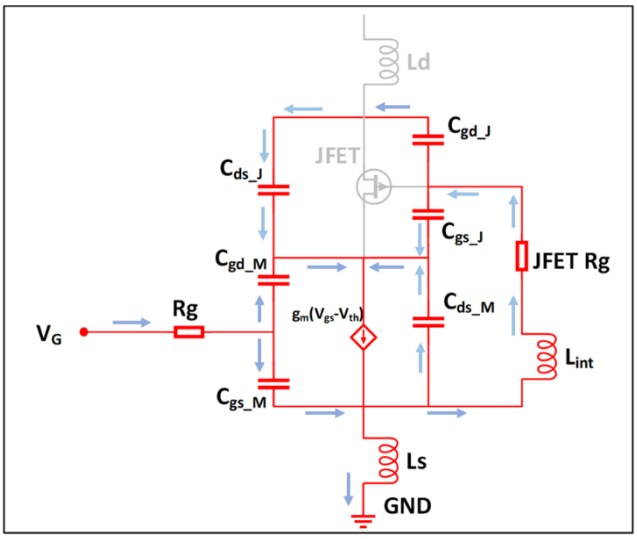


Figure 2.23 Equivalent circuit of SiC Cascode JFET during Stage 2 of turn-on.

At the start of the second stage Vgs_M is equal to the LV MOSFET V_{th} hence it starts to conduct current as the channel is open**.** C_{gs_M} charging rate slows down, hence the rise of V_{gs_M} slows down. The output capacitance, C_{gd_M} and C_{ds_M} continue to discharge as V_{ds_M} falls. During this stage, $V_{gs\_J} = -V_{ds\_M}$, hence as V_{ds_M} decreases, C_{gs_J} charges and V_{gs_J} rises towards V_{TH_J} (the pinch-off voltage of the JFET). This relationship is slightly different in reality because of the presence of JFET R_g and L_{int}. L_{int} contributes a phase delay between the V_{ds_M} and V_{gs_J}. The reduction in the Mosfet voltage V_{ds_M} due to the MOSFET causes the JFET must block additional voltage. Hence, V_{ds_J} rises slightly and C_{ds_J} charges due to this increase.

Stage 3 ($T_2 - T_3$)

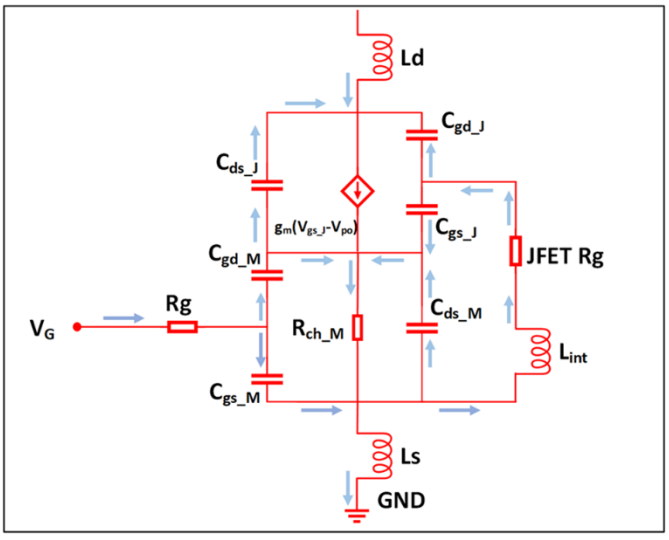


Figure 2.24 Equivalent circuit of SiC Cascode JFET during Stage 3 of turn-on.

At the start of this stage $V_{gs\_J} = V_{th\_J}$, and it continues to rise towards JFET $V_{plateau}$ throughout. C_{gs_J} charges as Vgs_J continues to rise. Also, the JFET current rises as its channel is open. C_{ds_J}

and C_{gd_J} are discharged. The rate at which C_{gs_M} charges increases, and V_{gs_M} tends towards MOSFET gate plateau voltage. C_{gd_M} continues to discharge as C_{ds_M} discharges completely at the end of this stage. Hence, the JFET gate voltage is dependent on the MOSFET channel resistance at the end of this stage.

Stage 4 ($T_3 - T_4$)

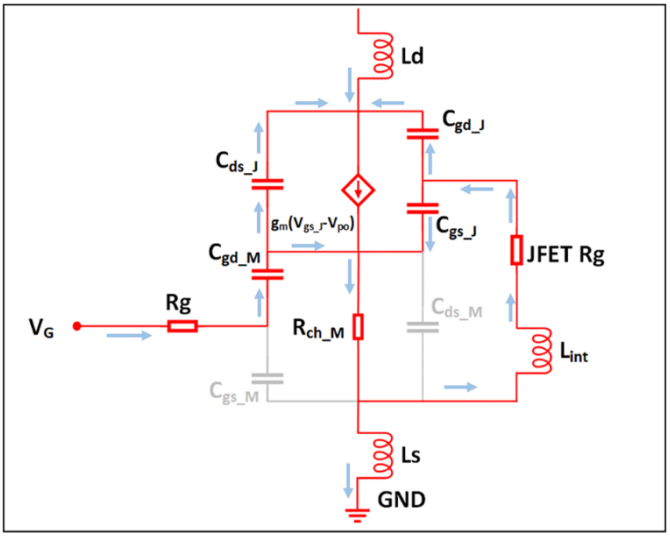


Figure 2.25 Equivalent circuit of SiC Cascode JFET during Stage 4 of turn-on.

At the start the cascode current is equal to the load current. There is induced overshoot and oscillations in the cascode current depending on the parasitic inductance. During this period, Vgs_J stays at the $V_{plateau\_J}$ as the cascode drain-source voltage (V_{ds_C}) falls exponentially. V_{gs_M} is also constant at $V_{plateau\_M}$.

Stage5 ($T_4 - T_5$)

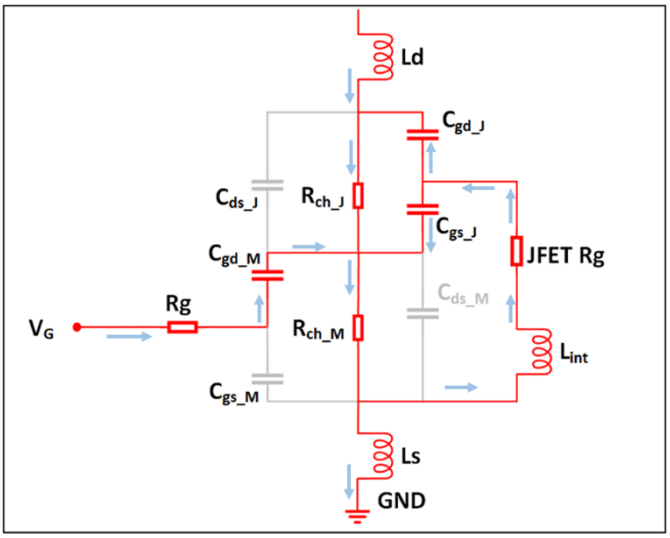


Figure 2.26 Equivalent circuit of SiC Cascode JFET during Stage 5 of turn-on.

During this stage, V_{gs_J} increases exponentially to 0, while V_{gs_M} is still at the MOSFET plateau. The JFET channel is equivalent to its channel Resistance.

Stage6 (> T_5)

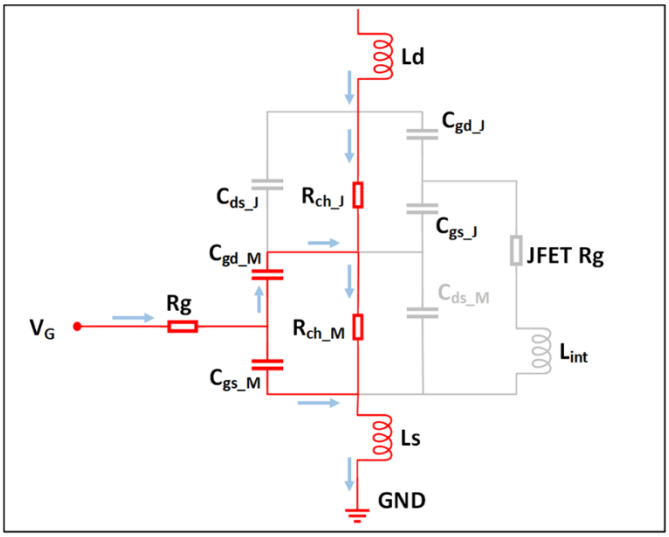
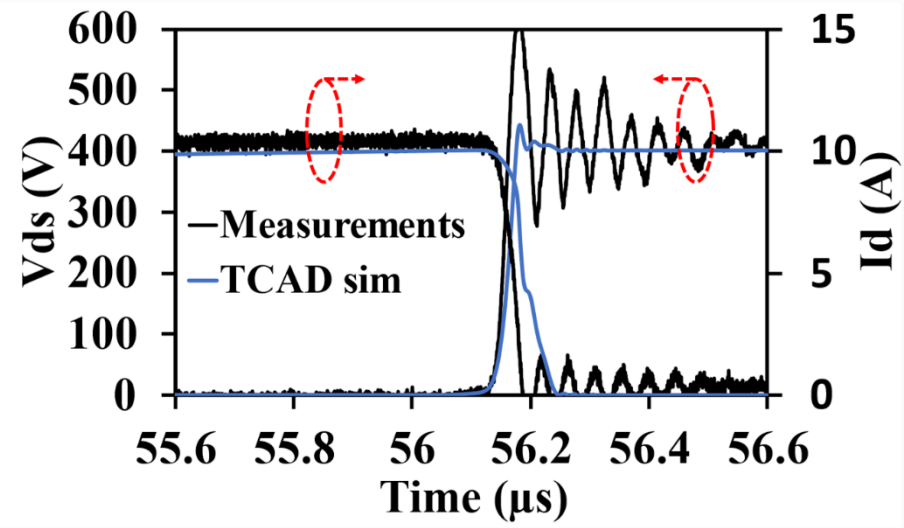


Figure 2.27 Equivalent circuit of SiC Cascode JFET during Stage 6 of turn-on.

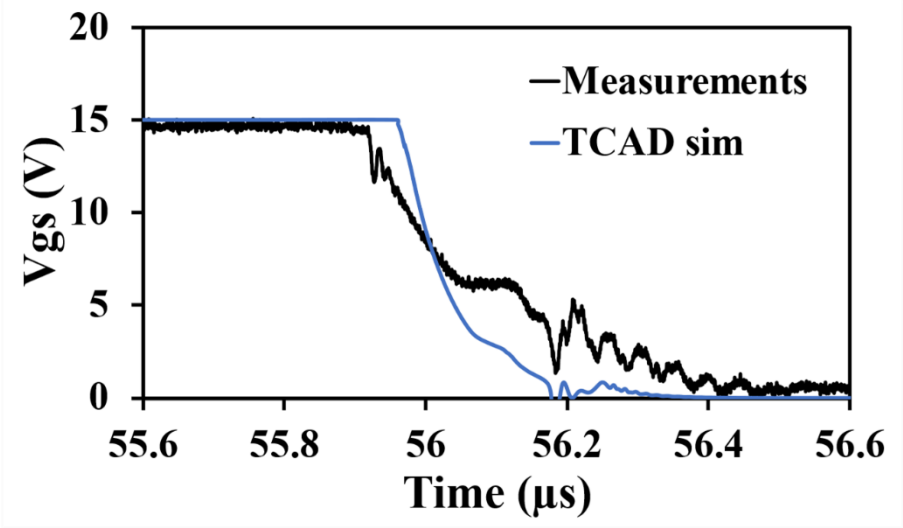
The last stage is characterised by the exponential increase of V_{gs_M} to V_G. The cascode current settles back to the inductor or load current.

Turn-off

Like the turn-on section, the SiC cascode turn off characteristics obtained experimentally and using mixed mode simulation are presented in Figure 2.28. Figure 2.29 shows the simplified and exaggerated version of the turn-off process used for the description in subsequent sections.



(a)



(b)

Figure 2.28 Experimental measurement and simulated turn-off transient in SiC cascode JFET (a) Cascode drain-source voltage and drain current (b) Gate-source Voltage.

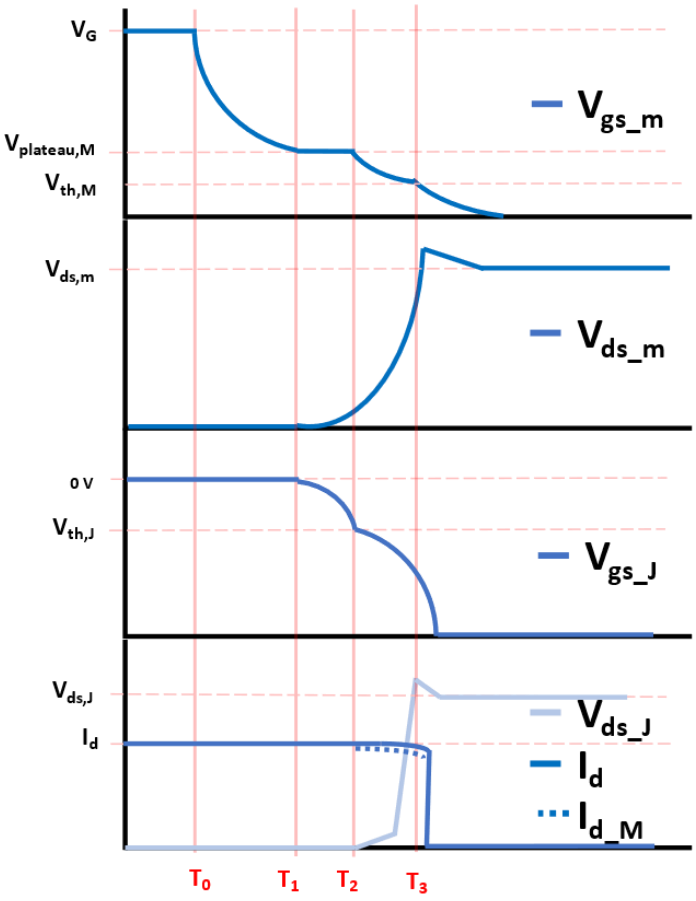


Figure 2.29 Turn-off transitions in a SiC Cascode JFET

Stage 1 ($T_0 - T_1$)

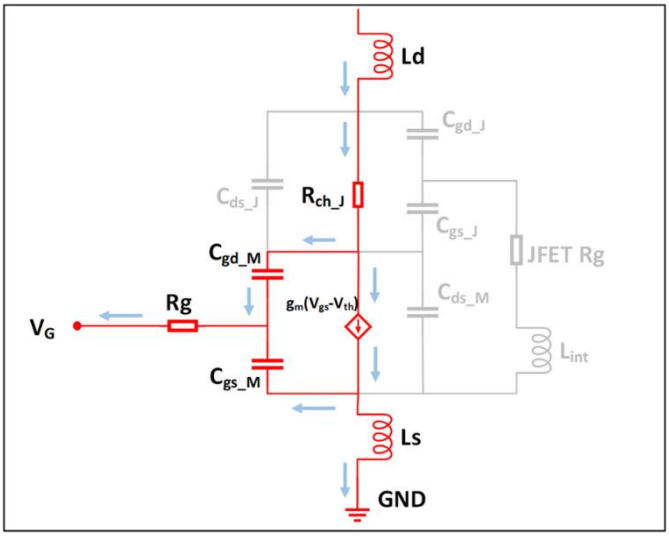


Figure 2.30 Equivalent circuit of SiC Cascode JFET during Stage 1 of turn-off.

V_G is set to zero in the first stage of turn-off causing C_{gs_M} to discharge and V_{gs_M} reduces exponentially. This stage ends when V_{gs_M} is equal to the MOSFET plateau voltage. All the other parasitic components remain unchanged with the cascode is still conducting the full load current, I_L.

Stage 2 ($T_1 - T_2$)

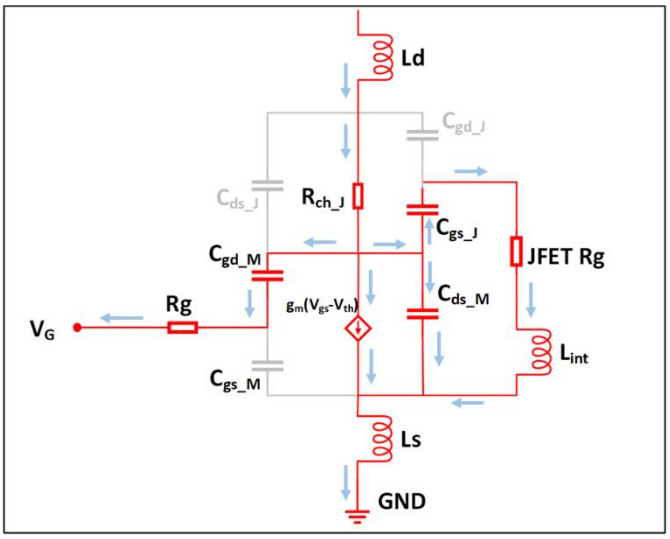


Figure 2.31 Equivalent circuit of SiC Cascode JFET during Stage 2 of turn-off.

At the start of this stage, V_{gs_M} is equal to $V_{Plateau}$. The MOS channel shrinks as the saturation current is less than I_L.

The excess current charges C_{ds_M} increasing V_{ds_M} and V_{gs_J} decreases. V_{ds_M} is in parallel with the V_{gs_J} with a phase delay introduced by L_{int}. This stage terminates when the V_{gs_J} reaches the JFET pinch off Voltage. V_{gs_M} is constant through this stage.

Stage 3 ($T_2 - T_3$)

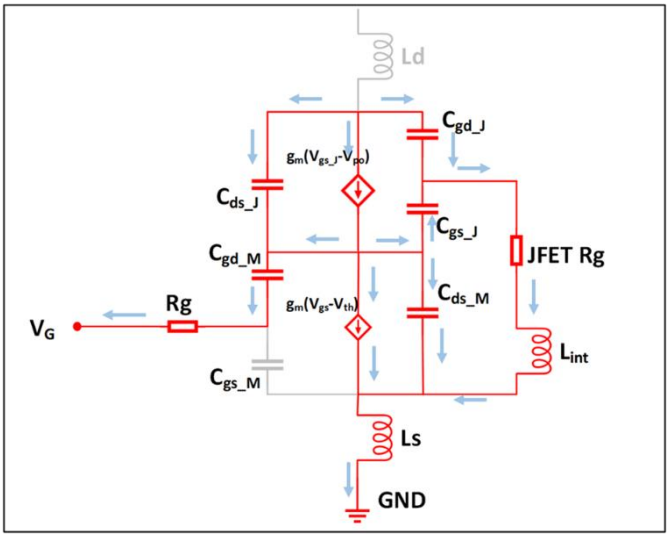


Figure 2.32 Equivalent circuit of SiC Cascode JFET during Stage 3 of turn-off.

This stage begins when V_{gs_J} reaches pinch-off and the JFET saturation current is less than I_L. Excess current from the I_L charges the JFET output capacitances (C_{gd_J} and C_{ds_J}), and the V_{ds_J} starts to increase. This voltage increasing causes a decrease in the freewheeling Diode Voltage.

The stage end when the current through the device is completely cut-off with the cascode voltage at the input Voltage (V_{DC}). V_{ds_M} reduces exponentially to the MOSFET V_{th}

Stage 4 (> T_3)

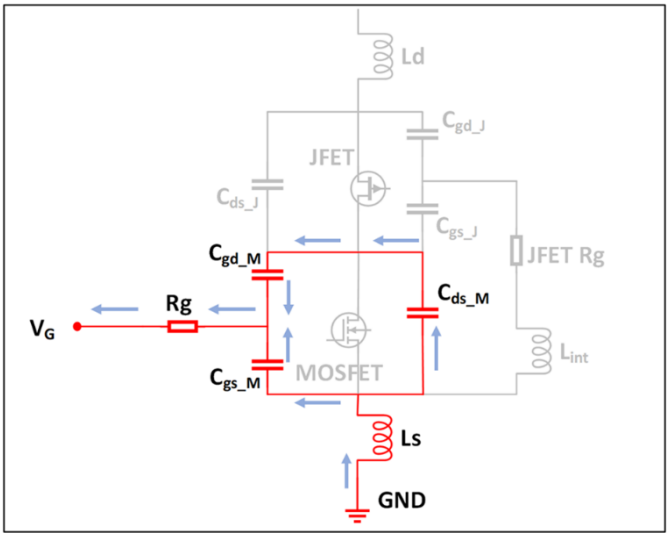


Figure 2.33 Equivalent circuit of SiC Cascode JFET during Stage 4 of turn-off.

The final stage is characterised by the complete transfer of the current to the freewheeling diode. The cascode fully turns off, and the inductor current flows through the Diode only. This stage ends when V_{gs_M} reduces to zero.

Reference

[1] Z. Li and A. Bhalla, "USCi SiC JFET Cascode and Super Cascode Technologies," in *PCIM Asia 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 26-28 June 2018 2018, pp. 1-6.

[2] A. R. Alonso, M. F. Díaz, D. G. Lamar, M. A. P. d. Azpeitia, M. M. Hernando, and J. Sebastián, "Switching Performance Comparison of the SiC JFET and SiC JFET/Si MOSFET Cascode Configuration," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2428-2440, 2014, doi: 10.1109/TPEL.2013.2283144.

[3] H. Mitlehner *et al.*, "Dynamic characteristics of high voltage 4H-SiC vertical JFETs," in *11th International Symposium on Power Semiconductor Devices and ICs. ISPSD'99 Proceedings (Cat. No.99CH36312)*: IEEE, doi: 10.1109/ispsd.1999.764129.

[4] P. Friedrichs *et al.*, "Static and Dynamic Characteristics of 4H-SiC JFETs Designed for Different Blocking Categories," *Materials Science Forum,* vol. 338-342, pp. 1243-1246, 2000-05-01 2000, doi: 10.4028/www.scientific.net/msf.338-342.1243.

[5] B. Weis, M. Braun, and P. Friedrichs, "Turn-off and short circuit behaviour of 4H SiC JFETs," in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248)*: IEEE, doi: 10.1109/ias.2001.955445.

[6] X. Li, A. Bhalla, P. Alexandrov, and L. Fursin, "Study of SiC vertical JFET behavior during unclamped inductive switching," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 16-20 March 2014 2014, pp. 2588-2592, doi: 10.1109/APEC.2014.6803668.

[7] P. Aiexandrov, A. Bhalla, Z. Li, X. Li, J. Bendel, and J. Dodge, "650V SiC cascode: A breakthrough for wide-bandgap switches," in *2016 European Conference on Silicon Carbide & Related Materials (ECSCRM)*, 25-29 Sept. 2016 2016, pp. 1-1, doi: 10.4028/www.scientific.net/MSF.897.673.

[8] X. Li, A. Bhalla, P. Alexandrov, J. Hostetler, and L. Fursin, "Investigation of SiC Stack and Discrete Cascodes," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 20-22 May 2014 2014, pp. 1-8.

[9] M. Meneghini *et al.*, "GaN-based power devices: Physics, reliability, and perspectives," *Journal of Applied Physics,* vol. 130, no. 18, p. 181101, 2021-11-14 2021, doi: 10.1063/5.0061354.

[10] J. Liu *et al.*, "1.2 kV Vertical GaN Fin JFETs with Robust Avalanche and Fast Switching Capabilities," in *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020-12-12 2020: IEEE, doi: 10.1109/iedm13553.2020.9372048.

[11] J. Liu *et al.*, "Tuning Avalanche Path in Vertical GaN JFETs By Gate Driver Design," *IEEE Transactions on Power Electronics,* vol. 37, no. 5, pp. 5433-5443, 2022-05-01 2022, doi: 10.1109/tpel.2021.3132906.

[12] R. Zhang *et al.*, "Exceptional Repetitive-Short-Circuit Robustness of Vertical GaN Fin-JFET at High Voltage," in *2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2022-05-22 2022: IEEE, doi: 10.1109/ispsd49238.2022.9813618.

[13] R. Zhang *et al.*, "Vertical GaN Fin JFET: A Power Device with Short Circuit Robustness at Avalanche Breakdown Voltage," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, 2022-03-01 2022: IEEE, doi: 10.1109/irps48227.2022.9764569.

[14] R. Zhang *et al.*, "Breakthrough Short Circuit Robustness Demonstrated in Vertical GaN Fin JFET," *IEEE Transactions on Power Electronics,* vol. 37, no. 6, pp. 6253-6258, 2022-06-01 2022, doi: 10.1109/tpel.2021.3138451.

[15] D. Ramanathan, "Re-inventing Power Electronics: NexGen Power Systems with Vertical GaN(TM)," in *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 10-12 May 2022 2022, pp. 1-8, doi: 10.30420/565822137.

[16] A. Jarndal, L. Arivazhagan, and D. Nirmal, "On the performance of GaN-on-Silicon, Silicon-Carbide, and Diamond substrates," *International Journal of RF and Microwave Computer-Aided Engineering,* vol. 30, no. 6, p. e22196, 2020, doi: https://doi.org/10.1002/mmce.22196.

[17] B. Setera and A. Christou, "Threading dislocations in GaN high-voltage switches," *Microelectronics Reliability,* vol. 124, p. 114336, 2021/09/01/ 2021, doi: https://doi.org/10.1016/j.microrel.2021.114336.

[18] Z. Islam, A. Haque, and N. Glavin, "Real-time visualization of GaN/AlGaN high electron mobility transistor failure at off-state," *Applied Physics Letters,* vol. 113, no. 18, p. 183102, 2018, doi: 10.1063/1.5046178.

[19] T. Kimoto, "2 - SiC material properties," in *Wide Bandgap Semiconductor Power Devices*, B. J. Baliga Ed.: Woodhead Publishing, 2019, pp. 21-42.

[20] T. T. Mnatsakanov, M. E. Levinshtein, L. I. Pomortseva, S. N. Yurkov, G. S. Simin, and M. Asif Khan, "Carrier mobility model for GaN," *Solid-State Electronics,* vol. 47, no. 1, pp. 111-115, 2003/01/01/ 2003, doi: https://doi.org/10.1016/S0038-1101(02)00256-3.

[21] W. Saito and T. Naka, "Relation between UIS withstanding capability and I-V characteristics in high-voltage GaN-HEMTs," *Microelectronics Reliability,* vol. 76-77, pp. 309-313, 2017/09/01/ 2017, doi: https://doi.org/10.1016/j.microrel.2017.07.009.

[22] J. P. Kozak, R. Zhang, J. Liu, Q. Song, M. Xiao, and Y. Zhang, "Hard-Switched Overvoltage Robustness of p-Gate GaN HEMTs at Increasing Temperatures," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020-10-11 2020: IEEE, doi: 10.1109/ecce44975.2020.9235461.

[23] R. Zhang, J. P. Kozak, M. Xiao, J. Liu, and Y. Zhang, "Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs," *IEEE Transactions on Power Electronics,* vol. 35, no. 12, pp. 13409-13419, 2020-12-01 2020, doi: 10.1109/tpel.2020.2993982.

[24] R. Zhang, J. P. Kozak, Q. Song, M. Xiao, J. Liu, and Y. Zhang, "Dynamic Breakdown Voltage of GaN Power HEMTs," in *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020-12-12 2020: IEEE, doi: 10.1109/iedm13553.2020.9371904.

[25] R. Zhang, J. P. Kozak, J. Liu, M. Xiao, and Y. Zhang, "Surge Energy Robustness of GaN Gate Injection Transistors," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 2020-04-01 2020: IEEE, doi: 10.1109/irps45951.2020.9129324.

[26] J. P. Kozak, Q. Song, R. Zhang, J. Liu, and Y. Zhang, "Robustness of GaN Gate Injection Transistors under Repetitive Surge Energy and Overvoltage," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021-03-01 2021: IEEE, doi: 10.1109/irps46558.2021.9405173.

[27] J. P. Kozak, R. Zhang, Q. Song, J. Liu, W. Saito, and Y. Zhang, "True Breakdown Voltage and Overvoltage Margin of GaN Power HEMTs in Hard Switching," *IEEE Electron Device Letters,* vol. 42, no. 4, pp. 505-508, 2021-04-01 2021, doi: 10.1109/led.2021.3063360.

[28] P. J. Martínez, S. Letz, E. Maset, and D. Zhao, "Failure analysis of normally-off GaN HEMTs under avalanche conditions," *Semiconductor Science and Technology,* vol. 35, no. 3, p. 035007, 2020/02/11 2020, doi: 10.1088/1361-6641/ab6bad.

[29] S. Liu *et al.*, "Single Pulse Unclamped-Inductive-Switching Induced Failure and Analysis for 650 V p-GaN HEMT," *IEEE Transactions on Power Electronics,* vol. 35, no. 11, pp. 11328-11331, 2020-11-01 2020, doi: 10.1109/tpel.2020.2988976.

[30] J. Marek *et al.*, "Impact of repetitive UIS on modern GaN power devices," in *2016 11th International Conference on Advanced Semiconductor Devices & Microsystems (ASDAM)*, 13-16 Nov. 2016 2016, pp. 173-176, doi: 10.1109/ASDAM.2016.7805923.

[31] J. Kozarik, J. Marek, M. Jagelka, L. Cernaj, A. Chvala, and D. Donoval, "Power P-GaN HEMT Under Single and Multi-Pulse UIS Conditions," in *2018 12th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)*, 2018-10-01 2018: IEEE, doi: 10.1109/asdam.2018.8544555.

[32] X. Huang *et al.*, "Experimental study of 650V AlGaN/GaN HEMT short-circuit safe operating area (SCSOA)," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2014-06-01 2014: IEEE, doi: 10.1109/ispsd.2014.6856029.

[33] H. Li *et al.*, "Robustness of 650-V Enhancement-Mode GaN HEMTs Under Various Short-Circuit Conditions," *IEEE Transactions on Industry Applications,* vol. 55, no. 2, pp. 1807-1816, 2019-03-01 2019, doi: 10.1109/tia.2018.2879289.

[34] R. Chen, Z. Yang, and F. Wang, "Overcurrent and Short-circuit Capability Experimental Investigation for GaN HEMT at Cryogenic Temperature," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021-06-14 2021: IEEE, doi: 10.1109/apec42165.2021.9487188.

[35] O. Alatise, A. Deb, E. Bashar, J. Ortiz Gonzalez, S. Jahdi, and W. Issa, "A Review of Power Electronic Devices for Heavy Goods Vehicles Electrification: Performance and Reliability," *Energies,* vol. 16, no. 11, p. 4380, 2023-05-28 2023, doi: 10.3390/en16114380.

[36] C. Abbate, G. Busatto, A. Sanseverino, D. Tedesco, and F. Velardi, "Failure analysis of 650 V enhancement mode GaN HEMT after short circuit tests," *Microelectronics Reliability,* vol. 88-90, pp. 677-683, 2018/09/01/ 2018, doi: https://doi.org/10.1016/j.microrel.2018.07.071.

[37] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Robustness of Cascode GaN HEMTs under Repetitive Overvoltage and Surge Energy Stresses," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021-06-14 2021: IEEE, doi: 10.1109/apec42165.2021.9487252.

[38] Q. Song, R. Zhang, J. Kozak, J. Liu, Q. Li, and Y. Zhang, "Robustness of Cascode GaN HEMTs in Unclamped Inductive Switching," *IEEE Transactions on Power Electronics,* vol. 37, no. 4, pp. 4148-4160, 2022-04-01 2022, doi: 10.1109/tpel.2021.3122740.

[39] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and Reliability Review of 650V and 900V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," *IEEE Transactions on Industrial Electronics,* pp. 1-1, 2019, doi: 10.1109/TIE.2019.2945299.

[40] A. Fayyaz, L. Yang, M. Riccio, A. Castellazzi, and A. Irace, "Single pulse avalanche robustness and repetitive stress ageing of SiC power MOSFETs," *Microelectronics Reliability,* vol. 54, no. 9, pp. 2185-2190, 2014/09/01/ 2014, doi: https://doi.org/10.1016/j.microrel.2014.07.078.

[41] C. DiMarino and B. Hull, "Characterization and prediction of the avalanche performance of 1.2 kV SiC MOSFETs," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2-4 Nov. 2015 2015, pp. 263-267, doi: 10.1109/WiPDA.2015.7369294.

[42] P. Alexakis, O. Alatise, J. Hu, S. Jahdi, L. Ran, and P. A. Mawby, "Improved Electrothermal Ruggedness in SiC MOSFETs Compared With Silicon IGBTs," *IEEE Transactions on Electron Devices,* vol. 61, no. 7, pp. 2278-2286, 2014, doi: 10.1109/TED.2014.2323152.

[43] N. Ren, H. Hu, K. L. Wang, Z. Zuo, R. Li, and K. Sheng, "Investigation on single pulse avalanche failure of 900V SiC MOSFETs," in *2018 IEEE 30th International Symposium*

on Power Semiconductor Devices and ICs (ISPSD), 13-17 May 2018 2018, pp. 431-434, doi: 10.1109/ISPSD.2018.8393695.

[44] V. Pala, B. Hull, J. Richmond, P. Butler, S. Allen, and J. Palmour, "Methodology to qualify silicon carbide MOSFETs for single shot avalanche events," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2-4 Nov. 2015 2015, pp. 56-59, doi: 10.1109/WiPDA.2015.7369276.

[45] A. Fayyaz *et al.*, "UIS failure mechanism of SiC power MOSFETs," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 7-9 Nov. 2016 2016, pp. 118-122, doi: 10.1109/WiPDA.2016.7799921.

[46] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, "SiC power MOSFETs performance, robustness and technology maturity," *Microelectronics Reliability,* vol. 58, pp. 164-176, 2016/03/01/ 2016, doi: https://doi.org/10.1016/j.microrel.2015.12.034.

[47] M. D. Kelley, B. N. Pushpakaran, and S. B. Bayne, "Single-Pulse Avalanche Mode Robustness of Commercial 1200 V/80 mΩ SiC MOSFETs," *IEEE Transactions on Power Electronics,* vol. 32, no. 8, pp. 6405-6415, 2017, doi: 10.1109/TPEL.2016.2621099.

[48] I. Dchar, M. Zolkos, C. Buttay, and H. Morel, "Robustness of SiC MOSFET under avalanche conditions," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 26-30 March 2017 2017, pp. 2263-2268, doi: 10.1109/APEC.2017.7931015.

[49] J. Wei, S. Liu, S. Li, J. Fang, T. Li, and W. Sun, "Comprehensive Investigations on Degradations of Dynamic Characteristics for SiC Power MOSFETs Under Repetitive Avalanche Shocks," *IEEE Transactions on Power Electronics,* vol. 34, no. 3, pp. 2748-2757, 2019, doi: 10.1109/TPEL.2018.2843559.

[50] T. Nguyen, A. Ahmed, T. V. Thang, and J. Park, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Transactions on Power Electronics,* vol. 30, no. 5, pp. 2445-2455, 2015, doi: 10.1109/TPEL.2014.2353417.

[51] J. O. Gonzalez and O. Alatise, "Impact of the Gate Oxide Reliability of SiC MOSFETs on the Junction Temperature Estimation Using Temperature Sensitive Electrical Parameters," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 23-27 Sept. 2018 2018, pp. 837-844, doi: 10.1109/ECCE.2018.8557810.

[52] H. Yano, N. Kanafuji, A. Osawa, T. Hatayama, and T. Fuyuki, "Threshold Voltage Instability in 4H-SiC MOSFETs With Phosphorus-Doped and Nitrided Gate Oxides," *IEEE Transactions on Electron Devices,* vol. 62, no. 2, pp. 324-332, 2015, doi: 10.1109/TED.2014.2358260.

[53] J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018/09/01/ 2018, doi: https://doi.org/10.1016/j.microrel.2018.06.045.

[54] J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC mosfets," *IEEE Transactions on Power Electronics,* vol. 34, no. 6, pp. 5737-5747, 2019, doi: 10.1109/TPEL.2018.2870067.

[55] Z. Chbili *et al.*, "Modeling Early Breakdown Failures of Gate Oxide in SiC Power MOSFETs," *IEEE Transactions on Electron Devices,* vol. 63, no. 9, pp. 3605-3613, 2016, doi: 10.1109/TED.2016.2586483.

[56] M. Dang Luong, "The cascode JFET as a means to avoid excess gate current," *IEEE Transactions on Electron Devices,* vol. 18, no. 8, pp. 603-604, 1971, doi: 10.1109/T-ED.1971.17248.

[57] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," *IEEE Transactions on Industrial Electronics,* vol. 67, no. 9, pp. 7375-7385, 2020, doi: 10.1109/TIE.2019.2945299.

[58] J. Ortiz Gonzalez, R. Wu, S. N. Agbo, and O. Alatise, "Robustness and reliability review of Si and SiC FET devices for more-electric-aircraft applications," *Microelectronics Reliability,* vol. 100-101, p. 113324, 2019/09/01/ 2019, doi: https://doi.org/10.1016/j.microrel.2019.06.016.

[59] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability," *IEEE Transactions on Electron Devices,* vol. 66, no. 11, pp. 4604-4616, 2019, doi: 10.1109/TED.2019.2938262.

[60] M. Beier-Moebius and J. Lutz, "Breakdown of Gate Oxide of SiC-MOSFETs and Si-IGBTs under High Temperature and High Gate Voltage," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 16-18 May 2017 2017, pp. 1-8.

[61] J. O. Gonzalez and O. Alatise, "Bias Temperature Instability and Junction Temperature Measurement Using Electrical Parameters in SiC Power MOSFETs," *IEEE Transactions on Industry Applications,* vol. 57, no. 2, pp. 1664-1676, 2021, doi: 10.1109/TIA.2020.3045120.

[62] Y. Gunaydin *et al.*, "Impact of Temperature and Switching Rate on Forward and Reverse Conduction of GaN and SiC Cascode devices: A Technology Evaluation," in *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*, 15-17 Dec. 2020 2020, vol. 2020, pp. 782-787, doi: 10.1049/icp.2021.1067.

[63] A. Bhalla, "Origins of SiC FETs and their evolution towards the perfect switch," 2021. [Online]. Available: https://unitedsic.com/whitepaper/Origins-of-SiC-FETs-and-their-evolution-towards-the-perfect-switch.pdf

[64] R. Wu, J. O. Gonzalez, Z. Davletzhanova, P. A. Mawby, and O. Alatise, "The Potential of SiC Cascode JFETs in Electric Vehicle Traction Inverters," *IEEE Transactions on Transportation Electrification,* vol. 5, no. 4, pp. 1349-1359, 2019, doi: 10.1109/TTE.2019.2954654.

[65] A. Bhalla, X. Li, and J. Dodge, "Circuit Protection with SiC FETs in dual-gate configuration," in *PCIM Asia 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 9-11 Sept. 2021 2021, pp. 1-8.

[66] T. Friedli, S. D. Round, and J. W. Kolar, "A 100 kHz SiC Sparse Matrix Converter," in *2007 IEEE Power Electronics Specialists Conference*, 2007-01-01 2007: IEEE, doi: 10.1109/pesc.2007.4342340.

[67] A. Vazquez, A. Rodriguez, M. Fernandez, M. M. Hernando, and J. Sebastian, "On the use of front-end cascode rectifiers based on normally-on SiC JFET and Si MOSFET," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013-03-01 2013: IEEE, doi: 10.1109/apec.2013.6520546.

[68] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage 25 kW, 50 kHz DC-DC converter based on SiC JFETs," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, 2008-02-01 2008: IEEE, doi: 10.1109/apec.2008.4522813.

[69] J. Biela, D. Aggeler, D. Bortis, and J. W. Kolar, "Balancing Circuit for a 5-kV/50-ns Pulsed-Power Switch Based on SiC-JFET Super Cascode," *IEEE Transactions on Plasma Science,* vol. 40, no. 10, pp. 2554-2560, 2012-10-01 2012, doi: 10.1109/tps.2011.2169090.

[70] R. W. D. D. S. Cui, "Series-Connected SiC JFETs as High-Voltage Switch," 2017.

[71] A. Bhalla, "The Cascode's Vital Role in the Success of SiC; And There's Still More to Come," ed: UnitedSiC, 2018.

[72] S. S. Alharbi and M. Matin, "Transformer-less High-Gain DC-DC Converter with SiC Cascode JFETs for High-Voltage Applications," in *2018 IEEE International Power*

Modulator and High Voltage Conference (IPMHVC), 3-7 June 2018 2018, pp. 37-41, doi: 10.1109/IPMHVC.2018.8936777.

[73] U. Mehrotra, B. Ballard, and D. C. Hopkins, "High Current Medium Voltage Bidirectional Solid State Circuit Breaker using SiC JFET Super Cascode," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 11-15 Oct. 2020 2020, pp. 6049-6056, doi: 10.1109/ECCE44975.2020.9236347.

[74] J. Liu, G. Zhang, B. Wang, W. Li, and J. Wang, "Gate Failure Physics of SiC MOSFETs Under Short-Circuit Stress," *IEEE Electron Device Letters,* vol. 41, no. 1, pp. 103-106, 2020, doi: 10.1109/LED.2019.2953235.

[75] P. D. Reigosa, F. Iannuzzo, H. Luo, and F. Blaabjerg, "A Short-Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules," *IEEE Transactions on Industry Applications,* vol. 53, no. 3, pp. 2880-2887, 2017, doi: 10.1109/TIA.2016.2628895.

[76] A. Agarwal, A. Kanale, K. Han, B. J. Baliga, and S. Bhattacharya, "Impact of Gate Oxide Thickness on Switching and Short Circuit Performance of 1200 V 4H-SiC Inversion-channel MOSFETs," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 29-31 Oct. 2019 2019, pp. 59-62, doi: 10.1109/WiPDA46397.2019.8998839.

[77] X. Chen *et al.*, "Investigation on Short-Circuit Characterization and Optimization of 3.3-kV SiC MOSFETs," *IEEE Transactions on Electron Devices,* vol. 68, no. 1, pp. 184-191, 2021, doi: 10.1109/TED.2020.3037262.

[78] K. Tani, J. i. Sakano, and A. Shima, "Analysis of short-circuit break-down point in 3.3 kV SiC-MOSFETs," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 13-17 May 2018 2018, pp. 383-386, doi: 10.1109/ISPSD.2018.8393683.

[79] R. Bonyadi *et al.*, "Compact Electrothermal Reliability Modeling and Experimental Characterization of Bipolar Latchup in SiC and CoolMOS Power MOSFETs," *IEEE Transactions on Power Electronics,* vol. 30, no. 12, pp. 6978-6992, 2015, doi: 10.1109/TPEL.2015.2388512.

[80] D. Marroqui, A. Garrigos, J. M. Blanes, R. Gutierrez, E. Maset, and F. Iannuzzo, "SiC MOSFET vs SiC/Si Cascode short circuit robustness benchmark," *Microelectronics Reliability,* vol. 100-101, p. 113429, 2019, doi: 10.1016/j.microrel.2019.113429.

[81] X. Li, A. Bhalla, and P. Alexandrov, "Short-Circuit Capability of SiC Cascode," *Materials Science Forum,* vol. 924, pp. 871-874, 2017, doi: 10.4028/www.scientific.net/MSF.924.871.

[82] S. N. Agbo, J. Ortiz Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "UIS performance and ruggedness of stand-alone and cascode SiC JFETs," *Microelectronics Reliability,* vol. 114, p. 113803, 2020/11/01/ 2020, doi: https://doi.org/10.1016/j.microrel.2020.113803.

[83] S. N. Agbo, J. Ortiz-Gonzalez, and O. Alatise, "Performance of SiC cascode JFETs under single and repetitive avalanche pulses," *Microelectronics Reliability,* vol. 110, p. 113644, 2020, doi: 10.1016/j.microrel.2020.113644.

[84] B. J. Baliga, "Material Properties and Transport Physics," in *Fundamentals of Power Semiconductor Devices*, B. J. Baliga Ed. Cham: Springer International Publishing, 2019, pp. 23-87.

[85] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proceedings of the IEEE,* vol. 55, no. 12, pp. 2192-2193, 1967, doi: 10.1109/PROC.1967.6123.

[86] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 7, no. 11, pp. 1164-1171, 1988-01-01 1988, doi: 10.1109/43.9186.

[87] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Physical Review,* vol. 87, no. 5, pp. 835-842, 1952-09-01 1952, doi: 10.1103/physrev.87.835.
[88] R. N. Hall, "Electron-Hole Recombination in Germanium," *Physical Review,* vol. 87, no. 2, pp. 387-387, 1952-07-15 1952, doi: 10.1103/physrev.87.387.
[89] W. S. Loh *et al.*, "Impact Ionization Coefficients in 4H-SiC," *IEEE Transactions on Electron Devices,* vol. 55, no. 8, pp. 1984-1990, 2008, doi: 10.1109/TED.2008.926679.
[90] S. DIONYSIOS, "Development of silicon carbide (SiC) micro vertical transverse field effect transistors," 2018.
[91] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, "Ionization rates and critical fields in 4H silicon carbide," *Applied Physics Letters,* vol. 71, no. 1, pp. 90-92, 1997, doi: 10.1063/1.119478.
[92] R. Raghunathan and B. J. Baliga, "Measurement of electron and hole impact ionization coefficients for SiC," in *Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's*, 26-29 May 1997 1997, pp. 173-176, doi: 10.1109/ISPSD.1997.601463.
[93] E. Bellotti, H.-E. Nilsson, K. F. Brennan, P. P. Ruden, and R. Trew, "Monte Carlo calculation of hole initiated impact ionization in 4H phase SiC," *Journal of Applied Physics,* vol. 87, no. 8, pp. 3864-3871, 2000, doi: 10.1063/1.372426.
[94] M. Hjelm, H.-E. Nilsson, A. Martinez, K. F. Brennan, and E. Bellotti, "Monte Carlo study of high-field carrier transport in 4H-SiC including band-to-band tunneling," *Journal of Applied Physics,* vol. 93, no. 2, pp. 1099-1107, 2002, doi: 10.1063/1.1530712.
[95] H. E. Nilsson, A. Martinez, U. Sannemo, M. Hjelm, E. Bellotti, and K. Brennan, "Monte Carlo simulation of high field hole transport in 4H–SiC including band to band tunneling and optical interband transitions," *Physica B: Condensed Matter,* vol. 314, no. 1, pp. 68-71, 2002/03/01/ 2002, doi: https://doi.org/10.1016/S0921-4526(01)01356-4.
[96] A. Akturk, N. Goldsman, S. Potbhare, and A. Lelis, "High field density-functional-theory based Monte Carlo: 4H-SiC impact ionization and velocity saturation," *Journal of Applied Physics,* vol. 105, no. 3, 2009, doi: 10.1063/1.3074107.
[97] T. Hatakeyama, "Measurements of impact ionization coefficients of electrons and holes in 4H-SiC and their application to device simulation," *physica status solidi (a),* vol. 206, no. 10, pp. 2284-2294, 2009, doi: https://doi.org/10.1002/pssa.200925213.
[98] D. M. Nguyen *et al.*, "OBIC Measurements on Avalanche Diodes in 4H-SiC for the Determination of Impact Ionization Coefficients," *Materials Science Forum,* vol. 717-720, pp. 545-548, 2012, doi: 10.4028/www.scientific.net/MSF.717-720.545.
[99] H. Niwa, J. Suda, and T. Kimoto, "Temperature Dependence of Impact Ionization Coefficients in 4H-SiC," *Materials Science Forum,* vol. 778-780, pp. 461-466, 2014, doi: 10.4028/www.scientific.net/MSF.778-780.461.
[100] A. Tsibizov, I. Kovacevic-Badstubner, B. Kakarla, and U. Grossner, "Accurate Temperature Estimation of SiC Power mosfets Under Extreme Operating Conditions," *IEEE Transactions on Power Electronics,* vol. 35, no. 2, pp. 1855-1865, 2020-02-01 2020, doi: 10.1109/tpel.2019.2917221.
[101] L. Hitova, R. Yakimova, E. P. Trifonova, A. Lenchev, and E. Janzen, "Heat Capacity of 4H-SiC Determined by Differential Scanning Calorimetry," *Journal of The Electrochemical Society,* vol. 147, no. 9, p. 3546, 2000-01-01 2000, doi: 10.1149/1.1393935.
[102] A. Bhalla, X. Li, and J. Bendel, "Switching Behavior of USCi ' s SiC Cascodes," 2016.

Chapter 3. AVALANCHE IN CASCODE JFET

3.1. Introduction to Unclamped Inductive Switching (UIS)

SiC MOSFETs are now an established power device technology competing with silicon MOSFETs and IGBTs in the 650 V to 1200 V application space [1]. As stated in previous chapters, improved energy conversion efficiency is widely cited as a benefit of SiC devices along with high temperature operation and fast switching rates, the reliability and robustness of SiC devices is however increasingly under scrutiny. SiC MOSFETs are well known for good avalanche performance in comparison with silicon MOSFETs and IGBTs [2-10]. This is due to the wide bandgap and high critical electric field characteristics of SiC which means more energy is required to generate electron-hole pairs through impact ionization [9]. SiC can sustain higher electric field and therefore a reduced rate of impact ionization. Although SiC MOSFETs have smaller active areas and higher junction-to-case transient thermal impedance, they are nevertheless very rugged under single and repetitive avalanche cycling. However, SiC devices continue to have reliability challenges regarding the performance of the gate oxide under short circuits [11, 12], threshold voltage shift from bias temperature instability [13-16] and time dependent dielectric breakdown [17]. Stand-alone SiC JFETs have negative threshold voltages and therefore operate in depletion mode with high gate leakage currents. Since this is not suitable for traditional power electronics that use normally-OFF devices with low standby gate currents, SiC JFETs were not widely accepted by the industry.

Failure of power devices under UIS conditions is dependent on the structure of the device. The structure and equivalent circuits of a conventional planar MOSFET and a conventional planar IGBT is shown in Figure 3.1 (a) and Figure 3.1 (b) illustrating the parasitic mechanisms responsible for failure under UIS. When conventional MOSFETs fail under UIS, it is either due to parasitic BJT latch-up with temperature/current hot-spots [18] or average junction temperature rise exceeding the device thermal limits. The first failure mode is associated with short duration and high-power avalanche pulses (where there is insufficient time for heat to diffuse from the junction) while the second failure mode is associated with low power and long duration avalanche pulses (where there is sufficient time for heat flow from the junction to the case). Figure 3.2 (a) and (b) show the different current paths in a conventional MOSFET during normal conduction and avalanche conduction respectively. The failure

current path through the parasitic BJT because of latch up is illustrated using red arrows in Figure 3.2 (b). Failure modes of power MOSFETs under repetitive avalanche are different from those under single-shot avalanche. Under repetitive avalanche conditions, degradation of the gate oxide due to hot-carrier-injection has been reported in SiC MOSFETs [2, 11, 20-22]. The failure of IGBTs under single shot UIS presents is reported to occur in two different ways also, high-current avalanche and low-current avalanche [19]. With high current avalanche, there is a latch up of the parasitic NPN like the case in MOSFETs. At low current avalanche, the failure is a latch up of the parasitic thyristor, this is due to a positive feedback effect which leads to the parasitic thyristor operating in the on-state and hence catastrophic failure. Figure 3.3 (a) shows the current path in an IGBT during normal conduction, and Figure 3.3 (b) demonstrates the avalanche current path illustrating the thyristor latch up mechanism.

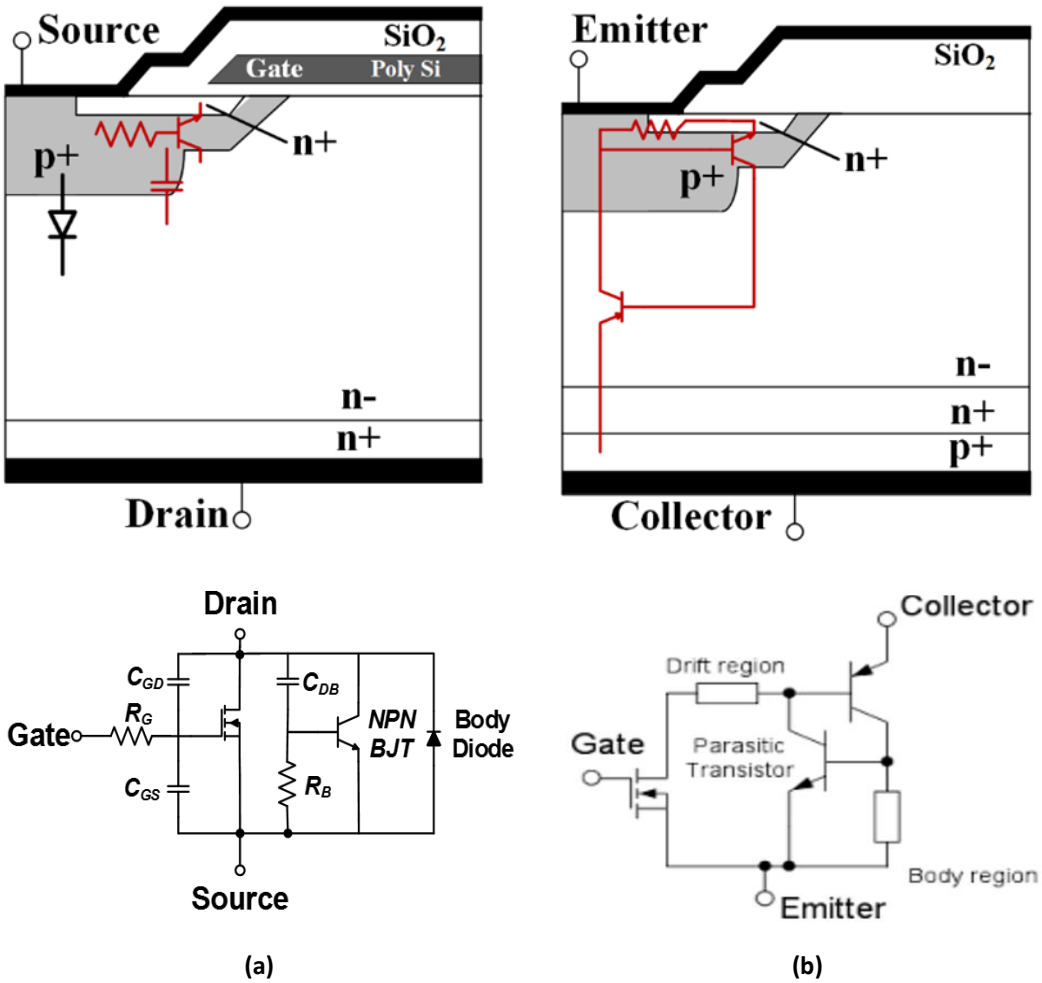


Figure 3.1 Conventional planar power device structures showing their parasitics (a) Planar MOSFET structure with parasitic BJT(top), MOSFET equivalent circuit with parasitics (bottom) (b) Planar IGBT structure with parasitic thyristor(top) IGBT equivalent circuit with parasitics (bottom)

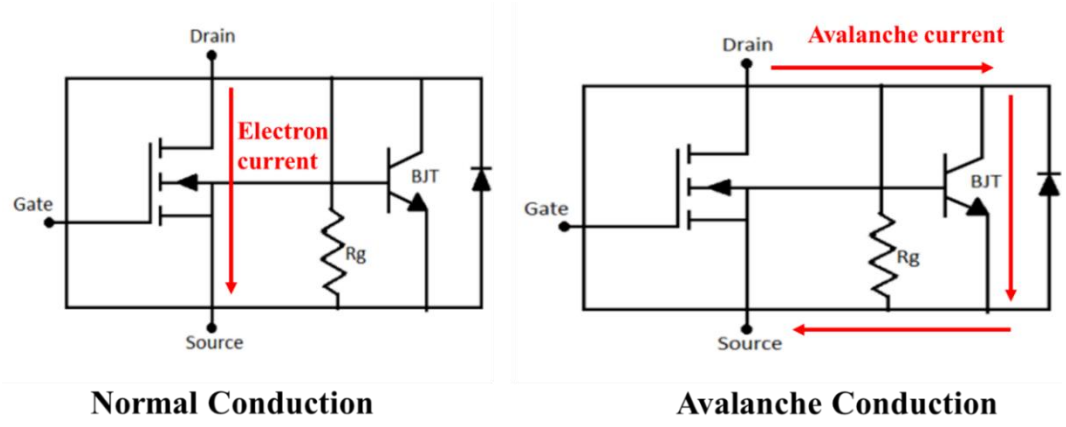


Figure 3.2 Current path in conventional MOSFETs during (a) Normal conduction (b) Avalanche conduction

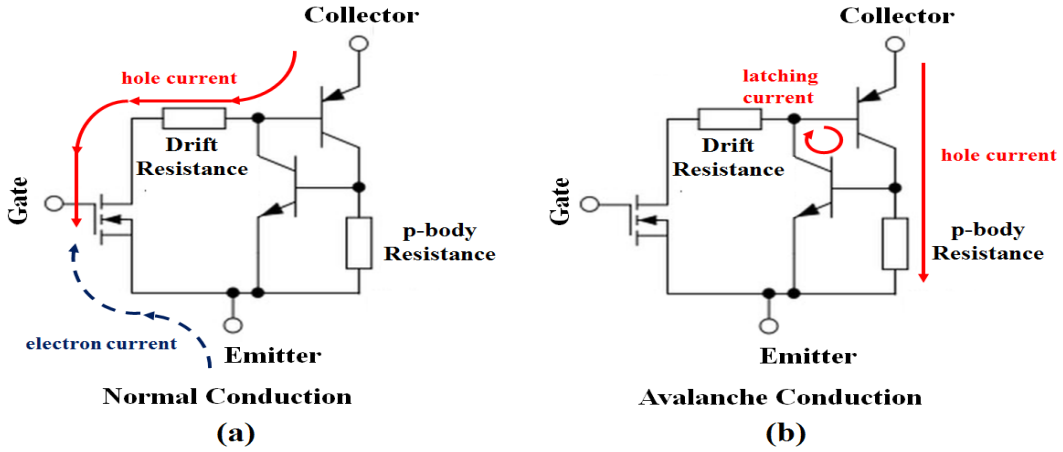
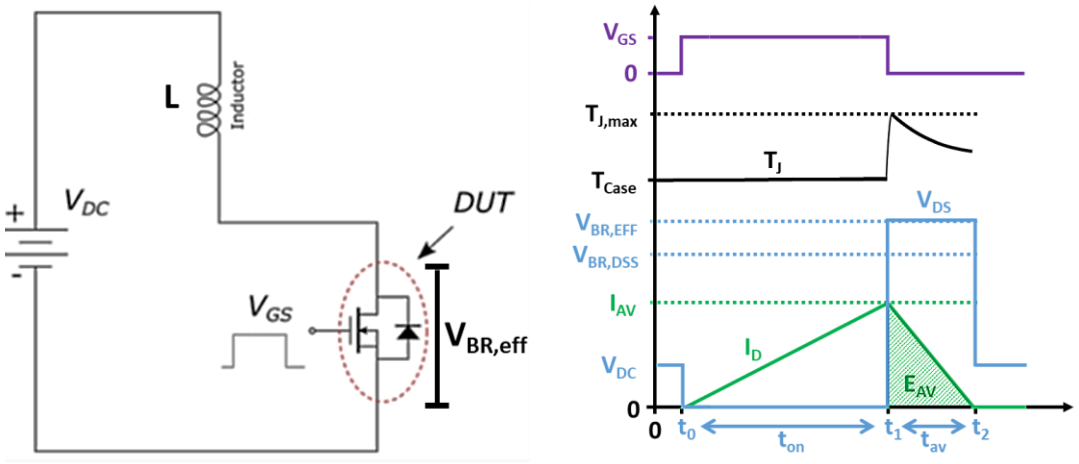


Figure 3.3 Current path in conventional IGBTs during (a) Normal conduction (b) Avalanche conduction

Less is known about how the SiC Cascode JFET fails in single or repetitive avalanche. Therefore, the failure modes and peculiarities of SiC Cascode JFETs under single and repetitive pulses of unclamped inductive switching (UIS) is investigated in this chapter. The theory guiding the behaviour of devices during UIS is derived in section 3.2. In section 3.3, experimental measurements of the avalanche characteristics in SiC Trench MOSFETs and Cascode JFETs under UIS are shown, and the difference in their failure modes is explained. In section 3.4, results of UIS in SiC standalone JFETs is presented displaying similar trends as the UIS characteristics in SiC cascode JFET. Section 3.5 presents the UIS performance of SiC cascode JFETs benchmarked against other power devices. In section 3.6, we discuss the results and introduce failure-analysis techniques used for analysing SiC Cascode JFETs. In Section 3.7, finite element simulations from SILVACO TCAD are presented to explain the failure mode in SiC Cascode JFETs. In section 3.8, the performance of the devices under repetitive UIS is presented, while section 3.9 concludes this chapter.

3.2. UIS theory



(a) (b)

Figure 3.4(a) Conventional UIS circuit (b) Typical avalanche characteristics, top-V_{GS}; middle-Junction Temperature; bottom-I_D,V_{DS}

The theory and equations guiding the behaviour of devices during UIS is well known and is derived by applying Kirchhoff's Voltage Law (KVL) to the UIS test circuit. A typical UIS circuit and avalanche characteristics are presented in Figure 3.4. Applying KVL in the circuit during turn-off yields,

$$V_{BR,eff} = L\frac{di}{dt} + V_{DC}$$

Eq. 3.1

Where $V_{BR,eff}$ is effective drain-to-source breakdown voltage at peak discharge current, L is the Load inductance, di/dt is the rate of change of current at turn-off, and V_{DC} is the supply voltage. From the above equation the avalanche duration or time in avalanche can be deduced as follows,

$$L\frac{dI}{dt} = V_{BR,eff} - V_{DC}$$

$$\int_0^{I_{av}} dI = \int_{t_1}^{t_2} \frac{V_{BR,eff} - V_{DC}}{L}\,dt = \frac{V_{BR,eff} - V_{DC}}{L}(t_2 - t_1)$$

$$I_{av} = \frac{V_{BR,eff} - V_{DC}}{L}\,t_{av}$$

Eq. 3.2

Where t_1 is the start of avalanche, t_2 is the end of avalanche, $t_{av} = t_2 - t_1$ (avalanche duration), and I_{av} is the peak current being discharged. Hence, avalanche duration is,

$$t_{av} = \frac{I_{av} \cdot L}{V_{BR,eff} - V_{DC}}$$

Eq. 3.3

The avalanche power dissipated by the DUT is given by,

$$P = VI = V_{BR,eff}\left(\frac{V_{BR,eff} - V_{DC}}{L}\right)t_{av}$$

Eq. 3.4

Integrating the power over the avalanche duration gives the avalanche energy (E_{AV}) below,

$$E_{av} = \int_{t_1}^{t_2} P.dt = \int_{t_1}^{t_2} V_{BR,eff}\left(\frac{V_{BR,eff} - V_{DC}}{L}\right)t_{av}.dt$$

$$E_{av} = \frac{V_{BR,eff}}{2}\left(\frac{V_{BR,eff} - V_{DC}}{L}\right)t_{av}(t_2 - t_1) = \frac{V_{BR,eff}}{2}\left(\frac{V_{BR,eff} - V_{DC}}{L}\right)t_{av}^2$$

$$E_{av} = \frac{1}{2}V_{BR,eff}I_{av}t_{av}$$

Eq. 3.5

Using the equation for avalanche duration in Eq. 3.3, the avalanche energy is as follows,

$$E_{av} = \frac{1}{2}\left[\frac{V_{BR,eff}}{V_{BR,eff} - V_{DC}}\right]\mathrm{I}_{av}^2 L$$

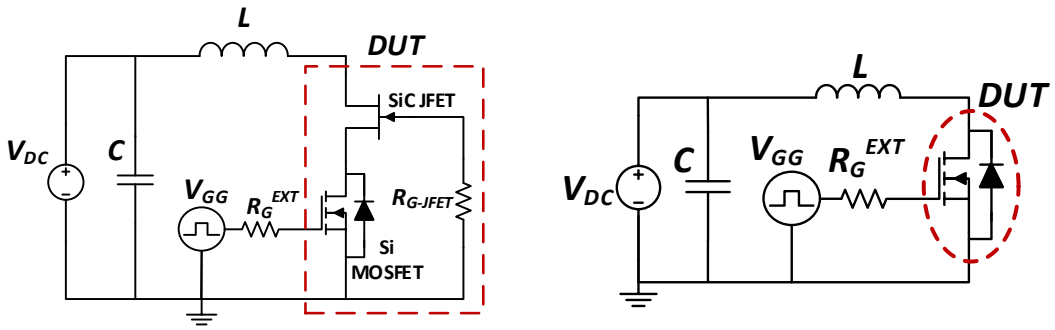
Eq. 3.6

3.3. Experimental Measurements of Single Shot UIS in Cascode JFETs

The avalanche ruggedness of power devices in this work is tested using the setup shown in Figure 3.5, the unclamped inductive switching circuit is shown in Figure 3.6, (a) for the SiC cascode JFET and (b) for the conventional SiC MOSFET. A gate pulse is applied to the device under test (DUT) which conducts a current thereby charging the inductor. As the DUT is turned-OFF, the inductor discharges its energy into the DUT thereby causing avalanche with the absence of a channel to conduct the current. The peak current is set by the duration of the gate pulse (t_{ON}) while the avalanche duration is set by the size of the inductance (according to Eq. 3.3). Tests were performed on a 650V SiC Trench MOSFET with datasheet reference SCT3060AL and a 650 V SiC Cascode JFET with datasheet reference UJ3C065080K3S. By using an electric heater attached to the back side of the device, single pulse UIS tests were performed at ambient (25 °C) and at high junction temperatures (105 °C and 150 °C). By increasing the length of the gate pulse, the avalanche current was increased until the device failed during avalanche conduction. During the tests, adequate time (5 minutes) is allowed between each stress to allow the device enough time to recover. It is also important to allow adequate time for the temperature to settle when performing high temperature measurements (30 minutes for this work).

(a) (b)

Figure 3.5 (a) Experimental test rig for UIS measurements (b) PCB Board for UIS testing



(a) (b)

Figure 3.6 (a) Circuit diagram for single shot avalanche test on SiC Cascode JFETs (b) Circuit diagram for single shot avalanche test on SiC MOSFET

Figure 3.7 (a) shows the avalanche current waveforms for the SiC trench MOSFET while Figure 3.7 (b) shows the corresponding measured avalanche voltage waveforms. Failure is evident at the point where the avalanche current starts rising which coincides with the point where the avalanche voltage drops to zero. The measurements performed at a junction temperature of 105 °C are shown in Figure 3.8 (a) and Figure 3.8 (b) for the avalanche currents and voltages respectively. By comparing the high and low temperature measurements, it is evident that increasing the junction temperature reduces the peak avalanche current before failure. In terms of avalanche energy, increasing the junction temperature from 25 °C to 105 °C reduces the maximum avalanche energy before failure from 229.25 mJ to 94.46 mJ.

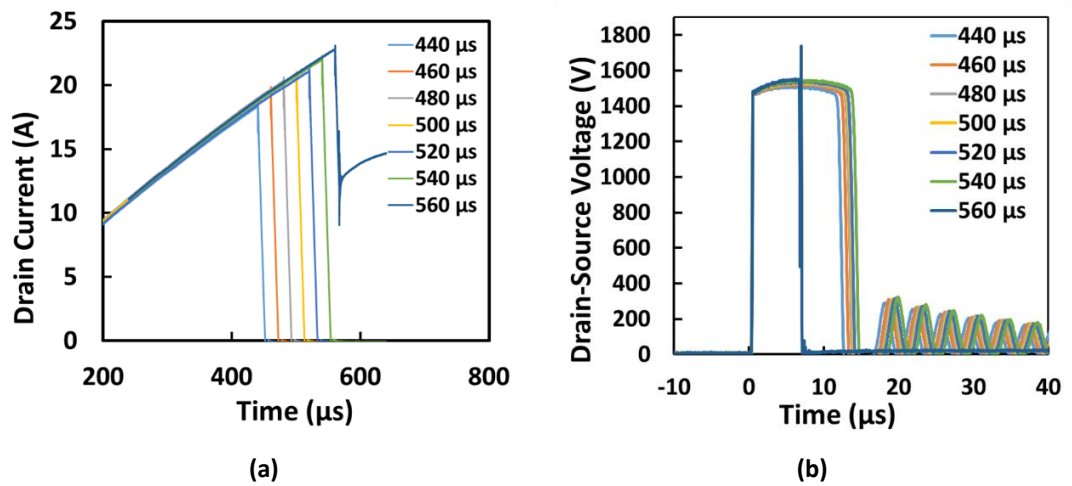


Figure 3.7 (a) Avalanche current waveforms for SiC Trench MOSFET at 25 °C (b) Avalanche voltage waveforms for SiC Trench MOSFET at 25 °C.

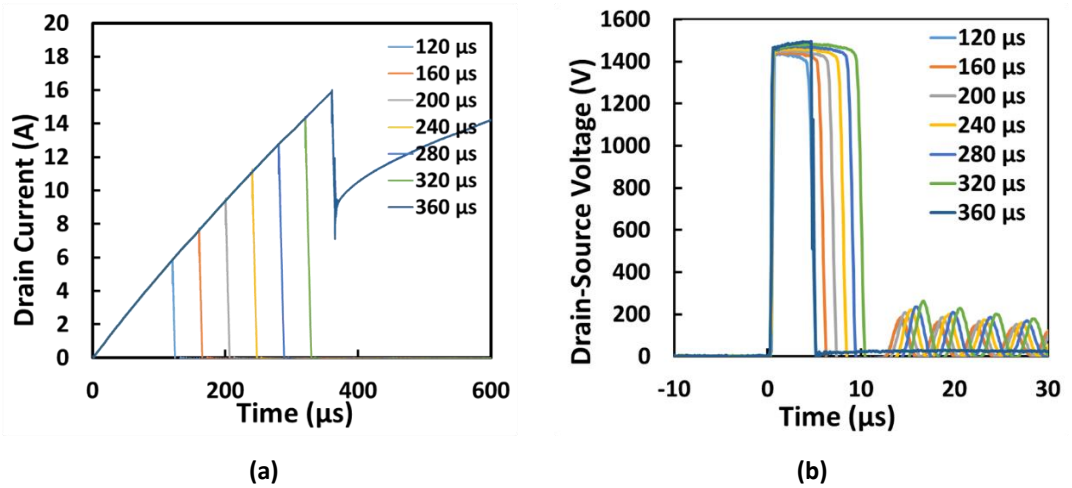
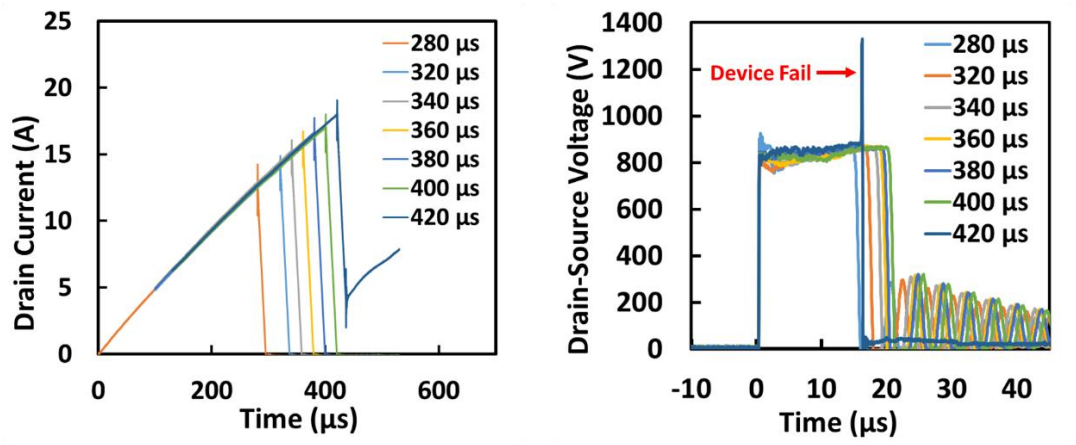


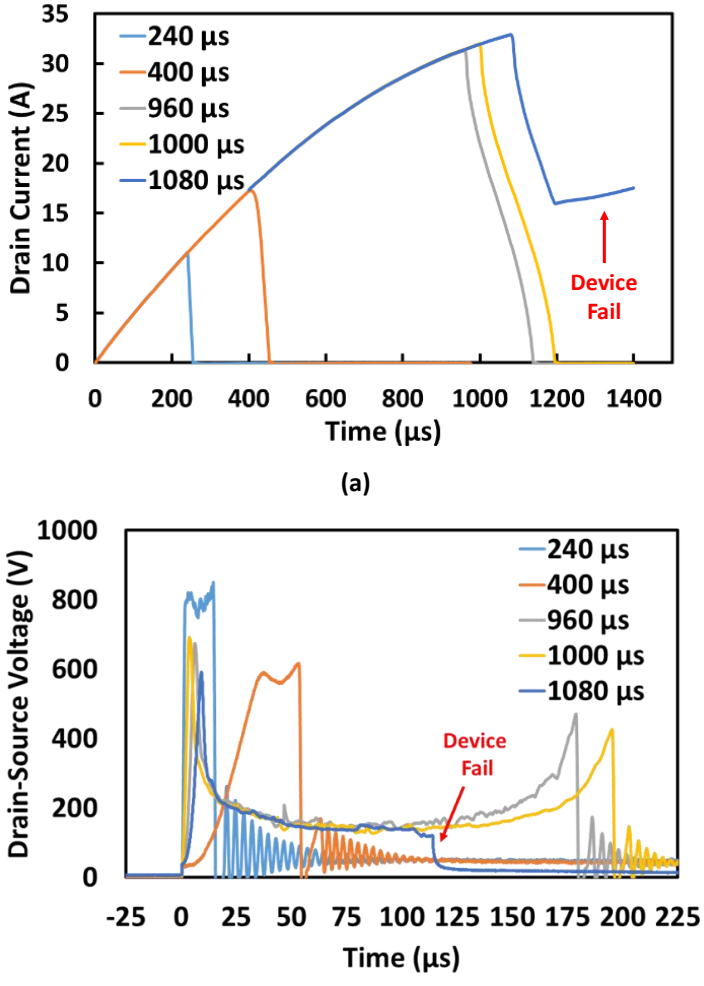
Figure 3.8 (a) Avalanche current waveforms for SiC Trench MOSFET at 105 °C (b) Avalanche voltage waveforms for SiC Trench MOSFET at 105 °C.

Similar single shot avalanche measurements were performed on the SiC cascode JFET. Figure 3.9 (a) shows the incremental avalanche currents until device failure at 25 °C while Figure 3.9 (b) shows the corresponding avalanche voltage measurements. However, as the junction temperature is increased to 105 °C, the avalanche characteristics in the SiC Cascode JFET exhibits non-typical characteristics. These include delayed voltage rise during turn-off and reduced peak avalanche voltages with prolonged avalanche duration at higher energy pulses. This atypical behaviour at 105 °C can be seen in Figure 3.10. SiC cascode JFET failure in avalanche can therefore be split into two modes, the first failure mode is a soft failure characterised by this atypical behaviour, and the second failure mode is catastrophic failure which is characterised by the reduction of V_{DS} to 0V. The avalanche energy dissipated by the SiC Cascode JFET was 154.03 mJ at 25 °C and 230.5 mJ at 105 °C (calculated for the pulse before catastrophic failure as shown in Figure 3.4).



(a) (b)

Figure 3.9 (a) Avalanche current waveforms for SiC Cascode JFET at 25 °C (b) Avalanche voltage waveforms for the SiC Cascode JFET at 25 °C.



(a)

(b)

Figure 3.10 (a) Avalanche current waveforms for SiC Cascode JFET at 105 °C (b) Avalanche voltage waveforms for the SiC Cascode JFET at 105 °C.

3.4. Bench Marking the SiC Cascode JFET UIS Performance

UIS measurements of various device technologies were done, and their performances benchmarked against the SiC cascode JFET (UJ3C065080K3S 31 A). The devices characterised were 900V SiC planar MOSFETs (C3M0065090D 36 A, C3M0120090D 23 A), 650V SiC trench MOSFETs (SCT3060AL 39 A, SCT3120AL 21 A), and a 650V silicon SJ MOSFETs (IPW65R150 22.4 A), see appendix for more details. These devices represent 650 V drive voltage SiC targeted applications. In these tests, a total of three (3) devices were evaluated from each technology and the average value is used for comparisons. The devices were characterised using high power avalanche at room temperature (25 °C) and high temperature (150 °C), and only 25 °C for low power avalanche. To achieve the high power avalanche, a small inductance (1 mH) is used is used with shorter gate pulses, while low power avalanche involves a longer pulse and a larger inductance (6 mH) resulting in a longer avalanche duration. This is designed to assess the two methods of MOSFET failure under UIS described in the introduction (section 3.1). All values for the SiC cascode JFET evaluated using catastrophic failure mode.

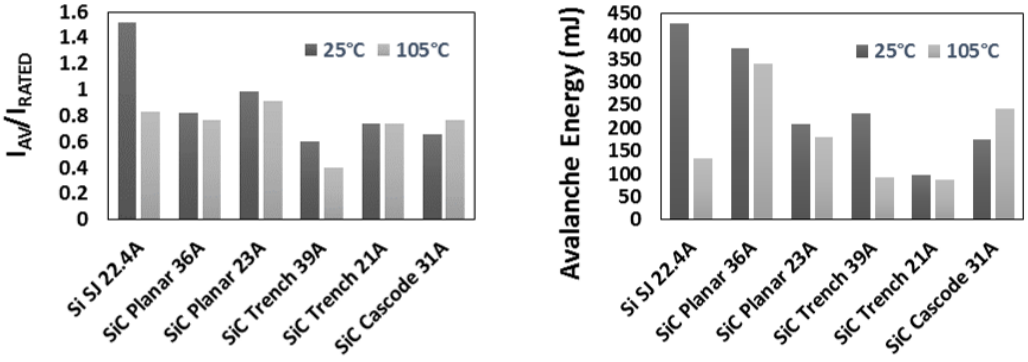


Figure 3.11 Avalanche performance comparison with L = 1 mH (a) Avalanche current to rated current ratio (b) Maximum avalanche energy

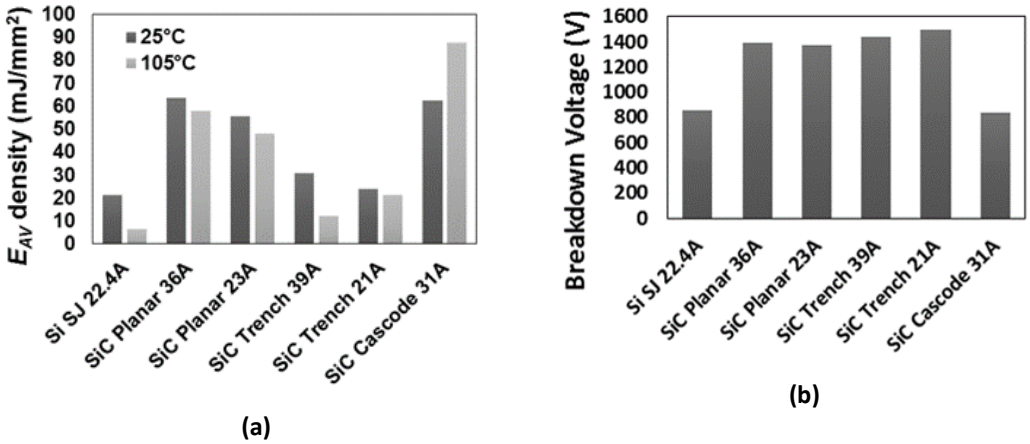


Figure 3.12 Avalanche performance comparison with L = 1 mH (a) Maximum avalanche energy density (b) UIS Avalanche Voltage

Figure 3.11 (a) shows the comparison of the maximum avalanche current as a ratio of rated current for each device at 1 mH. This normalises the avalanche current since the devices have distinct current ratings. Figure 3.11 (b) shows the maximum avalanche Energy dissipated for the same inductance value, while Figure 3.12 (a) presents the maximum avalanche energy density (this is the ratio of energy to chip areas in mm^2). From the results, it is evident that the Si SJ MOSFET has the most avalanche robustness at room temperature, with the performance deteriorating with temperature. The SiC cascode JFET on the other hand shows average avalanche robustness compared to the other SiC device technologies, with the only considerable advantage being in terms of maximum avalanche density. The actual breakdown voltages from UIS measurements of the various devices are presented in Figure 3.12 (b).

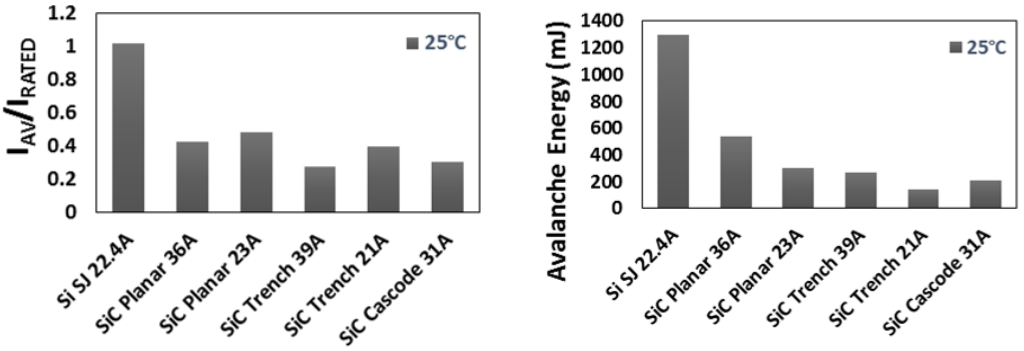


Figure 3.13 Avalanche performance comparison with L = 6 mH (a) Avalanche current to rated current ratio (b) maximum avalanche energy

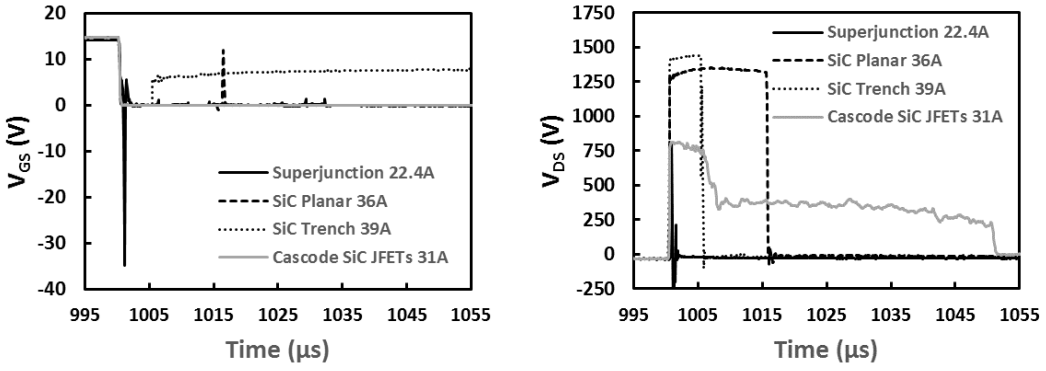


Figure 3.14 Avalanche performance comparison (a) Gate-Source voltage at failure (b) Drain-Source Voltage characteristics at failure

The performance at 6 mH is presented in Figure 3.13 (a) and Figure 3.13 (b). Only the 21 A trench MOSFET is worse than the SiC cascode JFET for the maximum energy recorded for all the devices compared. The Si SJ MOSFET appears to be the most avalanche robust, this is expected as the Si SJ has the largest chip size.

Figure 3.14 (a) and (b) shows the V_{GS} and V_{DS} waveforms during the avalanche failure pulse for the various devices tested. The SiC cascode JFET exhibits a completely different failure characteristic as is evident in Figure 3.14 (b) with two different voltages after failure (750V and 300V).

3.5. UIS in Stand-alone SiC JFETs

The stand-alone SiC JFET is a normally-ON device and a gate driver circuit which fixed the gate-source voltage at -16 V was used. An auxiliary SiC MOSFET of a voltage rating higher than the SiC JFET (UJ3N065080K3S, 650 V/ 32 A) under test is employed for charging the inductor to avoid turning on the switching the JFET as it requires negative gate Voltage. When the device used for charging the inductor is ON, the current ramps at a rate of V_{DC}/L and the peak current $I_{AV\text{-}PEAK}$ is defined by adjusting the duration of the gate pulse. When the device is turned-OFF, the current flows through the JFET as an avalanche current, because of its lower voltage rating. The voltage across the device increases to its breakdown voltage V_{BR}, causing a high power dissipation in the device.

The resulting current and voltage during avalanche for a SiC cascode are shown in Figure 3.15 (a) where the breakdown voltage of the device is clearly observed. As stated in the previous section, initial investigations [23] indicated a peculiar performance of SiC cascode JFETs during UIS, specially at high temperature, resulting in a reduced voltage switching rate and a dip of the voltage during avalanche, as shown in Figure 3.15 (b). This behaviour was predicted to be a consequence of gate current circulating through the gate resistance of the SiC JFET in the cascode configuration [4]. Hence, an important comparison and benchmarking of the performance of the stand-alone SiC JFETs under UIS to the SiC cascode JFET was conducted.

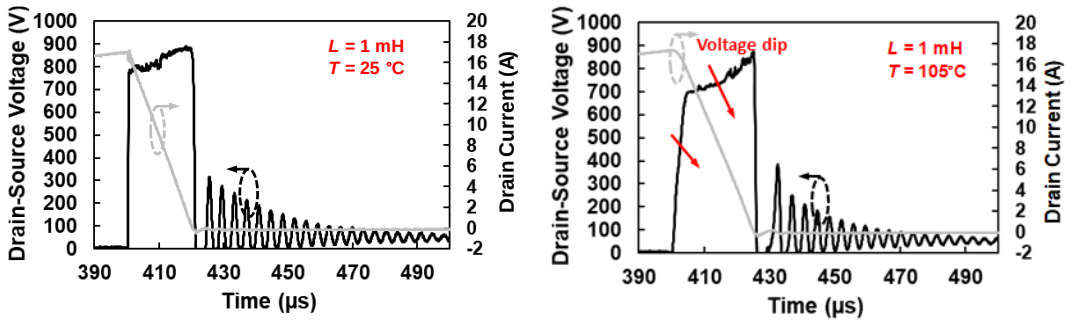
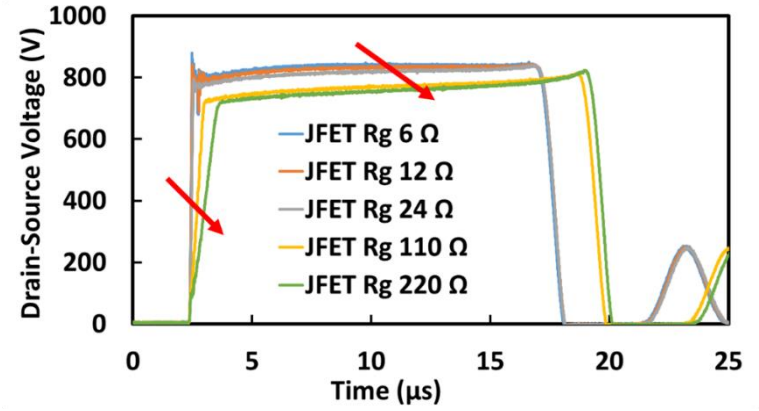
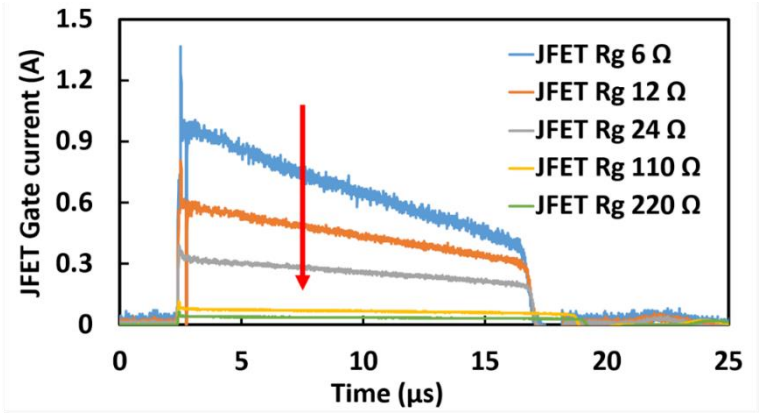


Figure 3.15 UIS test SiC Cascode, (a) Ambient temperature (b) Temperature 105°C

- Impact of JFET gate resistance on the UIS performance



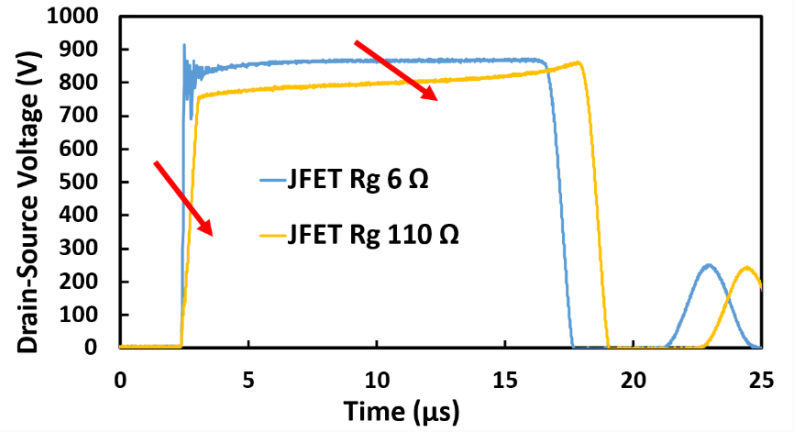
(a)



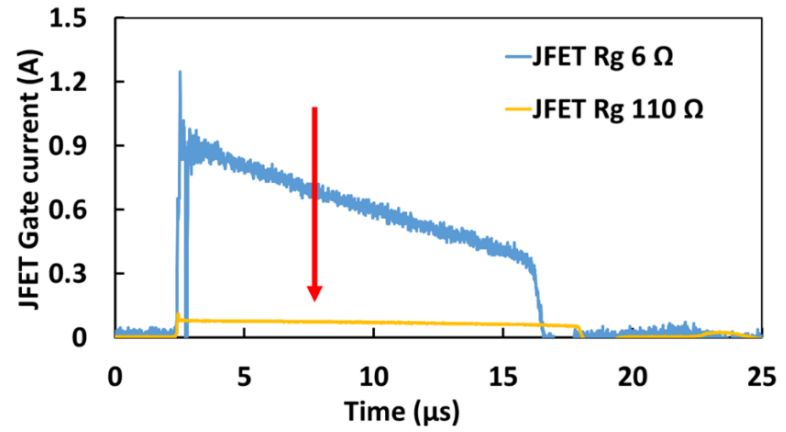
(b)

Figure 3.16 (a) Impact of RG-JFET on standalone SiC JFET drain-source voltage during UIS [ID=12.3 A, T=25 °C] (b) Impact of RG-JFET on JFET gate current during UIS [ID=12.3 A, T=25 °C]

In the commercially available SiC cascode JFET, the JFET gate terminal is not accessible, hence the role of the JFET gate resistance $R_{G\text{-}JFET}$ has been evaluated. The gate voltage was adjusted to -16 V and $R_{G\text{-}JFET}$ was varied from 6 to 220 Ω. The measured drain-source voltage V_{DS} and JFET gate current are show in Figure 3.16 (a) and Figure 3.16 (b) respectively, for $I_{AV\text{-}PEAK}$ of 12.3 A at 25 °C temperature. The same test is repeated at 150 °C temperature and illustrated in Figure 3.17. From the results in Figure 3.16 and Figure 3.17, it is clearly observed that increasing $R_{G\text{-}JFET}$ has an impact on V_{DS} during avalanche, causing a reduction of the V_{DS} transient during turn-off, a dip on V_{DS}, and a longer avalanche duration. Evaluating the gate current, increasing $R_{G\,JFET}$ reduces the value of the gate current, from a value close to 1 A for $R_{G\text{-}JFET}$=6 Ω to 80 mA for 220 Ω, this trend is seen to be repeated at 150 °C with negligible effect of temperature on the values. Figure 3.18 further illustrates this independence of the gate current on temperature. The gate current of the JFET at 25 °C, 75 °C, 125 °C, and 150 °C is illustrated. The tests in this case are all performed with a 10 A Drain current.



(a)



(b)

Figure 3.17 (a) Impact of RG-JFET on standalone SiC JFET drain-source voltage during UIS [ID=12.3 A, T=150 °C] (b) Impact of RG-JFET on JFET gate current during UIS (ID=12.3 A, T=150 °C)

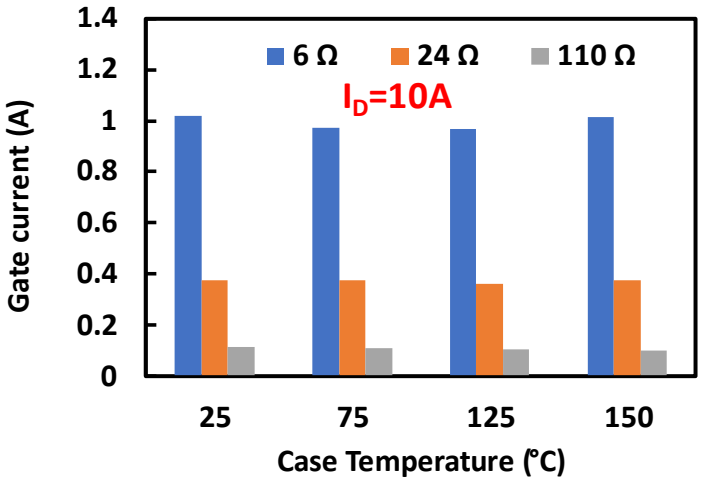
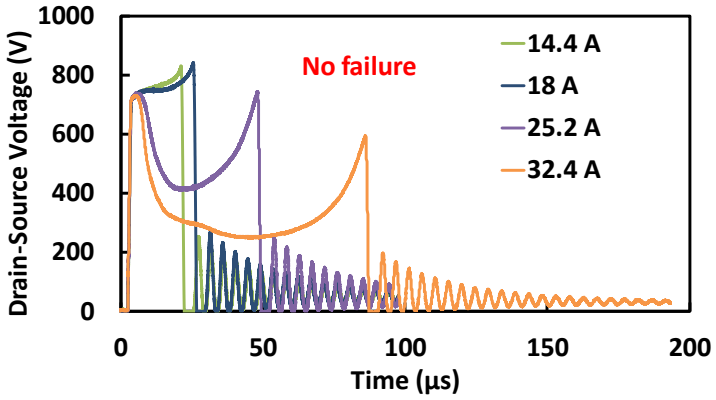


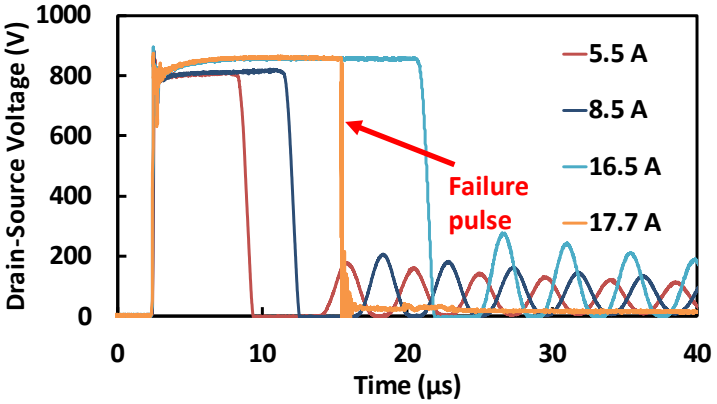
Figure 3.18 JFET gate current for different RG-JFET values at 25 °C, 75 °C, 125 °C, and 150 °C

- Impact of avalanche current on the UIS performance

Another fundamental element in the performance of the device under UIS is the peak avalanche current, as it is the parameter that will define the maximum avalanche capability of the device for a fixed inductor value. This has been evaluated for the SiC stand-alone JFET, for $R_{G\text{-}JFET}$=6 Ω and $R_{G\text{-}JFET}$= 220 Ω at 25 °C and 150 °C. Figure 3.19(a) and Figure 3.20(a) corresponding to $R_{G\text{-}JFET}$= 220 Ω/25 °C and $R_{G\text{-}JFET}$= 220 Ω/150 °C respectively show that as avalanche current increases, the dip in V_{DS} increases. This is a result of voltage drop across $R_{G\text{-}JFET}$ causing the operation of the JFET in linear mode rather than avalanche (i.e., the device is operating in the linear region, and not the blocking region). This is not observed in Figure 3.19 (b) and Figure 3.20(b), for $R_{G\text{-}JFET}$=6 Ω. In the test with $R_{G\text{-}JFET}$=6 Ω, the energy dissipated before failure is 122 mJ (25 °C, 16.5 A), and 71 mJ (150 °C, 13.3 A), however for $R_{G\text{-}JFET}$=220 Ω, the device can withstand UIS pulses of 32.4 A and 555 mJ (25 C) energy without failure. This energy is not actual avalanche energy since the device isn't in avalanche but is operating in linear mode. In this mode the energy and junction temperature continue to increase but the device does not fail (Catastrophic failure).

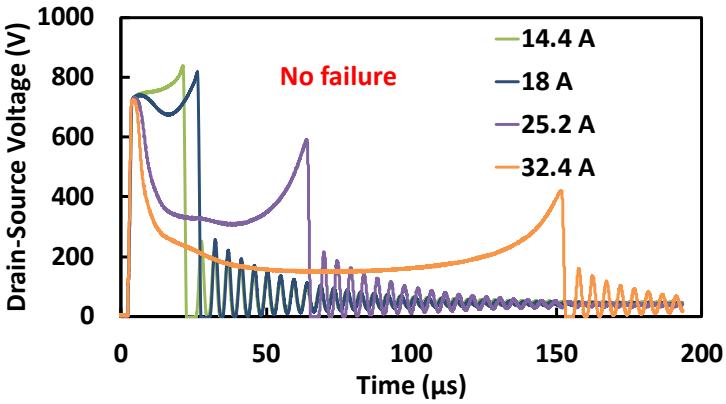


(a)

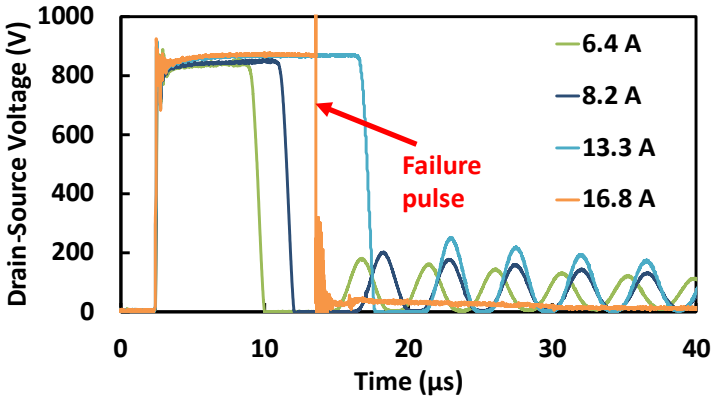


(b)

Figure 3.19 Impact of avalanche current on the stand alone SiC JFET drain-source voltage during UIS at 25 °C (a) $R_{G\text{-}JFET}$=220 Ω (b) $R_{G\text{-}JFET}$=6 Ω



(a)



(b)

Figure 3.20 Impact of avalanche current on the stand alone SiC JFET drain-source voltage during UIS at 150 °C (a) $R_{G\text{-}JFET}$=220 Ω (b) $R_{G\text{-}JFET}$=6 Ω

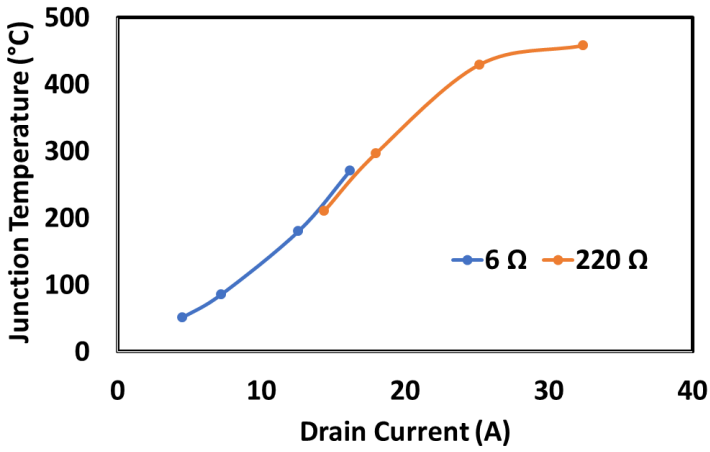


Figure 3.21 Maximum Junction temperature with increasing drain current for 6 Ω and 220 Ω test (T=25 C)

Figure 3.21 presents the calculated Junction temperature from Figure 3.20 for both low (6 Ω) and high (220 Ω) $R_{G\text{-}JFET}$ test. This is calculated from the power during t_{av} and thermal network provided by the manufacturer. The calculated temperature from the low $R_{G\text{-}JFET}$ test indicates

that the DUT fails with a junction temperature of approximately 300 °C, while in the high $R_{G,JFET}$ test the junction temperature to above 450 °C without failure as the device experiences a dip in the voltage and goes into linear mode. This indicated that temperature is not the main factor influencing the device failure.

3.6. Failure Analysis of SiC Cascode JEFT Under UIS

Closer inspection of the avalanche voltage characteristics of the SiC cascode JFET shown in Figure 3.10 is presented in Figure 3.22 showing that the SiC JFET undergoes delayed turn-off while the LV Silicon MOSFET goes into avalanche. Figure 3.22 (a) shows a closer inspection of the avalanche voltage transient of the SiC cascode JFET while Figure 3.22 (b) shows the zoomed in version.

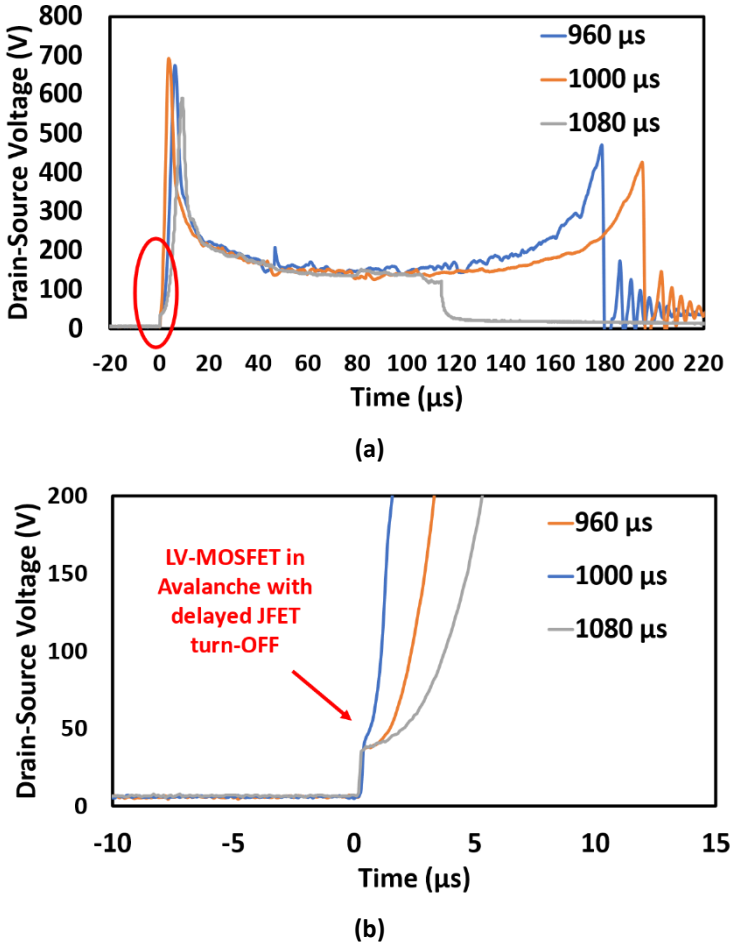


Figure 3.22 (a) Avalanche voltage transient showing delayed turn-off of the SiC JFET while the LV Si MOSFET is in avalanche. (b). Zoomed in version of 'a'.

The knee-point in Figure 3.22 (b) shows that the LV silicon MOSFET is in avalanche while the SiC JFET undergoes a delayed turn-off. This means that the SiC JFET operates in the linear mode (high voltage and current) while the LV-MOSFET is in avalanche. To further understand

this, finite element simulations of SiC Cascode JFETs in avalanche have been performed alongside SiC trench MOSFETs.

Failure analysis (FA) has been performed on the SiC trench MOSFETs and SiC Cascode JFET. As part of failure analysis, the source-drain resistance (R_{SD}) as well as drain-source resistance (R_{DS}) was measured across devices that have failed in avalanche to determine the nature of the short circuits across the device terminals. These measurements were made with the gate shorted to the source. Generally, R_{SD} was equal to R_{DS} in both devices. While the SiC Trench MOSFETs exhibited very low R_{SD} (0.5 to 2.4 Ω) thereby indicating a short circuit between the source and drain, the SiC Cascode JFET exhibited a higher R_{SD} (between 5.2 and 23.8 Ω) in failures under repetitive avalanche.

Gate capacitance measurements were also performed on both the SiC Trench MOSFET and Cascode JFET to determine the state of the oxide. While the gate-source terminal in the SiC Trench MOSFET was shorted (indicating a damaged oxide), in the case of the Cascode JFET, the gate oxide was still capable of blocking voltage. Figure 3.23 shows the gate voltage charging measurements on 3 SiC Cascode JFETs that failed under repetitive avalanche. The measurements indicate that the LV silicon MOSFET which acts as the gate input into the Cascode arrangement may still be functional.

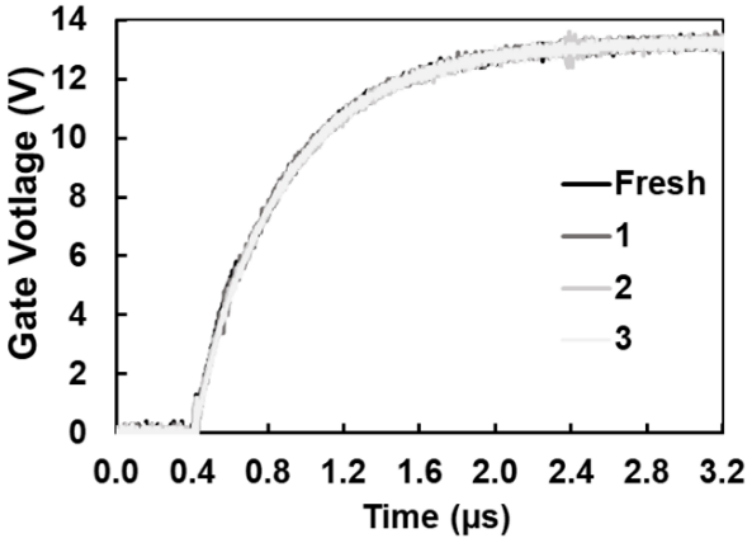


Figure 3.23 Gate voltage charging measurements with 220 Ω gate resistance.

Further FA tests were performed on the SiC Cascode JFET to determine the state of the body diode of the LV silicon MOSFET. For the SiC Cascode JFET, assuming that the JFET has been short-circuited from avalanche over-stress, Figure 3.24 (a) and (b) show the equivalent circuits. If a drain-source voltage is applied, the LV MOSFET body diode is reverse biased, hence, current flows through the shorted JFET and its gate resistance ($R_{G\text{-}JFET}$). On the

contrary, if a sufficient source-drain voltage (V_{SD}) is applied to forward bias the body diode, then there is a current divider between the forward biased diode and the SiC JFET gate resistance ($R_{G\text{-}JFET}$). This is shown in Figure 3.24 (b). In this case, the current divider depends on if the body diode is forward biased or not. If the V_{SD} voltage is below the body diode knee voltage, then current only flows through the SiC JFET gate resistance ($R_{G\text{-}JFET}$). If the V_{SD} voltage is above the diode knee voltage, then current will flow mainly through the LV MOSFET body diode since it will have a lower on-state resistance.

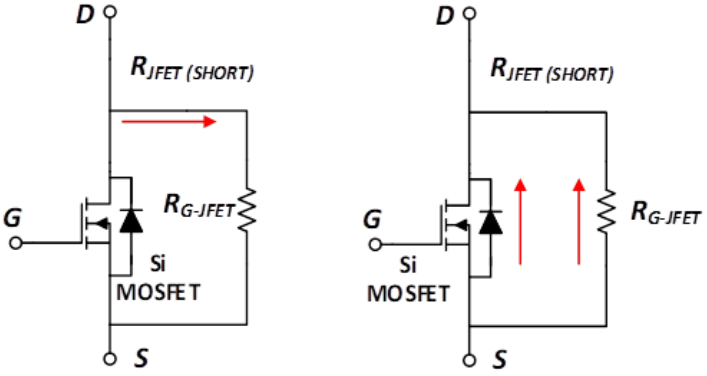


Figure 3.24 Equivalent circuits for the failed SiC Cascode JFET

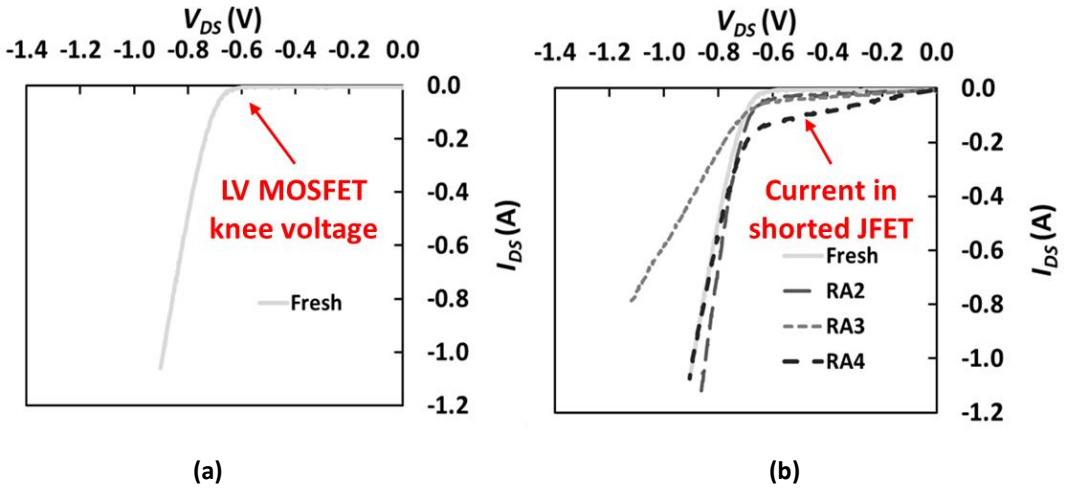


Figure 3.25 3rd quadrant characteristics of (a) unstressed SiC Cascode JFET and (b) damaged SiC Cascode JFET

To verify this, the 3rd quadrant characteristics (with V_{GS} = 0V) were measured for the unstressed and failed devices. When observing these characteristics, it is important to note that at low V_{SD} (below the knee voltage of the diode), a properly functioning cascode JFET should not have any current flow since the diode is not forward biased and the JFET is not ON. This is shown in Figure 3.25 (a). However, in a cascode device with a shorted JFET (due to failure under avalanche), at low V_{SD}, there will be current flowing in the circuit. This is

shown in Figure 3.25 (b) where a non-zero current is evident before the knee voltage of the body diode.

If the low voltage Si MOSFET is not damaged it will be possible to turn it ON and the current will flow through the channel of the MOSFET. To verify this assumption, a test has been defined, with the schematic shown in Figure 3.26. It consists of a resistive load switching test, where the current (I_S) and voltage across the device V_{DS} are measured. The selection of the resistive load is important as the failed devices are not able to block voltage. In this test, the current will flow through the series combination of R_{DEVICE} and R_{LOAD} as defined by Eq. 3.7

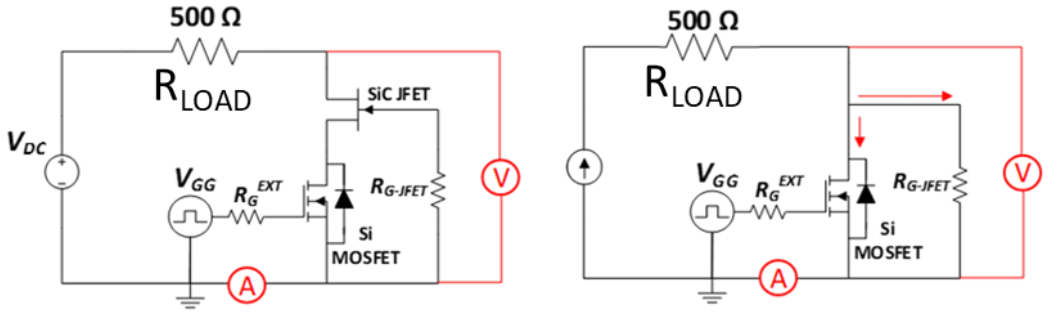
$$I_S = \frac{V_{DC}}{R_{DEVICE} + R_{LOAD}}$$

Eq. 3.7

The voltage across the device is given by a potential divider, where R_{DEVICE} is a function of the gate voltage level, and the measured voltage is determined by Eq. 3.8.

$$V_{DS} = \frac{R_{DEVICE}}{R_{DEVICE} + R_{LOAD}} V_{DC}$$

Eq. 3.8



(a) **(b)**

Figure 3.26 Test circuits for isolating LV silicon MOSFET from High-Voltage SiC JFET (a) unstressed device blocking voltage (b) Damaged device unable to block voltage.

For an unstressed device, if the device is turned ON, $R_{DEVICE} = R_{DS,ON}$ (cascode) and the current will flow through the channel of the LV Si MOSFET and the SiC JFET. If the unstressed SiC JFET cascode is OFF, the cascode will block voltage (R_{DEVICE} in the range of MΩ) and there is no current flowing through the device. The measured VDS will be equal to VDC according to the voltage divider Eq. 3.8. Using a power supply voltage V_{DC}= 30 V, a resistive load R_{LOAD} = 500 Ω and a pulse of 2 seconds, the measurement results of this test for an unstressed device are shown in Figure 3.27. Here it can be seen that the voltage across the device in the OFF-state is equal to 30 V i.e., the device is an open circuit.

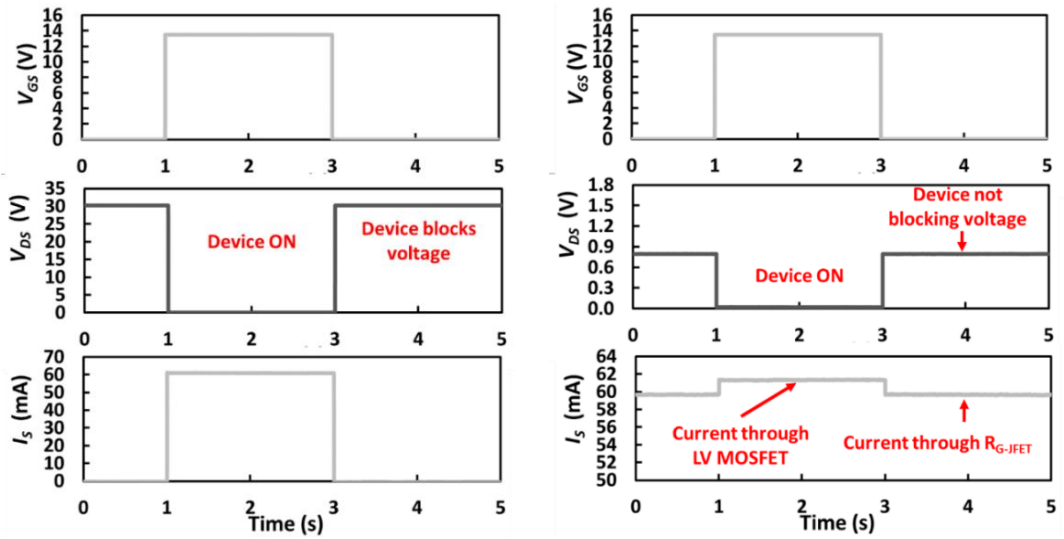


Figure 3.27 VGS, VDS and IS for (a) unstressed and (b) damaged SiC Cascode JFET

In the case of a damaged Cascode device where the SiC JFET is shorted, if the gate is OFF, R_{DEVICE}= $R_{G\text{-}JFET}$ hence there will be current flowing through the $R_{G\text{-}FET}$, as defined by Eq. 3.7. This can be seen in Figure 3.27 (b) where approximately 60 mA flows through the device in the OFF-state. If the gate is ON, the current will flow through the parallel combination of $R_{DS,ON}$ (Si MOSFET) and $R_{G\text{-}JFET}$, however, since $R_{DS,ON}$ is much smaller than $R_{G\text{-}JFET}$, then according to the current divider rule, it will mainly flow through the LV-MOSFET. It can be seen from Figure 3.27 (b), that the measured V_{DS} across the SiC Cascode JFET in the OFF-state is approximately 0.8 V, therefore indicating that the device is unable to block voltage.

From these measurements it can be verified that the LV Si MOSFET is still fully functional and has not been damaged by the UIS, however the presence of $R_{G\text{-}JFET}$ in parallel with the LV Si MOSFET impedes the blocking voltage capability of the device. The SiC JFET has lost its blocking voltage capability and the current flows through the gate of the JFET to the source terminal of the cascode, bypassing the low voltage Si MOSFET. The interaction between the low voltage Si MOSFET and the SiC cascode due to the presence of $R_{G\text{-}JFET}$ is key for this failure mechanism.

3.7. Finite Element Analysis (FEA) simulations of failure during unclamped inductive simulations (UIS)

In this section, SILVACO finite element simulations of Unclamped Inductive Switching (UIS) in SiC Trench MOSFETs and Cascode JFETs at failure is shown to explain the observations in the SiC Cascode JFET. The SiC devices structures are designed in SILVACO as shown in chapter 2 to match the voltage rating and static characteristics of the devices tested. The parameters

are defined in Table 3-1. Using the mixed-mode circuit simulator, the device structures is simulated in a similar circuit as in Figure 3.6 (a).

Table 3-1 Finite element simulation parameters for SiC Trench MOSFET and Cascode JFET

SiC Trench MOSFET Parameters	Value	SiC Cascode JFET Parameter	Value
Trench depth	1.2 µm	LV-MOSFET Breakdown Voltage	28 V
Drift layer thickness	5.8 µm	MOSFET gate oxide thickness	50 nm
Substrate doping	1x19 cm^{-3}	MOSFET p-body doping	8x17 cm^{-3}
N-source doping	1x19 cm^{-3}	SiC JFET drift layer thickness	6.2 µm
p-body doping	4x17 cm^{-3}	SiC JFET drift layer doping	2.33x16 cm^{-3}
Oxide thickness	50 nm,100 nm	SiC JFET channel width	1 µm
Drift layer doping	6.5x$10^{15}$$cm^{-3}$	SiC JFET gate p-doping	1x19 cm^{-3}
SiC MOSFET gate resistance	10 Ω	SiC JFET gate resistance	10 Ω
Avalanche Inductor	1 mH	Avalanche Inductor	1 mH

- SiC trench MOSFET UIS simulation

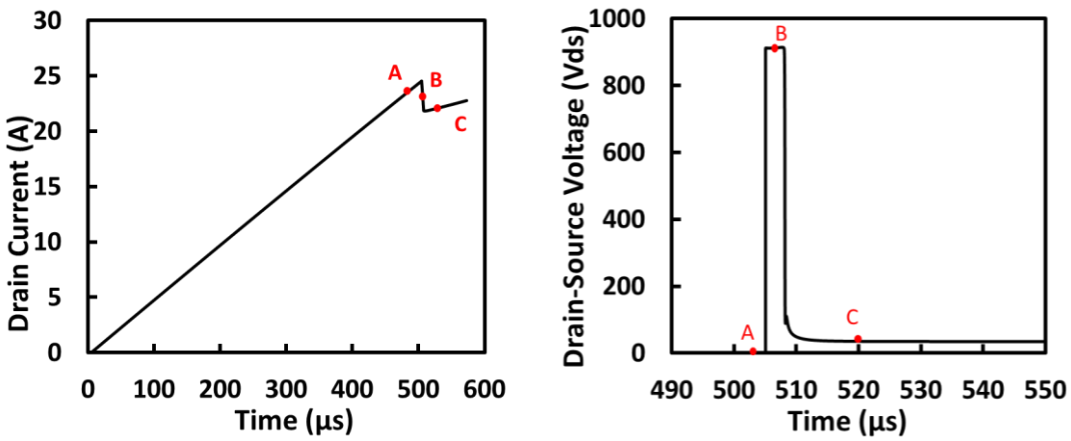


Figure 3.28 Simulated avalanche (a) Current and (b) Drain-source voltage of SiC Trench MOSFETs undergoing failure under UIS.

The avalanche current and voltage waveforms extracted from the simulator are shown in Figure 3.28 (a) and Figure 3.28 (b) for the SiC Trench MOSFET under UIS. Three points (A, B and C) in the avalanche current transients have been selected for closer investigation. Point A is an instant in time when the device is conducting current normally through the channel and charging the inductor. At point B, the MOSFET is in avalanche, but has not undergone parasitic BJT latch up while at point C, the device is undergoing BJT latch-up. Using the TonyPlot tool in SILVACO, 2-dimensional cross-sectional images have been extracted to further investigate the current flow paths during avalanche. The current densities and

electric fields within the device during stages A (conduction), B (avalanche) and C (electrothermal failure) have been extracted.

Figure 3.29 shows the simulated internal electric field while Figure 3.30 shows the simulated current density for the SiC Trench MOSFET during time instants A, B and C. The Trench MOSFET is clearly labelled with the body diode. Figure 3.29 and Figure 3.30 show that,

a) At point A, when the device conducts current normally through the channel, the current density is highest near the gate sidewall and spreads through the drift region. The electric field is confined to the channel.

b) At point B when the device is in avalanche, current diverts to the embedded PN body diode away from the channel and the peak electric field moves to the PN junction indicating that the device is blocking voltage while conducting a high current.

c) At point C, when the MOSFET is undergoing electrothermal failure, the current spreads through the NPN structure. Here, the internal electric field drops thereby indicating the device no longer blocks voltage.

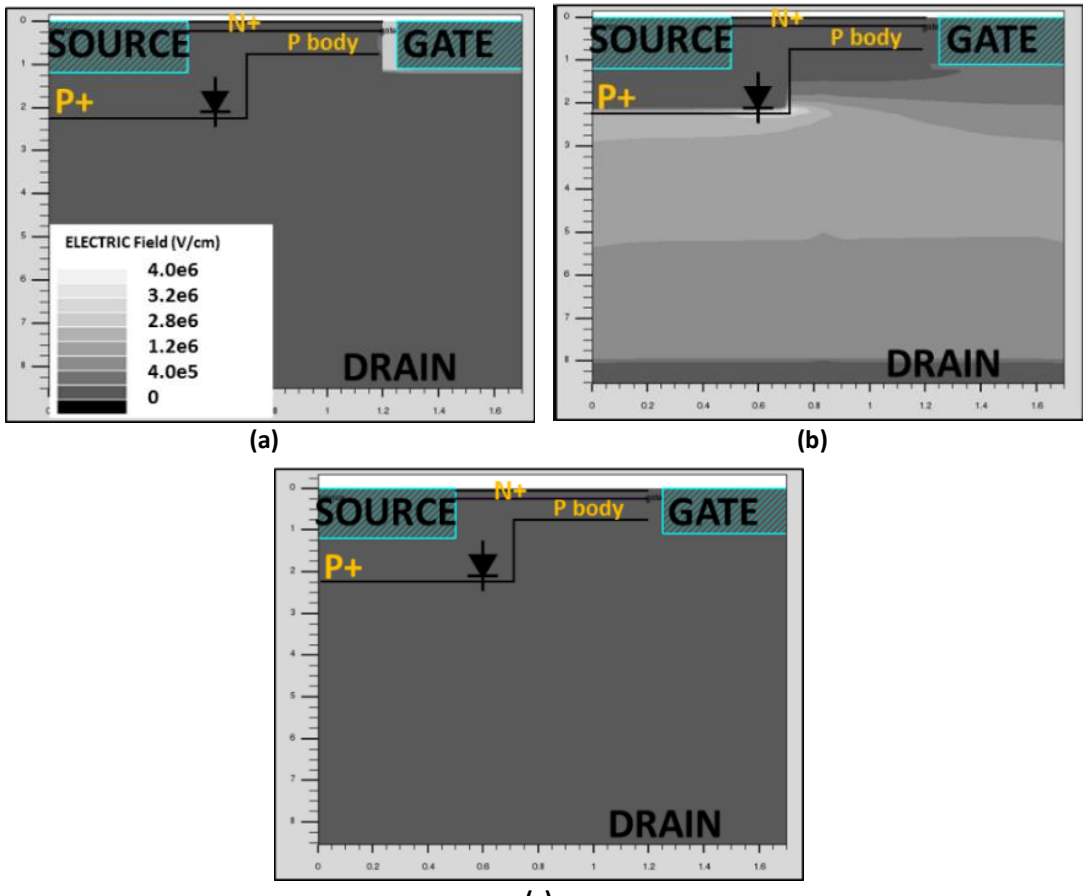


Figure 3.29 2D-Electric Fields contour plots showing E-field lines at points A, B and C in the SiC Trench MOSFET

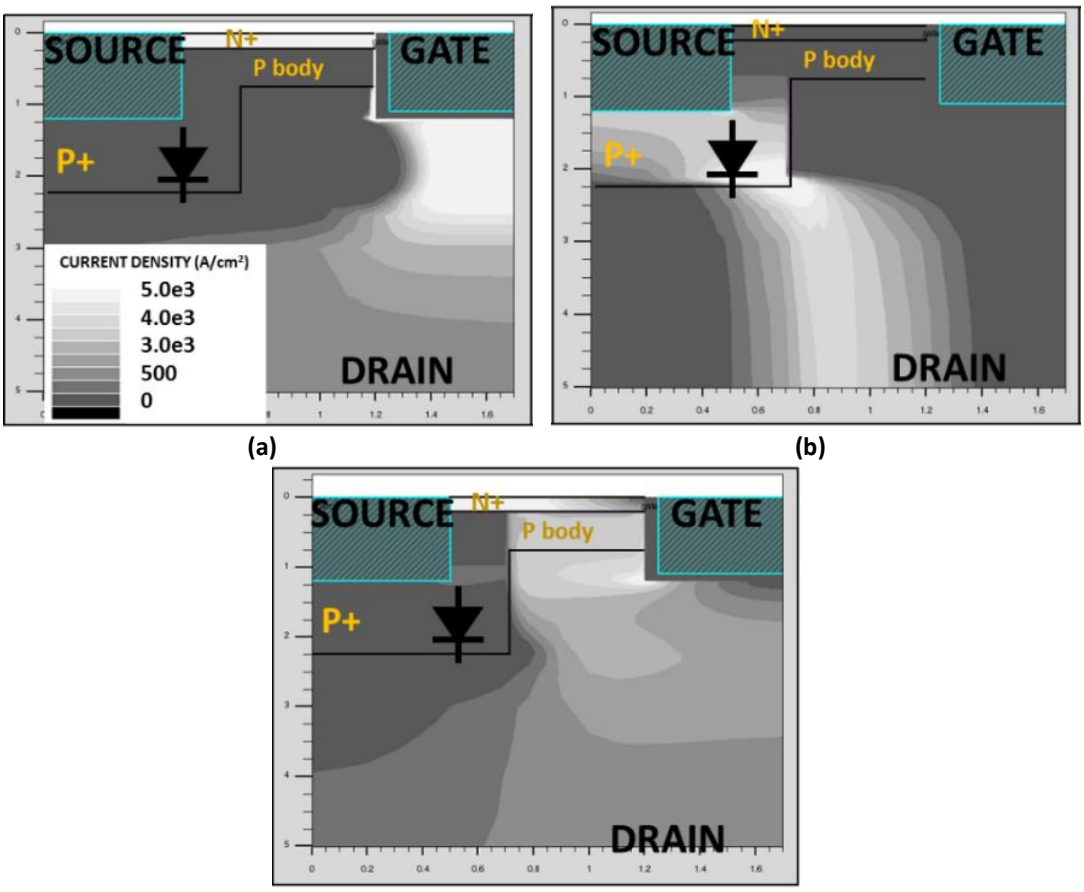


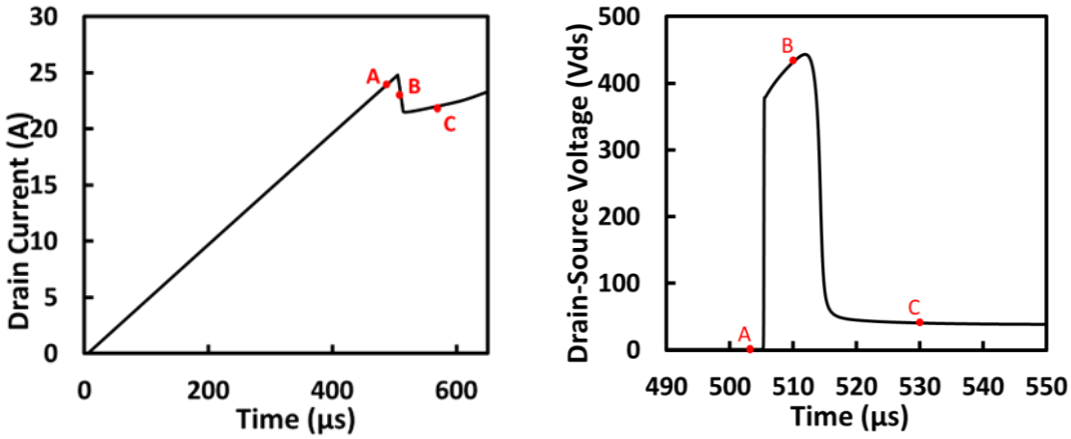
Figure 3.30 2D-Current density contour plots showing current flow path at points A, B and C in the SiC Trench MOSFET

- SiC cascode JFET UIS simulation.

The UIS tests from Figure 3.10 demonstrated anomalous avalanche characteristics in the SiC Cascode JFET evident in the delayed avalanche voltage transient resulting in low voltage turn-off. There was also a dip in the avalanche voltage waveform indicating that the SiC JFET was operating in linear mode (partially ON). This characteristic was evident at higher junction temperatures, thereby indicating that a temperature induced mechanism was causing the JFET turn-off dV/dt to reduce. Finite element simulations performed of the SiC cascode JFET under UIS were performed to further understand this behaviour. These provided further evidence that the cascode JFET anomalous behaviour can be characterised as failure. Hence, the cascode JFET failure during UIS can be categorised in to two types,

a) Catastrophic failure

b) Soft Failure

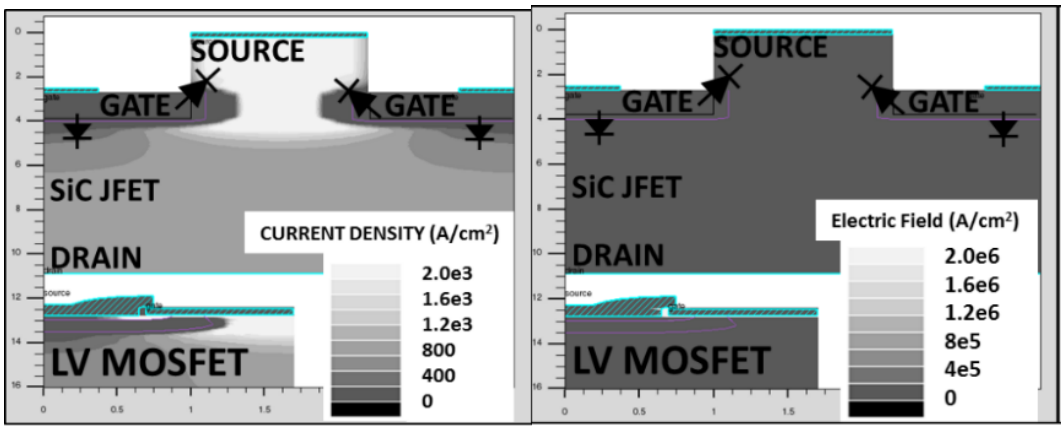


(a) (b)

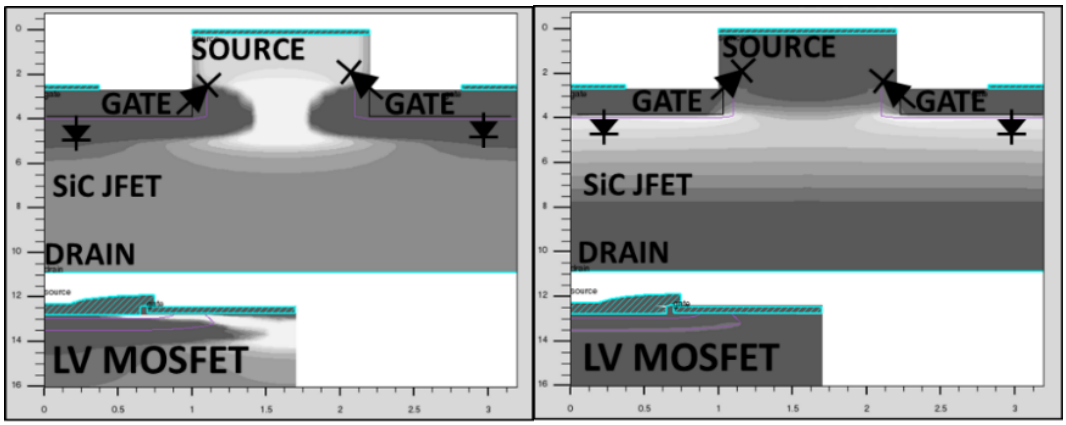
Figure 3.31 Simulated Avalanche (a) current and (b) Voltage for the SiC Cascode JFET during UIS showing conduction: A, avalanche: B, and electrothermal failure: C.

Catastrophic failure

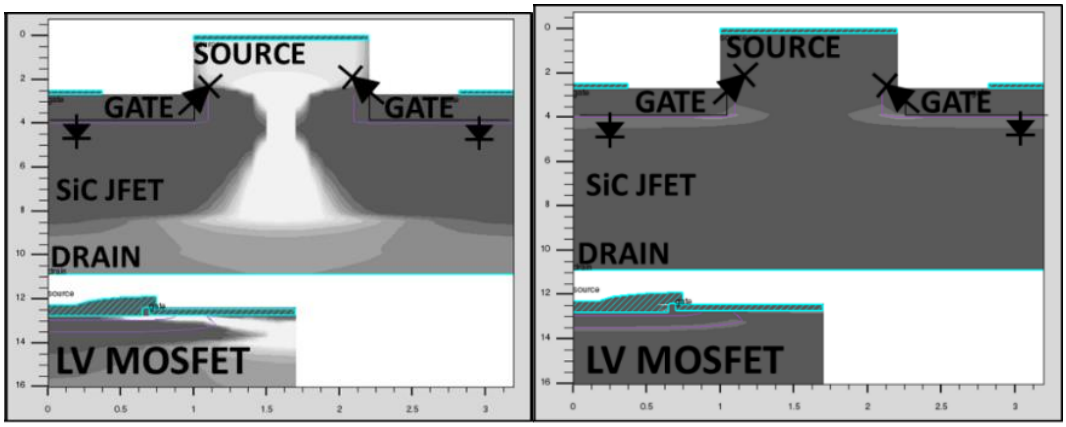
This failure is similar to failure mode under UIS in MOSFET. It is characterised by increase in current because of thermal runaway leading to a short between the cascode terminals. This failure is experienced at room temperature and also at high temperature operation Simulated avalanche current and voltage transients are respectively shown in Figure 3.31 (a) and Figure 3.31 (b). The internal current flow paths of the SiC Cascode JFET and the SiC Trench MOSFETs are different due to the differences between the MOSFET and the JFET structures. Figure 3.32 shows the current densities and electric fields within the JFET at points A, B and C from Figure 3.31. The current flow path during conduction, avalanche, and failure are all the same. The only difference is that the channel is open during conduction, hence the electric fields are low [seen in Figure 3.32(a)], whereas the channel is pinched OFF in avalanche, as evident by the high electric fields seen in Figure 3.32(b). The electric field reduces after failure as in Figure 3.32(c) showing the device is unable to block voltage.



(a)



(b)



(c)

Figure 3.32 2D contour plots of Current density(left) and Electric Fields (right) showing avalanche characteristics at points A, B and C in the SiC Cascode JFET

Soft Failure

The soft failure during UIS operation in the cascode device only occurs with high temperature operations. (above 100°C), it presents with anomalous characteristics as mentioned earlier. To reproduce the experimental observations shown in Figure 3.10, the resistance between the JFET gate and LV-MOSFET source ($R_{G,JFET}$) and avalanche current are varied in the simulator. The soft failure occurs in two stages.

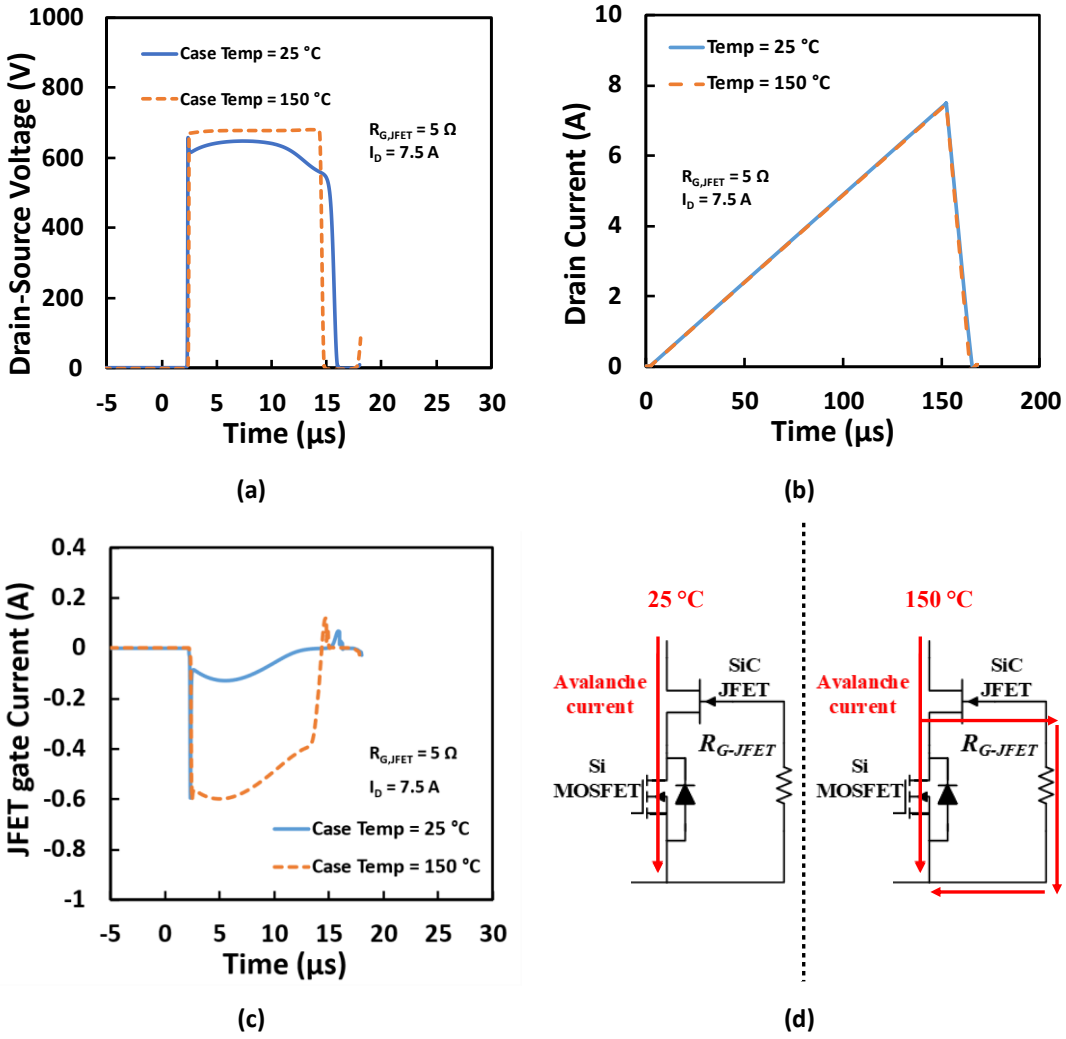


Figure 3.33 Simulated (a) V_{DS} and (b) I_D (c) $I_{G,J}$ for SiC Cascode JFET with R_{G-JFET} = 5Ω and (c) Current path

- **Stage 1**

Figure 3.33 shows the results of the simulations for $R_{G,JFET}$ =5 Ω, 7.5 A, and 150°C (5 Ω is the JFET internal from datasheet). Simulation result at 25°C is included as well to provide better understanding. It can be observed from Figure 3.33(a) that the V_{DS} characteristics at low I_{AV} and 150°C is typical like that of 25°C and experimental results from Figure 3.10 (240 µs). The current at 25°C and 150°C is also identical as seen Figure 3.33(b). The main difference appears when inspecting the JFET gate current shown in Figure 3.33(c). This illustrates much larger

current magnitudes due to thermally generated carriers through the JFET gate path. Figure 3.33(d) shows the current path in both low and high temperature cases. Hence, the UIS stress due to increased current damages the JFET gate path increasing the resistance (i.e., $R_{G,JFET}$).

- **Stage 2**

Figure 3.34 show the results of the simulations for increased values of $R_{G,JFET}$ and I_{AV}. It is observed that Figure 3.34 models the SiC Cascode JFET avalanche characteristics at higher junction temperatures as the I_{AV} is increased as from Figure 3.10. The dual slope in the avalanche current indicates the partial turn-on of the SiC JFET during avalanche. This occurs at the same time as the dip in the V_{DS} waveform. The JFET gate current is relatively lower because of the damage to the JFET gate path simulated by an increase in $R_{G,JFET}$. However, the current induces a very high voltage across the JFET gate due to the increased $R_{G,JFET}$. The current also increases with increased I_{AV} and further damages the JFET gate path. This anomalous behaviour is a result of the SiC Cascode JFET going into linear mode because of the significant gate current that flows through $R_{G,JFET}$ thereby partially turning the JFET on. Figure 3.34 (d) shows the current flow paths. The dotted lines represent relatively smaller current magnitude. Further increase in I_{AV} eventually lead to the catastrophic failure.

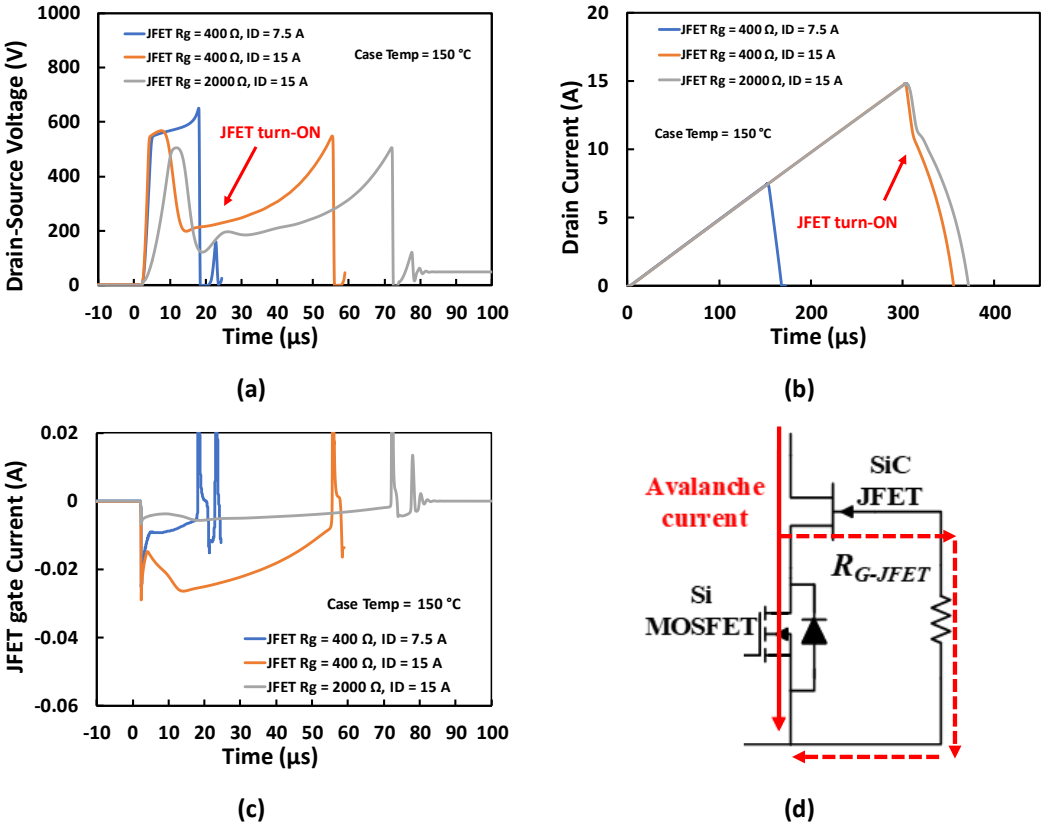
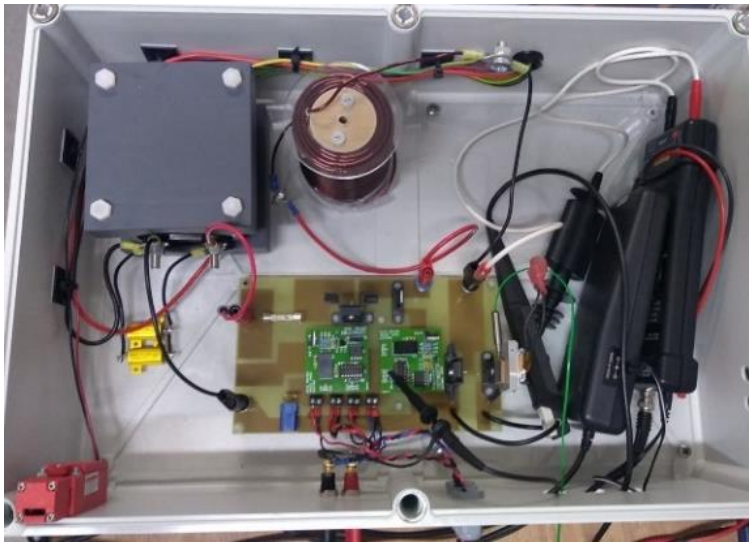


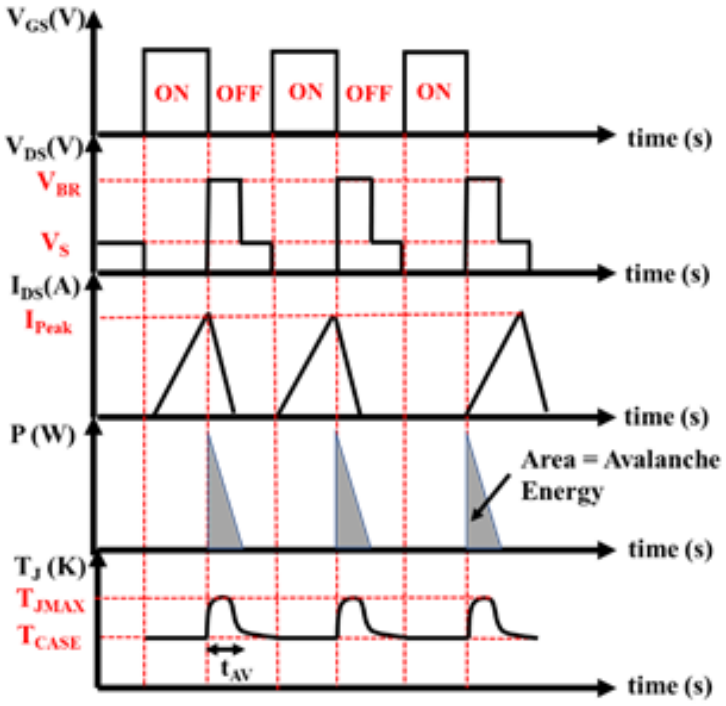
Figure 3.34 Simulated (a) V_{DS} and (b) I_D (c) $I_{G,J}$ for SiC Cascode JFET with increasing $R_{G\text{-}JFET}$ and I_{AV} and (d) Current path.

3.8. Experimental Measurement of Repetitive UIS

Figure 3.35 (a) shows the repetitive avalanche experimental setup and shown in Figure 3.35 (b) is a generic representation of the repetitive avalanche transient voltages, currents and idealized power and temperature plots. Devices under repetitive avalanche undergo periodic junction temperature excursions proportional to the avalanche power dissipated. The repetitive avalanche tests were performed to investigate the evolution of the anomalous VDS transients in the SiC cascode JFET.



(a)



(b)

Figure 3.35 (a) Repetitive avalanche test setup (b) Repetitive avalanche waveforms

The repetitive avalanche tests were performed using the circuit shown in Figure 3.36. In the repetitive avalanche circuit, there are three additional devices (2 transistors and a diode) along with the DUT. This circuit has been designed to enable failure analysis by separating the failure of the SiC JFET from the LV silicon MOSFET. Auxiliary transistor Q1 is required for isolating the DC power supply from the DUT, which is highly relevant for the SiC Cascode JFET tests, since the failure of the JFET into short circuit can lead to the LV silicon MOSFET being exposed to full DC voltage (which is higher than the rated voltage of the LV silicon MOSFET). The test sequence is as follows (shown in Figure 3.37),

1) First Auxiliary transistor Q1 is turned ON while the other devices are OFF. If there are no fails, there should be no current, hence, this stage is for checking for short circuit fails.

2) After a short deadtime, auxiliary transistor Q2 is also turned ON thereby charging the inductor to a desired current value depending on the load inductance and the pulse duration.

3) Both auxiliary transistors Q1 and Q2 are simultaneously turned OFF thereby causing the inductor to discharge its stored energy in the DUT while the diode D1 ensures the circuit is closed.

5

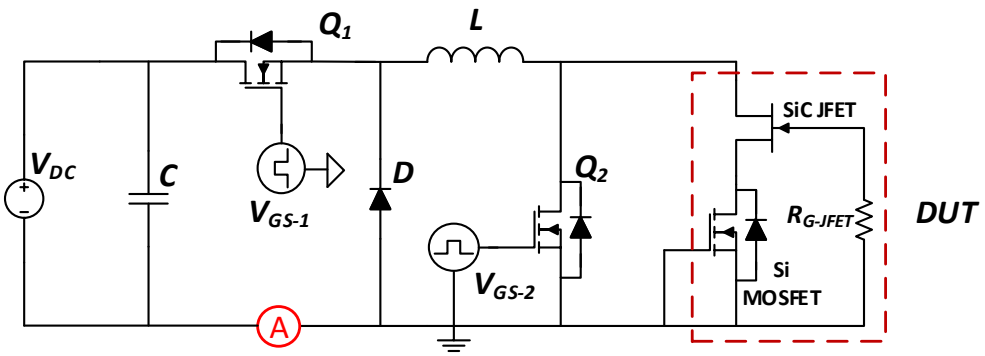


Figure 3.36 Repetitive avalanche circuit showing auxiliary devices.

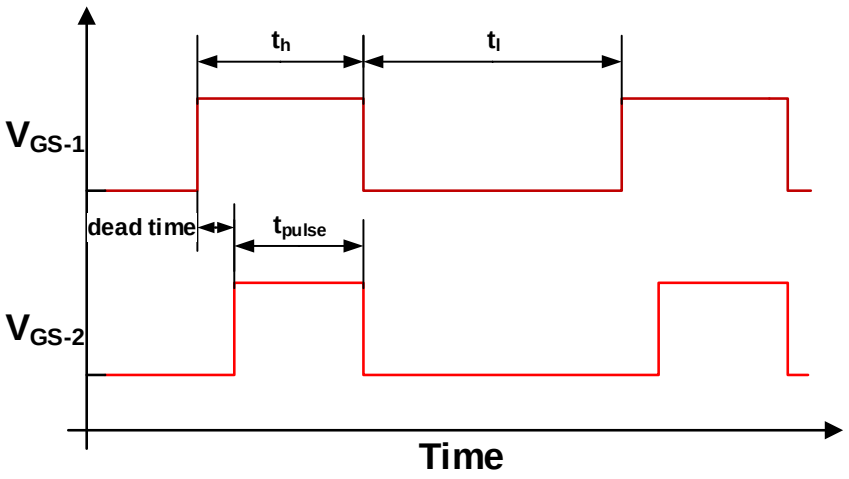


Figure 3.37 Test sequence pulses for the auxiliary devices

It is important to note that the current and voltage ratings of the auxiliary transistors should be higher than the DUT. The inductor used in the repetitive avalanche measurements is a 1 mH inductor and the DC voltage used is 50 V. A heatsink was attached to the device and the case temperature was monitored. The time interval between each avalanche pulse is sufficient to ensure that the case temperature rises by less than 3-4 °C. Since the peak avalanche current plays a critical role in the performance of the device, investigations have been performed with different peak avalanche currents, as summarised in Table 3-2 and Table 3-3.

Table 3-2 Repetitive avalanche pulses for device A

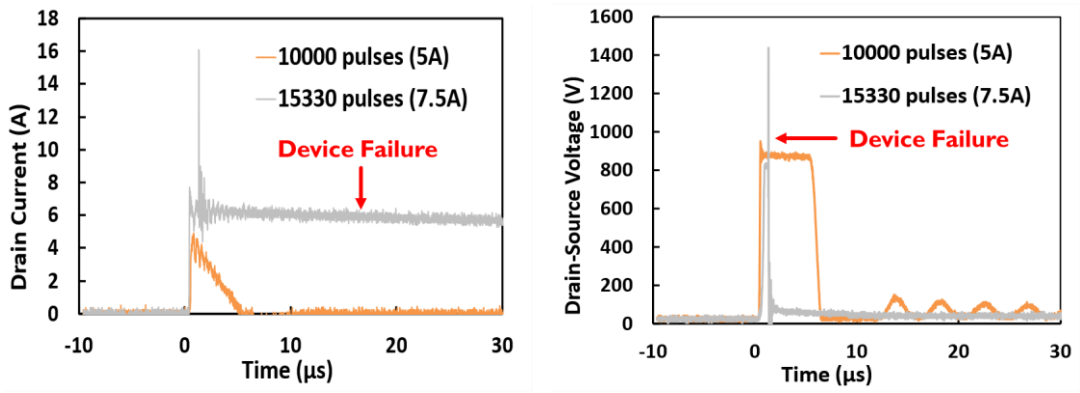
Cycle number	Avalanche current (A)
1-20000	5
20001-40000	7.5

Table 3-3 Repetitive avalanche pulses for device B

Cycle number	Avalanche current (A)
1-20000	5

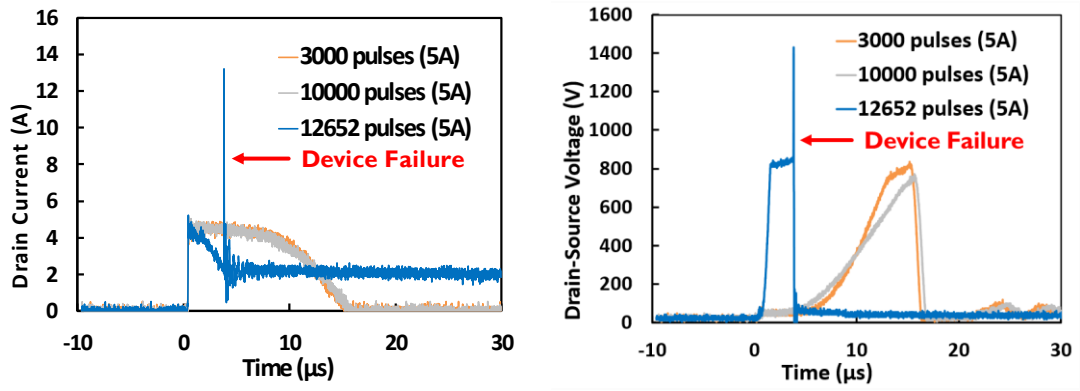
Figure 3.38 (a) shows the avalanche current waveform after 10,000 pulses of 5 A peak current along with the last avalanche pulse where failure occurs. Figure 3.38 (b) shows the corresponding avalanche voltage transients. It can be observed that during the failure pulse, the current through the device does not fall to zero while the voltage across the device drops to zero early in the avalanche pulse. Figure 3.39 (a) shows similar waveforms for a different SiC cascode device. Here, at 3000 and 10000 pulses, the avalanche current waveforms do not appear normal due to the reduced negative slope indicating delayed JFET turn-off, as shown in the finite element models in Figure 3.34. The corresponding avalanche voltage waveforms at 3000 and 10000 pulses shown in Figure 3.39 (b) exhibits a delayed voltage rise. The avalanche failure pulse (at 12,652 cycles) shows a similar failure profile as seen in Figure 3.38 (a).

Repetitive avalanche measurements were also performed on the SiC Trench MOSFETs under identical conditions. Figure 3.40 (a) and (b) respectively show the avalanche current and voltage waveforms after 20000 cycles at each avalanche current level, from 5 A to 10 A. It is apparent that no anomalous avalanche characteristics are observed, and the device exhibits the typical characteristics.



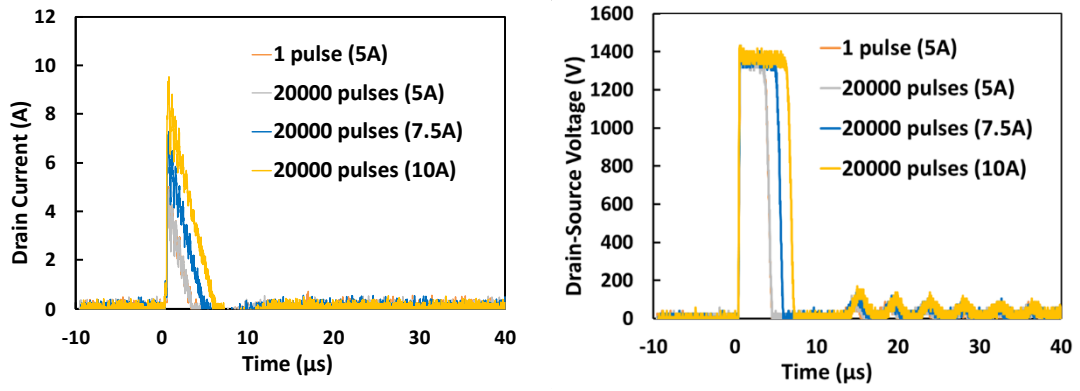
(a) (b)

Figure 3.38 Repetitive Avalanche measurements from Cascode JFET A (a) current and (b) voltage



(a) (b)

Figure 3.39 Repetitive Avalanche measurements from Cascode JFET B (a) current and (b) voltage



(a) (b)

Figure 3.40 (a) Repetitive avalanche current characteristics for SiC Trench MOSFET (b) Repetitive avalanche voltage characteristics for SiC Trench MOSFET

3.9. Conclusion

In this chapter, UIS tests both experimentally and with TCAD simulation have been performed on SiC cascode JFET. The results show that the SiC cascode JFET seems electrothermally robust and can withstand a competitive amount of avalanche energy without failure. It was also demonstrated that the SiC cascode JFET exhibits atypical behaviours during UIS tests. This atypical behaviour is a failure of the JFET gate path containing $R_{G\text{-}JFET}$ within the internal structure of the device. Hence, the SiC cascode JFET can be said to experience two failure modes under avalanche conduction.

The first is the usual catastrophic failure, this occurs at both low and high temperature UIS tests. It characterised by a thermal runaway of current and an inability to block high voltage like the usual failure in MOSFETs. The second failure is a soft failure, this occurs only at high temperature UIS tests. It is characterised by a delayed turn-off dv/dt, a large dip in drain-source voltage coupled with a change in the current slope, and longer avalanche durations.

The stand-alone SiC JFET were also characterised under UIS and confirmed the sensitivity of the gate path and $R_{G\text{-}JFET}$ during avalanche.

The SiC cascode JFET performance was also benchmarked against other device technologies showing the competitive robustness of the Cascode JFET technology. Its ability to turn on with a positive voltage and avoid gate oxide reliability issues partnered with this electrothermal robustness makes the SiC cascode JFET a real option for various applications. The reliability can also be further enhanced with a more robust gate path capable of operating at high temperatures.

Finally, the performance under repetitive avalanche pulses is characterised showing that the SiC cascode displays the soft failure characteristics at a much lower current that similar rated SiC MOSFETs for some of the devices selected. It also experiences catastrophic failure at lower currents and after less repetitive pulses.

References

[1] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and Reliability Review of 650V and 900V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," *IEEE Transactions on Industrial Electronics,* pp. 1-1, 2019, doi: 10.1109/TIE.2019.2945299.

[2] A. Fayyaz, L. Yang, M. Riccio, A. Castellazzi, and A. Irace, "Single pulse avalanche robustness and repetitive stress ageing of SiC power MOSFETs," *Microelectronics Reliability,* vol. 54, no. 9, pp. 2185-2190, 2014/09/01/ 2014, doi: https://doi.org/10.1016/j.microrel.2014.07.078.

[3] C. DiMarino and B. Hull, "Characterization and prediction of the avalanche performance of 1.2 kV SiC MOSFETs," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2-4 Nov. 2015 2015, pp. 263-267, doi: 10.1109/WiPDA.2015.7369294.

[4] P. Alexakis, O. Alatise, J. Hu, S. Jahdi, L. Ran, and P. A. Mawby, "Improved Electrothermal Ruggedness in SiC MOSFETs Compared With Silicon IGBTs," *IEEE Transactions on Electron Devices,* vol. 61, no. 7, pp. 2278-2286, 2014, doi: 10.1109/TED.2014.2323152.

[5] N. Ren, H. Hu, K. L. Wang, Z. Zuo, R. Li, and K. Sheng, "Investigation on single pulse avalanche failure of 900V SiC MOSFETs," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 13-17 May 2018 2018, pp. 431-434, doi: 10.1109/ISPSD.2018.8393695.

[6] V. Pala, B. Hull, J. Richmond, P. Butler, S. Allen, and J. Palmour, "Methodology to qualify silicon carbide MOSFETs for single shot avalanche events," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2-4 Nov. 2015 2015, pp. 56-59, doi: 10.1109/WiPDA.2015.7369276.

[7] A. Fayyaz *et al.*, "UIS failure mechanism of SiC power MOSFETs," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 7-9 Nov. 2016 2016, pp. 118-122, doi: 10.1109/WiPDA.2016.7799921.

[8] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, "SiC power MOSFETs performance, robustness and technology maturity," *Microelectronics Reliability,* vol. 58, pp. 164-176, 2016/03/01/ 2016, doi: https://doi.org/10.1016/j.microrel.2015.12.034.

[9] M. D. Kelley, B. N. Pushpakaran, and S. B. Bayne, "Single-Pulse Avalanche Mode Robustness of Commercial 1200 V/80 mΩ SiC MOSFETs," *IEEE Transactions on Power Electronics,* vol. 32, no. 8, pp. 6405-6415, 2017, doi: 10.1109/TPEL.2016.2621099.

[10] I. Dchar, M. Zolkos, C. Buttay, and H. Morel, "Robustness of SiC MOSFET under avalanche conditions," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 26-30 March 2017 2017, pp. 2263-2268, doi: 10.1109/APEC.2017.7931015.

[11] J. Wei, S. Liu, S. Li, J. Fang, T. Li, and W. Sun, "Comprehensive Investigations on Degradations of Dynamic Characteristics for SiC Power MOSFETs Under Repetitive Avalanche Shocks," *IEEE Transactions on Power Electronics,* vol. 34, no. 3, pp. 2748-2757, 2019, doi: 10.1109/TPEL.2018.2843559.

[12] T. Nguyen, A. Ahmed, T. V. Thang, and J. Park, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Transactions on Power Electronics,* vol. 30, no. 5, pp. 2445-2455, 2015, doi: 10.1109/TPEL.2014.2353417.

[13] J. O. Gonzalez and O. Alatise, "Impact of the Gate Oxide Reliability of SiC MOSFETs on the Junction Temperature Estimation Using Temperature Sensitive Electrical Parameters," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 23-27 Sept. 2018 2018, pp. 837-844, doi: 10.1109/ECCE.2018.8557810.

[14] H. Yano, N. Kanafuji, A. Osawa, T. Hatayama, and T. Fuyuki, "Threshold Voltage Instability in 4H-SiC MOSFETs With Phosphorus-Doped and Nitrided Gate Oxides," *IEEE Transactions on Electron Devices,* vol. 62, no. 2, pp. 324-332, 2015, doi: 10.1109/TED.2014.2358260.

[15] J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018/09/01/ 2018, doi: https://doi.org/10.1016/j.microrel.2018.06.045.

[16] J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC mosfets," *IEEE Transactions on Power Electronics,* vol. 34, no. 6, pp. 5737-5747, 2019, doi: 10.1109/TPEL.2018.2870067.

[17] Z. Chbili *et al.*, "Modeling Early Breakdown Failures of Gate Oxide in SiC Power MOSFETs," *IEEE Transactions on Electron Devices,* vol. 63, no. 9, pp. 3605-3613, 2016, doi: 10.1109/TED.2016.2586483.

[18] J. Hu, O. Alatise, J. A. O. González, R. Bonyadi, L. Ran, and P. A. Mawby, "The Effect of Electrothermal Nonuniformities on Parallel Connected SiC Power Devices Under Unclamped and Clamped Inductive Switching," *IEEE Transactions on Power Electronics,* vol. 31, no. 6, pp. 4526-4535, 2016, doi: 10.1109/TPEL.2015.2477831.

[19] J. Lu, X. Tian, S. Lu, H. Zhou, Y. Zhu, and Z. Han, "Dynamic avalanche behavior of power MOSFETs and IGBTs under unclamped inductive switching conditions," *Journal of Semiconductors,* vol. 34, no. 3, p. 034002, 2013/03 2013, doi: 10.1088/1674-4926/34/3/034002.

[20] J. Wei *et al.*, "Investigations on the Degradations of Double-Trench SiC Power MOSFETs Under Repetitive Avalanche Stress," *IEEE Transactions on Electron Devices,* vol. 66, no. 1, pp. 546-552, 2019, doi: 10.1109/TED.2018.2875080.

[21] X. Zhou *et al.*, "A Deep Insight Into the Degradation of 1.2-kV 4H-SiC mosfets Under Repetitive Unclamped Inductive Switching Stresses," *IEEE Transactions on Power Electronics,* vol. 33, no. 6, pp. 5251-5261, 2018, doi: 10.1109/TPEL.2017.2730259.

[22] S. Liu, C. Gu, J. Wei, Q. Qian, W. Sun, and A. Q. Huang, "Repetitive Unclamped-Inductive-Switching-Induced Electrical Parameters Degradations and Simulation Optimizations for 4H-SiC MOSFETs," *IEEE Transactions on Electron Devices,* vol. 63, no. 11, pp. 4331-4338, 2016, doi: 10.1109/TED.2016.2604253.

[23] J. Ortiz Gonzalez, R. Wu, S. N. Agbo, and O. Alatise, "Robustness and reliability review of Si and SiC FET devices for more-electric-aircraft applications," *Microelectronics Reliability,* vol. 100-101, p. 113324, 2019/09/01/ 2019, doi: https://doi.org/10.1016/j.microrel.2019.06.016.

Chapter 4. Short Circuit Performance of SiC Cascode JFETs

4.1. Introduction

Short circuits occur in power electronics when there is a malfunction either in the gate driver systems or on the load. A malfunction in the gate driver system can cause two devices in the same phase leg to turn-on simultaneously thereby causing a short circuit path across the DC link. Similarly, a malfunction in the load can cause a line-to-line short at the converter terminal, thereby causing a DC link voltage drop across the device while it is conducting the rated current. In both instances, the device is subjected to simultaneously high current and voltage thereby causing very significant instantaneous power dissipation. The high-power dissipation will cause a junction temperature excursion which can damage the device if the critical temperature limit is exceeded. Since gate driver or load malfunctions cannot be completely ruled out in the operation of power electronic systems, power devices are required to be able to withstand a certain duration of short circuit energy. The metric used to measure this is called the Short Circuit Withstand Time (SCWT). The SCWT is typically required to be a few microseconds up to ten microseconds for power devices. The short circuit ruggedness of silicon devices has been investigated over several decades, however, given the relatively recent arrival of SiC power devices, less is known about their short circuit ruggedness. It has been reported that the smaller die sizes in SiC MOSFETs (resulting from better specific ON-state resistance) results in higher thermal impedance and therefore higher junction temperatures [1]. The higher junction temperatures therefore limit the SCWT compared to comparatively rated silicon devices with lower thermal impedances. Hence, the advantage of small die size which results in small switching energy is at the cost of reduced SCWT due to higher junction temperatures resulting from higher thermal impedance. Another critical factor that has been reported to limit the SCWT of SiC MOSFETs is poor quality gate oxide compared to silicon MOSFETs and IGBTs [2-8]. The quality of the gate oxide interface in SiC MOSFETs is reported to be lower than that of silicon MOSFETs due to the higher magnitudes of interface trap densities, fixed oxide charge and other oxide trapped

charges [9-12]. This low-quality oxide interface leads to threshold voltage instability as well as a more easily damaged gate oxide during the short circuit event [7, 13-17].

Two failure modes have been identified in SiC MOSFETs undergoing short circuit stress tests [18]. The first failure mode corresponds to devices tested with a high rate of short circuit power over a small duration. Here the short circuit test is performed at higher drain source voltages. The failure mode in this condition usually results in a drain-source short circuit resulting from thermal runaway. A large tail current is usually observed at the end of the short circuit pulse indicating uncontrolled carrier generation resulting from high junction temperatures. The other short circuit failure mode corresponds to devices subjected to a low rate of short circuit power over a longer short circuit duration. In this test, the drain-source voltage is reduced so that longer short circuit durations are observed. In this failure mode, the gate oxide of the SiC device fails due to excessive heat generation and carrier tunnelling at the drain-end of the MOSFET channel.

Investigation into short circuit in SiC power devices have been reported previously. In [19], short circuit robustness of SiC MOSFETs were demonstrated along with an estimation of the junction temperature during the short circuit operation at 75 °C and 150 °C. The devices tested withstood a short circuit energy of 1.39 J and 1.24 J at 75 °C and 150 °C respectively. Short circuit characterisation in high voltage SiC MOSFETs and stand-alone SiC JFETs showed superior performance of JFETs because of its high mobility channel and negative temperature coefficient[20]. The SCWT of 1200 SiC MOSFET are investigated with a voltage much smaller than the device limits (0.33x of the DUT rated voltage), with an increase in the drain current and a tail current demonstrated close to failure. This is attributed to hole current and trapping effects at the SiC/SiO_2 interface[21]. A Similar failure mode was recorded for low to medium voltage SiC MOSFETs[22]. In [23], short circuit measurements were performed on 10kV/10kA SiC MOSFETs with a DC link voltage of 6 kV. A SCWT of 8.6 µs was measured with a maximum short circuit energy of 10.7 J. The failure mode was excessive drain leakage current after turn-off indicating uncontrolled carrier generation in the depletion region due to high junction temperatures. Degradation of the source metallisation were also reported with no recorded gate degradation unlike the case of the low to medium voltage SiC MOSFET devices. In [24], short circuit measurements were performed on 4.6 kV SiC DMOSFETs with a short circuit drain voltage of 2.1 kV and SCWT between 4 µs and 13 µs was reported. The researchers performed short circuit tests on SiC MOSFETs with different channel lengths and showed that the SCWT increased with the channel length thereby demonstrating the trade-off between channel resistance and SCWT. It was also shown that negative gate turn-off voltages increased the SCWT as well as reduced V_{GS} drive voltages. The failure during short

circuit operation was proven to be device structure dependent in [25], where the failure of a SWITCH (SBD-wall-integrated trench) MOSFET was demonstrated to be caused by damage to the aluminium metallisation using TCAD simulation and SEM imaging. The single and repetitive short circuit robustness of SiC MOSFETs were compared with that of SiC Cascode JFET in [26] with post-test static characterisation to investigate drift in electric parameters. The SiC cascode devices tested presented less degradation than SiC MOSFETs, with a peculiar reduction in leakage current after short circuit tests.

With the widespread preference of SiC MOSFET due to its normally-off operation more research into its robustness have been carried out. As has been stated previously, SiC MOSFETs suffer premature failure under short circuit conditions due to the poorer quality gate oxide. However, SiC Cascode JFETs, as was demonstrated in previous chapters use a low voltage silicon MOSFET as the input, hence, do not suffer from poor gate dielectric problems. This is an advantage for SiC Cascode JFETs. However, the thermal impedance of SiC Cascode JFETs remains high due to the high performance of the normally ON SiC JFET. Furthermore, the internal connection between the LV silicon MOSFET and the HV SiC JFET can cause reliability issues (i.e., a failed JFET gate path) under short circuit conditions. The goal of this chapter is to evaluate the performance of commercially available SiC Cascode JFETs under short circuit conditions in comparison with comparatively rated silicon and SiC power devices. Hence, Short circuit measurements were performed on SiC Cascode JFETs, SiC Planar MOSFETs, SiC Trench MOSFETs, silicon MOSFETs, silicon super-junction MOSFETs. Finite element simulations are used to understand the failure modes of SiC Cascode JFETs under short circuit conditions.

4.2. Theory of Short Circuit Current Flow

The main characteristics of the short circuit current are,

a) The peak short circuit current is determined by the limiting inductance in the current flow path. In some applications, inductors are placed in series with the device specifically for the purpose of limiting short circuit currents. Although, this will be at the expense of some switching loss in normal device operation.

b) The peak short circuit current will depend on the turn-on dI/dt, which will depend on the MOSFET switching speed. The MOSFET switching speed will depend on device parameters like the threshold voltage, transconductance and input capacitance.

c) The temperature excursion of the short circuit pulse will depend on the short circuit power and the thermal impedance of the device channel area. Since the short circuit pulse is typically on the order of microseconds, there will be insufficient time for the heat generated

in the junction to diffuse into the device bulk and into the heatsink within the duration of the pulse.

d) How the short circuit is limited will depend on the short circuit resistance of the device. This is different from the ON-state resistance quoted on datasheets since that resistance is measured at low drain source voltage. Hence, the short circuit resistance is the MOSFET saturation resistance not usually easily calculable from the output characteristics on the datasheets since the measurements provided are limited to low V_{DS} compared to the short circuit V_{DS}. The thermal impedance and short circuit resistance is determined by the device mobility vs temperature characteristics reported previously, which demonstrates the change of the dominant carrier scattering mechanisms at difference temperature[20, 27, 28].

e) The short circuit resistance is specific to the device technology and will depend on the chip size. Typically, there is a trade-off between conduction losses (which reduce with ON-state resistance) and short circuit performance (which will also reduce with ON-state resistance). Key to limiting short circuit current is a high short circuit resistance capable of supressing the short circuit current, however, this will usually come with high ON-state resistance.

Consider the equivalent circuit in Figure 4.1 for the MOSFET showing the parasitic capacitance (C_{GS}, C_{DS} and C_{GD}) and the parasitic inductances (L_G, L_S, and L_D). As the top switch is closed (V_D corresponds to the cathode of the top switch, and L_{circ} & R_{circ} are the circuit track impedances), a short circuit will flow through the device. However, the rate at which the top switch is closed will depend on the switching time constant of the device under short.

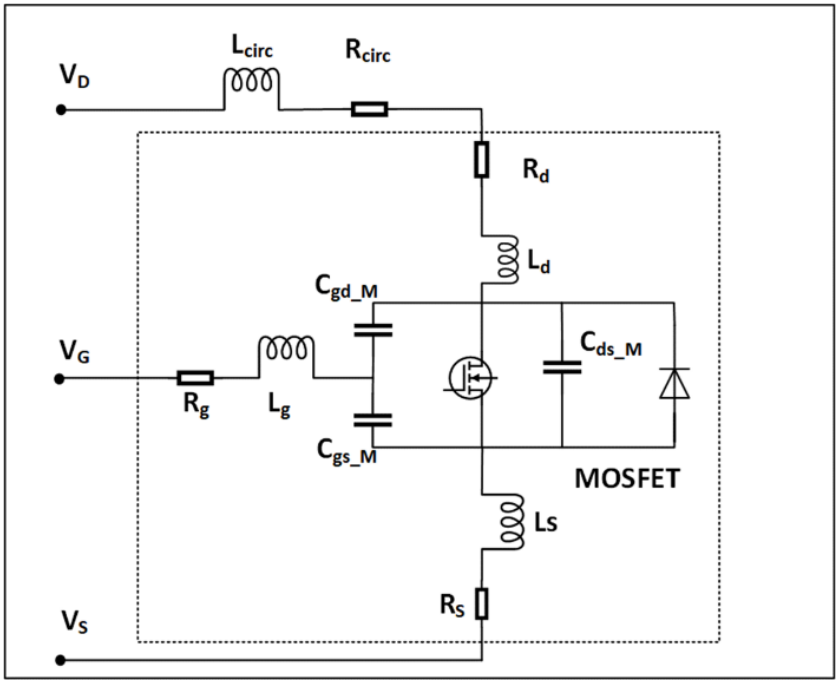


Figure 4.1 MOSFET equivalent circuit showing device parasitic capacitances and inductances.

Applying KVL in the gate loop yields Eq. 4.1,

$$V_{GG} = L_G \frac{di_G}{dt} + i_G R_G + \frac{1}{C_{GS}} \int i_G \, dt + L_s \frac{di_G}{dt} + i_G R_S$$

Eq. 4.1

When the V_{GS} exceeds the device threshold voltage, a short circuit current will flow equivalent to the MOSFET saturation current.

$$i_{SC} = \frac{\beta}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) = \frac{\beta}{2}(V_G - V_S - V_{TH})^2(1 + \lambda V_{DS})$$

Eq. 4.2

In Eq. 4.2 above, the channel length modulation factor (λ) is critical in determining the short circuit resistance. The channel length modulation factor occurs as a result of drain induced barrier lowering, which is essentially increased conductance of the MOSFET in saturation due to channel length reduction from drain depletion width extension into the channel.

$$(L_s + L_d + L_{circ}) \frac{di_{SC}}{dt} + i_{SC}(R_{SC} + R_{str}) = V_{DC}$$

Eq. 4.3

Where R_{str} = (R_s + R_d + R_{circ}) is the total stray resistance in the drain-source loop.
The short circuit energy can be estimated by Eq. 4.5Eq. 4.4]. From t_1 to t_2 is the duration of short circuit.

$$E_{SC} = \int_{t_1}^{t_2} I_D . V_{DS} \, dt$$

Eq. 4.4

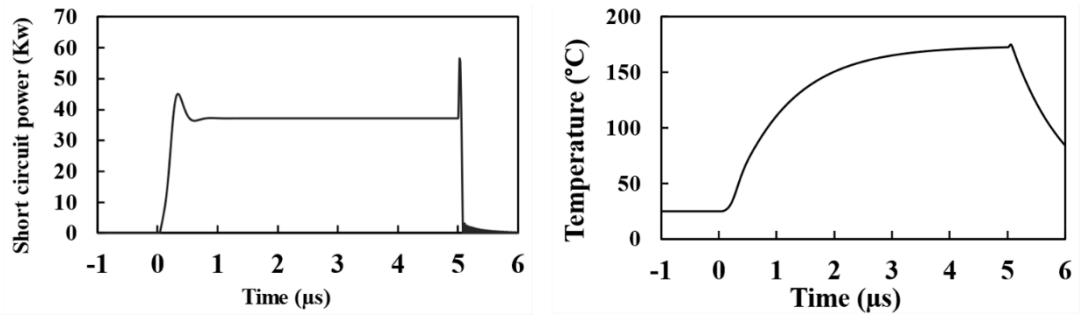
- ## SPICE Simulations of Short Circuits

To estimate the junction temperature of the device under short circuit measurements, the compact models have been performed in LT-SPICE. The simulator will solve compact device equations shown in Eq. 4.2] and use the thermal impedance characteristics provided by the manufacturer to predict the average junction temperature. Table 4-1 shows the parameters used in the SPICE simulation thermal network which is implemented as a Cauer network.

Table 4-1 Thermal network parameters from manufacturer used in SiC MOOSFET simulations.

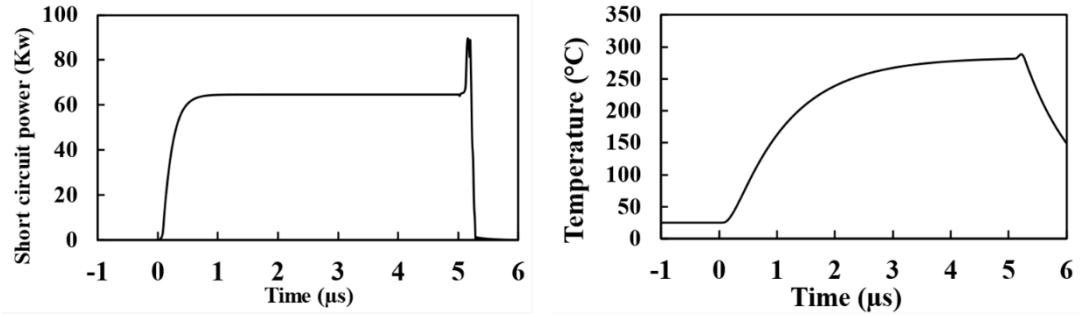
R_{TH1}	R_{TH2}	R_{TH3}	R_{TH4}	R_{TH5}	C_{TH1}	C_{TH2}	C_{TH3}	C_{TH4}	C_{TH5}
$1.24x10^{-2}$	$6.5x10^{-2}$	0.17	0.177	0.185	503u	1.59m	9.55m	38m	44.6m

Figure 4.2(a) & Figure 4.3(a) show the instantaneous short circuit power (calculated by multiplying the short circuit current by the short circuit voltage) for the SiC MOSFET and the SiC Cascode JFET, while Figure 4.2(b) & Figure 4.3(b) show the simulated junction temperature rise due to the short circuit power.



(a) (b)

Figure 4.2 Spice short circuit simulation of SiC MOSFET (a) Short circuit power (b) Simulated Junction Temperature rise.



(a) (b)

Figure 4.3 Spice short circuit simulation of SIC Cascode JFET (a) Short circuit power (b) Simulated Junction Temperature rise.

According to Figure 4.2(b) and Figure 4.3(b), the peak junction temperature rises for the SiC MOSFET and SiC Cascode JFET are about 175 °C and 288.5 °C respectively. This is the average junction temperature assuming that the heat generation rate is evenly distributed within the volume of the device. In reality, the heat generation rate is concentrated in certain areas which result in hot-spots. The temperature of these hot-spots could easily be twice those predicted by compact circuit simulators. Furthermore, a significant drawback of predicting short circuit junction temperatures using thermal impedance characteristics is due to the time limited duration of the short circuit pulse. Short circuit pulses occur over a few microseconds whereas thermal impedance characteristics are more suited to simulating junction temperature rise over several seconds. Hence, within the short circuit pulse duration, it can be assumed that the heat does not have sufficient time to diffuse from the junction to the heatsink via the substrate. Thus, using the thermal impedance characteristic underestimates the hot-spot temperature because it assumes sufficient time for heat diffusion across all the device thermal layers.

For this reason, SILVACO TCAD Finite Element Simulator was used to simulate thermal transient characteristics of power devices under short circuits. By defining the separate layers

of the device and solving the device equations coupled with the heat flow equation, it is possible to show the heat distribution within the different layers of the power device.

4.3. Short Circuit Benchmarking for 650 V Power Devices

The short circuit measurement system is shown in Figure 4.4, with the electrical schematic shown in Figure 4.5(a). It comprises of a DC voltage source (400 V), DC link capacitors, a control IGBT and the Device Under Test (DUT). The DUT is one of several devices in Table 4-2 and the control IGBT is a 1200 V/1000 A IGBT from Infineon with datasheet reference FF1000R17IE4. All DUTs in Table 4-2 are rated at 650 V with comparable current conduction capabilities (between 20 A and 30 A). The research objective here is to benchmark the short circuit performance of the SiC Cascode JFET against comparatively rated contemporary silicon and SiC devices. A DSP is used to control the gate drivers of the IGBT and the DUT in a non-destructive short circuit configuration [29]. The IGBT is turned ON before the DUT and turned-OFF after the DUT thereby ensuring the DUT is disconnected from the power supply after the defined short circuit test duration, as shown in the gate pulse sequences shown in Figure 4.5(b). The IGBT is a 1000 A power module, hence, is not susceptible to failure at the short circuit current levels of lower voltage DUTs.

Table 4-2 Power Devices and parameters from datasheet

Parameter	SiC Planar	SiC Trench	SiC Cascode	SJ MOSFET	IGBT	Si MOSFET
Pulsed Drain current (A)	51	75	65	137	80	100
Current rating at 25C (A)	22	30	31	43.3	40	33
Current rating at 100 C (A)	16	21	23	27	20	21
R_{TH} (K/W)	1.53	0.86	0.65	0.32	1.04	0.45
C_{ISS} (nF)	0.64	0.571	1.5	4.44	1.06	3.454
R_{DSON} (mΩ)	120	80	80	80		85
Die Size (mm^2)	2.89	6.25	2.92	41.7	9.71	31.6

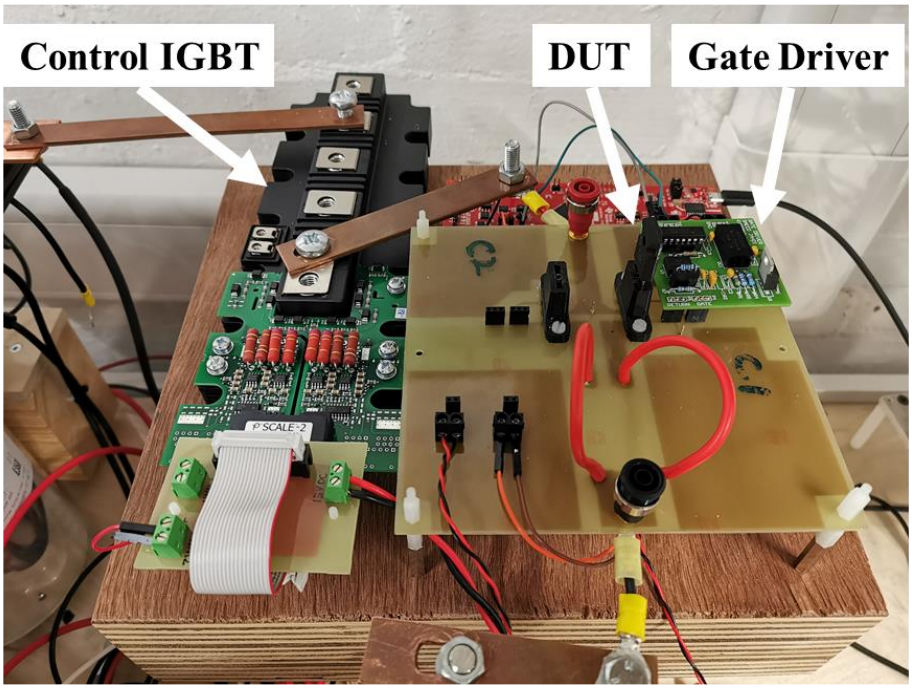


Figure 4.4 Short Circuit Measurement Test system

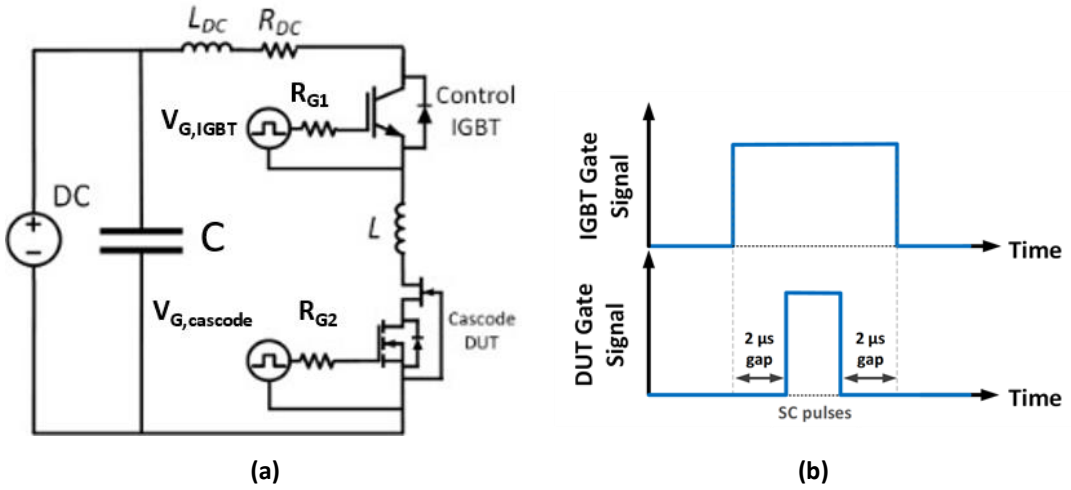
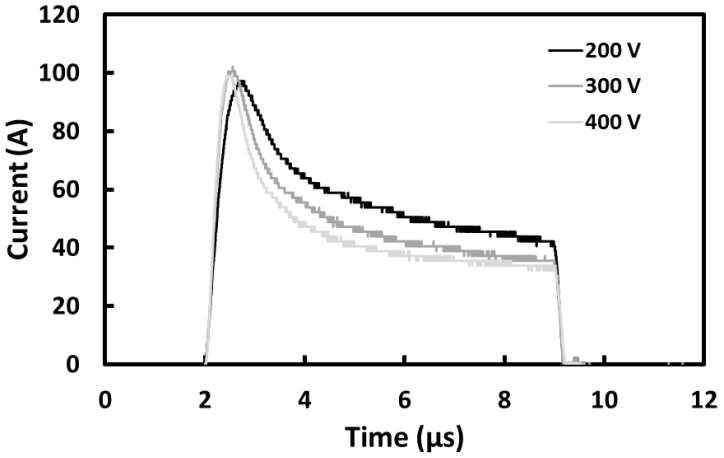


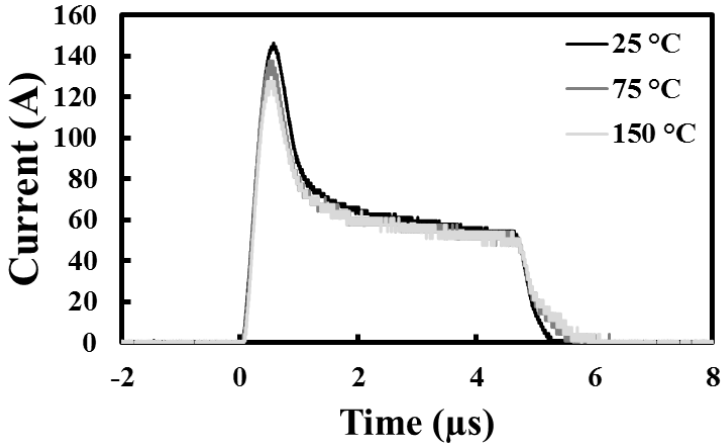
Figure 4.5(a). Short circuit test schematic (b) Gate pulses for short circuit measurements

To determine the short-circuit withstand time, the pulse width in Figure 4.5(b) is increased gradually in 0.5 µs time steps until the device fails at its thermal limit. Figure 4.6(a) shows the measured short circuit characteristics for the SiC Cascode JFET at different drain source voltages while Figure 4.6(b) shows similar measurements at varying initial junction temperatures. In Figure 4.6(a), the short circuit charge and energy is calculated by integrating the short circuit energy over time. As the V_{DS} increases from 200 V to 400 V, the short circuit charge changes from 60 µC to 30 µC. The reduction in the short circuit charge with increasing V_{DS} is due to the higher instantaneous short circuit power resulting from the increase in the short circuit energy as V_{DS} is increased. This increase in short circuit power will translate into

higher junction temperatures and consequently higher short circuit resistance which limits the current. Figure 4.6(b) shows that increasing the initial junction temperature reduces the peak short circuit current from 125 A to 145 A for the Cascode JFET. A slightly higher tail current is seen in the short circuit characteristics measured with the initial junction temperature of 150 °C.



(a)

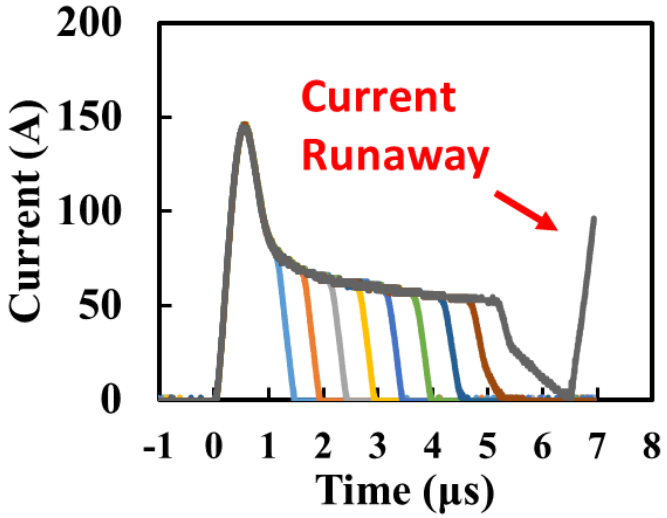


(b)

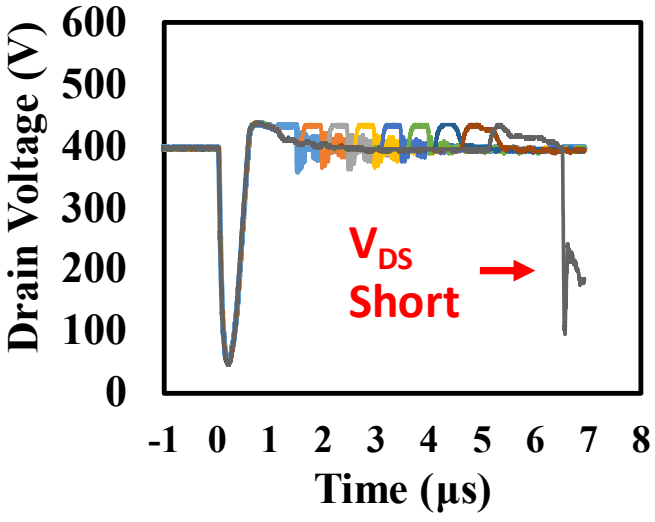
Figure 4.6 Short circuit current transients for the SiC Cascode JFET at (a) different VDS voltages (b) different initial Junction Temperatures

Figure 4.7(a) shows measurements of short circuit currents in the SiC Cascode JFET for increasing pulse durations. It is observed that the device fails with drain-source current runaway. Subsequent failure analysis revealed that the drain-source terminals of the Cascode device where short-circuited with the gate-source terminals still functional. Figure 4.7(b) shows the corresponding drain-source voltage measurements showing a precipitous reduction in V_{DS} although not to zero as would be expected in a proper drain-source short-circuit. Finite element simulations will show that this is due to the JFET turning ON. Also observable in the short circuit V_{DS} characteristics of the DUT are voltage dips and spikes

during the turn-on and turn-off of the short circuit current. The voltage drop at short circuit turn-on is due to the positive dI/dt across the drain inductance L_{DC} shown in Figure 4.5(a). Since the sum of the voltage across this inductance (V_L) and the voltage across the DUT must always equal the supply voltage, hence, as V_L rises, the voltage across the DUT must drop. Similarly, at turn-off, the negative short circuit dI/dt causes the voltage V_L to become negative, thereby adding to the DUT voltage. The ringing in the voltage is due to resonance between the DC link capacitance and the parasitic inductance in the path of the short circuit. Figure 4.8 shows the corresponding gate-source voltage measurements for the SiC Cascode JFET. Unlike the failure modes in SiC MOSFETs under short circuits reported in previous literature, there is no indication of device failure on the gate voltage transients.



(a)



(b)

Figure 4.7 Short circuit transients for the SiC Cascode JFET under different pulse durations until failure (a) Short circuit current (b) Short circuit VDS

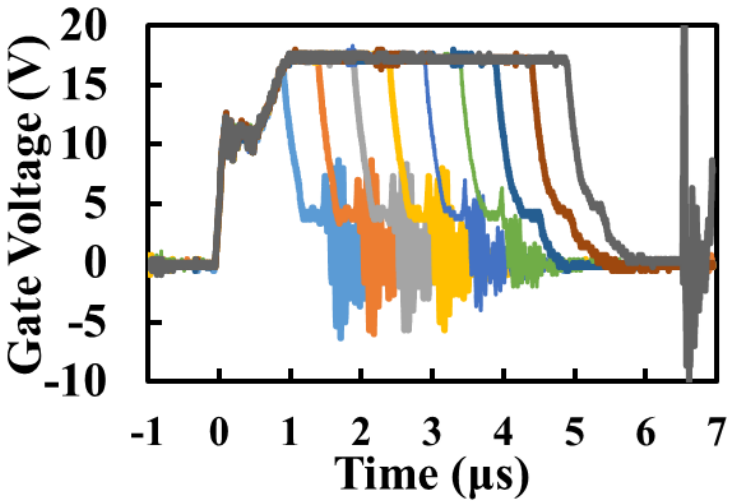


Figure 4.8 Short circuit VGS transients for the SiC Cascode JFET under different pulse durations until failure.

The short circuit measurements have been repeated for all the devices in Table 4-2 with the SCWT, peak short circuit current, short circuit energy density and the SCWT normalized by chip size all calculated from the measurements. Figure 4.9 shows the last pass short circuit currents for all the DUTs, with the wide variation in short circuit performance for the different technologies demonstrated. There is wide variation in the peak short circuit currents, energy densities and SCWT, with the SiC Cascode JFET being outperformed by all technologies except the SiC Planar MOSFET.

Figure 4.10(a) shows the measured peak short circuit currents for all the DUTs, while Figure 4.10(b) shows the SHORT CIRCUIT energy density, Figure 4.10(c) shows the measured SCWT while Figure 4.10(d) shows the SCWT normalized by chip size. The SiC Cascode JFET, as far as SCWT is used as a metric, is the least performing device being closely matched with the planar SiC MOSFET. However, when chip size is considered (short circuit energy density and SCWT/Area), the SiC Cascode JFET becomes the highest performing device. The reduced SCWT performance of the SiC Cascode JFET is related to the reduced chip size.

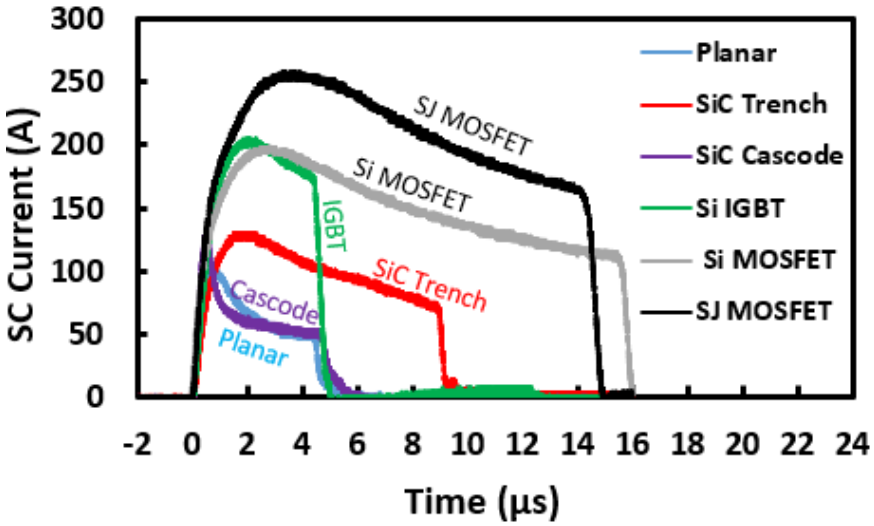
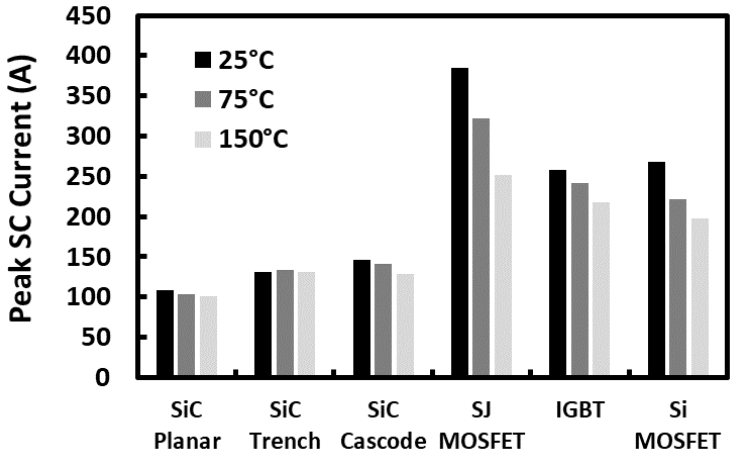
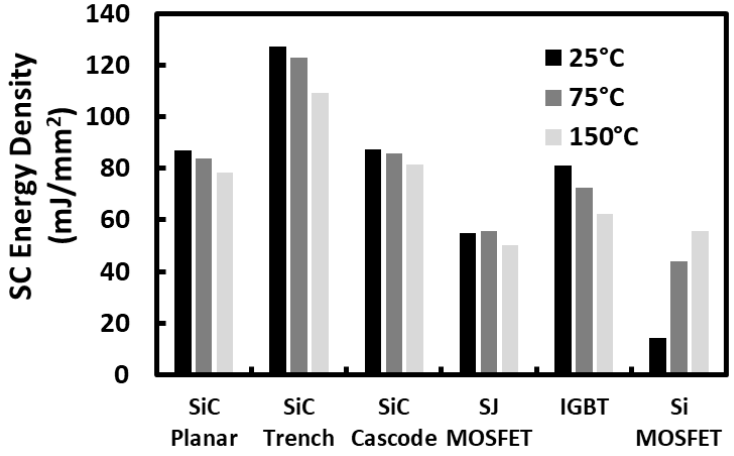


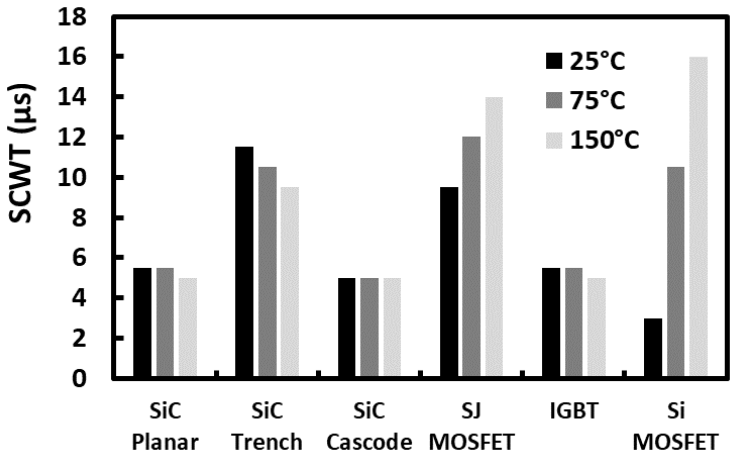
Figure 4.9 Short circuit currents for all DUTs in Table 4-2



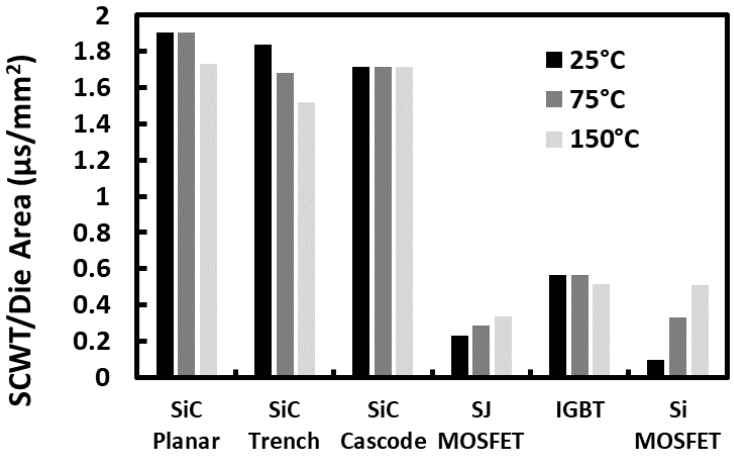
(a)



(b)



(c)



(d)

Figure 4.10 Peak SHORT CIRCUIT Current for all technologies (b) SHORT CIRCUIT Energy density for all technologies (c) SCWT for each technology (d) SCWT normalized by chip size.

Unlike the SiC Planar and Trench MOSFETs, the SiC Cascode JFET fails with a drain-source short. Also, the SiC Cascode JFET is the only device that shows a SCWT independent of initial junction temperature. This indicates that the failure mode of the SiC Cascode JFET is different from the other SiC devices. In section 4.5 finite element simulation is used to further investigate the failure mode of the SiC Cascode JFET under short circuit.

4.4. Simulations of short circuit in SiC MOSFETs

- Impact of circuit parameters on SiC MOSFET short circuit current.

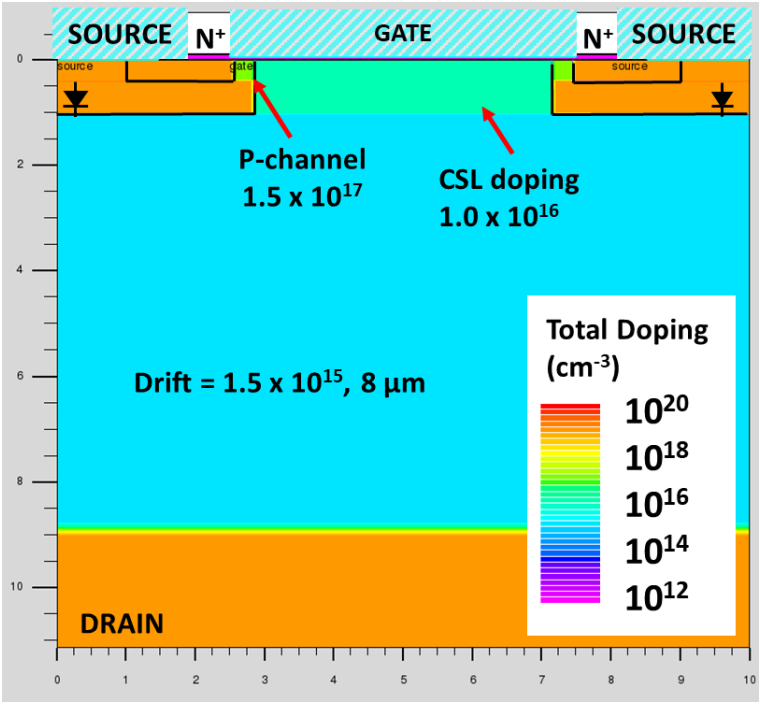


Figure 4.11. SiC MOSFET simulated in SILVACO TCAD

This section investigates variations in the circuit conditions in which the power devices are operated (e.g., Gate voltage, V_{GS}, Case temperature, T, Gate resistance, R_G,). Experiments and Finite element simulations in SILVACO were used to investigate the short circuit characteristics of SiC MOSFET power devices and how various parameter variations affect short circuit performance. All the simulations were performed using the structure in Figure 4.11. For the short circuit simulations, the physical models CVT (accounts for the inversion layer mobility), BGN (accounts for bandgap narrowing at high temperatures), SRH (accounts for carrier lifetime), ANALYTIC (accounts for the low field mobility), FLDMOB (accounts for field dependent effective mobility), and AUGER (accounts for Auger recombination at high carrier densities) were enabled. The heat flow within the device is calculated by enabling the LAT.TEMP model statement. To further increase the accuracy of the simulated chip junction temperature, the temperature dependent heat capacity of 4H-SiC is specified using values from the literature [30].

Impact of VGS on short circuit transient.

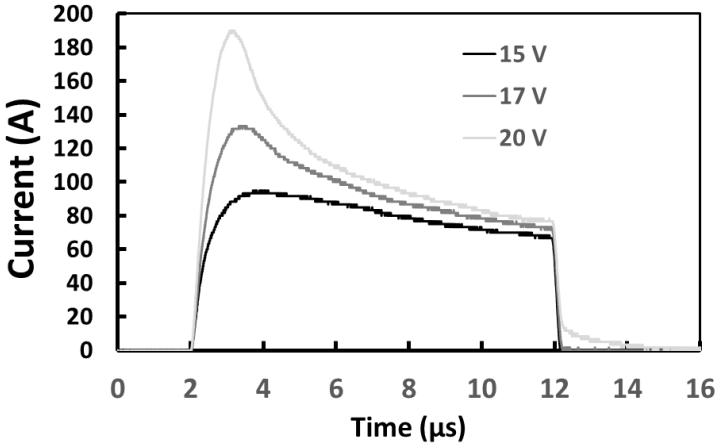
As the gate source voltage is increased, the channel resistance reduces according to Eq. 4.5 and hence, the short circuit current increases. This increase in the channel resistance reduces the short circuit current. Hence, the overall impact of a reduction in the V_{GS} voltage is a

corresponding reduction in the short circuit current. Figure 4.12 shows experimental results for short circuit measurements on 650V SiC MOSFETs with datasheet reference C3M0120065D. The results show that reducing the V_{GS} reduces the peak short circuit current and reduces the inductive undershoot evident in the V_{DS} transients. Figure 4.13(a) shows the simulated short circuit current and hot-spot temperature for the SiC MOSFET with different V_{GS} voltage (15V, 17V and 20V). Figure 4.13(b) shows the simulated V_{DS} voltage and Figure 4.13(c) shows the simulated V_{GS}.

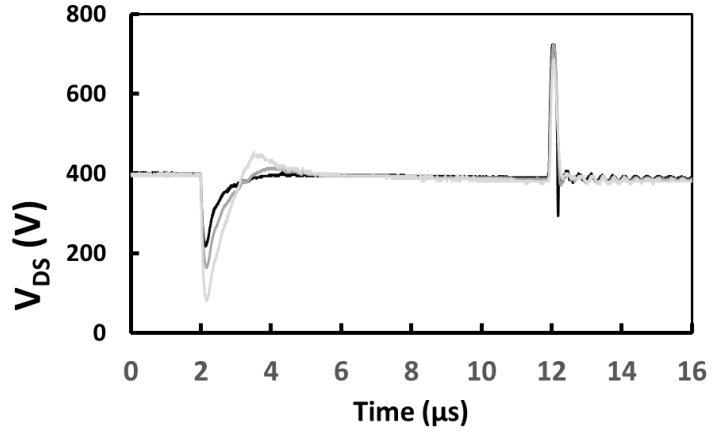
$$R_{DSON} = \frac{L_{ch}}{W\mu C_{OX}(V_{GS}-V_{TH})} + \frac{L_{drift}}{q\mu N_D A}$$

Eq. 4.5

Where L_{ch}, W, L_{drift}, & C_{ox} are channel length, orthogonal channel length, drift layer thickness, and oxide capacitance respectively. μ is the effective mobility and N_D is the drift layer doping.



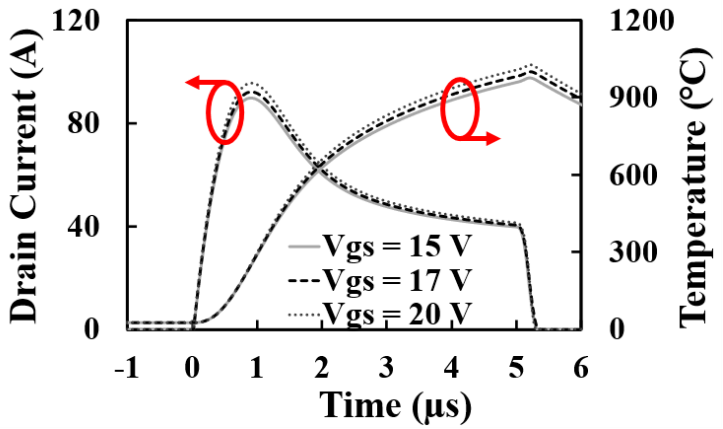
(a)



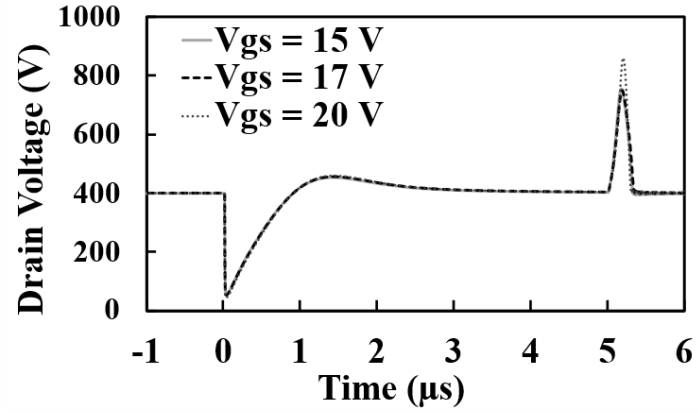
(b)

Figure 4.12 Experimental measurement of short circuit in SiC MOSFET showing the impact of different gate voltages (a) short circuit current (b) short circuit V_{DS}.

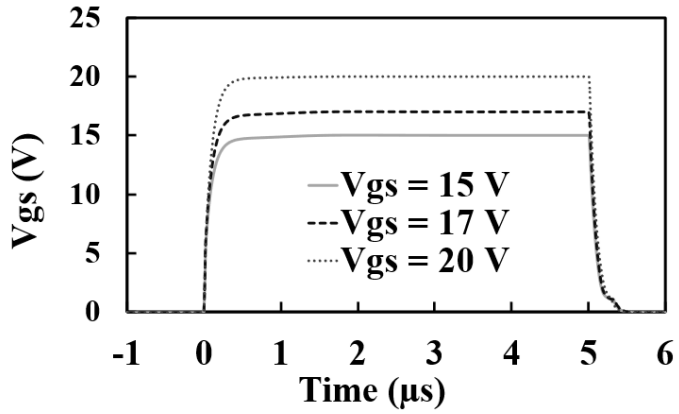
From the simulations presented in Figure 4.13, there is a 3 A and 6 A reduction in the peak short circuit current as the V_{GS} voltage is reduced from 20V to 17V and 15V respectively. This translates to a 28 °C and 52 °C reduction in hot-spot temperature. The V_{DS} undershoot and overshoot during short circuit turn ON and OFF increase with V_{GS} because of the slight increase in turn-on and turn-off dI/dt which is positively correlated with V_{GS}.



(a)



(b)



(c)

Figure 4.13 Short circuit TCAD Simulation of SiC MOSFET showing the Impact of *gate* voltage (a) Short circuit current and hot-spot temperature (b) Drain-source voltage (c) V_{GS} voltage transient of SiC MOSFET.

Impact of external gate resistance (R_G) on short circuit transient:

The external gate resistance (R_G) changes the device switching rate. Hence, as R_G is reduced, the turn-on and turn-off dV/dt and dI/dt increase. The equations relating the current and voltage commutation rates to the gate resistance are shown in Table 4-3 for both turn-on and turn-off. However, for a SiC device with an input capacitance of 640 pF, the additional time that results from increasing the gate resistance from 10 Ω to 100 Ω is 10 ns. Compared to the typical short circuit duration of more than 5 µs, this does not cause a significant time difference assuming a parasitic inductance of 300 nH in the short circuit path. Experimental measurements investigating the impact of the gate resistance on the short circuit currents and voltages on a SiC MOSFET are shown in Figure 4.14. From the measurements, there is no significant impact of the gate resistance on the short circuit characteristics of the device.

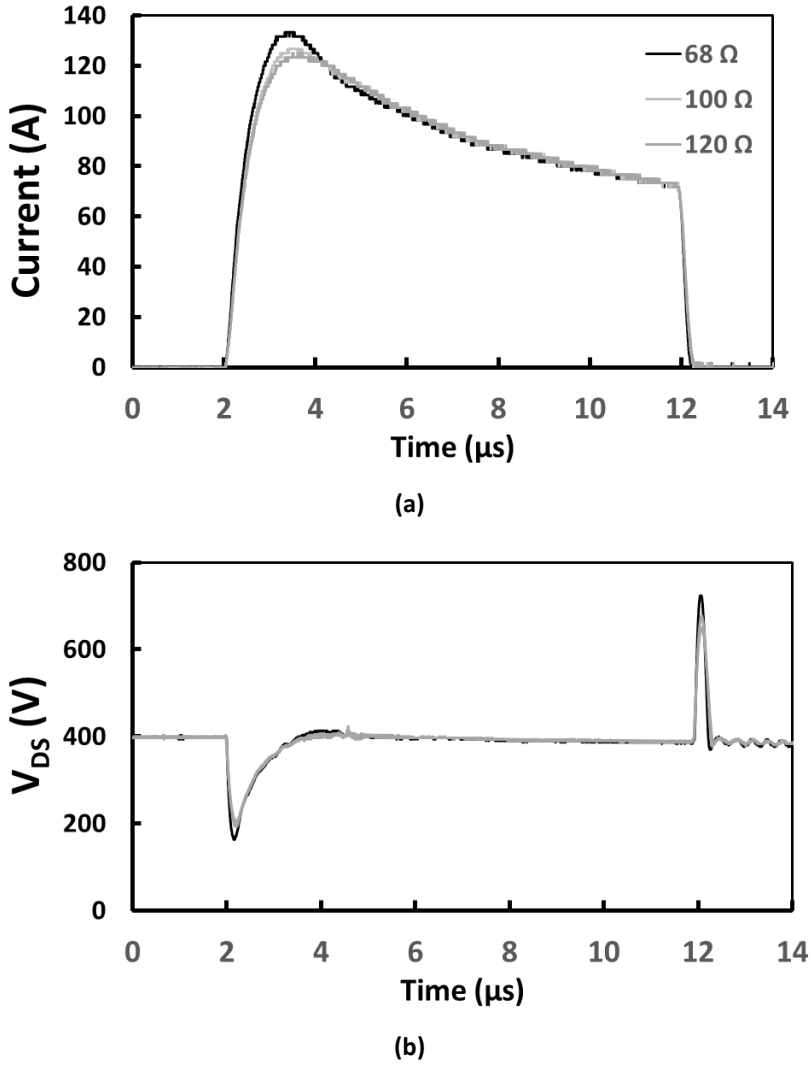


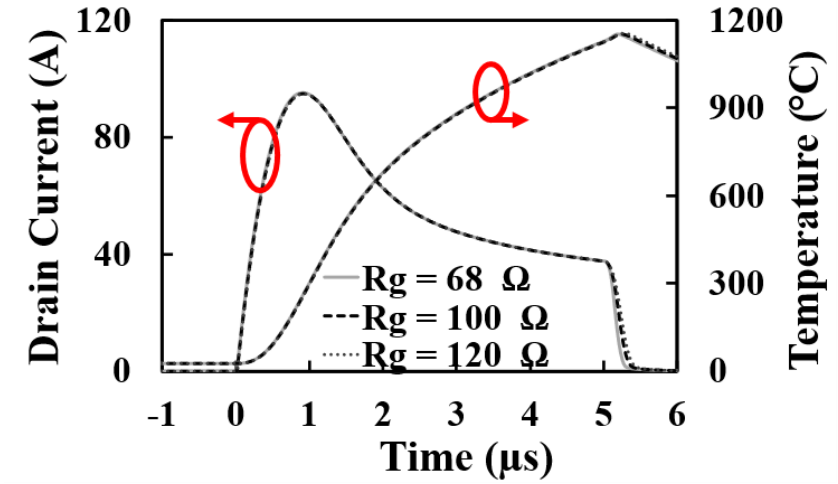
Figure 4.14 Experimental measurement of short circuit in SiC MOSFET showing the Impact of gate resistance (a) short circuit current (b) short circuit V_{DS}.

Table 4-3 Relationship between gate resistance R_G and the device switching rates.

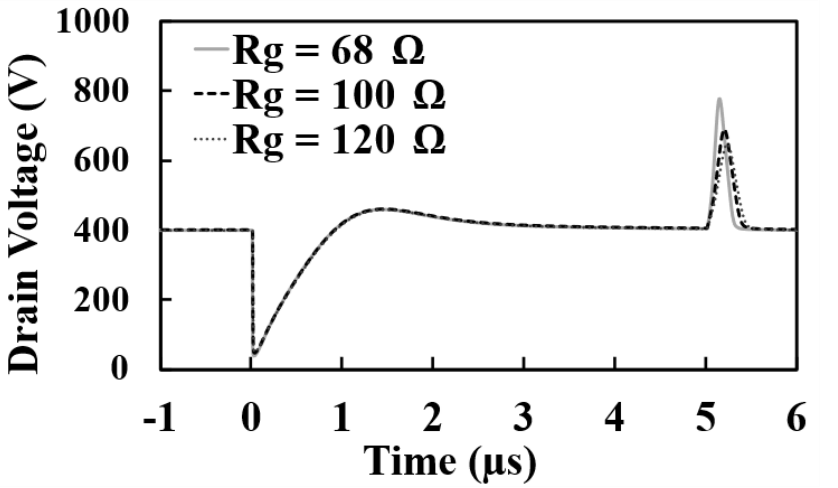
MOSFET Turn ON	MOSFET Turn-OFF
$\frac{dI_{DS}}{dt} = \frac{\beta V_{GG}(V_{GS} - V_{TH})e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}}{R_G(C_{GS} + C_{GD})}$	$\frac{dI_{DS}}{dt} = \frac{-\beta V_{GP}(V_{GS} - V_{TH})e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}}{R_G(C_{GS} + C_{GD})}$
$\frac{dV_{DS}}{dt} = \frac{V_{GG} - V_{GP}}{R_G C_{GD}}$	$\frac{dV_{DS}}{dt} = \frac{V_{GP}}{R_G C_{GD}}$

Where V_{GG} is the applied input voltage, and V_{GP} is miller plateau voltage.

Figure 4.15 shows the simulated impact of R_G on the short circuit V_{DS} characteristics of a SiC MOSFET. As predicted by the theory and demonstrated in the experiments, the simulations also show that changing R_G has no impact on the short circuit current, hot-spot temperatures, and drain-source voltages.



(a)

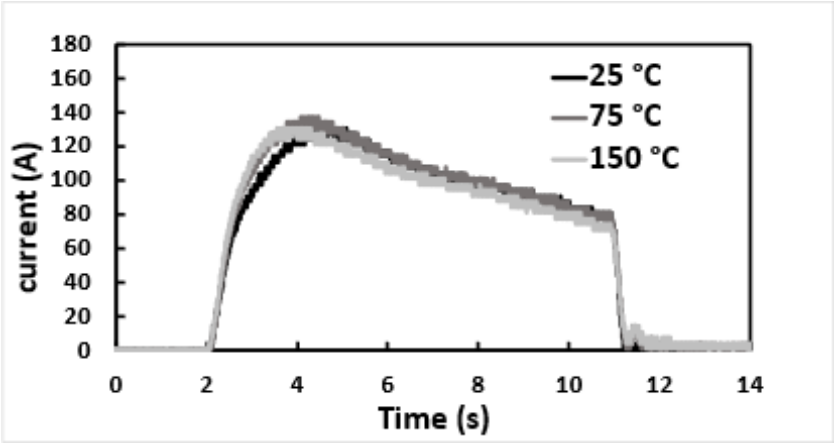


(b)

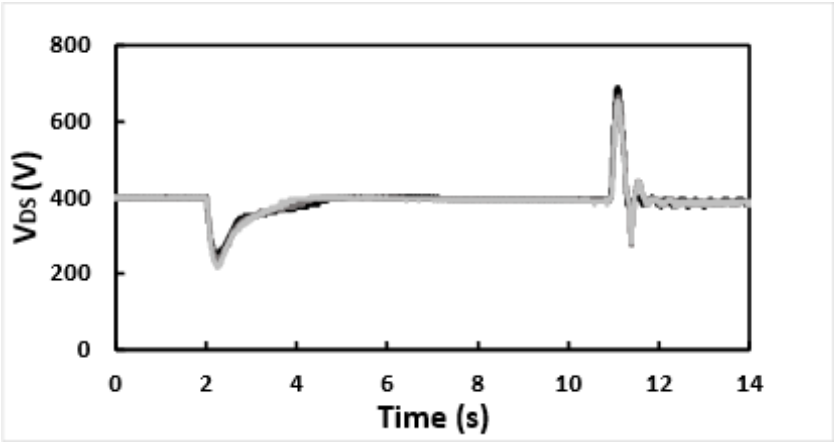
Figure 4.15 Short circuit TCAD Simulation of SiC MOSFET showing the Impact of R_G (a). Short circuit current and hot-spot temperature (b) Drain-source voltage

Impact of Junction Temperature on Short circuit transient:

As the junction temperature increases, the ON-state and short circuit resistance of the device increases therefore limiting the short circuit current. The increase in the short circuit resistance results from reduced effective mobility of the electrons in the MOSFET channel due to increased acoustic phonon scattering. Hence, an increase in junction temperature will lead to a reduction in the peak short circuit current. Figure 4.16 below shows the impact of the junction temperature on the short circuit current of the SiC MOSFET showing a 6.67 A reduction in the peak short circuit current as junction temperature is increased from 25°C to 150°C.



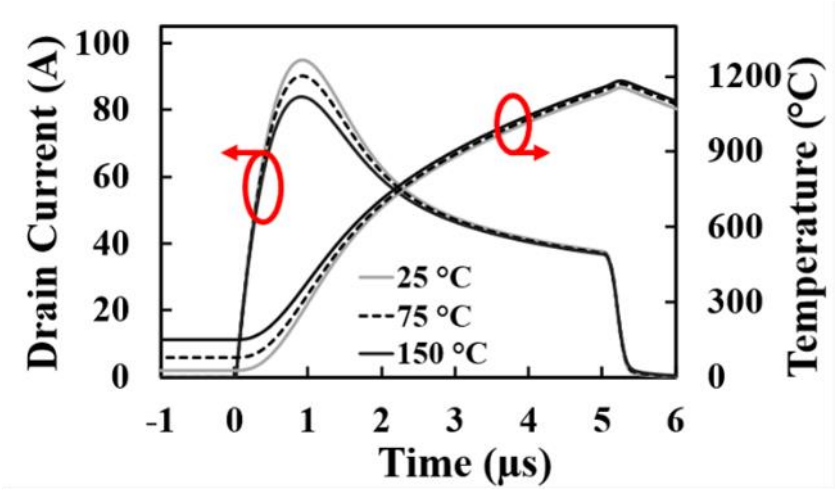
(a)



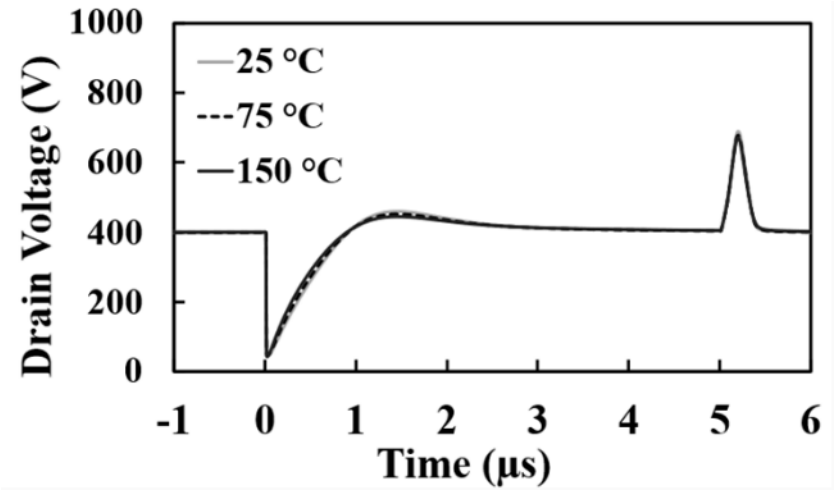
(b)

Figure 4.16 Experimental measurement of short circuit in SiC MOSFET showing the Impact of junction temperature (a) short circuit current (b) short circuit V_{DS}.

The finite element simulator was used to investigate the impact of initial junction temperature on the short circuit characteristics of the SiC MOSFET. Figure 4.17 shows the results of the simulations corroborating the experimental measurements which say that an increase in the junction temperature reduces the peak short circuit current.



(a)



(b)

Figure 4.17 Short circuit TCAD Simulation of SiC MOSFET showing the Impact of device temperature, T_{CASE} (a). Short circuit current and hot-spot temperature (b) Drain-source voltage

- Impact of Fabrication Parameters on Short circuit

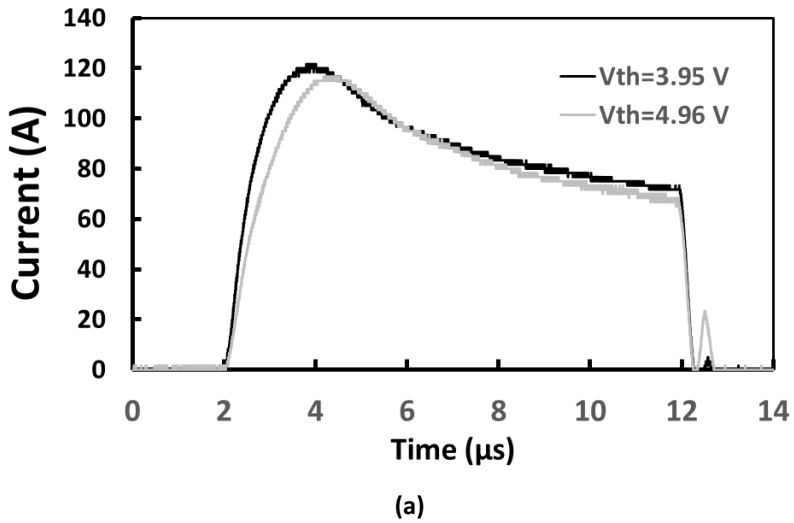
This section demonstrates the impact various fabrication parameters on the short circuit characteristics of SiC power MOSFETs. With SiC technology helping to achieving more compact power systems, the reduction power devices dimensions have seen a massive boost; the scaling has a direct consequence on the variability of the device parameters, especially with the immaturity in SiC processing. This is because device scaling adversely impacts the controllability of the fabrication processes. Also, atomic scale differences have more of an impact on the overall device operation for very small device dimensions. Small differences during the fabrication process steps and process step conditions (i.e., lithography, etch, various process step temperatures, temperature ramp, dose of implantation, implantation energy etc) lead to differences in the device parameters and characteristics[31, 32]. Fabrication parameter variation in devices have previously been reported and classified

into two types: Front-end variability, and Back-end variability. Front end variability is variability resulting from constraints in the control of the device fabrication and happen early in the fabrication process, while Back-end variability occurs while making device interconnects during the manufacturing process[33-37].

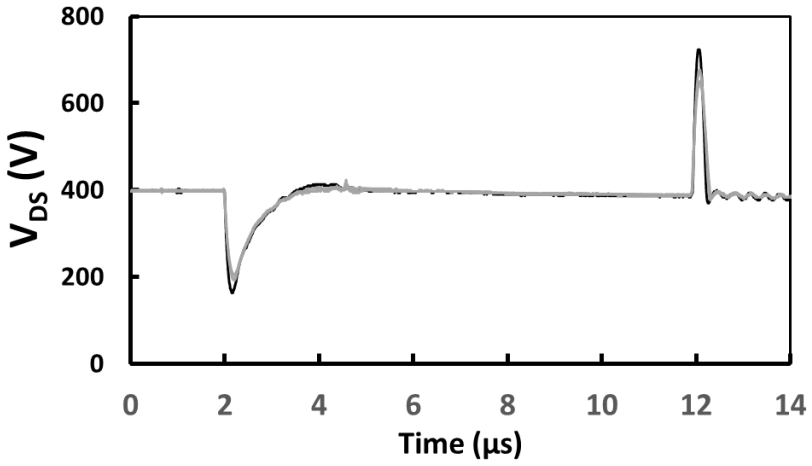
The threshold voltage (V_{TH}) variability of power electronic device is a function of front-end process variability [38]. This occurs with variations of parameters such as trap density variance (fixed oxides charge, interface traps etc.), gate width variations, p-well (channel) doping variation, Current spreading layer (CSL) doping etc. which are impacted by the processing steps and processing step conditions mentioned previously. Back-end variability results in variations in device parasitic parameters (e.g., parasitic inductance and resistance) and R_{ON}[39].

Impact of Threshold Voltage on Short Circuit Transient.

A reduction in the threshold voltage increases the switching rate of the device and hence, the peak short circuit current increases. This is because less V_{GS} voltage is required to drive the device, hence, the device responds with a higher current commutation rate during turn-on. The impact of threshold voltage on turn-on and turn-off dI/dt is shown in Table 4-3. Experimental measurements shown in Figure 4.18 show a slight increase in the peak short circuit current as the threshold voltage is reduced from 4.96 V to 3.95 V. The fast-switching device also exhibits slightly higher V_{DS} undershoot during turn-on and overshoot during turn-off. This is because the higher dI/dt coupled with the drain parasitic inductance induces larger voltages.



(a)



(b)

Figure 4.18 Experimental measurement of short circuit in SiC MOSFET showing the Impact of threshold voltage (a) short circuit current (b) short circuit V_{DS}.

To fully understand the V_{TH} variation effect on power device short circuit, V_{TH} is varied with the help of different fabrication parameters using TCAD simulations. The parameters used are Current spread layer (CSL) doping, Fixed oxide charges, and P-body doping. The equation for the V_{TH} of power MOSFET is given below:

$$V_{TH} = \frac{-Q_{OX}}{C_{OX}} + \frac{2KT}{q}\ln\left(\frac{N_A}{n_i}\right) + \frac{\sqrt{4\varepsilon_{SiC} \cdot K \cdot T \cdot N_A \cdot \ln\left(\frac{N_A}{n_i}\right)}}{C_{OX}}$$

Eq. 4.6

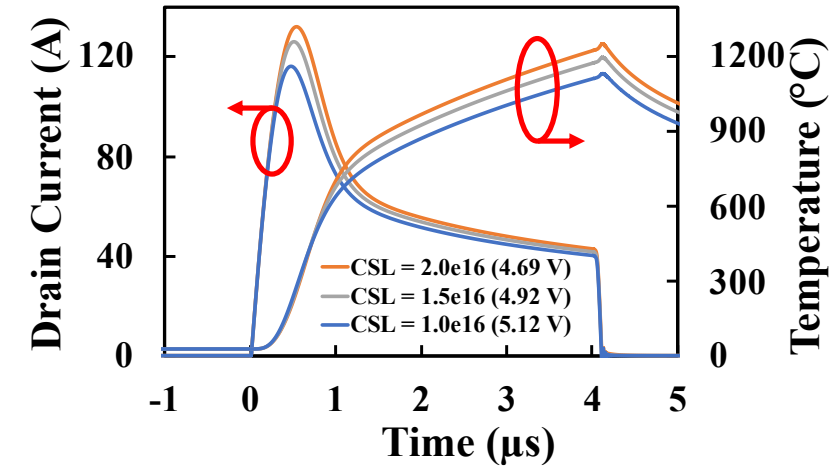
Where Q_{OX} is the total effective charge in the oxide (fixed oxides charge, interface traps etc.), and N_A is the P-body doping[40]. Table 4-4 to Table 4-6 shows the variation in each parameter while every other parameter is kept constant and the corresponding impact on impact V_{TH}. CSL doping, and Fixed oxide charges from Table 4-4 and Table 4-5 display an inverse proportional to the V_{TH}. Conversely, Table 4-6 show a direct proportionality between the values of P-body doping and the V_{TH} as predicted by the MOSFET V_{TH} equation, Eq. 4.6.

Table 4-4 CSL doping variation and impact on V_{TH}.

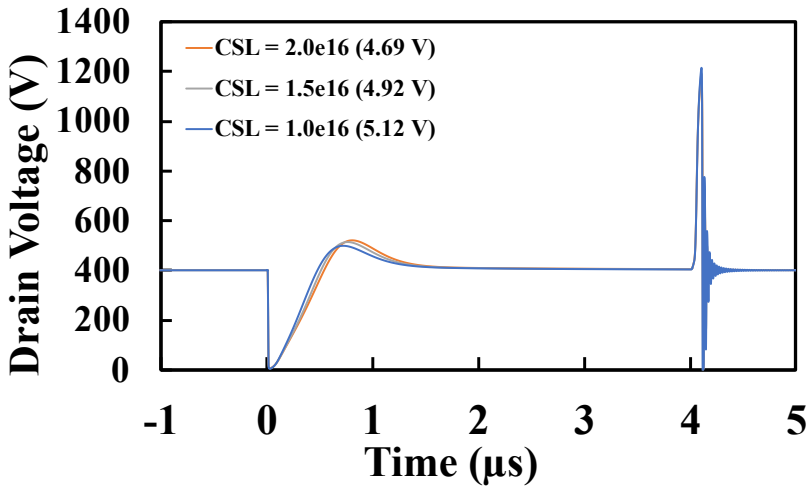
Name	CSL doping (cm^{-3})	V_{TH} (V)
Device 1	$1.0x10^{16}$	5.12
Device 2	$1.5x10^{16}$	4.92
Device 3	$2.0x10^{16}$	4.69

Similar to the experimental measurements, the simulations show the device with the lower V_{TH} has a higher peak short circuit current due to higher short circuit dI/dt, but this is most visible for variations in the CSL. The Impact of Current Spread Layer (CSL) on Short Circuit

transient is presented in Figure 4.19. From the Figure 4.19(a), it is evident that the simulated maximum short circuit current and maximum junction temperature increases with decreasing V_{TH} (increasing CSL doping). The drain voltage is presented in Figure 4.19(b).



(a)



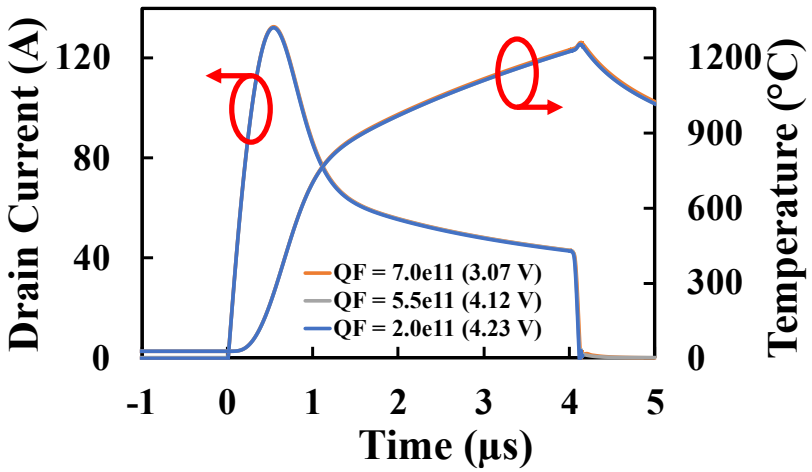
(b)

Figure 4.19 Short circuit TCAD Simulation of SiC MOSFET showing Impact of CSL on (a) Short circuit current and hot-spot temperature (b) Drain-source voltage.

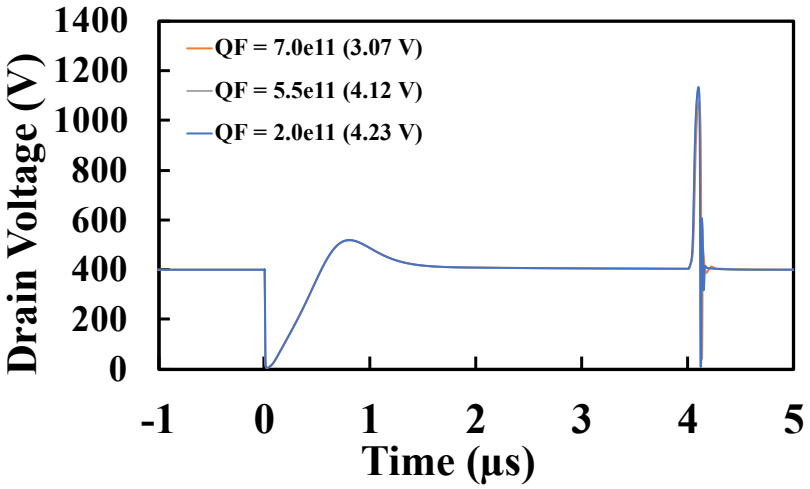
Figure 4.20 shows the Impact of fixed oxide charges on Short Circuit transient, here all three maximum short circuit current and temperature plots of varying V_{TH} are identical. Showing that the V_{TH} unlike the experimental plots.

Table 4-5 Fixed oxide variation and impact on V_{TH}

Name	Fixed oxide charges (cm^{-3})	V_{TH} (V)
Device 1	$2.0x10^{11}$	4.23
Device 2	$5.5x10^{11}$	4.12
Device 3	$7.0x10^{11}$	3.07



(a)



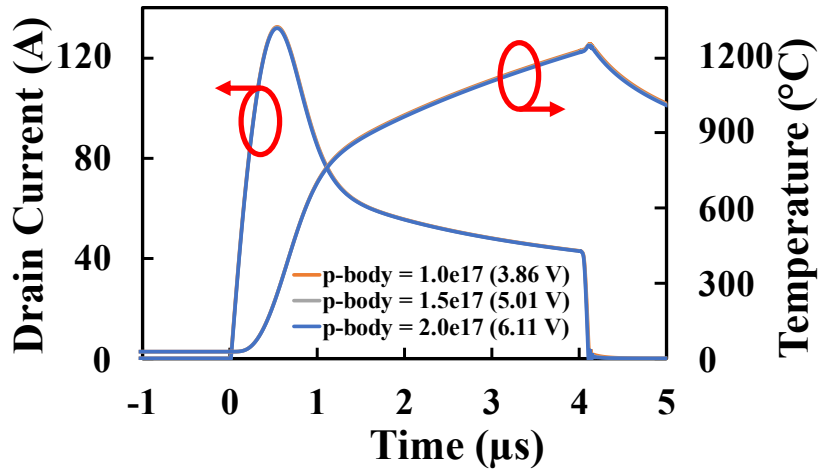
(b)

Figure 4.20 Short circuit TCAD Simulation of SiC MOSFET showing Impact of fixed oxide charges on (a) Short circuit current and hot-spot temperature (b) Drain-source voltage.

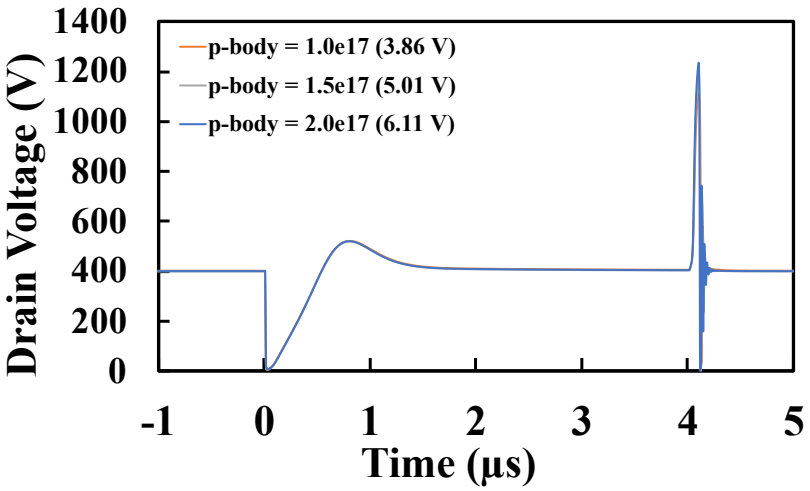
Finally, Figure 4.21 demonstrates the Impact of p-body doping on Short Circuit Transient. Like the simulated effects of fixed oxide charges on short circuit, the variation in V_{TH} using P-body doping shows almost no impact on the maximum short circuit current and temperature.

Table 4-6 P-body variation and impact on V_{TH}

Name	P-body doping (cm^{-3})	V_{TH} (V)
Device 1	$1.0x10^{17}$	3.86
Device 2	$1.5\ x10^{17}$	5.01
Device 3	$2.0x10^{17}$	6.11



(a)



(b)

Figure 4.21 Short circuit TCAD Simulation of SiC MOSFET showing Impact of p-body doping on (a) Short circuit current and hot-spot temperature (b) Drain-source voltage.

The effects of the various parameter variation on the maximum short circuit currents are summarised in Figure 4.22. It is evident that variations of CSL doping have the greatest effect on the maximum short circuit current even for small increases in V_{TH}. The Maximum short circuit current reduces from 132.11 A to 116.22.A, whereas the variations in fixed oxide charges and P-body doping result in much smaller short circuit changes, 132.52 A to 132.24 and 132.34 to 131.76 A respectively.

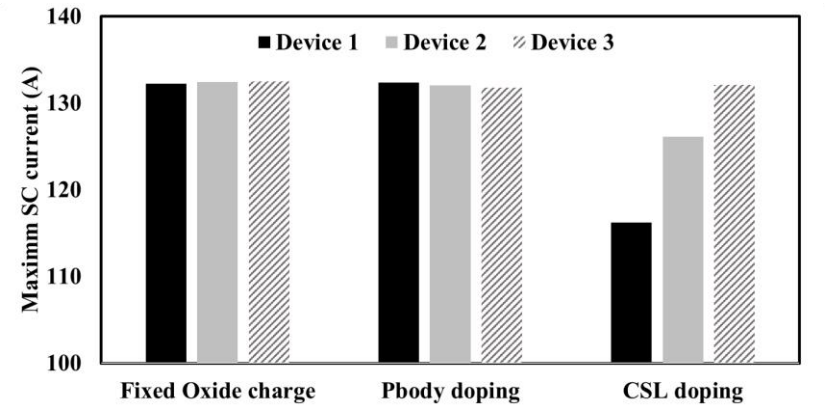
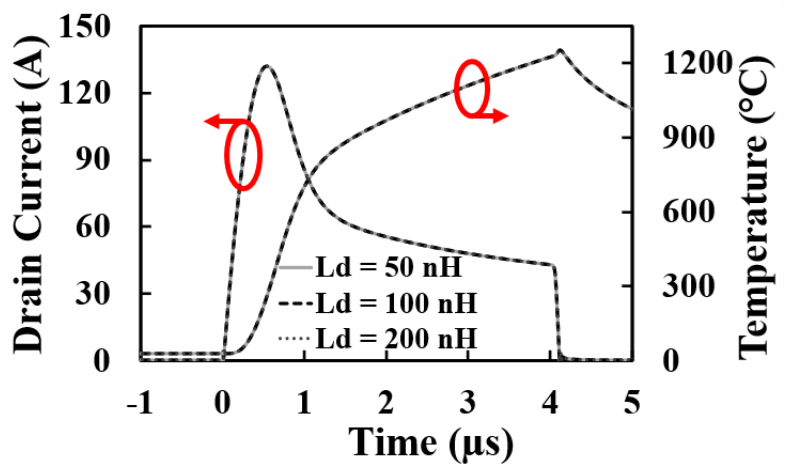


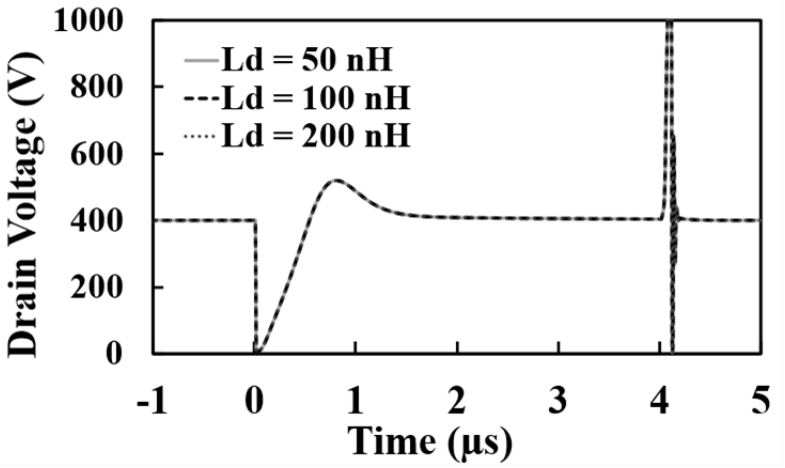
Figure 4.22 Effect of fabrication parameters on maximum short circuit current

Impact of Drain Inductance on Short Circuit Transient:

As the drain inductance increases, the peak short circuit current reduces since the drain inductance limits the short circuit dI/dt. Simulations have been performed on the impact of drain inductance on the short circuit transient. Figure 4.23(a) shows short circuit current, the difference is almost indistinguishable for an increase from 25 nH to 200 nH. Figure 4.23(b) shows the corresponding short circuit transient voltage and the undershoot and overshoot. This minute change can be attributed to the changes in parasitic inductance for similarly packaged devices which is in the order of nano Henries, and this value is much smaller than the values of circuit loop inductances.



(a)



(b)

Figure 4.23 Short circuit TCAD Simulation of SiC MOSFET showing Impact of parasitic drain inductance, L_D (a). Short circuit current and hot-spot temperature (b) Drain-source voltage

4.5. Simulations of Short Circuit in SiC Cascode JFETs

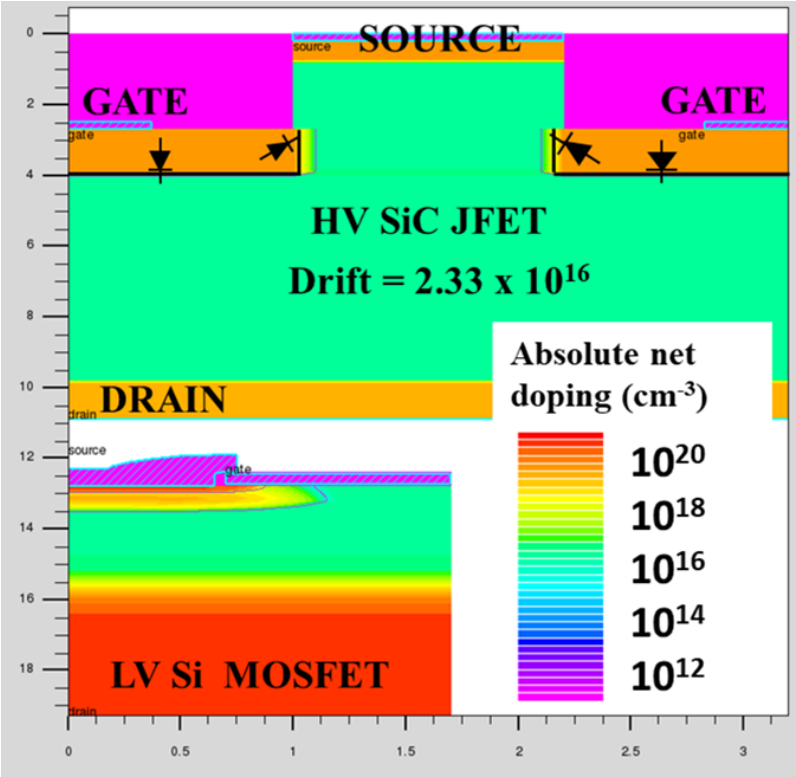


Figure 4.24 TCAD Structure of simulated SiC Cascode JFET and LV Si MOSFET

- Impact of Parameters on SiC Cascode JFETs Short Circuit Currents

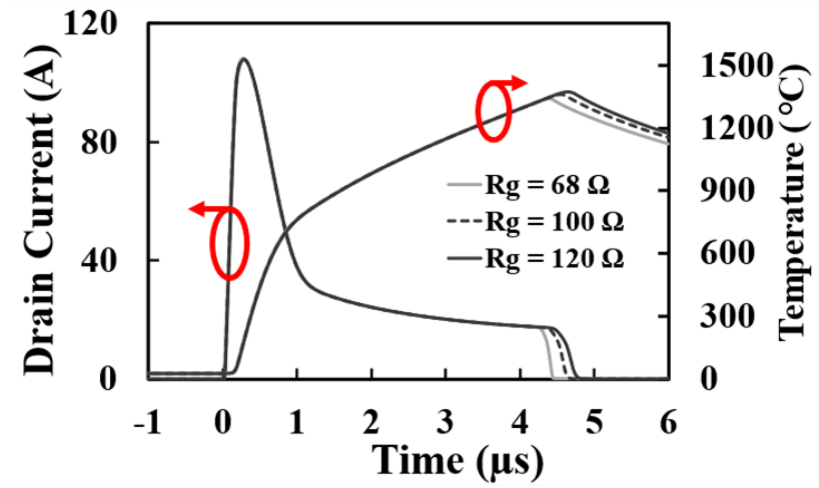
Short circuit in the SiC Cascode JFET was simulated in SILVACO using mixed-mode TCAD simulations with the structures (HV SiC JFET and LV silicon MOSFET) shown in Figure 4.24. Table 4-7. shows the structure parameters of the devices used in the simulations. The drift region of the simulated device is designed for a theoretical breakdown of 800 V which is usually the breakdown voltage for a 650 V rated device.

Table 4-7 Device simulation Parameters used for short circuit Simulations.

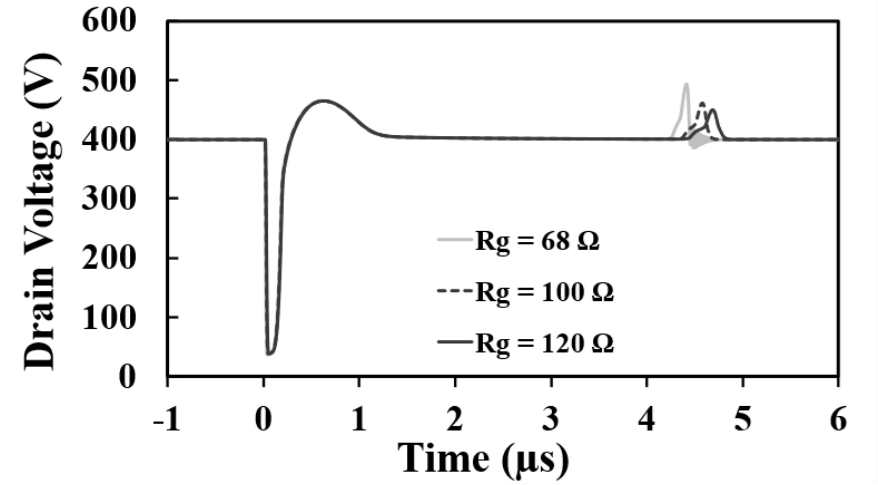
Parameter	HV JFET	LV MOSFET
Source doping (cm^{-3})	$1x10^{19}$	$4x10^{19}$
Channel Length (µm)	1.2	0.22
Drift layer thickness (µm)	6.0	3
Drift layer doping (cm^{-3})	$2.33x10^{16}$	$2.5x10^{16}$
Drain doping (cm^{-3})	$1x10^{19}$	$7.5x10^{19}$
Channel doping (cm^{-3})	$2.33x10^{16}$	$2x10^{17}$
JFET gate doping (cm^{-3})	$1x10^{19}$	-
Cell pitch (µm)	3.2	1.7
Area factor (µm)	$6x10^{5}$	$2x10^{6}$
Breakdown (V)	800	30

Impact of cascode R_G on short circuit transient.

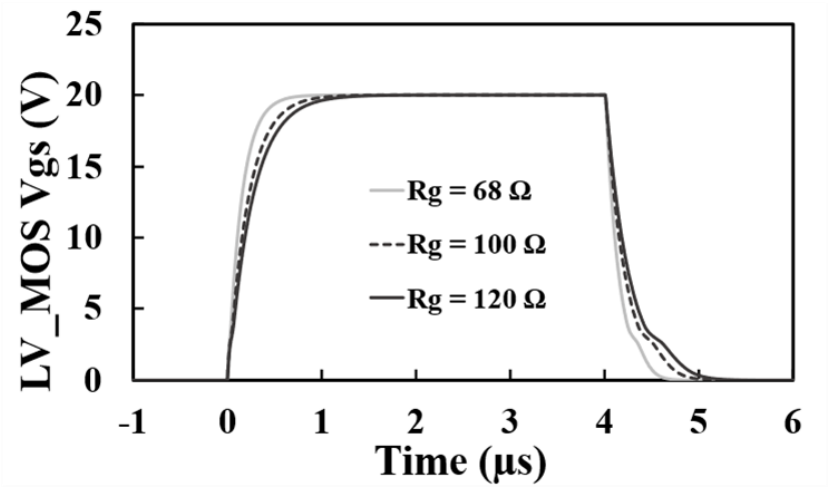
Figure 4.25 and Figure 4.26 presents the effects of varying the cascode external gate resistance (R_G) on the short circuit characteristics of the SiC Cascode JFET. Figure 4.25(a) shows the short circuit current and device temperature, while V_{DS} and V_{GS} are shown in Figure 4.25(b) and Figure 4.25(c) respectively. The maximum predicted short circuit currents for the three simulated cases are approximately the same while changing R_G (108.17 A for 68 Ω, 107.91 A for 100 Ω, and 107.73 A for 120 Ω). Also, the cascode experiences a delay at turn-off which increases with increase in R_G (approximately 250 ns for 100 Ω, and 350 ns for 120 Ω). This minute impact of R_G can be attributed to the selection of the LV MOSFET which is directly connected to the R_G. It is selected with a much larger saturation current than the JFET, hence it is only tasked with switching while the HV SiC JFET is responsible for regulating the short circuit current[41]. The temperature at turn-off also increases with this decrease in turn-off di/dt (increase R_G). The increase in temperature is 19.02 °C for 100 Ω, and 31.23 °C for 120 Ω. Figure 4.25(c) shows that there is a decrease in the dv/dt of the cascode V_{GS} as R_G increases, however this is after the plateau voltage which is after the turn-on of the JFET from double pulse simulations from previous chapters.



(a)



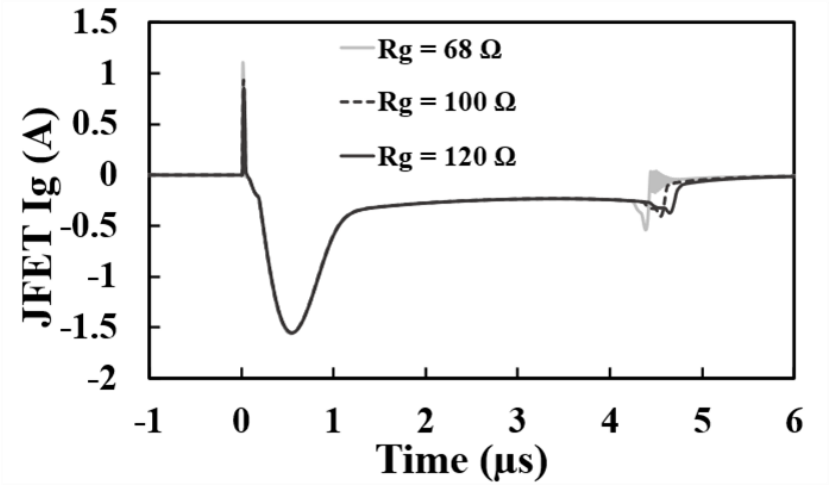
(b)



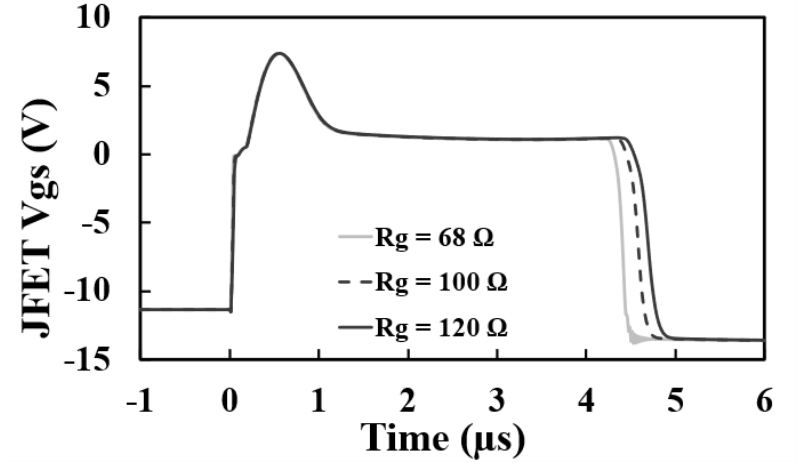
(c)

Figure 4.25 Short circuit TCAD Simulation of SiC Cascode JFET showing Impact of R_G on (a). Short circuit current and hot-spot temperature (b) Drain-source voltage (c) V_{GS} voltage

To fully examine the behaviour within the cascode configuration, additional plots of JFET gate current (I_{G-J}), and JFET gate voltage (V_{GS-J}) were extracted and presented in Figure 4.26(a) and Figure 4.26(b) respectively. From the plots, it is evident that the cascode R_G has almost no impact on the turn-on of the JFET, and only affects the turn-off. A high gate leakage current (1.5 A) is also observed for the JFET structure during short circuit operation. This could cause damage to the JFET gate loop path over time.



(a)

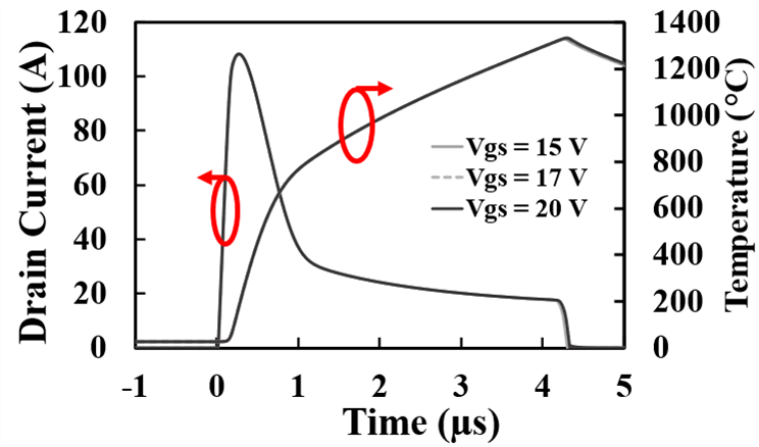


(b)

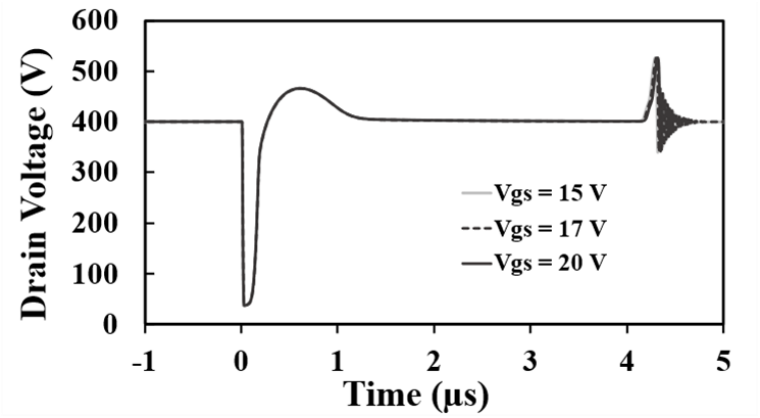
Figure 4.26 Short circuit TCAD simulation of SiC Cascode JFET showing impact of RG on (a) I_{G-J} (b) V_{GS-J}

Impact of Cascode gate voltage (V_{GS}) on short circuit transient.

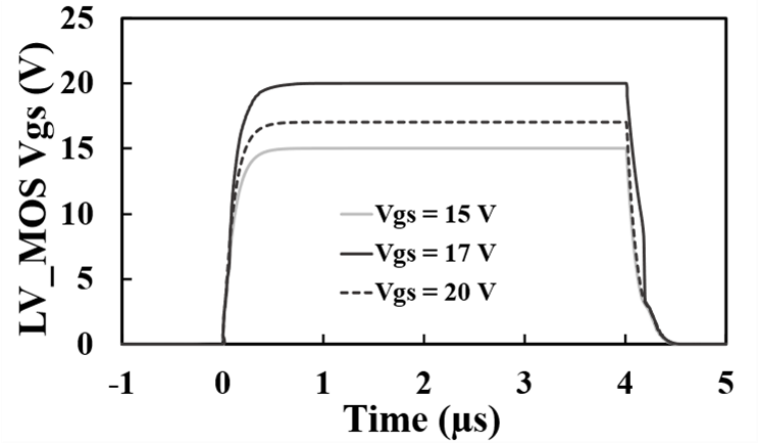
Figure 4.27 and Figure 4.28 show impact of the gate Voltage on the cascode JFET short circuit characteristics. Like the simulated impact of cascode R_G, the V_{GS} does not impact the short circuit current and on or temperature. All the simulated instances have identical plots with a maximum short circuit current of 108.30 A, and a maximum temperature of 1332.19 °C.



(a)

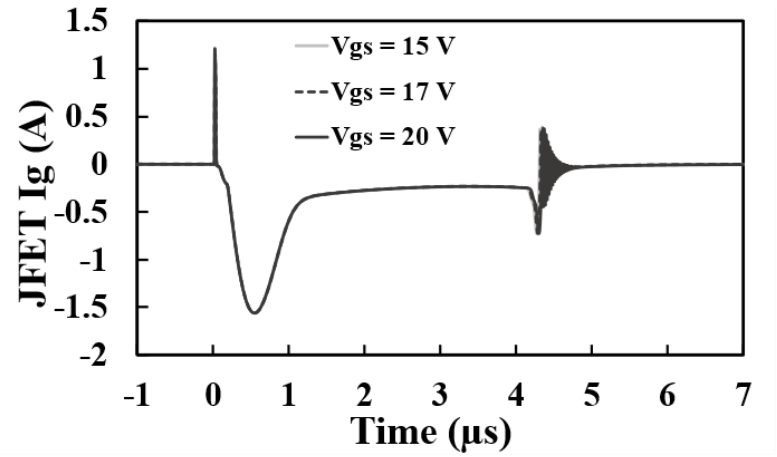


(b)

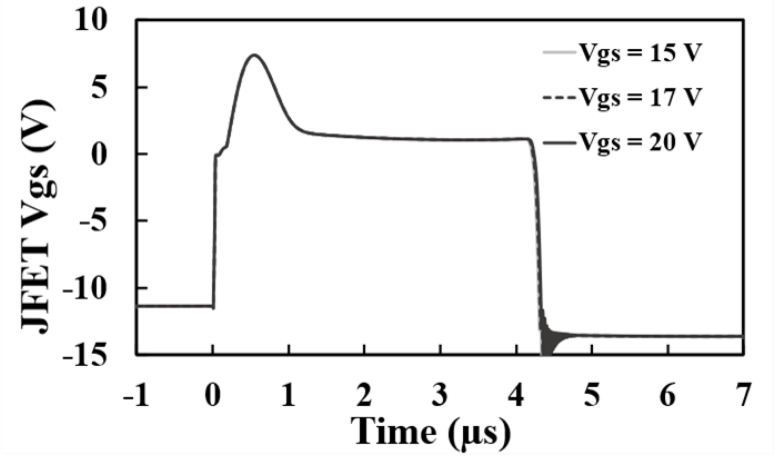


(c)

Figure 4.27 Short circuit TCAD Simulation of SiC Cascode JFET showing Impact of gate voltage on (a) Short circuit current and hot-spot temperature (b) Drain-source voltage (c) V_{GS}



(a)

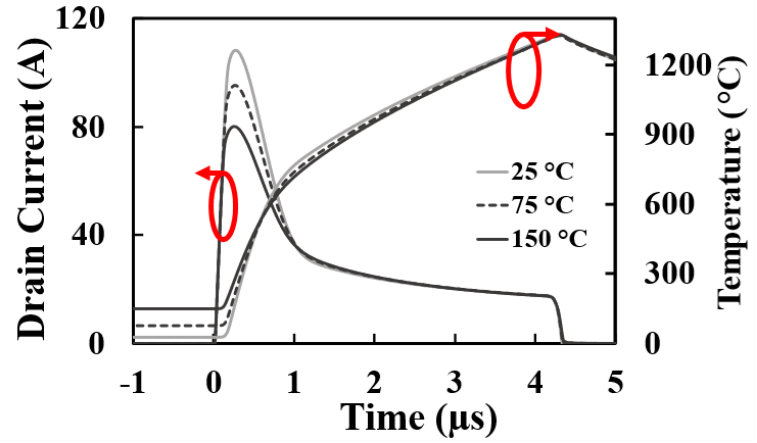


(b)

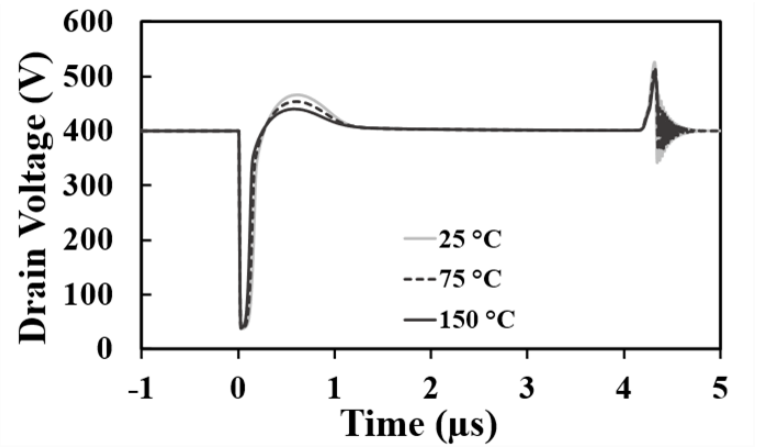
Figure 4.28 Short circuit TCAD Simulation of SiC Cascode JFET showing impact of gate voltage on (a) I_{G-J} (b) V_{GS-J}

Impact of case temperature on short circuit transient.

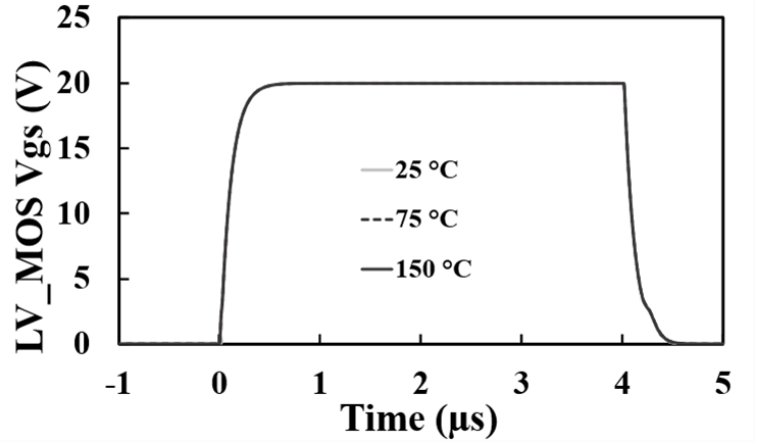
The impact of the case temperature on the cascode JEFT maximum short circuit current is simulated and presented in Figure 4.29 and Figure 4.30. From the simulation results of drain current in Figure 4.29(a), it is evident than an increase in the case temperature results in a reduction of the maximum current. However, the maximum Junction temperature experienced with the device is almost identical at 1330.5° C. This results from the inverse relationship between temperature and carrier mobility as already discussed in previous sections. Figure 4.29(b) shows a small decrease in the drain-source voltage of the cascode as case temperature is increased. However, the gate-source voltage of the cascode shown in Figure 4.29(c) remains unaffected by the change in temperature. This demonstrates that all the effects of the short circuit stress are on the HV SiC JFET, with the LV Si MOSFET unperturbed.



(a)



(b)

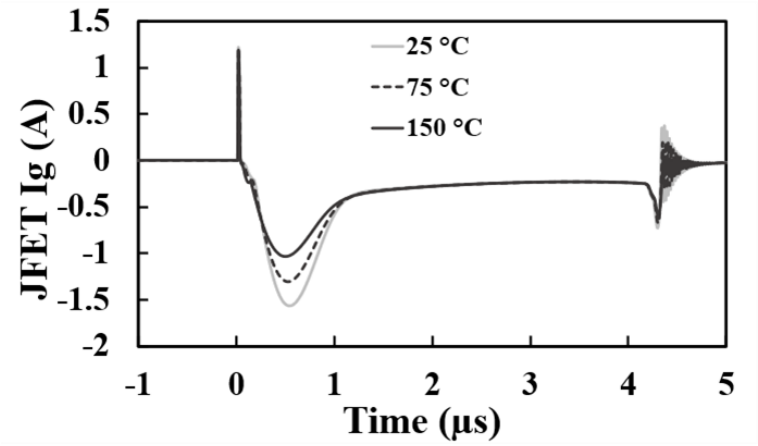


(c)

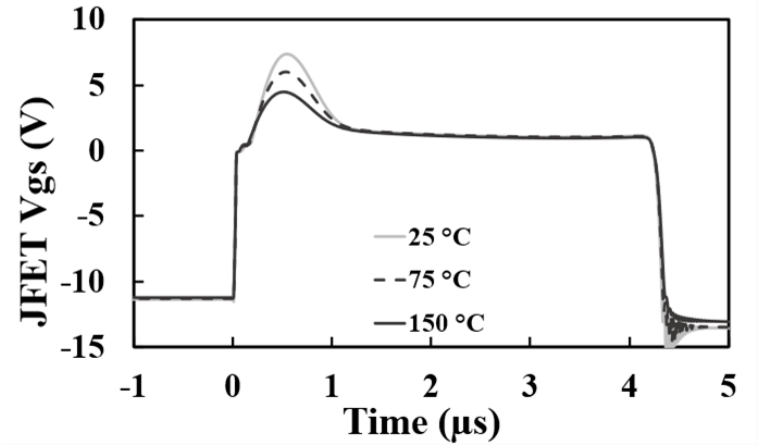
Figure 4.29 Short circuit TCAD Simulation of SiC Cascode JFET showing impact of of device temperature on (a) Short circuit current and hot-spot temperature (b) Drain-source voltage (c) V_{GS}

From Figure 4.30(a), it is worth noting that considerable variance in JFET gate current is demonstrated. The JFET gate voltage depicted in Figure 4.30(b) experiences a similar effect because of the voltage drop across the resistance in the gate loop path because of this current. The increase in case temperature caused a decrease in the absolute value of both.

Lesser current flows through the JFET gate path because reduced mobility causes an overall current density decrease. This is due to the inverse relationship between temperature and effective mobility around the channel and P-N junctions of the SiC JFET.



(a)



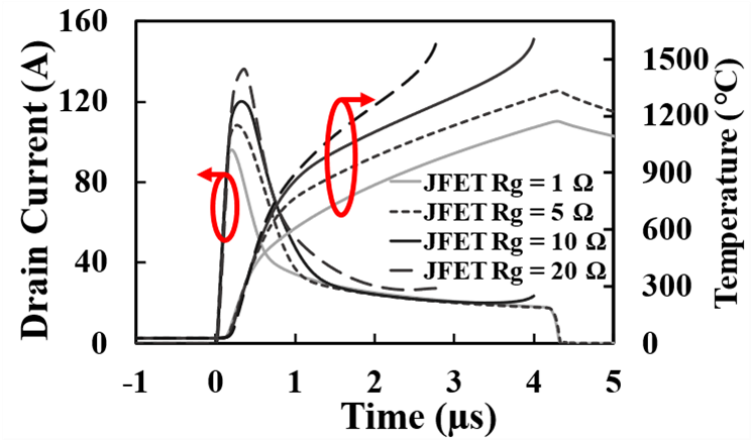
(b)

Figure 4.30 Short circuit TCAD Simulation of SiC Cascode JFET showing impact of device temperature on (a) I_{G-J} (b) V_{GS-J}

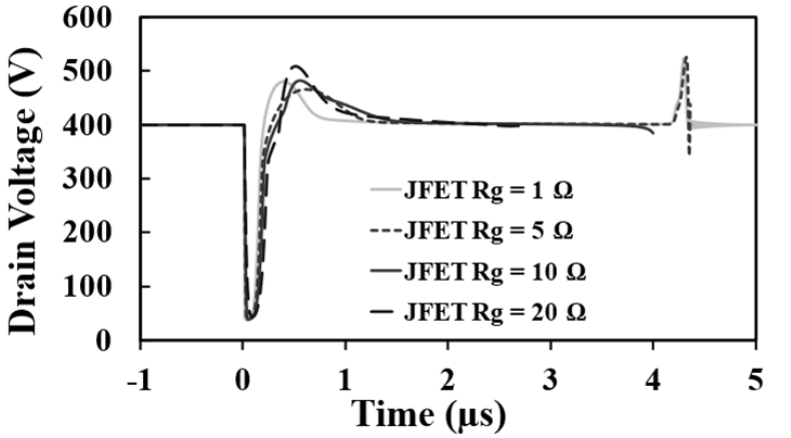
Impact of HV JFET gate resistance ($R_{G,JFET}$) on short circuit transient.

Figure 4.31 and Figure 4.32 demonstrate the characteristics of a SiC cascode JFET while the JFET R_G was varied. As previously mentioned, the JFET R_G is the JFET gate loop impedance located in the path between the gate of the HV JFET and the source of the LV MOSFET within the cascode configuration. Figure 4.31 (a) shows that the short circuit current is highly sensitive to this impedance. An increase in the JFET R_G leads to an increase in the maximum short current and junction temperature. Continued increase to this parameter increases the likelihood of thermal runaway and eventual failure. Figure 4.31(b) and Figure 4.31 (c) demonstrated a drain-source failure coupled with a gate-source failure within the cascode device for values of R_G greater than or equal to 10 Ω.

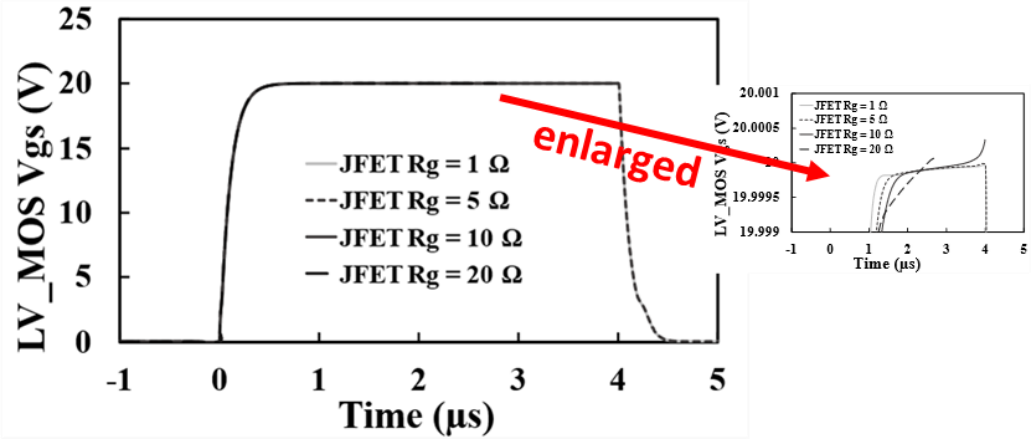
The JFET gate current and voltage are shown in Figure 4.32(a) and Figure 4.32(b) respectively. The gate current reduces with increasing R_G. However, with increased resistance the voltage-drop increases. The JFET gate eventually fails characterised by the second rise in the gate voltage. This is evident in the 10 Ω and 20 Ω waveforms of JFET gate voltage in Figure 4.32(b).



(a)

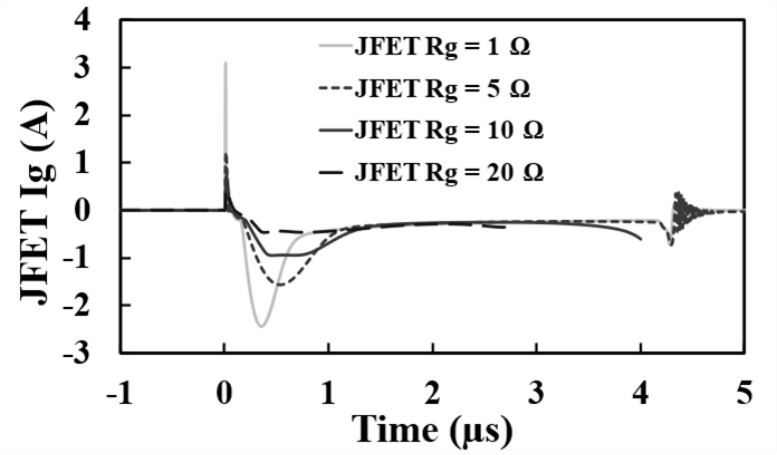


(b)

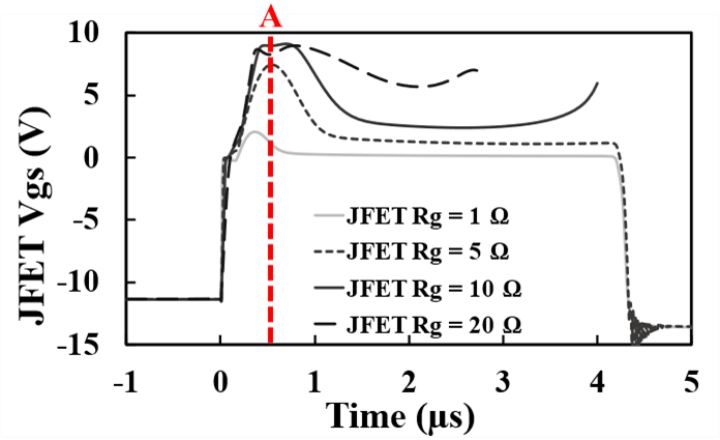


(c)

Figure 4.31 Short circuit TCAD Simulation of SiC Cascode JFET showing impact of JFET-R_G on (a) Short circuit current and hot-spot temperature (b) Drain-source voltage (c) V_{GS}



(a)

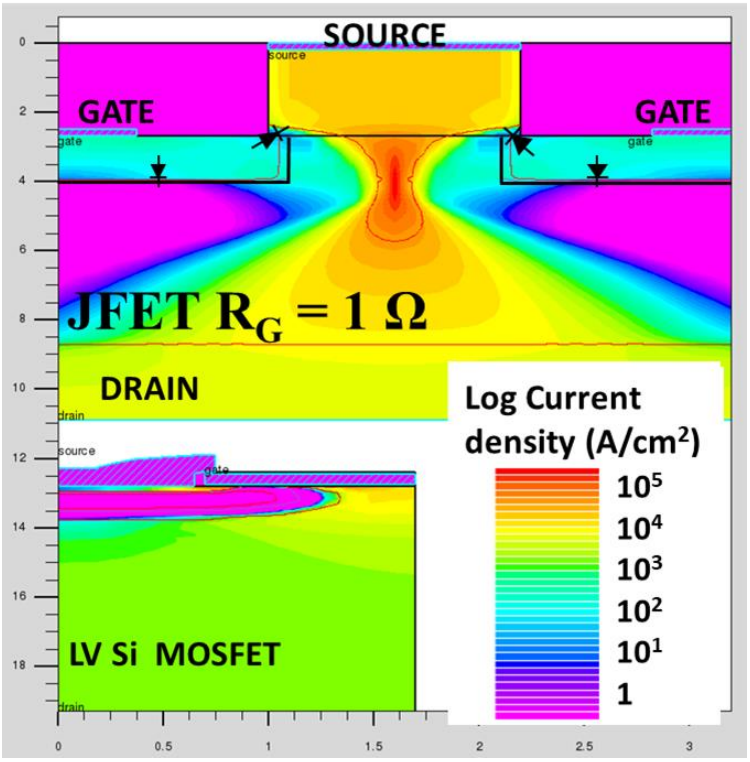


(b)

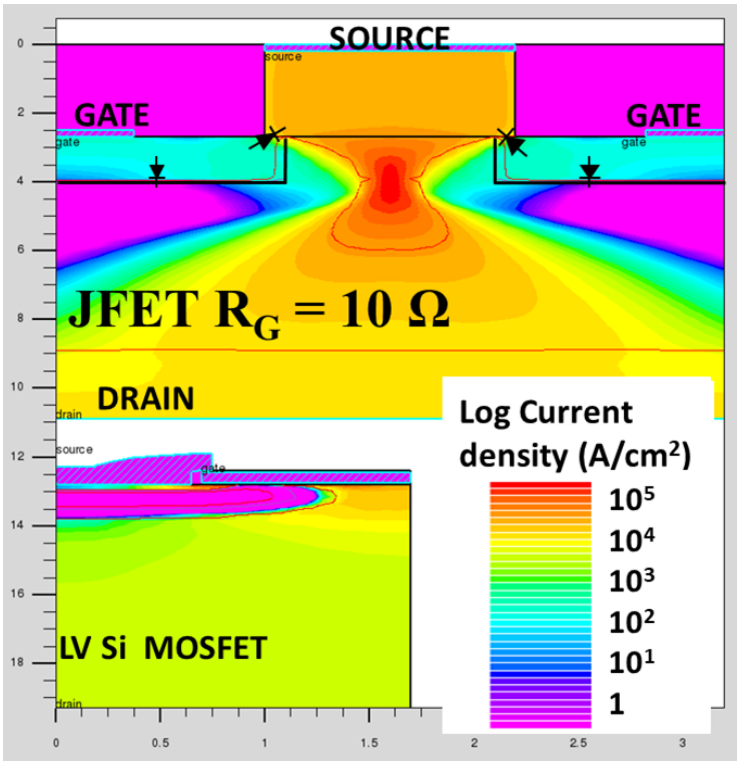
Figure 4.32 Short circuit TCAD Simulation of SiC Cascode JFET showing impact of JFET-R_G on (a) I_{G-J} (b) V_{GS-J}

Further analysis of cascode 2D contours of current density and junction temperature are presented in Figure 4.33 and Figure 4.34. The contours were all extracted at timestamp A depicted in Figure 4.33(b).The current density for 1 Ω and 10 Ω cases were presented in Figure 4.33(a) and Figure 4.33(b) respectively. These were picked to represent the cases of successful turn-off and failure because of increasing R_G. From the figures, it is evident that the 1 Ω JFET cell has a tighter channel and lower current density during short circuit. With the 10 Ω R_G, the channel is wider with the cell also experiences higher current density. This behaviour is a consequence of higher voltage drop across the JFET gate as shown in Figure 4.32(b).

Also, Figure 4.34 shows that the 10 Ω case reaches a higher junction temperature hence the reason for thermal runaway.

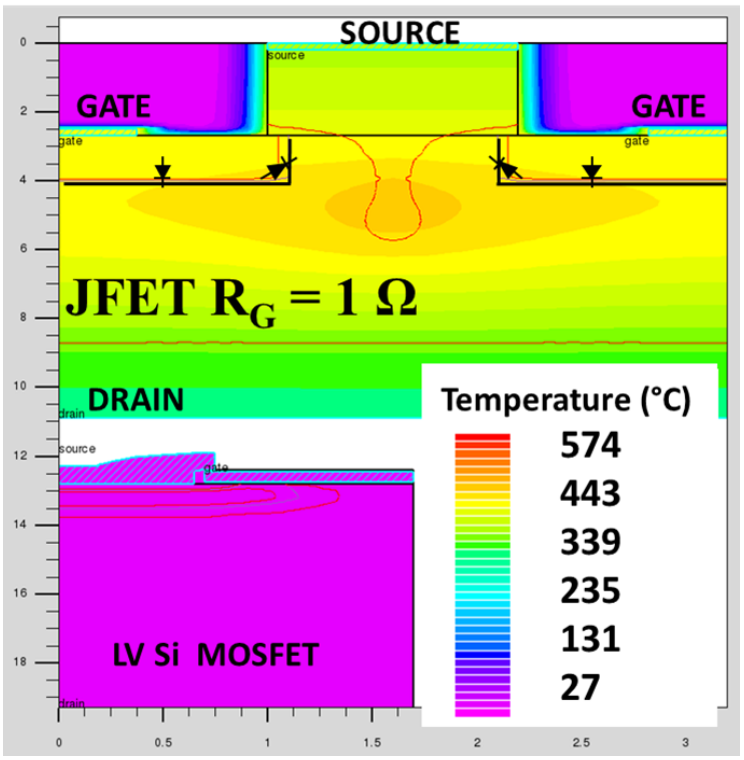


(a)

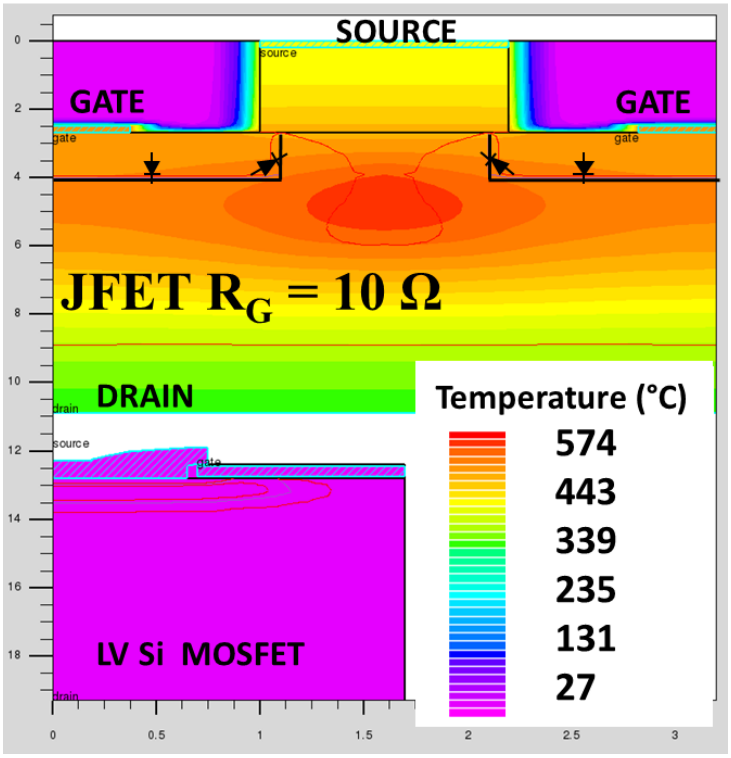


(b)

Figure 4.33 2D Current density contours of the SiC Cascode JFET with different JFET R_G (a) 1 Ω (b) 10 Ω



(a)

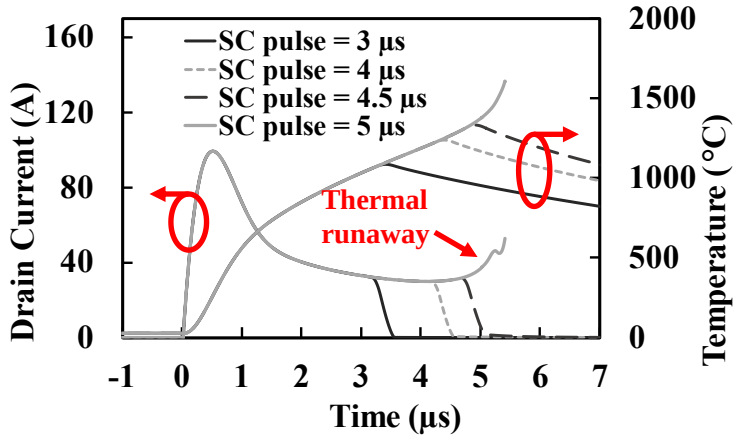


(b)

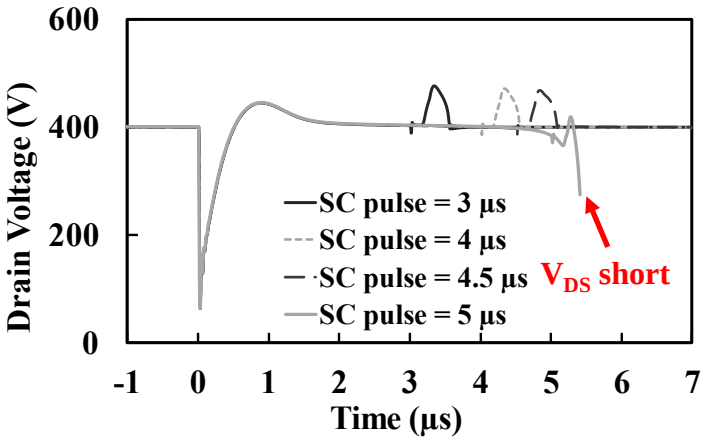
Figure 4.34 2D temperature contours of SiC Cascode JFET with different JFET R_G (a) 1 Ω (b) 10 Ω

- Cascode JFET failure during short circuit operation

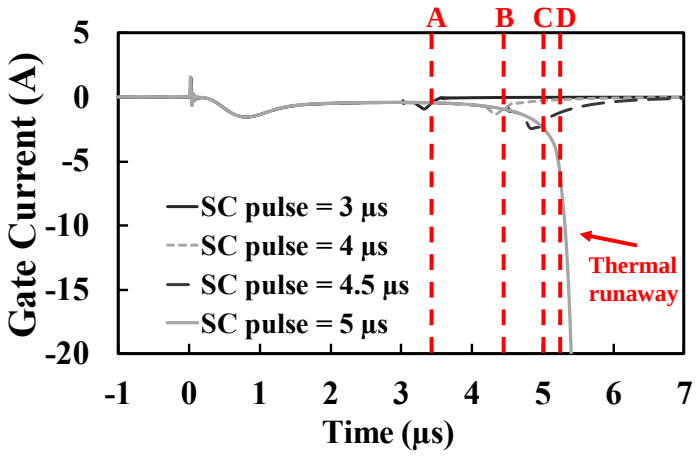
Figure 4.35(a) shows the simulated short circuit currents extracted from SILVACO for the SiC Cascode JFET. The hot-spot temperature of the device has also been extracted from the simulator and co-plotted with the short circuit current. Hot-spot temperatures of more than 1000°C can be observed in these simulations. These temperatures are approximately twice those predicted by the SPICE based compact circuit simulations in Figure 4.3(b). Figure 4.35(a) shows that thermal runaway occurs in the simulated device in a manner similar to the experimental measurements in Figure 4.7. Figure 4.35(b) shows the simulated drain-source voltage characteristics during the short circuit. In the V_{DS} characteristics, the experimental transients at turn-on and turn-off are replicated. As explained previously, the voltage drop at turn-on is due to the positive dI/dt across the drain inductance of the device at turn-on and the voltage rise at turn-off is due to the negative dI/dt across the drain inductance of the device at turn-off.



(a)



(b)



(c)

Figure 4.35. Short circuit TCAD Simulation for SiC cascode JFET with increasing pulse (a) Simulated short circuit current and hot-spot temperature (b) simulated V_{DS} characteristics (c) simulated JFET Gate Current characteristics.

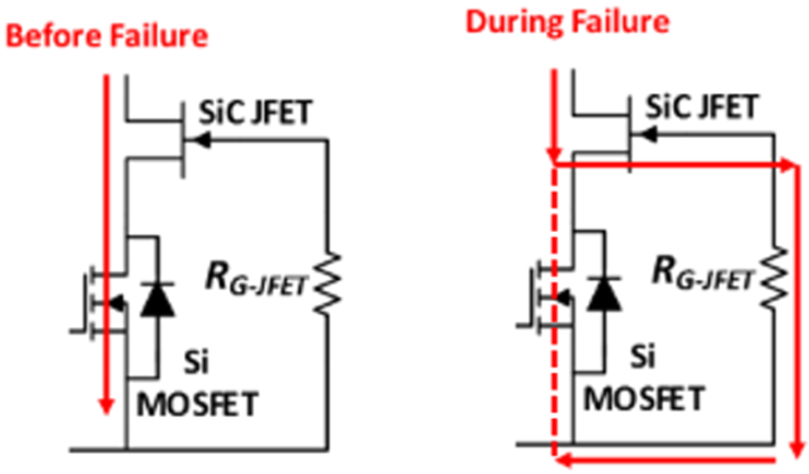


Figure 4.36 Schematic of SiC Cascode JFET before and after failure showing current flow paths.

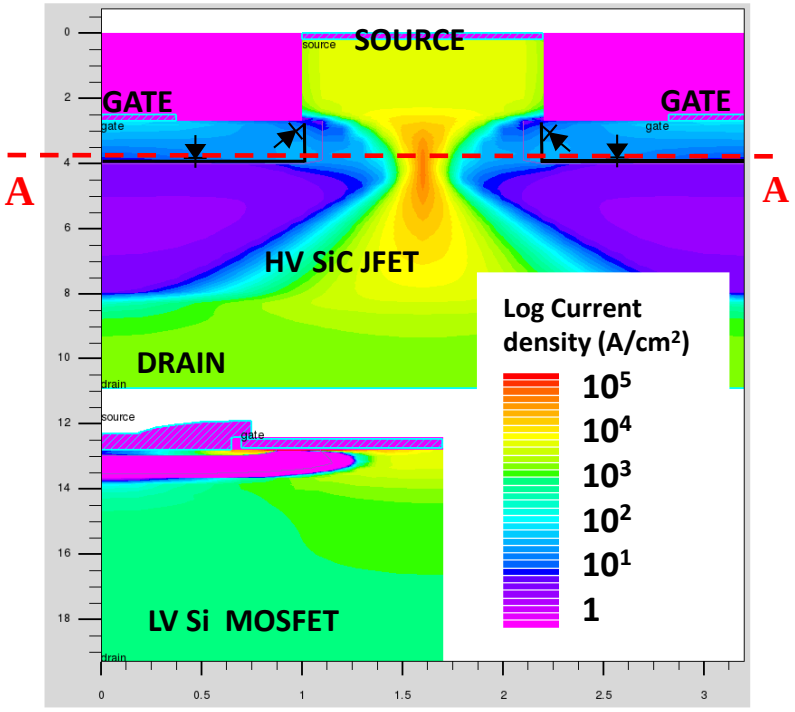
It was previously shown that the unlike the SiC Trench and Planar MOSFETs, the SiC Cascode JFET failed in a drain-to-source short circuit with the gate-to-source terminals still capable of blocking voltage. Hence, the gate oxide of the Cascode device was undamaged by the short circuit event, contrary to what is widely reported in literature for SiC MOSFETs [7, 8]. To understand the internal physics of failure of the SiC Cascode JFET, the gate current of the JFET is extracted from the simulation, as shown in Figure 4.35(c) for the different short circuit durations. This gate current should always be on the order of magnitude of micro-amperes since it is a leakage current of a reverse biased PN junction when the device is turned OFF. However, the point of failure (approximately point D in Figure 4.35(c)) shows a significant increase in the JFET gate leakage current, which occurs at the end of the LV silicon MOSFET turn-on duration. The leakage current observed here is the result of thermally generated

carriers in the device depletion regions thereby resulting in thermal runaway. This JFET gate leakage current causes a voltage-drop at the gate-source terminal of the JFET due to $R_{G\text{-}JFET}$. If the voltage drop across $R_{G\text{-}JFET}$ is large enough to turn the JFET ON, the device will operate in linear mode and since the silicon MOSFET is OFF and the channel is closed, the current will flow through the JFET gate thereby causing damage. Since the LV silicon MOSFET is OFF, it is not damaged by the excessive short circuit currents, hence, remains operational after the short circuit failure. Figure 4.36 shows the schematic of the Cascode JFET indicating the SHORT CIRCUIT current flow path before and during failure. Before failure, all the current flows through the LV Si MOSFET, but as the device is closer to failure, the JFET gate current increases. When the gate current increase is large enough to cause a voltage drop across $R_{G\text{-}JFET}$ capable of turning the JFET ON, the Cascode JFET undergoes thermal failure through the internal gate current path.

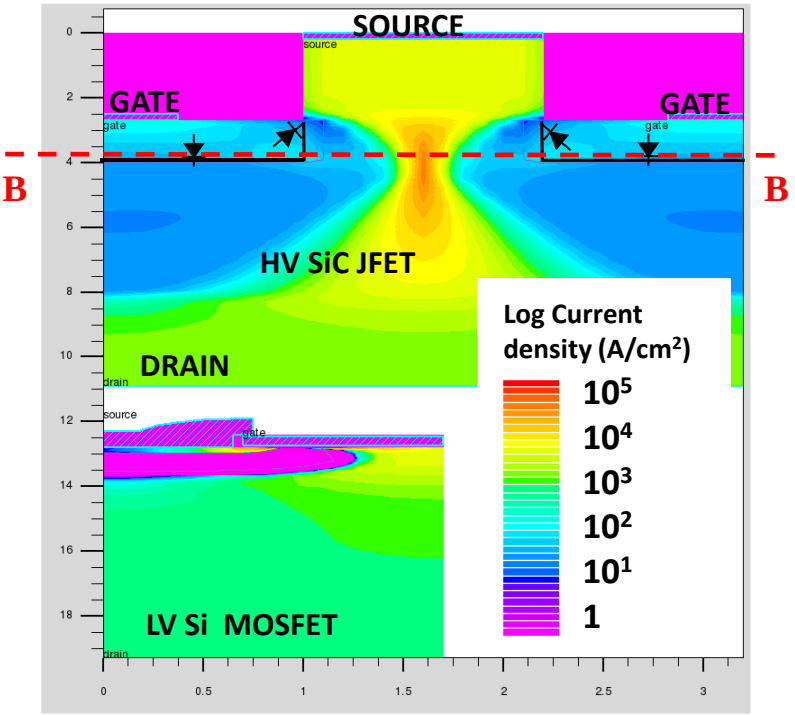
The 2D current density plots from the simulated Cascode JFET can be key for explaining this failure mechanism. The device 2D current density plots and 2D temperature plots have been extracted from the simulation for two different pulse durations. Case 1: pulse before failure (4.5 µs), and case 2: Failure pulse (5 µs). The 2D current density plots were extracted at time instants A (3.5 µs), B (4.5 µs), C (5 µs), and D (5.3 µs) indicated in the gate current characteristics shown in Figure 4.35(c).

Finite element simulation of short circuit in SiC Cascode JFET (successful case)

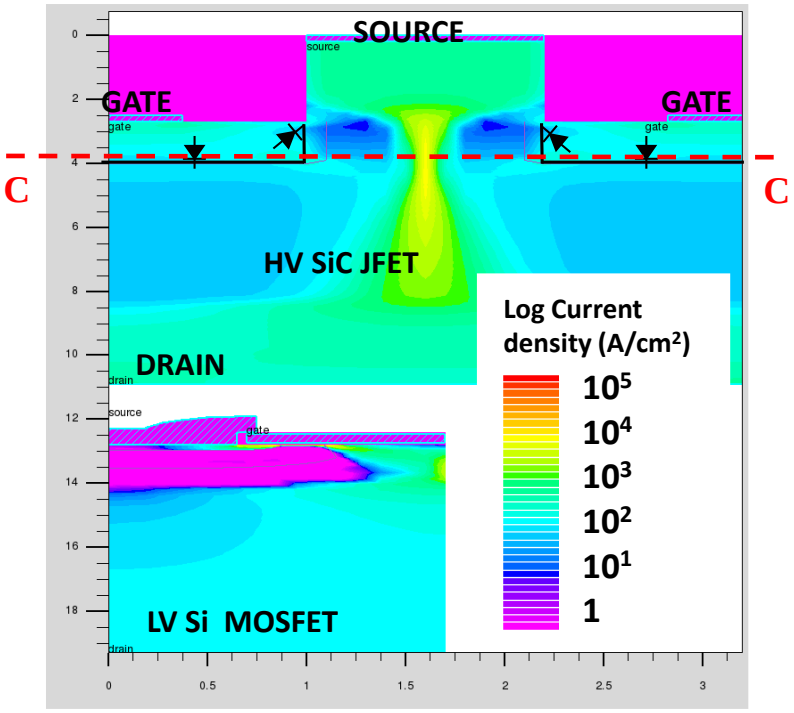
Figure 4.37(a) to (d) show the 2D current density contour plots corresponding to the short circuit pulse before failure case. Analysing the current contours in the figures show that the current density in the regions adjacent to the JFET gate does not increase substantially during the short-circuit pulse. As the LV MOSFET is switched OFF carrier generation in the JFET depletion region reduces indicating a successful suppression the SHORT CIRCUIT current. The leakage current through the JFET gate can be seen in all four current density plots and its peak value occurs at time instant C (Figure 4.37(c)) and a reduction is observed at time instant D, Figure 4.37(d) the current through the gate reduces


SOURCE
source
GATE
gate
GATE
gate
A
A
HV SiC JFET
DRAIN
drain
source
gate
LV Si MOSFET
drain
Log Current density (A/cm²)
10⁵
10⁴
10³
10²
10¹
1
0
2
4
6
8
10
12
14
16
18
0
0.5
1
1.5
2
2.5
3

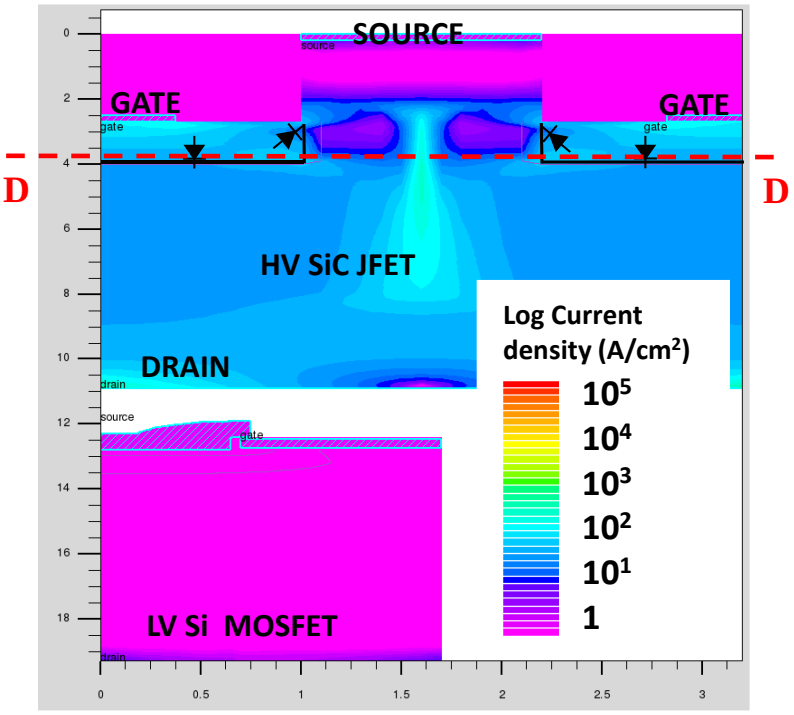
(a)


SOURCE
source
GATE
gate
GATE
gate
B
B
HV SiC JFET
DRAIN
drain
source
gate
LV Si MOSFET
drain
Log Current density (A/cm²)
10⁵
10⁴
10³
10²
10¹
1
0
2
4
6
8
10
12
14
16
18
0
0.5
1
1.5
2
2.5
3

(b)



(c)



(d)

Figure 4.37 2D Current density contour plots for the SiC Cascode JFET (normal operation mode) at (a) time point A (b) time point B (c) time point C (d) time point D

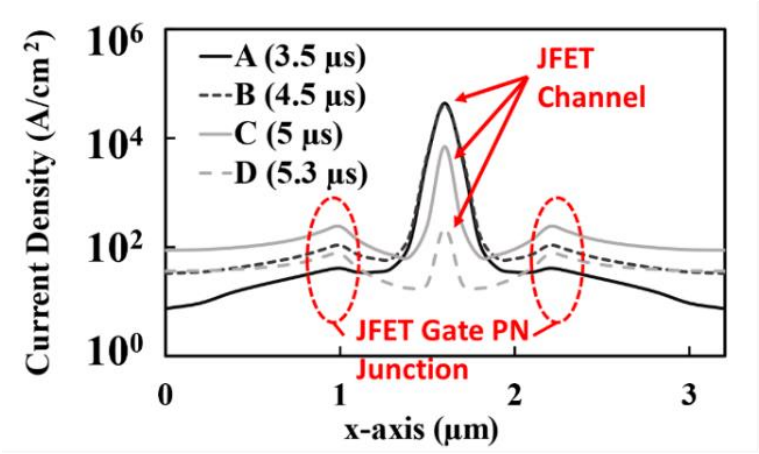


Figure 4.38 Carrier density across cutline of the JFET showing low current density in the gate terminals (normal operation mode)

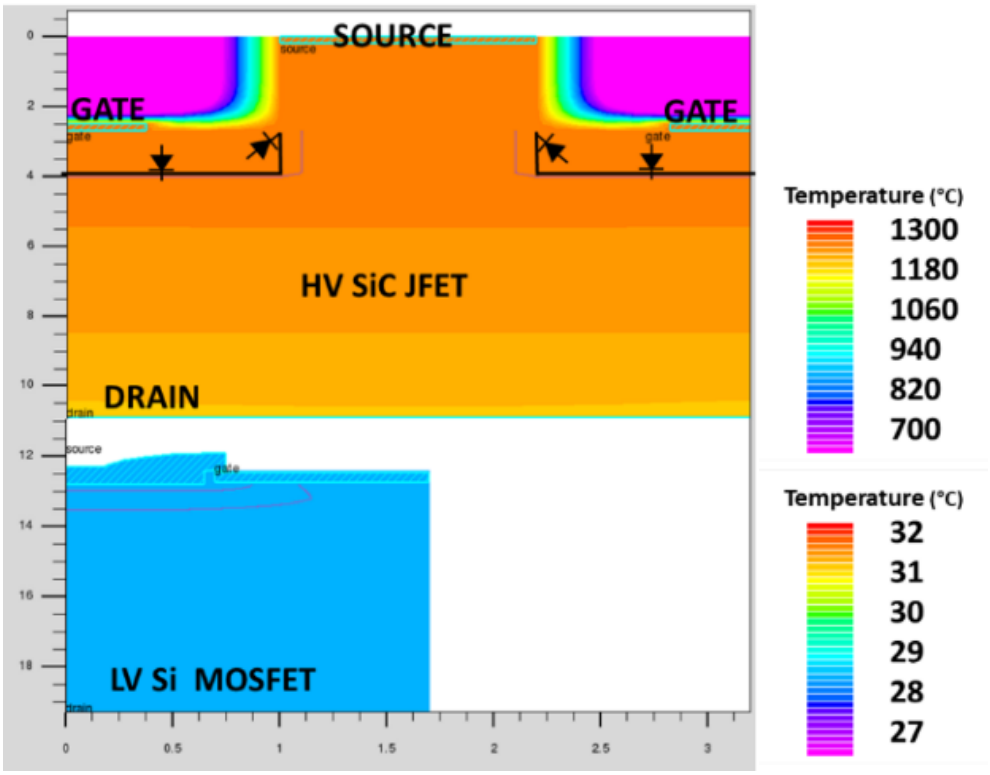


Figure 4.39. 2D temperature contour plots extracted from the simulator at time instant D.

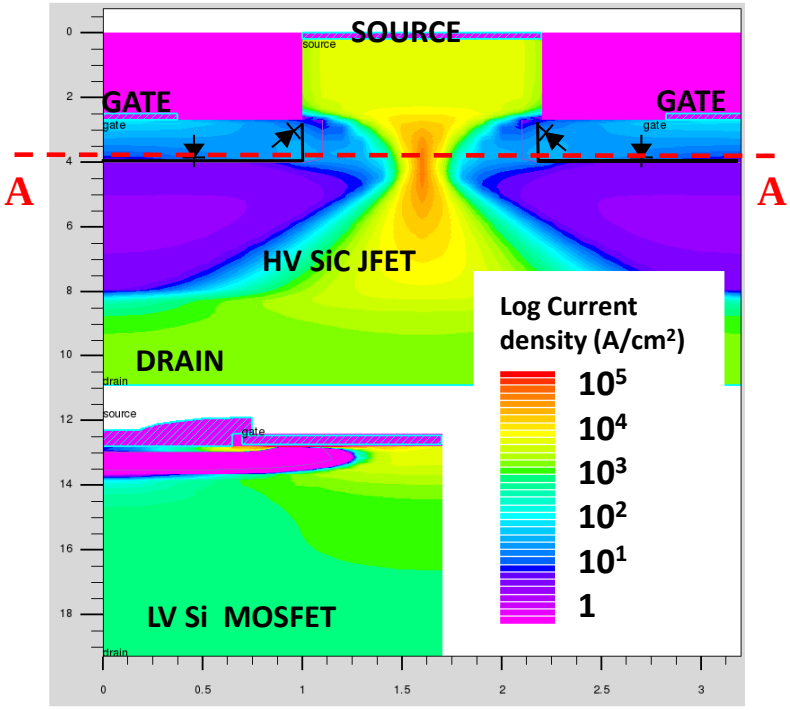
Figure 4.38 shows the extracted carrier density along the cross-sectional cutline from Figure 4.37. The extracted cross-sectional cutline is done horizontally along the JFET gate, providing a clearer assessment the JFET gate leakage current. As expected, the current density in the channel of the JFET is higher than that in the gate-source terminals of the JFET. This shows the JFET functioning normally. Figure 4.39 shows the simulated temperature in the JFET and the LV Si MOSFET at time instant D (5.3 µs) from Figure 4.35(c). The MOSFET is approximately at 29 °C indicating a slight increase from the starting temperature of 27 °C while the JFET hotspot has not reached the critical failure temperature. This shows that all the SHORT

CIRCUIT energy dissipated by the SiC Cascode JFET is dissipated by the HV JFET without any stress on the LV MOSFET, confirming results previously reported [3].

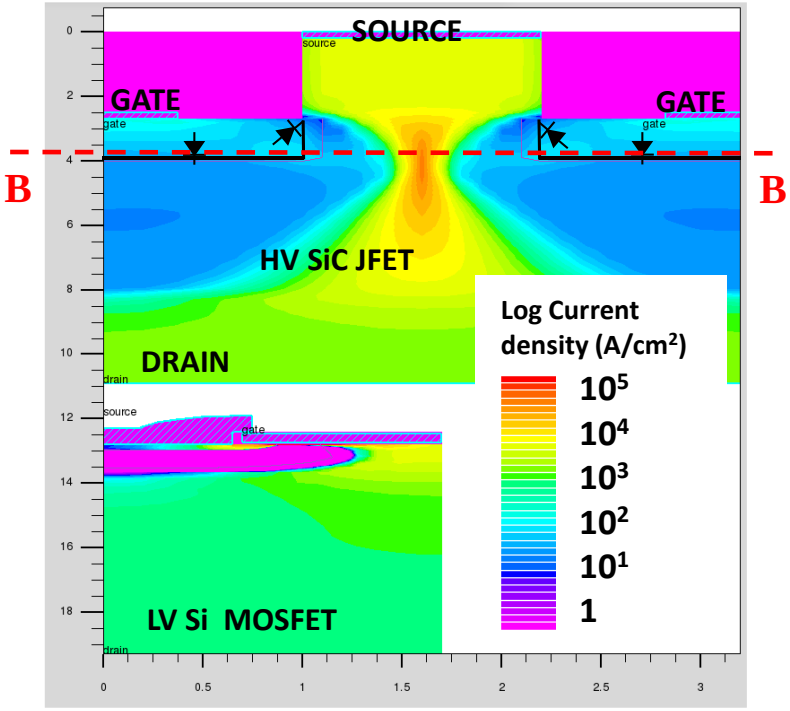
Finite element simulation of short circuit in SiC cascode JFET (failure case)

The 2D current density contour plots of the device subjected to the short circuit failure pulse case are shown in Figure 4.40(a) to (d). Compared with the no failure case, Figure 4.40(c) and Figure 4.40(d) show an increase in thermally generated carriers in the JFET depletion region. This causes a failure in the JFET gate PN junction leading to currents of magnitude greater than 20 A to flow out of the JFET gate, as can be seen in Figure 4.35(c). Current of this magnitude is enough to induce a voltage on R_{GJFET} greater than the magnitude of the JFET pinch-off, thereby turning ON the JFET channel and causing the JFET to operate in linear mode. In this mode, the short circuit current flows from the JFET drain into the gate terminal since the LV MOSFET is Operating in avalanche as shown in Figure 4.40(d). Figure 4.41 compares the extracted current density along the cross-sectional cutline of the JFET at the time instant D (5.3 µs), for the two evaluated cases, i.e. (i) device failing with 5 µs pulse and (ii) device successfully turning OFF with 4.5 µs pulse. The highest current density, as expected is in the JFET channel and a considerable increase of the JFET gate leakage current is observed in the case of the failed device.

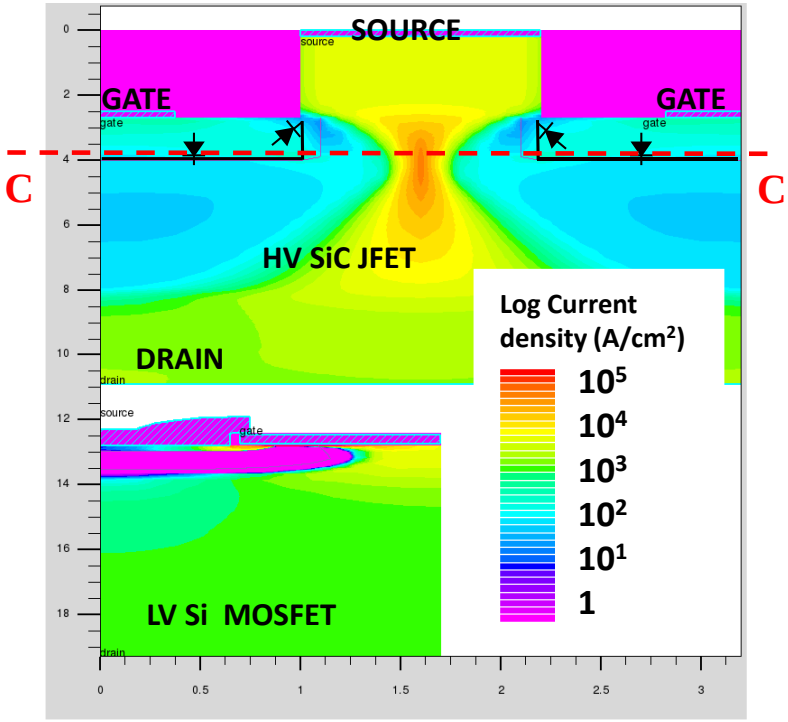
Figure 4.42 shows the simulated temperature in the JFET and the LV Si MOSFET at time instant D (5.3 µs) for the failed case. In this case, the MOSFET hotspot temperature only experiences a negligible increase (27 °C to 31 °C), whereas the JFET has exceeded the failure temperature for SiC and undergoes thermal failure.


SOURCE
source
GATE
gate
GATE
gate
A
A
HV SiC JFET
Log Current
density (A/cm²)
DRAIN
drain
source
gate
10⁵
10⁴
10³
10²
10¹
1
LV Si MOSFET
drain
0
2
4
6
8
10
12
14
16
18
0
0.5
1
1.5
2
2.5
3

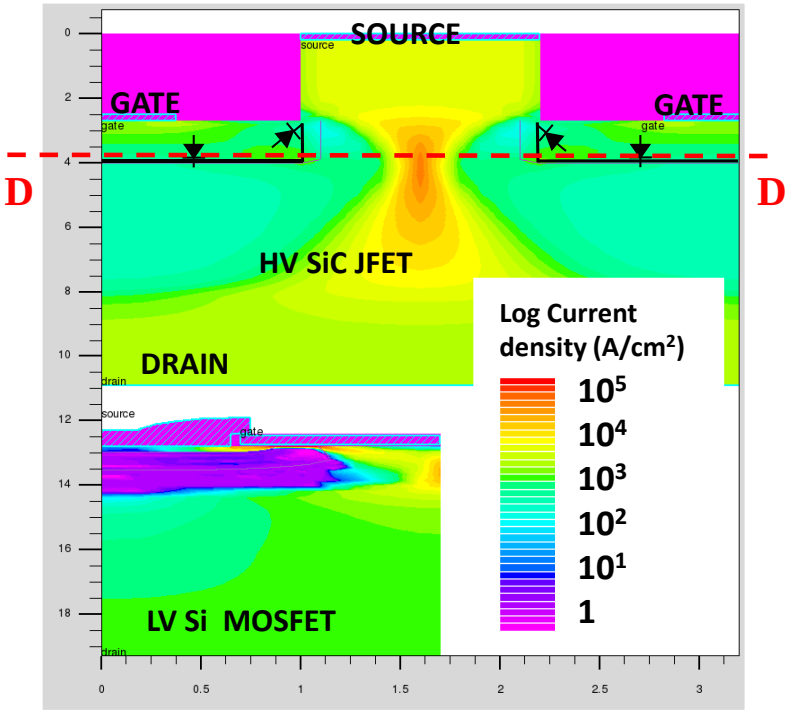
(a)


SOURCE
source
GATE
gate
GATE
gate
B
B
HV SiC JFET
Log Current
density (A/cm²)
DRAIN
drain
source
gate
10⁵
10⁴
10³
10²
10¹
1
LV Si MOSFET
drain
0
2
4
6
8
10
12
14
16
18
0
0.5
1
1.5
2
2.5
3

(b)



(c)



(d)

Figure 4.40. 2D Current density contour plots for the SiC Cascode JFET (Failure pulse) at (a) time point A (b) time point B (c) time point C (d) time point D

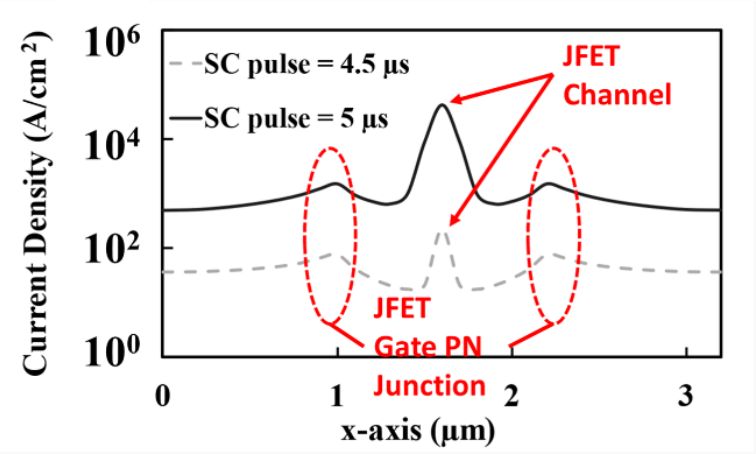


Figure 4.41 Comparison of simulated current density across JFET gate before and after short circuit failure

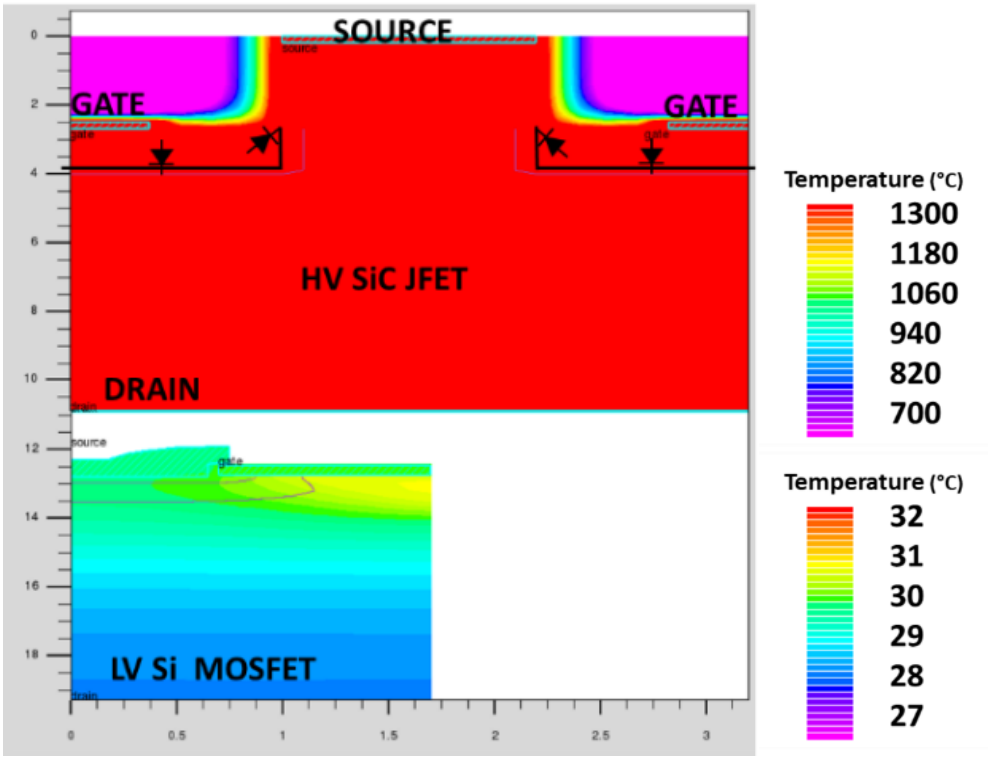


Figure 4.42 Simulated 2D lattice temperature for SiC Cascode JFET under Short circuit failure.

4.6. Conclusion

Ruggedness under short circuit stress is an important metric in power devices since malfunctions leading to short circuits can occur in power electronic systems. Under short circuit conditions, the device is subjected to the highest possible instantaneous power which results in uncontrolled junction temperature excursions. In this chapter, the short circuit performance of SiC Cascode JFETs have been benchmarked against comparatively rated device technologies including SiC Planar MOSFETs, SiC Trench MOSFETs, silicon super-

junction MOSFETs, silicon MOSFETs and silicon field-stop IGBTs. All the devices are rated at 650 V with current ratings between 30 A and 40 A. The experimental short circuit withstand time was measured by increasing the short circuit pulse until device failure. This was done for 4 devices to ensure statistical integrity of the data. The SiC Cascode JFET ranked lowest in terms of short circuit withstand time jointly with the SiC planar device. Unlike the SiC Trench and Planar MOSFET, the Cascode JFET failed with a shorted drain-source connection with the gate-source connection still intact (capable of blocking voltage). Measurements and simulations showed that the peak short circuit current decreased with decreasing gate-source voltage, increasing temperature, increasing threshold voltage, increasing drain inductance and was invariant of the gate resistance.

Compact model circuit simulators like SPICE assume uniform temperature distribution since junction temperatures are predicted using thermal networks based on lumped thermal resistances and capacitances. Hence, Finite Element Simulations are required to extract the hot-spot temperature of the device under short circuit conditions. Finite element simulations were used to investigate the internal physics of device failure in the SiC Cascode JFET. The simulations showed that excessive carrier generation in the JFET depletion region during turn-off causes large currents to flow from the gate of the HV SiC JFET to the source of the LV silicon MOSFET. This large current flows through the internal gate resistance of the Cascode structure and therefore causes a voltage drop larger than the JFET pinch OFF voltage. This causes the JFET to turn-on into linear mode and damages the internal gate resistance which is not rated to dissipate the power generated within it. Hence, the LV silicon MOSFET remains undamaged since it is OFF and the short circuit current flows through the JFET gate-drain capacitance. This failure mode is unlike SiC Planar and Trench MOSFETs which fail through gate rupture due to thermally energetic carriers tunnelling across the gate oxide. The SiC Cascode JFET does not suffer from poor gate oxide quality since the input of the device is a silicon MOSFET with excellent gate oxide characteristics unlike SiC MOSFETs with poorer gate oxide properties.

From the experimental measurements, the short circuit withstand time of the JFET is shown to be independent of the initial device temperature. This is unlike all other device technologies which have some dependence between the SCWT and initial junction temperature. Similar measurements performed on similarly rated silicon MOSFETs showed that the SCWT increases with temperature while in SiC Trench MOSFETs that SCWT reduces with initial junction temperature. This indicates that the failure mode in SiC Cascode JFETs is independent of initial device temperature.

References

[1] H. Kono *et al.*, "Improving the specific on-resistance and short-circuit ruggedness tradeoff of 1.2-kV-class SBD-embedded SiC MOSFETs through cell pitch reduction and internal resistance optimization," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 30 May-3 June 2021 2021, pp. 227-230, doi: 10.23919/ISPSD50666.2021.9452314.

[2] A. Agarwal, A. Kanale, K. Han, B. J. Baliga, and S. Bhattacharya, "Impact of Gate Oxide Thickness on Switching and Short Circuit Performance of 1200 V 4H-SiC Inversion-channel MOSFETs," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 29-31 Oct. 2019 2019, pp. 59-62, doi: 10.1109/WiPDA46397.2019.8998839.

[3] A. Agarwal, A. Kanale, K. Han, and B. J. Baliga, "Switching and Short-Circuit Performance of 27 nm Gate Oxide, 650 V SiC Planar-Gate MOSFETs with 10 to 15 V Gate Drive Voltage," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 13-18 Sept. 2020 2020, pp. 250-253, doi: 10.1109/ISPSD46842.2020.9170151.

[4] B. Kakarla, T. Ziemann, R. Stark, P. Natzke, and U. Grossner, "Short Circuit Ruggedness of New Generation 1.2 kV SiC MOSFETs," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 31 Oct.-2 Nov. 2018 2018, pp. 118-124, doi: 10.1109/WiPDA.2018.8569077.

[5] J. An, M. Namai, H. Yano, N. Iwamuro, Y. Kobayashi, and S. Harada, "Methodology for enhanced short-circuit capability of SiC MOSFETs," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 13-17 May 2018 2018, pp. 391-394, doi: 10.1109/ISPSD.2018.8393685.

[6] J. Sun, H. Xu, X. Wu, S. Yang, Q. Guo, and K. Sheng, "Short circuit capability and high temperature channel mobility of SiC MOSFETs," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 28 May-1 June 2017 2017, pp. 399-402, doi: 10.23919/ISPSD.2017.7988988.

[7] J. Liu, G. Zhang, B. Wang, W. Li, and J. Wang, "Gate Failure Physics of SiC MOSFETs Under Short-Circuit Stress," *IEEE Electron Device Letters,* vol. 41, no. 1, pp. 103-106, 2020, doi: 10.1109/LED.2019.2953235.

[8] P. D. Reigosa, F. Iannuzzo, and L. Ceccarelli, "Effect of short-circuit stress on the degradation of the SiO2 dielectric in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 577-583, 2018/09/01/ 2018, doi: https://doi.org/10.1016/j.microrel.2018.07.144.

[9] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability,* vol. 80, pp. 68-78, 2018/01/01/ 2018, doi: https://doi.org/10.1016/j.microrel.2017.11.020.

[10] J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC mosfets," *IEEE Transactions on Power Electronics,* vol. 34, no. 6, pp. 5737-5747, 2019, doi: 10.1109/TPEL.2018.2870067.

[11] D. Peters, T. Aichinger, T. Basler, G. Rescher, K. Puschkarsky, and H. Reisinger, "Investigation of threshold voltage stability of SiC MOSFETs," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 13-17 May 2018 2018, pp. 40-43, doi: 10.1109/ISPSD.2018.8393597.

[12] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability," *IEEE Transactions on Electron Devices,* vol. 66, no. 11, pp. 4604-4616, 2019, doi: 10.1109/TED.2019.2938262.

[13] S. Sundaresan, V. Mulpuri, J. Park, and R. Singh, "Reliability and Robustness Performance of 1200 V SiC DMOSFETs," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 28 April-30 May 2020 2020, pp. 1-4, doi: 10.1109/IRPS45951.2020.9128225.

[14] E. Mengotti, E. Bianda, D. Baumann, E. K. Papamichalis, A. Mihaila, and S. Wirths, "Temperature Dependent Transient Threshold Voltage Hysteresis in SiC Power MOSFETs and Implications for Short Circuit Events," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 30 May-3 June 2021 2021, pp. 259-262, doi: 10.23919/ISPSD50666.2021.9452290.

[15] X. Zhou, H. Su, Y. Wang, R. Yue, G. Dai, and J. Li, "Investigations on the Degradation of 1.2-kV 4H-SiC MOSFETs Under Repetitive Short-Circuit Tests," *IEEE Transactions on Electron Devices,* vol. 63, no. 11, pp. 4346-4351, 2016-11-01 2016, doi: 10.1109/ted.2016.2606882.

[16] Y. Li *et al.*, "Gate Bias Dependence of V _{TH} Degradation in Planar and Trench SiC MOSFETs Under Repetitive Short Circuit Tests," *IEEE Transactions on Electron Devices,* vol. 69, no. 5, pp. 2521-2527, 2022-05-01 2022, doi: 10.1109/ted.2022.3142237.

[17] S. Yu *et al.*, "Bias-Induced Threshold Voltage Instability and Interface Trap Density Extraction of 4H-SiC MOSFETs," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019-10-01 2019: IEEE, doi: 10.1109/wipda46397.2019.8998931.

[18] R. Green, D. P. Urciuoli, and A. J. Lelis, "Short-circuit robustness testing of SiC MOSFETs," in *2016 European Conference on Silicon Carbide & Related Materials (ECSCRM)*, 25-29 Sept. 2016 2016, pp. 1-1, doi: 10.4028/www.scientific.net/MSF.897.525.

[19] A. Fayyaz, L. Yang, and A. Castellazzi, "Transient robustness testing of silicon carbide (SiC) power MOSFETs," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013-09-01 2013: IEEE, doi: 10.1109/epe.2013.6634645.

[20] X. Huang, G. Wang, Y. Li, A. Q. Huang, and B. J. Baliga, "Short-circuit capability of 1200V SiC MOSFET and JFET for fault protection," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013-03-01 2013: IEEE, doi: 10.1109/apec.2013.6520207.

[21] P. D. Reigosa, H. Luo, and F. Iannuzzo, "Implications of Ageing Through Power Cycling on the Short-Circuit Robustness of 1.2-kV SiC mosfets," *IEEE Transactions on Power Electronics,* vol. 34, no. 11, pp. 11182-11190, 2019, doi: 10.1109/TPEL.2019.2897636.

[22] H. Chen *et al.*, "Investigation on Short Circuit Test of 3300V SiC MOSFET," in *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2019-06-01 2019: IEEE, doi: 10.1109/edssc.2019.8754286.

[23] E. Eni, S. Bęczkowski, S. Munk-Nielsen, T. Kerekes, and R. Teodorescu, "Short-circuit characterization of 10 kV 10A 4H-SiC MOSFET," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 20-24 March 2016 2016, pp. 974-978, doi: 10.1109/APEC.2016.7467988.

[24] S. Sundaresan, V. Mulpuri, S. Jeliazkov, and R. Singh, "Avalanche and Short-Circuit Robustness of 4600 V SiC DMOSFETs," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, 31 March-4 April 2019 2019, pp. 1-7, doi: 10.1109/IRPS.2019.8720488.

[25] M. Okawa, T. Kanamori, R. Aiba, H. Yano, N. Iwamuro, and S. Harada, "Analysis of 1.2 kV SiC SWITCH-MOS after Short-circuit Stress," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2020-09-01 2020: IEEE, doi: 10.1109/ispsd46842.2020.9170050.

[26] D. Marroqui, A. Garrigos, J. M. Blanes, R. Gutierrez, E. Maset, and F. Iannuzzo, "SiC MOSFET vs SiC/Si Cascode short circuit robustness benchmark," *Microelectronics Reliability,* vol. 100-101, p. 113429, 2019, doi: 10.1016/j.microrel.2019.113429.

[27] A. Pérez-Tomás *et al.*, "Field-effect mobility temperature modeling of 4H-SiC metal-oxide-semiconductor transistors," *Journal of Applied Physics,* vol. 100, no. 11, p. 114508, 2006/12/01 2006, doi: 10.1063/1.2395597.

[28] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, "Thermal instability effects in SiC Power MOSFETs," *Microelectronics Reliability,* vol. 52, no. 9, pp. 2414-2419, 2012/09/01/ 2012, doi: https://doi.org/10.1016/j.microrel.2012.06.096.

[29] J. O. Gonzalez and O. Alatise, "Impact of BTI-Induced Threshold Voltage Shifts in Shoot-Through Currents From Crosstalk in SiC MOSFETs," *IEEE Transactions on Power Electronics,* vol. 36, no. 3, pp. 3279-3291, 2021, doi: 10.1109/TPEL.2020.3012298.

[30] F. Boige, A. Fayyaz, A. Castellazzi, F. Richardeau, and S. Vinnac, "Short-circuit robustness of parallel SiC MOSFETs and fail-safe mode strategy," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 3-5 Sept. 2019 2019, pp. P.1-P.10, doi: 10.23919/EPE.2019.8914891.

[31] A. Borghese *et al.*, "Effect of Parameters Variability on the Performance of SiC MOSFET Modules," in *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, 2018-11-01 2018: IEEE, doi: 10.1109/esars-itec.2018.8607593.

[32] J. Muting, P. Natzke, A. Tsibizov, and U. Grossner, "Influence of Process Variations on the Electrical Performance of SiC Power MOSFETs," *IEEE Transactions on Electron Devices,* vol. 68, no. 1, pp. 230-235, 2021-01-01 2021, doi: 10.1109/ted.2020.3039434.

[33] "Introduction," in *Design for Manufacturability and Statistical Design: A Constructive Approach*, M. Orshansky, S. R. Nassif, and D. Boning Eds. Boston, MA: Springer US, 2008, pp. 1-8.

[34] Z. Al Tarawneh, "The effects of process variations on performance and robustness of bulk CMOS and SOI implementations of C-elements," PhD, Faculty of Engineering, Newcastle University, 2012-06-21, 2011.

[35] K. Bernstein *et al.*, "High-performance CMOS variability in the 65-nm regime and beyond," *IBM Journal of Research and Development,* vol. 50, no. 4.5, pp. 433-449, 2006-07-01 2006, doi: 10.1147/rd.504.0433.

[36] K. Agarwal and S. Nassif, "Characterizing Process Variation in Nanometer CMOS," in *2007 44th ACM/IEEE Design Automation Conference*, 4-8 June 2007 2007, pp. 396-399.

[37] P. J. Timans, W. Lerch, J. Niess, S. Paul, N. Acharya, and Z. Nenyei, "Challenges for ultra-shallow junction formation technologies beyond the 90 nm node," in *11th IEEE International Conference on Advanced Thermal Processing of Semiconductors. RTP 2003*: IEEE, doi: 10.1109/rtp.2003.1249120.

[38] "Front End Variability," in *Design for Manufacturability and Statistical Design: A Constructive Approach*, M. Orshansky, S. R. Nassif, and D. Boning Eds. Boston, MA: Springer US, 2008, pp. 11-41.

[39] "Back End Variability," in *Design for Manufacturability and Statistical Design: A Constructive Approach*, M. Orshansky, S. R. Nassif, and D. Boning Eds. Boston, MA: Springer US, 2008, pp. 43-57.

[40] B. J. Baliga, "Power MOSFETs," in *Fundamentals of Power Semiconductor Devices*: Springer US, 2008, pp. 276-503.

[41] A. Bhalla, J. Bendel, and X. Li, "Robustness of SiC JFETs and Cascodes United Silicon Carbide supplies a," 2016.

Chapter 5. Short Circuit performance of SiC CASCODE JFETs in Parallel

5.1. Introduction

Paralleling power devices (chips, discrete devices, or modules) is a common way to achieve high power systems because it provides a less expensive and convenient solution to operating at the desired higher currents/power. This is especially advantageous in high current Silicon Carbide (SiC) applications with the increasing need for high power SiC modules and converters. However, current mismatch or unequal current sharing is a major constraint to the reliability, ruggedness, and robustness of the power devices and modules connected in parallel and consequently the overall system. Proper current sharing also allows for the optimal operation of the devices without derating.[1-3]

The current shared between parallel connected devices is dictated by switching time and operating conditions of each individual device. The switching time is controlled by variations and spread in the device and circuit parameters [1, 4-7]. As discussed in the previous chapter, parameter variation occurs because of variations in device operating conditions, and the device fabrication process. Another factor that advances parameter variation for parallel connected devices is the rate of degradation in each device (e.g. Gate resistance degradation, and solder joint degradation)[8]. These parameters influencing the sharing of current include variation of parasitic impedances, V_{TH} mismatch, pinch-off variation, operating temperature etc. This unequal current sharing between parallel connected devices is often tackled through careful device selection, clever system layout designs, and optimised control strategies. However, more studies are required to accurately predict the effects of these parameters on various operating conditions, and design better systems.

With the dominance of silicon for semiconductor applications previously, (i.e., Si IGBT modules, and converters) the influence of parameter spread on various operating conditions have been studied extensively in parallel connected Si IGBTs[1, 3, 9-14]. The superior quality

of the Si/SiO_2 interface in silicon devices structures ensures lesser parameter variation as a result fabrication or variable degradation rates, and consequently very short circuit robust devices in parallel[11, 15-17]. Early attempts at characterising parallel SiC JFETs using experiments showed that faster switching devices could cause a mismatch in current sharing, a mismatch switching losses, and reverse breakdown of the gate owing to parameter spread [4, 18, 19], all of these studies were done with the SiCED fast switching structure which required a buried p-layer and this is no longer the standard. Subsequently, little to no research was conducted on SiC JFETs with better performing normally-off the SiC MOSFET. In [20, 21], the authors demonstrated the competitive performance of a 100 A SiC MOSFET module employing five (5) 20 A, 1.2 KV, SiC switches connected in parallel to achieve the desired operating current, the electrical performance of the SiC modules was characterised at various temperatures up to 250 °C and benchmarked against similarly rated Si IGBT power modules. The SiC modules showcased better performance while being limited by immature substrate and encapsulation technology, with the authors recommending further research into more reliable packaging, more robust encapsulation materials, and better substrates. In subsequent publications, improved paralleled SiC MOSFET devices and module designs (i.e., converter and module layout, Gate driver design etc), better packaging approaches (Direct Bonded Copper, DBC, Direct Bonded Aluminium, DBA etc), and more suitable packaging materials (aluminium-nitride, AlN, alumina, Al_2O_3, Silicon-nitride, Si_3N_4 etc) were extensively studied using simulations and experiments. Switching characterisations at higher currents, 100-300 A, frequencies, ~50 kHz, and temperatures, 150-300 °C, are demonstrated whilst showcasing improved reliability metrics (Thermal cycling, HTGB, HTTB etc) [22-26]. With more compact designs, minimised parasitics, and optimised switching losses in SiC MOSFET modules, the short circuit robustness and the failure modes of parallel connected SiC devices (Cree's 1.2 KV/300 A and Rohm's 1.2 KV/180 A modules) were investigated in[27] providing some recommendations for operating in the Short Circuit Safe Operating Area (SCSOA). This was done with the use of an algorithm to limit the drain current or gate voltage during the short circuit event. In [28], the factors influencing the failure of parallel connected chips in a multi-chip configuration (Cree 1.2 KV/300 A) is investigated with only a few chips in the configuration undergoing failure after module failure, the authors attribute this failure mechanism to a non-uniformity of the short circuit stress experienced in each SiC chip. This conclusion is drawn after demonstrating a similar failure in parallel connected SiC discrete (TO-247, 1.2 KV/80 mΩ) devices of varying V_{TH} under short circuit. Consequently, a PSpice model is developed in [29] to estimate the short circuit performance and failure modes within Cree's 1.2 KV/300 A module, and the influences of parameter mismatch on short

circuit operation was investigated. The authors showed that V_{TH} mismatch during short circuit operation has a higher influence on failure than mismatch in the parasitic inductance. The results demonstrated that the device with the lowest V_{TH} switched fastest and takes the most current during short circuit operation coupled with the highest predicted junction temperature. Similar conclusions on parameter variation during short circuit parallel operation was drawn in [30-32]. A comprehensive characterisation of parasitic Inductance mismatch during short circuit parallel operation is conducted using experiments and LTSPICE simulations in [33], the author demonstrated that a combination of mismatch in a combination two parasitic inductances within the gate-source circuit loop creates the most imbalance in Short Circuit energy. A method for screening devices connected in parallel for better short circuit current sharing is proposed in [34] using the transfer curves of the power devices. The experimental results in this chapter were done collaboratively and published in [8, 35, 36].

Most of the work on characterising the parallel operation of SiC power devices especially under short circuit operation have been conducted on SiC MOSFETs with little studies on the SiC cascode JFET. Most of the studies employ compact models which sacrifices accuracy for shorter simulation time (e.g., Poor predictions of junction temperature within the power devices). Also, there's little studies on the impact of varying case temperature. Hence, this chapter demonstrates the short circuit characteristics of the SiC Cascode JFETs and SiC MOSFETs operated in parallel and explores the effects of parameter variation using experiments and finite element analysis (FEA).

In section 5.2, results of short circuit experiments for parallel connected devices with various parameter variations are presented. In sections 5.3 & 5.4, FEA mixed mode simulations (SILVACO ATLAS) were used to investigate the short circuit physics of SiC Planar, and Trench MOSFETs respectively whilst exploring the effects of parameter variation., Simulations with the same setup for SiC Cascode JFETs is presented in Section 5.5. The final section is the chapter conclusion.

5.2. Experimental setup and measurements

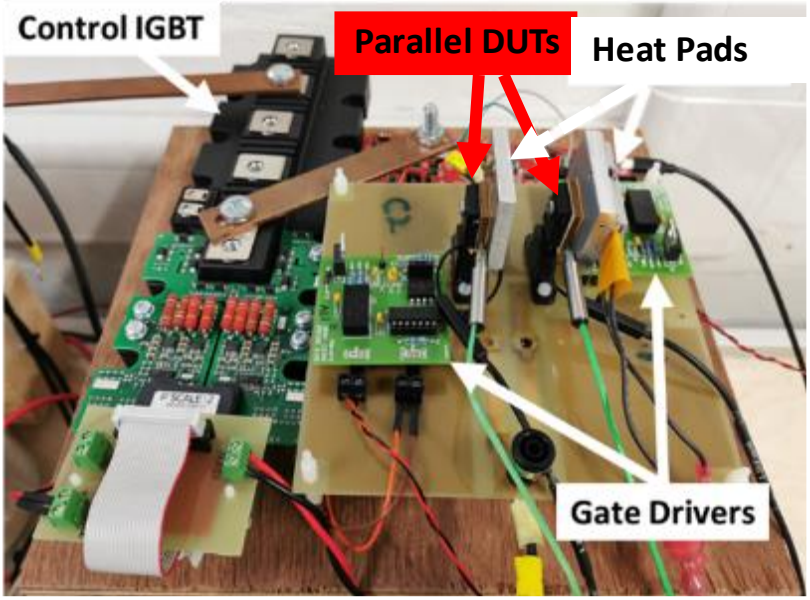
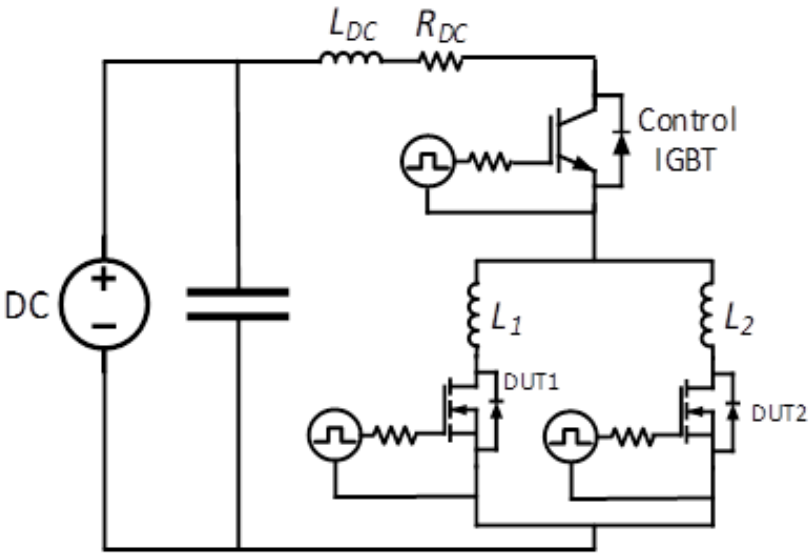


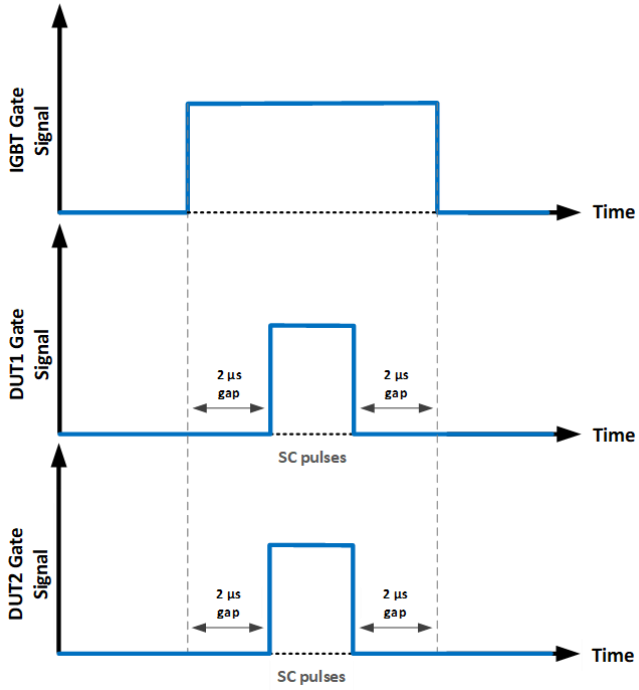
Figure 5.1 Parallel short Circuit Measurement setup

The experimental setup for parallel short circuit is the setup used in the single short circuit test with a second DUT socket added in parallel. A picture of the test circuit is shown in Figure 5.1. The figure also shows a separate gate driver used to drive the parallel DUT. This enables control of the parameters varied (e.g., external R_G). The test-rig comprises a DC power source, a 90 µF capacitor bank, a 1.2 kV/1 kA control IGBT module with datasheet reference FF1000R17IE4 and the devices under test (DUTs). The DUTs are 1200 V/20A SiC MOSFETs from ST with datasheet reference SCT20N120 while the SiC Cascode JFETs are 1200 V/18.4 A devices from United SiC with datasheet reference UJ3C120150K3S. Rogowski coils are used for current measurements and differential voltage probes are used for voltage measurement. Attached to the DUT is an electric heater connected to a power supply for performing measurements at higher temperatures.

Figure 5.2(a) shows the simplified circuit diagram of the test setup and Figure 5.2(b) shows the pulse sequence for the protection IGBT and the two DUTs in parallel. The signals for all three gate drivers are provided by a microcontroller. Like the test strategy during single short circuit, a buffer period is provided between the IGBT gate pulse and the two DUT gate pulses providing sufficient time for the DUTs to be disconnected. The measurements presented in this section are performed with variations in three parameters, (i) V_{TH} variation, (ii) R_G variation, and (ii) Temperature variation.

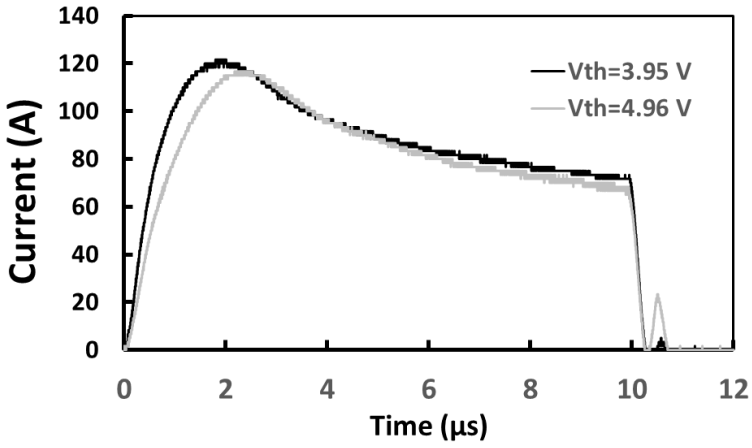


(a)

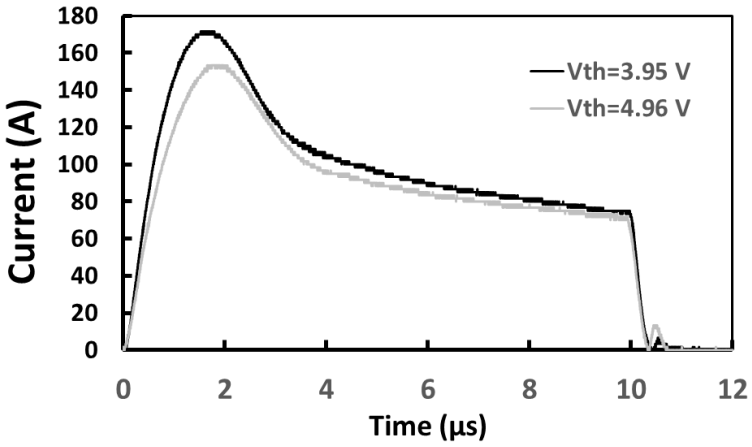


(b)

Figure 5.2 (a) Parallel short circuit test circuit (b) Gate pulse sequence



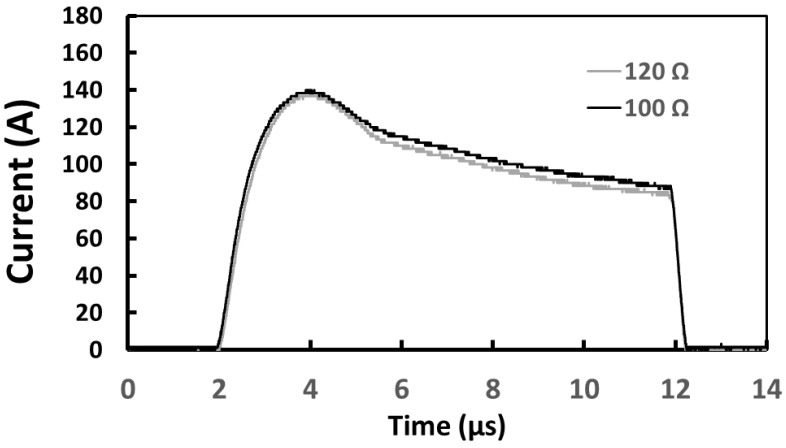
(a)



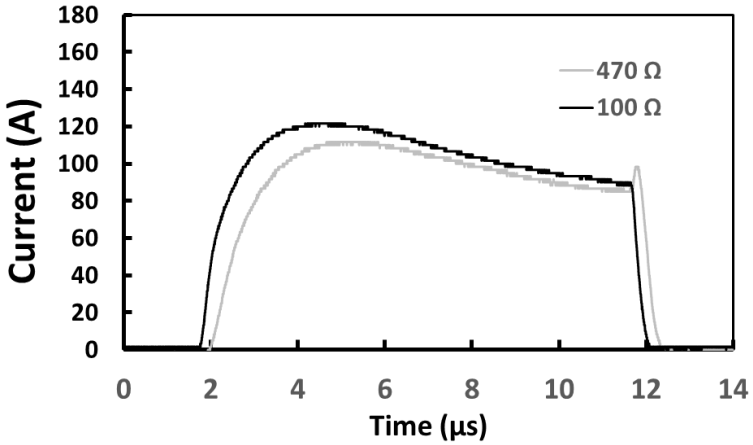
(b)

Figure 5.3 Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with 20% difference in V_{TH} with (a) 15 V gate voltages (b) 17 V gate voltage.

Figure 5.3(a) and Figure 5.3(b) shows the short circuit current for 1.2kV/20A SiC MOSFETs with a 20% variation in V_{TH} at gate voltages of 15 V and 17 V respectively. The maximum short circuit current for both DUTs increases from approximately 115 A and 120 A for the V_{GS} = 15 V to 150 A and 170 A for V_{GS} = 20 V. The DUT with lesser V_{TH} takes more current in both cases indicating reduced channel resistance. The difference in the SC energy of both DUTs is 5.1% and 8.1% for 15 V and 20 V respectively.



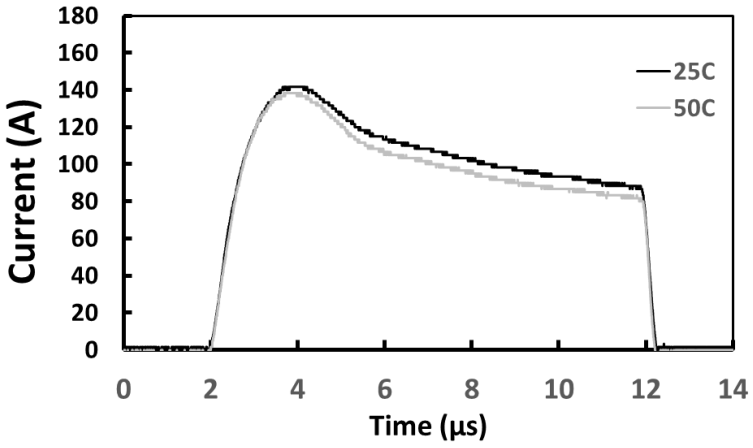
(a)



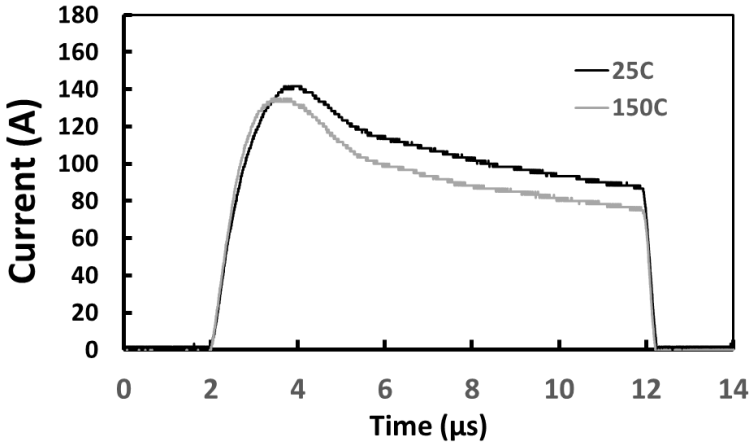
(b)

Figure 5.4 Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with (a) 20% difference in R_G (b) 370% difference in R_G.

Figure 5.4(a) and Figure 5.4(b) show short circuit current in parallel with varying gate resistances, R_G (R_G difference of 20%.and 370% respectively). An increase in the R_G of one of the DUTs in parallel causes an increased switching time and reduced short circuit duration for the corresponding device. This leads to a reduction in the short circuit energy evident in Figure 5.4. The case of 20% R_G increase corresponds to a 4.02% decrease in short circuit energy, while the 370% R_G increase corresponds to a 5.35% short circuit energy decrease.



(a)

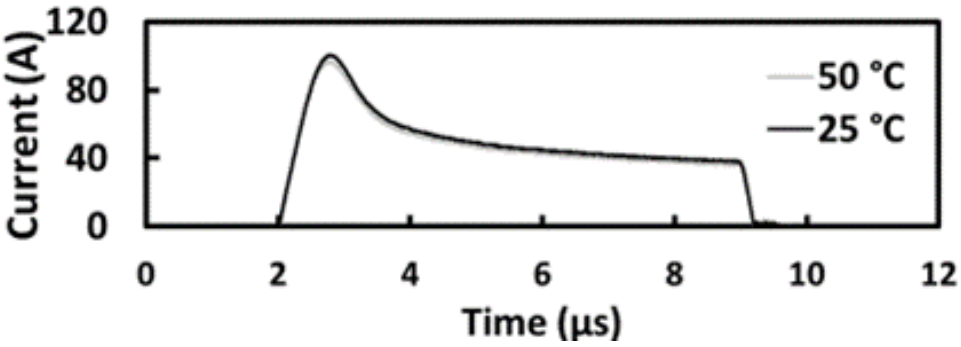


(b)

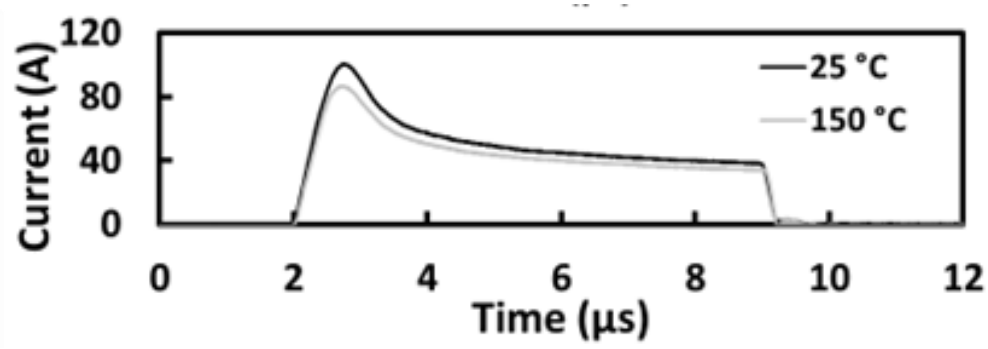
Figure 5.5 Measured Short circuit current for parallel 1.2kV/20A SiC MOSFETs with (a) 100% difference in T_{CASE} (b) 500% difference in T_{CASE}.

The measurements for variation in case temperature, T_{CASE} (initial Junction temperature, T_J) are shown in Figure 5.5. Figure 5.5(a) is for a 100% difference in T_{CASE}, while Figure 5.5(b) corresponds to a 500% difference in the T_{CASE}. The measurements show that the device with the lower initial T_J/T_{CASE} conducts a higher maximum short circuit current. The 100% and 500% T_{CASE} difference show a 6.36% and 12.31% difference in short circuit energy respectively. This can be attributed to the positive temperature coefficient of the short circuit resistance (mobility vs temperature curve) discussed in chapter 4.

Short circuit current measurements performed with variation in T_{CASE} (starting T_J) for the SiC cascode JFET (UnitedSiC 1.2 KV/20A). are shown in Figure 5.6. Figure 5.6(a) shows the measurements with a 20% difference in starting T_J, while Figure 5.6(b) shows the measurements with 500% starting T_J difference. A similar trend to the case of paralleled SiC MOSFETs is visible in the Cascode JFET measurements, the DUT with a higher starting T_J conducts lesser current.



(a)



(b)

Figure 5.6 Measured Short circuit current for parallel 1.2kV/18.4 A SiC CASCODE JFET with (a) 100% difference in T_{CASE} (b) 500% difference in T_{CASE}.

5.3. Simulation of short circuit in parallel SiC planar MOSFET

While a lot of effort has been made to model current sharing during parallel operation of power devices, most of these attempts have used compact models. Compact models are very useful for fast simulations, providing reasonable predictions for the parameter variation effects on current sharing during parallel operation, however these models usually take advantage of lumped parameters and simplified equations which help to provide better simulation time. In this section and the subsequent sections, the simulation of short circuit in parallel SiC devices using TCAD FEA analysis is presented with better insight into the device physics. This will provide more control of the device parameters varied and hence better predict the factors responsible for uneven current sharing while providing approximately more accurate values for TJ.

This section presents the simulations for SiC planar MOSFETs. Table 5-1 shows the parameters for the device structure used. The test circuit implemented in SILVACO mixed mode is presented in Figure 5.7. The structure has a breakdown of 1.2 KV like the SiC MOSFET used during experimental measurements. The parameters varied in the simulation are consistent with the parameters varied in the experiments, i.e., (i) V_{TH} variation, (ii) R_G variation (iii) Temperature variation, and additionally (iv) Parasitic inductance.

Table 5-1 SiC planar MOSFET structure parameters

Parameter	Planar
Source doping (cm-3)	$1x10^{19}$
Channel Length (µm)	0.5
Drift layer thickness (µm)	8.0
Drift layer doping (cm-3)	$1.5x10^{15}$
Drain doping (cm-3)	$1x10^{19}$
P-body doping (cm-3)	$1.5x10^{17}$
Oxide thickness (nm)	50
Cell pitch (µm)	10
Area factor (µm)	$1.2x10^{5}$
Breakdown (V)	1200

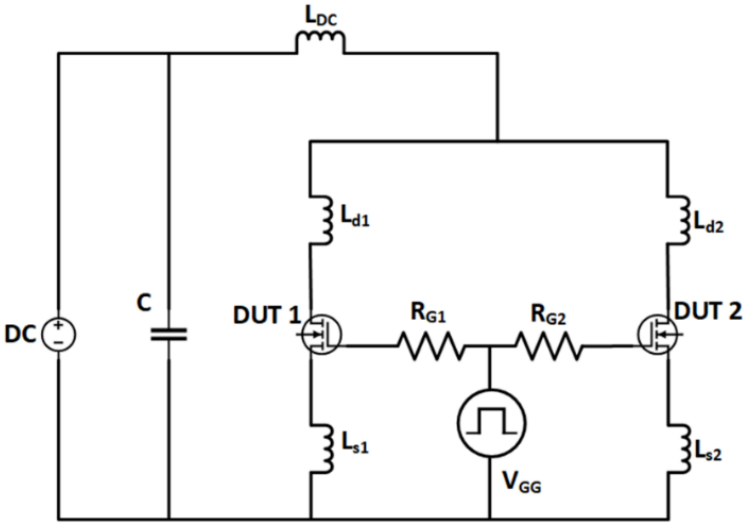


Figure 5.7 Mixed mode simulation circuit

- Varying V_{TH}

As discussed previously the V_{TH} of the MOSFET varies with various fabrication parameters. In this section the fabrication parameters varied to achieve a variation in V_{TH} were Current Spread Layer (CSL) doping, and fixed oxide charge (Q_F).

CSL doping.

Doping values in the CSL region of $1x10^{16}$ cm^{-3} and $2x10^{16}$ cm^{-3} corresponds to a V_{TH} of 5.11 V and 4.69 V respectively. Figure 5.8 shows the short circuit current of the parallel DUTs with the lower V_{TH} DUT conducting more current like the short circuit measurements. The DUT with V_{TH} = 4.69 V conducted a 12.4% higher maximum short circuit current than the 5.11 V DUT. There is also a change in T_J of 12.4%, with actual values predicted to be 1299°C and

1155.8 °C for the 4.69 V and 5.11 V DUTs respectively. This is much greater than the predicted temperature for compact models from various literature.

The CSL is located at the JFET region of the MOSFET and is used to optimise the device current density. It is responsible for shaping the current path and area, and hence determines the short circuit current density of the MOSFET. Therefore, a variation in the doping of this region will correspond to a difference in the maximum short circuit current, maximum T_J, and short circuit energy. This is evident in Figure 5.9(a) and (b), which is a plot of the 2D contours of current density and temperature respectively, this is extracted from Figure 5.8 at timestamp A. Figure 5.9 (a), shows that the current density in the device with V_{TH} = 4.63 V is greater than the device with V_{TH} = 5.12 V.

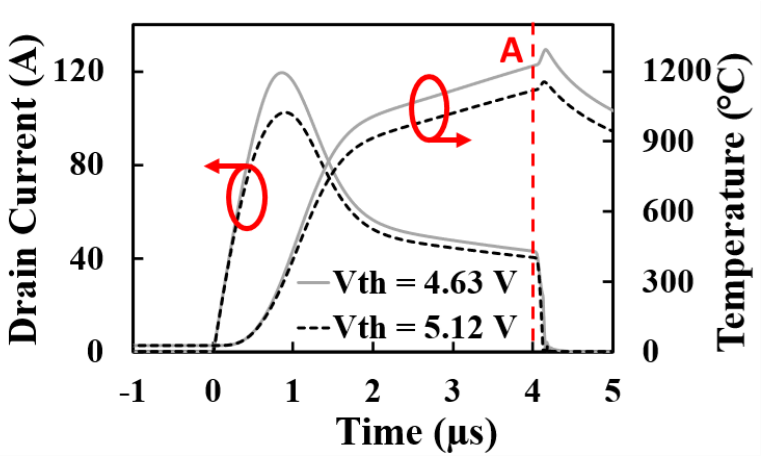
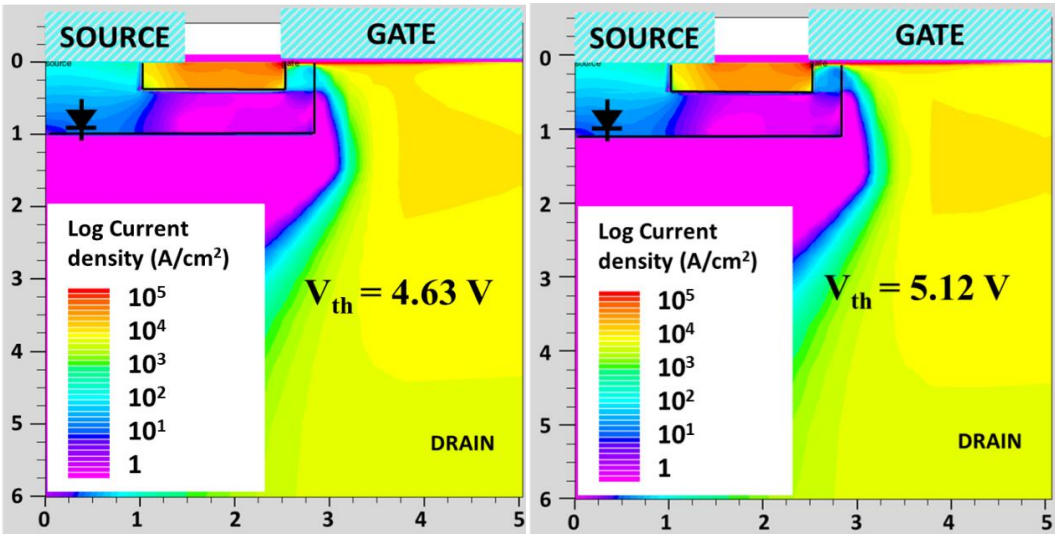
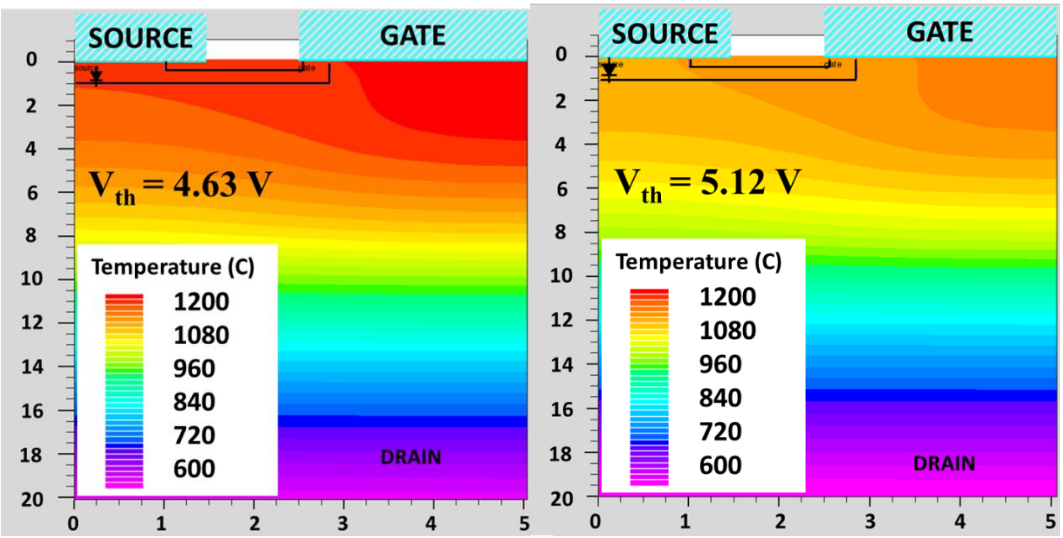


Figure 5.8 Simulated Short Circuit current and Junction temperature for parallel planar MOSFETs with varied V_{TH} (V_{TH} is varied through CSL doping)



(a)

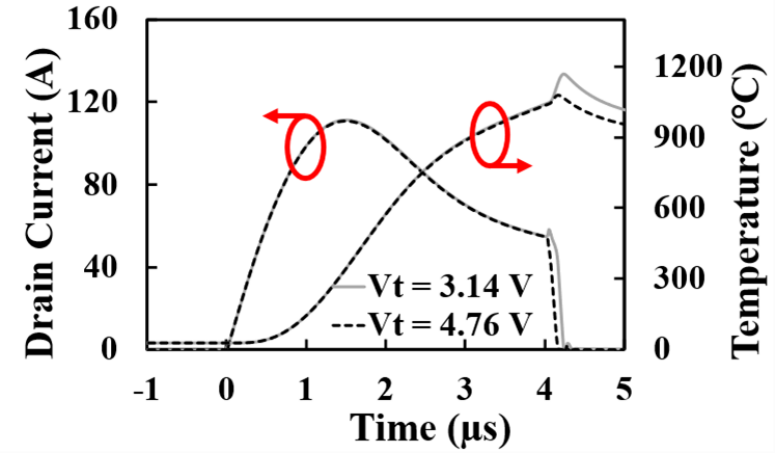


(b)

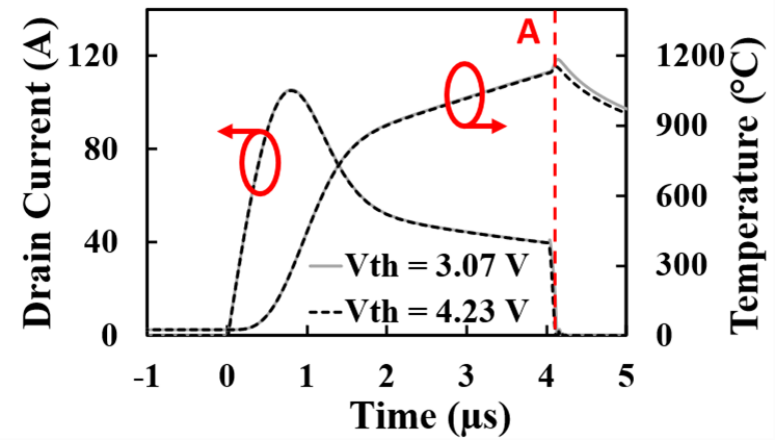
Figure 5.9 2D contours for parallel planar SiC MOSFETs with varied V_{TH} (a) Current Density (b) Temperature (V_{TH} is varied using CSL doping)

Fixed oxide charge (Q_F)

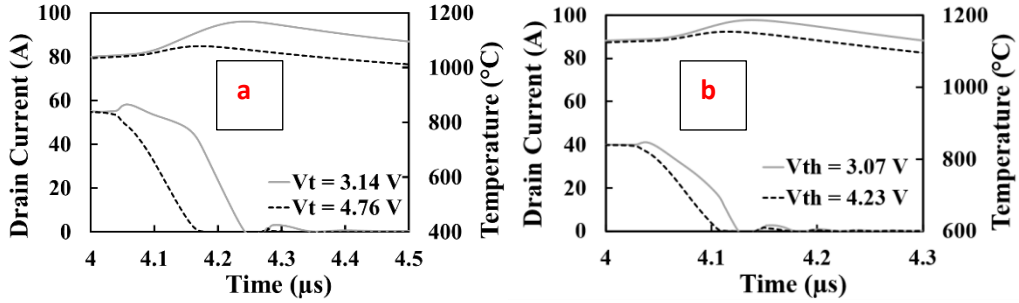
Figure 5.10 shows the simulated short circuit current of parallel planar SiC MOSFET structures with varied Q_F. Figure 5.10 (a) is for planar MOSFET structures with no CSL region while Figure 5.10 (b) is for structures with a CSL region of $1x10^{16}$, Figure 5.10 (c) is a plot of Figure 5.10 (a) and (b) zoomed in to the turn-off region at 4 µs. The structures are simulated with a Q_F density of $2x10^{11}$ and $7x10^{11}$, this corresponds to a V_{TH} of 4.76 V and 3.14 V respectively for the no-CSL case, and 4.23 V and 3.07 V for the case with a CSL region. Figure 5.10 (a) and (b) demonstrate a minuscule effect on current sharing during turn-on with a variation in Q_F density at the SiC/SiO_2 interface, hence there is no effect on the peak short circuit current shared between the devices in parallel. However, the results show that there is an effect during the turn-off, this effect is similar to the turn-off behaviour from experimental measurements with varying R_G (Figure 5.4). The device with higher Q_F densities experiences a delayed turn-off of 25 ns and 100ns for the CSL case and no CSL case respectively, which leads to a spike in the temperature within this MOSFET at turn-off. The corresponding difference in temperature for both the CSL case and no CSL are 32.15°C and 90°C respectively. The use of a CSL region to optimise the device is evident in Figure 5.10(b), the structure suppresses the short circuit current better and switches faster than the case of no CSL. It also reduces the delay experienced by the higher Q_F structure and the temperature spike. However, the CSL does not fully eliminate the delayed turn-off and temperature spike. Over the lifetime of the MOSFET, variations in Q_F combined with other parameter variations can further degrade the gates in parallel unevenly and further increase this difference in the T_J.



(a)



(b)

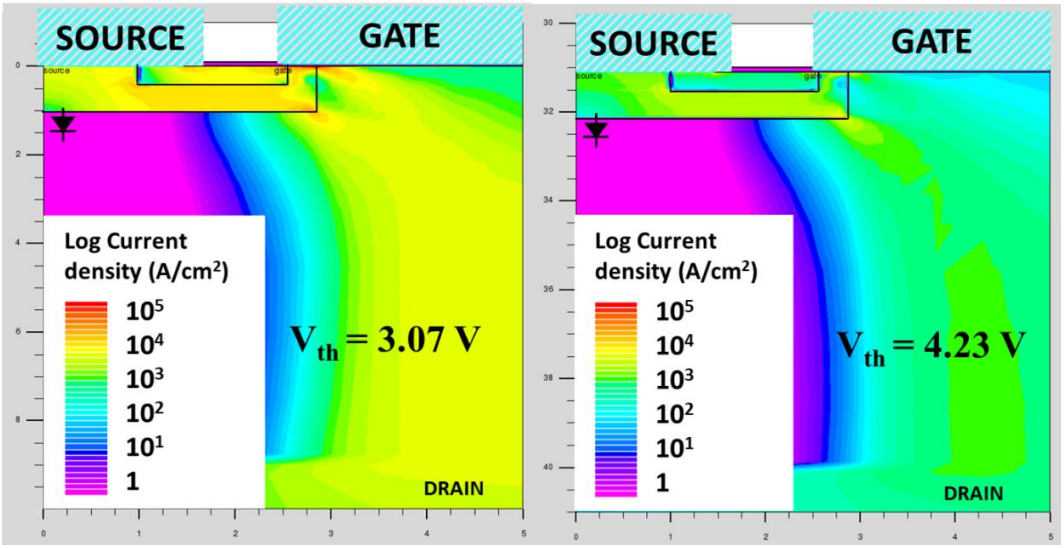


(c)

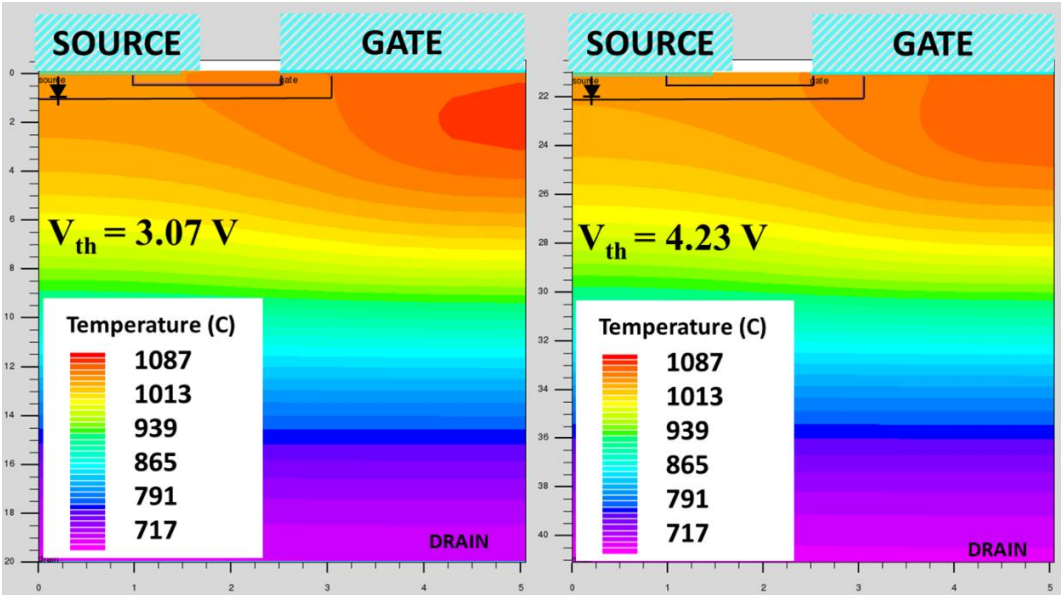
Figure 5.10 Simulated Short Circuit current and Junction temperature for parallel planar MOSFETs with varied V_{TH} (V_{TH} is varied through fixed oxide charge Q_F) (a) No-CSL case (b) CSL case (c) Zoomed in plots of a & b at point A

Figure 5.11(a) and (b) shows the CSL case contour plots of current density and temperature at timestamp A from Figure 5.10(b). At turn-off, the current density contour of the device with higher Q_f (lower V_{TH}) is more saturated. Two current paths can be seen in the figure, the top current path is due to electron current, and the lower current path is due to the hole

current. The sharp increase in T_J at turn-off is evident in the 2D contours of temperature in Figure 5.11(b)



(a)



(b)

Figure 5.11 2D contours for parallel planar SiC MOSFETs with varied V_{TH} for the NO-CSL case (a) Current Density (b) Temperature (V_{TH} is varied using interface charge

- Varying R_G

The measurements performed for parallel SiC MOSFETs devices with variable R_G (external gate resistance) are analysed using TCAD simulations and presented in Figure 5.12 and Figure 5.13. The simulation with 20% difference in R_G is shown in Figure 5.12 while the simulation with 370% R_G difference is shown in Figure 5.13. The short circuit current sharing behaviour of the from experiments (Figure 5.4) is predicted with high fidelity for both cases, showing that there is a spike in the short circuit current at turn off. From Figure 5.13, the curve of T_J

shows a spike at turn off in the DUT with 470 Ω, with a 10.9% difference in T_J between the two MOSFETs in parallel. To explain this characteristic, 2D contour plots of Hole current density and temperature were extracted at timestamp A in Figure 5.13 and are shown in Figure 5.14.

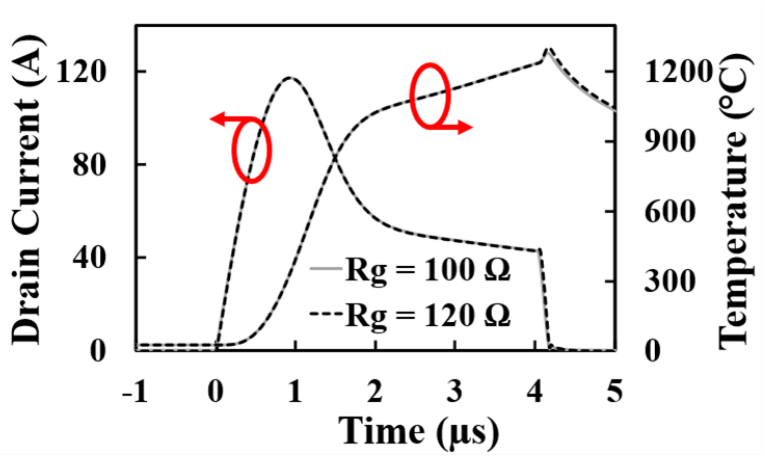


Figure 5.12 Simulated Short circuit current and Junction temperature for parallel SiC MOSFETs with 20% difference in R_G.

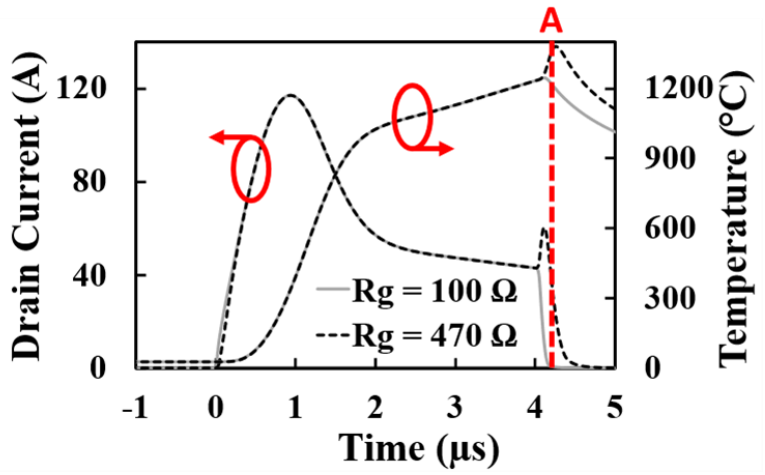
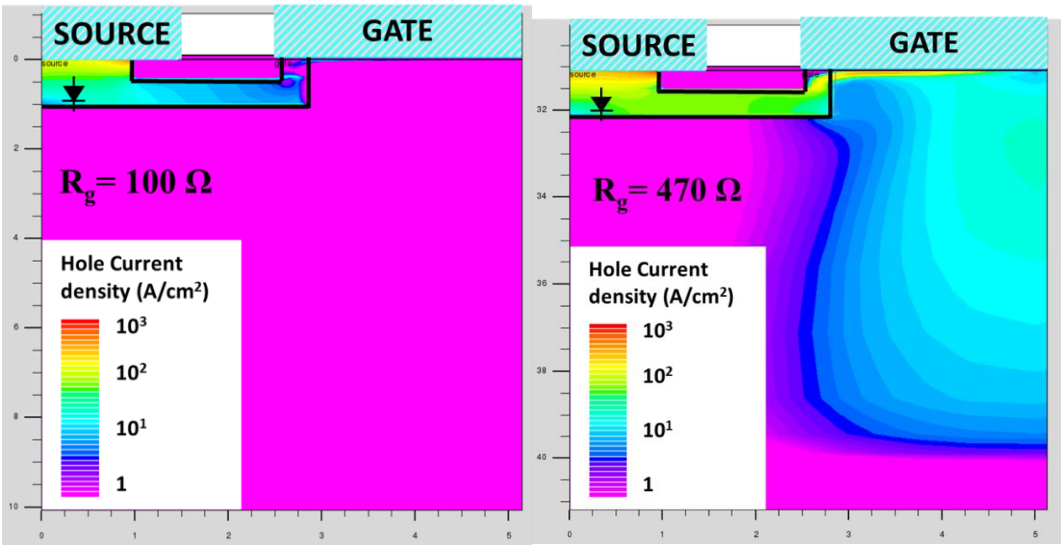
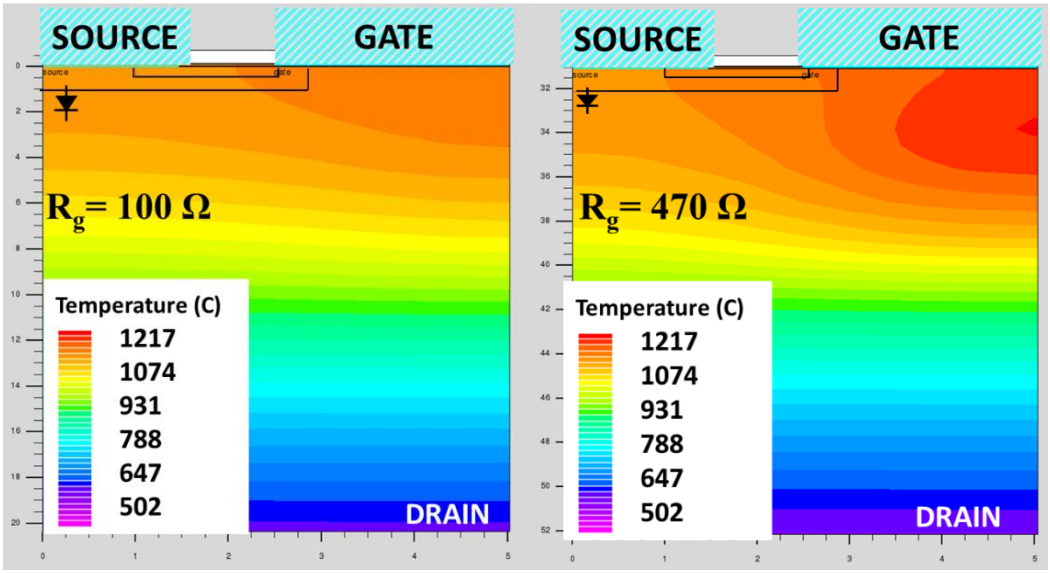


Figure 5.13 Simulated short circuit current and Junction temperature for parallel SiC MOSFETs with 370% difference in R_G.

From Figure 5.14(a), a substantial flow in the hole current is observed flowing from the P-well region of the device with 470 Ω R_G into its gate, the device with 100 Ω R_G successfully turns off with no hole current flowing within the device cell. Figure 5.14(b) shows the difference between the temperature at the junction of the two DUTs in parallel.



(a)



(b)

Figure 5.14 2D contours of planar SiC MOSFETs in parallel with 370% difference in R_G (a) Hole current density (b) Temperature

- Varying Temperatures

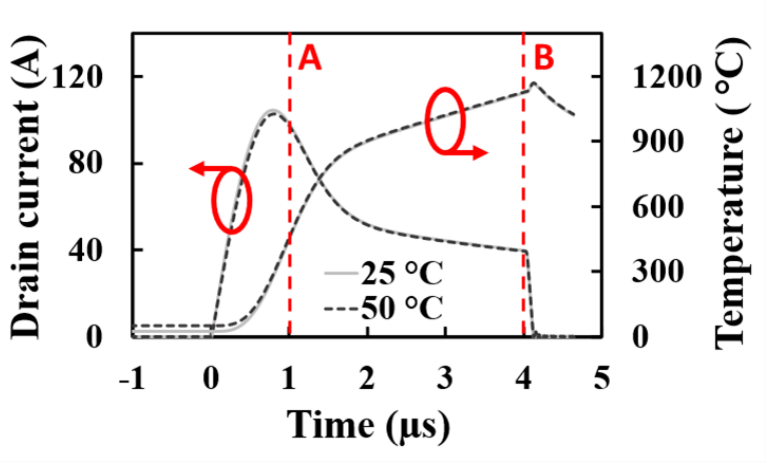
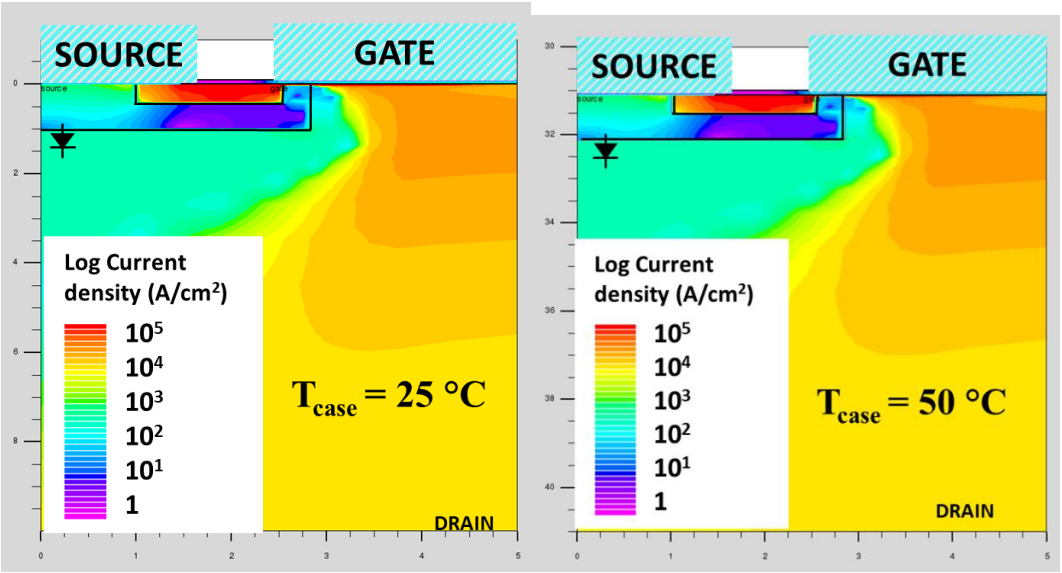
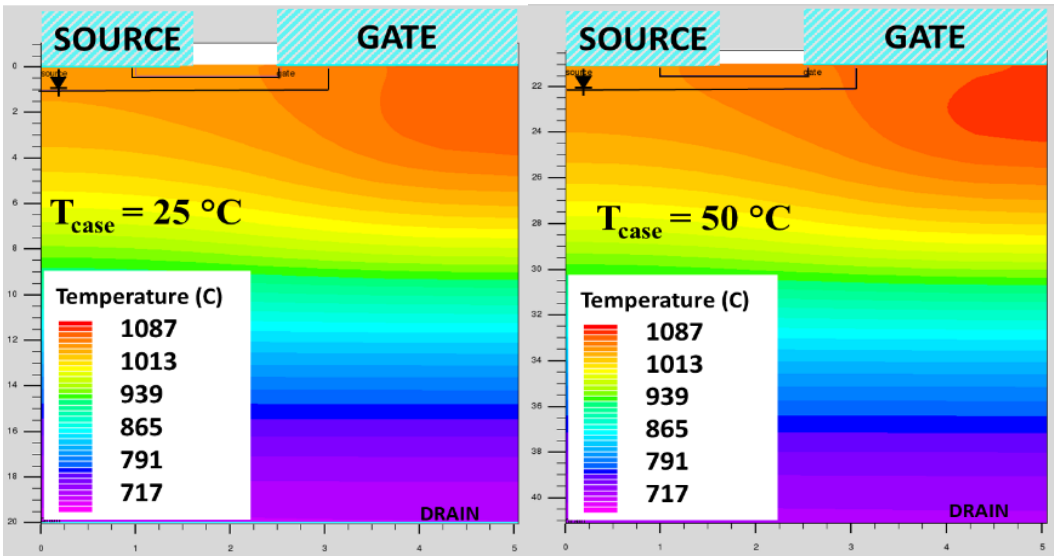


Figure 5.15 Simulated short circuit current and junction temperature of parallel SiC planar MOSFETs with 100% case temperature difference.

Figure 5.15 shows the short circuit current plot of parallel SiC MOSFETs simulated with 100% difference in starting T_J. The predicted current sharing between the two DUTs follow a similar trend as experimental results shown in Figure 5.5, the DUT with a higher starting T_J takes less current, however the difference in maximum short circuit current predicted is much lesser than in experiments (104.59 A and 102.77 A corresponding to 25 °C and 50 °C respectively). The difference in the maximum T_J within the device is 8 °C. 2D contours of the two MOSFETs at timestamp A and B from Figure 5.15 are extracted and shown in Figure 5.16. Figure 5.16(a) shows the current density contours from timestamp A with both figures almost identical and Figure 5.16(b) shows the temperature contours extracted at timestamp B.



(a)



(b)

Figure 5.16 2D contours for parallel planar SiC MOSFETs with varied T_{CASE} (a) Current Density (b) Temperature

Figure 5.17 demonstrates the simulated short circuit current with 500% difference in T_J, the 25 °C MOSFET conducts a current of 103.15 A while the 150 °C MOSFET conducts 94.07 A. There was a 3.8% difference with respect to maximum T_J within the MOSFETs, with the 25 °C MOSFET reaching a maximum T_J of 1160.48 °C and 1204.64 °C for the 150 °C MOSFET. The extracted 2D contours of current density and temperature are shown in Figure 5.18(a) and (b) respectively. The plot of current density demonstrates the higher current density within the device of lower starting T_J.

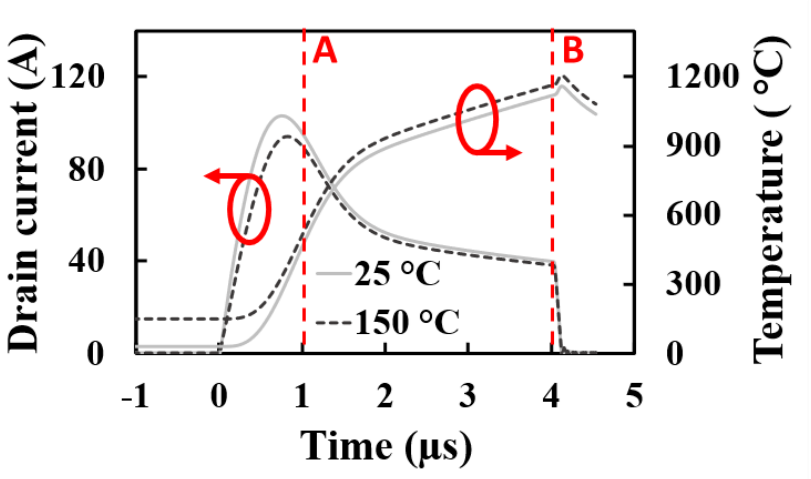
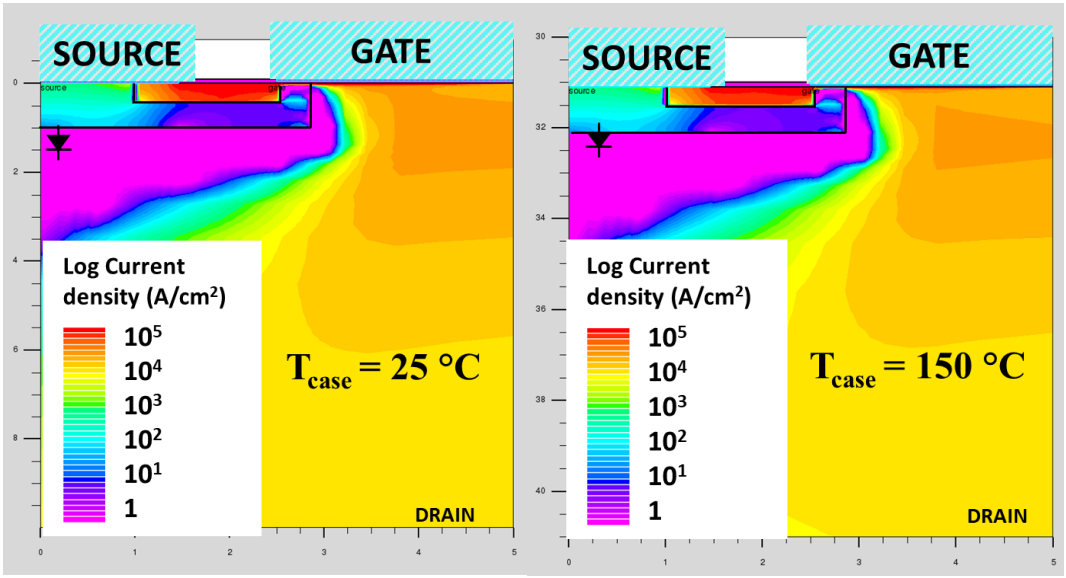
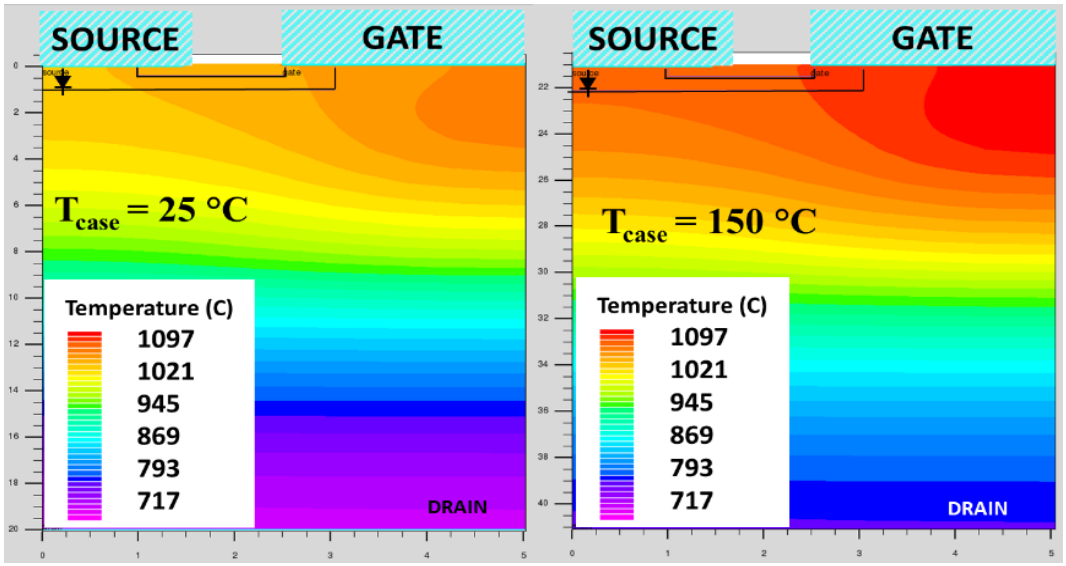


Figure 5.17 Simulated short circuit current and junction temperature for parallel SiC planar MOSFETs with 500% case temperature difference.



(a)



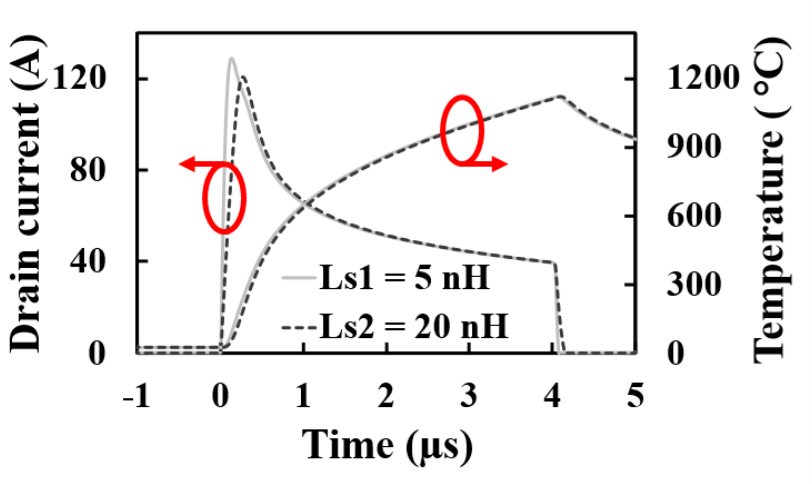
(b)

Figure 5.18 2D contours for parallel planar SiC MOSFETs with varied T_{CASE} (a) Currnt Density at Timestamp A of Figure 5.17 (b) Temperature at Timestamp B of Figure 5.17

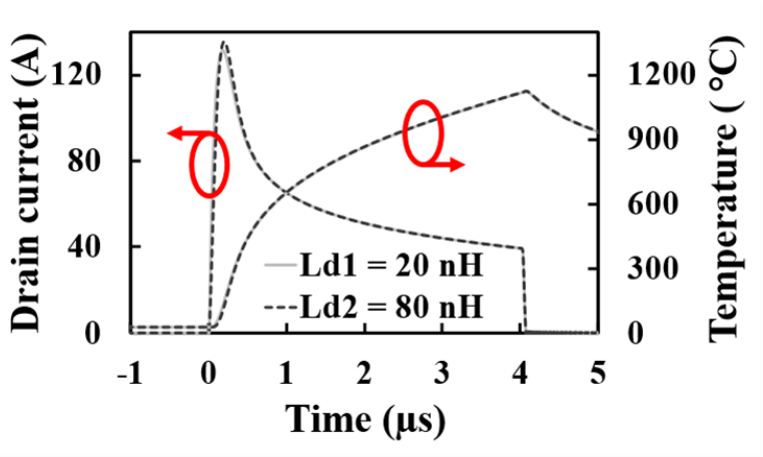
- Varying parasitic inductance

The parasitic inductances varied for the parallel short circuit simulations are identified in the simulation circuit (Figure 5.7), that is, the parasitic drain inductance, L_d, and parasitic source inductance, L_s. The simulation was done with a low power loop inductance (L_{DC} = 100 nH), and a high power loop inductance (L_{DC} = 900nH). The low L_{DC} corresponds to power chips, optimised module designs, and discrete devices packages with a kelvin source (TO-247-4). The test system and devices used for the parallel short circuit experiments in section 2 corresponds to the high L_{DC} case. This is because the devices used were TO-247-3 packaged discrete devices and the extra inductances introduced by the PCB. Figure 5.19 shows the

current and temperature of the parallel DUTs with varied parasitic Inductance for the low L_{DC} instance. Figure 5.19(a) shows the simulation with a 400% difference in L_s while Figure 5.19 (b) is for a 400% difference in L_d at. In terms of the current sharing, a variation in source inductance, L_s at low L_{DC} has the largest impact on current sharing. There was an increase of 6.8% in the maximum I_{SC} conducted by the DUT with a lower L_s as it turns on faster than the second DUT in parallel. The T_J difference is however minuscule with a change of 0.06%. This is because the device with a higher L_s turns on and off slower with a longer SC time, hence the short circuit energy conducted by both devices is approximately the same (94 mJ). The variations in L_d have almost no effect on the device current sharing and short circuit energy at low L_{DC} for the 400% difference.



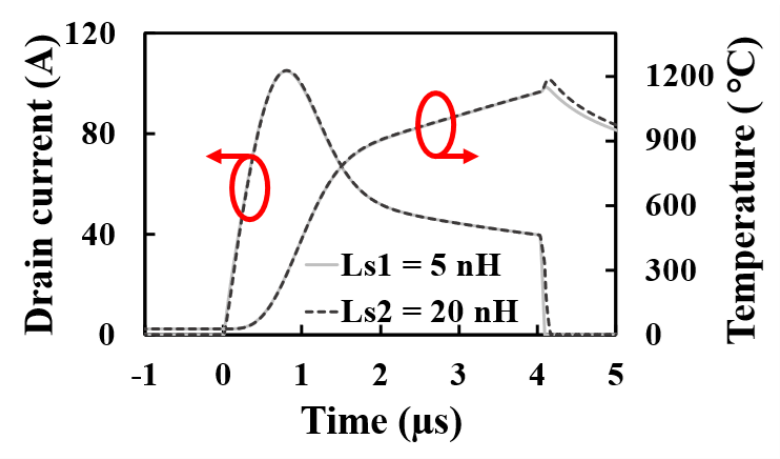
(a)



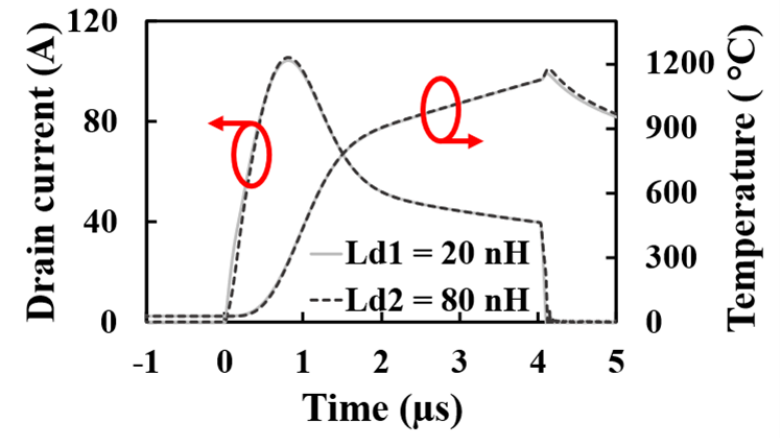
(b)

Figure 5.19 Simulated short circuit current and Junction temperature for parallel SiC planar MOSFETs with 400% variation in parasitic source inductance L_S (a) Low power loop inductance (b) High power loop Inductance.

The simulation is repeated for the instance of High L_{DC} while keeping the same parameters as the low L_{DC} case and the simulation results are shown in Figure 5.20. From the plots, it is obvious that with high L_{DC}, the DUTs conducts lesser short circuit and with decreased di/dt for both simulations. The device maximum I_{SC} is suppressed and the turn on is regulated by the L_{DC}, hence both devices conduct similar maximum I_{SC}. Variations in both L_s and L_d present with almost no difference in maximum I_{SC} in the DUTs. However, there are small differences in the switching which cause a spike in the maximum T_J at turns off for both cases. The spike in T_J for variation in L_s is larger because it has a higher impact on the switching time as is evident in Figure 5.20(a)



(a)



(b)

Figure 5.20 Simulated short circuit current and Junction temperature for parallel SiC planar MOSFETs with 400% variation in parasitic drain inductance L_D (a) Low power loop inductance (b) High power loop Inductance.

5.4. Simulation of short circuit in parallel SiC trench MOSFET.

The parameters varied during experiments in section 5.2, and the SiC planar MOSFET simulations in section 5.3 have been replicated except in a few cases. These are the cases constrained by the difference in device structures. The circuit for the simulation is the same as in Figure 5.7, and the key dimensions for the SiC Trench MOSFET used in this section are shown in Table 5-2 while Figure 5.21 depicts a 2D half-cell structure of the Trench MOSFET. The structure is based on the double trench design with channels on either side of the gate trench[37, 38].

Table 5-2 Trench structure parameters

Parameter	Trench
Source doping (cm-3)	$1.0x10^{19}$
Drift layer doping (cm-3)	$1.5x10^{15}$
Drain doping (cm-3)	$1.0x10^{19}$
Gate trench depth (µm)	1.2
Gate trench width (µm)	1.0
Source trench depth (µm)	1.2
Source trench width (µm)	1.0
Channel Length (µm)	0.5
Drift layer thickness (µm)	8.0
Oxide thickness (nm)	50
P-body doping (cm-3)	$2.5x10^{17}$
Half Cell pitch (µm)	1.7
Area factor (µm)	$1.5x10^{6}$
Breakdown (V)	1200

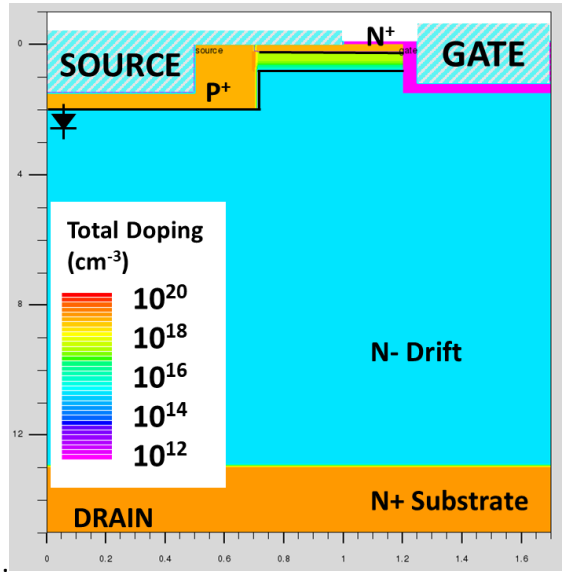


Figure 5.21 SiC Trench MOSFET Device structure (Half cell pitch)

- Varying V_{TH}

CSL doping.

Figure 5.22 shows the simulated current and temperature for variations in the V_{TH} of the SiC Trench MOSFET. The V_{TH} variation is achieved by varying the CSL region doping. In practice this is achieved either by a double epitaxy layer with the desired CSL doping or an extra implantation step for the CSL region during device fabrication. In both cases variations can be introduced more so for the implantation case. The simulation is performed with a doping of $1x10^{16}$ and $2x10^{16}$ (cm^{-3}) corresponding to a V_{TH} of 8.01 V and 7.9 V respectively. The lower V_{TH} device conducts a larger I_{SC} and has a higher T_J within the device structure. The max I_{sc} increases by 7.6 %, while the T_J increases by 5.2%.

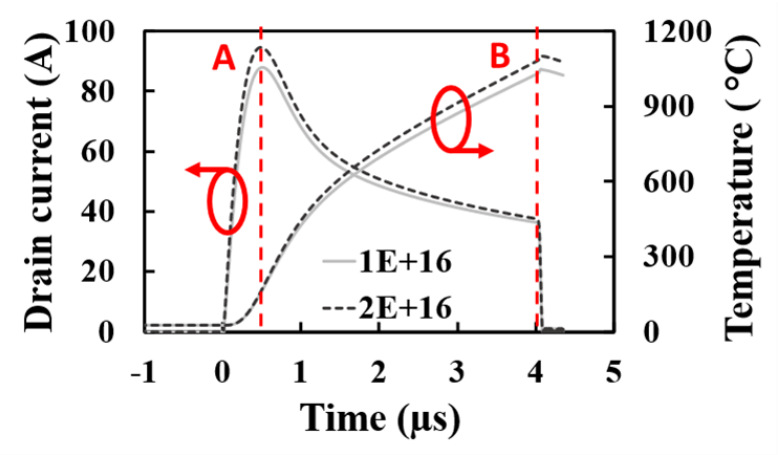
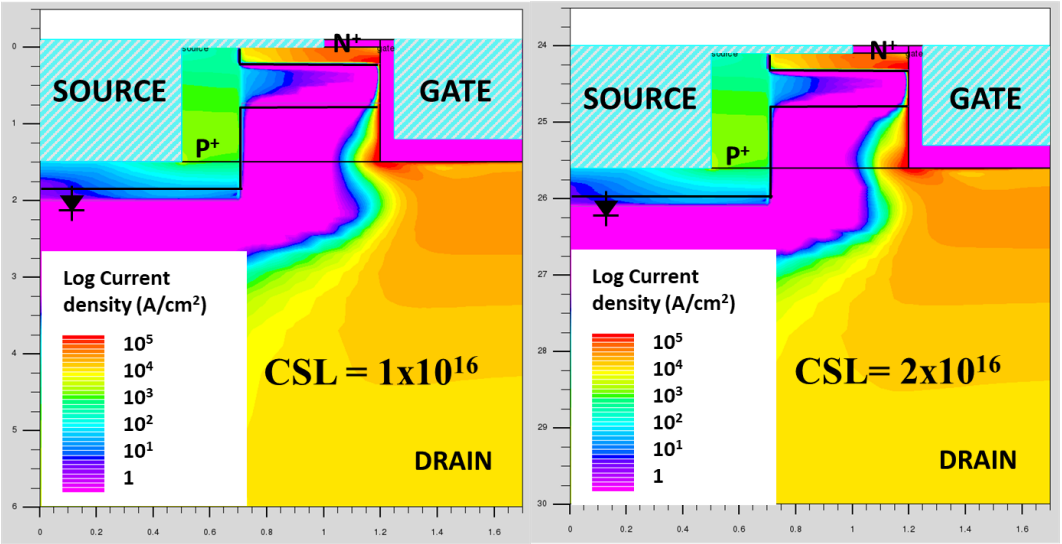
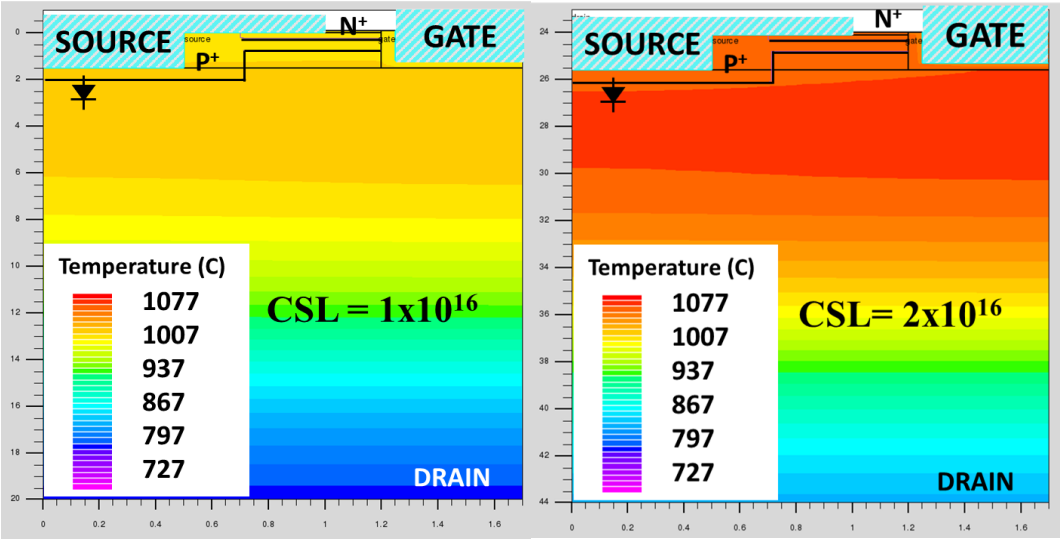


Figure 5.22 Simulated Short Circuit current and Junction temperature for parallel SiC Trench MOSFETs with varied V_{TH} (V_{TH} is varied through CSL doping)

The 2D contour plots of total current density and temperature within the Trench MOSFET structures are extracted at timestamp A and B from Figure 5.22 and shown in Figure 5.23(a) and (b) respectively. The plots show that during a short circuit event, the hotspot is just below the trench gate. It is evident that the device with lesser V_{TH} from Figure 5.23(a) go through a much higher temperature leading to higher stress on the gate oxide.



(a)



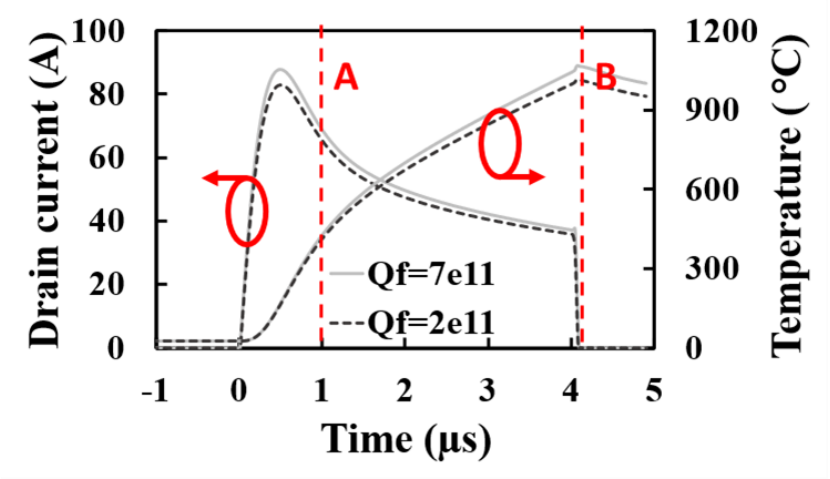
(b)

Figure 5.23 2D contours for parallel Trench SiC MOSFETs with varied V_{TH} using CSL (a) Current Density (b) Temperature

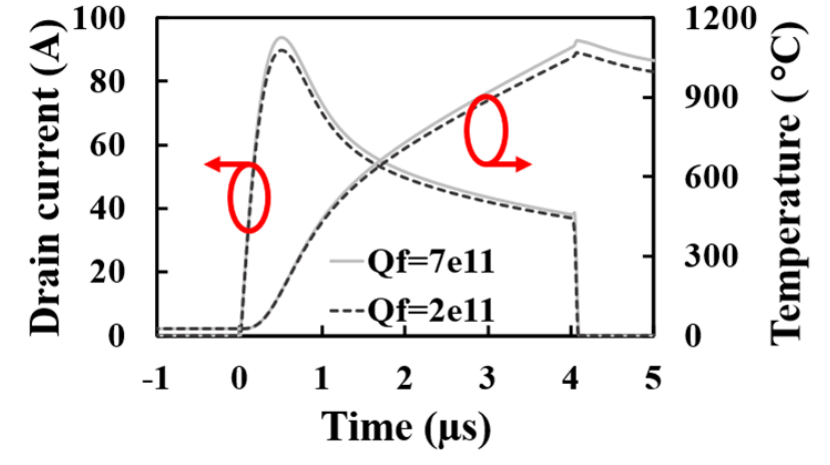
Fixed oxide charge (Q_F)

To achieve variation in the V_{TH} of the trench device under parallel short circuit conduction, the Fixed oxide charge was also varied. Similar to section with the SiC planar MOSFET structure , the simulations were done for two variations in the trench structure, i) structure without a CSL region (Figure 5.24(a)) and ii) a structure with CSL region (Figure 5.24(b)). The charge density used were $7x10^{11}$ and $2x10^{11}$ (cm^{-3}) corresponding to a V_{TH} of 6.37 V and 7.53 V in the CSL case, and 7.64 V and 6.47 V in the no CSL case. Unlike the case of the planar structures where the Q_F showed a minute impact on the current sharing between the paralleled device in short circuit, the case of the SiC trench device presents with relatively higher differences in the short circuit stress experienced within the paralleled devices. The

device with higher Q_F (less V_{TH}) conducts a higher short circuit energy and experiences a higher temperature at the gate oxide like the CSL variation in the previous section. The difference in maximum I_{SC} and maximum T_J is 5.90% and 5.12% respectively for the no CSL case, while the structures with a CSL region has a 4.50% and 4.32% increase in max I_{SC} and T_J respectively. Like simulations in the planar MOSFET structure, the CSL region can be used to optimise the device structure, and the CSL doping increases the JFET region mobility and reduces the $R_{DS\text{-}ON}$. As a result, it reduces the difference in maximum current conducted by the devices in parallel, and the difference in short circuit stress.



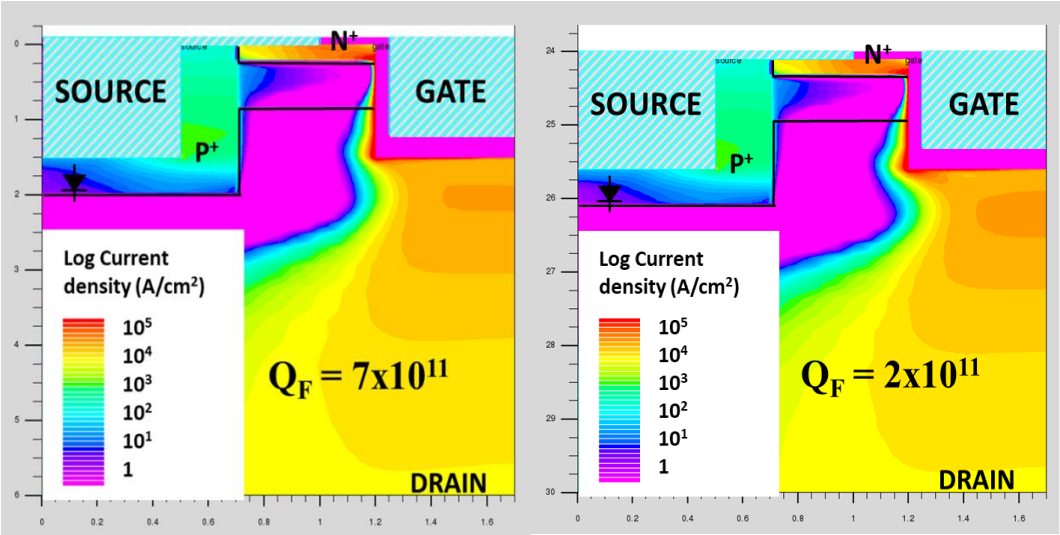
(a)



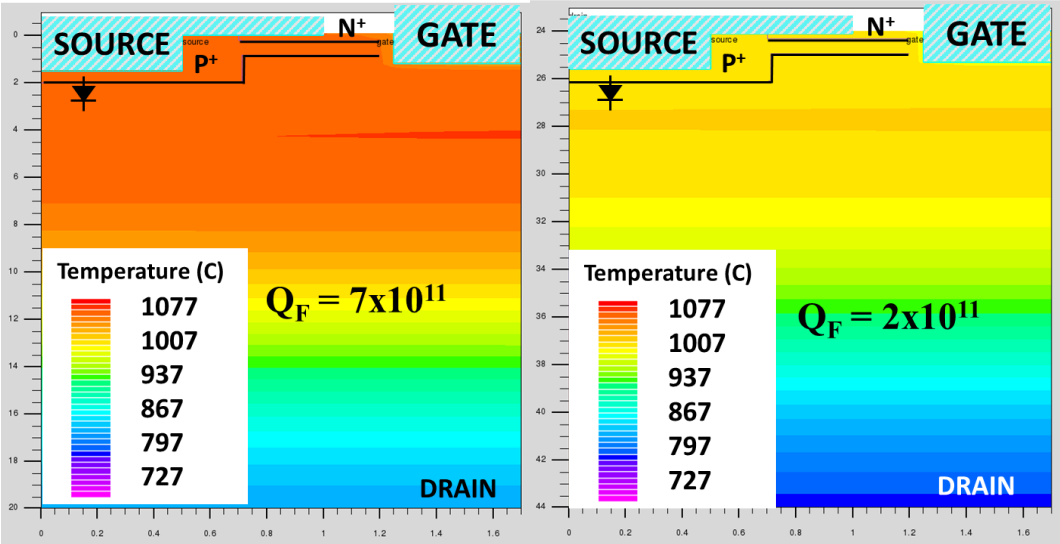
(b)

Figure 5.24 Simulated Short Circuit current and Junction temperature for parallel SiC Trench MOSFETs with varied V_{TH} (V_{TH} is varied through fixed oxide charge QF) (a) No CSL case (b) CSL case.

Figure 5.25(a) shows the contours of total current density at timestamp A from Figure 5.24(a), and Figure 5.25(b) shows the temperature within the structure at timestamp B from Figure 5.24(a). Both plots are for the no CSL case of variations in oxide charge, Q_F, with the higher temperature evident in the higher Q_F trench structure.



(a)



(b)

Figure 5.25 2D contours for parallel SiC Trench MOSFETs with varied V_{TH} using interface charge (NO-CSL case) (a) Current Density (b) Temperature

- Varying R_G

Figure 5.26 presents the short circuit current of parallel Trench MOSFET with 20% variation in the external gate resistance, R_G. The plot presents with almost no difference in the current shared between the parallel devices. However, a small spike in the temperature is visible at turn off for the MOSFET with R_G = 120 Ω. The reason is the larger R_G caused a longer short circuit duration, and hence greater short circuit energy like the simulations with a difference in L_s and Q_F. The 2D contour plots of total current density and temperature at timestamp A from Figure 5.26 are extracted and presented in Figure 5.27(a) and Figure 5.27(b) respectively. From the plots, it is evident that the two paralleled devices experience almost identical short circuit stress.

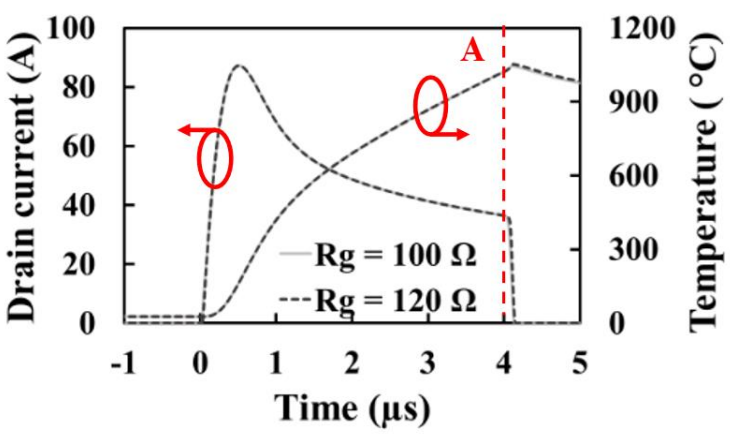
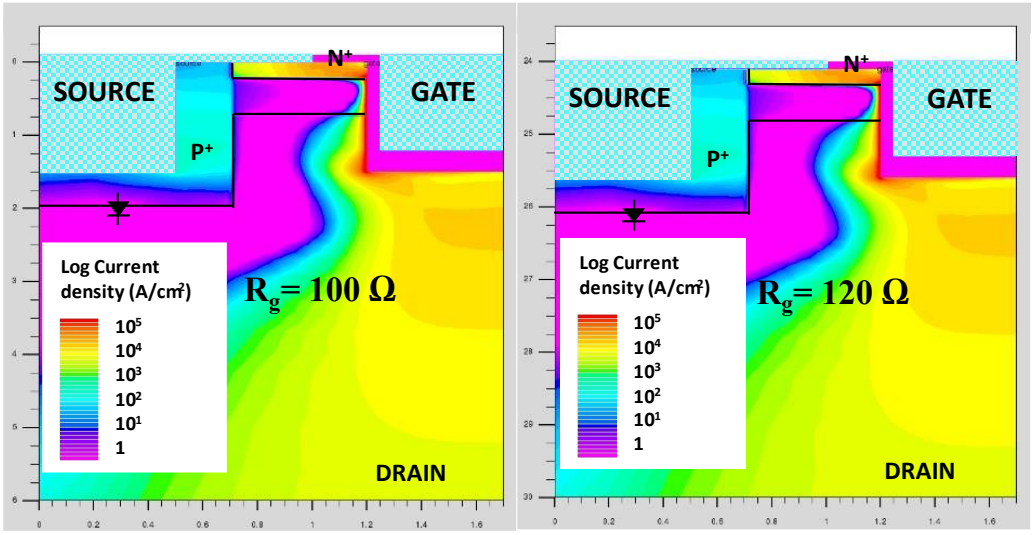
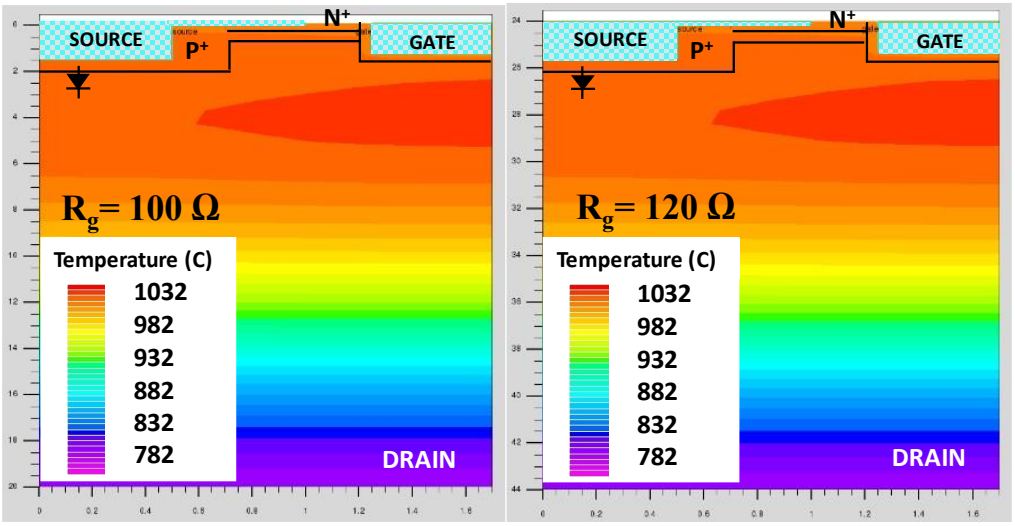


Figure 5.26 Simulated short circuit current and Junction temperature of parallel Trench SiC MOSFETs with 20% difference in R_G



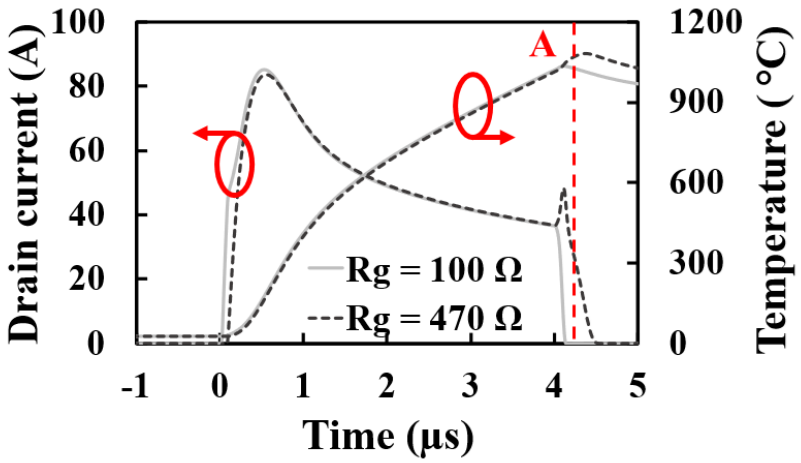
(a)



(b)

Figure 5.27 2D contours for parallel SiC Trench MOSFETs with varied R_G (a) Current Density (b) Temperature

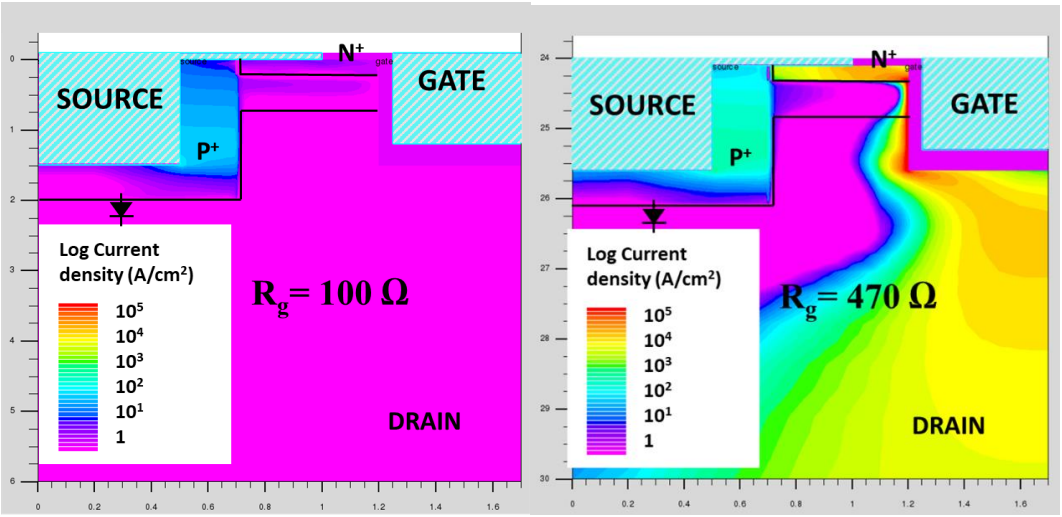
The simulation result for a 370% variation in R_G is shown in Figure 5.28. Again, only the turn-off is considerably impacted, but the turn-off procedure is slightly different in this case. The short circuit current exhibited a spike at turn-off for the larger R_G MOSFET, with the T_J also considerably larger. The difference in current at turn-off was 33%, and difference in maximum T_J was 4.42%.



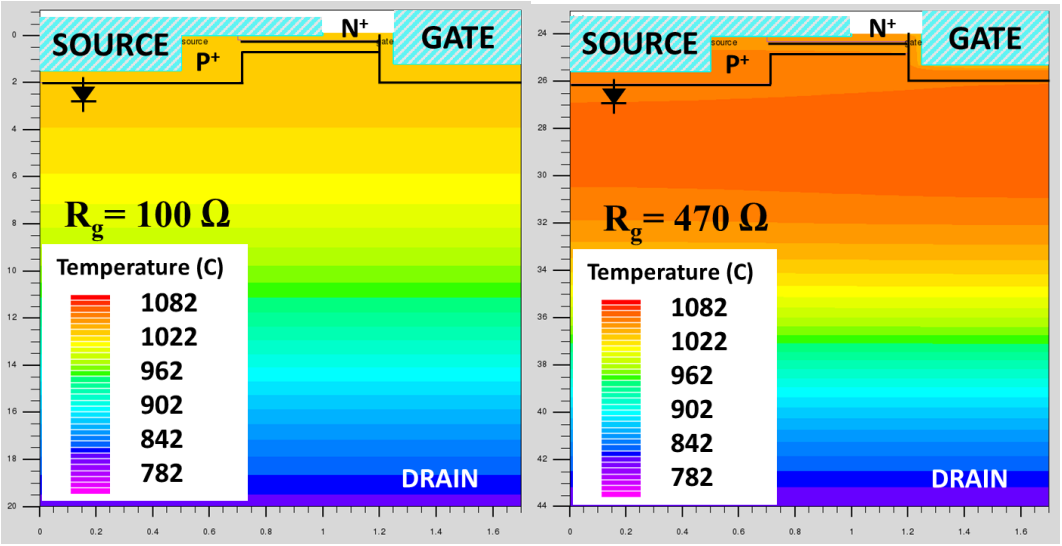
(a)

Figure 5.28 Simulated short circuit current and Junction temperature of parallel SiC Trench MOSFETs with 370% difference in R_G

Figure 5.29 shows the 2D contour plots for SiC trench MOSFET with 370% variation from time stamp A in Figure 5.28. The cutline represents the turn-off point where the higher R_G device takes all the current as is evident on the current density plot 2D profile in Figure 5.29(a).



(a)



(b)

Figure 5.29 2D contours for parallel SiC Trench MOSFETs with varied R_G (a) Current Density (b) Temperature

- Varying Temperatures

Figure 5.30 to Figure 5.32 demonstrates the impact of a variation in device starting temperatures on current sharing during short circuit operation of SiC Trench MOSFETs. For a difference in temperature of 100% represented in Figure 5.30, the trench devices in parallel share approximately equal current through the duration of the short circuit event. With and increased difference in an R_G (500%) presented in Figure 5.31, the difference in current between the parallel Trench MOSFETs is 13.8%, and the maximum T_J is increased by only 4%. This relatively small increase in temperature is because of the temperature coefficient of the MOSFET short circuit current, which caused the two devices to have the same short circuit duration and have a relatively small difference in short circuit energy (84.3 mJ and 79.1 mJ) despite a large difference in the maximum I_{SC}.

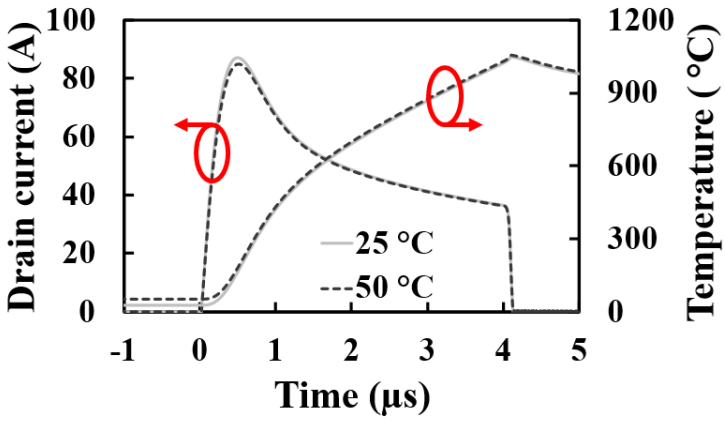
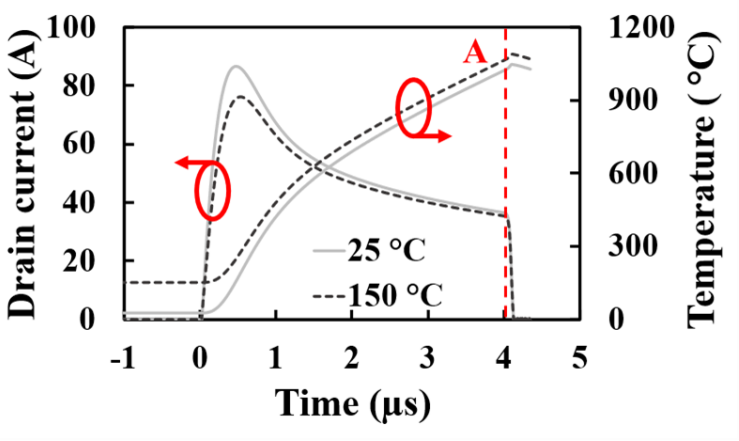


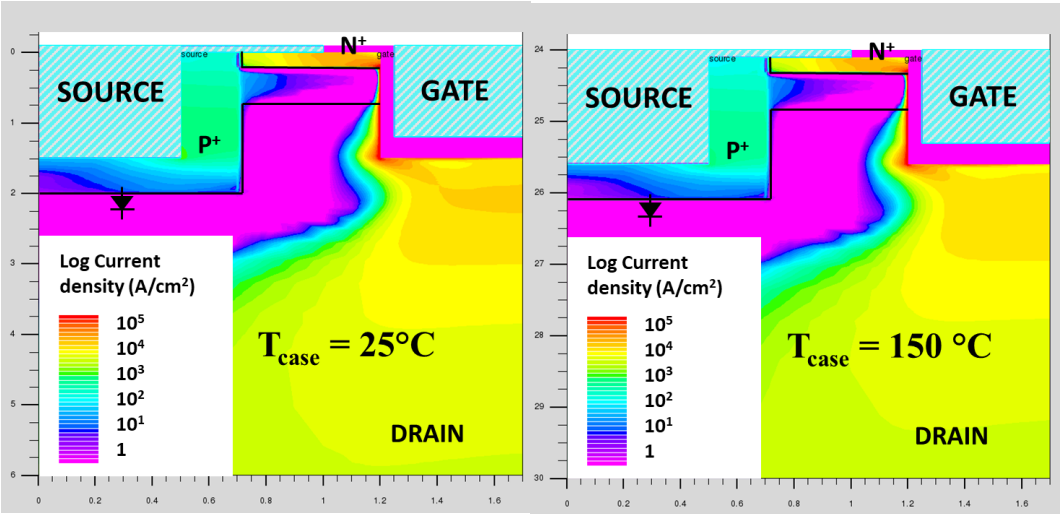
Figure 5.30 (a) Simulated short circuit current and Junction temperature of parallel Trench SiC MOSFETs with 100% case temperature difference.



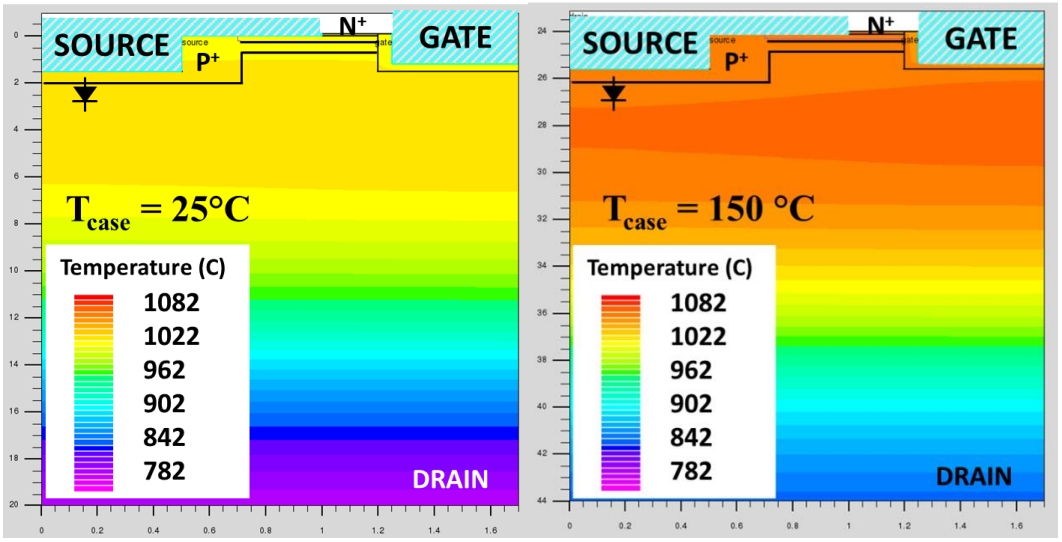
(a)

Figure 5.31 Simulated short circuit current and Junction temperature for parallel SiC Trench MOSFETs with 500% Case temperature difference.

Figure 5.32 is a 2D contour plot of the two devices with 500% variation in R_G extracted at timestamp A from Figure 5.31. It is evident from Figure 5.32(a) that the total current density within the two Trench structures is comparable at turn-off.



(a)

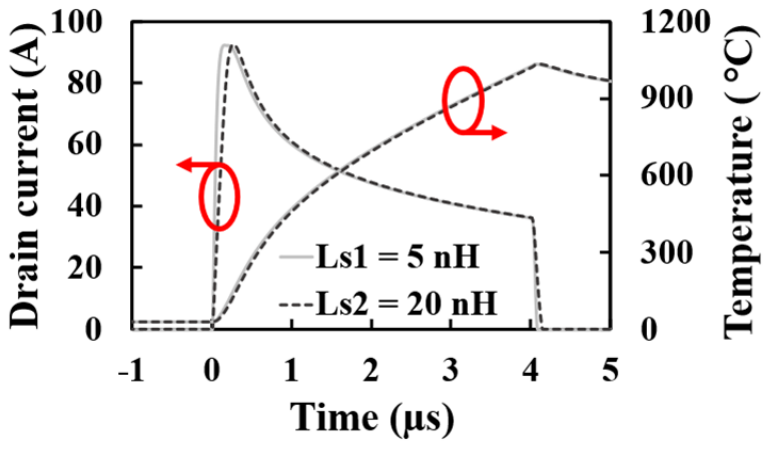


(b)

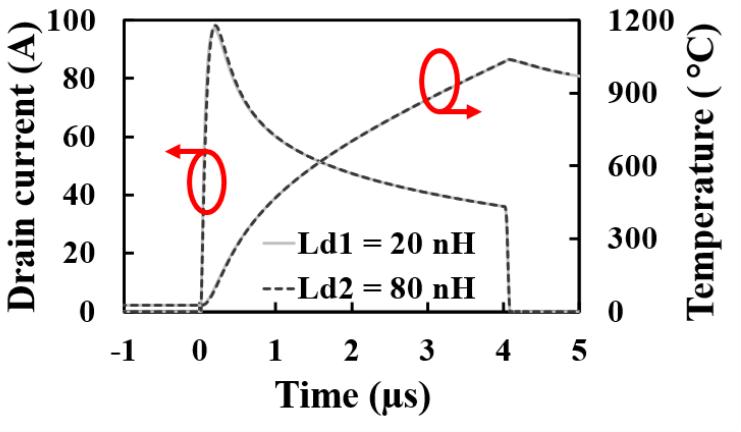
Figure 5.32 2D contours for parallel SiC Trench MOSFETs with varied T_{CASE} (a) Current Density (b) Temperature

- Varying parasitic inductance

Figure 5.33 demonstrates the effects of parasitic inductance variation on current sharing in SiC trench MOSFET. Figure 5.33(a) is for a 400% difference in source inductance, L_s with the maximum short circuit current within the two structures approximately equal (92.24 A and 92.69 A). Also, the two devices have approximately the same short circuit energy with a slight delay at turn-on and turn-off for the 20 nH DUT compared to the 5 nH DUT. This shows that the parasitic source inductance does not affect short circuit energy shared between parallel connected Trench MOSFETs similar with the effects in parallel connected Planar MOSFET (Figure 5.19). The same conclusion can be drawn for a 400% difference in drain inductance L_d seen in Figure 5.33(b) with two almost identical plots that possess minute delay (indistinguishable in the current plots).



(a)



(b)

Figure 5.33 Simulated short circuit current and Junction temperature for parallel SiC Trench MOSFETs with 400% variation in parasitic inductance (a) Source Inductance, L_s (b) Drain Inductance, L_d

5.5. Simulation of short circuit in parallel SiC Cascode JFET

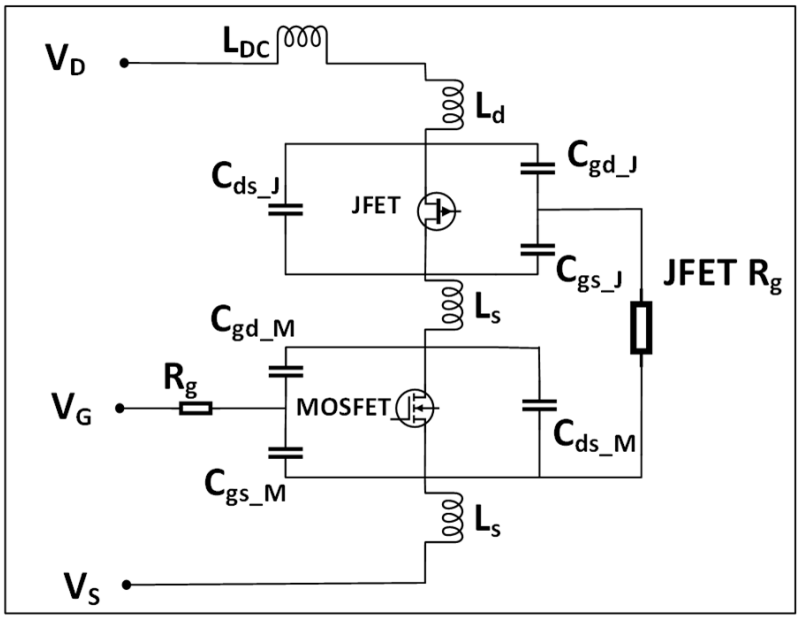


Figure 5.34 Schematic of SiC Cascode JFET with parasitics.

The simulations of current sharing in parallel cascode JFET during short circuit conduction used the circuit in Figure 5.7. Figure 5.34 shows the Cascode structure including the device parasitics. The parameters varied in the previous three sections are replicated to aid benchmarking the performance of the SiC Cascode JFET against the SiC MOSFETs. However, since the cascode JFET is a combination of two devices, and the interconnects between the two devices have been found to be very important for different modes of operation, the JFET R_G is added as an extra parameter to assess. Except stated otherwise, the SiC cascode

structure parameters are the same as previously used in single short circuit simulations (Table 4-5 & Figure 4.25).

- Varying V_{TH}

To vary the impact of V_{TH} spread on current sharing between parallel SiC Cascode JFETs in short circuit, the fixed oxide charge at the Si/SiO_2 interface within the LV MOSFET is utilised. Figure 5.35 shows the simulated current and temperature for this parameter variation, while Figure 5.36(a) and Figure 5.36(b) shows the 2D contours of Current density and temperature respectively at timestamp A from Figure 5.35. The plot of Figure 5.35 shows that the current is shared equally among the two parallel connected devices, with a delayed turn-off and spike in temperature of the lower V_{TH} cascode. It is worth mentioning here that the LV Si MOSFET is a planar structure, and earlier simulations in planar SiC MOSFET suggest Q_F does not affect the maximum current during short circuit. Also, the Si/SiO_2 interface of Si devices are very reliable due to the maturity of the fabrication process.

Analysing the 2D contour plots in Figure 5.36(b) shows that this high temperature is only experienced across the HV SiC JFET, both LV Si MOSFETs had a T_J of 28 C. As explained in the previous chapter, the LV Si MOSFET selection process ensures it takes greater saturation current than the HV SiC JFET, allowing the JFET to set the saturation current, and therefore, the short circuit withstand time[39]. This allows the HV JFET to control the current sharing within parallel connected SiC cascode devices.

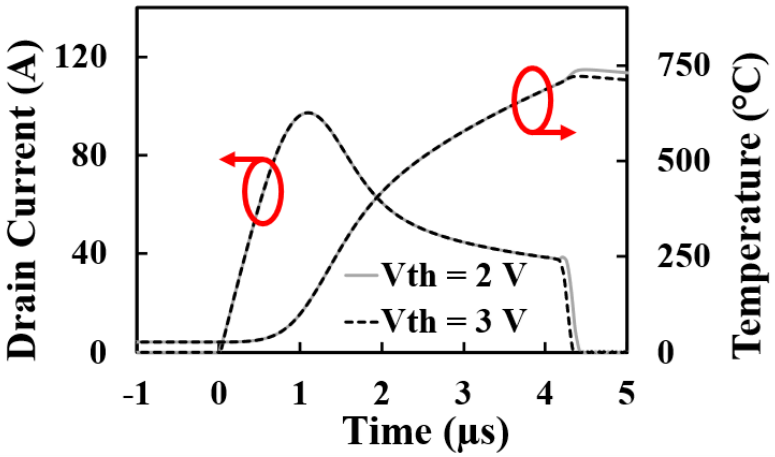
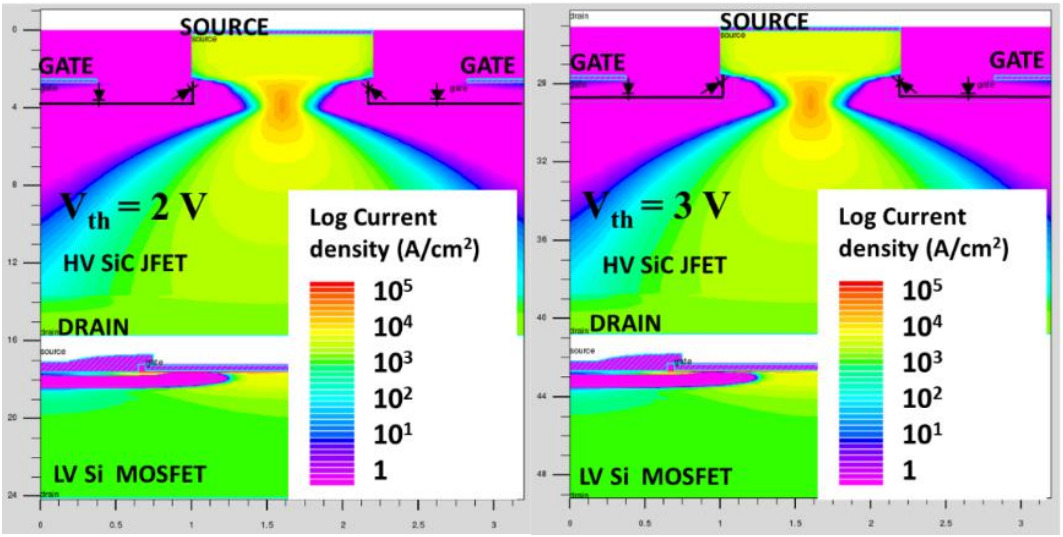
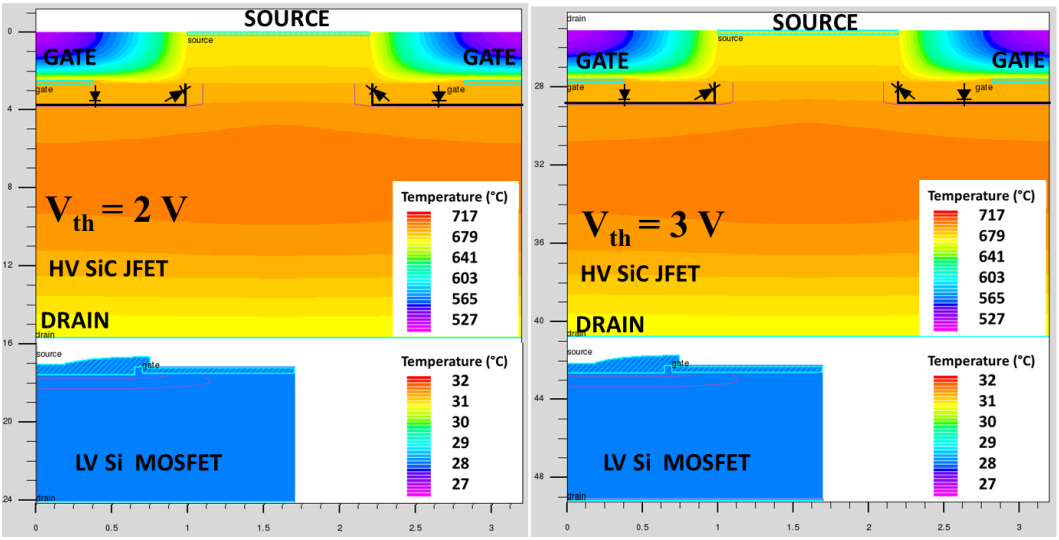


Figure 5.35 Simulated short circuit current and Junction temperature for parallel SiC cascode JFETs with varied V_{TH} (V_{TH} varied through oxide charge of LV MOSFET)



(a)

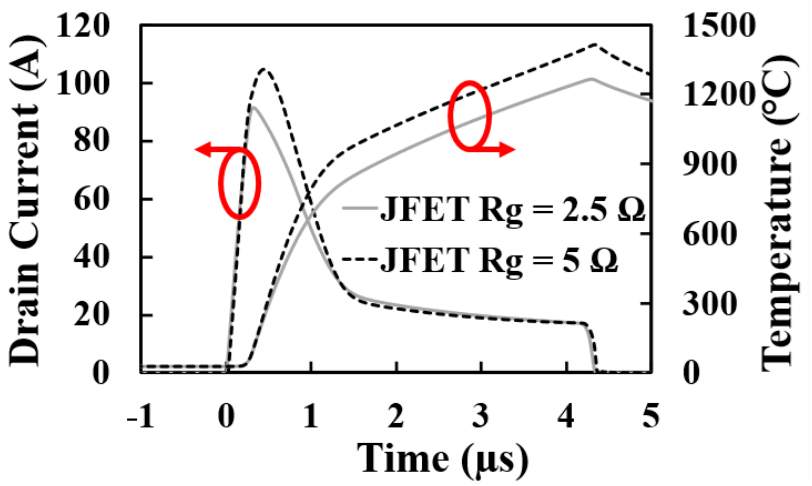


(b)

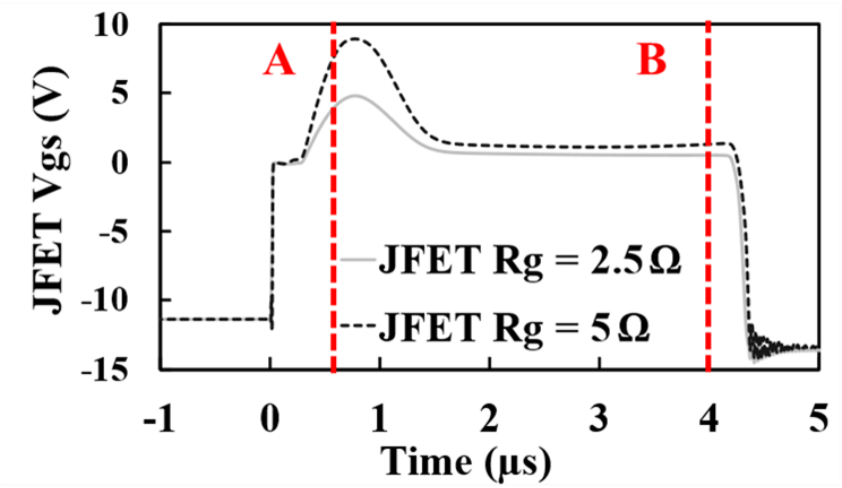
Figure 5.36 2D pots for parallel SiC Cascode JFET with varied V_{TH} (a) Total current density (b) Temperature

- ## Varying JFET Gate Resistance (JFET-R_G)

Figure 5.37 shows the effects of varying JFET-R_G located between the JFET Gate and the MOSFET source (shown in Figure 5.34). Figure 5.37(a) is the short circuit current and temperature of cascode devices in parallel with R_G = 2.5 Ω and R_G = 5 Ω shows, while Figure 5.37(b) shows the JFET gate voltage. 5 Ω is the internal R_G from the SiC JFET datasheet. From the plots, the parallel devices have a 14.16% difference in maximum I_{SC}, and difference of 11.90% in maximum T_J. The cascode with higher JFET-R_G causes a peak JFET gate voltage of approximately 2x higher than the cascode with lower JFET-R_G. This causes a difference in the depletion within the JFET channel and hence the difference in short circuit current shared between the devices.



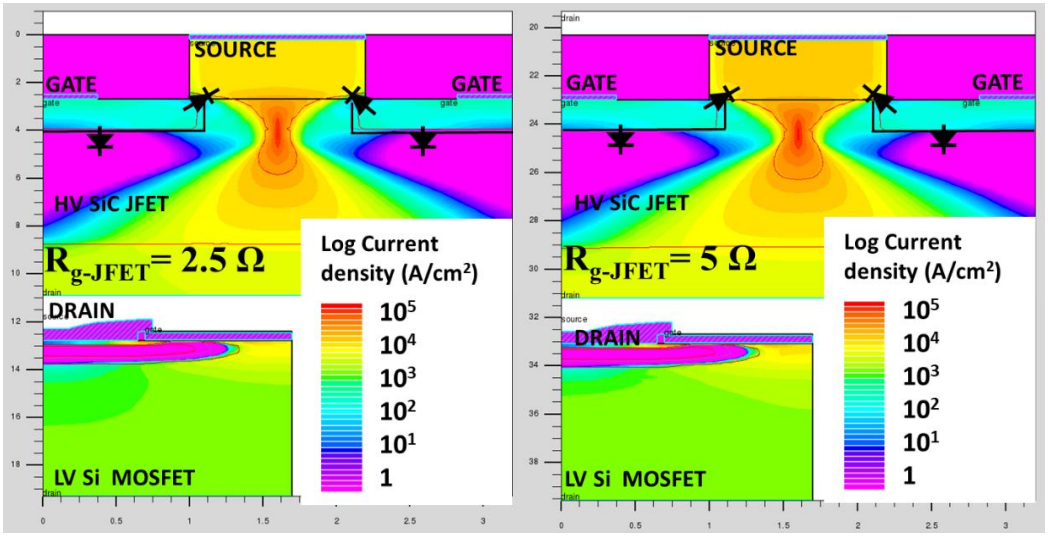
(a)



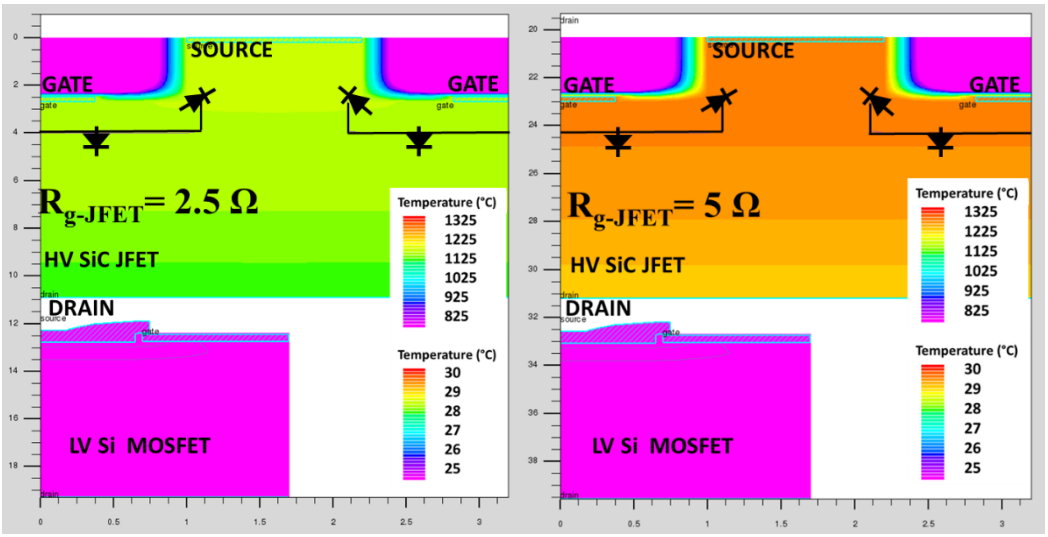
(b)

Figure 5.37 Simulated short circuit current and Junction temperature for parallel 650 V SiC Cascode JFET

Figure 5.38(a) and (b) show the 2D contour plots of total current density and temperature respectively. The current density plots are extracted at timestamp A, and the temperature plots are extracted from timestamp B of Figure 5.37(b). In Figure 5.38(a), the channel opening of the JFET is much wider in the High JFET-R_G structure hence it conducts more current. The temperature plots again show that the LV MOSFET is at a much lower temperature, and the JFET with an R_G = 5 Ω is much hotter with the cell.



(a)



(b)

Figure 5.38 2D contour for parallel 650 V SiC cascode JFETs with difference in JFET R_G (a) Total current density (b) Temperature.

- ## Varying JFET Temperature (T_{CASE})

Figure 5.39 demonstrates the effects of a 100% variation in the starting T_J of two SiC cascode JFETs in parallel on their short circuit current and temperature, while Figure 5.40 shows the 2D contour plots extracted at 4 us timestamp from Figure 5.39. Like the simulations in SiC MOSFET in the previous sections, it is evident from the figure that the short circuit energy of the cascode JFETs in parallel is not affected much by the 100% variation in starting T_J. The DUT have an identical maximum T_J and the same switching time, this shows a negative temperature coefficient of the short circuit current which caused a self-regulated total short circuit energy. The contour plots further help to show that the two structures experience identical short circuit stress during turn-off.

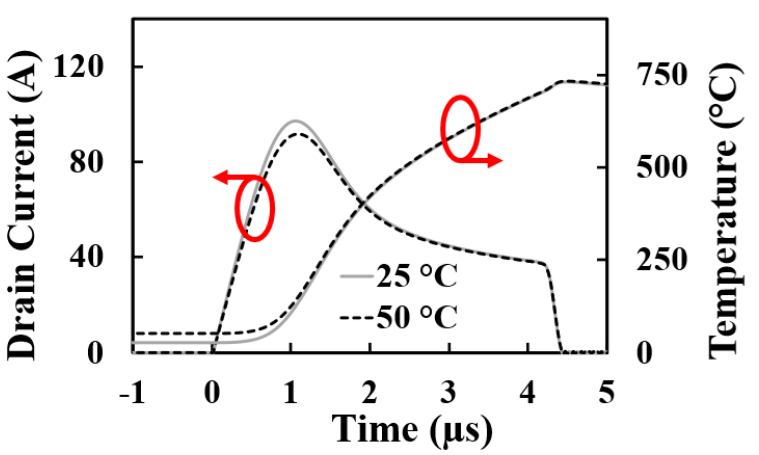
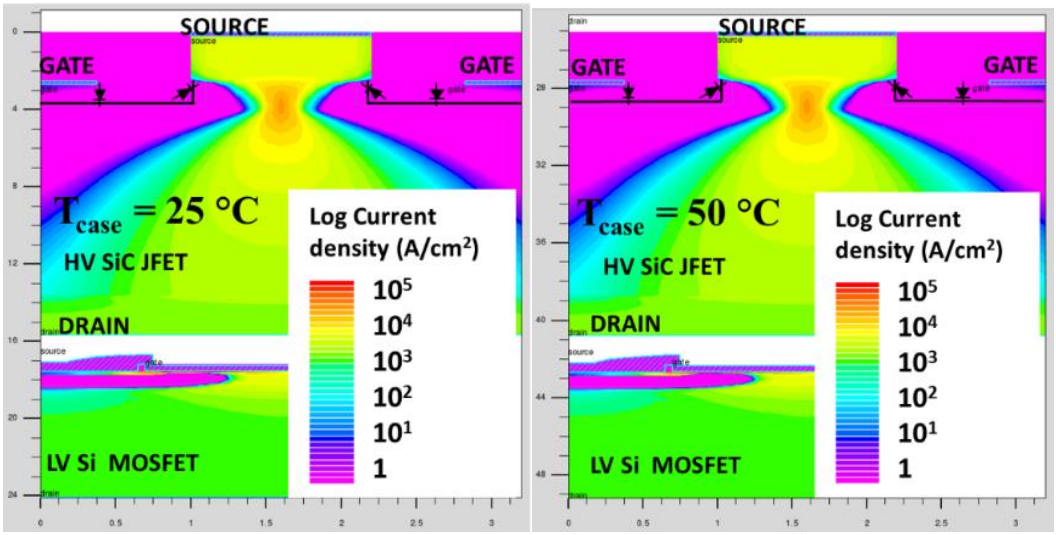
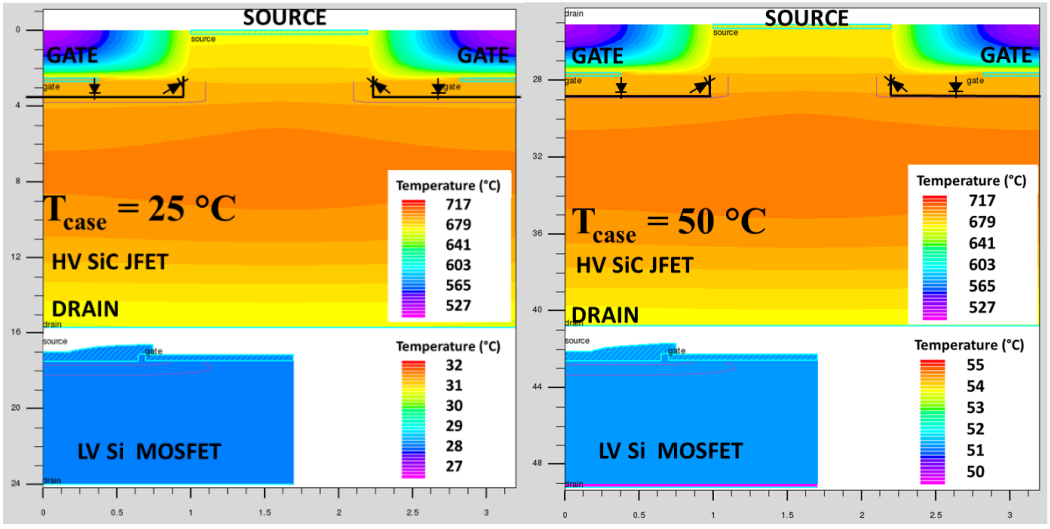


Figure 5.39 Simulated short circuit current and Junction temperature for parallel cascode JFETs with 100% Case temperature difference.



(a)



(b)

Figure 5.40 2D plots for parallel SiC Cascode JFET with 100% varied T_{CASE} (a) Total current density (b) Temperature

The simulation is repeated with a 500% variation in starting T_J and Figure 5.41 demonstrates how the short circuit current and temperature of the two SiC cascode JFETs in parallel are affected, while Figure 5.42 shows the 2D contour plots extracted at 4 us timestamp from Figure 5.41. With a 500% variation in starting T_J, the difference in maximum I_{sc} is 32.10%. While there is a big difference in current shared between the parallel cascode devices, and a larger difference in starting T_J between the two structures, they have approximately the same maximum T_J with only a 2.15% difference. The difference in short circuit energy is 14%. From the contour plots, the temperatures of the two LV Si MOSFETs stay almost the same as the starting T_J (25 and 150 respectively), while the JFET structures have much larger internal temperatures. This indicates that all the short circuit stress is handled by the HV SiC JFETs which ensures that the cascode structure is very robust against the possibility of gate stress on the LV MOSFET unlike the SiC MOSFETs.

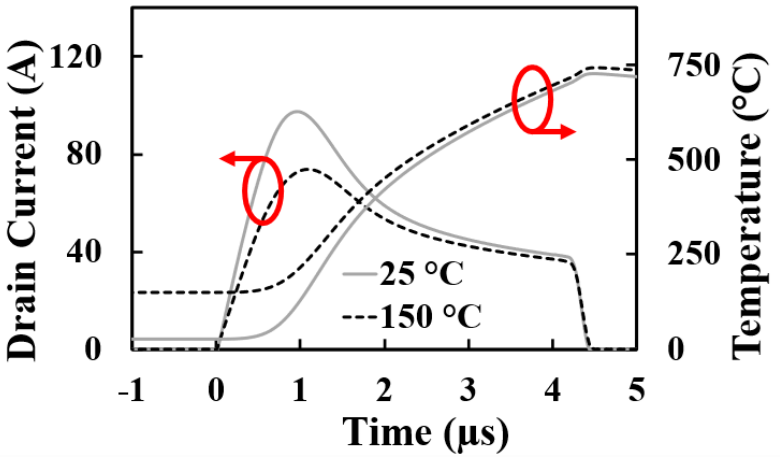
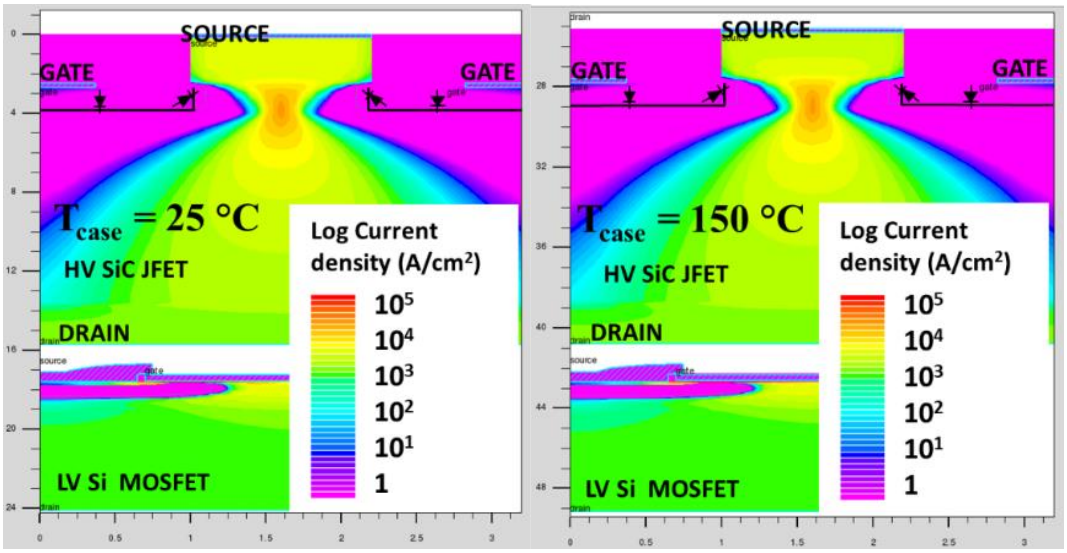
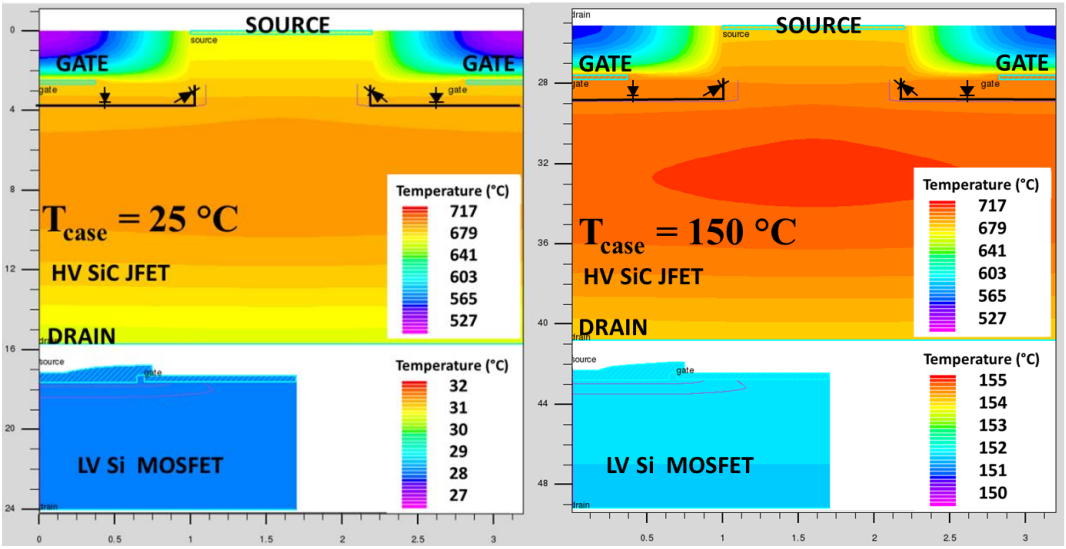


Figure 5.41 Simulated short Circuit current and Junction temperature of parallel cascode JFETs with 500% case temperature difference.



(a)



(b)

Figure 5.42 2D plots for parallel SiC Cascode JFET with 500% varied T_{CASE} (a) Total current density (b) Temperature

5.6. Conclusion

This chapter uses experimental measurements and TCAD simulations to demonstrate the operation of parallel connected SiC cascode JFETs during short circuit conduction. The current sharing between parallel operated devices were studied and quantified. Also, device parameters effects during short circuit operation were studied using their impact on short circuit current and Junction temperature (T_J). Similar parameters were also evaluated through measurements and Simulations in SiC MOSFETs to benchmark the operation of the SiC cascode JFET. The parameters evaluated were Threshold voltage (V_{TH}), DUT Gate resistance (R_G), Starting temperatures (T_{CASE}), Parasitic Inductances (L_d, L_s), and Internal JFET gate resistance, JFET-R_G (cascode only). The V_{TH} variation in experiments were achieved by varying current spread layer (CSL) doping and Fixed oxide charge (Q_F).

The results show that the parameters explored and their effects on current sharing can be split in to three groups,

i) Parameters that affect the maximum short circuit current only. This is the starting T_{CASE}/T_J. This parameter has self-regulating dynamics, ensuring the device with higher temperature takes the least current, and hence the devices in parallel tend towards similar short circuit stress.

ii) Parameters that affect short circuit switching rate only (i.e., turn-off and turn-on). These include the L_s, Q_F (Planar MOSFETs and Cascode), and R_G. These parameters do not affect the current sharing during short circuit operation but can cause a spike in temperature because of the delayed turn-off. With this, the

short circuit stress experienced by one of the parallel devices is higher at turn off. This can lead to uneven degradation over device operation lifetime.

iii) Parameters that affect both switching rate and current sharing. These include CSL doping, Fixed oxide charge (Trench MOSFET only), JFET R_G (Cascode only). With variations in these parameters, the device that conducts the highest short circuit current also has the highest temperature. This is a negative feedback loop that leads to diverging short circuit stress, and one device takes the bulk of the stress.

References

[1] R. Schnell, U. Schlapbach, K. Haas, and G. Debled, "Parallel Operation of LoPak Modules," *Proceedings of the Power Conversion Intelligent Motion Conference, PCIM 2003,* 01/01 2003.

[2] IXYS, "Parallel Operation of IGBT Discrete Devices," ed, 2006.

[3] A. S. L. Semiconductors, "Paralleling of IGBT modules," in *Application Note 5SYA 2098-00*, ed, 2013.

[4] D. Peftitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy, and H.-P. Nee, "Challenges regarding parallel-connection of SiC JFETs," in *8th International Conference on Power Electronics - ECCE Asia*, 2011-05-01 2011: IEEE, doi: 10.1109/icpe.2011.5944660.

[5] J. Fabre and P. Ladoux, "Parallel Connection of 1200 V/100 A SiC MOSFET Half-bridge Modules," *IEEE Transactions on Industry Applications,* pp. 1-1, 2015-01-01 2015, doi: 10.1109/tia.2015.2496109.

[6] J. Colmenares, D. Peftitsis, J. Rabkowski, D.-P. Sadik, G. Tolstoy, and H.-P. Nee, "High-Efficiency 312-kVA Three-Phase Inverter Using Parallel Connection of Silicon Carbide MOSFET Power Modules," *IEEE Transactions on Industry Applications,* vol. 51, no. 6, pp. 4664-4676, 2015-11-01 2015, doi: 10.1109/tia.2015.2456422.

[7] R. Wang, J. Sabate, F. Tao, F. Xu, X. Liu, and C. Li, "H-bridge building block with SiC power MOSFETs for pulsed power applications," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016-09-01 2016: IEEE, doi: 10.1109/ecce.2016.7855143.

[8] R. Wu *et al.*, "Measurement and simulation of short circuit current sharing under parallel connection: SiC MOSFETs and SiC Cascode JFETs," *Microelectronics Reliability,* p. 114271, 2021-10-01 2021, doi: 10.1016/j.microrel.2021.114271.

[9] S. Musumeci, R. Pagano, A. Raciti, F. Frisina, and M. Melito, "Parallel strings of IGBTs in short circuit transients: analysis of the parameter influence and experimental behavior," in *IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02*: IEEE, doi: 10.1109/iecon.2002.1187568.

[10] P. R. Palmer, H. S. Rajamani, and J. C. Joyce, "Behaviour of IGBT modules under short circuit conditions," in *Conference Record of the 2000 IEEE Industry Applications Conference. Thirty-Fifth IAS Annual Meeting and World Conference on Industrial Applications of Electrical Energy (Cat. No.00CH37129)*: IEEE, doi: 10.1109/ias.2000.882594.

[11] N. Chen, F. Chimento, M. Nawaz, and L. Wang, "Dynamic characterization of parallel-connected high-power IGBT modules," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013-09-01 2013: IEEE, doi: 10.1109/ecce.2013.6647270.

[12] M. Spang and G. Katzenberger, "Current sharing between parallel IGBTs in power modules during short circuit with unsymmetrically connected load," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016-09-01 2016: IEEE, doi: 10.1109/epe.2016.7695365.

[13] R. Wu, P. Diaz Reigosa, F. Iannuzzo, H. Wang, and F. Blaabjerg, "A comprehensive investigation on the short circuit performance of MW-level IGBT power modules," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015-09-01 2015: IEEE, doi: 10.1109/epe.2015.7311761.

[14] E. W. B. M.J. Barnes, "Analysis of high power IGBT short circuit failures," in *Conference Record of the Twenty-Sixth International Power Modulator Symposium, 2004 and 2004 High-Voltage Workshop.*: IEEE, doi: 10.1109/modsym.2004.1433603.

[15] R. Azar, R. Udrea, W. T. Ng, F. Dawson, W. Findlay, and P. Waind, "The Current Sharing Optimization of Paralleled IGBTs in a Power Module Tile Using a PSpice Frequency Dependent Impedance Model," *IEEE Transactions on Power Electronics,* vol. 23, no. 1, pp. 206-217, 2008-01-01 2008, doi: 10.1109/tpel.2007.909182.

[16] R. Wu, L. Smirnova, H. Wang, F. Iannuzzo, and F. Blaabjerg, "Comprehensive investigation on current imbalance among parallel chips inside MW-scale IGBT power modules," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015-06-01 2015: IEEE, doi: 10.1109/icpe.2015.7167881.

[17] R. Perez-Delgado, G. Velasco-Quesada, and M. Roman-Lumbreras, "Current Sharing Control Strategy for IGBTs Connected in Parallel," *Journal of Power Electronics,* vol. 16, no. 2, pp. 769-777, 2016-03-20 2016, doi: 10.6113/jpe.2016.16.2.769.

[18] D. Peftitsis *et al.*, "High-power modular multilevel converters with SiC JFETs," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010-09-01 2010: IEEE, doi: 10.1109/ecce.2010.5618274.

[19] M. Chinthavali, P. Ning, Y. Cui, and L. M. Tolbert, "Investigation on the parallel operation of discrete SiC BJTs and JFETs," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011-03-01 2011: IEEE, doi: 10.1109/apec.2011.5744728.

[20] J. D. Scofield, J. N. Merrett, J. Richmond, A. K. Agarwal, and S. Leslie, "Electrical and Thermal Performance of 1200 V, 100 A, 200°C 4H-SiC MOSFET-Based Power Switch Modules," *Materials Science Forum,* vol. 645-648, pp. 1119-1122, 2010, doi: 10.4028/www.scientific.net/MSF.645-648.1119.

[21] J. D. Scofield, J. N. Merrett, J. Richmond, A. Agarwal, and S. Leslie, "Performance and Reliability Characteristics of 1200 V, 100 A, 200°C Half-Bridge SiC MOSFET-JBS Diode Power Modules," *Additional Conferences (Device Packaging, HiTEC, HiTEN, and CICMT),* vol. 2010, no. HITEC, pp. 000289-000296, 2010-01-01 2010, doi: 10.4071/hitec-jscofield-wp22.

[22] M. J. Palmer, R. W. Johnson, T. Autry, R. Aguirre, V. Lee, and J. D. Scofield, "Silicon Carbide Power Modules for High-Temperature Applications," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 2, no. 2, pp. 208-216, 2012-02-01 2012, doi: 10.1109/tcpmt.2011.2171343.

[23] Z. Chen *et al.*, "Development of a 1200 V, 120 A SiC MOSFET module for high-temperature and high-frequency applications," in *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2013-10-01 2013: IEEE, doi: 10.1109/wipda.2013.6695561.

[24] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2307-2320, 2014-05-01 2014, doi: 10.1109/tpel.2013.2283245.

[25] S. Hazra, S. Madhusoodhanan, S. Bhattacharya, G. K. Moghaddam, and K. Hatua, "Design considerations and performance evaluation of 1200 V, 100 a SiC MOSFET based converter for high power density application," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013-09-01 2013: IEEE, doi: 10.1109/ecce.2013.6647272.

[26] C.-K. Liu *et al.*, "Development of packaging technologies for SiC power module," in *2015 10th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2015-10-01 2015: IEEE, doi: 10.1109/impact.2015.7365232.

[27] P. D. Reigosa, F. Iannuzzo, H. Luo, and F. Blaabjerg, "A Short-Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules," *IEEE Transactions on*

Industry Applications, vol. 53, no. 3, pp. 2880-2887, 2017, doi: 10.1109/TIA.2016.2628895.

[28] A. Kadavelugu, E. Aeloiza, and C. Belcastro, "Short-circuit performance of multi-chip SiC MOSFET modules," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017-10-01 2017: IEEE, doi: 10.1109/wipda.2017.8170561.

[29] L. Ceccarelli, P. Diaz Reigosa, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "Compact electro-thermal modeling of a SiC MOSFET power module under short-circuit conditions," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017-10-01 2017: IEEE, doi: 10.1109/iecon.2017.8216842.

[30] A. Castellazzi, A. Fayyaz, and R. Kraus, "SiC MOSFET Device Parameter Spread and Ruggedness of Parallel Multichip Structures," *Materials Science Forum,* vol. 924, pp. 811-817, 2018, doi: 10.4028/www.scientific.net/MSF.924.811.

[31] D. H. Lu, H. Takubo, S. Takano, and Y. Suzuki, "Paralleling six 320A 1200V All-SiC Half-bridge Modules for a Large Capacity Power Stack," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018-05-01 2018: IEEE, doi: 10.23919/ipec.2018.8507687.

[32] F. Boige, A. Fayyaz, A. Castellazzi, F. Richardeau, and S. Vinnac, "Short-circuit robustness of parallel SiC MOSFETs and fail-safe mode strategy," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019-09-01 2019: IEEE, doi: 10.23919/epe.2019.8914891.

[33] Q. Zou, J. Ke, J. Peng, and Z. Zhao, "Effect of Parasitic Inductance Mismatch on Short-Circuit Characterization of Paralleled SiC MOSFETs," in *2019 4th IEEE Workshop on the Electronic Grid (eGRID)*, 2019-11-01 2019: IEEE, doi: 10.1109/egrid48402.2019.9092772.

[34] J. Ke, Z. Zhao, Q. Zou, J. Peng, Z. Chen, and X. Cui, "Device Screening Strategy for Balancing Short-Circuit Behavior of Paralleling Silicon Carbide MOSFETs," *IEEE Transactions on Device and Materials Reliability,* vol. 19, no. 4, pp. 757-765, 2019-12-01 2019, doi: 10.1109/tdmr.2019.2949449.

[35] R. Wu, S. Mendy, N. Agbo, J. O. Gonzalez, S. Jahdi, and O. Alatise, "Performance of Parallel Connected SiC MOSFETs under Short Circuits Conditions," *Energies,* vol. 14, no. 20, p. 6834, 2021-10-19 2021, doi: 10.3390/en14206834.

[36] R. Wu, S. Mendy, J. O. Gonzalez, S. Jahdi, and O. Alatise, "Current Sharing of Parallel SiC MOSFETs under Short Circuit Conditions," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021-09-06 2021: IEEE, doi: 10.23919/epe21ecceeurope50061.2021.9570690.

[37] R. Nakamura, Y. Nakano, M. Aketa, K. Noriaki, and K. Ino, "1200V 4H-SiC Trench Devices," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 20-22 May 2014 2014, pp. 1-7.

[38] T. Nakamura *et al.*, "High performance SiC trench devices with ultra-low ron," in *2011 International Electron Devices Meeting*, 2011-12-01 2011: IEEE, doi: 10.1109/iedm.2011.6131619.

[39] A. Bhalla, J. Bendel, and X. Li, "Robustness of SiC JFETs and Cascodes United Silicon Carbide supplies a," 2016.

Chapter 6. CONCLUSION AND FUTURE WORK

6.1. Conclusions

The research presented in this thesis focused on the methodical evaluation of SiC cascode JFET robustness. With all the device advantage itemised previously including avoiding the issue associated with operating SiC MOSFTs (i.e., the SiC/SiO_2 interface), standalone JFET (i.e., operating in depletion mode), and Si devices (i.e., material constraints), analysing the robustness is hence very important to fully maximise these advantages. Also crucial was benchmarking the robustness performance against other key technologies.

The studies required building a comprehensive FEA model which helped to explain the effects of various parameters on robustness and reliability. The model proved very useful because of its flexibility in accessing the various current paths within the device which was especially useful for the TO-247 packaged SiC cascode JFET analysed in this thesis. This model can also be extended to any possible packages necessary while demonstrating a good compromise between simulation time and accuracy.

From the Simulation and experimental results one major conclusion is the importance of properly optimising the JFET gate path within the cascode structure. While under avalanche stress and Short circuit stress, which are analysed in chapters 3 and 4 respectively, the gate path of the SiC cascode JFET was a key failure path. In the case of avalanche, the gate path experiences a soft failure initially while displaying an uncharacteristic behaviour comprised of a slow dv/dt, dip in the drain voltage, a change in the drain current slope, and an elongated avalanche time. The device eventually experiences catastrophic failure; however, this depends on the frequency of the pulses. More frequent pulses (repetitive UIS) cause a much-reduced avalanche robustness relative to SiC MOSFET technologies. In the case of short circuit robustness, the effects of the gate path are again evident as the SiC cascode JFET always fails with Drain-Source short circuit while the gate-source junction is still operational. On further analysis using FEA simulation, it is demonstrated that the failure current from cascode drain to source flows through the JFET gate path highlighting its importance.

Another Key take away is that the SiC cascode avalanche robustness was demonstrated to be very temperature dependent, while the performance under short circuit pulses was temperature independent.

This work has demonstrated the robustness of the SiC cascode JFET. It also demonstrates the weaknesses of the JFET in relation to the other key technologies. The standard device package can be further optimised accounting for the obvious failure points exhibited in this thesis.

6.2. Future work

Future work on SiC Cascode JFET robustness have been split into the following sections.

- Structures

This SiC Cascode JFET investigated in this work focused on a simple SiC vertical JFET structure comprising of a uniform doping profile in the JFET channel and drift region. Future research into JFET structures and their impact on robustness can be explored.

One such structure variation is a JFET structure with separate doping profiles for channel and drift region. Another key structure variation to the JFET is the inclusion of side P doped walls in the channel. This is predicted to affect the depletion profiles, capacitance, current density, etc, of the JFET and consequently the operation of the cascode. Hence, studying these variations would improve the knowledge of SiC cascode JFET robustness and their dependence on the JFET structures.

Another structure that requires more investigation into its robustness specifically short circuit robustness is the GaN HEMT cascode.

- Multi-device packages

The avalanche robustness in the SiC Cascode JFET studied in this work for both single pulse and repetitive avalanche were solely for single devices. In the analyses of Shor Circuit, all investigations on parallel devices were limited to 2 parallel devices. Future investigations exploring the robustness performance of multi-device packages will help improve the implementation and deployment of semiconductor modules.

- Harsh environments

Because of the advantages of SiC devices, they have also seen increased adoption in applications such as space, aviation electronics, and high-energy accelerators. These applications present a different type of robustness challenge from those assessed in this work. This can include operations in sub-zero temperatures and temperatures much higher than the scope accessed in this work (25° C-150° C), as well as exposure to radiation and different failure mechanisms. Hence exploring the robustness of SiC cascode JFETs in these conditions will be a useful area for future research.

APPENDIX A TCAD script

APPENDIX A1. High Voltage JFET structure

```
## High Voltage JFET structure

set ver= Jfet
set temp = 300

go Atlas

mesh outf=$ver.str # Save structure

## Mesh
# X mesh
x.mesh loc=0.0 spac=0.2
x.mesh loc=1.0 spac=0.1
x.mesh loc=1.6 spac=0.3
x.mesh loc=2.2 spac=0.1
x.mesh loc=3.2 spac=0.2
# Y mesh
y.mesh loc=0.0 spac=0.1
y.mesh loc=0.9 spac=0.1
y.mesh loc=1.0 spac=0.7
y.mesh loc=2.5 spac=0.1
y.mesh loc=4.1 spac=0.1
y.mesh loc=5 spac=1.0
y.mesh loc=9 spac=0.1
y.mesh loc=11 spac=1.0

## Material and Region Definition
region num=1 material=4H-SiC x.min=1.0 x.max=2.2 y.min=0 y.max=2.7
region num=2 material=4H-SiC x.min=0 x.max=3.2 y.min=2.7 y.max=15.7
region num=3 material=air x.min=0 x.max=1.0 y.min=0 y.max=2.7
region num=4 material=air x.min=2.2 x.max=3.2 y.min=0 y.max=2.7

## Contacts
# 1- Source; 2- Drain; 3-Gate
electrode name=source x.min=1.0 x.max=2.2 y.min=0 y.max=0.2
electrode bottom name=drain
electrode name=gate x.min=0 x.max=0.4 y.min=2.5 y.max=2.7
electrode name=gate x.min=2.8 x.max=3.2 y.min=2.5 y.max=2.7

## Impurity profile
# Source doping
doping region=1 uniform conc=2.33e16 n.type
doping region=1 uniform conc=1.0e19 n.type x.min=1.0 x.max=2.2
y.min=0.2 y.max=0.7
# channel doping
doping region=2 uniform conc=2.33e16 n.type y.min=2.7 y.max=4
# Drift Layer doping
doping region=2 uniform conc=2.33e16 n.type x.min=0 x.max=3.2 y.min=4
# Left & Right gate doping
doping region=2 uniform conc=1.0e19 p.type x.max=1.0 y.min=2.7 y.max=4
doping region=2 uniform conc=1.0e19 p.type x.min=2.2 y.min=2.7 y.max=4
# Substrate doping
doping region=2 uniform conc=5.0e18 n.type x.min=0 x.max=3.2 y.min=9
y.max=11
```

```
# Plot structure
tonyplot $ver.str

## TRANSFER Characteristics
go atlas

# Input structure file
mesh infile = $ver.str width=8e5

# Set models
models BGN cvt srh Analytic fldmob Auger temperature=$temp print
MATERIAL mat=4H-SiC ni.min=5e4
mobility altcvt.n ^alt.sr.n
mobility n.lcrit =1.0e-6 p.lcrit=1.0e-6


# Set contact workfunction
contact name=gate

# method statement
method newton maxtrap=20

# structure outputs
output e.mob h.mob con.band val.band qss

# Begin solution
solve init
solve previous
solve vdrain=0.05
solve vdrain=0.1
solve vdrain=1.0
solve vstep=1 vfinal=5 name=drain

# Ramp gate and log results
log outf = $"ver"Vth.log
solve vgate=-20
solve vgate=-20 vstep=0.2 vfinal=0 name=gate

# Extract JFET Pinch-off value from log plot
extract init infile = "$"ver"Vth.log"
extract   name="vt"   x.val   from   curve(v."gate",i."drain")   where
y.val=20e-3


# Save final structure results
save outf = $"ver"Vth.str
tonyplot $"ver"Vth.log


## Static Breakdown Characteristics
go atlas simflag="-160 -P 16"

# Input structure file
mesh infile = $"ver".str width=8e5

# Set contact work function gate electrode
contact name=gate workf=4.3

# Model statements
material material=4H-SiC ni.min=5e4
```

```
models BGN cvt srh Analytic fldmob Auger temperature=$temp print
#
# Impact ionization models
impact device=af selb AN1=2.78E6 AN2=2.78E6 BN1=1.05E7 BN2=1.05E7
AP1=3.51E6 AP2=3.51E6 BP1=1.03E7 BP2=1.03E7 BETAN=1.37 BETAP=1.09
#
# method statement
method newton maxtrap=10
# Find initial solution and fix JFET gate to negative voltage
solve vgate=-20

save outf = $"ver"_Vbr.str
log outf = $"ver"_Vbr.log

solve vdrain=0.025
solve vdrain=0.05
solve vdrain=0.1
solve vdrain=0.5
solve vstep=1 vfinal=5 name=drain
save outf = $"ver"_Vbr5.str
#
solve vstep=5 vfinal=100 name=drain
save outf = $"ver"_Vbr100.str
#
solve vstep=10 vfinal=500 name=drain
save outf = $"ver"_Vbr500.str
#
solve vstep=50 vfinal=1200 name=drain compl=1e-3 cname=drain
save outf = $"ver"_Vbr1200.str
#
log off

# Extract JFET breakdown voltage
extract init infile = "$"ver"_Vbr.log"
extract name="bv" max(v."drain")
extract name="NVbd" x.val from curve(abs(v."drain"),abs(i."drain"))
where y.val=1.0e-3

# Plots
tonyplot $"ver"_Vbr1200.str
tonyplot $"ver"_Vbr.log

quit
```

APPENDIX A2. Low Voltage MOSFET structure

```
## Low Voltage MOSFET structure

# (c) Silvaco Inc., 2021
# This example is based on the reference:
#
# K.Shenai, C.Cavallaro, S.Musumeci, R. Pagano, A.Raciti
# "Modeling Low-Voltage Power MOSFETs as Synchronous rectifiers in
Buck Converter
# Applications", Industry Applications Conference, 2003. 38th IAS
Annual Meeting
# pp. 1794- 1801 vol.3.
```

```
go athena

## Mesh
# X mesh
line x location=0
line x location=0.65 spacing=0.01
line x location=0.7  spacing=0.01
line x location=0.75 spacing=0.01
line x location=1    spacing=0.02
line x location=1.7
# Y mesh
line y location=3.5 spacing=0.2
line y location=6.5 spacing=1

init silicon phosphor resistivity=0.001 orientation=100

epitaxy time=240 temp=1000 thickness=1.75 divisions=8 dy=0.2 ydy=1.75
\
        c.phosphor=2.7e16
epitaxy time=240 temp=1000 thickness=1.75 divisions=15 dy=0.001 ydy=0
\
        c.phosphor=2.7e16
deposit oxide thick=0.0235 divisions=5 dy=0.001 ydy=0.0235
deposit oxide thick=0.0235 divisions=5 dy=0.001 ydy=0
deposit polysilicon thick=0.15 divisions=5 dy=0.001 ydy=0.15
deposit polysilicon thick=0.15 divisions=8 dy=0.001 ydy=0
deposit barrier thick=1 divisions=5 dy=0.001 ydy=0.15
deposit barrier thick=1 divisions=8 dy=0.001 ydy=0
etch barrier left p1.x=0.7
etch polysilicon left p1.x=0.7
implant boron dose=1.8e14 energy=120 s.oxide=0.047
etch barrier all
implant arsenic dose=1e15 energy=80 s.oxide=0.047
deposit oxide thick=0.025 divisions=5 dy=0.001 ydy=0.025
deposit oxide thick=0.025 divisions=5 dy=0.001 ydy=0
diffus time=60 temp=1000 nitro
etch oxide left p1.x=0.65
deposit aluminum thick=0.25 divisions=5 dy=0.001 ydy=0.047
deposit aluminum thick=0.25 divisions=5 dy=0.001 ydy=0
etch aluminum right p1.x=0.75
electrode name=source x=0.4
electrode name=gate x=1
electrode name=drain bottom
struct outfile=LVmos_0.str

tonyplot LVmos_0.str

# remesh before Device simulation

go devedit

init inf=LVmos_0.str

# Set Meshing Parameters

base.mesh height=0.2 width=0.2
bound.cond    !apply    max.slope=28    max.ratio=300    rnd.unit=0.001
line.straightening=1 align.points when=automatic

imp.refine imp="Net Doping" scale=log
imp.refine min.spacing=0.02
```

```
constr.mesh max.angle=90 max.ratio=300 max.height=10000 \
        max.width=10000 min.height=0.0001 min.width=0.0001

constr.mesh type=Semiconductor default
constr.mesh type=Insulator default
constr.mesh type=Metal default
constr.mesh type=Other default

constr.mesh region=2 default max.height=0.01
constr.mesh id=1 x1=0.8 y1=0 x2=1.1 y2=0.2 default max.height=0.02
Mesh Mode=MeshBuild

structure outf=LVmos_1.str

set ver = "LVmos"
set temp = 300
set qf = "5e11"


## TRANSFER XTICS
go atlas

# Input file
mesh infile= $"ver"_1.str width=2e6

# Model statement
models cvt consrh fermi temperature=$temp print

# interface traps
INTERFACE device=amos QF=$"qf" Y.MAX=0.4

# method statement
method newton

# Set gate contact work function
contact name=gate workf=4.37

#
output e.mob h.mob con.band val.band qss

# Begin solution
solve init
solve previous
solve vdrain=0.05
solve vdrain=0.1
solve vdrain=1.0
solve vstep=1 vfinal=20 name=drain
#
log outf = $"ver"Vth_qf$"qf1".log
#
# Ramp gate and log results
solve vgate=0.2
solve vgate=0 vstep=0.2 vfinal=20 name=gate

#extract
extract init infile = "$"ver"Vth_qf$"qf1".log"
extract                                                    name="vt"
(xintercept(maxslope(curve((v."gate"),(i."drain")))))

save outf = $"ver"Vth_qf$"qf1".str
```

```
## BREAKDOWN XTICS
go atlas

# Input file
mesh infile = $"ver"_1.str width=2e6

# interface traps
INTERFACE device=amos QF=$"qf" Y.MAX=0.4

# Set gate contact workfunction
contact name=gate workf=4.37

# Model statement
models cvt consrh fermi temperature=$temp print

# Impact ionization models
IMPACT SELB

# Method statement
method newton

solve init

save outf = $"ver"_Vbr.str
log outf = $"ver"_Vbr.log

solve vdrain=0.025
solve vdrain=0.05
solve vdrain=0.1
solve vdrain=0.5
solve vstep=1 vfinal=5 name=drain
save outf = $"ver"_Vbr5.str

solve vstep=5 vfinal=100 name=drain compl=1e-6 cname=drain
save outf = $"ver"_Vbr100.str


tonyplot $"ver"_Vbr100.str
tonyplot $"ver"_Vbr.log

quit
```

APPENDIX A3. Cascode JFET Double Pulse test

```
## Cascode JFET Double Pulse test

set pulse="55us"
set period="75us"
set Rg = 68             # Cascode Gate resistance
set re1=10              # JFET Gate resistance
set lg=10               # JFET Parasitic Gate Inductance
set ls=5                # Cascode Parasitic Source Inductance
set ld=80               # Cascode Parasitic Drain Inductance
set Te=300              # Case Temperature
set Vgs = 15            # Gate Voltage
#set alph = "100"       # Heat conductance
set struc = "Jfet"

# Structure input file set to the correct directory (DIR)
```

```
set infile1 = "/..DIR../$"struc".str"
set infile2 = "/..DIR../LVmos_1.str"

# DC solution
go atlas

.begin
.model dmod1 d(level=1 IS=18.8p RS=0 BV=650 CJO=460p M=0.333 N=2.0)
vin 4 0 0
d1   2 3 dmod1
af 6=drain 8=gate 10=source infile=$"infile1" width=8e5
am 5=drain 1=gate 7=source infile=$"infile2" width=2e6
L1 2 3 2.2mH
r1 4 1 $"Rg"
r2 8 9 $"re1"
Lg 9 7 $"lg"nH
Lj 10 5 10nH
Ld 6 2 $"ld"nH
Ls 0 7 $"ls"nH
vdd 3 0 0
Cdd 3 0 4.7mF
.nodeset v(1)=0 v(3)=0 v(2)=0 v(4)=0 v(5)=0 v(6)=0
.dc vdd 0 400 5
.numeric vchange=1 toldc=1e-6 imaxdc=800
.save
outfile=$"struc"_$"re1"DPT_R$"Rg"_V$"Vgs"_$"ld"_$"ls"_$"lg"_save
.end
#
contact device=am name=gate workf=4.37
#
models device=af cvt bgn srh Analytic fldmob Auger print
models device=am cvt consrh fermi print

go atlas


# Transient Solution
go atlas

.begin
.model dmod1 d(level=1 IS=18.8p RS=0 BV=650 CJO=460p M=0.333 N=2.0)
vin 4 0 pulse 0 $"Vgs" 1us 0.01us 0.01us $"pulse" $"period"
d1   2 3 dmod1
af 6=drain 8=gate 10=source infile=$"infile1" width=8e5
am 5=drain 1=gate 7=source infile=$"infile2" width=2e6
L1 2 3 2.2mH
r1 4 1 $"Rg"
r2 8 9 $"re1"
Lg 9 7 $"lg"nH
Lj 10 5 10nH
Ld 6 2 $"ld"nH
Ls 0 7 $"ls"nH
vdd 3 0 400
Cdd 3 0 4.7mF
.nodeset v(1)=0 v(4)=0 v(3)=400
.numeric lte=0.01 dtmin=0.0001ps dtmax=1us
.load
infile=$"struc"_$"re1"DPT_R$"Rg"_V$"Vgs"_$"ld"_$"ls"_$"lg"_save
.log outfile=$"struc"_$"re1"DPT_R$"Rg"_V$"Vgs"_$"ld"_$"ls"_$"lg"
.save      master=$"struc"_$"re1"DPT_R$"Rg"_V$"Vgs"_$"ld"_$"ls"_$"lg"
tsave= 26us,28us,32us
```

```
.tran 1ns 150us
.end

# Structure outputs
OUTPUT E.MOBILITY H.MOBILITY con.band val.band

# Set work function for gate electrode
contact device=am name=gate workf=4.37

# Model statements
models device=af cvt srh Analytic fldmob Auger print
models device=am cvt consrh fermi print
#
method newton maxtrap=30

# Impact ionization models
impact  device=af  selb  AN1=2.78E6  AN2=2.78E6  BN1=1.05E7  BN2=1.05E7
AP1=3.51E6 AP2=3.51E6 BP1=1.03E7 BP2=1.03E7 BETAN=1.37 BETAP=1.09
impact device=am selb an2=7.03e05*1.25

go atlas

# Plot log results
tonyplot $"struc"_$"re1"DPT_R$"Rg"_V$"Vgs"_$"ld"_$"ls"_$"lg"_tr.log

quit
```

APPENDIX A4. Cascode JFET UIS

```
## Cascode JFET Unclamped Inductive switching (UIS)

set struc = "Jfet2"
set re1=5               # JFET Gate resistance
set rg = 50             # Cascode Gate resistance
set pulse="300us"
set period="400us"
set Te1=423
set vdd1 = 50
set Ldd = 1
set alph = 80
set timestamp = "280us,305us,307us,309us,311us,320us,331us,350us"

# Structure input file set to the correct directory
set infile1 = "/..DIR../$"struc".str"
set infile2 = "/..DIR../LVmos_1.str"


# DC solution
go atlas
.begin
vin 4 0 0
af 6=drain 8=gate 5=source infile=$"infile1" width=6e5
am 5=drain 1=gate 0=source infile=$"infile2" width=2e6
r1 4 1 $"rg"
L1 3 6 $"Ldd"mH
r2 8 0 $"re1"
vdd 3 0 $"vdd1"
Cdd 3 0 5.0mF
.nodeset v(1)=0 v(2)=0 v(3)=0 v(4)=0 v(0)=0 v(5)=0 v(6)=0 v(7)=0
.numeric vchange=1. toldc=1.e-6 imaxdc=800
```

```
.options print noshift m2ln
.save outfile=UIS$"struc"_$"re1"Vsave
.end

#
contact device=af name=gate
contact device=am name=gate workf=4.37

#
models device=af cvt srh Analytic fldmob Auger print
models device=am cvt consrh fermi print
#
go atlas


#
go atlas
.begin
vin 4 0 pulse 0 20 2us 0.01us 0.01us $"pulse" $"period"
af 6=drain 8=gate 5=source infile=$"infile1" width=6e5
am 5=drain 1=gate 0=source infile=$"infile2" width=2e6
r1 4 1 $"rg"
L1 3 6 $"Ldd"mH
r2 8 0 $"re1"
vdd 3 0 $"vdd1"
Cdd 3 0 5.0mF
.numeric lte=0.01 dtmin=0.01ps dtmax=1us
.options print noshift
.load infile=UIS$"struc"_$"re1"Vsave
.log outfile=UIS$"struc"_$"re1"
.save master=UIS$"struc"_$"re1" tsave = $"timestamp"
.tran 1ns $"period"
.end
#
OUTPUT E.MOBILITY H.MOBILITY con.band val.band DEVDEG CHARGE OX.CHARGE
qss TRAPS
#
## Tsivizov heat conctivity & capacity models
MATERIAL mat=4H-SiC TCON.POLYN TC.A=-0.171 TC.B=1.488e-3 TC.C=0
MATERIAL mat=4H-SiC HC.STD HC.A=0.676 HC.B=6.565e-3 HC.C=-3.697e-7
HC.D=6.852e-10
#
contact device=af name=gate
contact device=am name=gate workf=4.37
#
thermcontact device=af num=5 ext.temp=$"Te1" alpha=$"alph" y.min=10
thermcontact device=am num=7 ext.temp=$"Te1" alpha=100 y.min=6.0
#
models device=af cvt srh Analytic fldmob Auger print lat.temp
models device=am cvt consrh fermi print lat.temp

#
probe device=af x=1.5 y=4.0 lat.temp
probe device=am x=1.2 y=1.0 lat.temp
#
impact device=af selb AN1=2.78E6 AN2=2.78E6 BN1=1.05E7 BN2=1.05E7
AP1=3.51E6 AP2=3.51E6 BP1=1.03E7 BP2=1.03E7 BETAN=1.37 BETAP=1.09
impact device=am selb an2=7.03e05*1.25

#
method newton maxtrap=30
```

```
#
go atlas

#
tonyplot UIS$"struc"_$"re1"_tr.log

quit
```

APPENDIX A5. Cascode JFET Short circuit

```
## Cascode JFET Short circuit
set struc = "Jfet2"
set re=5                # JFET Gate resistance
set rg = 100            # Cascode Gate resistance
set pulse="4us"
set period="12us"
set Te=350
set vdd1=400
set Ldd = 500
set Ld = 50
set alph = "200"
set                                timestamp                                =
"1us,2.2us,2.5us,3us,4us,5us,6us,7us,8.2us,9.4us,11us"

# Structure input file set to the correct directory
set infile1 = "/..DIR../$"struc".str"
set infile2 = "/..DIR../LVmos_1.str"

# DC solution
go atlas
.begin
vin 4 0 0
afet 6=drain 8=gate 5=source infile=$"infile1" width=4e5
amos 5=drain 1=gate 0=source infile=$"infile2" width=2e6
r1 4 1 $"rg"
r2 8 0 $"re"
L2 2 6 $"Ld"nH
L3 3 2 $"Ldd"nH
vdd 3 0 $"vdd1"
.nodeset  v(1)=0  v(2)=0  v(3)=0  v(4)=0  v(0)=0  v(5)=0  v(6)=0  v(7)=0
v(8)=0
.numeric vchange=1. toldc=1.e-6 imaxdc=800
.options print noshift m2ln
.save outfile=$"struc"_T$"Te"SS
.end
#
contact device=afet name=gate
contact device=amos name=gate workf=4.37
#
models device=afet cvt BGN srh Analytic fldmob Auger print
models device=amos cvt consrh fermi print

go atlas

# Transient Solution
go atlas
.begin
vin 4 0 pulse 0 20 2us 0.01us 0.01us $"pulse" $"period"
afet 6=drain 8=gate 5=source infile=$"infile1" width=4e5
amos 5=drain 1=gate 0=source infile=$"infile2" width=2e6
```

```
r1 4 1 $"rg"
r2 8 0 $"re"
L2 2 6 $"Ld"nH
L3 3 2 $"Ldd"nH
vdd 3 0 $"vdd1"
.numeric lte=0.01 dtmin=0.01ps dtmax=1us
.options print noshift
.load infile=$"struc"_T$"Te"SS
.log outfile=$"struc"_T$"Te"
.save master=$"struc"_T$"Te" tsave = $"timestamp"
.tran 1ns $"period"
.end

# Structure outputs
OUTPUT E.MOBILITY H.MOBILITY
# LV MOSFET gate Interface traps
INTERFACE device=amos QF=-5e11 Y.MAX=0.2

# Material model
## Tsivizov heat conctivity & capacity models
MATERIAL mat=4H-SiC TCON.POLYN TC.A=-0.171 TC.B=1.488e-3 TC.C=0
MATERIAL mat=4H-SiC HC.STD HC.A=0.676 HC.B=6.565e-3 HC.C=-3.697e-7
HC.D=6.852e-10

# Set work function gate electrode
contact device=afet name=gate
contact device=amos name=gate workf=4.37

# Thermal contact
thermcontact device=afet ext.temp=$Te alpha=$"alph" y.min=10.5
thermcontact device=amos ext.temp=$Te alpha=100 y.min=6.0

# Model statements
models device=afet cvt BGN srh Analytic fldmob Auger print lat.temp
models device=amos cvt consrh fermi print lat.temp

# Temperature probe
probe device=afet x=1.5 y=2.5 lat.temp
probe device=amos x=1.2 y=1.0 lat.temp

# Impact ionization models
impact device=af selb AN1=2.78E6 AN2=2.78E6 BN1=1.05E7 BN2=1.05E7
AP1=3.51E6 AP2=3.51E6 BP1=1.03E7 BP2=1.03E7 BETAN=1.37 BETAP=1.09
impact device=am selb an2=7.03e05*1.25

#
method newton
#
go atlas
# Plot log results
tonyplot $"struc"_T$"Te"_tr.log
quit
```

APPENDIX B JFET Cell Structure

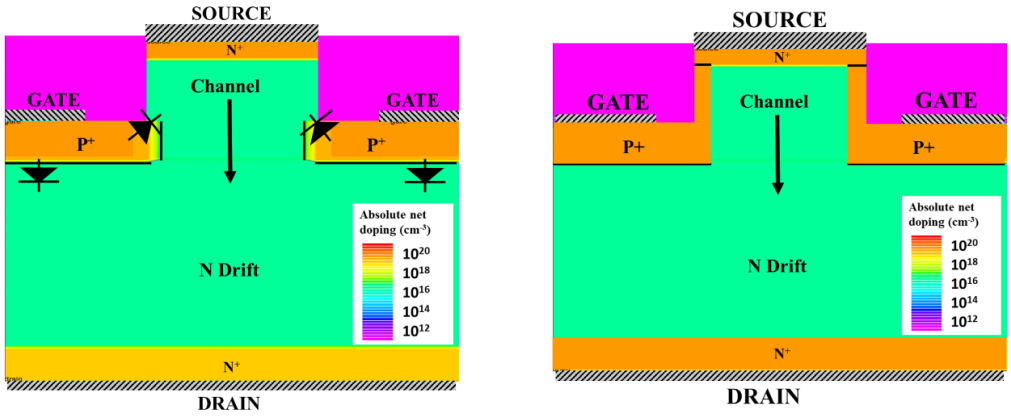


Figure. B 1 JFET cell structure variation (a) JFET without P+ side walls (b) JFET cell with P+ side walls

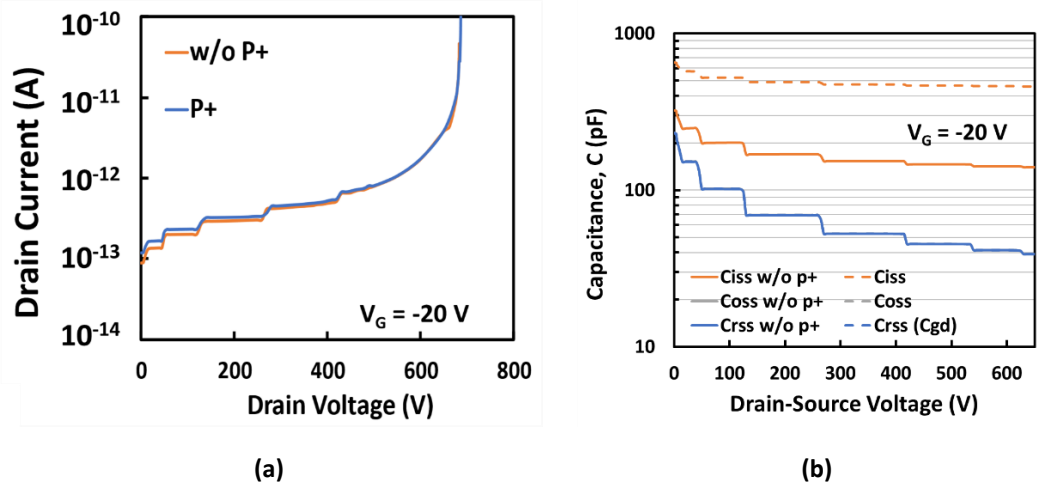


Figure. B 2. (a) Static breakdown characteristics (b) Capacitance characteristics showing the impact of the JFET cell structure without and with the P+ side walls.

Table B - 1. Impact of P+ side walls on JFET threshold voltage (DIBL)

Structure	Channel length (um)	Channel width (um)	V_{TH} (V_{DS} = 0.05 V, I_D = 20 mA)	V_{TH} (V_{DS} = 2 V, I_D = 20 mA)	ΔV_{TH} by DIBL
JFET w/o P+	1.3	1.0	-5.46 V	-5.92 V	0.46 V
JFET with P+	3.3	1.0	-4.93 V	-4.99 V	0.06 V

This section summarises the impact of the side wall on device characteristics. From Figure XX(a) it is evident that the inclusion of the P+ has a negligible impact on the JFET breakdown. In contrast, the input capacitance (C_{ISS}) for the JFET with P+ (dotted line) is considerable larger because the gate source capacitance is increased. Table XX shows how the P+ helps to reduce the impact of DIBL (reduced ΔV_{TH}). This is the result of the longer channel.

APPENDIX C PCB Design drawings

APPENDIX C1. Schematic drawings

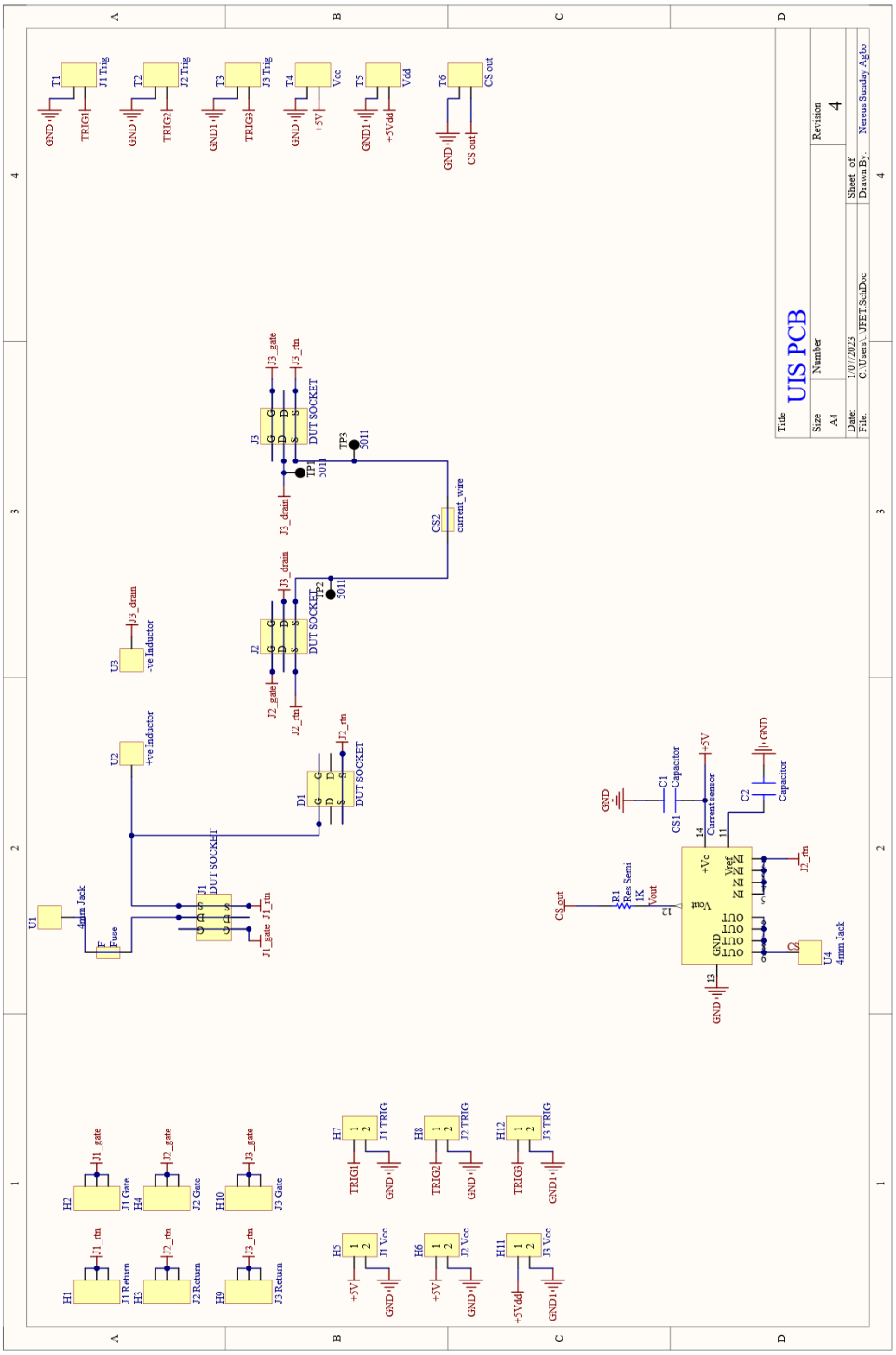


Figure. C 1 PCB schematic for the UIS test setup

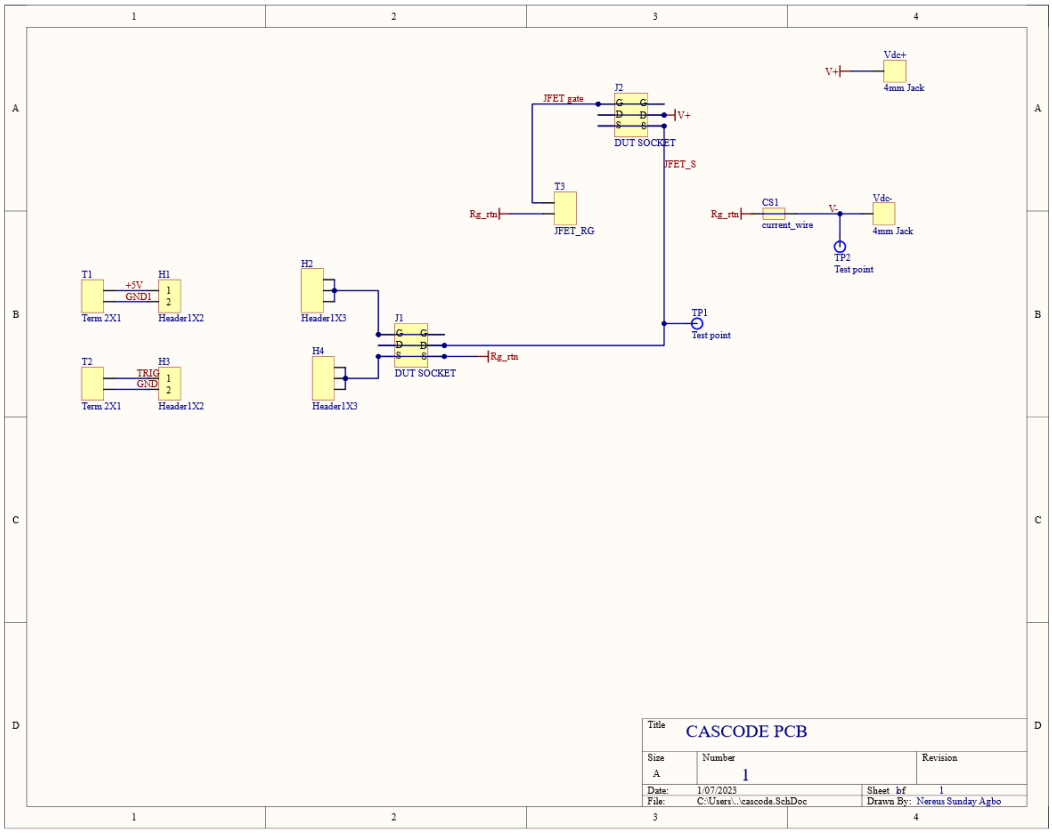


Figure. C 2 PCB schematic for the customised cascode circuit

APPENDIX C2. Layout drawings

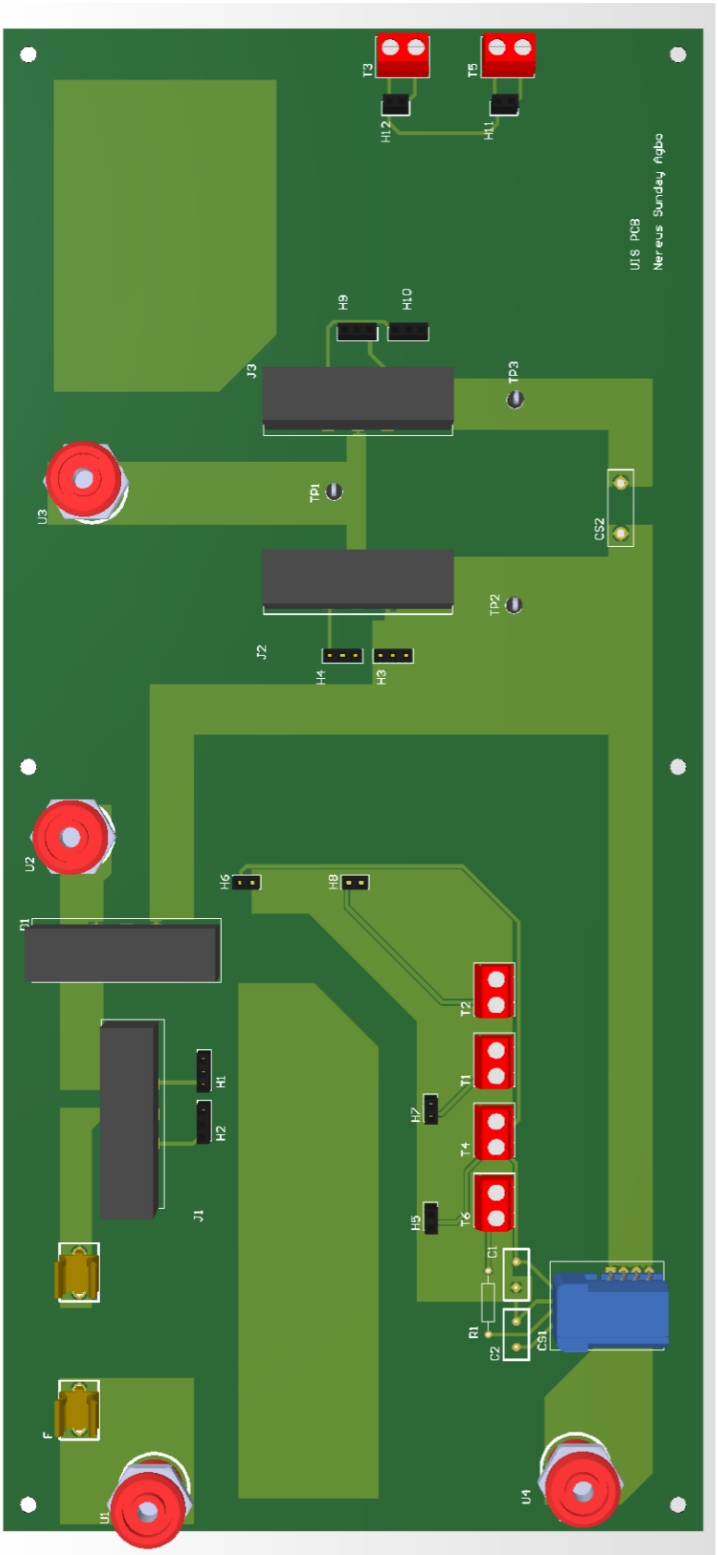


Figure. C 3 PCB 3D layout for the UIS test setup

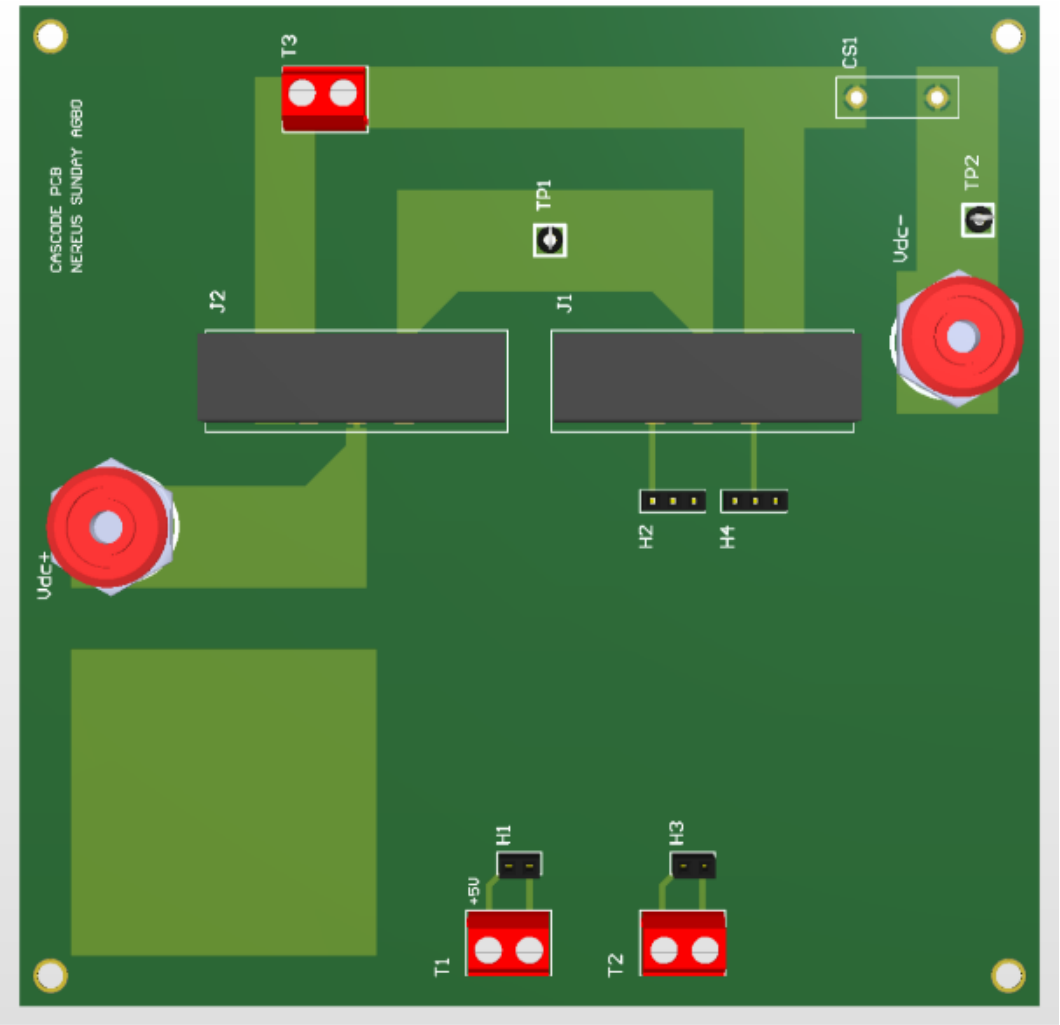


Figure. C 4 PCB 3D layout for the customised cascode circuit

APPENDIX D Reference Datasheets

APPENDIX D1. SiC Standalone JFET datasheet

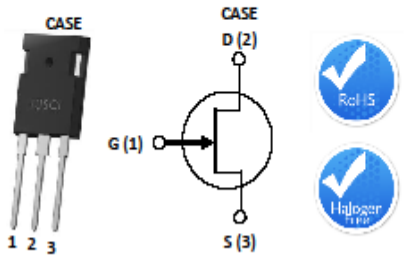
UnitedSiC

80mΩ - 650V SiC Normally-On JFET | UJ3N065080K3S

Datasheet

Description

United Silicon Carbide, Inc offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at V_{GS} = 0 V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.



Part Number	Package	Marking
UJ3N065080K3S	TO-247-3L	UJ3N065080K3S

Features

- Typical on-resistance $R_{DS(on),typ}$ of 80mΩ
- Voltage controlled
- Maximum operating temperature of 175°C
- Extremely fast switching not dependent on temperature
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant

Typical Applications

- Over current protection circuits
- DC-AC inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC (1)	-20 to +20	
Continuous drain current (2)	I_D	T_C = 25°C	32	A
		T_C = 100°C	24	A
Pulsed drain current (3)	I_{DM}	T_C = 25°C	72	A
Power dissipation	P_{tot}	T_C=25°C	190	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

(1) +20V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.

(2) Limited by $T_{J,max}$

(3) Pulse width t_p limited by $T_{J,max}$

APPENDIX D2. SiC Cascode JFET datasheet.

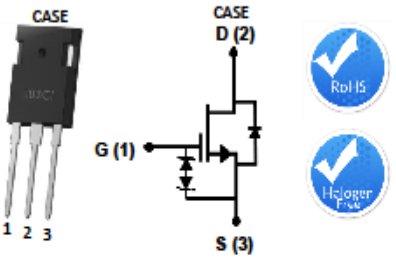
UnitedSiC

80mΩ - 650V SiC Cascode | UJ3C065080K3S

Datasheet

Description

United Silicon Carbide's cascode products co-package its high-performance G3 SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.



Part Number	Package	Marking
UJ3C065080K3S	TO-247-3L	UJ3C065080K3S

Features

- Typical on-resistance $R_{DS(on),typ}$ of 80mΩ
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class 2

Typical Applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C=25°C	31	A
		T_C=100°C	23	A
Pulsed drain current [2]	I_{DM}	T_C=25°C	65	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS}=2.1A	33	mJ
Power dissipation	P_{tot}	T_C=25°C	190	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

1 Limited by $T_{J,max}$

2 Pulse width t_p limited by $T_{J,max}$

3 Starting T_J = 25°C

APPENDIX D3. SiC Trench MOSFET datasheet.

SCT3060AL

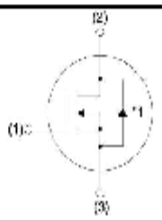
N-channel SiC power MOSFET **Datasheet**

V_{DSS}	650V
$R_{DS(on)}$ (Typ.)	60mΩ
I_D	39A
P_D	165W

●**Outline**

TO-247N

●**Inner circuit**



(1) Gate
(2) Drain
(3) Source

*1 Body Diode

●**Features**

1) Low on-resistance
2) Fast switching speed
3) Fast reverse recovery
4) Easy to parallel
5) Simple to drive
6) Pb-free lead plating ; RoHS compliant

●**Application**

- Solar inverters
- DC/DC converters
- Switch mode power supplies
- Induction heating
- Motor drives

●**Packaging specifications**

Type	Packing	Tube
	Reel size (mm)	-
	Tape width (mm)	-
	Basic ordering unit (pcs)	30
	Taping code	C11
	Marking	SCT3060AL

●**Absolute maximum ratings** (T_a = 25°C)

Parameter		Symbol	Value	Unit
Drain - Source voltage		V_{DSS}	650	V
Continuous drain current	T_c = 25°C	I_D *1	39	A
	T_c = 100°C	I_D *1	27	A
Pulsed drain current		$I_{D,pulse}$ *2	97	A
Gate - Source voltage (DC)		V_{GSS}	−4 to +22	V
Gate-Source Surge Voltage (t_{surge} < 300nsec)		V_{GSS_surge} *3	−4 to +26	V
Recommended Drive Voltage		V_{GS_op} *4	0 / +18	V
Junction temperature		T_j	175	°C
Range of storage temperature		T_{stg}	−55 to +175	°C

APPENDIX D4. SiC Planar MOSFET datasheet.

CREE

C3M0065090D

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology

N-Channel Enhancement Mode

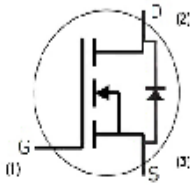
V_{DS}	900 V
I_{D} @ 25°C	36 A
$R_{DS(on)}$	65 mΩ

Features

- C3M SiC MOSFET technology
- High blocking voltage with low On-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Qrr)
- Halogen free, RoHS compliant

Package

RoHS



Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch Mode Power Supplies

Part Number	Package	Marking
C3M0065090D	TO-247-3	C3M0065090

Maximum Ratings (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	900	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage (dynamic)	-8/+19	V	AC (f >1 Hz)	Note: 1
V_{GSop}	Gate - Source Voltage (static)	-4/+15	V	Static	Note: 2
I_D	Continuous Drain Current	36	A	V_{GS} = 15 V, T_C = 25°C	Fig. 19
		23		V_{GS} = 15 V, T_C = 100°C	
$I_{D(pulse)}$	Pulsed Drain Current	90	A	Pulse width t_P limited by T_{jmax}	Fig. 22
E_{AS}	Avalanche energy, Single pulse	110	mJ	I_D = 22A, V_{DD} = 50V	
P_D	Power Dissipation	125	W	T_C=25°C, T_J = 150 °C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	°C		
T_L	Solder Temperature	260	°C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): When using MOSFET Body Diode V_{GSmax} = -4V/+19V
Note (2): MOSFET can also safely operate at 0/+15 V

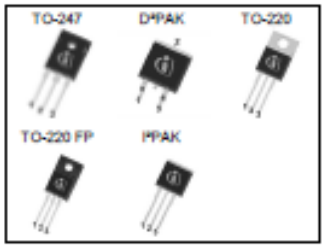
APPENDIX D5. Si Superjuction MOSFET datasheet.

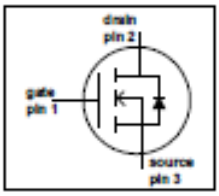
650V CoolMOS™ CFD2 Power Transistor

IPW65R150CFD , IPB65R150CFD , IPP65R150CFD
IPA65R150CFD , IPI65R150CFD

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.





Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Easy to use/drive
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Pb-free plating, Halogen free for mold compound

Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server, Telecom and Solar.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
RDS(on),max	0.15	Ω
Qg,typ	86	nC
ID,pulse	72	A
Eoss @ 400V	6.8	µJ
Body diode di/dt	900	A/µs
Qrr	0.7	µC
trr	140	ns
Irrm	8.8	A

Type / Ordering Code	Package	Marking	Related Links
IPW65R150CFD	PG-TO 247	65F6150	see Appendix A
IPB65R150CFD	PG-TO 263		
IPP65R150CFD	PG-TO 220		
IPA65R150CFD	PG-TO 220 FullPAK		
IPI65R150CFD	PG-TO 262		

2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D			22.4	A	T_C = 25°C
				14.2		T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$			72	A	T_C = 25°C
Avalanche energy, single pulse	E_{AS}			614	mJ	I_D = 4.5A, V_{DD} = 50V
Avalanche energy, repetitive	E_{AR}			0.93	mJ	I_D = 4.5A, V_{DD} = 50V
Avalanche current, repetitive	I_{AR}			4.5	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	V_{DS} = 0 ... 400V
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC (f > 1 Hz)
Power dissipation (non FullPAK) TO-247, TO-220, I²PAK	P_{tot}			195.3	W	T_C = 25°C
Power dissipation (FullPAK) TO-220 FP	P_{tot}			34.7	W	T_C = 25°C
Operating and storage temperature	T_j, T_{stg}	-55		150	°C	
Mounting torque (non FullPAK) TO-247, TO-220, I²PAK				60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220 FP				50	Ncm	M2.5 screws
Continuous diode forward current	I_S			22.4	A	T_C = 25°C
Diode pulse current	$I_{S,pulse}$			72	A	T_C = 25°C
Reverse diode dv/dt[3]	dv/dt			50	V/ns	V_{DS} = 0 ... 400V, $I_{SD} \le I_D$, T_j = 25°C
Maximum diode commutation speed	di/dt			900	A/µs	

[1] Limited by $T_{j,max}$. Maximum
[2] Pulse width t_p limited by $T_{j,max}$
[3] V_{peak}<$V_{(BR)DSS}$, T_j<$T_{j,max}$, identical low side and high side switch with same Rg