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Nanoscale Hafnium Oxide Passivation for Photovoltaic and Electronic Devices

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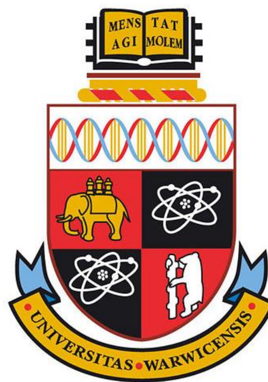

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Publications

Journal publications

A. Wratten, S. L. Pain, D. Walker, A. B. Renz, E. Khorani, T. Niewelt, N. E. Grant, J. D. Murphy, "Mechanisms of Silicon Surface Passivation by Negatively Charged Hafnium Oxide Thin Films", *IEEE Journal of Photovoltaics*, vol. 13(1), p. 40-47, 2023

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Declaration of Authorship

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Ailish Wratten

May 2023

Abstract

This thesis presents a collection of work investigating the application of hafnium oxide (HfO_2) thin films as both wet-chemical and surface-state passivation layers for photovoltaic (PV) and electronic devices. Surface-state passivation layers are an essential aspect of silicon (Si) based PV devices, preventing carrier recombination that would otherwise occur for direct metal-Si contacts; thus increasing conversion efficiency. Such layers – often dielectric thin films – can either be used as 'passivation layers' whereby the films are regionally etched to allow direct metal-Si contact, as in the case of Passivated Emitter and Rear Contact (PERC) cells, or 'passivation interlayers' where the dielectric is kept in place between the metal and Si in a passivating contact structure, with the Tunnel Oxide Passivated Contact (TOPCon) cell.

HfO_2 is shown to have excellent potential as a passivation layer, producing surface recombination velocities (SRVs) <1 cm/s with just 2.5 nm of material, which is competitive with current commercially used dielectric passivation layers. However, the conflicting annealing temperature dependence of passivation and conductance suggests that the use of HfO_2 as a passivating interlayer is limited. A novel form of passivating contact structure is introduced, that utilises dielectric stacks with HfO_2, which could provide a low-temperature alternative to the current silicon dioxide (SiO_x)/poly-Si passivating contact structure used in TOPCon.

This novel structure relies upon the unique etching characteristics of HfO_2 when combined with an aluminium oxide (Al_2O_3) layer, which results in pinhole formation. HfO_2 is found to be highly resistant to HF etching when crystallised, but etches rapidly whilst in an amorphous state. This varying etch resistance could potentially provide a route to wafer patterning, through a combination of laser annealing and a simple HF dip. This technique is more easily scaled-up for industrial application than existing photolithography processes. This strong etch resistance suggests great potential for HfO_2 thin films to be utilised as protective barrier layers in complex device fabrication for both electronic and photovoltaic applications.

Chapter 1

Introduction

1.1 Motivation

Global temperatures are rising significantly, with data showing a rate of increase of 0.0014–0.0018 °C per year since the 1970's [1, 2]. This temperature increase can be attributed to human activity, specifically the burning of fossil fuels [3]. Fossil fuels are essentially large stores of carbon which, when burned, release so called 'greenhouse gases' (GHGs), such as carbon dioxide (CO_2) and methane (CH_4). These gases, when released into the Earth's atmosphere, trap heat by preventing reflected solar radiation from escaping into space, similar to the role of the glass in a greenhouse. This global temperature increase can have devastating consequences on the ecosystem, increasing the risk of extreme weather events, such as flooding and drought, negatively impacting biodiversity, crop yields, and the general health of the population [4-6]. We must reduce our reliance on fossil fuels and expand our use of renewable energy resources if we are to keep the global temperature increase below 1.5 °C above pre-industry levels, and mitigate the impacts of climate change, in line with the Paris Agreement [7].

Solar photovoltaic (PV) technologies convert sunlight into electricity. This is a clean and renewable form of energy that does not rely upon the consumption of limited fossil fuel sources, and does not produce harmful greenhouse gases, beyond what is produced during the creation of the PV devices. Solar energy is currently the fastest growing energy resource, with almost half of additional renewable energy coming from solar additions in 2021 [8]. Based on the increasing rate of PV energy generation, it is estimated that we reached 1TW of global PV capacity in 2022. This rapid growth in the PV sector can be at least partially attributed to the massive decrease in costs.

In the last 10 years there has been a 60-80% decrease in PV system costs (inflation adjusted), for residential to utility scale PV [9].

Devices based upon crystalline silicon (c-Si) dominate the PV market, with estimates of 70-95% market share [10, 11]. This will likely remain the case, largely due to the availability of Si, being the second most abundant element on earth. Within the sector of c-Si PV there are several different cell designs on the market, including passivated emitter and rear contact (PERC) cells and tunnel oxide passivated contact (TOPCon) cells. Current data indicates that PERC cells currently dominate the Si PV market, with almost an 80% market share. However, this is set to shift substantially with projections of 60% market share for TOPCon cells by 2033 [12]. As such, both research on cell types will play an important role over the next 10 years in determining the future of PV.

Note that both of these cell designs include an aspect of 'passivation'. In the case of PERC cells the passivation comes in the form of a dielectric passivating layer on the rear of the cell. TOPCon designs usually include a passivating layer at the front and a passivating contact interlayer at the rear. A passivation layer is designed to minimise the recombination of charge carriers at the Si surface and is often locally removed to allow for a direct interface between the Si and the metal contact. A passivating contact interlayer, on the other hand, is kept in place between the metal and Si, and must therefore also have high conductance. The inclusion of such layers is essential for improving the conversion efficiencies of c-Si solar cells.

The development of passivating contact structures has led to substantial efficiency gains within the last few years, with improvements to device efficiency within the last 4 years equivalent to the previous 25 years [13, 14]. However, the challenge of industrial-scale application remains. The simplest and most cost-effective approach to this is to address the recombination losses at the hole-collecting contact, via upgrades that build upon existing industrial processes [13].

The passivating contact structure of current TOPCon cells includes a thin SiO_x layer and a thicker poly-Si layer, which enables carrier transport through both tunnelling and pinhole mechanisms, thus maintaining high conductivity [15, 16]. However, the thermal budget to produce such a device is very high, with temperatures 800-900 °C required to create the tunnelling structure [17, 18]. Reaching higher processing temperatures requires more energy, resulting in higher operational costs and carbon emissions. Additionally, the band alignment of SiO_x compared to Si shows quite strong favourability towards electron transport [19]. Whilst this makes SiO_x a strong electron selective layer, it is not so suitable for hole-transport. Selectivity for both electrons and holes is a necessary step for improving solar cell efficiencies, as it would allow for increased conversion efficiency at both the front and rear of the cell. Thus, this leaves the need for the development of a lower temperature passivating contact structure, with the potential of hole-selectivity.

Hafnium oxide (HfO_2) is an interesting candidate to investigate for this, due to the lower barrier height for hole transport, compared to more commonly used dielectrics like SiO_2 and Al_2O_3 [19]. Additionally, the variable charge polarity of the material could potentially lend itself to either electron or hole transport, depending on the deposition parameters [20-26]. This material has also shown promise as an anti-reflective coating (ARC) [27, 28], meaning a single HfO_2 layer could potentially be implemented as a multi-use film, providing multiple benefits to the solar cell device whilst also decreasing the process complexity.

Furthermore, HfO_2 has demonstrated remarkable robustness, having been investigated for applications as protective barrier layers in varying extreme environments [27, 29, 30]. This may be of great benefit in the harsh conditions often utilised in PV device manufacturing, with the potential for HfO_2 to either replace the much more sensitive dielectrics currently in use, such as Al_2O_3, or to shield these dielectrics during the manufacturing process. The application of this could extend beyond PV to the manufacturing of other semiconductor devices.

For HfO_2 to be an effective layer in PV device structures it must demonstrate both good passivation and high conductance. This work shall investigate these parameters, as well as the stability of the material in typical Si processing conditions, with the aim of developing multi-use passivation interlayers for both photovoltaic and electronic applications.

1.2 Thesis Outline

This thesis investigates physical and electrical properties of HfO_2, both as a single layer, and incorporated into dielectric stacks, for intended applications in photovoltaic and electronic devices, with particular focus on implementation as a passivating interlayer.

The three main objectives of this work are as follows:

1. Study the etch resistance of HfO_2 to chemical solutions commonly used in Si processing, comparing single layer HfO_2 films to Al_2O_3/HfO_2 dielectric stacks, and utilise this within a device fabrication process.
2. Optimise the post-deposition conditions of HfO_2 films grown *via* atomic layer deposition (ALD) to maximise passivation quality, and investigate the material properties to better understand the passivation mechanisms.
3. Investigate the performance of HfO_2 films incorporated into metal contact structures to better understand the potential of this material for passivating contact structures, and expand upon this to consider more complex dielectric structures.

These three main objectives will be split into three separate research chapters, each containing an introduction, methodology, and conclusion section, as well as several sections reporting and discussing various results. These chapters will be preceded by individual introductory and background chapters that will detail the necessary theory, methodology, and literature relevant to this work. This thesis will then be summarised

in an overall concluding chapter that will also discuss the future outlook of this area of research.

Chapter 2 covers the existing literature and important background theory needed to understand the context of this research, such as an explanation of semiconductor materials and a literature review on the development and investigation of ALD grown HfO_2.

Chapter 3 provides details of the methodologies used within this work, both in terms of experimental apparatus/processes, and data analysis. This chapter includes descriptions and schematics of general processes, but does not detail any specific pieces of equipment or recipes. These details are instead included in the individual results chapters where the methodologies are utilized. Examples of methodologies detailed in this section include atomic layer deposition, X-ray diffraction, and the Expanded Cox and Strack method.

Chapter 4 is the first of the results chapters, focusing on the etching mechanisms of HfO_2 to solutions used in Si processing. Single layer HfO_2 films are compared to layers incorporated into dielectric stacks. The post-deposition annealing temperatures are varied and a correlation between the etch resistance and physical parameters, such as film crystallinity and pinhole formation, is identified. An example is given of HfO_2 being utilised as a protective barrier layer in a device fabrication process. Attempts are made to locally anneal HfO_2 films in order to make use of the varied etch resistance of the material, and produce a patterned dielectric layer.

Chapter 5 focuses on investigating the passivation quality of HfO_2 films on Si. Post-deposition annealing conditions are varied, including annealing time, ambient, and temperature. The variations in measured carrier lifetime, representative of surface passivation, are distinguished from contributions of the bulk Si material using a superacid re-passivation technique. Material parameters such as film crystallinity and dielectric charge are studied for various annealing conditions. The results of this are

used to distinguish between the contributions of chemical and field-effect passivation mechanisms that are provided by the HfO_2 layer.

Chapter 6 is the final results chapter, which starts with a continuation of the investigations in the previous chapter, this time instead focusing on decreasing the film thickness, for intended applications in a passivating contact structure. A preliminary investigation is made by incorporating HfO_2 into a simple and low thermal budget Si-dielectric-metal stack, and the IV characteristics are measured. The final experiment brings all three results chapters together by utilising the pinhole formation discovered in Chapter 4 to create a novel contact structure, coined 'Micro-PERC'.

Chapter 7 summarises the work reported in this thesis and discusses the outlook of the research presented here.

Chapter 2

Background

This chapter covers the foundational knowledge necessary to grasp the context of the research that has been conducted in this work. The fundamental theories of several key concepts are introduced, as well as the central materials and their applications, including existing literature on the topic.

2.1 Semiconductors

In the section the basic properties of semiconductor devices are explained, including the approaches that are used to describe such materials. A description of dielectric materials is also included, since they are often utilised alongside semiconductor materials.

2.1.1 Semiconductor materials

Semiconductor materials have properties that fall somewhere between that of conducting and insulating materials [31]. In semiconductors, energy is required to free electrons from the bonds they form with the material structure. These free electrons are what enable current flow. The bonds in semiconductors are typically stronger than those in conductors, which instead have a very large number of weakly bonded electrons.

The energy of electrons within a material can be described by the materials band structure. Based upon the different types of bonds that can be formed within a material, electrons can have discrete amounts of energy. A band structure is made up of the energy levels that electrons may have, and energy band gaps, which are the

range of energies that electrons cannot have. The valance band (VB) of a material is the highest energy band that electrons can occupy whilst in orbit around an atom of that material. If a valence electron breaks free from its orbit, it becomes a conduction electron, or free electron, and is able to conduct current through the material. The lowest energy band occupied by free electrons is called the conduction band (CB).

Between the VB and CB is a band gap, which is the energy barrier that electrons need to overcome to break their valance bonds and move from the VB up to the CB. Insulators have a very large band gap, which prohibits the transfer of electrons from VB to CB. In conductors the VB and CB may actually overlap, meaning that all electrons within the material behave as free electrons. Semiconductors are somewhere in between. They have a small enough band gap that movement of electrons from the VB to CB is still a prominent occurrence.

Electrons are not the only charge carriers within semiconductor materials. The vacancy caused by the freeing of an electron creates a positively charged vacancy called a 'hole'. Holes move when an electron from elsewhere in the structure occupies the vacancy, thus creating a vacancy in the original location of the electron. Therefore holes travel in the opposite direction to electrons. Carrier mobility is much higher for electrons than holes as each time a hole moves an electron much break its covalent bonds with the material, whereas the free electrons can already move freely. This carrier transport mechanism becomes apparent under the application of an applied external electric field, thus the net flow of current in a semiconductor flows in the direction of the external field. When a free electron travels close to a hole, within the hole's so called capture cross section, the electron may occupy the space, and the two charge carriers are lost. This is called carrier recombination, and results in a reduced current flow.

The number of free electrons available in a semiconductor material at any given temperature is called the intrinsic concentration, n_i, with an equivalent number of holes, p_i. Doping is a process by which impurities are implanted into a material in

order to introduce either more electrons or holes. These impurities, called dopants, are either donors or acceptors, depending on whether they provide electrons or holes. The level of doping is such that the carriers provided by the dopant are significantly higher than the intrinsic concentration ($n \gg n_i$ or $p \gg p_i$). Semiconductors with electrons as the majority carriers are called *n*-type semiconductors, and those with majority holes are called *p*-type.

When a *p*-type and *n*-type semiconductor are brought together, they create a *pn* junction. In the area immediately surrounding the interface between these two materials a space is created where the charge carriers from each material come into contact with each other and recombine, leaving almost no free charge carriers; this is called the depletion region. In this region only the carriers bonded to the material are present. The *n*-type material in this region is therefore positively charged, and the *p*-type material is negatively charged. This separation of charge gives rise to an electric field pointing from the *n*- to the *p*- side; this is called the contact potential. A schematic of a *pn* junction can be seen in Figure 2.1.

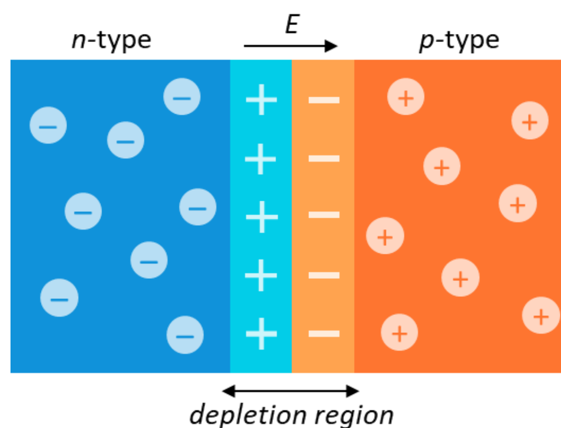


Figure 2.1: Schematic of a pn junction, where an n-type and p-type material come into contact, forming a depletion region between the two materials that produces an internal electric field.

Carriers tend to diffuse from areas of high carrier concentration to low. So a hole will tend to diffuse from the *p*-type material, which has majority hole carriers, to the *n*-type material. This creates a so-called diffusion current that is aided by an applied external voltage.

Semiconductor materials do not have only one type of charge carrier. Previous discussion has focused on majority charge carriers, but there also exist oppositely charged minority charge carriers. In *n*-type semiconductors, holes are the minority carriers, and *vice versa* for *p*-type. Some minority carriers will drift into the depletion region and are pushed across the junction by the existing electric field. The net effect of the drifting of the two minority carrier types creates a small reverse saturation current. This current is determined via thermal carrier generation, rather than the junction voltage, and flows in the opposite direction to the diffusion current.

2.1.2 Metal-semiconductor interfaces

When contact is made between a metal and a semiconductor there is a transfer of free electrons, caused by the difference in work function between the two materials [32]. The work function of a material is the energy required to free an electron from the bonds of a material. If the work function of the metal is higher than the semiconductor, then the electrons will flow from the semiconductor to the metal. This flow will continue until the Fermi levels of the materials are aligned. The Fermi level can be considered as a hypothetical energy level, existing within the bandgap, at which the most probable state of a level changes from occupied to unoccupied.

The concentration of free carriers in a semiconductor is comparatively much lower than in a metal, resulting in the free charge carriers near the surface of the semiconductor being depleted compared to the bulk; this is called a space charge region. In this case, the space charge region is equivalent to the depletion region that was previously discussed. In the case that the semiconductor work function is greater than the metal then electrons instead flow from the metal to the semiconductor and accumulate in the space charge region, thus creating an accumulation layer. If a space charge region is heavily depleted, such that the majority carrier concentration falls below the intrinsic concentration, the material can change to *p*-type (or vice versa for *p*-type to *n*-type). This is called an inversion layer.

Metal-semiconductor interfaces can generally result in two different types of contact. If the metal work function is less than the semiconductor, then the contact produced is Ohmic. If the metal work function is greater than the semiconductor, then a Schottky barrier is produced. Figure 2.2 shows the current-voltage (IV) characteristics of the two types of contact.

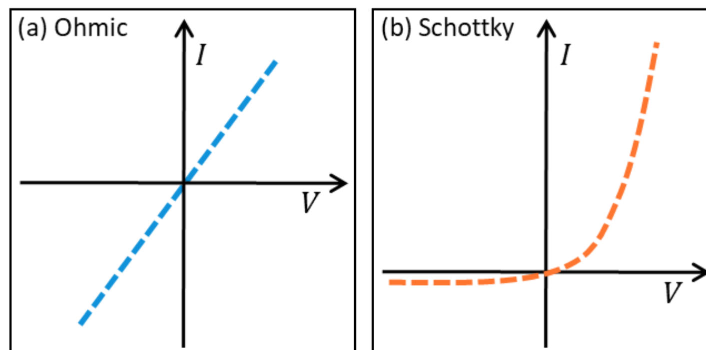


Figure 2.2: Current-voltage (IV) characteristics of (a) an Ohmic contact, and (b) a Schottky contact.

2.1.3 Band bending

In the space charge region, the electric field produced by the charge transfer between materials results in shifts within the energy bands of the semiconductor. This is called band bending. Bands will bend upwards when the metal work function is greater than the semiconductor (Figure 2.3(a)), and bend downwards when the opposite is true (Figure 2.3(b)). The degree of band bending is equivalent to the difference in work function between the two materials. Figure 2.4 shows the difference in band structures for accumulation, depletion, and inversion layers, for an *n*-type semiconductor.

Bend bending can also be induced by the application of an external field. This is known as field-effect-induced band bending. When a positive voltage is applied to bands, that were initially flat in the absence of applied voltage, an accumulation region is formed near the semiconductor surface, causing downward band bending. The opposite occurs for a negative applied voltage.

Band bending can also be induced by surface states. When a surface is terminated, many bonds at the surface of the material are left broken. These are known as dangling bonds. These bonds can form additional electronic states within the band gap of the semiconductor. In an *n*-type semiconductor electrons travel from the bulk to the surface, causing the Fermi level of the bulk to decrease and the Fermi level of the surface to increase. As these levels reach equilibrium the bands bend upward. In a *p*-type material the equivalent process results in downwards band bending. The density of surface states is usually much larger than the number of dopant states in the bulk, thus the Fermi level of a semiconductor is mostly determined by the surface states. The impact of surface-state-induced band bending can be controlled through surface passivation, which reduces the number of surface states that can act as recombination centres for carriers.

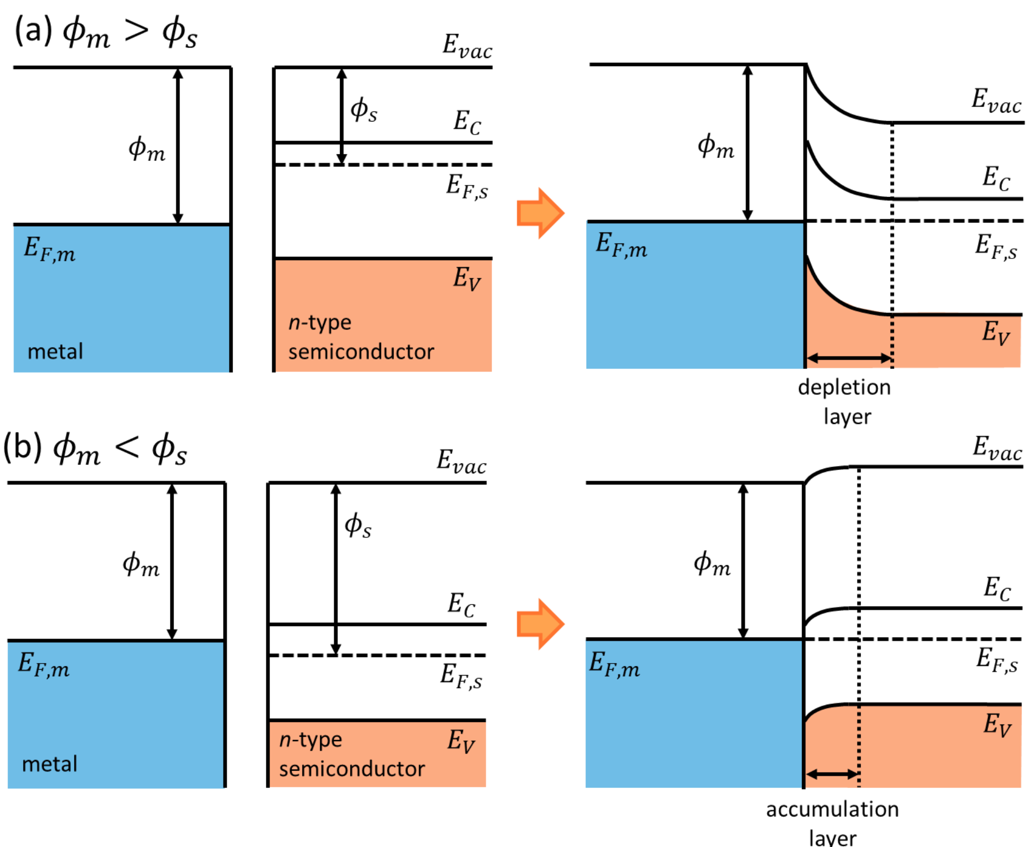


Figure 2.3: Band diagrams of metal-semiconductor contacts, depicting band bending when (a) the metal work function is greater than the semiconductor work function, and (b) vice versa. E_{vac} is the vacuum energy, φ is the work function, E_F is the Fermi level, and E_V and E_C are the valance and conduction band energies, respectively, This figure has been adapted from [32].

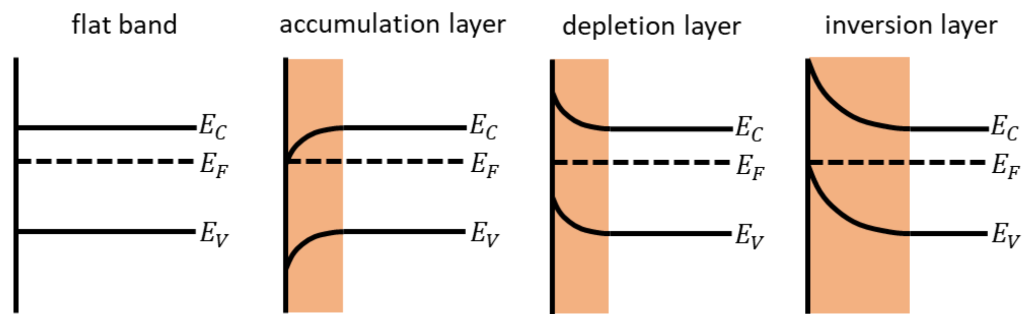


Figure 2.4: Band diagrams of n-type semiconductors with accumulation, depletion, or inversion layers. The orange box highlights the space charge region for each structure. This figure has been adapted from [32].

2.1.4 Dielectrics

Dielectrics are insulating materials, meaning no current flows through them in the presence of an electric field. However, unlike a standard insulator, dielectrics are capable of electric polarisation. This means that, in the presence of an external electric field, charge carriers can be slightly displaced in the direction of the field, as depicted in Figure 2.5. In this figure charges are depicted as dipoles, representing electron and hole pairs that are created simultaneously. This polarisation creates an internal electric field which reduces the influence of the external field.

Dielectrics are often incorporated into semiconductor devices due to their abilities to 'passivate' the semiconductor materials by mitigating surface-state recombination mechanisms.

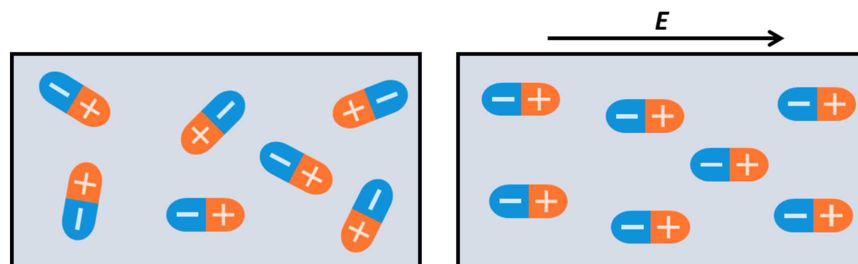


Figure 2.5: Schematic of electric polarisation within a dielectric material, resulting from the application of an external electric field, E.

2.2 Passivation

This section discusses the different forms of passivation required in the formation of different electronic and photovoltaic devices. The term ‘passivation’ is used to describe the process by which a surface is made inert in some form. This can be used to describe electronic surface-passivation layers, as is often the case with photovoltaic devices, and also protective layers, as is more common in electronics.

2.2.1 Photovoltaic devices

Termination of a semiconductor material surface creates discontinuities in the crystal lattice structure, leaving dangling bonds [33]. This means that the band structure is disrupted, and additional states can appear within the bandgap. These bandgap states are points of recombination for charge carriers; known as Shockley-read-Hall (SRH) recombination [34-37].

Measured carrier lifetimes, known as effective lifetimes, are a reflection of the length of time charge carriers typically exist before recombining, and are a contribution of the various recombination mechanisms within both the bulk and the surface material. Within the bulk material, lifetimes are limited by Auger-Meitner and radiative recombination mechanisms [38, 39]. It is also possible for SRH recombination to occur due to bulk impurities. However, bulk recombination mechanisms are usually negligible when compared to the contributions from the surface region. The lifetime of carriers at the surface can be determined by the difference between effective lifetime and the contribution of bulk mechanisms

$$\frac{1}{\tau_s} = \frac{1}{\tau_{eff}} - \frac{1}{\tau_{rad}} - \frac{1}{\tau_{Aug}} - \frac{1}{\tau_{SRH}} . \qquad (1)$$

The speed at which high charge carriers recombine within the surface region of a material, otherwise known as the effective surface recombination velocity (SRV) is given by:

$$S_{eff} = \frac{1}{\Delta n_d} \frac{n_s p_s - n_i^2}{\left(\frac{n_s + n_i}{S_{p0}}\right) + \left(\frac{p_s + n_i}{S_{n0}}\right)}, \quad (2)$$

where $S_{n0} = v_{th} D_{it} \sigma_n$ is electron recombination velocity, defined by the thermal velocity, v_{th}, the capture cross section, σ_n, and the density of states, D_{it}. S_{p0} is the equivalent capture velocity for holes. n_s and p_s are the steady state carrier concentrations, n_i is the intrinsic carrier concentration, and Δn_d is the excess minority carrier concentration, which is dependent upon the width of charge space region, d.

From this equation it can be seen that reducing S_{n0} and S_{p0} results in a smaller SRV, S_{eff}. This can be done by decreasing the rate of carrier capture by the interface states, by occupying the dangling bonds; this is known as 'chemical passivation'. It is also possible to change the ratio between p_s and n_s, by reducing the number of one type of carrier. Generally, minority carriers are what determine rate of recombination, so a lower p_s/n_s ratio is required for n-type silicon. Physically, this involves the formation of a fixed charge density, Q_f, at the surface, which will produce an electric field that penetrates into the semiconductor surface region, resulting in a change in carrier concentration. This is known as 'field-effect passivation'. This form of passivation can also be achieved through the implantation of dopants into the semiconductor surface in a high concentration, thus producing a carrier gradient. In this case, the dopants are known as emitters.

The SRV can be mathematically approximated as an integral of decaying exponents, describing the variation in carrier lifetime throughout the material as a result of spatial variations in carrier concentrations and carrier diffusion. A carrier generated in the bulk must diffuse to the surface before it can recombine, and carriers generated at the surface can either recombine immediate or may diffuse into the bulk, thus creating these spatial variations. The dominant term of this mathematical approximation is:

$$S_{eff} = \sqrt{D\left(\frac{1}{\tau_s}\right)} \tan\left(\frac{W}{2}\sqrt{\frac{1}{D}\left(\frac{1}{\tau_s}\right)}\right), \quad (3)$$

where W is the sample width, and D is the carrier diffusion coefficient. For a sufficiently low SRV, this equation can be simplified further to

$$S_{eff} = \frac{W}{2}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right). \quad (4)$$

This SRV is considered to be an effective SRV, S_{eff}, since this definition is formed through mathematical approximations which result in the recombination current actually being calculated for a virtual surface within the space charge region, rather than at the real surface.

Some alternative metrics used to evaluate surface recombination, and compare the passivation quality achieved from different dielectrics, are the saturation current density, J_0, and the implied open-circuit voltage iV_{oc}.

Surface passivation through dielectrics has become an essential field of research for the development of crystalline silicon (c-Si) photovoltaic devices [13]. Current cell performance has been limited by surface recombination, resulting from the direct metal-Si contacts in most existing cell architectures.

Three of the most prominent cell architectures in today's market are passivated emitter and rear contact (PERC) cells [12, 40, 41], tunnel oxide passivated contact (TOPCon) cells [12, 42, 43], and silicon heterojunction (HTJ or SHJ) cells [12, 44, 45]. Before the development of the PERC cell, a typical solar cell consisted of a full area aluminium contact on the rear, known as an aluminium back surface field (Al-BSF) cell. This cell design is depicted in Figure 2.6(a). The direct metal-Si contact interface caused high recombination losses in the cell. Additionally, much of the longer wavelength light, with energies below the silicon bandgap, would pass through the silicon, unable to generate electron-hole pairs, and be absorbed by the Al layer, causing the cell to heat up [46]. The high recombination, loss of light energy, and thermal instability meant that these cells were limited to an efficiency of ~20%. The development of the PERC cell introduced a passivation layer to the rear of the cell,

which prevents recombination and also reflects photons back into the silicon layer, thus increasing the efficiency limit. This passivation layer is then capped with an insulating dielectric, and localised regions of the passivation layer are etched away so that the silicon can be contacted. A schematic of an example PERC cell can be seen in Figure 2.6(b).

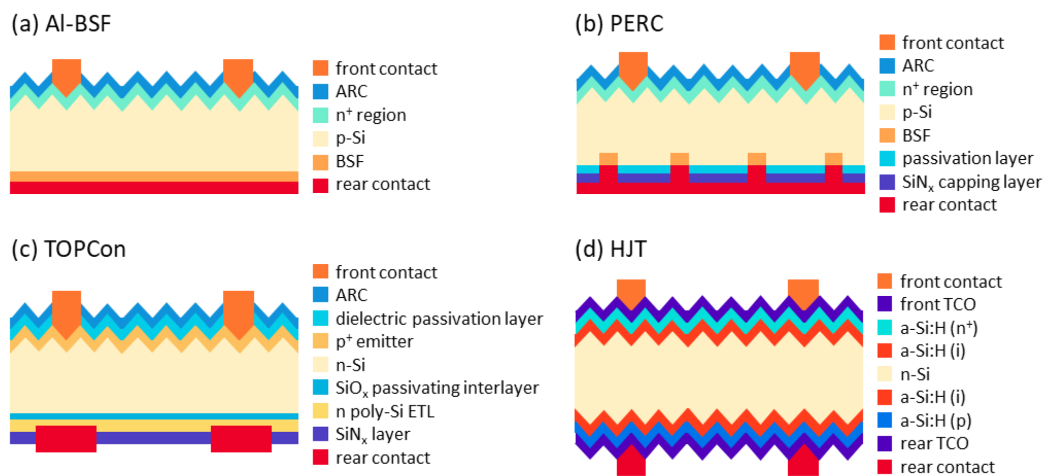


Figure 2.6: Schematics of (a) an Al-BSF cell, (b) a PERC cell, (c) a TOPCon cell, and (d) a HJT cell. Structures include anti-reflective coatings (ARC), back surface fields (BSF), electron transport layers (ETL), and transparent conductive oxides (TCO).

TOPCon cells have a somewhat similar structure to PERC, in terms of industrial processing, but include a doped conductive poly-Si layer and thin dielectric (SiO_2) passivating interlayer, as can be seen in Figure 2.6(c). HTJ cells consist of stacks of crystalline and amorphous silicon (c-Si and a-Si), doped in various ways, designed to absorb more wavelengths of light. This can be seen in Figure 2.6(d). This cell design can result in even higher efficiencies, and thus far has lead the way in tandem cell research with record breaking results, largely due the lateral charge carrier movement within these cell structures [47]. However, production of these cells requires restructuring of industrial processes, which significantly increases the capital expenditure (CapEx) compared to other cell designs.

As can be seen in the schematic of the TOPCon structure, the metal contacts on the rear to not directly interact with the Si wafer. Instead, the metal terminates within the

conductive poly-Si layer, and there is a thin SiO_x layer between the metal and the Si. This is an example of a passivating contact structure. Unlike with regular passivating layers, which are locally etched to allow for direct metal contacts, in a passivating contact there is a thin passivating interlayer between the metal and Si. This interlayer further reduces recombination at the surface in the regions surrounding the metal contacts. However, charge carriers must still be able to travel from the bulk material to the metal, meaning the passivating interlayer must have high conductivity.

There are two main mechanisms for carrier transport in passivating contact structures: tunnelling and pinholes. The probability of a carrier tunnelling through the layer is related to the thickness of the layer, as determined by the following equation [48]

$$P_T = \exp\left(\frac{-2}{\hbar} t \cdot \sqrt{2m^* \cdot q \cdot \Delta\phi_b}\right) \quad (5)$$

where $\hbar$ is given by Planck's constant, t Is the dielectric film thickness, m^* is the effective mass, q is charge, and $\Delta\phi_b$ is the barrier height in eV. Thus, the passivating dielectric must be kept as thin as possible, to facilitate carrier transport across the interlayer. However, in the case of pinhole transport, this thickness limitation is not as rigorous. An example of such carrier transport can be seen in the formation of pinholes in SiO_x/poly-Si structures [15, 16].

This work investigates dielectric materials for potential applications in photovoltaic devices as both passivating layers, as in the case of the PERC cell design, and passivating contact interlayers, as in the case of the TOPCon cell.

2.2.2 Barrier layers

As mentioned previously, passivation can also refer to the protection of a surface from external damage, including etching, corrosion, water, *etc*. This passivation layer essentially forms a protective barrier from environmental factors.

For example, in the research of photoelectrochemical (PEC) devices, as well as the passivation mechanisms mentioned in the above section, passivating films can also be used to stabilise the surface of a material by acting as a coating where there is no electrocatalytic activity, thus protecting the bulk material from oxidation [49, 50]. Similar processes are also used in the fields of metals and ceramics, where materials are often utilized in extreme environments, and for extended periods of time [51-53].

As electronic devices continue to increase in complexity, the processes for developing them also become more difficult. Going forward, having protective layers that can be deposited and removed at different stages of the production process may become an essential part of device development. This work will investigate the application of dielectric materials as protective layers that can protect against processing solutions commonly used in Si semiconductor device fabrication.

2.3 Film growth

Thin film structures are formed in a self-organising manner, driven by thermodynamic processes. This growth occurs in three main stages: nucleation, crystal growth, and grain growth. Nucleation involves the diffusion of atoms across a surface, clustering to form a lattice structure, at which point crystal growth begins. The combination of multiple crystal lattice structures during crystal growth is known as coalescence.

Grain boundaries occur due to sections of crystal structure within the material having different orientations. These grain boundaries are associated with an increase in energy; thus the overall energy of the system is lowered by movement of the grain boundaries in order to increase the grain size. This is the final stage of the growth process. Diagrams of these processes can be found in Figure 2.7, which has been adapted from [54].

There are three degrees of crystallinity a thin film can have: monocrystalline, polycrystalline, or amorphous. Monocrystalline films are typically grown on a single

seed crystal and, as such, consist of a single continuous crystal lattice; this is known as epitaxial growth. These are typically the most difficult thin films to produce. By contrast, an amorphous film is categorised by its complete lack of crystal structure and thus lack of long-range order. Polycrystalline films consist of several different crystals of varying size and orientation, separated by grain boundaries. Each type of film has advantages and disadvantages, and are suitable for different applications.

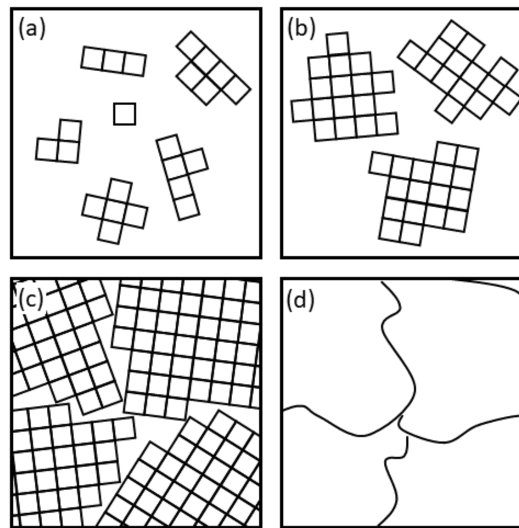


Figure 2.7: Schematic to illustrate the three main stages involved in the formation of a thin film structure: (a) nucleation, (b) crystal growth, (c) grain formation, and (d) grain boundaries as they would be seen through a microscope. This figure has been adapted from Mehl et al. [54].

Deposition of thin films onto a substrate can be done chemically or physically. Physical Vapour Deposition (PVD) methods, such as sputtering and evaporation, involve conversion of a material into a vapour phase and then reversion back to a condensed state in the presence of a substrate. With Chemical Vapour Deposition (CVD) the substrate is exposed to a gas precursor and the chemical reaction between the two produces the desired deposit on top of the substrate. There also exist methods of chemical deposition which do not fit under the umbrella of CVD, such as spin coating and electroplating.

Different deposition methods produce films of varying quality and, as such, are suitable for different applications. There are two main factors to consider in terms of

film quality: uniformity and conformality. Uniformity relates to how evenly a film is deposited across the entire expanse of a surface. A non-uniform surface may be very rough or have build-up in certain areas. Conformality is how well the film is able to coat all areas of a substrate. This is relevant for more complex structures where films may need to be deposited into trenches or around 3D objects. Film thickness is also an important aspect to consider when determining appropriate deposition methods.

For some applications, films several micrometres thick may be required, and so a deposition method with a rate on the order of nanometres per hour would be impractical. By contrast, some applications may require very fine control of the film thickness at a monolayer scale, thus a method which deposits dozens of nanometres of film in a very short space of time would not be suitable for this purpose. As an example of this, metal contacts for PV devices are usually on the order of 100 nm thick. A thermal or electron-beam evaporation system is able to deposit this much material within a few hours. However, the same evaporation system cannot be used to deposit the dielectric passivation interlayers that go beneath the metal contacts, as these layers are typically on the order of 1 nm thick. The evaporation system is not able to produce such thin films with a high degree of uniformity.

The focus of this work will be on thin films grown via atomic layer deposition (ALD), which is a form of chemical vapour deposition, capable of producing high-quality thin films, with the ability to control film thickness at the nanometre-scale. This deposition method is ideal for the dielectric passivation layers mentioned above.

2.4 Hafnium oxide

This sections covers the existing literature on hafnium oxide, which is the focal material of this thesis. This literature review includes the development of deposition processes, conflicting reports on material properties, and post-deposition processes, such as etching and patterning.

2.4.1 Development of HfO_2 thin films

Hafnium oxide (HfO_2) is a dielectric material with a bandgap of 5.6 eV and a dielectric constant of 16-18 (for undoped, monoclinic HfO_2) [55-57]. This material has been extensively researched in the field of electronics, for utilization in transistors and capacitors. This report considers the physical properties of HfO_2 films, which may prove useful within semiconductor device processing. Additionally, investigations are conducted into whether the physical and electrical properties of HfO_2 thin films lend themselves to photovoltaic application.

The first evidence that growing HfO_2 via ALD was possible came from a paper published by Kattelus *et al.* in 1992, on tantalum based oxide films [58]. To do this they used a glass substrate and $HfCl_4$ and H_2O precursors. Unfortunately, they were unable to find a constant growth per cycle (GPC) that did not depend upon temperature. The first paper which actually focused on the growth and characterisation of HfO_2 via ALD was published in 1994 by Ritala *et al.* [59]. Using the same substrate and precursors as Kattelus *et al.* they were able to grow a HfO_2 film at a constant rate of 0.5 Å/cycle. They discovered that the HfO_2 deposition began as an amorphous film, followed by a monoclinic polycrystalline HfO_2 layer, with roughness increasing as the thickness increased.

In the following years, many reports were published on optimising the growth of HfO_2 films. It was found that defects and surface roughness could be reduced by using lower deposition temperatures, to prevent crystal growth [59-62]. Unfortunately, low temperature deposition may result in an increase in chlorine and hydrogen impurities, depending on the precursors used [63, 64]. Growing amorphous films allows for the option of controlling material properties through post-deposition annealing.

Zhang *et al.* published a paper in 2019 on post-deposition annealing temperatures of HfO_2 films grown via ALD [65]. They found that at temperatures below 400 °C there is an amorphous interfacial layer consisting of SiO_2 and HfO_2, which forms due to the

diffusion of oxygen impurities from the HfO_2 towards the Si interface. Above 400 °C both the film and interfacial layer begin to crystallise, and by 550 °C the polycrystalline HfO_2 film becomes dominated by one phase, and the interfacial layer becomes crystallised SiO_2.

In 2020, Lo Nigro *et al.* compared the deposition of HfO_2 using plasma-enhanced ALD (PE-ALD) and thermal ALD [66], finding PE-ALD resulted in a faster deposition rate, a thinner interface layer, and a higher dielectric constant. Interestingly, the optimal deposition temperature was found to be ~250 °C for both deposition methods.

In 2006, Sreenivasan *et al.* investigated the effect of changing precursors on HfO_2 films and their fixed charge [20]. The precursors were tetrakis(diethylamido)hafium (TDEAH) and $HfCl_4$, and with H_2O used as the co-reactant in both cases. It was found that the chloride-based films had a positive shift in the flat band voltage, which indicates a negative fixed charge. They then postulate that impurities within the film may contribute to this fixed charge, as the chloride-based HfO_2 film had a large build-up of Cl impurities at the substrate interface. However, the full story relating to the charge polarity of HfO_2 seems to be more complex.

As mentioned, Sreenivasan *et al.* found that using chloride-based precursors results in a negative charge polarity. This result is supported by Aubriet *et al.* but is contradicted by Wang *et al.* who found their chloride-based HfO_2 films were positively charged [26, 67]. The discrepancies only continue when other precursors and deposition methods are considered.

The most frequently reported precursor is tetrakis(methylethylamide)hafnium (TEMAH). The majority of such reports suggest that using TEMAH in a thermal ALD process results in positive charge polarity, but this is not necessarily true for PE-ALD processes, or for unannealed samples [21-23, 68, 69]. Some literature suggests that use of an N_2 annealing ambient, on samples created with TEMAH, creates a negative charge polarity, but this is conflicted by others who have reported positive charges

under the exact same conditions [23, 68]. Current literature suggests that, generally, trimethylhafnium (TMHf) and tetrakis(dimethylamido)hafnium (TDMAH) precursors produce negatively charged films, whilst tetrakis(diethylamido)hafnium (TDEAH) results in positive charge polarity [20, 24, 25].

A summary of various reports on HfO_2 charge polarity can be found in Table 2.1. This table details the factors which have the potential to influence the charge. It should be considered that the metal contacting used for some measurement approaches may influence the resulting charge, and so have also been included in the table.

First author	Precursor	Substrate	Deposition	Ambient	Measurement	Polarity	q/cm^2
Singh [69]	TEMAH[a]	*n*-type FZ	Plasma (O_2)	N_2	CV	Positive	10^{12}
Singh [69]	TEMAH	*n*-type FZ	Plasma (O_2)	N_2	CV	Negative	10^{12}
Gope [68]	TEMAH	*n*-type FZ	Thermal (H_2O)	N_2	CV	Positive	10^{12}
Tomer [23]	TEMAH	*n*-type FZ	Thermal (H_2O)	N_2	CV	Negative	$<10^{11}$
Tomer [23]	TEMAH	*n*-type FZ	Thermal (H_2O)	H_2	CV	Positive	10^{12}
Tomer [23]	TEMAH	*n*-type FZ	Thermal (H_2O)	None	CV	Negative	10^{12}
Cui [21]	TEMAH	*p*-type FZ	Thermal (H_2O)	H_2/N_2	Corona/CV	Positive	10^{11}
Gougam [22]	TEMAH	*n*-type FZ	Thermal (H_2O)	Air	CV	Positive	10^{12}
Wang [26]	$HfCl_4$[b]	*n*-type FZ	Thermal (H_2O)	None	CV	Positive	10^{12}
Aubriet [67]	$HfCl_4$	*n*-type Cz	Thermal	N_2	KP/COCOS	Negative	10^{11}
Sreenivasan [20]	$HfCl_4$	*p*-type	Thermal (H_2O)	H_2/N_2	CV	Negative	10^{12}
Sreenivasan [20]	TDEAH[c]	*p*-type	Thermal (H_2O)	H_2/N_2	CV	Positive	10^{11}
Lin [25]	TMHf[d]	*n*-type FZ	Thermal (H_2O)	N_2	CV	Negative	10^{12}
Lin [25]	TMHf	*p*-type FZ	Thermal (H_2O)	N_2	CV	Negative	10^{12}
Cheng [24]	TDMAH[e]	*n*-type Cz	Thermal (H_2O)	-	COCOS	Negative	10^{11}
Wratten [70]	TDMAH	*n*-type Cz	Plasma (O_2)	Air	Corona	Negative	10^{12}
Pain [71]	TDMAH	*n*-type Cz	Plasma (O_2)	Air	Corona	Negative	10^{12}

(a) tetrakis(ethylmethylamido)hafnium, (b) hafnium tetrachloride, (c) tetrakis(diethylamido)hafnium, (d) trimethylhafnium, (e) tetrakis(dimethylamido)hafnium

Table 2.1: Existing literature reporting on the charge polarity of HfO2 thin films. This table includes deposition, post-deposition, and measurement variables that have the potential to influence the resulting measured charge of a sample.

It is not just the charge polarity of HfO_2 that has been challenging to determine. There are also many conflicting reports about the optimal postdeposition annealing conditions for HfO_2 films. It should be noted that this report focuses on the optimal conditions specifically to maximise surface passivation quality, as described in Chapter 5. Table 2.2 includes examples of existing literature on HfO_2 passivation, including the post deposition annealing conditions used and the minority carrier lifetime, τ_{eff}, achieved.

Author	Publication Year	Annealing Temperature (°C)	Annealing Ambient	Wafer Type (Ωcm)	τ_{eff} (cm/s)
Lin [25]	2012	440	N_2	3.3 (n-type FZ)	24
Cui [21]	2017	350	N_2/H_2	1 (n-type FZ)	3.3
Cheng [24]	2017	450	-	1.0 (n-type (Cz)	11
Gougam [22]	2019	400	Air	1-5 (n-type FZ)	1.2
Tomer [23]	2020	400	H_2	5.0 (n-type FZ)	5

Table 2.2: A chronological report of some of the existing literature on HfO_2 passivating films. The post-deposition annealing conditions used in each publication are highlighted alongside the minority carrier lifetime, τ_{eff}.

2.4.2 Etching and patterning of HfO_2

In addition to its ability to passivate silicon, HfO_2, particularly crystalline HfO_2, is notoriously difficult to degrade. This has been demonstrated in its application as a protective layer against oxidisation, copper corrosion, and general weathering [27, 29, 30]. Understanding and controlling the etching behaviour of HfO_2 could prove very useful for integration into semiconductor devices, as both a protective barrier layer, utilising its strong etch resistance, and, potentially, as a patterned dielectric (should the etch resistance prove controllable). It should be noted that the etching rates of HfO_2 can vary substantially depending on the deposition methods utilised [72-75]. The existing literature on etching that is discussed in this section, and the experimental results presented later in this project, will focus solely on HfO_2 produced *via* atomic layer deposition.

Saenger *et al.* published a paper in 2002 on the etching of crystalline HfO_2 films using HF-based solutions [76]. Crystalline HfO_2 is very difficult to etch using wet chemical methods. However, through use of ion bombardment, the time taken for films to degrade from hydrophobic to hydrophilic was less than half that of a standard crystalline HfO_2 film. The degradation was performed *via* a wet etch, using a 5 % HF solution. In 2004, Lowalekar and Raghavan distinguished between as-deposited as heat-treated HfO_2 [77]. They found very low etch rates for heat-treated HfO_2, of <0.1 Å/min, which is supported by the results of Saenger *et al.* However, the as-deposited HfO_2 films, and other similar Hf-based films, could easily and quickly be etched in relatively low concentrations of HF.

In 2015, Lee *et al.* published a paper on the atomic layer etching (ALEt) of HfO_2 using HF and $Sn(acac)_2$ [78]. Not only did this allow for the linear and controllable etching of the HfO_2 films, but it also resulted in a decrease in surface roughness. This was supported by Murdzek and George in 2019, when they demonstrated ALEt of HfO_2 using HF and dimethylaluminium chloride (DMAC) [79]. They achieved etch rates of 0.08 Å/cycle and 0.68 Å/cycle for crystalline and amorphous HfO_2 respectively, and put forward the idea of creating high-quality ultra-thin films by etching back thicker crystalline films. The benefit of ALEt for etching films is that it uses an ALD system meaning that, theoretically, deposition and etching can be done using the same device.

If the etching of HfO_2 can be combined with a method of localised annealing, it may lead to a novel approach of creating patterned films. In 2013, Larkin *et al.* demonstrated that localised annealing of HfO_2 was possible, by irradiating the film using an e-beam with an electron dose of 106 e/nm^2 [80, 81]. During irradiation, the film slowing transitioned from amorphous to crystalline. In 2020, results published by Toshiyuki Tabata indicated that HfO_2 can be annealed via UV pulsed laser annealing [82]. From simulations, the temperatures reached in this process were ~1250 °C, which is much higher than the standard crystallisation temperature of HfO_2. However, the

aim of Tabata's paper was to produce cubic, rather than monoclinic, HfO_2 which may explain the need for such high temperatures.

A section of this work will attempt to investigate different approaches to producing localised regions of crystallised monoclinic HfO_2, in order to utilise both its etching characteristics and passivation properties to create patterned dielectrics for potential electronic and photovoltaic device applications.

Chapter 3

Methodology

This chapter details the various techniques that have been implemented throughout this project, including descriptions of the relevant systems and processes, as well as the theoretical principals behind them. Specific information relating to exact apparatus and recipes can be found within the relevant results chapters in which the techniques have been applied.

3.1 Sample processing

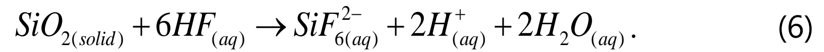
3.1.1 Wafer cleaning

For thin films to be deposited effectively onto a substrate the surface must first be appropriately prepared. Different substrates have different cleaning requirements and thus different cleaning recipes. There have been many different approaches to Si wafer cleaning, but one of the most common methods today is the RCA clean [83, 84].

RCA stands for 'Radio Corporation of America' and is a cleaning method that was developed by Werner Kern in the 1960's [85]. It is also sometimes called the standard clean (SC). An RCA1 solution is composed of de-ionised (DI) H_2O, NH_4OH, and H_2O_2, and is used to remove organic residue from wafers. RCA2 is composed of DI H_2O, HCl, and H_2O_2, and removes metal ions from the silicon. For most applications it is necessary to use both RCA solutions in a cleaning process.

Since both of these solutions leave a thin oxide layer on the surface, it is good practice to perform a dip in hydrofluoric acid (HF) after each step. HF is a colourless, odourless,

corrosive acid that is commonly used in silicon processing. Dilute HF solutions are able to etch native oxide layers on silicon via the following reaction [86, 87]:



$$SiO_{2(solid)} + 6HF_{(aq)} \rightarrow SiF^{2-}_{6(aq)} + 2H^{+}_{(aq)} + 2H_2O_{(aq)}. \quad (6)$$

This reaction leaves a hydrophobic hydrogen-terminated Si surface that provides temporary chemical surface passivation of the wafer [88].

Tetramethylammonium hydroxide (TMAH) is a salt with the chemical formula:

$$N(CH_3)^{+}_{4}OH^{-}. \quad (7)$$

Solutions of TMAH in water are a common approach for the anisotropic etching of Si wafers. Substrates of Si(100) can be etched to form square based pyramid patterns, as the TMAH will etch along the Si(111) planes. Etching rates and roughness of the Si surface can be controlled through the solution temperature and TMAH concentration, respectively. This etching step is often utilized to remove saw damage and smoothen the Si surface prior to surface passivation [89].

In addition to surface cleaning, it may be beneficial to texture a substrate before thin film deposition. Similarly to TMAH etching, random texturing of the Si surface can be achieved via wet or dry processing, such as KOH chemical etching and Reactive Ion Etching (RIE), respectively [90], though the resultant textures often vary in scale compared to the pyramids produced with TMAH. This randomised texturing increases the amount of light absorbed into the substrate, seen in Figure 3.1 [91], thus increasing generation of carriers. However, increasing surface area also increases the number of surface-state traps, thus passivation becomes even more important.

3.2 Fabrication

3.2.1 Atomic layer deposition

Atomic Layer Deposition (ALD) is a form of chemical deposition with a relatively slow growth rate, that is capable of producing ultrathin films of excellent uniformity and

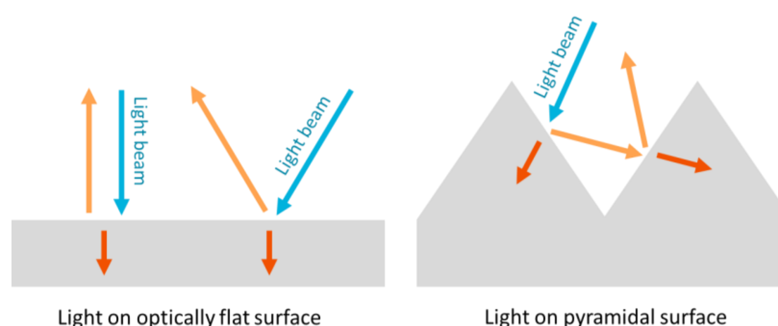


Figure 3.1: Schematic comparing light reflection on flat and textured surfaces. Arrows indicate the direction of light rays, with each interaction at the surface allowing for further absorption into the substrate. This image has been adapted from [91].

conformality, which can be performed at relatively low temperatures, especially if using an energy enhanced method such as plasma enhanced ALD (PE-ALD) [92-94]. This makes it a very attractive method for thin film growth, particularly in the fields of electronics and photovoltaics where high film quality is essential.

The rate of film growth can be split into two sections: a brief initial nucleation period (dependent on the film type and substrate), followed by a steady-state period. During the steady-state period the growth rate will typically be constant, however, this may differ in the initial stages of growth due to nucleation inhibition or enhancement [95]. The growth of thin films *via* ALD is therefore mainly controlled through the number of cycles completed. A cycle consists of sequential pulses and purges of each gas precursor. During each pulse the precursor reacts with the substrate until there are no reactive sites left on the surface, at which point the reaction terminates. This self-limiting behaviour produces a standard growth rate per cycle (GPC) and is what allows for excellent control over the film thickness. After each cycle there is a purge step which serves two purposes: to prevent the precursors from reacting with each other, and to remove any by-products of the precursor-substrate reaction from the chamber.

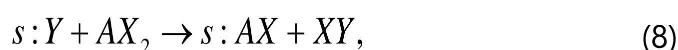
Typically the first precursor will be a type of metal whilst the second precursor, also known as the co-reactant, will be a non-metal such as oxygen or nitrogen. In order to maintain self-limiting growth it is essential that the chosen precursors are reactive

with the surface and leave reactive surface groups, but do not react with themselves, or with the surface groups they create.

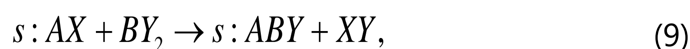
The deposition temperature must also be carefully selected in order to avoid additional processes occurring, such as decomposition, which may interfere with the steady self-limiting growth. The ideal temperature window for deposition is the range at which the GPC shows no temperature dependence [93].

As previously mentioned, the films produced by ALD show high uniformity and conformality. This is due to the self-limiting behaviour of the reactions. As long as there is sufficient flux into the reaction chamber, the precursor will interact with all available surface sites, creating an even thickness of film across the entire substrate, no matter the shape of the surface. If there is not sufficient flux the surface sites will not be saturated and the uniformity and conformality will become flux controlled.

The process of a single ALD cycle can be understood through these equations [93]:



$$s : Y + AX_2 \rightarrow s : AX + XY, \tag{8}$$



$$s : AX + BY_2 \rightarrow s : ABY + XY, \tag{9}$$

where s is the substrate with surface groups Y, A is the precursor with two ligands X, and B is the co-reactant with two ligands Y. XY is the reaction product. The process described in these equations is depicted in Figure 3.2 [92]. This is the simplest form of an ALD cycle. Including materials with more ligands or additional precursors can lead to more complex reactions on the surface. Examples of these multistep cycles and supercycles can be seen in Figure 3.3 [93].

Ligand exchange is not the only reaction type capable of facilitating ALD growth. Association is when a precursor remains intact and bonds with the surface without release of ligands. By contrast, dissociation involves the precursor being adsorbed to the surface in several smaller pieces. Combustion is the replacement of surface groups

with an oxidised surface; similarly with nitridation and nitride surfaces. Often a mixture of several different mechanisms will be involved in the ALD process.

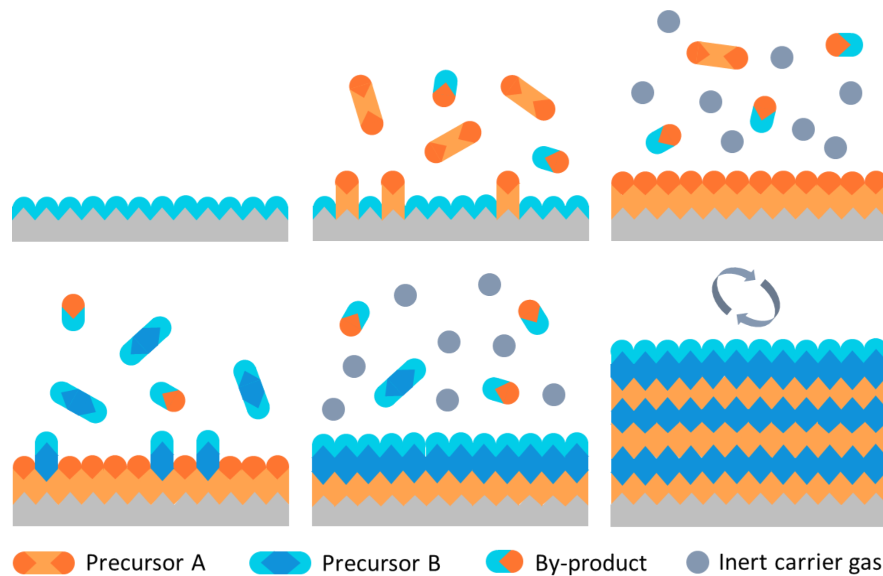


Figure 3.2: Depiction of the stages involved in a standard ALD cycle: (a) prepared substrate, (b) precursor A reacts with surface, (c) by-products are purged using carrier gas, (d) precursor B reacts with surface, (e) by-products purged using carrier gas, (f) cycle repeats. This figure has been adapted from Ref. [92].

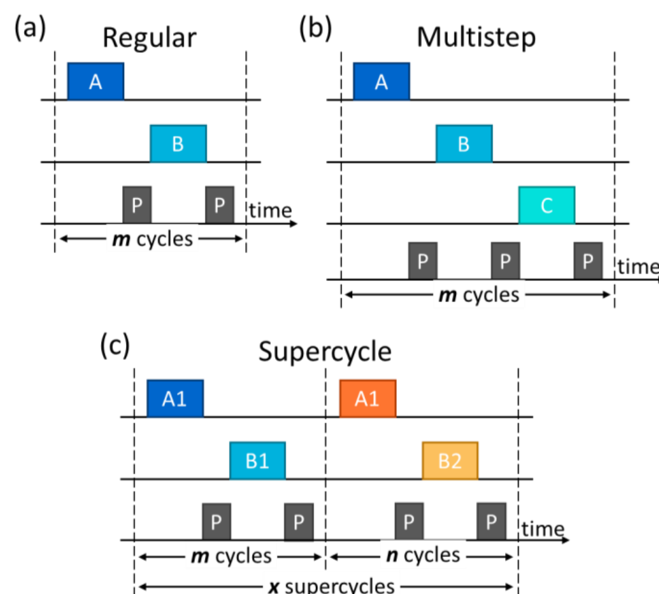


Figure 3.3: Depiction of various types of cycles possible through atomic layer deposition: (a) a standard cycle involving only two precursors, (b) a multistep cycle where more than two precursors are needed, and (c) a supercycle where a number of cycles involving one pair of precursors is followed by another set of cycles involving different precursors. This image has been adapted from Ref. [93].

3.2.2 Electron beam evaporation

Electron beam, or e-beam, evaporation is a form of physical vapour deposition in which electron bombardment is used to evaporate a target material under vacuum [96, 97]. The gaseous material will then precipitate and coat the entire surrounding area with a thin film, including any substrate placed within the chamber. Figure 3.4 shows a schematic of a typical e-beam evaporation system [98].

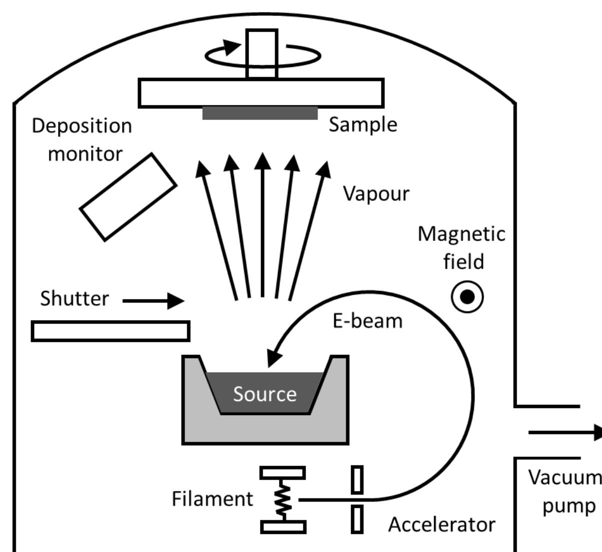


Figure 3.4: A schematic of a typical e-beam evaporation system, including a heated filament, e-beam path (as directed by magnetic field), target material, resultant vapour, and sample wafer, all within a vacuum sealed chamber [96, 98].

The electron beam is produced through use of a hot filament, usually tungsten, which causes the thermionic emission of electronics. The resultant e-beam is then directed, through use of a magnetic field, to the target material. The use of a magnetic field allows for the filament and source material to be kept physically separate from each other, helping prevent cross-contamination. The energy from the e-beam can then be directly transferred to the target, enabling evaporation of materials with high melting points. As such, e-beam evaporation can be considered a thermal evaporation process, despite no heat being applied to the rest of the crucible. The lack of heating to the chamber and, by extension, the substrate can reduce the possibility of heat damage to the substrate. However, it should be noted that e-beam evaporation can

instead cause ion implantation into the substrate which may reduce device performance.

Beneficially, e-beam evaporation has a high deposition rate and material utilization, which is particularly important when depositing rare and expensive materials such as gold (Au) [97].

3.2.3 Photolithography

Photolithography is a process by which light can be utilised to produced patterned thin films [99, 100]. This process relies upon the use of an optical mask containing a desired pattern. A photoresist will be spin coated onto a substrate, and then exposed to light (typically UV light) through the optical mask. Depending on whether the resist is 'positive' or negative' it will either harden or breakdown when exposed to the light. A developer can then be used to remove un-hardened areas of the resist. Depending on the photoresist used, heat-treatment may be required before or after light exposure; these are referred to as soft-bakes and hard-bakes, respectively.

There are two approaches to patterning thin films using photolithography. In the first approach the photolithography step is conducted straight onto the substrate. Once the patterned photoresist layer is in place, a deposition method, such as e-beam evaporation, can be used to deposit a thin film layer over the entire substrate. A solvent-based solution can then be used to remove the resist, and thereby lift off the thin film deposited directly over it. The second approach involves having a thin film layer already in place on the substrate. Once the patterned photoresist layer is in place, an etching solution can be used to selectively etch areas of the film not protected by the photoresist. The remaining photoresist can then be stripped away. A schematic of a typical photoresist process, using the second approach, can be seen in Figure 3.5.

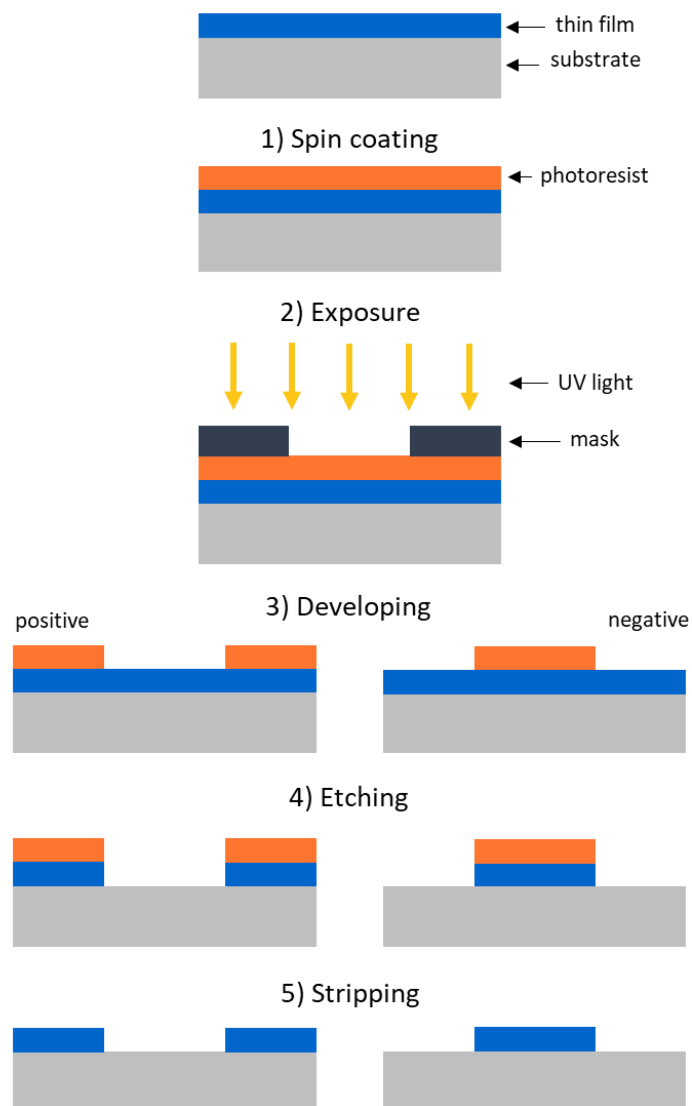


Figure 3.5: A schematic depicting a standard photolithography process, using UV light exposure. A comparison is made between the use of positive and negative photoresists. In this process a thin film layer is already in place and an etching solution is used to selectively etch back this film around the remaining photoresist, as determined by the pattern of the optical mask. This figure has been adapted from [100, 101].

Photolithography is particularly beneficial for its versatility, being compatible with most substrate materials, and allowing for patterning on scales differing by orders of magnitude. This process can be used for patterning with lateral resolutions as low as 1 µm [99]. However, although photolithography is highly valuable in a research environment, it does not necessarily translate well to an industrial scale due to the complexity and speed of the process, and the cost of equipment and materials.

3.3 Characterisation

3.3.1 Spectral reflectance

The thickness of thin films can be assessed using either a physical approach, such as a stylus technique, or an optical approach, such as reflectometry or ellipsometry. Optical approaches are generally preferred as they are simple processes, not requiring any sample preparation, and are non-destructive, as there is no direct contact with the sample [102].

Spectral reflectance is the simplest optical measurement technique. Light is shone perpendicular to a sample, over a range of different wavelengths, and the reflected light is measured and used to calculate certain material properties. Ellipsometry takes this a step further by measuring light with non-normal incidence, using two polarizations. As a consequence, ellipsometry is a more complex and expensive process. For the purposes of this project, reflectometry is sufficient in most cases.

When light crosses an interface between different materials, there are three possibilities that may occur: the light may be reflected, transmitted, or absorbed. In reality, there is usually a mixture of all three. It has long since been established that the angle that a ray of light will reflect off of a surface will be equal to the incident angle. This is known as the Law of Reflection, and can be described mathematically, through the following equation:

$$\varphi_r = \varphi_1 . \tag{10}$$

Snell's Law instead considers what will occur to light that is refracted:

$$n_1 \sin \varphi_1 = n_2 \sin \varphi_2 , \tag{11}$$

where the refractive index n provides a ratio of the speed of light in a vacuum to the speed of light in a given material. In this case n_1 is the refractive index of the medium, and thus φ_1 is the angle of incidence, where as n_2 and φ_2 denote the refractive index of the target material and the angle of refraction, respectively. This can be seen in Figure 3.6.

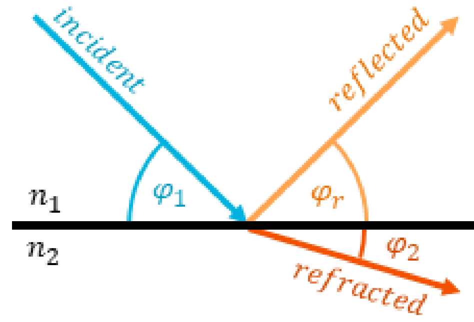


Figure 3.6: A visual representation of light interacting with the interface between two different mediums, according to Snell's Law and the Law of Reflectance.

Reflected wavelengths may combine either constructively or destructively, depending on the phase difference. The principal of linear superposition was first proposed by Thomas Young in 1801 [103]. This interference behaviour is possible due to the periodicity of electromagnetic waves, whereby there exists points in space and time where the waves appear identical. The distance between successive identical points is called the wavelength, λ. The Fresnel equations consider the resultant amplitudes of light rays that have been either reflected or transmitted. The coefficients relating to the reflected light are as follows:

$$r_s = \frac{n_1 \cos\theta_i - n_2 \cos\theta_t}{n_1 \cos\theta_i + n_2 \cos\theta_t}, \tag{12}$$

$$r_p = \frac{n_2 \cos\theta_i - n_1 \cos\theta_t}{n_2 \cos\theta_i + n_1 \cos\theta_t}, \tag{13}$$

where n is the refractive index for each material at the interface, θ_i is the angle of incidence, and θ_t is the angle of transmission. The reflectance coefficients r_s and r_p consider the electric and magnetic components of the wave, respectively. These equations can be derived from first principals using both macroscopic and microscopic approaches [104-106].

Reflectance can be defined as:

$$R = \frac{A + B\cos\left(\left(4\pi/\lambda\right)nd + \Phi\right)}{C + B\cos\left(\left(4\pi/\lambda\right)nd + \Phi\right)}, \tag{14}$$

where n is the refractive index of the thin film material, d is the thickness of the layer, and Φ is the phase shift, which is dependent upon light absorption in the material. The factors A, B, and C are all some combination of Fresnel reflectance coefficients for the medium, the thin film, and the substrate [107, 108].

In practice, this equation should be evaluated for a range of wavelengths, as the refractive index of a material is often wavelength dependent; this is known as dispersion. A films material properties can be extracted through application of a mathematical model, whereby the reflectance spectra for a range of wavelengths is calculated based upon trial values, which are then adjusted until the measured and calculated reflectance values align. The adjustable parameters may include the film thickness, the refractive index, and the extinction coefficient, which provides information on the amount of light absorbed by the material.

There are some limitations to the use of spectral reflectance. If a film is very thin, such that there is less than one reflectance oscillation, there will be less information available to determine the adjustable model parameters. Generally, the minimum single-layer thickness that can be measured using spectral reflectance is in the range of 1 nm to 30 nm, depending upon material, wavelength range, and number the of adjustable parameters in the model. This thickness limitation increases further when addition films are incorporated into the measurement. Most films discussed in this work have thicknesses in the range of 10-30 nm, and appear either as a single layer or as a two-layer stack; thus spectral reflectometry is sufficient to determine accurate values of film thickness.

3.3.2 X-ray diffraction

A crystallised material is composed of unit structures that are repeated across three dimensions in a periodic manner, creating a lattice structure with long-range order. Each unit cell contains all the atoms and chemical bonds necessary to describe the full structure, and has dimensions a, b, and c along the x, y, and z axes. No two

materials have exactly the same unit cell dimensions, and so the angles at which light diffracts off of every crystal structure is unique.

Diffraction occurs most strongly when wavelengths are of a similar magnitude to the physical structure they interact with; for crystals structures, x-ray radiation is most appropriate. X-ray diffraction (XRD) techniques rely on cathode ray tubes to create monochromatic x-ray radiation, which is then collimated and directed towards a crystallised sample [109]. A schematic of a typical XRD setup can be seen in Figure 3.7.

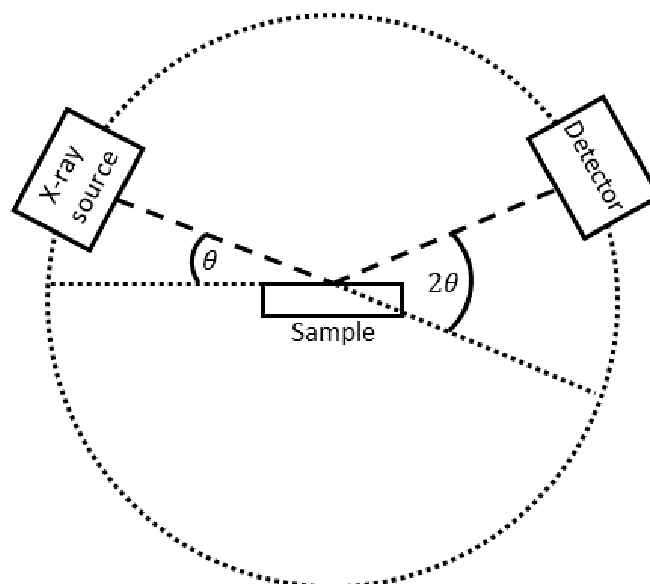


Figure 3.7: A schematic of a typically x-ray diffractometer, including a cathode ray tube x-ray source, x-ray detector, and a sample around which the source and detector will rotate with scattering angle 2θ.

XRD produces unique intensity patterns, generated by the interactions between incident x-ray beams and atoms within a lattice [110, 111]. When an x-ray interacts with electrons in a target atom, energy is transferred, and the electron moves to a higher energy level. As higher energy electrons then move to fill the vacancies created by the excited electrons, they emit photons with the energy equivalent to the energy transition in the levels. These energy levels are finite and are unique to for each material. The emitted photons behave like spherical waves, diffracting off of the crystal structure and interfering with each other, creating peaks in intensity in certain

directions where the waves interfere constructively. This constructive interference is called Bragg reflection, and occurs when the phase difference between two waves, i.e. the distance between two scattering points or planes, is equal to an integer number of wavelengths. This can be described mathematically through the Bragg equation:

$$n\lambda = 2d \sin \varphi \tag{15}$$

where n is an integer, λ is the wavelength, d is the distance between planes, and φ is the angle between the lattice place and the incident beam. The amplitude of the resultant wave varies with the scattering angle 2θ.

There are several different approaches to XRD. The Laue method involves applying incident x-ray beams with a continuous range of wavelengths, which can provide information about the symmetry and orientation of a crystal. For the crystal rotation method, a sample will be rotated about one of the crystallographic axes. The technique that has been described in this work is called the powder method, and is one of the most commonly used forms of XRD today due to its ability to detect crystals with incredibly small grain sizes [112].

3.3.3 Photoconductance

Photoconductance measurements detect the change in conductivity of a material under illumination. A typical device setup, as depicted in Figure 3.8 [113], will include a light source directed at a target sample. A reference sample will be used to determine the illumination of the light source and a metal coil beneath the target sample measures its conductance.

When a semiconductor is exposed to a light source, the electrons in the bulk material become excited and transition from the valance band to the conduction band, creating electron-hole pairs; this is known as generation. Contrastingly, recombination is the process by which an excited electron moves to an unoccupied state in the valance band, eliminating electron-hole pairs. The generation rate, $G(t)$, within a sample, given as a function of time, t, can be calculated *via*:

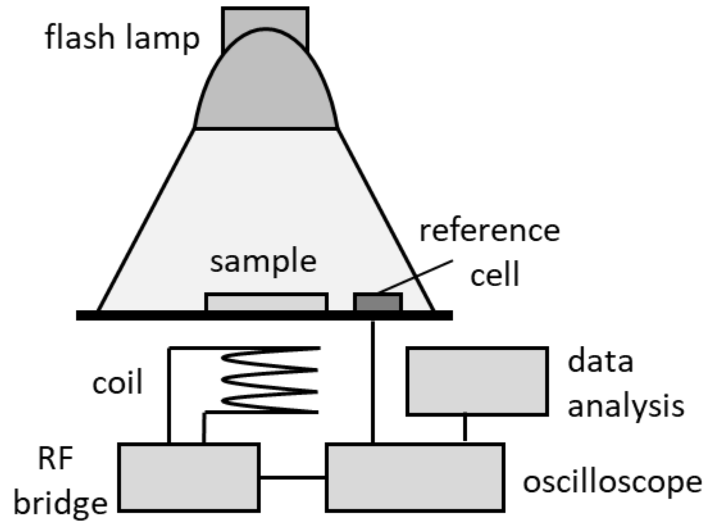


Figure 3.8: Schematic of a typical photoconductance decay measurement device, including a light source, metal coil, and reference sample [113].

$$G(t) = \frac{I(t) f_{abs} N_{ph}^{\odot}}{W}, \tag{16}$$

where $I(t)$ is the illumination intensity, W is the thickness of the sample, f_{abs} is the fraction of incident photons absorbed by the sample, and $N_{ph}^{\odot}$ is the flux of photons with an irradiance of 1 sun (1000 W/m^2) which generate electron-hole pairs. The average density of the excess carriers generated, $\Delta n(t)$, is given by:

$$\Delta n(t) = \frac{\Delta \sigma(t)}{q(\mu_n + \mu_p)W}, \tag{17}$$

where $\Delta\sigma(t)$ is the excess photoconductance of the sample, and μ_n and μ_p are the electron and hole mobilities, respectively.

The effective lifetime, τ_{eff}, of a sample indicates how long generated carriers will typically last before recombining, and is described mathematically through the following continuity equation:

$$\tau_{eff}(\Delta n) = \frac{\Delta n(t)}{G(t) - \frac{\partial \Delta n(t)}{\partial t}}. \tag{18}$$

However, this differential equation is very challenging to solve. There are two main approaches to simplifying this problem: quasi-steady-state (QSS) and transient measurement modes.

In transient mode a very short flash is used, such that the vast majority of the photoconductance measurement is taken in the dark. As such, it can be assumed that no generation processes are occurring during the measurement, and the $G(t)$ term is negligible. This approach is fast and simple, relying on fewer variables. As a result of this, however, these measurements are strongly impacted by lateral inhomogeneity in the sample. Typical measurement uncertainties for transient measurements, with $\Delta n \sim \mathcal{O}(10^{15})$, are ± 8 % [114].

With QSS measurements it is assumed that there is no time dependence to the excess carrier density of the sample, justified by the application of a prolonged "slow" flash. The $\partial \Delta n(t)/\partial t$ term can this be eliminated from the above equation. However, this approach still requires the calculation of the generation rate which, by extension, requires f_{abs}. In practice, this value is typically determined through an iterative process, whereby lifetime curves resulting from "fast" and "slow" flashes are compared, and f_{abs} altered until the curves match. Measurement uncertainties for this approach, with $\Delta n \sim \mathcal{O}(10^{15})$, are around ± 11 % [114]. Figure 3.9 shows a comparison between transient and QSS mode measurements [113].

There are several different mechanisms through which carriers may recombine, either through intrinsic processes involving band-to-band transitions, or extrinsic processes that that occur due to defect centres within the bandgap. In radiative recombination processes, the excess energy resulting from an excited electron transitioning from the conduction to valance band will be released in the form of a photon. With Auger-Meitner recombination, previously known as Auger recombination [38], this excess energy is instead transferred to another carrier. These are both examples of intrinsic mechanisms, though an extrinsic variant of Auger-Meitner recombination is possible, known as trap-assisted Auger-Meitner recombination. The process of recombination

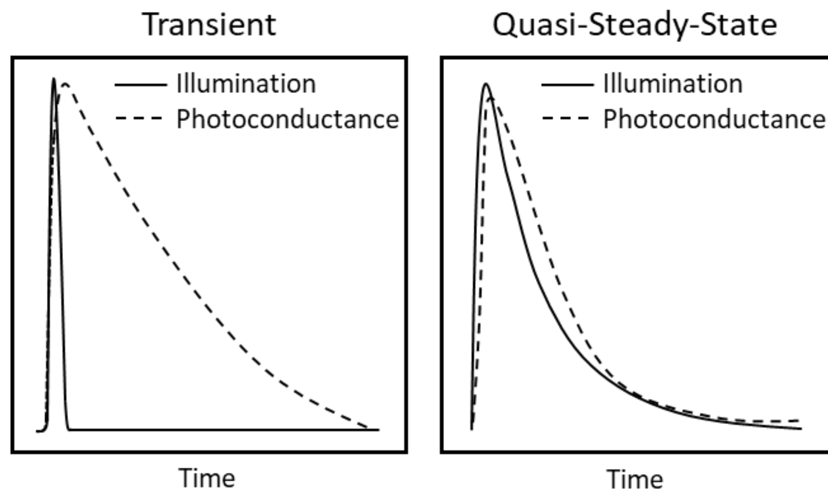


Figure 3.9: *A comparison between illumination and photoconductance intensities for (a) transient) and (b) quasi-steady-state modes of photoconductance decay measurements. This figure has been adapted from Ref. [113].*

via intermediate energy levels in the band gap is known as Shockley-Read-Hall (SRH) recombination. Such recombination affects are a result of impurities and lattice defects within the bulk crystal structure, as well as surface recombination states resulting from dangling bonds at the wafer surface.

Defect levels within the bandgap can interact with carriers in the conduction and valance bands in several different manners. In some cases an electron from the conduction band and a hole from the valance band will be captured by the defect level and mutually annihilate; this is known as a recombination centre. The inverse of this is called a generation centre. In the case of a trap centre, a carrier is captured by the defect centre and then returned to its original state. Such states will interact solely with either the conduction band or valance band carriers.

The effective lifetime of a material can thus be considered as a combination of affects from the various recombination processes within the surface and bulk material.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} + \frac{2S}{W}, \quad (19)$$

where the final term on the right accounts for surface recombination affects, considering the sample thickness, W (cm), and the surface recombination velocity of carriers, S (cm/s). The τ_{rad}, τ_{Aug}, and τ_{SRH} terms correspond to contributions from radiative, Auger-Meitner, and Shockley-Read-Hall recombination, respectively.

3.3.4 Kelvin probe

Kelvin probe is a non-contact method of measuring the work function of metals and semiconductor materials to a micron-scale resolution. This approach relies on creating a parallel plate capacitor though the suspension of an oscillating measurement tip above a sample, thus forming two electrodes. Electrical contact is made between the two electrodes, resulting in a potential gradient known as the contact potential, V_c. A backing potential, V_b, is then applied. Figure 3.10 shows a schematic of this [115].

Traditionally this backing potential is set such that $V_b = -V_c$, to produce a null output signal. However, null measurements are often heavily influenced by noise, and so many modern Kelvin probe setups intentionally take off-null measurements, and then extrapolate from this using the Baikie method [116].

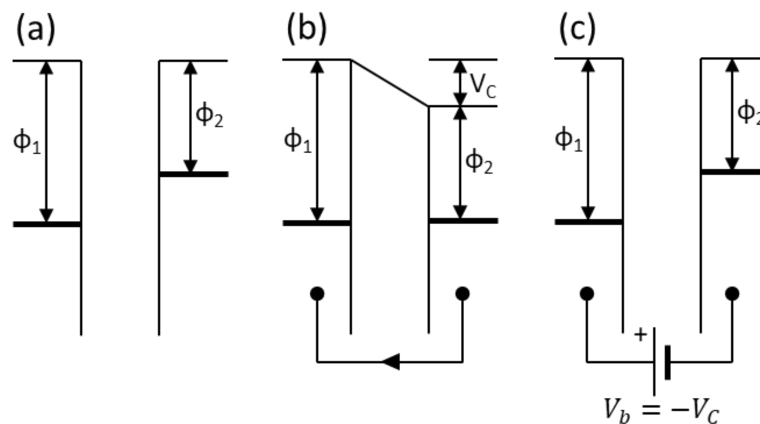


Figure 3.10: (a) An energy band diagram of two materials, representing a measurement tip and a sample, with ϕ_1 and ϕ_2 being the respective work functions of each material. (b) Electrical contact made between the materials, with potential gradient V_c. (c) A backing potential, V_b, applied to the circuit. This image has been adapted from Ref. [115].

For semiconductor materials, the work function (WF) of a sample can be determined by measuring the contact potential difference (CPD) and then performing a linear translation, using the work function of the measurement tip.

$$WF_{sample} = WF_{tip} + CPD \tag{20}$$

In the case of stacked materials, such as a dielectric thin film deposited on top of a semiconductor substrate, the resultant 'effective' work function can be obtained by considering the setup as a series of parallel plate capacitors [117].

$$CPD = \varphi_{metal} - \varphi_{insulator} - \varphi_{semiconductor}\,, \tag{21}$$

where φ_{metal}, $\varphi_{insulator}$, and $\varphi_{semiconductor}$ are the potentials across the metal measurement probe tip, the dielectric, and the semiconductor, respectively. A band diagram depicting a semiconductor and positively charge dielectric can be seen in Figure 3.11.

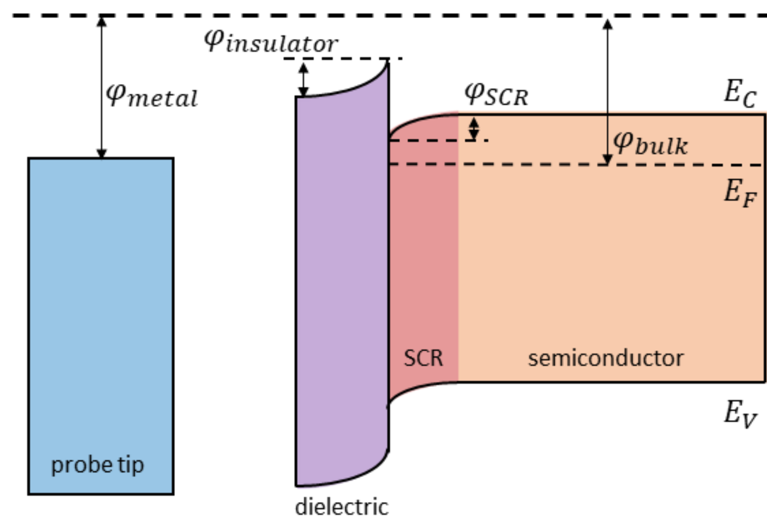


Figure 3.11: Band diagram of a semiconductor and positively charged dielectric stack, alongside a metal probe tip. Potentials across each region are labelled, as well as conduction and valance bands, and the Fermi energy.

The potential of the metal probe tip is equivalent to the work function of the probe material:

$$\varphi_{metal} = \Phi_m\,. \tag{22}$$

In the semiconductor, a surface charge region (SCR) is generated at the interface between the semiconductor and dielectric, resulting from charge carriers in the semiconductor mirroring the opposing charge carriers within the dielectric layer. Thus, the potential in the semiconductor is equal to the combined potential across the bulk and the surface charge region, with the bulk potential being equal to the work function of the semiconductor:

$$\varphi_{semiconductor} = \varphi_{bulk} + \varphi_{SCR} = \Phi_s + \varphi_{SCR} . \tag{23}$$

The potential across the insulator, or dielectric, is equivalent to the voltage difference across a parallel plate capacitor with a dielectric layer:

$$\varphi_{insulator} = \Delta V_i = \frac{x_c Q_f}{\kappa_i \varepsilon_0} , \tag{24}$$

where κ_i is the dielectric constant, also known as the relative permittivity of the dielectric, ε_0 is the permittivity of free space, and the charge distribution is approximated using a Dirac-delta function where the effective charge density, Q_f, is located at a distance, x_c, from the interface. Thus the contact potential difference reveals information on both the work function of the semiconductor, and the fixed charge within the dielectric layer:

$$CPD = \Phi_m - \Phi_s - \varphi_{SCR} - \frac{x_c Q_f}{\kappa_i \varepsilon_0} . \tag{25}$$

It is important to take into consideration that the dielectric constant of a material is not always fixed. Shifts in 'effective' work function may be due to changes in the charge of the dielectric layer, but may also result from structural changes which influence the dielectric constant.

Contact potential difference measurements are typically taken in the dark, thus eliminating photoexcitation mechanisms. Under illumination the number of free charge carriers increases, thus altering the potential across the SCR. Surface photovoltage (SPV) considers the difference in contact potential difference between measurements in darkness and under illumination, which can reveal information on barrier heights [118] and interface defects [119].

3.3.5 Corona charging

Corona charging involves the ionization of air around an electrode through application of a voltage. In a typical corona charging setup a point electrode, held at a fixed voltage, will be suspended a distance above a sample which has been grounded using a plate electrode. The ions generated in the immediate area around the point electrode will then drift, following the electrical field lines, downwards and are deposited onto the surface of the sample, as shown in Figure 3.12. The average corona charge deposited onto the surface over time can be approximated via

$$Q_{Cavg} = \frac{1}{A_C}\int_0^{t'} I_C dt = \frac{1}{A_C} I_C t', \tag{26}$$

where I_C is the current, and A_C is the effective area where the ions will land, approximated using Warburg's law [120].

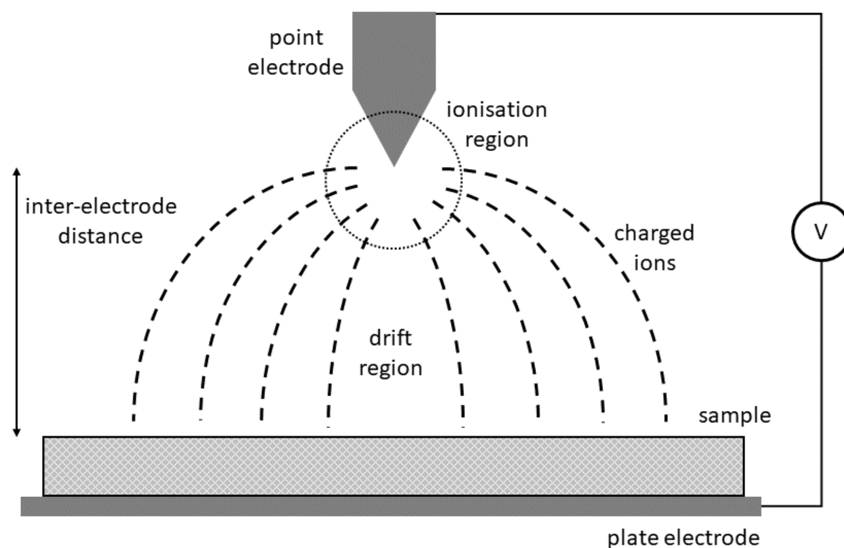


Figure 3.12: Schematic of an example corona charging setup, whereby a voltage applied to an electrode, results in the generation of charged ions which are then deposited onto the surface below.

In the field of dielectrics, corona charging can be used to enhance field effect passivation, assuming the extrinsic corona charge and intrinsic dielectric charge have the same polarity [121, 122]. With opposite charge polarities the field effect can instead be negated [123, 124].

As opposing extrinsic charge is deposited onto the surface of the dielectric it neutralises the charge within the dielectric layer and the field effect reduces. By extension, the effective lifetime is also reduced. The lifetime will continue to decrease until the field effect is fully neutralised, and will then start to increase again as further charge is added. The amount of charge required to reach this minimum lifetime point provides a qualitative indication of the amount of charge initially present within the dielectric. Figure 3.13 shows this affect occurring, using simulated SRV measurements of positive corona charge deposited onto a negatively charged Al_2O_3 layer [124]. Considering that there are no field-effect passivation mechanisms occurring at this point, the minimum lifetime, or maximum SRV, reached is an indication of the chemical passivation provided by the dielectric. Though this cannot provide a quantitative description, it can highlight relative changes in chemical passivation quality between samples.

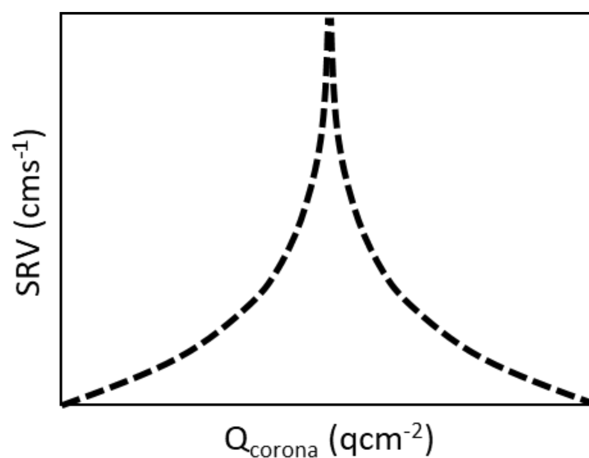


Figure 3.13: *Simulated SRV values, S_{eff}, for positive corona charge deposited onto a sample consisting of a negatively charged dielectric layer deposited onto an n-type crystalline silicon wafer, adapted from Ref. [124].*

The combination of a corona charging setup with in-situ kelvin probe measurements can be used to investigate Flatband voltages, dielectric capacitance, and interface state densities; this is known as the COCOS method [125].

3.3.6 Expanded Cox and Strack method

The Cox and Strack method (CSM) is an approach used to calculate the contact resistance of thin films [126]. Contact resistance considers the total resistance resulting from interfaces between a device and the point where electrical contact is made to the rest of the circuit. This method has become particularly prominent in the field of photovoltaics, where device structures consist of numerous thin film architectures [127].

The necessary device structure to conduct CSM consists of a full coverage rear contact and circular front contacts, varying in size. The exact material used for these contacts will depend upon the device itself.

In CSM, total resistance of a device and contact structure, R_T, is defined as

$$R_T = R_C + R_S + R_0, \tag{27}$$

where R_C is contact resistance, R_S is spreading resistance within the substrate, and R_0 is residual resistance from the full coverage rear contact, which is presumed negligible. Spreading resistance is defined by

$$R_S = \frac{\rho}{d\pi}\tan^{-1}\left(\frac{4t}{d}\right), \tag{28}$$

where ρ is substrate resistivity, t is substrate thickness, and d is contact, or diode, diameter. Contact resistance is defined by

$$R_C = \frac{\rho_c}{\pi\left(d^2/4\right)}, \tag{29}$$

where the contact resistivity, ρ_c, is the desired output.

Traditional CSM applies to Ohmic contact structures. However, for photovoltaic devices in particular, a Schottky heterojunction is more common. To account for this, Cheung’s method of calculating resistance for Schottky contacts can be applied [128, 129]. Following Cheung’s method

$$\frac{d(V)}{d(\ln I)} = R_T I + \frac{nq}{kT}, \tag{30}$$

where n is an ideality factor, q is the charge of an electron, k is the Boltzmann constant, and T is temperature. Thus R_T is the gradient of a plot with $d(V)/d(lnI)$ on the y-axis and I on the x-axis. Combining these two methods gives the Expanded Cox and Strack (ECSM) method, where ρ_c is the gradient of the plot of $R_T - R_S$ by $1/S$, where the diode area $S = \pi d^2/4$.

To apply this method a region of data after the threshold voltage should be selected, for example, the dashed black box in Figure 3.14(a). From there, a linear fit should be made of $\mathrm{d(V)/d(lnI)}$, to obtain values for $\mathrm{R_T}$. This step will likely require smoothing of the original data, as small fluctuations become greatly magnified as can be seen in Figure 3.14(b). The gradients of each of these linear fits should then be plotted on a graph of $\mathrm{R_T - R_S}$ vs $1/S$ as previously described. The gradient of the linear fit of these data points, as visualised in Figure 3.14(c), will give the contact resistivity of the measured sample. It should be noted that Figure 3.14 only provides a visual representation of the process, and the data and fitting provided should not be considered accurate.

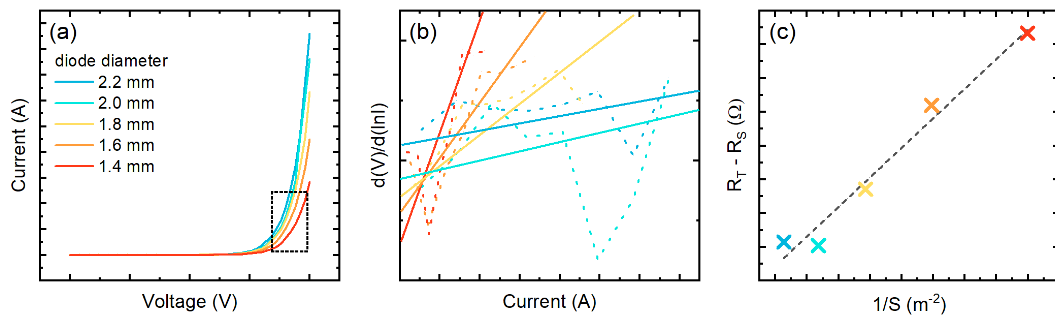


Figure 3.14: Examples of graphs used in the application of the ECSM. (a) Raw current-voltage data, with a dashed black box highlighting the range of data used for further steps in the process. (b) Linear fits over the raw data of $d(V)/d(lnI)$ vs I, resulting in values for R_T. It should be noted that while data smoothing has not been visualised in this figure, it was still applied before data fitting. This is necessary due to the high levels of noise in the data (this is particularly true for the blue and green fits). (c) A plot of $R_T - R_S$ vs $1/S$, with the gradient of the linear fit providing the final contact resistivity value.

Chapter 4

Controllable Etch Resistance in HfO_2 Thin Films

Thin film dielectrics are ubiquitous in the manufacture of electronic devices and are frequently deposited and etched away at various stages of device fabrication. This chapter demonstrates that hafnium oxide (HfO_2) thin films grown *via* ALD on silicon, and silicon pre-coated with aluminium oxide (Al_2O_3) have etch resistance properties which can be tuned simply by changing the post-deposition annealing temperature. The etching rates of films in hydrofluoric acid (HF) solutions were found to be dependent upon annealing temperature, with the etch rate decreasing with increasing temperature. A transition region in the etch rate was identified between 300 and 350 °C, corresponding to the crystallisation of the HfO_2 films, as identified *via* X-ray diffraction. HfO_2 films deposited directly onto silicon annealed above 350 °C were resistant to 10% HF solutions over the course of several hours. In the case of $Si/Al_2O_3/HfO_2$ stacks, closer inspection reveals the existence of channels which reduces etch resistance to HF, as evidenced by TMAH etching of the silicon substrate. Crystallized HfO_2 can be used to protect other dielectrics in device processing, and this chapter demonstrates its use in single-sided fabrication of patterned structures of Al_2O_3 which can control the effective charge-carrier lifetime in silicon wafers for use in modulating THz and mm-wave radiation.

4.1 Motivation

The manufacturing of semiconductor devices often requires the deposition and selective removal of thin-film dielectric layers. As such, it is vital to have a portfolio of

dielectrics available with different etch resistances. Hafnium oxide (HfO_2) is a versatile material with applications in areas ranging from the high-temperature extreme environments of refractory ceramics [29] to sensitive structures for microelectronics [130]. As a high-*k* dielectric [131], it has been well established that HfO_2 is capable of enhancing the performance of transistors [132] and capacitors [133] and, beyond this, has been found to have useful anti-reflective [134] and surface passivating properties [70],[71]. Interestingly, HfO_2 is also remarkably robust, having demonstrated resistance to oxidation [29], copper corrosion [30], and general weathering [27]. Understanding and controlling the robustness of HfO_2 would enable the utilization of these films as protective barrier layers in semiconductor processing. It may also be possible to create smooth and uniform ultrathin (~ 1 nm) films by etching back thicker films without incurring the surface roughness and nucleation defects issues which occur in the direct growth of films at the single nanometre scale [135].

This chapter determines the conditions under which HfO_2 grown by ALD has etch resistance. ALD is a low temperature process that allows for precise control and conformality of thin films [92-94]. The potential for low thermal budget depositions, combined with the compatibility with existing industrial processes makes ALD an attractive approach for thin film deposition. ALD systems can also be used for the selective removal of thin films, known as atomic layer etching (ALE). ALE allows for fine control over etching rates, but has the potential to result in surface damage, as with the case of plasma-etching [136], or requires a higher temperature operating window, as with thermal-ALE [137]. As such, this chapter instead focuses on investigating the wet chemical etching behaviour of HfO_2 films, as a less destructive, lower temperature alternative. Utilizing plasma-enhanced ALD and low/room temperature wet chemical etching could provide a low-thermal budget approach to ultrathin film growth.

The primary aim of this chapter is to demonstrate the capabilities of HfO_2 as a controllable protective layer for electronic and photovoltaic device processing. As such, several solutions commonly used in silicon processing are investigated as

potential etchants. This includes standard clean 1 (SC1 or RCA1), standard clean 2 (SC2 or RCA2), tetramethylammonium hydroxide (TMAH), and hydrofluoric acid (HF). Where previous works have focused solely on HfO_2 layers deposited directly onto silicon [77, 79], this chapter also investigates the etch resistance of HfO_2 that has been incorporated into $Si/Al_2O_3/HfO_2$ stacks. It is important to establish whether, in addition to protecting silicon, HfO_2 is also able to protect other sensitive dielectrics. This diversifies the ways in which HfO_2 protective layers may be incorporated into complex electronic device structures.

The results of this investigation have already proven useful in the development of devices for the modulation of THz and mm-wave radiation. HfO_2 films have been utilized to protect passivating Al_2O_3 layers on the rear of samples as they undergo patterning processes necessary for modulation [138]. A case study for the use of HfO_2's etch resistance is provided at the end of the chapter in section 4.5.

4.2 Experimental details

This section reports specific details detailing to the apparatus and experimental processes utilised within this chapter. For general information relating to methodology and theory, please refer to Chapter 3.

4.2.1 Sample Fabrication

Si/HfO_2 and $Si/Al_2O_3/HfO_2$ stacked layers were deposited onto mirror polished silicon (100) wafers, cut to 5 × 5 cm squares, *via* plasma-enhanced ALD (PE-ALD) using a Veeco Fiji G2 system. Before deposition, the silicon wafers were cleaned using established processes [89], starting with immersion in an RCA1 solution, consisting of de-ionized (DI) H_2O, NH_4OH (30 %), H_2O_2 (30 %) in a 5:1:1 ratio. This was then followed by an RCA2 solution: DI H_2O, HCl (37 %), H_2O_2 (30 %) in a 5:1:1 ratio. Both solutions were heated in a water bath to approximately 80 °C, with the H_2O_2 only added immediately before sample immersion. The samples spent 10 minutes in each

solution, preceded by a DI water rinse and a 60 s 1 % HF dip each time. The clean was completed with a final DI water rinse and 2 % HF dip. Each sample was individually dipped until it could be pulled dry from the HF solution, and was then immediately transferred to the ALD stage.

Depositions were performed at 200 °C, using O_2 plasma as the co-reactant, and argon as the inert carrier gas. To produce HfO_2 films, a tetrakis(dimethylamido)hafnium (TDMAH) precursor was pulsed for 0.25 s, followed by 6 s of O_2 plasma at 300 W, with a 5 s purge step before and after each. Al_2O_3 films were produced by pulsing a trimethylaluminium (TMA) precursor for 0.06 s and O_2 plasma for 6 s at 300 W, purging for 4 s between each step. For single layer samples, 200 process cycles of HfO_2 were deposited on each side of the wafer. This was preceded by 160 cycles of Al_2O_3 for the $Si/Al_2O_3/HfO_2$ samples. Samples were then either left in their as-deposited state, or annealed *ex-situ* in air for 30 minutes using a quartz tube furnace at temperatures ranging from 250 °C to 400 °C.

4.2.2 Characterization

The etch resistance of the single and stacked samples was investigated through measurement of HfO_2 film thickness, using a Filmetrics F40 reflectometry tool. Point measurements were taken at five different locations on a sample, and the results averaged. Figure 4.1 shows an example of the five measured data points for eight nominally identical HfO_2 samples, measured separately. The scatter in the data for each sample provides an indication of sample uniformity, as well as measurement error. The variation in thickness from sample to sample highlights the limitations of this measurement setup in terms of reproducibility, despite the controlled environment. The results of these eight samples provides an average thickness of 27.6 with a standard deviation of ± 1 nm. However, when reproducibility and the advertised uncertainty of the Filmetrics F40 system are taken into account, an error margin of ± 3 nm is used. Conclusively, the initial HfO_2 and Al_2O_3 film thicknesses were measured to be approximately 27 nm ± 3 nm and 21 nm ± 3 nm, respectively.

It should be considered that the mathematical model implemented in the Filmetrics system assumes a constant density; it is therefore possible that measurement variations attributed to film thickness may also be influenced by changes in film density or surface roughness. This is discussed further in section 4.4.4.

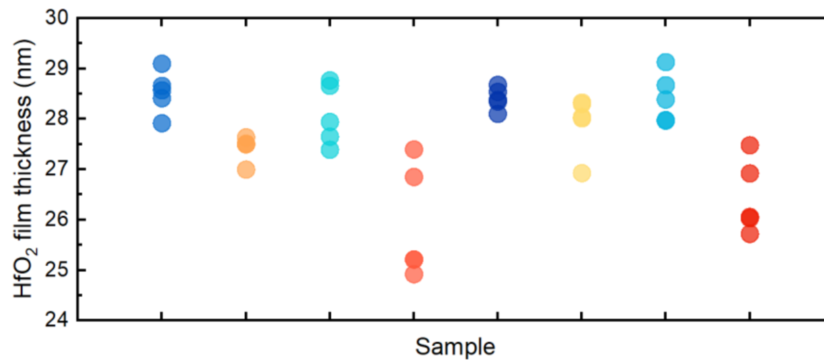


Figure 4.1: Data acquired from a Filmetrics F40 reflectometry system, measuring the thickness of HfO_2 films deposited on silicon. The results of eight different samples (colour coded) are compared, with five data points taken across each sample.

Samples were then submersed in one of the following solutions: RCA1, RCA2, 25 % TMAH, or 10 % HF. These are all solutions commonly used in the processing of silicon wafers. The RCA solutions were prepared as described for the initial cleaning process, the TMAH solution was heated to 80 °C, and the HF solution was kept at room temperature. At regular intervals the samples would be removed from solution and rinsed with DI water to pause the etching process, and the film thickness was measured.

Film crystallinity was investigated with grazing incidence X-ray diffraction (GI-XRD), using a 3rd generation Malvern Panalytical Empyrean XRD diffractometer, equipped with a Pixcel3D detector and multicore (iCore, iCore) optics providing Cu $K\alpha_{1/2}$ radiation. The sample surface was aligned to the direct beam to ensure that it was at the centre of rotation of the goniometer and the incident angle was set to 0.5°. 2θ measurements were made in the range 15° - 70° 2θ. The data was fitted using the Malvern Panalytical HighScore Plus data analysis software.

Atomic force microscopy (AFM) was performed on certain etched samples using a Bruker Dimension Icon microscope in PeakForce Tapping Mode, with a ScanAsyst-Air tip [139]. The resulting images were processed using Gwyddion 2.60.

4.2.3 Case study

To demonstrate the utility of HfO_2 in device processing, a case study of patterned surface passivation is provided. Samples were produced with Al_2O_3 on both the front and the rear of the Si substrate. HfO_2 was then applied to the back side only, to protect the rear Al_2O_3 layer from etching during the patterning of the front Al_2O_3 layer. In this part of the work photolithography was performed using a custom-made photomask. The mask consisted of 9 distinct 2.5 × 2.5 cm regions, with different filling fractions of periodic square holes. S1818 photoresist was spin-coated at 5000 rpm for 30 s, followed by a soft bake at 115 °C for 1 minute. The photoresist was then exposed for 3 s (equivalent to a dose of ~130 mJ/cm^2) in soft contact mode with 100 µm mask-wafer separation, using a Suss MicroTec BA8 Gen3 mask aligner. Following exposure, the photoresist was developed in an MF319 solution for 45 s, followed by a rinse in DI water. To protect the photoresist during wet chemical etching, a hard bake at 130 °C for 5 minutes was conducted following development. The resulting structure was then etched in a 2 % TMAH solution at room temperature for 25 minutes. Photoluminescence images were taken using a BT Imaging iLS-L1, with an exposure of 1 Sun (~1000 Wm^{-2}) for 5 s.

4.3 Wet chemical etching behaviour

This section investigates and compares the wet chemical etch resistance of HfO_2 films deposited directly onto silicon wafers (referred to as Si/HfO_2), and HfO_2 films deposited over an Al_2O_3 layer (referred to as $Si/Al_2O_3/HfO_2$), to various solutions commonly utilized in silicon processing.

4.3.1 HfO_2 and HfO_2/Al_2O_3 Chemical etch resistance

The wet chemical etch resistance of Si/HfO_2 samples kept in their as-deposited state (at 200 °C) are compared to samples annealed at 400 °C in air for 30 minutes. Figure 4.2 shows how the film thickness of HfO_2, as measured *via* reflectometry, varies with time spent in each of the solutions. As seen in Figure 4.2(a), (b), and (c), excellent resistance is demonstrated for samples in RCA1, RCA2, and TMAH solutions, with no change in film thickness observed after 1 hour, for both as-deposited and annealed samples. Remarkably, annealed Si/HfO_2 layers also shows no change in film thickness, even after 1 hour in a 10% HF solution (Figure 4.2(d)) This outperforms both SiO_2, which has an etch rate of 1 nm/s with the same HF concentration [140], and Al_2O_3 which has an etch rate of 0.8 nm/s in only 1% HF [141]. For a wet chemical etching approach to create ultrathin crystalline HfO_2 films to be viable, the use of higher concentrations of HF could be considered.

In contrast, rapid etching is seen in the as-deposited sample, as can be seen in the inset of Figure 4.2(d). This result is supported by the works of Murdzek *et al*. [79] and Lowalekar and Raghavan [77], who also noticed a significantly more rapid etch rate for as-deposited Si/HfO_2 samples compared to ones that had been heat-treated. The fact that it is possible to control the chemical etch resistance with a simple anneal treatment is investigated further in section 4.3.2.

Considering an intended application of this HfO_2 layer is to protect other dielectric layers from being etched, the wet chemical etch resistance of Si/Al_2O_3/HfO_2 stacks was also studied. As such, Figure 4.2 also shows the variation in thickness of HfO_2 films, deposited on Al_2O_3, during immersion in RCA1, RCA2, TMAH or HF solutions. In the first three solutions (Figure 4.2(a), (b), and (c)), stacked samples show a similar response to single layer HfO_2 films, in both the as-deposited and annealed cases. This would indicate that the integrity of the HfO_2 etch resistance to these solutions is not influenced by a layer beneath. Looking at the etch resistance to HF in Figure 4.2(d), similar etch rates between as-deposited single layer and stacked samples can be seen,

with rapid, linear etching in under 2 minutes. However, it is apparent that, once annealed, the inclusion of an Al_2O_3 layer reduces the etch resistance of the HfO_2 film to HF, with the $Si/Al_2O_3/HfO_2$ etching slowly over the course of several hours. The etching of the annealed $Si/Al_2O_3/HfO_2$ sample is much slower, less linear, and less uniform than in the as-deposited case, indicating that a different etching mechanism is responsible. It should be noted that, although reduced, the stacked sample still demonstrates a substantially increased etch resistance compared to an Al_2O_3 layer alone, and thus would provide sufficient protection in most chemical processing scenarios.

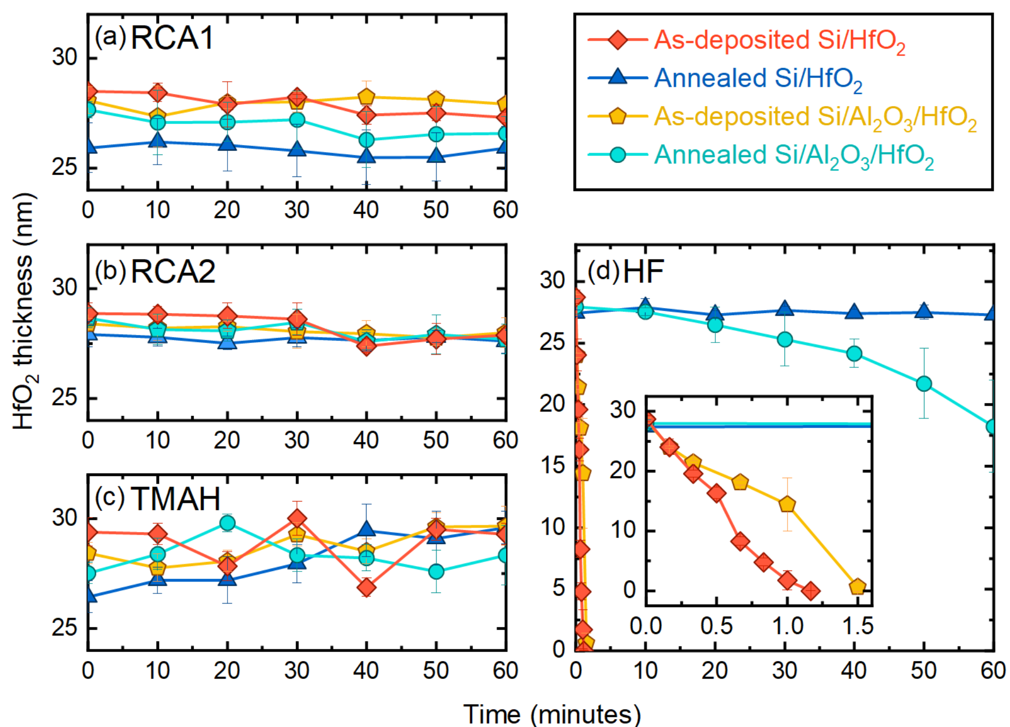


Figure 4.2: Measured thickness of HfO_2 films deposited on silicon and Al_2O_3 on silicon, as modelled via Filmetrics reflectometry, assuming a fixed thickness of Al_2O_3 beneath. Results are plotted as a function of time spent in a (a) RCA1, (b) RCA2, (c) TMAH (25%), or (d) HF (10%) solution. The inset in (d) shows the first 1.5 min of etching. As-deposited Si/HfO_2 (red diamond) and $Si/Al_2O_3/HfO_2$ (yellow pentagon) films are compared to samples annealed at 400 °C for 30 min in air (dark blue triangles, and light blue circles for single layers and stacks, respectively). It should be noted that these measurements may be influenced by limitations in the measurement setup, particularly the assumed fixed density and thickness of the Al_2O_3 layer.

It should be noted that for some samples, particularly the samples immersed in a TMAH solution, the thickness can be seen gradually increasing over time. This is, most likely, not a true description of the dielectric film thickness, but instead the result of residue on the surface. TMAH, in particular, is a very viscous solution. Figure 4.3 shows a close up of the HfO_2 film thickness of an annealed sample as it is immersed in a 25% TMAH solution. Film thickness appears to increase from around 26 nm to almost 30 nm. However, after a 10 s dip in a 10% HF solution, the film thickness then returns to its original value. It is likely that a DI water rinse was not enough to fully remove the TMAH, and so a residue was building up on the surface. The HF solution was then able to remove this residue, without etching any of the annealed HfO_2 film.

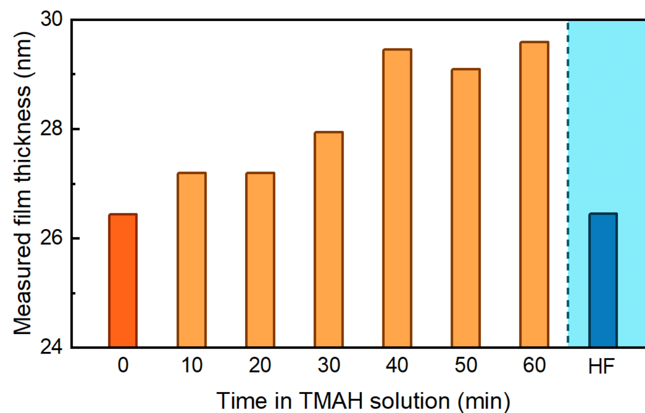


Figure 4.3: Thickness measurements of HfO_2 films deposited on silicon, measured via reflectometry, as a function of time spent in a 25% TMAH solution. The dark orange bar is the initial measured thickness before immersion in TMAH. The blue section highlights the measured thickness after the sample is immersed in a 10% HF solution for 10 s, following 60 min in TMAH.

4.3.2 Temperature dependence of HF etching

From Figure 4.2, it is clear that a post deposition annealing treatment substantially changes the wet chemical etching behaviour of the single- and double-layer dielectric films. Therefore, to investigate this dependence further, the etch resistance of Si/HfO_2 and Si/Al_2O_3/HfO_2 samples annealed at temperatures between 250 – 400 °C for 30 minutes is examined. In Figure 4.4 the results of this investigation, averaged across several repeated experiments, are plotted. For the Si/HfO_2 samples, Figure 4.4(a) demonstrates that etching occurs on three different time scales. Samples annealed

above 350 °C typically show no measurable sign of etching after 3 hours in a 10% HF solution, whilst samples annealed below 300 °C etch rapidly, being fully removed within a few minutes. Between these two temperatures there is a transition region, highlighted by the orange band, where samples etch slowly over the course of several hours. To the best of the authors' knowledge, this is the first time such a transition period has been identified in the wet chemical etch resistance of HfO_2 films. Etching of films annealed within this temperature region may provide a route to high-quality, non-amorphous, ultrathin HfO_2 layers, without the need for higher HF concentrations.

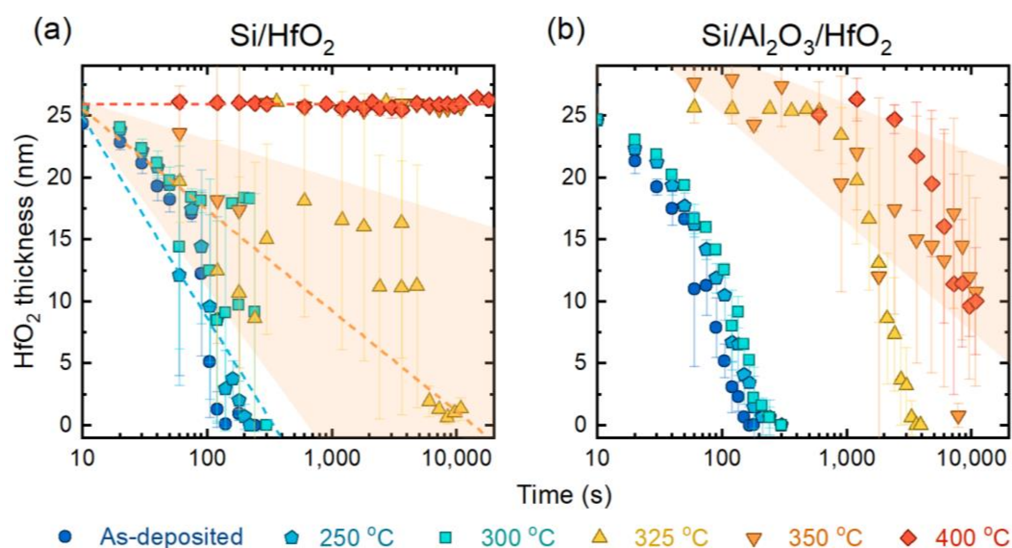


Figure 4.4: Thickness of HfO_2 films deposited at 200 °C on (a) silicon and (b) ~20 nm of Al_2O_3 on silicon, annealed at different temperatures, measured via reflectometry, as a function of time spent in a 10% HF solution. This data set is produced from averaging results across up to six repeated experiments. The orange shaded bands highlight areas of interest discussed in the main text.

Figure 4.4(b) shows the annealing temperature dependence of the etch resistance of stacked $Si/Al_2O_3/HfO_2$ samples to HF. A low-temperature region can again be identified, where films etch rapidly, as well as a transition region, between 300 and 350 °C, where films etch more slowly, similar to the single layer HfO_2 films shown in Figure 4.4(a). However, looking at the temperatures ≥350 °C, very slow etching of the stacked samples can be seen, as highlighted by the orange band. At these temperatures, where the single layer HfO_2 films showed complete resistance to etching, the corresponding Al_2O_3/HfO_2 stacked layers in Figure 4.4(b) do not. From

this, it can be inferred that the dependence of the underlayer on the etch resistance (in HF solutions) only becomes apparent once annealed at temperatures ≥350 °C.

4.3.3 Film crystallinity

To investigate any potential correlation between the etch resistance of the single or stacked samples and the crystallinity of the HfO_2 layer, GI-XRD is applied to samples that are annealed between 250 – 400 °C, with the patterns presented in Figure 4.5. From Figure 4.5(a), it can be identified that ~26 nm thick HfO_2 films on silicon crystallise between 300 and 350 °C. Below this temperature range, the HfO_2 films are primarily in an amorphous state, whilst above 350 °C clear peaks can be seen that correspond to a distinct crystal structure. These peaks have been indexed according to a monoclinic HfO_2 crystal structure [142].

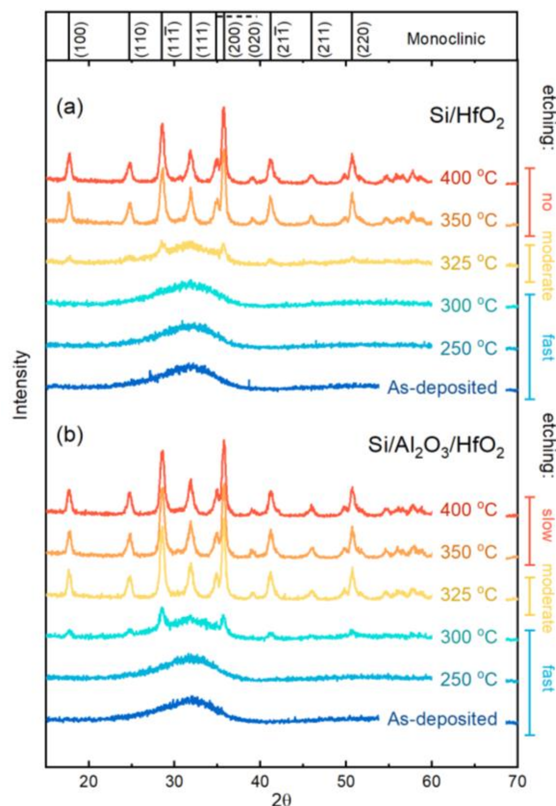


Figure 4.5: GI-XRD patterns, using a Cu K-α source, taken from samples of ~26 nm (200 cycles) of HfO_2 deposited (a) directly onto polished silicon, and (b) on polished silicon samples with a ~20 nm (160 cycles) Al_2O_3 interlayer. Samples were annealed in air for 30 min at temperatures ranging from as-deposited (200 °C) to 400 °C. Patterns have been vertically offset for clarity and the main crystallographic planes indexed at the top. The different regimes of etching are labelled on the right.

The variation in crystal structure with annealing temperature corresponds closely to the three stages of HF etch resistance observed in Figure 4.4, with amorphous samples etching quickly, crystallised samples showing no evidence of etching, and samples around the crystallisation region etching at an intermediate time scale. In contrast however, no notable distinction is seen in the crystal structure of HfO_2 on Al_2O_3 compared to HfO_2 on silicon, as shown in Figure 4.5(b). Thus, the etch resistance of the 400 °C annealed stacked samples is not related to differences in the crystallised structure of the HfO_2 layer itself.

4.4 Etching mechanisms

4.4.1 Physical damage

To investigate potential causes for variations in etching rates, it was first necessary to ensure that this difference in behaviour was not a matter of physical damage to the samples which could occur during handling. To examine this, a scratch test was conducted, whereby a sample of each type was scratched diagonally from corner to corner and placed alongside unscratched samples in a HF solution. The result of this investigation can be seen in Figure 4.6, which also includes a schematic of the scratch and approximate measurement points. Measurements were taken at varying distances from the scratch, but not directly over it. It is apparent that this degree of physical damage has no influence upon the etching behaviour of either the single layer Si/HfO_2 or the stacked Si/Al_2O_3/HfO_2 films. This demonstrates that the protective capabilities of HfO_2 are remarkably unimpeded by physical damage. It also implies that there must be other mechanisms responsible for the reduced etch resistance of high temperature stacked samples.

4.4.2 Pinholes

The possibility that the etching solutions are, in some way, travelling through the overlaying films to the underlying substrate is next considered. It has been well established that TMAH etching solutions create distinct square-based pyramid etch

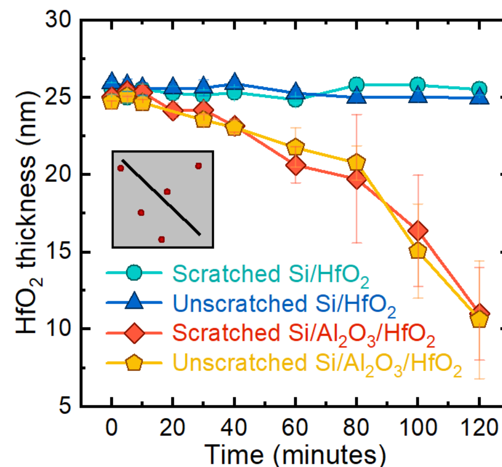


Figure 4.6: Thickness of HfO_2 films, deposited on top of either a ~20 nm thick Al_2O_3 layer or directly onto silicon, annealed at 400 °C in air for 30 min, as a function of time in a 10% HF solution. Samples scratched with a diamond scribe are compared to unscratched samples. A diagram of the method of scratching, and measurement locations, is shown within the figure.

pits in Si(100) [143],[144]. Si/HfO_2 and Si/Al_2O_3/HfO_2 samples in their as-deposited and annealed states are compared after 1 hour in a 25% TMAH solution at 80 °C. In the case of single layer Si/HfO_2 samples, no evidence of TMAH etching can be seen under an optical microscope; this is also the case for the as-deposited stacked samples. However, once annealed, the stacked sample shows extensive etching of the underlying silicon substrate across the entire sample, despite having already established there is no change in measured film thickness.

A close-up optical microscope image of the annealed and TMAH-etched stacked sample can be seen in Figure 4.7(a), which clearly shows the distinct square shape of the etch pits. This implies that the annealing of Si/HfO_2/Al_2O_3 stacked samples creates channels throughout the entire structure, through which the TMAH can pass through to the underlying silicon, as depicted in Figure 4.7(b).

Through application of AFM, the shape of these channels after the etching process was imaged. An image of a single etch pit, as well as the corresponding depth profile, can be seen in Figure 4.7(c) and (d). Note that the dimensions of the AFM tip prevent measurement of the full depth of the etch pit, with the value obtained here cutting

off at around −0.8 μm. These results would suggest that the dielectrics directly over the etch pits become undermined, and are thus removed by the solution, leaving a channel through the entire structure that is the size and shape of the etch pit below. The initial form of these channels before etching has not yet been identified, though there is the potential for them to take the form of pinholes. If controlled, pinholes can behave as a beneficial charge carrier transport mechanism, acting as an alternative tunnelling process through thin film structures. In particular, this may prove useful in the field of photovoltaics, for applications in passivating contacts [145]. These channels do not appear to be present in the as-deposited case or in the single layer Si/HfO_2 samples.

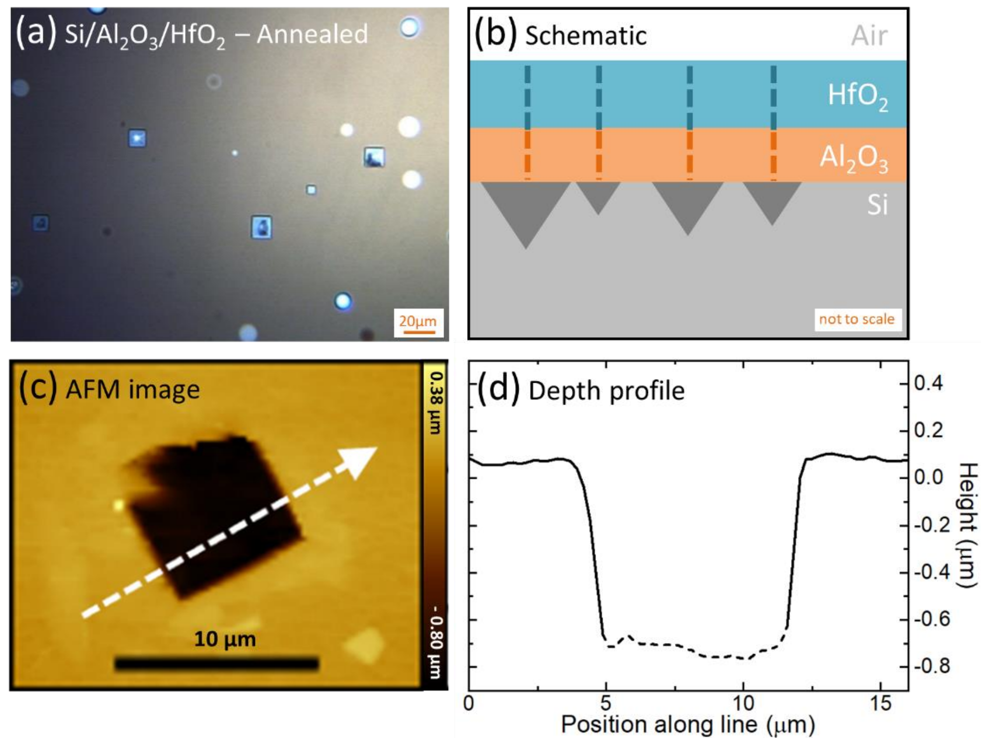


Figure 4.7: (a) An optical microscope image of a stacked Si/Al_2O_3/HfO_2 sample annealed at 400 °C, after 1 hour in a 25% TMAGH solution. (b) An illustration of the etch pits apparent in the structure, with the dashed lines representing some form of channel through the structure. (c) An AFM scan of a single etch pit in the annealed Si/Al_2O_3/HfO_2 sample. (d) The depth profile of the etch pit in (c), with the data collected along the white arrow. The dashed section in (d) does not correspond to the physical profile of the base of the etch pit and results from limitations of the AFM tip dimensions.

The same behaviour can be seen in annealed stacked samples during immersion in HF, as depicted in Figure 4.8. Visible channels appear in the stacked structure after around 20 minutes, which then expand over time. This is likely due to the HF passing through channels in the HfO_2 layer to the Al_2O_3 layer beneath, which will then etch more quickly in localised regions. The HfO_2 is eventually undermined and will delaminate, as can be seen in the final micrograph. This apparent channel structure may be responsible for the change in etching behaviour that we see in annealed stacked samples, compared to the other sample variations that have been investigated. However, it is not yet clear why these channels are not present in either single layer Si/HfO_2 samples, or as-deposited stacked Si/Al_2O_3/HfO_2 samples. A possible explanation would be the diffusion of hydrogen, or other elements, through the layers in the sample, which occurs during the post-deposition annealing stage. Blistering, resulting from high temperature anneals, may also be a potential factor [146],[147].

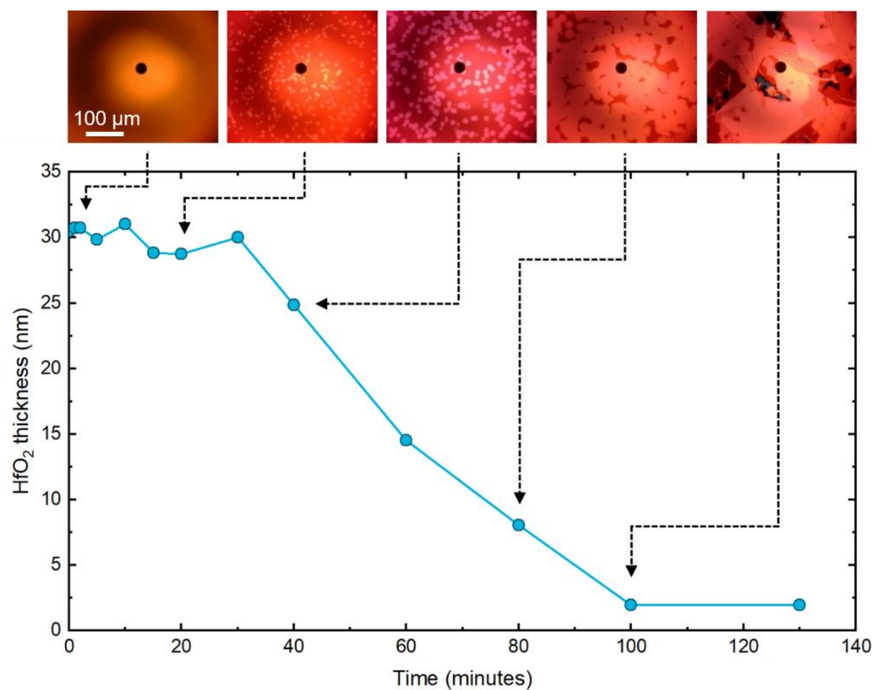


Figure 4.8: Thickness measurements and optical micrographs of a specific region on a stacked Si/Al_2O_3/HfO_2 sample, annealed at 350 °C, during immersion in a 10% HF solution. Each micrograph corresponds to a specific data point on the thickness plot. The black dots on each image highlight the reflectometry measurement point.

4.4.3 $Si/Al_2O_3/HfO_2$ vs $Si/HfO_2/Al_2O_3$

As discussed in section 4.4.2, the existence of channels within a $Si/Al_2O_3/HfO_2$ structure has been established. This section investigates whether these channels are unique to this particular stack, or whether they can be found in other film structures. As previously mentioned, no evidence of these channels was found in Si/HfO2 samples, and it is difficult to examine Si/Al_2O_3 samples due to the etch rates of Al_2O_3. However, it is possible to investigate $Si/HfO_2/Al_2O_3$ samples, which is the inverse of the initial $Si/Al_2O_3/HfO_2$ stack structure.

The thickness of the combined dielectric layer of $Si/Al_2O_3/HfO_2$ samples was measured using a Filmetrics F40 system, by assuming a fixed Al_2O_3 film thickness of 20 nm, and a variable HfO_2 film thickness. This was compared to $Si/HfO_2/Al_2O_3$ samples, where a fixed HfO_2 film thickness of 25 nm was assumed, with a variable Al_2O_3 film thickness. The results of this can be seen in Figure 4.9, with fixed and variable thicknesses depicted by solid and patterned sections, respectively.

After 1 hour in a 25% TMAH solution at 80 °C, the $Si/Al_2O_3/HfO_2$ films show no change in film thickness, as was established in section 4.3.1. For the $Si/HfO_2/Al_2O_3$ samples, the Al_2O_3 layer became thinner than could be accurately detected by the Filmetrics system. However, these samples could be accurately modelled using a single layer variable HfO_2 model, with a thickness that is slightly higher than the initially assumed 25 nm. It is, therefore, likely that the Al_2O_3 layer was fully removed, whilst the HfO_2 remained unetched.

Analysing these samples under a microscope, etch pits were seen in the annealed $Si/Al_2O_3/HfO_2$, as seen in Figure 4.7(a). However, no evidence of etching was found in $Si/HfO_2/Al_2O_3$ stacks, annealed or as-deposited. If pinhole formations do exist within this stack structure, they exist in such a way that solutions are unable to widen and travel through them to the silicon substrate below.

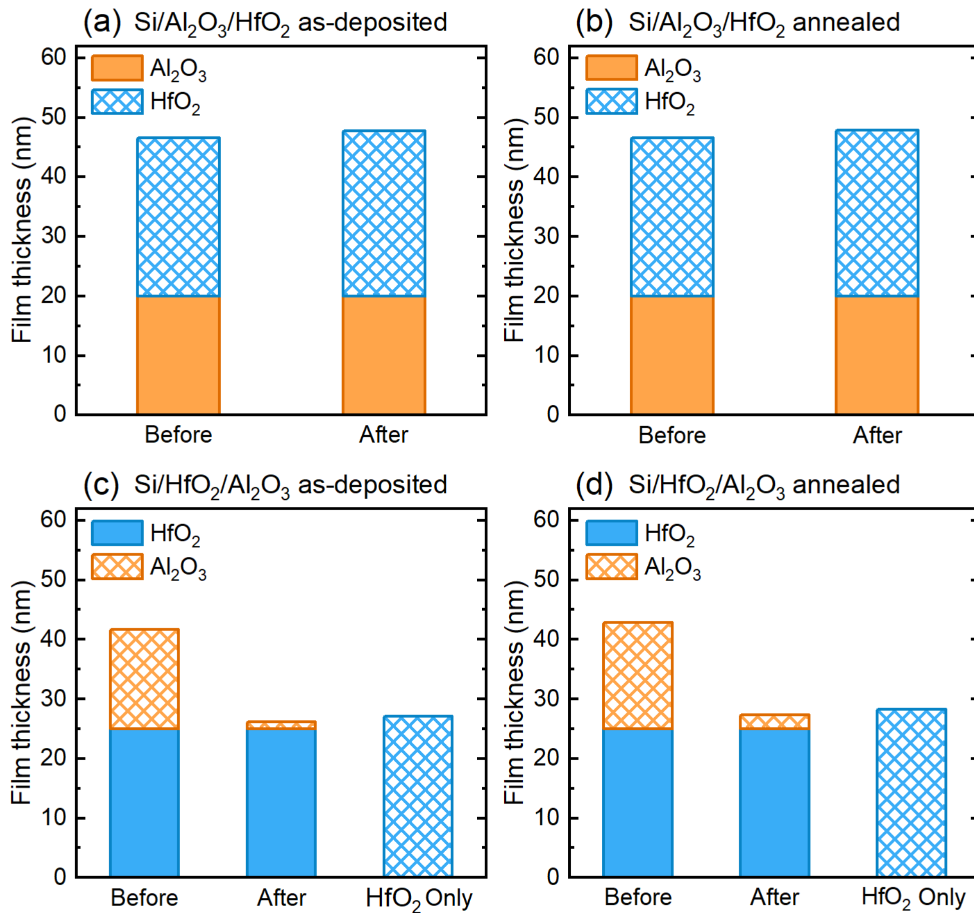


Figure 4.9: Thickness of (a),(b) Si/Al_2O_3/HfO_2 stacks and (c),(d) Si/HfO_2/Al_2O_3 stacks, measured via reflectometry, before and after 1 hour in a 25% TMAH solution at 80 °C. Both as-deposited samples and samples annealed at 400 °C are included. In the reflectometry model the bottom layer of the stack is set to a fixed thickness (solid), and the upper layer thickness is variable (patterned).

4.4.4 Thickness vs density

As previously discussed, the Filmetrics modelling system used in this work assumes a fixed film density. However, this is not the case for the Malvern Panalytical AMAS software, which considers film thickness and density to be variable.

Figure 4.10(a) shows the Filmetrics measurement results for three samples after immersion in a 10% HF solution. Two of these samples were annealed at approximately 300 °C, and the final sample, annealed at a higher temperature above the crystallisation region, was used as a control. As expected, the measured thickness

of the control sample does not vary after 1 hour in the HF solution, whilst the 300°C annealed samples get thinner with longer immersion times (as the HfO_2 films etch), consistent with the data presented in Figure 4.4. These samples were kept in solution for 2 min and 4 min, denoted as 2 min HF and 4 min HF, respectively. Figure 4.10(b) shows x-ray reflectivity (XRR) data of the same samples, after immersion in HF. The reflectivity curves of the control sample and the 4 min HF sample have the same frequency, indicating similar film thickness. The frequency of the 2 min HF sample reflectivity curve, however, is approximately half that of the other two samples, suggesting a thinner film. The results of these two figures are summarised in Table 4.1.

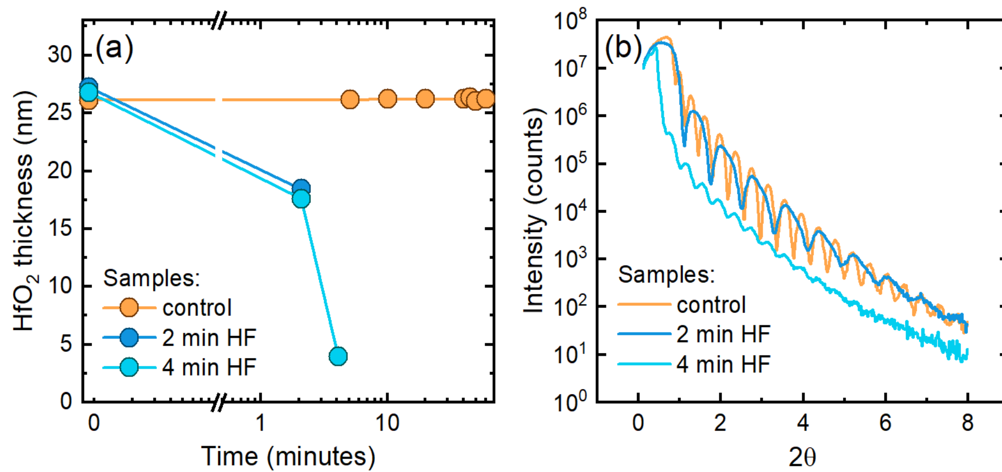


Figure 4.10: (a) Thickness of HfO_2 films deposited on silicon, measured via reflectometry, as a function of time spent in a 10% HF solution. Samples include: one sample annealed at approximately 300 °C, immersed in HF for 2 min, a nominally identical sample immersed for 4 min, and a control sample which has been annealed at a higher temperature.

As seen from the results in Table 4.1, the XRR model suggest that the HfO_2 films are initially getting thinner whilst maintaining a relatively consistent density, but with continued immersion in HF, the samples return to their initial thickness with a significantly lower density. This does not make physical sense, indicating there must be a limitation within the model.

Sample	Filmetrics Thickness (nm)	X-ray Reflectivity Thickness (nm)	X-ray Reflectivity Density (g/cm^3)
control	26.23	21.54	8.81
2 min HF	18.45	10.88	9.68
4 min HF	3.97	23.42	2.70

Table 4.1: A comparison between measured results of HfO_2 film thickness, from a Filmetrics F40 reflectometry system and x-ray reflectometry data fitted using the Panalytical AMAS software. The Filmetrics system assumes a fixed film density, whilst the AMAS software considers both film thickness and film density to be variable.

To elucidate the inconsistency between film thickness and density via XRR, we perform a Fourier thickness analysis, derived from the XRR measurements. Figure 4.11(a)-(c) shows thickness analysis Fourier plots for the three samples, with the raw data in blue and the model in red. The raw data for the 2 min HF sample in Figure 4.11(b) still shows a peak at ~20 nm, which could not be fit by the model. This indicates that the thickness of 10.88 nm in Table 4.1, as suggested by the model, is not accurate. Figure 4.11(d) shows a density plot of this sample. The top of the HfO_2 film appears to have a low density of around 2 g/cm^3, which is similar to the 2.70 g/cm^3 density of the 4 min HF sample film. At a thickness of around 11 nm there is a transition, where the density increases up to almost 10 g/cm^3, which then remains consistent throughout the bottom section of the film. This lower region is what was modelled by the AMAS software, resulting in the appearance of a reduced film thickness.

With this exception accounted for, the overall results from the XRR data suggest film density, rather than film thickness, is decreasing with increased etch time. Additionally, film density does not appear to decrease uniformly throughout the film, but instead decreases from the top downwards. This data is not enough to conclusively state which model is more accurately depicting the real physical changes within the HfO_2 films, but it is important to consider how film thickness and density are integrated into such models for future studies.

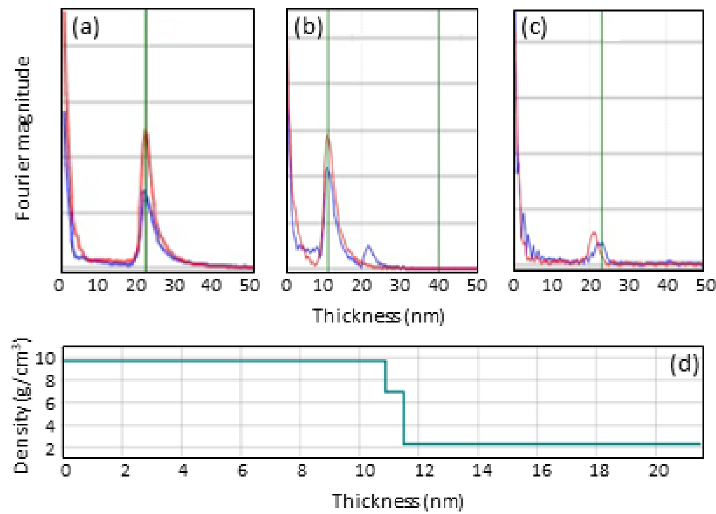


Figure 4.11: Film thickness Fourier analysis of XRR data for samples consisting of HfO_2 films deposited onto silicon, with the data plotted in blue and the model fit in red. These samples include: (a) a control sample, which remains unetched after immersion in HF, (b) a sample annealed at approximately 300 °C after 2 min in a 10% HF solution, (c) a nominally identical sample after 4 min in HF. (d) A density profile of the 2 min HF sample from (b).

4.5. Case Study

4.5.1 Lifetime control

The benefits of the etch resistance of HfO_2 films are shown in the following example of a fabrication process used to produce patterned passivation layer to control carrier lifetime in semiconductor devices. Such lifetime control is needed in the fabrication of mm-wave or THz modulation devices. Such devices are particularly useful for quality-control and security imaging purposes, enabling for non-invasive screening of stacked or concealed materials, like dielectric, plastics, and textiles [148].

To achieve a suitable trade-off between modulation and switching speed in THz photomodulators, it is necessary to control the effective lifetime in the device [149]. The carrier lifetime level required often lies in between the value required given by two well passivated surfaces and a completely unpassivated wafer (e.g. 10µs to 10ms). One way of achieving such an intermediate lifetime is to pattern the surface passivation on one side, which was the approach used in a recent study by Hooper *et*

al. [138]. The production of such a photomodulator was enabled by the use of etch-resistant HfO_2 layer on the rear, as described in this section.

A schematic of the fabrication process can be seen in Figure 4.12(a). Both sides of a high lifetime silicon wafer were passivated by Al_2O_3 films. A HfO_2 layer is then deposited over the Al_2O_3 on the rear. The sample is then annealed at 450 °C, with the temperature required for optimal Al_2O_3 passivation being above the crystallisation temperature of the HfO_2 layer. The crystallised HfO_2 becomes strongly resistant to wet chemical etching, in comparison to the exposed Al_2O_3 layer on the front. Photolithography is then used to pattern the front Al_2O_3 layer, and immersion in a 2% TMAH solution at room temperature results in the front Al_2O_3 etching according to the photolithography pattern, whilst the rear Al_2O_3 is protected by the HfO_2.

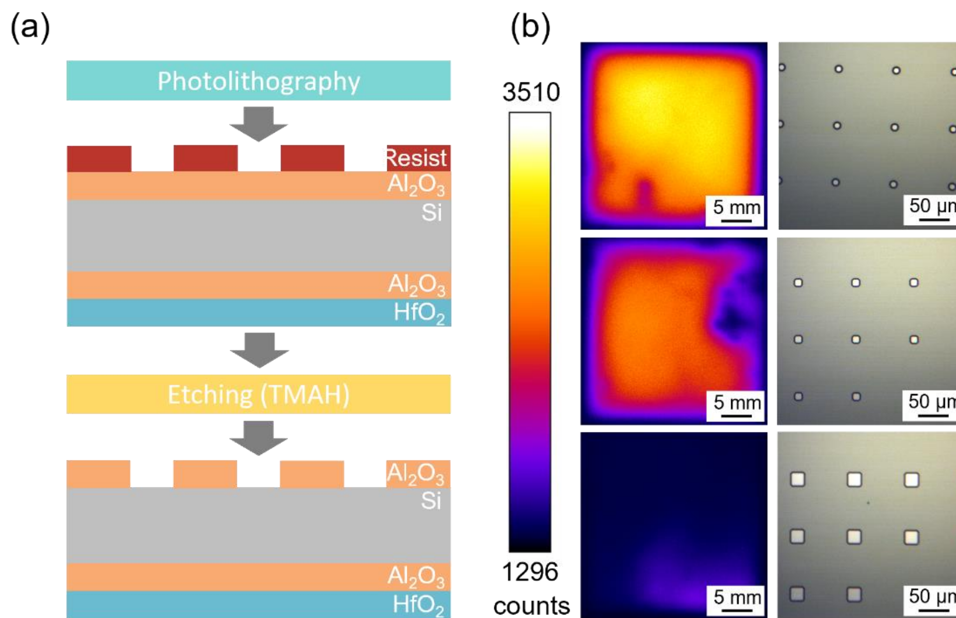


Figure 4.12: (a) A process sequence involving the use of a rear HfO_2 protective layer to fabricate a patterned front-side passivated THz photomodulator. The HfO_2 layer provides protection against etching for the rear Al_2O_3 passivation, whilst the front is patterned and etched through a combination of photolithography and immersion in a 2% TMAH solution. (b) Photoluminescence images acquired with the same exposure conditions (1 Sun, 5 s) of samples with different filling fractions on the front Al_2O_3 surface, producing samples with tuneable carrier lifetimes. The optical micrographs show the patterned passivation structures with Al_2O_3 having been removed from the lighter-coloured periodic features.

Importantly, stacking the Al_2O_3 and HfO_2 does not result in any substantial decline in passivation quality. Consistent and high-quality passivation is essential, so that the carrier lifetime of each device can then be carefully controlled through the patterning process on the front side. Each pattern has a different filling fraction, with an increased filling fraction indicating the increasing size of holes within the passivation layer, corresponding to a decrease in carrier lifetime. Examples of samples with patterns of increasing filling fraction, and thus decreasing passivation, can be seen in Figure 4.12(b). This example illustrates the potential of using HfO_2 protective films in the fabrication of semiconductor devices.

4.6 Conclusions

This chapter has studied the etch resistance of single layer Si/HfO_2 and stacked Si/Al_2O_3/HfO_2 structures to solutions commonly used in silicon processing. HfO_2 deposited directly onto Si has been demonstrated to have excellent etch resistance to RCA1, RCA2, and TMAH, showing no indication of variation in film thickness after 1 hour in each solution. Si/HfO_2 samples annealed above 350 °C also show no sign of etching after 1 hour in a 10% HF solution, though etch rates increase dramatically with lower temperature anneals. A direct correlation between the etch rates of HfO_2 films in HF to the HfO_2 film crystallinity was identified, with amorphous films annealed <300 °C etching quickly, crystallised films annealed ≥350 °C not etching within the timeframe, and a transition period between these temperatures where the film begins to crystallise.

In the case of annealed Si/Al_2O_3/HfO_2 stacked samples, a reduction in etch resistance was identified, compared to the single layer counterparts. It has been established that this reduced etch resistance is not a consequence of changes in the HfO_2 crystallised structure, and is not likely to be related to handling damage of the samples. By investigating the TMAH etching of stacked samples, evidence for channels has been found within the annealed Si/Al_2O_3/HfO_2 structure, which allow chemical solutions to penetrate down to the silicon below. In the case of TMAH, the HfO_2 and Al_2O_3 films

themselves are not etched, as there is no change in measured film thickness. However, in a 10% HF solution the Al_2O_3 layer beneath the HfO_2 does appear to etch away, resulting in undermining and delamination of the HfO_2 film.

Different interlayers may influence chemical etch resistance, as with the $Si/Al_2O_3/HfO_2$ stack, due to the formation of channels within the sample structure. However, the etch resistance of the stack is still significantly greater than in the case of an exposed Al_2O_3 layer.

The excellent etch resistance of HfO_2 films, as demonstrated in this chapter, suggests a promising potential for applications as protective barrier layers in silicon-based electronic and photovoltaic device structures. The use of HfO_2 thin films as a protective barrier has already proved useful in the research of THz and mm-wave modulation, and has the potential to be applied to a variety of different stacked structures. This work will become even more important as device structures and silicon processing techniques continue to develop in complexity.

4.7 Future Work: Localised annealing

This section details initial investigations into utilising the controllable etch resistance of HfO2 demonstrated in this chapter. Though these investigations have not been pursued to completion, they provide insight into potential routes for further work.

4.7.1 Laser annealing

As mentioned in this chapter, the patterning of thin film dielectrics can be useful for the fabrication of semiconductor devices, such as THz modulators. Current patterning methods require photolithography, which is a time-consuming process that is not easily expanded to an industrial scale. This section investigates using the unique etching characteristics of HfO_2 films to develop an alternative approach to wafer patterning.

As demonstrated throughout this chapter, the etch rate of HfO_2 films can be controlled through a simple heat-treatment of the sample. Amorphous HfO_2 will etch rapidly in HF, whilst fully crystallised HfO_2 has strong resistance to HF etching. If a HfO_2 thin film can be locally crystallised through an annealing process, then a pattern can be produced through a simple HF dip.

T. Tabata demonstrated the localised annealing of HfO_2 through the application of a UV pulsed laser [82]. However, this resulted in a cubic structure, rather than monoclinic. This may have been due to the increased cooling rate compared to conventional furnace annealing, which prevented relaxation of the structure into a monoclinic form. The etching characteristics of cubic HfO_2 have not yet been investigated.

Similarly, Larkin *et al.* used a condensed e-beam, with an electron dose of 10^6 e/nm^2, to produce a slow transition from amorphous to crystallised HfO_2, with a resolution of 10 nm [80, 81]. The crystallisation of the HfO_2 is visible through a TEM microscope, though the exact crystallised structure was not determined.

To investigate the potential of laser annealing on HfO_2 films, a Universal Laser Systems 50 W CO_2 laser setup was utilized. A grid pattern was designed, to be annealed onto a 10 cm silicon wafer, with approximately 27 nm of HfO_2 deposited on both sides. This grid was made up of 0.5 × 0.5 cm squares, 6 squares across and 6 squares down, as seen in Figure 4.13. Speed, power, and points per inch (PPI) were all varied across the grid pattern. Initially, speed was varied between 100% - 5%, with power and PPI at maximum, then power was varied from 10% - 60%, with speed at 5% and PPI at maximum, and finally PPI was varied between 50 – 200 PPI, with power at maximum, and speed also varying from 5% - 40%. Every other row, the settings would be repeated, with the anneal conducted on both sides of the wafer, rather than the top side only. These settings are summarised in Table 4.2, with each box corresponding to a square on the grid pattern.

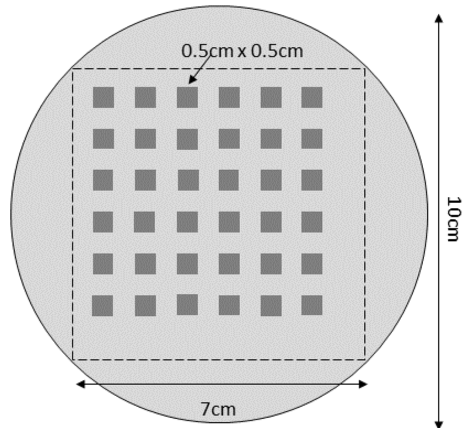


Figure 4.13: A schematic of a laser pattern on a 10 cm wafer, consisting of a grid of 0.5 × 0.5 cm squares, 6 across and 6 down. The laser settings are varied in each square, in attempt to locally anneal the HfO_2 film on the sample, without damage to the Si wafer.

Speed	100%	80%	60%	40%	20%	5%	
Speed	100%	80%	60%	40%	20%	5%	double sided
Power	10%	20%	30%	40%	50%	60%	
Power	10%	20%	30%	40%	50%	60%	double sided
PPI	50 (5%)	50 (10%)	50 (20%)	100 (20%)	100 (40%)	200 (40%)	
PPI	50 (5%)	50 (10%)	50 (20%)	100 (20%)	100 (40%)	200 (40%)	double sided

Table 4.2: A table showing the laser settings that were varied throughout the initial laser annealing investigation, with each box corresponding to a square on the grid in Figure 4.13. As speed was varied, power and PPI were set to maximum. When power was varied, PPI was at maximum and speed was at 5%. When PPI was varied, power was at maximum and speed was varied as shown by the numbers in brackets.

Figure 4.14(a)-(c) compares PL imaging of the sample before and after the localised annealing process, alongside a control sample annealed in a furnace at 400 °C. Crystallised monoclinic HfO_2 is known to passivate silicon, resulting in higher carrier

lifetimes than amorphous HfO_2 [21, 22, 24, 70, 71], and the variation in carrier lifetime can be detected through PL imaging. However, there is no change in PL intensity between the wafer before and after the laser process, indicating that no crystallised monoclinic HfO_2 is present on the surface. Figure 4.14(d) and (e) show microscope images of the laser damage that is present in some of the squares on the pattern. This occurs should the speed of the laser be too low, or the power or PPI be too high.

From these initial results, it is clear that laser annealing of HfO_2 films is a very involved process. Initial experiments with this particular set-up proved unsuccessful, though more success may be had through use of a different laser, as demonstrated by Tabata [82].

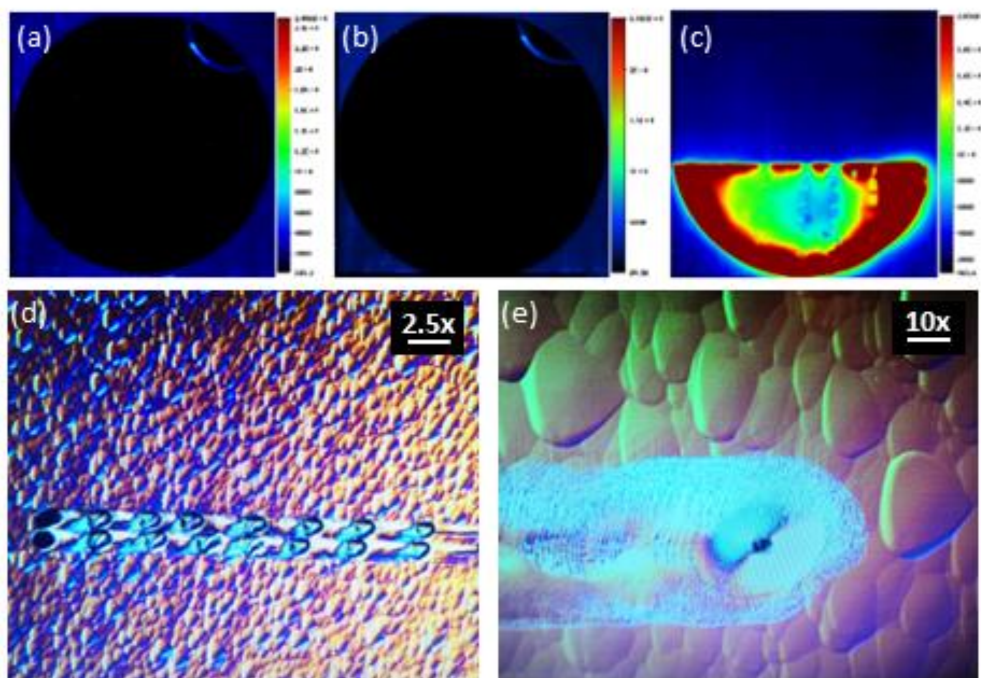


Figure 4.14: PL images acquired with the same exposure conditions (1 Sun, 5 s) of (a) a silicon wafer with ~12 nm amorphous HfO_2, (b) the same sample after a laser annealing process, and (c) a control wafer annealed in a furnace at 400 °C. (d) A microscope image of laser damage to the silicon wafer, showing the frequency of the laser pulsing, with (e) a close-up image of the damage caused by a single pulse.

4.7.2 Stamp annealing

A simpler approach to localised annealing is to use a stamp method. For this process a ceramic washer, heated in a furnace to around 600 °C (well above the crystallisation temperature of HfO_2) was stamped onto Si samples, as demonstrated in Figure 4.15(a). A Si sample, with approximately 27 nm HfO_2 on both sides, was placed on a hotplate heated to 300 °C (just below the crystallisation temperature of HfO_2). The washer was removed from the furnace, quickly transferred to the wafer, and pressed onto the surface for 2 minutes. This was repeated on both sides of the sample. Figure 4.15(b) shows a photograph of a sample after stamp annealing, with a ring of particulates on the surface, likely picked up from the furnace. Figure 4.15(c) shows a PL image of the same sample. A faint ring is of higher PL intensity is present; however, this is likely due to the luminescence of dirt particles, rather than any crystallisation of the HfO_2 film.

As will be demonstrated in section 5.3.2, it takes several minutes for samples to heat up enough for crystallisation to occur and improve carrier lifetime. It is likely that with the stamp annealing approach, the washer cools down too quickly to have any significant impact on the film crystallinity. This stamp method was also attempted using a soldering iron; however, this again yielded no successful results. Similarly, this could be due to temperature limitations, or potentially metal contamination.

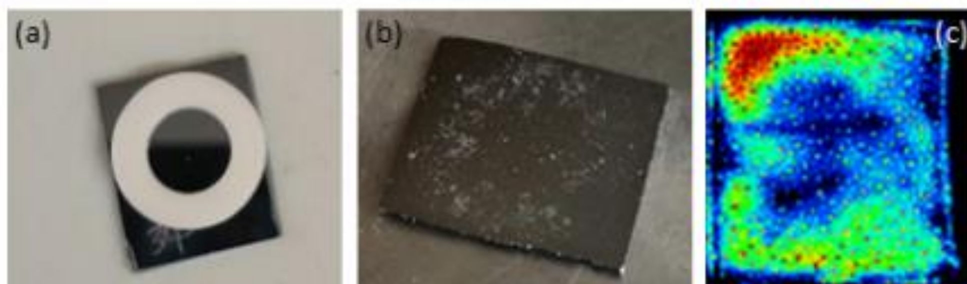


Figure 4.15: (a) A photograph of the ceramic washer used for the stamp annealing process, placed atop a Si wafer cut to approximately 1 x1 cm. (b) A photograph of a sample after the stamp annealing process, with a ring of particulates on the surface, left by the washer. (c) A PL image of the same sample.

4.7.3 Heat-gun annealing

A final attempt at localised annealing was made through the application of a heat-gun. This approach was designed to replicate the conditions of an annealing furnace in a very localised area, with hot air being the heat transfer mechanism. In this case, a DURATOOL 240 V Hot Air Rework Station was used, with a small circular nozzle, in order to minimise the spot size. A schematic of the experimental setup can be seen in Figure 4.16(a). The heat gun was turned up to 500 °C, and kept at a constant temperature for 30 min, with the air flow at lowest possible setting, to align with the relatively low gas flows in a tube furnace.

Figure 4.16(b) shows a photograph of a sample after the heat gun annealing process. A dark spot can be seen in the centre of the sample, at the point which would have been just below the nozzle of the heat gun. This could possibly be dirt, similar to the stamp annealing process, which was burnt onto the sample.

Filmetrics measurements of the film thickness were taken at five points across a sample after annealing, as shown by the red crosses in Figure 4.16(b). The sample was then dipped in a 10% HF solution for 1 min, and the measurements were repeated. The results of this can be seen in Figure 4.16(c).

As expected, after 1 min in HF the HfO_2 film is substantially thinner, indicating that the film did not crystallise. However, at measurement point 5, which was the location underneath the heat gun nozzle, the film appears to be around 7 nm thicker than the rest of the sample. It is a possibility that the film was beginning the crystallise, and thus had a slightly slower etch rate. However, it is also possible that this is instead related to the dark spot, indicating some kind of deposit, left on the surface after the heat gun process, which may have interfered with the etching.

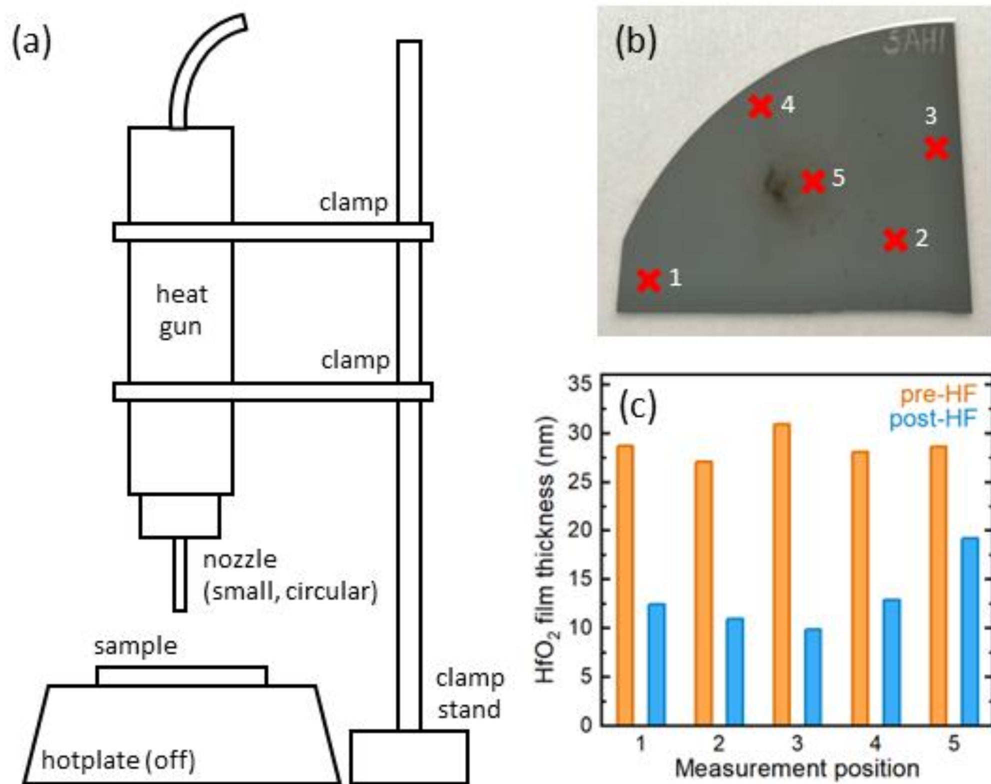


Figure 4.16: (a) A schematic of a localised annealing setup, composed of a heat gun with a small nozzle, positioned over a double sided HfO_2 Si sample on a hotplate (turned off). (b) A photograph of a sample after the annealing process, with the red crosses depicting Filmetrics measurement points. (c) Filmetrics data of the sample in (b) before and after immersion in a 10% HF solution for 1 min.

These initial investigations into localised annealing show a promising route to a simplified wafer patterning process, utilising the controllable etch resistance of HfO_2 films to eliminate the need for photolithography in device fabrication. Future work on this topic should focus on optimising localised annealing processes, to produce clear and consistent results. If this approach were to become industrialised, it would require high resolution and flexibility in patterning options. As such, laser annealing would be the most practical route to take. However, the stamp annealing and heat gun processes are much simpler, and are more likely to produce verifiable results in the short term.

4.8 Contributions

The content of this chapter has been published [150] and parts of the text have been included verbatim. The reported results include experimental contributions from Brendan Healy and Edris Khorani in the form of AFM measurements, and the fabrication and imaging of lifetime control samples, respectively.

Chapter 5

Mechanisms of Silicon Surface Passivation by HfO_2 Thin Films

This chapter studies the mechanisms underpinning effective surface passivation of silicon with hafnium oxide thin films grown *via* atomic layer deposition (ALD). Plasma-enhanced ALD with O_2 plasma and a tetrakis(dimethylamido)hafnium (TDMAH) precursor was used to deposit 12 nm thick HfO_2 films at 200 °C on high-lifetime 5 Ωcm *n*-type Czochralski silicon wafers. The passivation was activated by post-deposition annealing, with 30 min in air at 475 °C found to be the most effective. High-resolution grazing incidence X-ray diffraction measurements revealed the film crystallised between 325 and 375 °C, and this coincided with the onset of good passivation. Once crystallised, the level of passivation continued to increase with higher annealing temperatures, exhibiting a peak at 475 °C and yielding surface recombination velocities of <5 cm s^{-1} at 5 × 10^{14} cm^{-3} injection. A steady decrease in effective lifetime was then observed for activation temperatures >475 °C. By superacid re-passivation, it was demonstrated that this reduction in lifetime was not due to a decrease in the bulk lifetime, but rather due to changes in the passivating films themselves. Kelvin probe measurements showed the films are negatively charged. Corona charging experiments showed the charge magnitude is of order 10^{12} qcm^{-2} and that the reduced passivation above 475 °C was mainly due to a loss of chemical passivation. This study therefore demonstrates the development of highly charged HfO_2 films and quantifies their benefits as a standalone passivating film for silicon based solar cells.

5.1 Motivation

High-quality surface passivation plays an essential role in the operation of high efficiency silicon photovoltaic cells. Passivation is achieved by deposition or growth of a dielectric thin film, which suppresses surface recombination by terminating dangling bonds (chemical passivation) and/or by repelling carriers away from surfaces by a built-in charge (field effect passivation). A variety of such films have been researched [33] and from the perspective of commercial silicon photovoltaics, Al_2O_3 grown by atomic layer deposition (ALD) and SiN_x grown by plasma enhanced chemical vapour deposition (PECVD) are the most commonly used at present.

Hafnium oxide (HfO_2) is a dielectric that has been extensively researched by the electronics industry for applications in transistors and capacitors [132, 133]. It has also been investigated for applications as a protective barrier layer, demonstrating resistance to oxidation, copper corrosion, and general weathering [27, 29, 30]. HfO_2 has the potential to become a useful passivation layer for photovoltaics as it can be grown by established ALD processes and can have either positive or negative charge polarity [20-26]. The benefits of HfO_2 as a passivation layer are especially apparent for ultra-thin films below 5 nm, where it has been shown to outperform Al_2O_3 [71]. This advantage suggests a potential application for HfO_2 films in passivating contact structures.

In common with most ALD-based passivation schemes, a post-deposition anneal is required to “activate” the passivation by HfO_2. Previous investigations have been conducted on both the deposition parameters, including precursors, deposition temperatures and cycles [20-22], as well as the post-deposition annealing conditions [21-23] for HfO_2. Most studies find HfO_2 passivation to give a surface recombination velocity (SRV) of 3–5 cm/s [21, 23], though some studies have claimed as low as 1.2 cm/s [22]. Most passivation studies have been performed on float-zone (FZ) silicon substrates, which have been shown to degrade at the temperatures necessary to activate the HfO_2 passivation [151]. This work instead uses Czochralski (Cz) silicon,

which is the material of choice for the photovoltaics industry. Importantly, this study includes a room temperature superacid re-passivation process after HfO_2 passivation. This enables the separation of changes in surface recombination from those in bulk recombination, which has not done in previous studies.

The aim of this chapter is to establish the mechanisms of the activation process necessary to achieve good levels of passivation from HfO_2 thin films. Therefore, charge carrier lifetime investigations are complimented by with high-resolution X-ray diffraction (XRD), Kelvin probe, and corona charging, which provides an in-depth understanding of the physical and electrical characteristics of the HfO_2 films. These investigations give insight into the post-deposition treatments necessary to maximise the overall HfO_2 passivation quality, distinguishing between the contributions of chemical and field-effect passivation.

5.2 Experimental details

This section reports specific details detailing to the apparatus and experimental processes utilised within this chapter. For general information relating to methodology and theory, please refer to Chapter 3.

5.2.1 Sample fabrication

Lifetime samples were fabricated from chemically etched 120 μm thick 5 Ωcm *n*-type Cz-Si (100)-orientation wafers, cut into 5 × 5 cm squares. Lifetime optimisation investigations were performed on the same batch of wafers to minimise variations between batches. A separate batch of samples was used for the corona charging measurements and these samples were nominally identical except for being 150 μm thick. The samples used for the XRD measurements were thicker, mirror polished silicon substrates. Before ALD, all samples were first subjected to a rigorous cleaning and etching process developed previously [89]. This involves submerging the samples in a “standard clean 1” (SC1) solution (500 ml de-ionised (DI) H_2O, 100 ml NH_4OH

(30%), 100 ml H_2O_2 (30%)) for 10 min, followed by a “standard clean 2” (SC2) solution (500 ml DI H_2O, 100 ml HCl (37%), 100 ml H_2O_2 (30%)) for 10 min. Both solutions were heated to 80 °C, with the H_2O_2 being added once the solutions were up to temperature. Between these two steps, the samples were immersed in a 25% tetramethylammonium hydroxide (TMAH) solution for 10 min, again heated to 80 °C. A de-ionized (DI) water rinse and 60 s dip in a 1% HF solution (490 ml DI H_2O, 10 ml 50% HF) were conducted before each cleaning and etching step.

Literature suggests that the surface pre-treatment applied immediately before deposition can have an influence on resulting film quality [22, 24, 25, 88]. Figure 5.1 shows a comparison between samples that have undergone three different surface pre-treatments: a 2% HF dip for 10 s, a 2% HF dip followed by a 30 s DI water rinse, or a 10 s 1% HF 1% HCl dip. Lifetime measurements were taken immediately following the pre-treatment, and again after HfO_2 deposition and annealing. In this case, all explored pre-treatments result in a similar level of performance. As such, a 2% HF dip was used, in line with previously developed processes [89]. Once samples pulled dry, they were immediately placed onto the ALD stage.

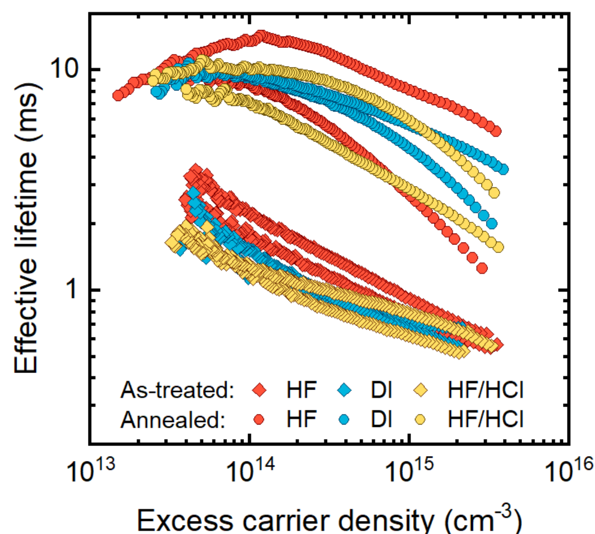


Figure 5.1: Lifetime curves for 6 wafers, immediately after cleaning (diamonds), with either a final 2% HF dip, a 1% HF 1% HCl dip, or a DI water rinse. Lifetimes of the same samples, once coated with HfO_2 annealed at 475 °C for 30 minutes, are also shown (circles).

A Veeco Fiji G2 system was used for the plasma-enhanced ALD of HfO_2 at 200 °C with an O_2 plasma and tetrakis(dimethylamido)hafnium (TDMAH) used as the co-reactant and precursor, respectively. Argon was used as the inert purge gas. TDMAH is pulsed into the chamber for 0.25 s, followed by a 6 s pulse of O_2 plasma at 300 W. A 5 s purge is conducted before and after each step. For all samples, 100 process cycles were performed per side, which was later confirmed by X-ray reflectivity (XRR) to give a film thickness of ~12 nm. For some experiments, Al_2O_3 passivation was used for control purposes, which was also deposited at 200 °C by plasma enhanced ALD. The precursors used for Al_2O_3 were trimethylaluminium (TMA) and O_2 plasma, with argon again used as the purge gas. For this recipe the TMA was pulsed into the chamber for 0.06 s, followed by a 6 s pulse of O_2 plasma at 300 W, with a 4 s purge after each precursor. 160 cycles of this process were completed, resulting in a film thickness of ~20 nm.

After ALD, samples were annealed *ex situ* in a quartz tube furnace with the times chosen in the range 2 to 60 min and the temperatures up to 625 °C. The ambient was air unless otherwise specified.

5.2.2 Characterisation

The effective lifetime of the coated and annealed samples was measured by transient photoconductance decay using a Sinton WCT-120 lifetime tester. Lifetimes were assumed to be accurate to ± 10% guided by the work of Blum *et al.* [114]. This was then used to calculate SRV according to:

$$SRV = \frac{W}{2}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right), \tag{31}$$

where W is the substrate thickness, τ_{eff} is the effective lifetime, and τ_{bulk} is the bulk lifetime. It is assumed that there is no other bulk recombination and thus τ_{bulk} is the intrinsic lifetime ($\tau_{intrinsic}$), which is taken from Ref. [152]. Consequently, these values of SRV should be regarded as upper limits. The recombination parameter, J_0, is also

calculated, using the Sinton Instruments Lifetime Software (version 4.5.2), through application of a similar approach to Kane and Swanson [153]. Single-sided J_0 values are reported, which are half of the extracted J_0 values.

To isolate potential bulk and surface degradation effects, certain samples were stripped of their HfO_2 passivation and re-passivated with a temporary superacid scheme [89, 154, 155]. This is known to provide very good surface passivation (SRV <1 cm/s) without modifying the sample's bulk lifetime due to temperature or hydrogenation effects. HfO_2 films were stripped by immersion in a 10% HF solution until the surface became hydrophobic, then cleaned and etched once again as described previously. The samples were then dipped in a solution of bis(trifluoromethanesulfonyl)amide (TFSA) in pentane (2 mg/ml) for 1 min to create the temporary surface passivation before lifetime measurements were made. TFSA and pentane (purity ≥95.0% and >99%, respectively) were obtained from Sigma-Aldrich.

Grazing incidence XRD (GI-XRD) was carried out on annealed, HfO_2-coated, mirror-polished wafers using a 3rd generation Panalytical Empyrean XRD Diffractometer, equipped with multicore (iCore, iCore) optics and a Pixcel3D detector under Cu $K_{\alpha 1/2}$ radiation. Peaks were fitted using the Panalytical XRD crystallography data analysis software HighScore Plus and verified using GSAS-II [156]. Film thickness was obtained by analysing XRR data with Panalytical's AMAS software, and this was confirmed by a Filmetrics F40 reflectometry measurement tool.

Contact potential difference (CPD) and surface photovoltage (SPV) were measured using a KP Technology SKP5050 Kelvin probe system, with a 2 mm diameter gold-plated tip, following the method of Baikie *et al.* [116]. An effective work function was calculated from the CPD using a gold reference sample and the SPV was measured by cycling through 50 data points in the dark and 50 data points under illumination, taken every 0.5 s. SPV was determined as the difference between the averaged dark and light values.

Corona charging was used to investigate the magnitude of bulk charge within the HfO_2 films. Positive charge was deposited onto the surface of the HfO_2 layer through use of a custom-built setup composed of a needle positioned 7 cm above the sample and held at approximately 7 kV for 5 s on each side of the sample. Charge deposition was calibrated *via* a Kelvin probe method proposed by Bonilla *et al.* [122, 157].

5.3 Optimisation of activation annealing conditions

This section presents the results of a study to optimise the post-ALD activation conditions for HfO_2 surface passivation, including annealing ambient, time, and temperature.

5.3.1 Annealing ambient

Figure 5.2 shows results for optimisation of annealing ambient. In Figure 5.2(a), effective lifetime curves are shown for HfO_2 and Al_2O_3 annealed at 475 °C in different ambients (air, N_2 and Ar). Two curves are shown for each condition to give an indication of process reproducibility. Annealing in air gave the best results for both HfO_2 and Al_2O_3; N_2 and Ar annealing resulted in marginally worse performance for Al_2O_3 and considerably worse performance for HfO_2. This can also be seen from the comparison of lifetime values, extracted at a fixed carrier density of 5×10^{14} cm^{-3}, seen in Figure 5.2(b). Based on these results, air was used as the post-deposition annealing ambient for the rest of this study.

5.3.2 Annealing time

The effect of annealing time on measured lifetime for HfO_2 annealed at 475 °C in air for different times is shown in Figure 5.3. The effective lifetime values (and hence the passivation levels) initially increase with time up to 25 min and, after this time, no further improvements occur. There is no obvious degradation in the measured lifetimes at longer annealing times, indicating there is a broad temporal process

window for thermal activation. Based upon these results, subsequent experiments in this chapter used an annealing time of 30 min.

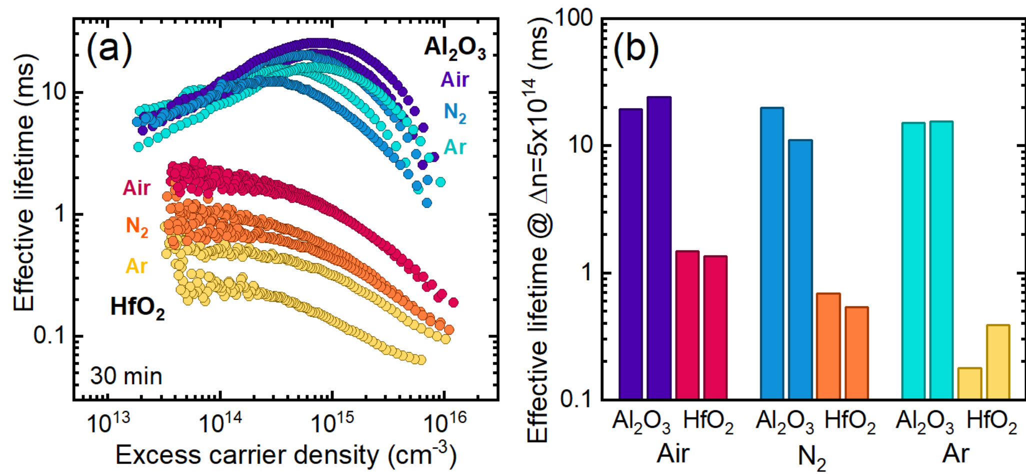


Figure 5.2: (a) Lifetime curves for 120 µm thick 5 Ωcm n-type Cz-Si wafers coated with HfO_2 and Al_2O_3 films annealed in various ambients at 475 °C for 30 minutes. (b) Effective lifetimes at an excess carrier density of 5 × 10^{14} cm^{-3} for each annealing time in (a).

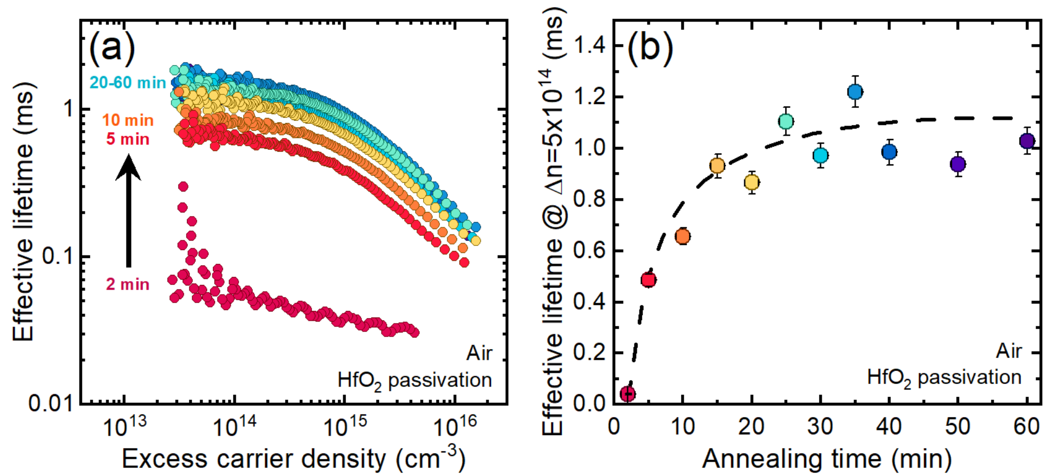


Figure 5.3: (a) Lifetime curves for 120 µm thick 5 Ωcm n-type Cz-Si wafers coated with ~12 nm HfO_2 films annealed at 475 °C for different lengths of time. (b) Effective lifetimes at an excess carrier density of 5 × 10^{14} cm^{-3} for each annealing time in (a), with the dashed curve providing a guide to the eye.

5.3.3 Annealing temperature

Results for the temperature dependence of the activation of the HfO_2 passivation with isochronal 30 min annealing in air are shown in Figure 5.4. Effective lifetimes in

samples annealed below 300 °C were too low to measure reliably. Effective lifetime increases with temperature up to 475 °C, then decreases at higher temperatures. The lifetime curves are plotted systematically increasing up to 475 °C in Figure 5.4(a) and systematically decreasing at higher temperatures up to 625 °C in Figure 5.4(b). SRV values extracted at an excess carrier density of 5×10^{14} cm^{-3} are shown in Figure 5.4(d), with the minimum value of 4.1 cm/s determined at 475 °C. This value is significantly lower than initial investigations into HfO_2 passivation [25], but is in line with more recently published results by Cui *et al.* and Tomer *et al.* who achieved SRV values of 3.3 cm/s and 5 cm/s, respectively [21, 23]. Direct comparison between literature SRV values is not always possible due to the influence of doping concentration [158], but these comparisons have been made between Si wafers with similar resistivities (in the 1-5 Ωcm range). J_0 values are also plotted in Figure 5.4(d), with a value of 37.1 fA/cm^2 at 475 °C and a minimum of 28.4 fA/cm^2 at 500 °C. There is a lack of direct reporting of J_0 values for HfO_2 passivated surfaces in the literature, but one recent paper reports values an order of magnitude higher than what is reported in this chapter [146].

5.4 Distinguishing between surface and bulk effects

As the effective lifetime is determined by competing bulk and surface effects, it is important to ascertain whether bulk or surface (or both) effects are responsible for the activation temperature dependence shown in Figure 5.4. This balance was not considered in prior studies of HfO_2 passivation [21-24], so it has not yet been proven that there is a peak temperature for HfO_2 passivation activation.

5.4.1 Superacid re-passivation

By removing the HfO_2 passivation and re-passivating the samples with a temporary superacid-based passivation scheme it is possible to measure the effective lifetime consistently with the same surface recombination level to deduce information on the bulk lifetime. Figure 5.5(a) compares the lifetime curves of samples coated with HfO_2 and the same samples when re-passivated with the superacid-based approach after

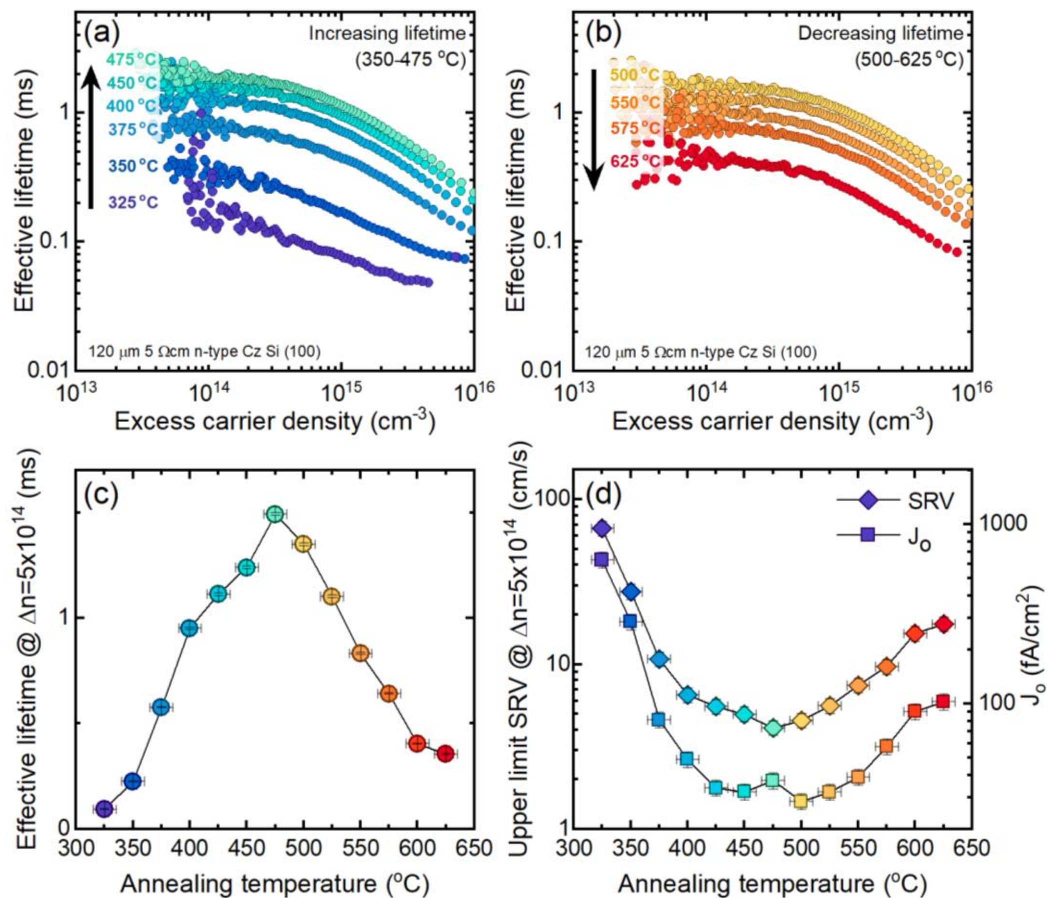


Figure 5.4: (a) Lifetime curves for ~12 nm (100 cycles) of ALD deposited HfO_2 films on 120 µm 5 Ωcm n-type Cz-Si wafers, annealed at various temperatures (300-475 °C) for 30 min. (b) Lifetime curves of the same type of samples annealed at higher temperatures (500-625 °C) for 30 min. (c) Effective lifetimes at an excess carrier density of 5×10^{14} cm^{-3} for each annealing time (d) Upper limit SRV values calculated using equation (31) at an excess carrier density of 5×10^{14} cm^{-3}, and single sided J_0 values [153] plotted as a function of activation temperature.

being subjected to activation anneals at three different temperatures: 325 °C, 475 °C, and 625 °C. Effective lifetimes are higher with superacid passivation since this approach provides a short-term SRV <1 cm/s [89, 154, 155] which is better than the investigated HfO_2 layers. The difference in injection dependence between the HfO_2 and superacid curves is likely caused by the lower concentration of fixed charges in the superacid passivation [88, 155]. The injection dependence of the superacid passivated samples is relatively consistent, irrespective of the thermal history of the sample.

Figure 5.5(b) shows a comparison in effective lifetime between HfO_2 passivated and superacid passivated samples, extracted at an excess carrier density of 5 × 10^{14} cm^{-3}. With superacid-passivation, no reduction in effective lifetime was found to occur above 475 °C, which demonstrates that the reduction in effective lifetime at higher activation temperatures with HfO_2 is not due to bulk lifetime degradation.

In fact, there is a slight increase in effective lifetime for higher annealing temperatures which may be due to thermal deactivation of recombination centres within the silicon bulk [159, 160]. This shows that the cause of the decline in effective lifetimes at higher temperatures shown in Figure 5.4 is not related to the bulk of the material, but rather due to a decline in passivation from the HfO_2 films.

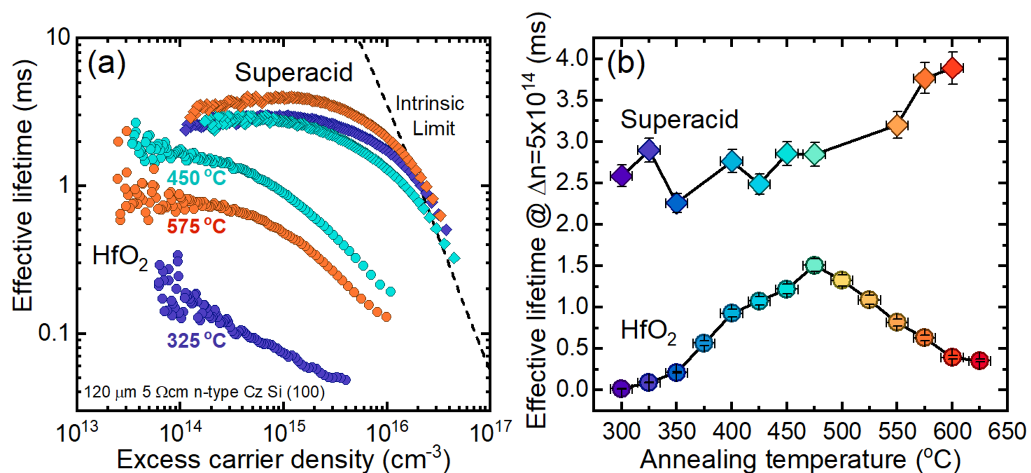


Figure 5.5: (a) Lifetime curves for select HfO_2 passivated samples (circles) activated at the temperatures shown, together with lifetime curves for the same samples after HfO_2 removal and superacid re-passivation (diamonds). The intrinsic limit of Niewelt et al. [152] is also plotted. (b) Comparison between effective lifetimes measured on 120 µm thick 5 Ωcm n-type Cz-Si samples passivated with ~12 nm (100 cycles) of ALD-deposited HfO_2 versus a TFSA superacid solution, taken at an excess carrier density of 5 × 10^{14} cm^{-3}.

Comparing this work to literature, a similar trend in annealing temperature dependence can be seen in the work of Cheng *et al.* who also used Cz-Si in their investigations and found a peak in effective lifetime at 450 °C [24]. Other works, however, have demonstrated peaks in HfO_2 passivation at significantly lower

temperatures. Gougam *et al.* found their lifetimes to peak at 400 °C and Cui *et al.* reached a minimum SRV value at 350 °C [21, 22]. Importantly, these papers used FZ-Si in their investigations, which has been shown to often be prone to degradation above these temperatures [89, 161]. As such, the temperature dependence of the activation of HfO_2 passivation shown in publications using FZ-Si may have been influenced by the effect of bulk degradation. Consequently, it is likely that studies using FZ-Si underestimate the activation temperature required to optimize passivation from HfO_2 films.

5.5 Physical characteristics

It is possible that physical changes within the structure of the HfO_2 films during post-deposition annealing may influence the chemical or field-effect passivation, through changes in, for example, energetically favourable chemical bonds or dielectric constant.

5.5.1 Film crystallinity

GI-XRD measurements were taken to investigate any potential correlation between the passivation quality and film crystallinity of the HfO_2 films. Figure 5.6 shows the XRD spectra for ~12 nm HfO_2 films annealed with the same conditions used in the initial annealing temperature study Figure 5.4. The main crystallographic planes have been indexed based upon monoclinic HfO_2 [142]. A crystallisation stage was identified between 325 °C and 375 °C, at which point the films transition from a mostly amorphous state to a distinct crystallised structure. Notably, there is no significant change in peak intensity or peak position within the films annealed above 375 °C, whereas effective lifetimes continue to improve up to 475 °C and degrade at higher temperatures. It is therefore inferred that, once the film has initially crystallised, the passivation quality is not directly related to the HfO_2 film crystallinity. This is not unexpected as it has been established that, in general, crystallinity is not necessary to activate the passivation of dielectric films. Al_2O_3, for example, provides excellent

passivation whilst in an amorphous state [162]. Furthermore, titanium dioxide (TiO_2) provides decreased passivation quality with higher annealing temperatures, as the film transitions from an anatase to rutile phase [163, 164].

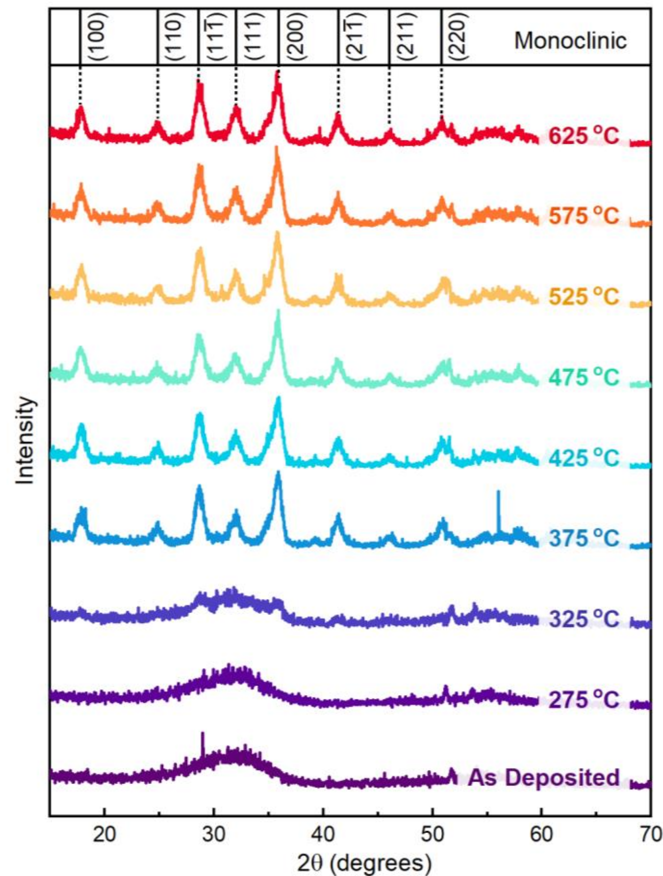


Figure 5.6: GI-XRD measurements, using Cu $K_{\alpha 1/2}$, taken from polished silicon wafers coated with ~12 nm (100 cycles) of hafnium oxide grown via ALD, annealing in air for 30 min at temperatures ranging from as-deposited (200 °C) to 625 °C. The main crystallographic planes present are labelled at the top. Spectra are vertically offset for clarity.

5.6 Electrical characteristics

Measurement of certain electrical characteristics, such as effective work function and dielectric charge, can reveal how the contributions of chemical and field-effect passivation mechanisms change with annealing temperature.

5.6.1 Contact potential difference

Kelvin probe measurements can be used to determine the work function of a material [165], which is important when considering factors like conductivity and charge carrier tunnelling probability. For complex structures including dielectric layers, an 'effective' work function can be used to extract information about the charge in the dielectric layer [117].

The relation between activation annealing temperature and the effective work function of ~12 nm HfO_2 films deposited on silicon can be seen in Figure 5.7(a). At low annealing temperatures the effective work function of the HfO_2 films is around 4.6 eV. This remains relatively constant until the temperature reaches 375 °C, where the effective work function begins to increase up to 5.1 eV at 450 °C. The effective work function then remains relatively stable for all higher annealing temperatures investigated. Interestingly, the initial turning point roughly corresponds to the crystallisation of the HfO_2 films, as determined *via* XRD, whereas the second turning point at 450 °C is close to the 475 °C annealing temperature which produces the best effective lifetimes. From this, a potential link can be inferred between the observed enhancement in measured lifetime and the effective work function, which may result from varying charge within the dielectric layer [117]. It is also possible that the initial shift in effective work function relates to changes within the physical structure of the HfO_2 layer as it crystallises, which impact the dielectric constant. The plateau in effective work function at higher annealing temperatures suggests that the decrease in effective lifetime occurs due to a different mechanism than changes in the crystallinity or effective work function, and thus is likely chemical in nature.

5.6.2 Surface photovoltage

To investigate the surface charge polarity of the HfO_2 films, SPV was used, which is determined by measuring the difference in CPD in the dark compared to under illumination. An example of this can be seen in Figure 5.7(b), where the shaded regions

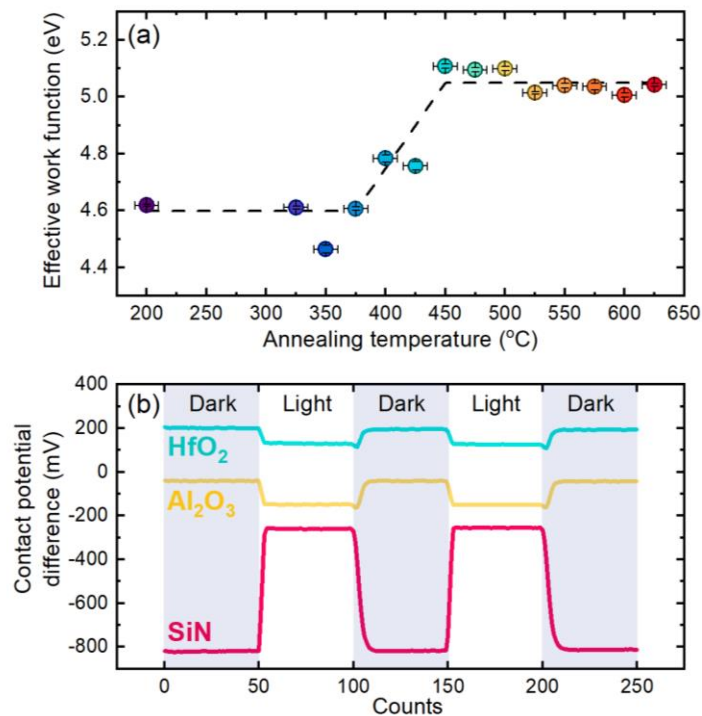


Figure 5.7: (a) Effective work functions of ~12 nm HfO_2 films deposited on 120 µm thick 5 Ωcm n-type Cz-Si wafers and annealed for 30 min at different temperatures, as determined from Kelvin probe measurements, with the dashed curve providing a guide to the eye. (b) Contact potential different (CPD) data measured under dark and light conditions for an ALD HfO_2 film annealed at 475 °C, an ALD Al_2O_3 film annealed at 460 °C, and a PECVD SiN film.

represent data points measured in the dark, and non-shaded regions measured under illumination. For all annealing temperatures, the SPV of the HfO_2 films was negative. To support these results, the CPD response of the HfO_2 was directly compared to Al_2O_3 (known to have a negative charge) and SiN_x (known to have a positive charge) [166]. These results match those of Aubriet *et al.* [67]. Literature shows evidence for either positive [21, 26] or negative [24, 25] fixed charges in HfO_2 films, though the exact mechanisms through which a certain charge polarity is achieved is currently unknown. Suggestions have been made that incorporation of Cl or N_2 may produce a negative charge polarity [20, 23]. It is important to note that a range of different hafnium-containing precursors have been used to create HfO_2 films by ALD, including TDMAH [24], tetrakis(methylethylamide)hafnium (TEMAH) [21-23, 167], $HfCl_4$ [20], and trimethylhafnium [25], and this may explain variations in charge polarities reported.

5.6.3 Field-effect vs chemical passivation

To assess the magnitude of charge in our HfO_2 films, positive corona charging of the surface was used to neutralise the negative fixed charge. As net charge is neutralised, field-effect passivation decreases, and thus effective lifetime decreases [167]. As further charge is deposited onto the surface of the passivating layer, the field-effect passivation and hence effective lifetime increases again. The amount of corona charge deposited onto the surface, Q_{corona}, that is required to reach the minimum effective lifetime, τ_{min}, provides an indication of the amount of charge initially present. Since, at the minimum lifetime value, the field-effect is neutralised and only chemical passivation remains, we use τ_{min} as a measure of the level of chemical passivation given by the film. It has been assumed that the capture cross-sections for carrier recombination are not influenced by factors such as recrystallisation and, as such, remain consistent across measurements.

Examples of corona charge curves for ~12 nm thick samples of HfO_2, annealed at different temperatures for 30 min in air, can be seen in Figure 5.8. A clear minimum value can be seen for each curve, at which point the data for Q_{corona} and τ_{min} are extracted. In all cases, the effective lifetime rises again as positive charge continues to be applied, as field-effect passivation of positive polarity increases. The recovery in lifetime indicates that the charge leakage is minimal over the timescales considered.

The applied positive corona charge to neutralize the negative charge within the HfO_2 layer, plotted in Figure 5.9(a), shows a significant increase between 300 and 425 °C. The implied level of charge in the films then begins to plateau around 2×10^{12} qcm^{-2}, before gradually decreasing, as the annealing temperature increases. This level of charge is broadly consistent with some previous studies, where negative HfO_2 is found to be on the order of 10^{11}-10^{12} qcm^{-2} [20, 23-25]. Based upon the trends observed in Figure 5.6, Figure 5.7(a), and Figure 5.9(a) , it is possible that the crystallisation has an influence on the effective charge density within the film and, by extension, the effective work function.

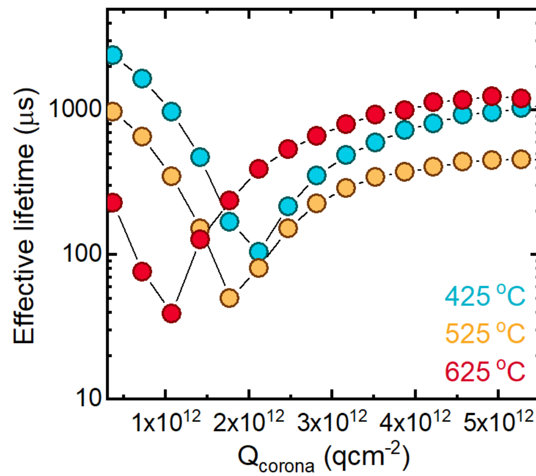


Figure 5.8: Corona charging curves showing effective lifetime, extracted at an excess carrier density of 1×10^{15} cm^{-3}, of ~12 nm HfO_2 passivated 150 µm 5 Ωcm n-type Cz-Si samples as positive corona charge is increased, at a range of selected activation temperatures.

The minimum lifetime reached for each temperature is shown in Figure 5.9(b), which provides an indication of the annealing temperature dependence of chemical passivation. The trend is broadly consistent with the trend in lifetime values shown in Figure 5.4(c), with lifetimes increasing and then decreasing as annealing temperature increases. Figure 5.9(b) shows that chemical passivation peaks around 425 °C. Cheng *et al.* also found a similar temperature dependence of chemical passivation, with their density of interface states (D_{it}) reaching a minimum at 450 °C [24]. This trend suggests that chemical passivation may be the dominant factor when considering the decrease in passivation quality, especially when considering the bulk lifetime of the wafers used in this study was found to increase with annealing temperature.

Using the values for Q_{corona} and τ_{min} as a guideline, the lifetime curves from Figure 5.4(a) and (b) were modelled. Given the injection range of these curves, it was not possible to extract exact values of Q_f and D_{it}. However, it was possible to quantify the relative changes in these parameters between high and low lifetime curves. The passivation enhancement between 325 °C and 475 °C can be attributed to a 75 % decrease in D_{it} and a 100 % increase in Q_f. Between 475 °C and 625 °C, D_{it} returns towards its initial value, whereas the relative decrease in Q_f is only 10 %, This

simulation supports this work's claim that passivation enhancement is a contribution of both chemical and field-effect mechanisms, and the decrease in passivation quality at higher temperatures is chemical in nature.

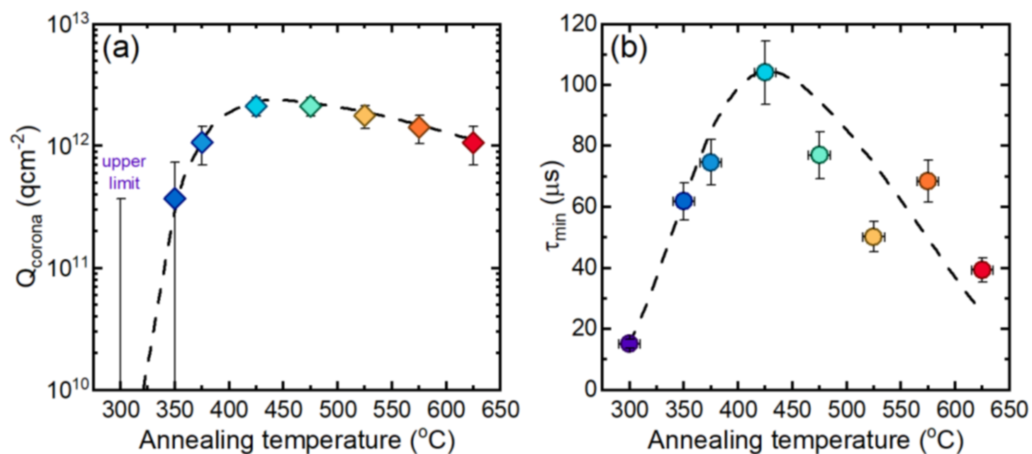


Figure 5.9: (a) The positive corona charge required to minimize the effective lifetime (i.e. neutralize the negative field-effect passivation), as a function of activation temperature. (b) The minimum lifetime reached during corona charging as a function of annealing temperature, which is indicative of the level of chemical passivation. The dashed curves in (a) and (b) provide a guide to the eye.

5.7 Conclusions

This chapter has studied the mechanisms underpinning the post-deposition activation annealing conditions for HfO_2 films on Si deposited *via* ALD, determining a preferred annealing time of 30 min, annealing ambient of air (rather than Ar or N_2), and a distinct temperature dependence. Effective lifetime peaks at an annealing temperature of 475 °C, with a minimum SRV value of 4.1 cm/s and corresponding single sided J_0 value of 37.1 fA/cm^2. Above this temperature, effective lifetime steadily decreases which, through use of room temperature superacid re-passivation, has been shown not to be due to bulk lifetime degradation.

GI-XRD revealed a distinct crystallised monoclinic HfO_2 structure in all HfO_2 films annealed above 375 °C, with crystallisation occurring between 325 and 375 °C. This temperature range coincides with an initial increase in measured lifetime, with further lifetime variations not corresponding to changes in film crystallinity. Kelvin probe

measurements indicated a potential relationship between initial passivation enhancement and a positive effective work function shift between 375 and 450 °C. Through a combination of SPV measurements and positive corona charging, it was determined that the HfO_2 films have a negative charge polarity. The maximum charge density was observed after 425 °C annealing and was on the order of 2×10^{12} qcm^{-2}.

Analysis of the corona charging results highlighted a significant change in negative charge density within the HfO_2 layer as it crystallises, with the charge density reaching its peak around the optimal annealing temperatures for best lifetime values. This was followed by a gradual decrease in negative charge as lifetime decreases at higher annealing temperatures. Investigations into chemical passivation indicated a very similar trend between chemical passivation and effective lifetime as functions of annealing temperature. Overall, the results suggest a combined contribution of chemical and field-effect mechanisms is responsible for passivation enhancement, with similar relative changes in D_{it} and Q_f. The decrease in passivation quality at higher temperatures is likely dominated by chemical factors.

In conjunction with the well-known properties of HfO_2 (e.g. electrically insulating, high dielectric constant, and chemically resistant), this work has demonstrated that thin HfO_2 layers can provide a very high level of passivation. Understanding of passivation mechanisms in HfO_2 enables further investigation into enhancement of passivation quality and ultimately incorporation of HfO_2 into various photovoltaic architectures.

5.8 Future Work: Passivation enhancement

Through distinguishing between the contributions of chemical and field-effect passivation mechanisms, it becomes simpler to investigate potential methods for enhancing the passivation quality. For example, to prevent passivation degradation occurring at higher annealing temperatures, it is necessary to focus on improving the chemical passivation provided by the HfO_2 films.

Since, for these HfO_2 films, the initial increase in passivation quality, at lower temperatures, is influenced by both chemical and field-effect passivation, there is the potential to improve this by either increasing the charge within the dielectric layer, or by improving the chemical passivation. This section demonstrates preliminary investigations into this concept, attempting to focus on the former of these approaches, though there has also been some work reported on the latter option [168].

5.8.1 Annealing Ambient

As shown in Table 2.1, there is no obvious cause for variations in charge polarity of HfO_2 films. Some literature suggests that inclusion of Cl or N_2 in the process will result in an increase in negative charges within the film [20, 23]. To investigate whether the charge of HfO_2 films can be controlled by introducing elements through ambient anneals, a quartz tube furnace was used to anneal HfO_2 films in various ambients, at 475 °C for 30 min. The effective work function and lifetime of the samples was measured, before being subjected to positive corona charging. The results of this study can be seen in Figure 5.10.

Initial effective lifetime values, as seen in Figure 5.10(a) show a similar trend to those in Figure 5.2, as would be expected. After corona charging, a similar trend can be seen in the minimum lifetime values in Figure 5.10(b), although relative changes are much smaller. Since field-effect is neutralised at the minimum point, this would indicate that annealing in air provides the best chemical passivation, followed by N_2 and then Ar.

Focusing on the change in charge within the dielectric layer, as seen in Figure 5.10(c), it is apparent that air provides the highest level of charge, at approximately 1×10^{12} qcm^{-2}. N_2 and Ar both produce a similar amount of around 6×10^{11} qcm^{-2}. However, this variation in charge is relatively small, and would fall within the bounds of uncertainty for this experimental setup. It is, therefore, still possible that all three ambients provide similar levels of charge. This is supported by the effective work

function measurements in Figure 5.10(d), which are indicative of dielectric charge, and show very little change, regardless of annealing ambient.

In this particular case, it is apparent that varying the annealing ambient does not provide a route to increasing the dielectric charge to any significant degree, though may somewhat influence the chemical passivation. These results are likely dependent upon the hafnium precursor used in the deposition process.

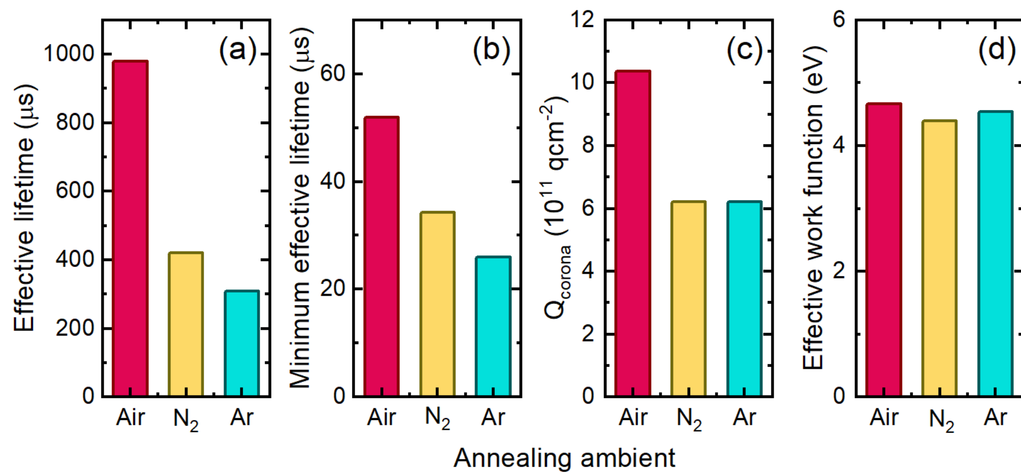


Figure 5.10: Comparison of HfO_2 films annealed in air, N_2, and Ar ambients. (a) Initial effective lifetime values, extracted at 1×10^{15} cm^{-3}. (b) Minimum lifetime values, extract at 1×10^{15} cm^{-3}, achieved from corona charging. (c) Corona charge corresponding to the values in (b). (d) Effective work function values, measured before corona charging.

5.9 Contributions

The content of this chapter has been published [70] and parts of the text have been included verbatim. The reported results include experimental contributions from Sophie Pain in the form of superacid deposition.

Chapter 6

The Potential of HfO_2 Thin Films as Passivating Contacts

This chapter investigates the potential of nanometre-scale HfO_2 films deposited by atomic layer deposition for passivating contacts to silicon focusing on variations in film thickness. A peak in passivation quality as assessed by lifetime measurements, is reported for 2.5 nm thick films annealed at 475 °C, for which a surface recombination velocity <1 cm/s is determined. For samples <2.5 nm thick, there is a marked decrease in passivation quality. X-ray diffraction highlights a change from crystallised monoclinic HfO_2 to amorphous, as film thickness decreases from 10 nm to 2.5 nm. An initial investigation into a passivating contact structure utilizing HfO_2 reveals a strong annealing temperature dependence, with the lowest resistance achieved below 375 °C, followed by a decrease in performance as temperature increases towards the optimal temperature for passivation (475 °C). Limitations in the existing contact structure are discussed.

6.1 Motivation

Many cell architectures that currently dominate the silicon PV market are limited by recombination losses due to direct metal/Si interfaces at the electrode. However, these losses can potentially be mitigated by the inclusion of a passivating interlayer between the Si and metal, preventing recombination in the contacted region without significant reduction in contact conductance [13, 169-172]. Such interlayer structures are referred to as passivating contacts.

The most promising passivating contact structures for silicon solar cells thus far have been amorphous silicon (a-Si) heterojunction (HJT), tunnel oxide passivated contact (TOPCon), and polysilicon on oxide (POLO) architectures [13, 42, 173]. Where dielectric films have been used, existing literature has focused on SiO_2 and Al_2O_3 due to their established performance as passivating layers, and their respective positive and negative fixed charges [174-178]. In the case of SiO_2, pinholes that are produced at high temperatures enable the material to be utilised for both electron and hole extraction [15, 16]. However, the band off-sets of SiO_2 strongly indicate electron-favourability, which is reflected in the higher performance as an electron-selective layer, rather than hole-selective [19]. A hole-selective contact that can match the performance of existing electron-selective contacts is yet to be produced.

Hafnium oxide (HfO_2) is a dielectric material with existing application in transistors and capacitors [132, 133], and has shown promise in recent years in the area of passivating layers for silicon photovoltaics [21, 22, 24, 70]. Literature demonstrates that HfO_2 passivating films perform particularly well at ultra-thin thicknesses, below 3 nm, outperforming Al_2O_3 layers of a similar thickness [71]. This is especially useful for passivating contacts, as dielectric layers inherently have high resistance and so must be kept very thin to facilitate charge carrier transport mechanisms. The mechanisms involved for charge carrier transport are still under debate, but two main explanations are quantum tunnelling and/or pinholes [179]. As discussed in section 2.2.1, The probability of charge carrier tunnelling increases as film thickness decreases [48]. Consequently, the thinner the film, the higher the probability of charge tunnelling and hence the greater charge carrier transport can be.

Interestingly, HfO_2 can be either positive or negatively charged. There is currently no consensus on the mechanisms that result in charge polarity, though there have been some suggestions that the choice of precursor or annealing ambient may have an impact [20, 23]. Table 2.1 provides a review of existing literature where HfO_2 fixed charge is reported, alongside the deposition technique, post-deposition treatment, and measurement approach used. The charge of a dielectric layer plays an important

role in determining the selectivity of a passivating contact. Since HfO_2 can have either charge polarity, it lends itself to potential applications in both electron and hole selective contacts. Previous literature has shown that whilst the ratio of band off-sets for negatively charged HfO_2 indicates electron favourability, the potential barrier for hole transport is lower than in both Al_2O_3 and SiO_2 [19].

This chapter further investigates the characteristics of negatively charged ultra-thin HfO_2 layers, focusing of thickness dependence, through photoconductance decay lifetime, x-ray diffraction (XRD), and Kelvin probe measurements. This is reported alongside an initial study into an Au/*n*Si/HfO_2/Al contact structure, containing a negatively charged HfO_2 layer, through the Expanded Cox and Strack method (ECSM). Potential limitations within the contact structure and the HfO_2 layer itself are discussed.

6.2 Experimental Details

This section reports specific details relating to the apparatus and experimental processes utilised within this chapter. For general information relating to methodology and theory, please refer to Chapter 3.

6.2.1 Dielectric layer deposition

5 x 5 cm samples were fabricated from 150 µm thick, 5 Ωcm, *n*-type or *p*-type Cz-Si (100) wafers. These samples were first cleaned with an established process [89], involving 10 min in each of the following solutions, heated to 80 °C: RCA1 (DI H_2O, NH_4OH (30%), and H_2O_2 (30%) in a 5:1:1 ratio), tetramethylammonium hydroxide (TMAH (25%)), and RCA2 (DI H_2O, HCl (37%), and H_2O_2 (30%) in a 5:1:1 ratio). Before each cleaning and etching step, a DI water rinse and 60 s HF (1%) dip was conducted. The cleaning process was concluded with submersion in either a 1% HF/1% HCl solution (for XRD and lifetime measurements) or 2% HF solution (otherwise) until the

samples became hydrophobic (approximately 10 s). No water rinse was performed prior to film deposition.

HfO_2 films were grown *via* plasma-enhanced ALD (PE-ALD) using a Veeco Fiji G2 system, with tetrakis(dimethylamido)hafnium (TDMAH) and O_2 plasma as the precursor and co-reactant, respectively. Argon was used as the inert purge gas. The TDMAH precursor, heated to 75 °C, was pulsed into the chamber for 0.25 s, followed by a 6 s pulse of O_2 plasma at 300 W. A 5 s purge was conducted before and after each step. The growth rate, for a deposition temperature of 200 °C, is approximately 1 Å/cycle (as reported by the supplier [180], and verified in previous work with this apparatus [71]). This growth rate is used when referring to estimated film thickness in this work. The samples were then either left as deposited, or annealed ex-situ in air in a quartz tube furnace for 30 min at 475 °C.

6.2.2 Film characterisation

Photoconductance decay charge carrier lifetime measurements of double-sided samples (Figure 6.1(a)) were performed at room temperature, using a Sinton Instruments WCT-120PL lifetime tester (software version 5.74). The measurements were conducted in a transient mode and averaged over five flashes.

Film crystallinity was investigated using grazing incidence X-ray diffraction (GI-XRD). These measurements require using thicker, mirror polished Si wafers, as depicted in Figure 6.1(b). Measurements were conducted using a 3rd generation Malvern Panalytical Empyrean XRD Diffractometer, with multicore optics (iCore, iCore), and a Pixcel3D detector, under Cu $K_{\alpha1/2}$ radiation. An incidence angle of 0.5° was used for all measurements. 2θ measurements were taken in a range of 15°–70°, with a step size of 0.3°. For samples coated with 10 cycles HfO_2, the step size was reduced to 0.2° in an attempt to improve the signal to noise ratio and improve detection of the ultra-thin film. Data were fitted using the Malvern Panalytical data analysis software HighScore Plus.

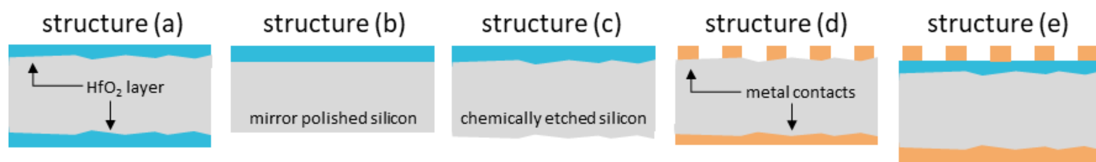


Figure 6.1: Schematics of the various sample structures considered in these investigations. These images are designed as visual aids and are not to scale. (a) Double sided HfO_2 films on textured n-type Si for lifetime measurements. (b) Single sided HfO_2 on mirror polished Si for XRD measurements. (c) Single sided HfO_2 on textured n-type Si for Kelvin probe measurements. (d) Full area rear metal contacts and patterned front metal contacts for optimisation of the rear contact structure. (e) A completed sample with full area rear contact, front side HfO_2 layer, and patterned front contact.

6.2.3 Contact fabrication

Photolithography was performed using an AZ2035 photoresist (MicroChemicals), spin-coated at 5000 rpm for 50 s, with a 5 s ramp step, and soft baked at 110 °C for 60 s. Samples were then exposed to UV light through a photomask consisting of rows of circles, which varied in size from 1.4–2.4 mm in diameter. UV exposure was conducted using a Suss MicroTec BA8 Gen3 mask aligner in hard-contact mode, with an equivalent dose of 120 mJ/cm^2. This was then followed by a hard bake at 110 °C for 90 s, and development in an MF-319 (MICROPOSIT) solution for 35 s.

200 nm Al or 100 nm Au metal contacts were deposited using a Scientific Vacuum Systems Ltd electron-beam (e-beam) evaporation system. The exposed Si was etched *in-situ* using an integrated ion beam gun to remove any native oxide before the deposition of the full-area rear contact. Metal lift-off was then performed by leaving samples in dimethyl sulfoxide (DMSO) overnight.

The IV characteristics of direct metal-Si contacts, as depicted in Figure 6.1(d), for *n*- and *p*-type wafers with Al and Au can be seen in Figure 6.2. Figure 6.2(a) shows the IV curve of an *n*-type sample with a full area Al rear contact and 2.4 mm diameter Al front contact (labelled Al/*n*Si/Al). The initial IV data produces a curved plot, rather

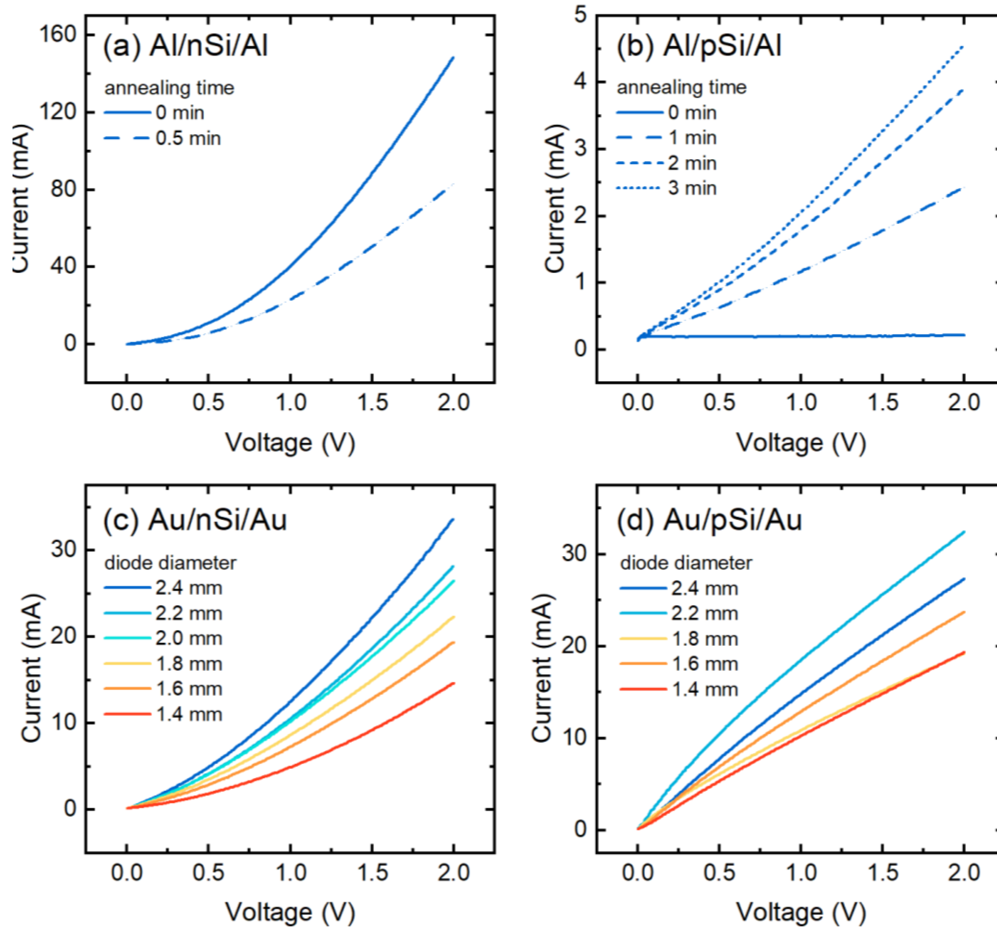


Figure 6.2: Current-voltage characteristics of various direct metal-Si contact structures (corresponding to structure (d) in Figure 6.1), with full area rear contacts and mm-scale circular front contacts. (a) Al/nSi/Al, with a 2.4 mm diameter front contact, before and after a 30 s sintering step at 400 °C in air. (b) Al/pSi/Al, with a 2.4 mm diameter front contact, after successive sintering steps. (c) Au/nSi/Au, un-sintered, for various front diode sizes. (d) Au/pSi/Au, un-sintered, for various front diode sizes.

than linear, indicating a non-ohmic contact. Sintering for 30 s at 400 °C begins to straighten the curve but results in a reduced current. The equivalent structure on *p*-type Si (Al/*p*Si/Al) initially produces a negligible current flow after deposition, implying a bad contact structure. This can be improved significantly through sintering, as demonstrated in Figure 6.2(b); however, the current values are still substantially lower than the Al/*n*Si/Al structure and deviate from ideal ohmic linearity.

Using Au results in similar current values for both *n*- and *p*-type samples, being higher than achieved for the Al/*p*Si/Al structure, but lower than the Al/*n*Si/Al structure, as seen in Figure 6.2(c) and (d). Having direct metal-Si rear contacts that behave similarly for both wafer types is beneficial when making comparisons between the effectiveness of different metal-dielectric-Si front contacts, as the effects of the rear contact can be considered consistent throughout. The IV curves are also relatively ohmic, though not completely ideal. This deviation from an ideal ohmic response may be due to the growth of a native oxide during the photolithography process. Importantly, not requiring a sintering step reduces the processing complexity and thermal budget of the sample development. Based upon these results, all sample structures considered in the rest of this work include a full area Au rear contact.

Current-voltage (IV) measurements were conducted using a Wentworth probe station with an Agilent B1500A Parameter Analyser. Figure 6.1(d) and (e) show the sample structures considered. The resultant IV data was analysed using the Expanded Cox and Strack Method (ECSM) as discussed in section 3.3.6 [126-128].

6.3 Characterisation of ultra-thin HfO_2 films

This section investigates the structural changes within HfO_2 films as the thickness is varied, and the effect that this has on the passivation quality.

6.3.1 Passivation potential

In order to demonstrate the effectiveness of ultra-thin HfO_2 films as passivation layers, Figure 6.3(a) shows the effective lifetime curves of samples with HfO_2 layers of varying thickness, deposited on *n*-type Si wafers and annealed for 30 min at 475 °C, structured as in Figure 6.1(a). Figure 6.3(b) shows effective lifetime values for each of these samples, extracted at an excess carrier density of 10^{15} cm^{-3}. A clear trend can be seen, with the effective lifetime increasing as film thickness decreases from approximately 10 nm to 2.5 nm. However, the passivation quality then rapidly decreases for thinner

films, with the effective lifetime dropping by an order of magnitude. These results are in line with previous investigations, which found that passivation peaks at a HfO_2 film thickness between 2.2–3.3 nm, achieving surface recombination values (SRVs) as low as 2.5 cm/s [71]. The effective lifetimes determined here for ~2.5 nm (25 cycles) of HfO_2 correspond to an SRV of 0.6 cm/s, the lowest SRV to date, and competitive with more conventional Al_2O_3 passivation [88]. J_0 values are also plotted in this figure, as well as in Figure 6.4. Whilst SRV values often require an assumption of bulk lifetime, or intrinsic limit, J_0 is less reliant upon these assumptions, and is typically less injection-dependent [181-183]. J_0 values are particularly useful for considering the performance of a structure when incorporated into a full cell, rather than the individual performance of the layer/interface itself.

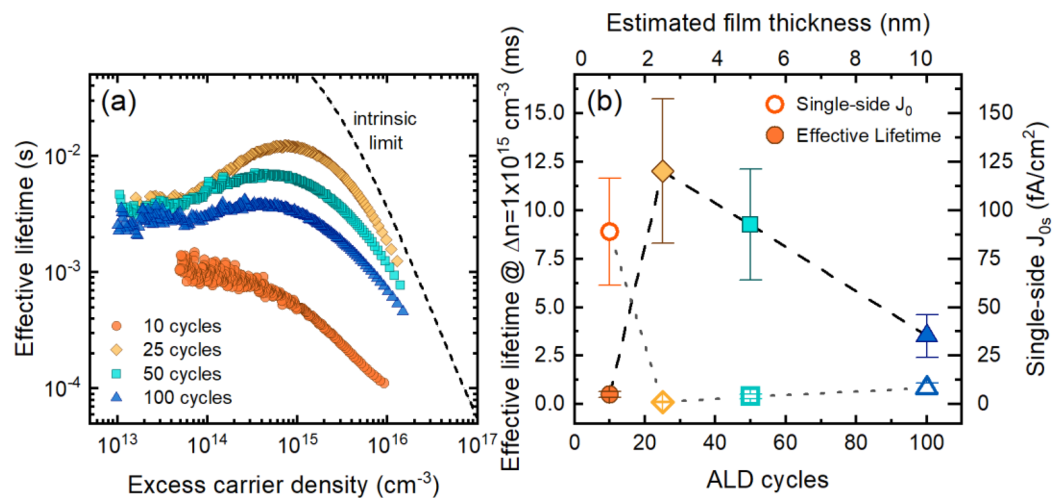


Figure 6.3: (a) Measured effective lifetime curves for different HfO_2 films (10–100 cycles, corresponding to 1-10 nm estimated thickness), deposited via PE-ALD, on 150 µm 5 Ωcm n-type Cz-Si (100) wafers, annealed in air at 475 °C for 30 min. The intrinsic lifetime limit of Niewelt et al. [152] is also plotted. (b) Single-side J_0 values, and effective lifetimes, extracted at an excess carrier density of 1×10^{15} cm^{-3}, for each film thickness in (a). Error bars correspond to the relative variation in measured values experienced between samples.

Figure 6.4 shows a comparison between the annealing temperature dependence of effective lifetimes for 'thin' and 'thick' HfO_2 films, with estimated thicknesses of 1 nm (10 cycles) and 10 nm (100 cycles), respectively. Notably, the relation between annealing temperature and effective lifetime remains consistent, regardless of film

thickness, with optimal results found around 450 °C [70, 71]. This implies a promising outlook on the application of HfO_2 films in passivating contacts processed with a moderate thermal budget – if effective diode structures can be produced using 1–2.5 nm thick HfO_2 layers, annealed around 450 °C.

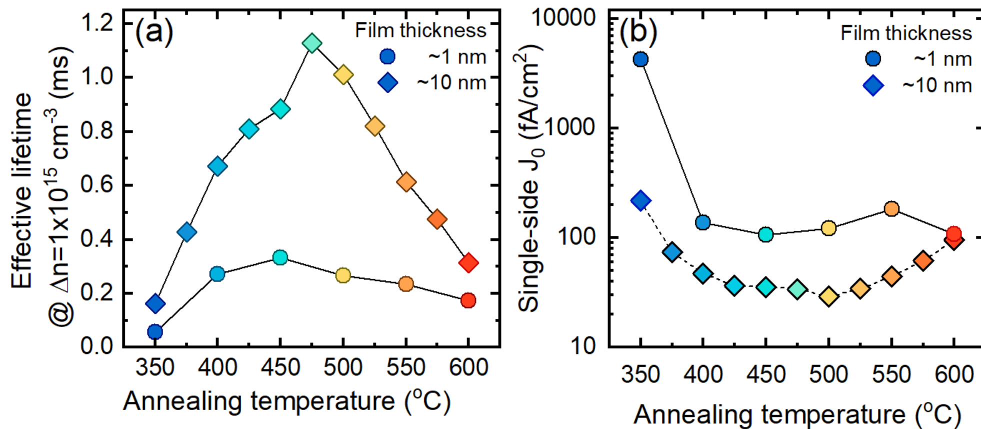


Figure 6.4: (a) Effective lifetimes and (b) single-sided J_0 values extracted at an excess carrier density of 1×10^{15} cm^{-3} of HfO_2 films deposited via PE-ALD, on 150 µm 5 Ωcm n-type Cz-Si (100) wafers, annealed in air for 30 min at temperatures ranging from 350–625 °C. A comparison is made between 'thick' (~10 nm/100 cycles) and 'thin' (~1 nm/10 cycles) HfO_2 films. Effective lifetime data has been previously published in Refs [70, 71]. A discussion on extracting J_0 from the region around 1×10^{15} cm^{-3} can be found in Ref.[183].

6.3.2 Film crystallinity

All films for XRD analysis, as seen in Figure 6.5, were annealed at 475 °C, above the crystallisation temperature window previously observed for 100 cycles HfO_2 [70]. For 50-100 cycles of HfO_2 annealed at this temperature, the peaks present correspond to monoclinic HfO_2 [142], consistent with results reported in previous chapters. The main diffraction peaks corresponding to the monoclinic phase occur at 2θ = 15-45 °, but with decreasing cycle number (and layer thickness), these peaks become broader and less distinct. By 25 cycles of HfO_2, no clear peaks are evident in this region. Instead, there is a low intensity 'hump' between 2θ = 25-35 °, the position of which coincides with a similar feature observed for amorphous ALD-grown HfO_2 in previous chapters [70]. The features seen in the 2θ range of 50°—60° can be attributed to the (311) plane

of the underlying c-Si (100) substrate [184]. Note that though no overlayer peaks could be detected with this set-up, for ~1 nm, this does not necessarily imply that no HfO_2 is present on the surface, as the presence of HfO_2 has been verified *via* XPS [71].

The change in the XRD pattern for ~2.5 nm (25 cycles) of HfO_2 likely indicates that the films are now amorphous. An alternative explanation may be that the film is in a mixed state, where there are regions of both amorphous and crystallised material, but GI-XRD is not able to detect this. Indeed, there are reports of HfO_2 thin films (<4 nm) appearing amorphous by XRD yet being determined as crystalline by other approaches [185]. However, etching studies conducted for HfO_2 films of these thicknesses, based on the results in Chapter 4, suggests the XRD measurements have accurately determined the transition from amorphous to crystalline, with films <5 nm etching rapidly in HF, and films >5 nm maintaining their passivation quality [186].

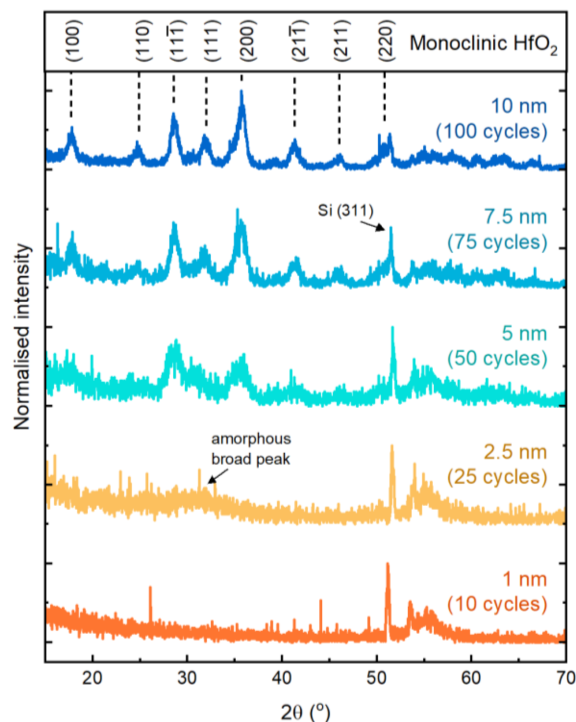


Figure 6.5: GI-XRD measurements, using Cu $K_{\alpha1/2}$, taken from polished silicon wafers coated with 10-100 cycles (corresponding to ~1-10 nm) of HfO_2 grown by ALD and annealed in air for 30 min at 475 °C. The main crystallographic planes present are labelled at the top. Patterns are vertically offset for clarity. To allow comparison, all patterns have been normalised to their most intense peak. The sharp peaks at 2θ = 25° and 33° in the 10 cycles HfO_2 pattern are thought to be artefacts, amplified by the normalisation process.

6.4 Contact optimisation

To maximise c-Si solar cell efficiency, passivation quality needs to be maximised and J_0 minimised [178], with good passivating contacts/interlayers generally having J_0 values of ≪10 fA/cm^2 [178, 187]. However, J_0 is not the only metric under consideration, as contact resistivity (ρ_c) must also be minimised for good cell efficiencies [178]. Although ~2.5 nm (25 cycles) HfO_2 gave the most promising passivation, for contact measurements the HfO_2 should be kept as thin as possible to maximise charge carrier transport, according to equation (5). Prior computational studies show that contact resistivity for HfO_2 is only competitive when the films are ≤1.4 nm thick [19]. Thus ~1 nm (10 cycles) HfO_2 was used as a starting point for passivating contact experiments.

Figure 6.6 compares Al and Au front contacts on top of ~1 nm (10 cycles) of as-deposited HfO_2, for *n*- and *p*-type Si wafers, with full area Au rear contacts, as determined in Figure 6.2. A depiction of this sample structure can be seen in Figure 6.1(e). In all cases, the front contacts remained un-sintered, to avoid damaging the Au rear contacts.

The samples with the strongest diode response were the *n*- and *p*-type Au/Si/HfO_2/Al structures, in Figure 6.6(a) and (b) respectively. The *n*-type variant resulted in higher current values than the *p*-type and had a clearer relation between current and contact size, with smaller diodes resulting in reduced current, as is necessary for the application of the ECSM. However, the shape of these diode curves is not ideal, with an initial current increase, before the forward threshold voltage (at approximately 1.5 V), indicating non-negligible shunting. This shunt could possibly be a result of the e-beam evaporation process, whereby the Al may be driven down to the Si surface, creating a direct Al-*n*Si contact.

In the case of both *n*- and *p*-type wafers, the current values for the Au/Si/HfO_2/Au samples are lower than their Au/Si/HfO_2/Al counterparts, though both still produce a

clear relation between current and contact size, as seen in Figure 6.6(c) and (d). Again, the current values are higher in the *n*-type variant than the *p*-type. The shunt resistance is also less apparent in these structures, though this is difficult to determine due to the shape of the IV curves. In the case of the Au/*p*Si/HfO_2/Au sample structure Figure 6.6(d), there is no consistent threshold voltage across the different contact sizes. Based upon these results, further investigations focus on the use of *n*-type wafers with an Au/Si/HfO_2/Al sample structure.

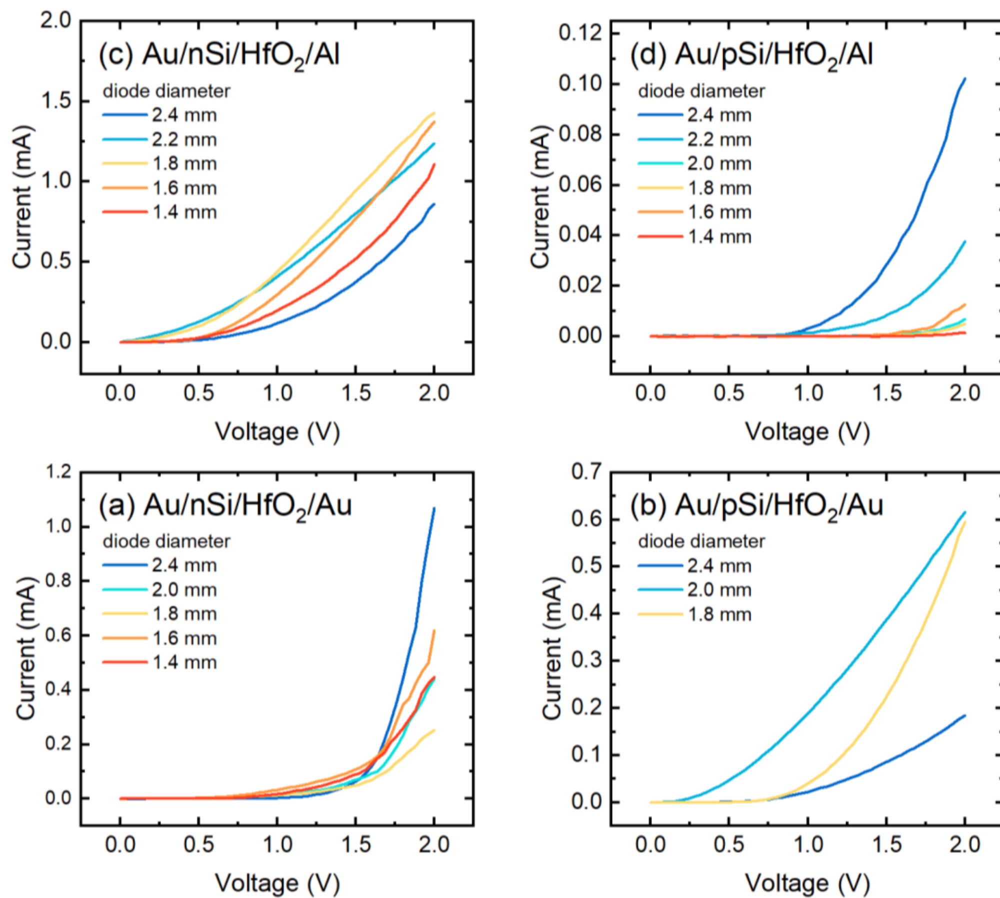


Figure 6.6: Current-voltage characteristics of various metal-HfO_2-Si contact structures, with 1 nm (10 cycles) of as-deposited HfO_2, full area Au rear contacts and mm-scale circular front contacts. Sample structures include: (a) Au/nSi/HfO_2/Al, (b) Au/pSi/HfO_2/Al, (c) Au/nSi/HfO_2/Au, and (d) Au/pSi/HfO_2/Au.

6.5 Variations of the HfO_2 layer

In this section some of the deposition and post-deposition processing conditions of the HfO_2 dielectric layer are varied in order to investigate the effects on the current-

voltage characteristics of the overall structure. Optimal conditions for passivation do not necessarily align with the optimal conditions for conduction.

6.5.1 Film thickness

Figure 6.7(a) shows various IV measurements for different contact sizes, taken on a sample with a ~1 nm (10 cycle) as-deposited HfO_2 layer. Six different contact sizes were considered, with three measurements taken for each contact size. In general, the samples show an approximate diode response, with current decreasing as contact size decreases, which is the required behaviour to apply the ECSM. However, the existence of some form of shunting, notable below the forward threshold voltage at 1.5 V, complicates the situation. This shunt appears to be more pronounced for larger contact sizes and has a negligible impact on the reverse bias measurements. Additionally, the results are relatively inconsistent between contacts of the same geometry, with some contacts producing considerably different IV curve characteristics, for example the blue curve in Figure 6.7(a). Overall, this data is not ideal for the application of the ECSM.

It is still possible to extract contact resistivity values through the ECSM by selecting consistent IV data across the six different contact sizes; however, these values should rather be considered as an estimate than as an exact value. The result of these calculations, for varying HfO_2 film thickness can be seen in Figure 6.7(b). Contact resistivity values are recorded in the order of 1 Ωcm^2 which, at first glance, would suggest poor performance from the HfO_2 sample structures. However, the difference between 0 cycles of HfO_2 – *i.e.,* Al directly on Si (structure d in Figure 6.1) – and 10 cycles HfO_2 (structure e in Figure 6.1) is on the order of only 100 $m\Omega cm^2$. This indicates that the limiting factor in these measurements is more likely the metallisation than the HfO_2 layer itself. Achieving a contact resistivity 100 $m\Omega cm^2$ is often considered a benchmark, as this is the maximum contact resistivity a full area contact structure can have where no significant power conversion efficiency (PCE) losses occur [13, 19]. The

potential of the HfO_2 layer may become more apparent if included in a better performing contact structure.

The contact resistivity increases substantially with thicker HfO_2 layers, with the value at ~2 nm (20 cycles) an order of magnitude higher than at ~1 nm (10 cycles). By ~3 nm (30 cycles) current values were indistinguishable from the measurement noise of the experimental setup, and so an approximation of contact resistivity was not possible.

Overall, these results would suggest that ultra-thin (<2 nm) as-deposited HfO_2 films show some promise as interlayers in contact structures, though more investigation into the surrounding contact structure is required, to improve contact resistivity values, and to investigate the possible origin of the shunt resistance.

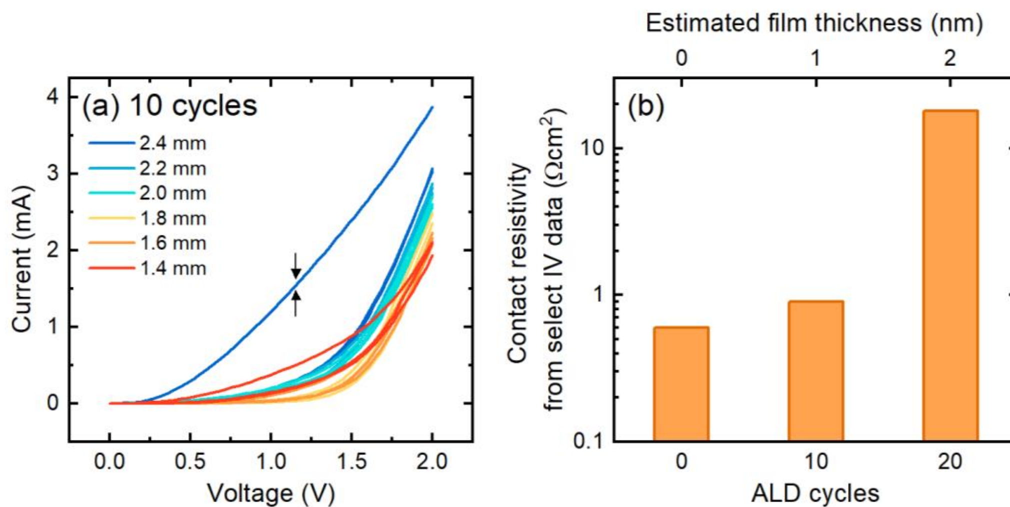


Figure 6.7: (a) Repeated current-voltage measurements, with various contact sizes, for an Au/nSi/HfO_2/Al contact structure (Figure 6.1(e)), with ~1nm (10 cycles) of as-deposited HfO_2 (no activation anneal). The arrows highlight an example of IV characteristics that do not fit the typical diode response. (b) Approximate contact resistivity measurements, calculated from applying the ECSM to select IV data. These values are intended as a guide and should not be used for direct comparison, due to the unsuitability if the approach.

6.5.2 Annealing Temperature

Figure 6.8 shows a plot of conductance (defined as the inverse of resistance), calculated above the forward threshold voltage, against the annealing temperature of a ~1 nm (10 cycle) HfO_2 layer (before contact deposition), with each colour representing a different contact size. Since the contact resistivity values extracted from this data through the ECSM cannot be reported to a high degree of accuracy, it was necessary to use a different metric to compare between samples that resulted in similar levels of performance.

Lower temperature anneals result in higher conductance, with a peak in performance occurring between 275–325 °C. There is then a downward shift in the data, corresponding to an increase in resistance, which then plateaus around 475 °C. This shift in resistance is unlikely to be due to crystallisation of the material, despite the temperature range aligning with the previously determined crystallisation region for thicker HfO_2 films [70], as these ultra-thin films (~1 nm) appear to remain amorphous at these temperatures, demonstrated through the XRD results in Figure 6.5.

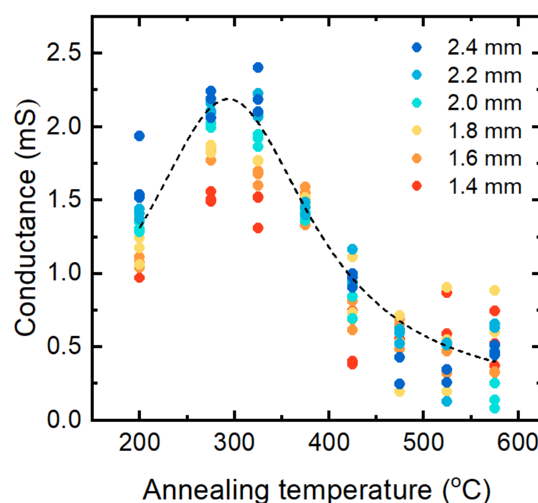


Figure 6.8: A comparison between sample conductance (1/R) and HfO_2 annealing temperature, for an Au/nSi/HfO_2/Al sample structure (Figure 6.1 (e)), with ~1 nm (10 cycles) of HfO_2. Different contact sizes are represented by different coloured data points. The dashed line provides a guide for the eye.

Additionally, the lower temperature samples show a clear relation between resistance and contact size, with larger contacts resulting in lower resistance. This trend is lost for samples annealed above 375 °C, indicating that more complex mechanisms of carrier transport may become involved in this higher temperature region. The loss of a current to contact size dependence is seen in all contact structures considered in this study, once the HfO_2 layer is annealed at temperatures above 375 °C. This can be seen in Figure 6.9.

From these data, it can be concluded that samples annealed at lower temperatures, (<375 °C) create better performing contact structures than those annealed at higher temperatures. This conflicts with the passivating performance of HfO_2 films, in which it has been shown that higher annealing temperatures (~450 °C) are necessary for high quality passivation [70].

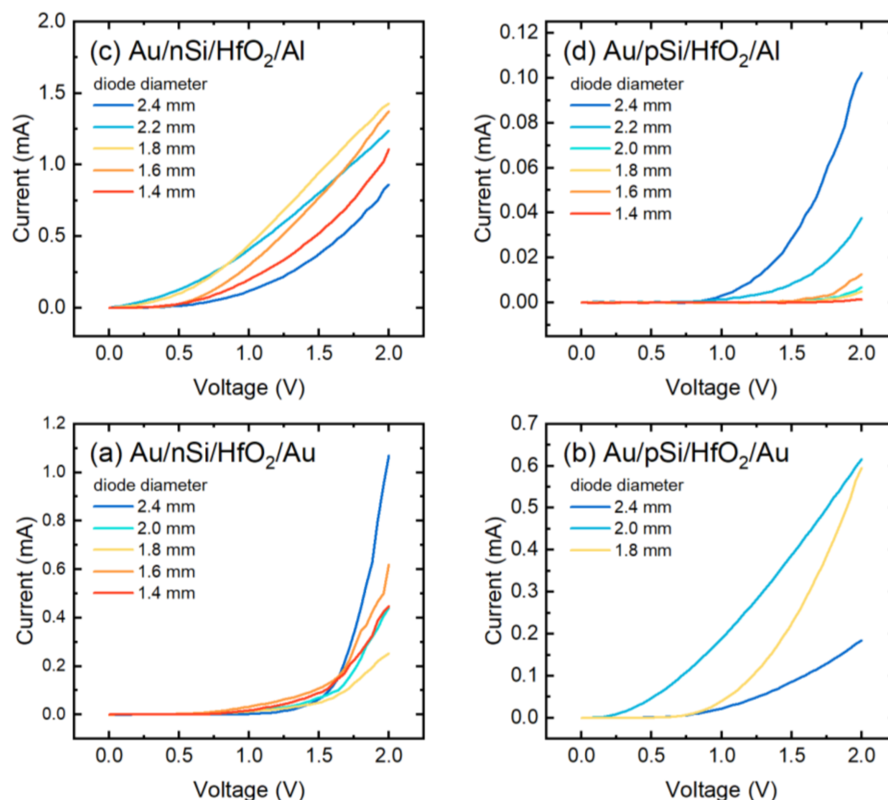


Figure 6.9: Current-voltage characteristics of various mental-HfO_2-Si contact structures, with 1 nm (10 cycles) of HfO_2, annealed at 475 °C in air for 30 min, full area Au rear contacts and mm-scale circular front contacts. Sample structures include: (a) Au/nSi/HfO_2/Au, (b) Au/pSi/HfO_2/Au, (c) Au/nSi/HfO_2/Al, and (d) Au/pSi/HfO_2/Al.

6.6 Enhancing carrier transport

As discussed in section 2.2.1, tunnelling is not the only possible form of carrier transport mechanism. The formation of pinhole structures within some materials, such as SiO_x/poly-Si, can improve conductance by enabling multiple methods of carrier transport [15, 16]. It has been demonstrated in Chapter 4 that stacks of Al_2O_3 and HfO_2 on Si produce potential pinhole structures. There is a possibility that these pinholes may be beneficial for carrier transport, and thus this material stack makes a good candidate to investigate for application as a passivating contact interlayer.

6.6.1 Thin stacks

As reported in this chapter, conductance is highest when films are as thin as possible (~1 nm), however, passivation quality is significantly reduced at this ultra-thin film thickness. The passivation quality of HfO_2 films is maximised at ~2.5 nm. This section investigates whether combining an Al_2O_3 layer with a HfO_2 layer may introduce pinholes that would allow conductance to increase at a total film (Al_2O_3 + HfO_2) thickness of 2-3 nm (20-25 cycles).

Figure 6.10(a) compares the effective lifetimes of three different dielectric structures: HfO_2, Al_2O_3, and an Al_2O_3/HfO_2 stack, all totalling 25 ALD process cycles. It can be seen that the stacked material results in passivation equivalent to a single layer Al_2O_3 film, despite there only being 5 cycles of Al_2O_3 at the interlayer. This is likely due to the passivation from Al_2O_3 mainly being influenced by the dielectric charge that remains in the surface region.

Figure 6.10(b) shows the IV characteristics of a dielectric stack with 5 cycles of Al_2O_3 and 15 cycles of HfO_2, totalling 20 cycles. Unfortunately, the current values obtained for this structure are of the same order of the values obtained for the 20 cycle HfO_2 structure in Figure 6.7(b). This implies that there is no improvement in conductance, and thus no enhancement of carrier transport via pinholes. However, it should be

noted that the stacked structure was annealed at 475 °C, as opposed to the HfO_2 structure in Figure 6.7(b) that was kept in its as-deposited state, thus this is not a direct comparison. It does appear that the inclusion of a 5 cycle Al_2O_3 interlayer somewhat improves the behaviour of the structure, in terms of reliability of IV curves, when compared to the data of annealed HfO_2 structures in Figure 6.9.

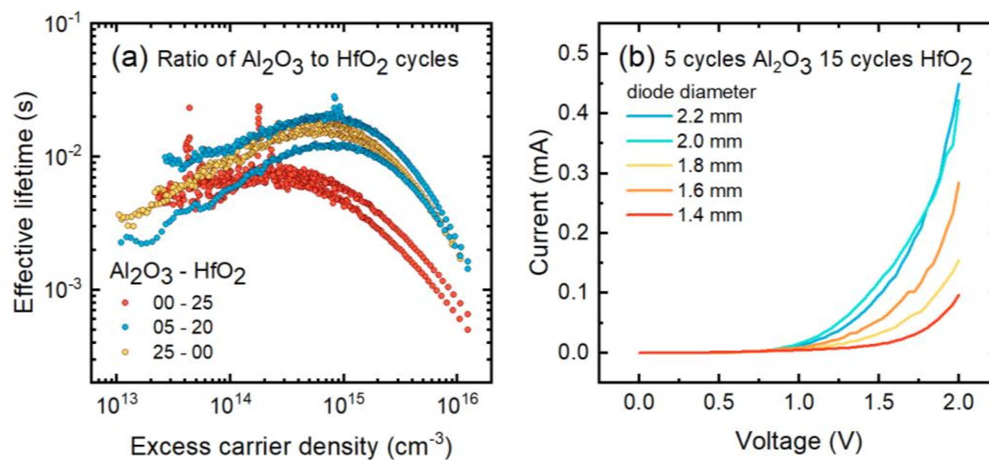


Figure 6.10: (a) Lifetime curves of three difference dielectric stacks, all 2-3 nm thick (25 cycles). The ratio of Al_2O_3 to HfO_2 is varied, with a fully HfO_2 film (red) being compared to a fully Al2O3 film (yellow) and a stack with 20 cycles of HfO_2 and 5 cycles of Al_2O_3 at the interface (blue). (b) IV measurements of a sample with 5 cycles of Al_2O_3 and 15 cycles of HfO_2, totally 20 cycles (~2 nm), in a $Si/Al_2O_3/HfO_2$ stack.

6.6.2 Micro-PERC

Thin stacks of Al_2O_3 and HfO_2 do not appear to produce pinhole transport mechanisms. It may be the case that pinholes are not formed in structures with such thin films, or in these ratio of thicknesses. Thus far such pinholes have only been demonstrated in stacked structures almost 50 nm thick. It may also be the case that the structure of the pinholes themselves may not facilitate carrier transport. However, it is still possible to utilise these pinholes in another way.

As depicted in Figure 4.7, when a $Si/Al_2O_3/HfO_2$ structure is etched in a TMAH solution, etch pits are formed in the Si substrate, with channels the shape and width of the etch pit left in the dielectric layers above. If a metal is then deposited over the top of this structure, then some metal may be deposited in channels which make contact with

the Si surface. This essentially creates a passivated surface with micro-scale regions of direct metal-Si contact. This structure is similar to the rear design of a PERC cell, though produced in a self-forming manner without the need for patterned etching or laser ablation. The regions of direct metal-Si contact are also much smaller in scale. Hence, this structure has been coined ‘micro-PERC’. A schematic of the process can be seen in Figure 6.11.

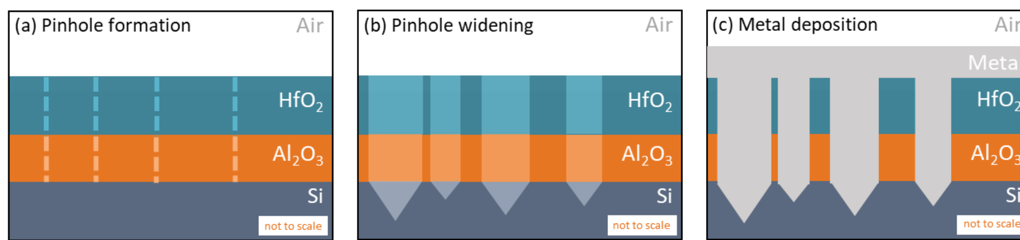


Figure 6.11: A schematic of the production of a micro-PERC structure. (a) Initial pinhole formation, where the exact form of these pinholes is still unknown. (b) The intentional expansion of pinholes through immersion in an etching solution. (c) Metal deposition, potentially aided with a heat treatment to allow metal through the channels to the Si surface.

For this study, the contact structure was changed from Au rear and Al front, as in the previous sections, to Al on both the front and rear. This was done so that the structure could be sintered at 250 °C for 30 min in order to aid the movement of the metal towards the Si surface. Figure 6.12 shows the resulting IV measurements from such structures, with each curve being an average of up to 9 measurements for the 0 min sample, or 27 measurements otherwise.

From Figure 6.12(a) it can be seen that without TMAH treatment there is negligible conductance in the structure, as would be expected with almost 50 nm of insulating dielectric. However, with immersion in a 25% TMAH solution for 30 min (prior to metallisation and sintering), an electrical response can be detected, as shown through the measured IV curves in Figure 6.12(b). With continued immersion in the TMAH solution from 30-90 min the current decreases by approximately 50% (Figure 6.12(b)-(d)). It is possible that prolonged exposure to the TMAH solution damages the stacked structure, such as in the case of HF etching where the Al_2O_3 layer is undermined. It

has been reported that undermining in stacked passivating interlayer structures can have a negative influence on the conductance [188]. Faster immersion times, or a lower TMAH concentration may potentially result in even higher conductance. It should be noted that, for the lifetime control case study in section 4.5.1, the impact of TMAH etching has been investigated and found negligible with these stacked structures for concentrations as high as 2%. However, it is likely that higher concentrations of TMAH would have a more significant impact.

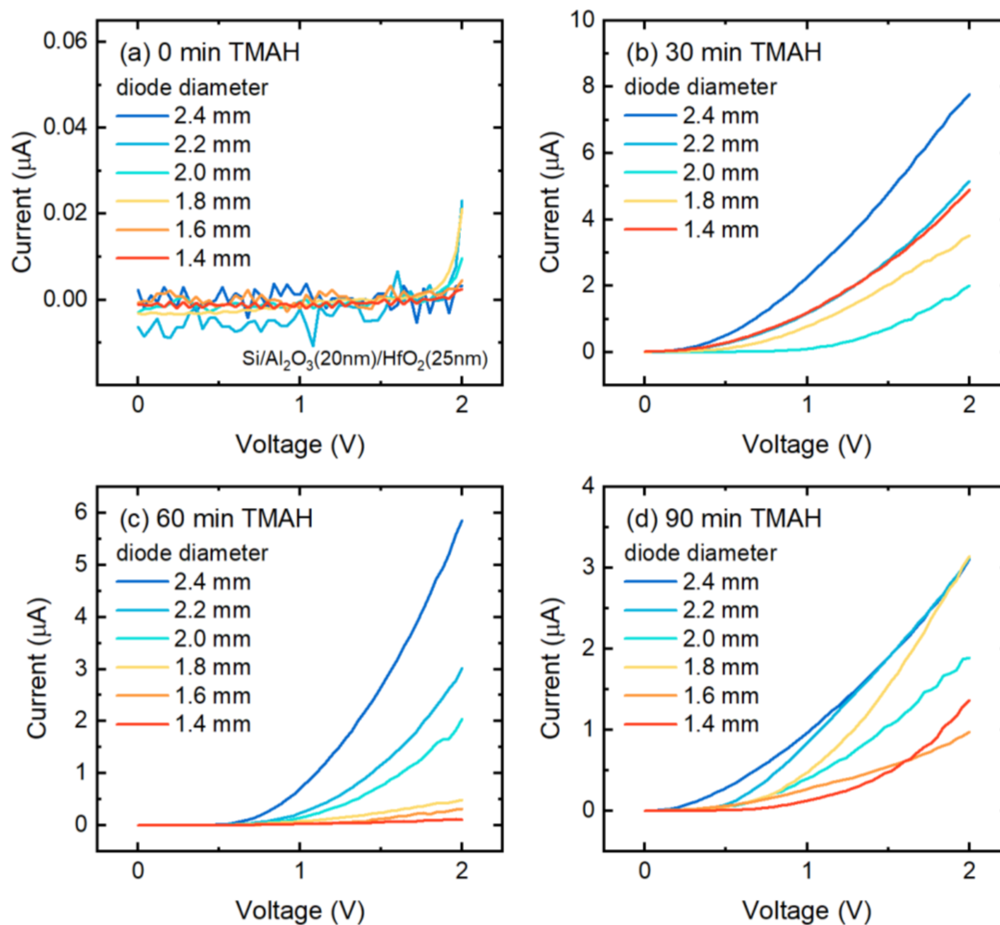


Figure 6.12: IV measurements of a structure with ~20 nm Al_2O_3 and ~25 nm HfO_2 dielectric interlayers after immersion in a 25% TMAH solution heated to 80 C for (a) 0 min, (b) 30 min, (c) 60 min, and (d) 90 min.

Whilst current values are still very low (~10^3 x smaller than typical passivating contact structures), this method provides a promising and exciting new route to the formation of passivating contact structures. Further work should focus on optimising the process

parameters, including film thickness, annealing temperature, contact structure, sintering temperature and time, etching solution and concentration, and immersion time.

6.7 Conclusion

This chapter has studied the thickness dependence of HfO_2 films, highlighting a peak in passivation performance around 2.5 nm thick, for films annealed at 475 °C. XRD measurements suggest that between 10 nm and 2.5 nm thickness HfO_2 films shift from a crystallised monoclinic structure to amorphous, when annealed at temperatures around 475 °C. The lack of crystallinity at this temperature, in conjunction with the good passivation performance, contradicts prior reports suggesting that HfO_2 passivation may rely on a crystallised film [70].

Alongside the material characterisation of HfO_2, a preliminary study was conducted into the application of thin HfO_2 layers in passivating contacts. Front and rear contacts were optimised, using a simple architecture and low-temperature processing, finding the best performance with an Au/*n*Si/HfO_2/Al sample structure. The thickness dependence of contact resistivity was estimated using the ECSM, though the non-ideal IV characteristics of these samples limits the accuracy of this approach. Potential causes of the apparent shunt in the diode structure are discussed, with some indications this may be due to metal implantation from the high energy e-beam process, resulting in a one-directional shunt.

The annealing temperature dependence of Au/*n*Si/HfO_2/Al samples were investigated through conductance measurements, finding that resistance is lowest for samples annealed below 375 °C. For higher temperature anneals, the resistance increases and the relation between current values and contact size is lost, indicating a change in carrier transport mechanisms. This shift in performance is consistent with the crystallisation region of HfO_2, however, as demonstrated by XRD, the ultra-thin HfO_2 layers should remain amorphous. This suggests that there are other factors

influencing the material within this temperature region, such as a change in dielectric charge. The temperature dependence of the sample contact performance and passivation are in direct conflict with each other, as passivation has been shown to peak around 475 °C, which is significantly higher than the optimal temperature range for the contact performance.

HfO_2 has been established to have excellent passivation, particularly at the sub-10 nm scale, which would make it a promising candidate for applications in passivating contact structures. This chapter provides a preliminary exploration of the topic, highlighting changes in performance resulting from HfO_2 film thickness and annealing temperature. Further work is required on optimising the contact structure, to achieve ideal diode performance. This may require increasing the complexity of the contact architecture and thermal budget.

Investigations have been made into the incorporation of HfO_2 layers into stacked structures, including the development of a novel contact structure that utilizes the pinhole formation within, and etching characteristics of, $Si/Al_2O_3/HfO_2$ stacks to allow carrier transport through thicker dielectric films.

6.8 Contributions

The content of this chapter has been published [186] and parts of the text have been included verbatim. The reported results include experimental contributions from Sophie Pain and Anup Yadav in the form of sample fabrication and measurements for lifetime and XRD studies.

Chapter 7

Conclusion

7.1 Key findings

This work has focused on investigating various physical and electrical properties of HfO_2 thin films, grown *via* ALD, for potential application as passivating interlayers in PV device structures. Particular attention was paid to maximising the passivation quality through optimisation of the post-deposition conditions. Various material parameters were studied which enabled the separation of surface and bulk contributions, as well as chemical and field-effect passivation mechanisms. The conductive performance of the thin films was then analysed in a simple, low-thermal budget, passivating contact structure. Additionally, the robustness of the HfO_2 thin films was investigated through testing the wet chemical etch resistance. The results of this were then used for the purposes of lifetime control in a THz modulation device, and in the formation of a novel contact structure for PV devices. The key findings were as follows:

In **Chapter 4**, a relation between the etch rate of HfO_2 in HF and the HfO_2 film crystallinity was determined, with amorphous films etching quickly, fully crystallised films not etching within the time-frame considered, and an intermediate stage around the crystallisation region where films etch slowly. A difference in performance was discovered between HfO_2 films deposited directly on Si and stacks with an Al_2O_3 interlayer between the HfO_2 and Si. The reduced etch resistance for annealed stacked samples was determined to be due to the formation of pinholes within the structure, causing undermining of the dielectric layers. A comparison between different measurement approaches was made. It was found that either a change in film thickness or film density was recorded during etching, depending on whether a Filmetrics or X-ray reflectometry system was used, respectively. The benefits of using

HfO_2 as a protective barrier layer was demonstrated through the production of lifetime control samples, where the rear Al_2O_3 passivation layer was protected during the patterning of the sample front.

In **Chapter 5**, the post-deposition annealing conditions were varied in order to maximise passivation quality. A peak in performance was found around 475 °C, were SRVs reach a minimum value <5 cm/s. This annealing temperature dependence was distinguished from any bulk-degradation in the Si through application of a room-temperature superacid re-passivation technique. This is the first time such a technique has been utilised in this context. The chemical and field-effect passivation mechanisms were investigated, with degradation of the chemical passivation determined to be the cause of the decrease in lifetime at higher temperatures.

In **Chapter 6**, the thickness dependence of the passivation quality was investigated, with lifetimes found to be increasing with decreasing thickness. A minimum SRV of 0.6 cm/s was measured at 2.5 nm, which is the lowest reported value for HfO_2, and is competitive with previously reported Al_2O_3 SRVs. An annealing temperature dependence was found for the conductance of HfO_2 layers in a passivating contact structure, with the conductance decreasing for temperatures >350 °C. This directly conflicts with the optimal temperatures for HfO_2 passivation. Additionally, contact resistivity/ conductance appeared to be severely limited by the contact structure used. The pinhole formation discovered in Chapter 4 was then utilised to develop a novel passivating contact structure, by incorporating HfO_2 into a stack with Al_2O_3. The pinholes were intentionally widened with an etching solution so that micro-scale regions of direct metal-Si contact could be formed, whilst leaving the rest of the Si surface passivated with the dielectric stack.

These findings demonstrate the effectiveness of HfO_2 as a passivating layer, producing SRVs that compete with leading commercial dielectric layers. The potential of single layer HfO_2 as a passivating interlayer is limited, due to the conflicting annealing temperature dependence of the passivation and conductance. However,

when the unique etching characteristics of HfO_2 films are considered, this creates numerous possibilities for the fields of photovoltaics and electronics, including the development of a unique passivating contact structure, and protective barrier layers for complex device fabrication.

7.2 Research outlook

As mentioned, this research opens up various new routes to utilise HfO_2 in device fabrication. This research can be furthered through the continued investigation of etching mechanics and material parameters, as briefly described in the following sections.

7.2.1 Protective barrier layers

In order for the full potential of HfO_2 thin films as protective barrier layers to be realised, further investigations should be made into the integrity of the etch resistance for various stacked materials. It has already been demonstrated that HfO_2 is able to substantially increase the longevity of Al_2O_3 layers in Si processing solutions. Should this behaviour also be demonstrated for other commonly used materials, such as SiO_x or SiN_x, it would greatly increase the flexibility of device fabrication processes. In particular, it would make single side etching possible without the need for specialist equipment that is often only available in industry and large-scale laboratories.

7.2.2 Wafer patterning

Brief attempts were made in this work to locally anneal HfO_2 thin films. If a localised heating process could be used to crystalise specific regions of a HfO_2 layer, a patterned wafer could be produced through a simple HF dip. This is possible because of the varying etch rates of HfO_2 films, with crystallised monoclinic HfO_2 demonstrating incredibly strong etch resistance, and amorphous HfO_2 etching very quickly. In particular, laser annealing would allow for high flexibility in pattern design, as well as pattern resolution. The localised annealing of HfO_2 films *via* a laser process

has been previously demonstrated, though the resultant film had a cubic structure [82]. If a monoclinic variation could be produced, where the passivation and etching characteristics are well understood, it would greatly reduce the time and cost of patterning processes. Current wafer patterning is mostly done with lithography, which is a relatively slow and costly processes, and is not easily translated to an industrial scale. By comparison, laser annealing processes are generally quite fast and simple, as is a room-temperature HF dip, thus making this a potentially more viable approach for industrial-scale patterning.

7.2.3 Micro-PERC

This work has reported the development of a novel dielectric stack structure for passivating contact formation. This structure could potentially provide a lower temperature approach to passivating contacts, as it does not require high-temperature processes (>800 °C for current SiO_x/poly-Si architectures) to form the pinholes that are critical for carrier transport. However, a significant amount of research still needs to be conducted to determine whether such a structure is actually viable. Measured current values are still very low for this design, as parameters have not yet been optimised. Further work should focus on varying material and process parameters, such as film thickness, etching solution concentration, contact materials, and heat treatments. With optimisation of these variables, the performance of the design should improve, and it can then be compared to existing cell architectures.

7.2.4 Zirconium

Whilst HfO_2 is an incredibly interesting material, with promising applications in electronics and photovoltaics, Hafnium is, unfortunately, quite limited. Particularly for the PV sector, where global energy generation is now above 1 TW and growing rapidly, material availability can be a very limiting factor. Zirconium is a material that is very chemically similar to Hafnium. In fact, they are often naturally found together and must be separated when mined through complex and costly processes. This is

part of what makes Hafnium so limited and expensive. However, Zirconium is far more abundant, and much cheaper. Since the two materials are so chemically similar, it is possible that monoclinic zirconium oxide (ZrO_2) could behave very similarly to monoclinic HfO_2. If so, ZrO_2 could potentially become a replacement or a dopant, reducing the material consumption of Hafnium, without major loss of material properties. If similar levels of passivation and etch resistance could be demonstrated, it would provide a more viable and sustainable route to the implementation of the processes reported in this work at an industrial scale.

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