Understanding Linear Mode Robustness in Low Voltage Trench Power MOSFETs

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***Abstract*: The high temperature electrothermal stability and linear mode robustness of low voltage discrete power trench MOSFETs is assessed. The linear mode robustness is shown to be dependent on the positive temperature coefficient of the subthreshold diffusion current and the MOSFET gain factor. The datasheet threshold voltage temperature coefficient (V_{GSTX} TC) of a power MOSFET is important because it correlates with the linear mode robustness and the zero-temperature-coefficient (ZTC) point of the device. The impact of the MOSFET active area and the cell pitch on the V_{GSTX} TC is experimentally assessed on fabricated devices. It is shown that the magnitude of the V_{GSTX} TC increases as the MOSFET active area increases whereas it reduces as the cell pitch increases. The drain voltage at the onset of thermal runaway is shown to increase as the V_{GSTX} TC reduces for the same active area thereby making the V_{GSTX} TC an indicator of linear mode robustness. Although the gate voltage at the ZTC point and the magnitude of the V_{GSTX} TC increases with the MOSFET active area, the reduced thermal resistance improves the linear mode robustness. The implication is that improved device performance in terms of lower specific on-state resistance (R_{SPEC} *in* $\Omega.mm^2$) is at the expense of the linear mode robustness of the power MOSFET since lower R_{SPEC} devices have higher gain factors and higher currents are delivered at weaker inversion levels (and therefore contain higher proportions of subthreshold diffusion currents). In designing power MOSFETs, these parameters must be taken into consideration so as to minimize high temperature instability and improve linear mode robustness.**

***Index Terms* – Cell pitch, Linear mode, Thermal runaway, Trench MOSFETs and Zero Temperature Coefficient.**

I. INTRODUCTION

Power MOSFETs exhibit better switching characteristics than bipolars and are thus usually preferred for high frequency applications where switching speed is an essential application requirement [1, 2]. Power MOSFETs are also known to exhibit better electrothermal stability than bipolars because of the positive temperature coefficient of the on-state resistance and the breakdown voltage which limits the possibility for thermal runaway in the on-state and avalanche respectively. The high temperature performance of power MOSFETs is important because some applications require MOSFETs that can operate at elevated temperatures with manageable deviation from room temperature characteristics while simultaneously exhibiting electrothermal stability in the "linear mode" i.e. constant current mode. Examples of such applications include linear regulators, amplifiers and active clamps where the power MOSFET is biased at high drain currents and drain voltages as opposed to switched mode MOSFETs [3, 4]. The high operating temperature can be due to external heat sources and/or MOSFET *J.E* self-heating where *J* is the current density and *E* is the electric field strength. The critical MOSFET parameters usually listed on datasheets all exhibit temperature dependency e.g. breakdown voltage (B_{VDSS}), on-state resistance (R_{DSON}), threshold voltage (V_{GSTX}) and source-drain leakage (I_{DSS}). The threshold voltage typically quoted on datasheets (V_{GSTX}) is defined as the gate-source voltage required for delivering a pre-defined drain-source current which is usually 250 µA or 1 mA depending on the manufacturer. V_{GSTX} depends on the MOSFETs physical parameters and differs from the intrinsic or theoretical threshold voltage (V_{TH}) of the MOSFET which is defined as the gate-source voltage at which the surface potential is twice the bulk potential (the onset of strong inversion) and depends on the body doping, flatband voltage and oxide thickness. Due to the physics behind the operation of the power MOSFET, R_{DSON} increases with B_{VDSS}.

Trench MOSFETs were therefore developed so as to reduce the R_{DSON} without compromising B_{VDSS}, hence cell pitch scaling (reducing the inter-stripe distance) has been used to drive forward in this direction [5-9]. Cell pitch scaling improves the gain factor ($W\mu_{EFF}C_{OX}/L$) in new generation MOSFETs; where W is the width, L is the channel length, C_{OX} is the gate dielectric capacitance density and μ_{EFF} is the effective carrier mobility. Reducing the trench pitch reduces the specific on-state resistance (R_{SPEC} in $\Omega.mm^2$) by increasing the number of source-drain conduction paths thereby increasing the current density [9]. However, trench MOSFETs have been shown to exhibit less electrothermal stability than planar MOSFETs for linear mode applications [3, 4, 10]. In some designs, increasing the active area can be pursued as an alternative to reducing trench pitch in delivering low R_{DSON}, however, this also has implications for temperature dependencies and linear mode robustness. In this paper, the impact of the cell pitch and active area on the V_{GSTX} temperature coefficient and high temperature electrothermal stability is assessed. The impact of these parameters on the temperature threshold coefficient is used to assess the linear mode robustness of the power MOSFETs.

II. DEVICE FABRICATION

The starting silicon comprising of n^+ and n^- epitaxial layers is chosen to meet the requirements of the breakdown-voltage class of the MOSFETs. Device active areas were defined and trenches were etched into the silicon wafers. Masks with 4 µm and 6 µm cell pitches were used in the fabrication process with 25 mm^2 and 49 mm^2 area MOSFETs. Silicon dioxide layers were grown by thermal oxidation thereby forming the gate oxide after which the polysilicon gates were deposited and planarised. The p-body implant was done to target the room temperature threshold voltage. Then followed the source n^+ implant, anneal, TEOS deposition, contact window definition, contact etch and source metal deposition. The

MOSFETs were packaged in standard TO-220 packages with the 3 pins for the source, gate and drain contacts. Three aluminum wires were bonded on the source metal as shown in Fig. 1 where a picture of the processed MOSFET can be seen. Fig. 2 shows a cross-sectional SEM image of the processed power MOSFET with the trench, gate poly, source epitaxial layer and TEOS passivation labeled. The breakdown voltage of the MOSFETs was confirmed to be approximately 25 V as shown in Fig. 3 where the drain current is shown as a function of the drain voltage for the 25 mm^2 MOSFET with the 4 μm cell pitch. When the breakdown voltage is reached as the drain voltage is ramped, the high electric field causes impact ionization which triggers an avalanche current.

III. ELECTRICAL RESULTS AND DISCUSSION

The V_{TH} and V_{GSTX} of the power MOSFET have negative temperature coefficients since they reduce in magnitude as the MOSFET's temperature increases [11]. The negative temperature coefficient of V_{TH} is due to the increased intrinsic carrier concentration from the reduction of the semiconductor energy bandgap whereas the negative temperature coefficient of V_{GSTX} is due to diffusion contribution to I_{DS} at low levels of channel inversion. Depending on the bias terminals of a MOSFET, I_{DS} comprises of both diffusion and drift components in varying proportions. A single-piece MOSFET model valid from weak inversion to strong inversion can be used to model the respective contributions of the drift and diffusion currents [12].

$$I_{DS} = \frac{W\mu_{EFF}C_{OX}}{L} 2\Phi_{TH}^2 m\left(\left[\ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}}{2m\Phi_{TH}}\right)\right)\right]^2 - \left[\ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}-mV_{DS}}{2m\Phi_{TH}}\right)\right)\right]^2\right) \quad (1)$$

$$\Phi_{TH} = \frac{K_B T}{q}$$

where V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, I_{DS} is the drain-source current, q is the electronic charge, T is the temperature, K_B is the Boltzmann's constant, Φ_{TH} is the thermal voltage and m is the body factor. When V_{GS} is positive but below the V_{TH}, the source-channel junction is forward biased while the drain-channel junction is reverse biased. If V_{DS} is greater in magnitude than the potential difference between the gate voltage and the threshold voltage (V_{GS}-V_{TH}), the drain end of the channel is fully depleted. The current that flows through the device therefore depends on the carrier concentration gradient between the drain and the source. A diffusion current thus flows from the source to the drain which can be derived from (1) by assuming that the exponential terms are less than 1 and $\ln(1+x) \approx x$ [12].

$$I_{DS} = \frac{W}{L} \frac{\mu_{EFF} \sqrt{2q\varepsilon_{Si} N_A}}{2\sqrt{\phi_S}} \Phi_{TH}^2 \exp\left(\frac{V_{GS} - V_{TH}}{m\Phi_{TH}}\right) \quad (2)$$

where N_A is the channel doping density and Φ_S is the MOSFET surface potential. The MOSFET operates similar to a bipolar transistor in the sense that electrons are injected from the source into the channel similar to a forward biased emitter-base junction. The carriers diffuse across the channel to the drain terminal where a reverse biased drain-body pn junction sweeps the electrons into the drain as in a reverse biased collector-base junction. It can be seen in (2) that the diffusion current is proportional to the square of the temperature through the thermal voltage. Hence, a MOSFET biased in weak inversion, like a bipolar transistor, is more susceptible to thermal runaway because the current increases with temperature [13]. Because I_{DS} at threshold contains a significant diffusion contribution, at higher temperatures

the magnitude of V_{GS} required to deliver a pre-defined current is reduced; hence, the V_{GSTX} is reduced. This positive feedback loop between the diffusion current and the temperature makes MOSFET operation in region of high V_{DS}, high I_{DS} and/or low V_{GS} unstable since it is a self-amplifying or regenerative process. This is why power MOSFETs are known to be prone to localized thermal runaway when operating in the region of high V_{DS}. Because of this, the forward-biased safe operating area (FBSOA) is usually specified on datasheets. The FBSOA defines the capability of the power MOSFET to operate in the linear mode and is sometimes referred to as linear mode robustness. The term "linear mode robustness" must be taken with caution because power MOSFET engineers regard the saturation point ($V_{DS} > V_{GS}-V_{TH}$) as the linear mode (as in bipolars) whereas IC engineers regard the triode region ($V_{DS} < V_{GS}-V_{TH}$) as the linear mode. Fig. 4 shows the output characteristics (I_{DS} as a function of V_{DS} for different V_{GS}) of one of the trench MOSFETs under investigation with the triode and saturation regions in the graph labeled. MOSFET switches operate primarily between points A and B of the load-line shown in Fig. 4 whereas linear mode MOSFETs can operate anywhere in region C. Furthermore, the high power density in the linear mode (due to high $I_{DS}V_{DS}$) increases the temperature through *J.E* self-heating thereby increasing the likelihood of thermal runaway. Fig. 5(a) shows a pictorial depiction of this self-amplifying or regenerative process that leads to thermal runaway in the linear mode. Fig. 5(b) shows an example of a 25 mm^2 power MOSFET that has been deliberately driven into thermal runaway by extended linear mode stressing. The failure signature is usually a fusion burn mark on the metal surface caused by very high temperatures localized to the failure point. An ideal power MOSFET should share the current equally between all the trenches; however, variations between the cells result in unequal current distribution. These variations could be due to the spreading resistance in the source metallization as the current is distributed from the bond wires into the MOSFET, variations in the gate resistance, voids in the solder between the drain and the package

substrate, particles on the wafer during processing causing variations in local parameters like oxide thickness, trench depth, p-body doping or even ionic contaminants that lodge anywhere in the MOSFET. If these process imperfections cause a reduction in the local V_{TH} of the affected trench, then that part of the device becomes susceptible to thermal runaway in the linear mode. This is because subthreshold conduction will cause increased local temperatures which feeds back positively to the localized drain current as shown in Fig. 5(a).

As V_{GS} is increased, the diffusion contribution of the I_{DS} reduces whilst the drift contribution increases. When a sufficiently high V_{GS} uniformly inverts the channel from the source to the drain, the MOSFET acts like a linear resistor and I_{DS} is dominated by the drift component. This is the triode part of the output characteristics labeled on the loadline in Fig. 4 as point B. When the MOSFET is in strong inversion, the exponential terms are much greater than unity and (1) reduces to the recognizable equation for the MOSFET.

$$I_{DS} = \frac{W\mu_{EFF}C_{OX}}{L}\left(V_{GS} - V_{TH} - mV_{DS}\right)V_{DS} \tag{3}$$

This is usually the case in applications where the MOSFET is used as a switch with R_{DSON} simply computed as V_{DS}/I_{DS}. This mode of operation is inherently stable and is significantly less prone to thermal runaway due to the negative temperature coefficient of the effective mobility. Any localized increase in I_{DS} causes $J.E$ self-heating, which exacerbates phonon scattering and hence reduces the effective mobility by reducing the carrier relaxation time. The reduction in effective mobility is translated into a reduction in I_{DS}, which in turn reduces the temperature of the trench i.e. it is self-regulating.

In the saturation regime (linear mode for power MOSFET engineers), the drain

current can be described by the well known equation

$$I_{DSAT} = \frac{W\mu_{EFF}C_{OX}}{2L}(V_{GS} - V_{TH})^2 \quad (4)$$

The temperature dependence of the saturation drain current can be expressed as

$$\frac{\partial I_{DSAT}}{\partial T} = \frac{WC_{OX}}{2L}\frac{\partial \mu_{EFF}}{\partial T}(V_{GS} - V_{TH})^2 - \frac{W\mu_{EFF}C_{OX}}{L}\frac{\partial V_{TH}}{\partial T}(V_{GS} - V_{TH}) \quad (5)$$

It was shown by Consoli et al [14], that the maximum current temperature coefficient is proportional to the square of $\delta V_{TH}/\delta T$ and proportional to $W\mu_{EFF}C_{OX}/L$. Hence for power MOSFETs biased in the saturation regime, the interplay between the V_{TH} temperature coefficient and the μ_{EFF} dependence on temperature determines the linear mode robustness.

It can be seen from (2) that I_{DS} is exponentially dependent on V_{GS} in weak inversion and from (3) that I_{DS} is linearly dependent on V_{GS} in strong inversion. As a result, R_{DSON} reduces very rapidly as V_{GS} is increased in the subthreshold and less rapidly in strong inversion. This is shown graphically in Fig. 6 where R_{DSON} is shown as a function of V_{GS}. Hence, $\delta R_{DSON}/\delta V_{GS}$ decreases as the inversion level increases i.e. the responsiveness of the channel resistance reduces with increasing V_{GS}. If the power MOSFET is operating in the region close to subthreshold diffusion labeled in Fig. 6 (high $\delta R_{DSON}/\delta V_{GS}$), it is possible for the R_{DSON} to vary considerably between the individual trenches due to local variations in V_{TH} as a result of the process imperfections described earlier. This encourages thermal runaway (even at low power densities) due to current crowding since electrons will always be diverted to the cell with the least resistance. The *J.E* self-heating generated from current crowding triggers the cycle shown in Fig. 5(a) and the kind of thermal destruction shown in Fig. 5(b).

The greater the variation in R_{DSON} between neighboring trenches, the greater the likelihood of the thermal runaway cycle depicted in Fig. 5(a) occurring at low power densities. As the inversion level increases ($\delta R_{DSON}/\delta V_{GS}$ reduces), the R_{DSON} difference between the trenches is reduced; hence, thermal stability is improved.

The reduction in V_{TH} at elevated temperatures increases the drain current (I_{DS}), which acts in opposition to the negative temperature coefficient of the μ_{EFF}. Hence, the magnitude of the gate voltage bias of the power MOSFET will determine which mechanism is dominant. If the MOSFET is biased in subthreshold, then the negative temperature coefficient of V_{TH} dominates because of the subthreshold diffusion current. In this case, the MOSFET is susceptible to thermal runaway as in Fig. 5(a). However, if the MOSFET is biased in strong inversion (above threshold, $V_{GS} >> V_{TH}$), then the self-limiting nature of the negative temperature coefficient of μ_{EFF} dominates and thermal run-away/hot spots become less likely since *J.E* heating reduces I_{DS}. The zero-temperature-coefficient (ZTC) is the bias point where the I_{DS} is independent of the temperature due to the fact that both effects are equal and opposite [15, 16]. Fig. 7 shows the gate transfer characteristics of the power MOSFET at 25 °C and 185 °C. The intersection point between the I_{DS} at both temperatures is the ZTC as labeled in Fig. 7 and occurs at a V_{GS} of 6.5 V. The bias points below the ZTC are the region of $\delta I_{DS}/\delta T > 0$ and is thus thermally unstable [10]. The bias points above the ZTC are the region of $\delta I_{DS}/\delta T < 0$ and are thus thermally stable. The high temperature V_{GSTX} (or the $\delta V_{GSTX}/\delta T$) of the power MOSFET can be used as one of the indicators of the linear-mode robustness of the device with a given active area. The lower the high temperature V_{GSTX} of the MOSFET (or the higher the $\delta V_{GSTX}/\delta T$), the more susceptible it will be to thermal runaway in the linear mode as in Fig. 5(a). Mathematical models presented by Consoli et al [14] showed that the V_{TH} temperature coefficient ($\delta V_{TH}/\delta T$) determined when current temperature coefficient ($\delta J/\delta T$) changed polarity from positive (thermal instability) to negative (thermal stability) with

$\delta J/\delta T=0$ being the ZTC. It was shown in [14] that the drain current range over which there is thermal instability ($\delta J/\delta T > 0$) is proportional to the square of $\delta V_{TH}/\delta T$ and that the features that led to lower R_{DSON} (higher gain factor) made the devices less robust in the linear mode.

Impact of cell pitch: Variable temperature measurements were done on 30 samples each of 25 mm^2 power MOSFETs with 4 μm and 6 μm cell pitch so as to investigate the impact of the pitch on the V_{GSTX} temperature coefficient. The V_{GSTX} is studied because this is what is usually quoted on datasheets and this is what designers usually work with. Since application engineers are usually not concerned with the theoretical V_{TH} and are more concerned with current delivery, the behavior of V_{GSTX} is more pertinent. In order to ensure the statistical integrity of the analysis, the standard deviation of V_{GSTX} was calculated over the sample set. The V_{GSTX} standard deviation did not exceed 1.8% of the average V_{GSTX} hence there is confidence that the analysis is not affected by outliers. V_{GSTX} was normalized over the temperature range by dividing the values by the V_{GSTX} at 25 °C. Fig. 8 shows the normalized average V_{GSTX} as a function of temperature for power MOSFETs with the different cell pitches. It can be seen from Fig. 8 that both MOSFETs have equal V_{GSTX} at -55 °C. However, as the mounting base temperature is increased to 185 °C, V_{GSTX} falls by 50% and 66% in the 6 μm and 4 μm trench pitch MOSFETs respectively. Hence, as the pitch is reduced from 6 μm to 4 μm, the magnitude of the temperature coefficient of the V_{GSTX} increases from 9.4 mVK^{-1} to 10.9 mVK^{-1} thereby indicating that the susceptibility to linear mode robustness failure increases as the cell pitch is reduced. Also, the V_{GS} at the ZTC intersection point is 6.5 V for the 4 μm pitch MOSFET and 4.3 V for the 6 μm pitch power MOSFET thereby further indicating better electrothermal stability for the larger pitch device. The inversion level required to deliver a predefined current will reduce as the cell pitch reduces thus increasing the diffusion component of I_{DS}. As the cell pitch is reduced and the number of cells in the

MOSFET is increased, the current in each cell at a given drain current will be lower for the MOSFETs with the smaller cell pitches. As a result, the current per unit cell in the 4 μm pitch MOSFET at V_{GSTX} is lower (more diffusion current at weaker inversion levels) and therefore more prone to temperature instability than the 6 μm pitch MOSFET. Solving (5) for the maximum I_{DS} temperature coefficient yields [14, 17]

$$\frac{\partial I_{DS}}{\partial T} \propto -K^2\left(\frac{\partial K}{\partial T}\right)^{-1}\left(\frac{\partial V_{TH}}{\partial T}\right)^2 \tag{6}$$

where $K = \dfrac{W\mu_{EFF}C_{OX}}{2L}$

Increasing the number of cells in a MOSFET is analogous to increasing W and the gain factor ($2K$) of the MOSFET. It was also shown in [14], that the drain current at ZTC (i.e. the range of I_{DS} over which $\delta I_{DS}/\delta T > 0$) is proportional to the maximum $\delta I_{DS}/\delta T$ and is also therefore proportional to the gain factor. The result of this is a trade-off between R_{DSON} and linear mode robustness hence; the application requirement will determine which parameter is more important.

Impact of active area: Variable temperature measurements were performed on 30 samples each of 4 μm pitch MOSFETs with 25 mm^2 and 49 mm^2 area (21 mm^2 and 45mm^2 active area) so as to investigate the impact of the active area on high temperature performance. As with the previous samples, the standard deviation of V_{GSTX} did not exceed 1.5% of the average V_{GSTX}. Fig. 9 shows the normalized average V_{GSTX} as a function of the temperature for the 25 mm^2 and 49 mm^2 area MOSFETs. It can be seen from Fig. 9 that the magnitude of the V_{GSTX} temperature coefficient of the 49 mm^2 MOSFET is larger since its high temperature V_{GSTX} is 15% lower than that of the 25 mm^2 MOSFET. The magnitude of the V_{GSTX} temperature

coefficient of the 49 mm^2 power MOSFET is 13.9 mVK^{-1} whereas that of the 25 mm^2 power MOSFET is 10.9 mVK^{-1}. The V_{GS} at the ZTC intersection point increases from 6.5 V for the 25 mm^2 MOSFET to 8.4 V for the 49 mm^2 MOSFET. Increasing the active area of the MOSFET reduces the R_{DSON} since a larger active area draws more current. As in the case with cell pitch reduction, this increases the ZTC intersection point and the magnitude of the V_{GSTX} temperature coefficient since the larger area MOSFET has a lower V_{GSTX} at 185 °C. The V_{GSTX} of the power MOSFET is reached in the 49 mm^2 MOSFET at a weaker inversion level (i.e. smaller current density) and hence, with a greater diffusion component than the 25 mm^2 MOSFET. The 49 mm^2 MOSFET will also have a higher gain factor, which has been shown to be detrimental for linear mode electrothermal stability. However, the impact of this on the linear mode robustness is not immediately clear since the added thermal mass and reduced power density (in W/mm^2) of the 49 mm^2 power MOSFET means less average *J.E* self-heating. The reduced thermal resistance counteracts the impact of the higher ZTC intersection point and the higher V_{TH} temperature coefficient. It was shown by Spirito et al [17], that thermal runaway occurs for the following conditions

$$\frac{\partial I_{DS}}{\partial T} \geq \frac{1}{V_{DS} R_{TH}} \tag{7}$$

where R_{TH} is the thermal resistance of the MOSFET. Although increasing the size of the MOSFET increases $\delta I_{DS}/\delta T$ according to (6), however, it also reduces R_{TH}. The linear mode stressing in the next section reveals which mechanism is dominant.

The linear mode robustness of the MOSFETs is evaluated by ramping up the drain voltage of the MOSFET while keeping V_{GS} constant. A DC supply voltage is connected to the gate and kept constant at 6 V while the drain voltage is incrementally raised at 250 mV steps

and applied for duration of 2 seconds (approximating DC). A V_{GS} of 6 V is chosen so that there is sufficient current (10 A) to warm up the device and increase the possibility of thermal runaway during the 2 second drain pulse. The drain-source current reading is taken from the drain supply meter which indicates thermal runaway by a rapid rise in current and a simultaneous drop in voltage i.e. the MOSFET is now short circuited between the drain and the source. As V_{DS} is increased, the diffusion current increases and the MOSFET is driven from the triode region into saturation and the drain end of the channel is driven into depletion and subthreshold. The value of V_{DS} at which the MOSFET fails due to thermal runaway is taken as the measure of the linear mode robustness. This experiment was performed over a sample set of 10 MOSFETs for each cell pitch and active area. So as to ensure that the sample set was free of maverick devices and all MOSFETs were of high quality, all the MOSFETs were subjected to uniformity tests which ensured that there were no outliers. The results of the thermal runaway experiment can be seen in Fig. 10 where the distributions are shown for the 4 μm and 6 μm cell pitch MOSFETs with 25 mm^2 and 49 mm^2 active area. The maximum V_{DS} at the onset of thermal runaway have been normalized by dividing by the V_{DS} of the highest performing devices in the sample set. The 49 mm^2 MOSFETs on average require 80% more V_{DS} to reach thermal runaway because of their larger thermal mass (hence lower average temperatures). However for the same active areas, the 6 μm pitch devices exhibited better linear mode robustness compared with the 4 μm pitch devices. For the 25 mm^2 area MOSFETs, the V_{DS} at the onset of thermal runaway for the 6 μm pitch was on average 18% higher than that of the 4 μm pitch devices. The standard deviations of the measured data from the 10 MOSFETs did not exceed 4.6% of the average. For the 49 mm^2 MOSFETs, the average V_{DS} at the onset of thermal runaway was on average 10% higher for 6 μm pitch MOSFETs. These results show that larger pitch MOSFETs with the same active area exhibit better linear mode robustness. They also show that the V_{GSTX} temperature coefficient and ZTC intersection

point can be used as indicators of linear mode robustness. More work will have to be done on quantifying this correlation.

CONCLUSIONS

It has been shown that power MOSFETs suffer thermal runaway in the linear mode due to subthreshold diffusion currents that exhibit positive temperature coefficients and due to the negative threshold temperature coefficients. The high $\delta R_{DSON}/\delta V_{GS}$ in the subthreshold regime (weak inversion) means that small variations in threshold between individual cells greatly increases the likelihood of current crowding and thermal runaway compared with the low $\delta R_{DSON}/\delta V_{GS}$ in the triode regime (strong inversion). The high temperature characteristics of trench power MOSFETs have been studied as functions of the cell pitch and the active area. Reducing the cell pitch from 6 μm to 4 μm increases the magnitude of the V_{GSTX} temperature coefficient whereas increasing the MOSFET area from 25 mm^2 to 49 mm^2 increases the magnitude of the V_{GSTX} temperature coefficient. It has been shown that MOSFETs of the same active area with larger cell pitches have lower ZTC points and exhibit better linear mode robustness since higher drain voltages are required to trigger thermal runaway in the linear mode. Although increasing the active area of a MOSFET increases the ZTC point and the magnitude of the V_{GSTX} temperature coefficient, the larger thermal mass and reduced thermal resistance increases the maximum drain voltage at the onset of thermal runaway. Operating at low current densities increases the likelihood of thermal runaway because the positive I_{DS} temperature coefficient increases as the current density is reduced. Since reducing the cell pitch reduces the current per unit cell for a given current without changing the thermal resistance, new generation MOSFETs with low specific R_{DSON} tend to exhibit less electrothermal robustness in the linear mode. A correlation between the V_{GSTX} temperature

coefficient, the ZTC and the maximum V_{DS} at the onset of thermal runaway has been established.

REFRENCES

[1] R. Hueting, E. Hijzen, A. Ludikhuize, and M. Zandt, "Switching performance of low voltage N Channel trench MOSFETs," *Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs*, pp. 177-180, 2002.

[2] R. Hueting, H. Erwin, A. Heringa, A. Ludikhuize, and M. Zandt, "Gate Drain Charge Analysis for Switching in Power Trench MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, pp. 1323-1330, 2004.

[3] J. Ely, "Are Trench FETs too Fragile for Linear Applications," *Power Electronics Technology*, pp. 14-24, 2004.

[4] A. Sattar and V. Tsukanov, "MOSFETs to Fragile for Linear Mode Applications," *Power Electronics Technology*, vol. pp 34-39, 2007.

[5] D. Ueda, H. Takagi, and G. Kano, "Deep Trench Power MOSFET with Ron Area Product of 160 $m.mm^2$," *in IEDM Tech Dig*, pp. 638-641, 1986.

[6] S. Peake, R. Grover, F. Farr, C. Rogers, and G. Petkos, "Fully self-aligned power trench MOSFET utilizing 1 um pitch and 0.2 um trench width," *in Proceedings of the 14th international Symposium on Power Semiconductor Devices and ICs*, pp. 29-32, 2002.

[7] F. Chien, C. Liao, C. Wang, H. Chiu, and Y. Tsai, "Low on resistance trench power MOSFET designs," *Electronics Letters*, vol. 44, pp. 232-234, 2008.

[8] K. Shenai, "Optimized Trench MOSFET Technologies for Power Devices," *IEEE Trans. Electron Devices*, vol. 39, pp. 1435-1444, 1992.

[9] P. Goarin, R. Dalen, G. Koops, and C. Cam, "Power Trench MOSFETs with very low specific on-resistance for 25 V applications," *Solid State Electron*, vol. 51, pp. 1589-1595, 2007.

[10] P. Wilson, "Automotive MOSFETs in Linear Applications: Thermal Stability," *Infineon Technologies Application notes*, 2005.

[11] G. Groeseneken, J. Colinge, H. Maes, J. Alderman, and S. Holt, "Temperature Dependence of Threshold Voltage in Thin Film SOI MOSFETs," *IEEE Electron Dev Lett*, vol. 11, pp. pp 329-331, 1990.

[12] Y. Tsividis, "Operation and modelling of the MOS Transistor," 1999.

[13] K. Kanda, K. Nose, H. Kawaguchi, and T. Sakurai, "Design Impact of Positive Temperature Dependence on Drain Current in Sub-1-V CMOS VLSIs," *IEEE J. Solid State Circuits*, vol. 36, pp. 1559-1564, 2001.

[14] A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor, and A. Magri, "Thermal Instability of Low Voltage Power MOSFETs," *IEEE Trans. Power Electron*, vol. 15, pp. 575-581, 2000.

[15] Z. Prijic, Z. Pavlovic, S. Ristic, and N. Stojandinovic, "Zero-Temperature-Coefficient Biasing of Power VDMOS Transistors," *Electronics Letters*, vol. 29, pp. 435-437, 1993.

[16] I. Filanovksy and A Allam, "Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits," *IEEE Trans. Circuits and Systems*, vol. 48, pp. 876-885, 2001.

[17] P Spirito, G Breglio, V Alessandro, N Rinaldi, "Analytical Model for Thermal Instability of Low Voltage Power MOS and S.O.A in Pulse Operation," *in Proc 14th International Symposium on Power Semiconductor Devices and IC*. pp. 269-272, 2002.

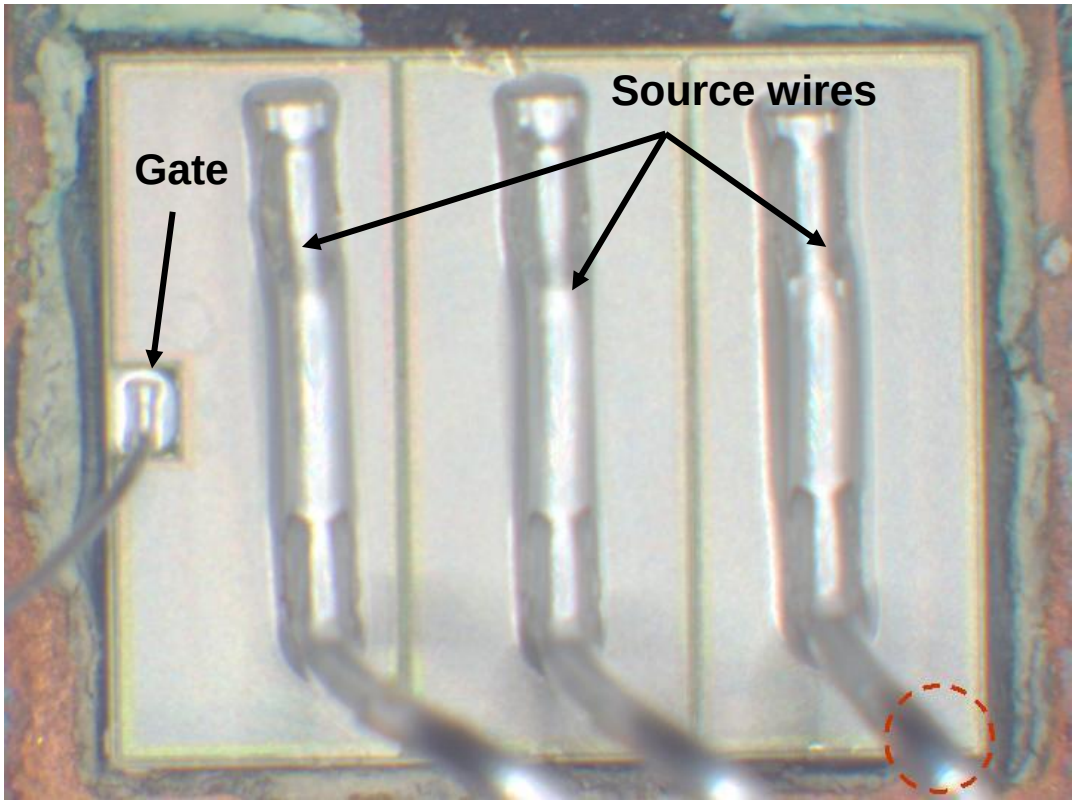

Fig. 1. 25 mm^2 power MOSFETs with 3 source wires and a gate bond wire. The back side contact acts as the drain terminal.

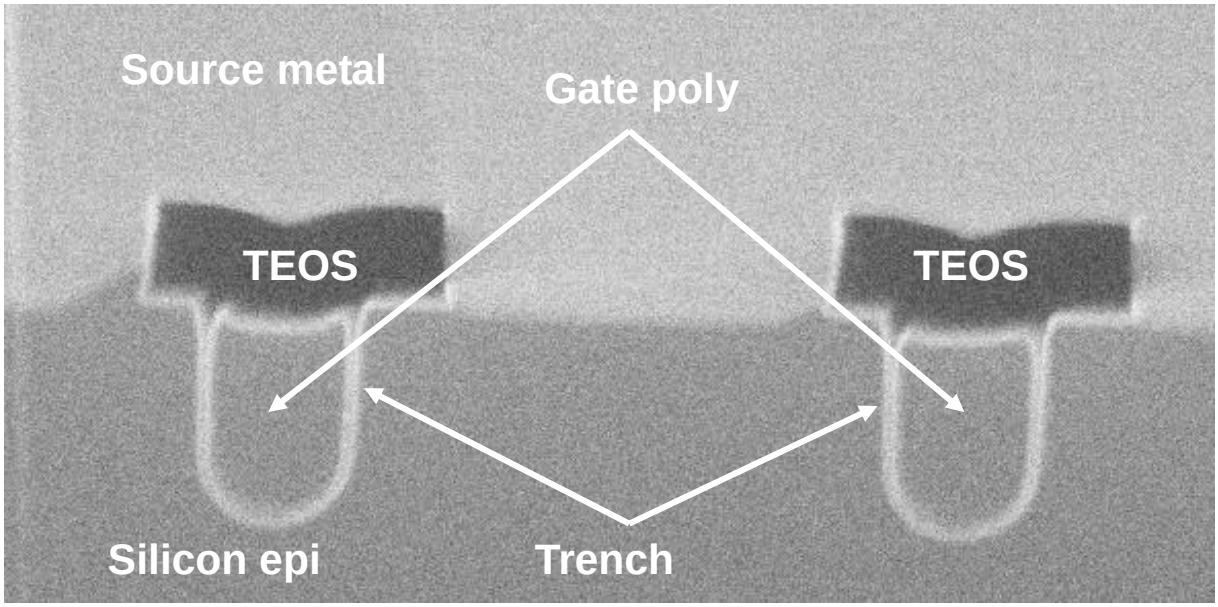

Fig. 2. Cross-sectional SEM image of the discrete trench power MOSFETs showing the polysilicon gate, the passivation and source metalisation.

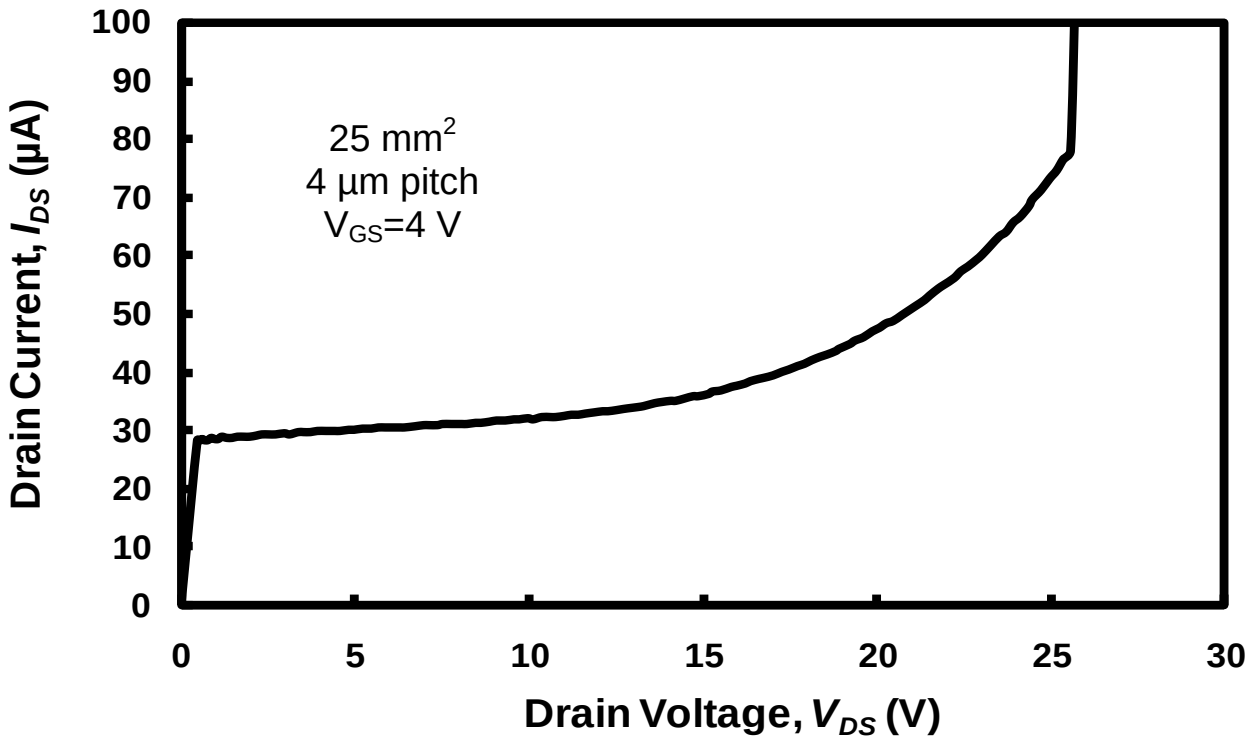

Fig. 3. The MOSFET drain current as a function of the drain voltage showing avalanche breakdown at 25 V.

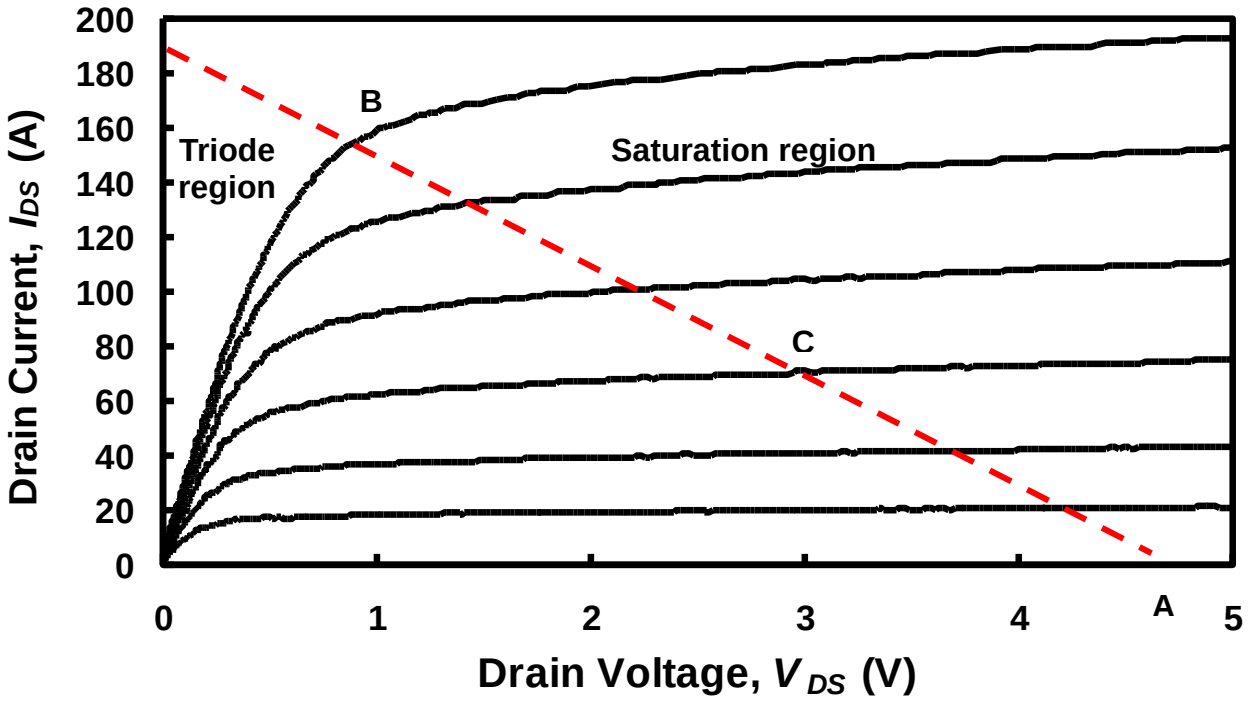

Fig. 4. The drain current as a function of the drain voltage for the 25 mm^2 4 µm pitch MOSFETs showing the bias regions prone to thermal runaway.

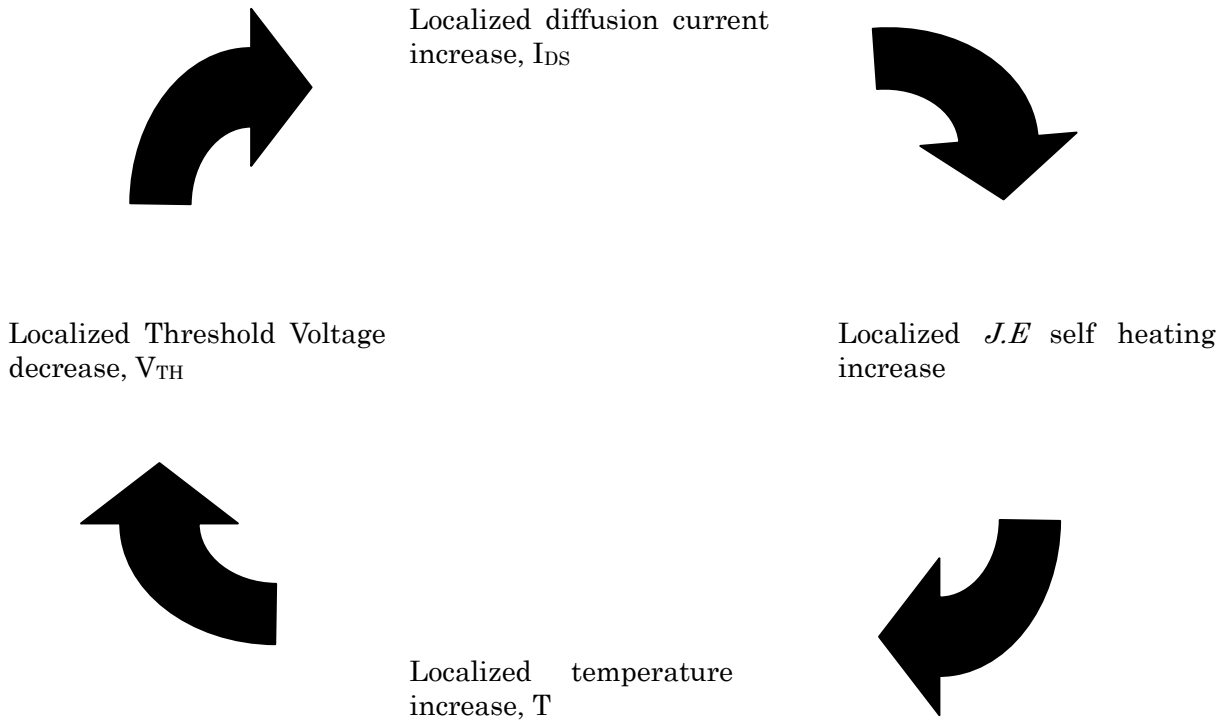

Fig. 5(a). An illustration of the thermal runaway cycle showing how localized self-heating causes an increase in temperature, reduction in the threshold voltage and increase in drain current.

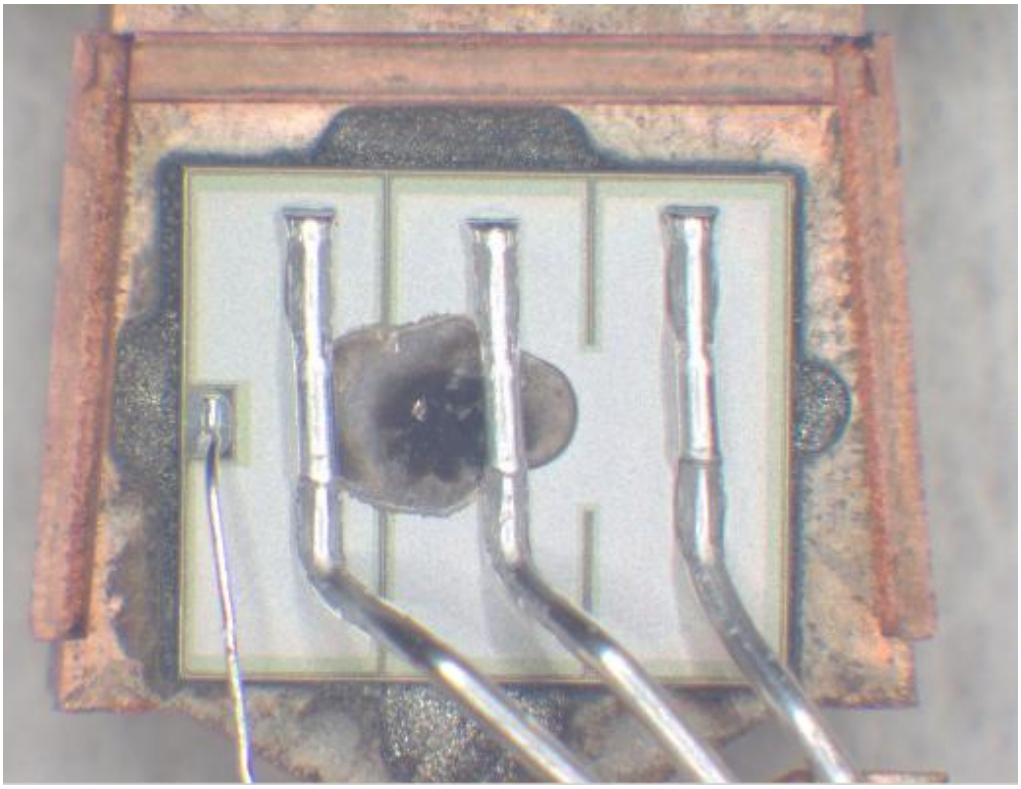

Fig. 5(b). A MOSFET that has been deliberately destroyed by thermal runaway due to subthreshold conduction in the linear mode. Localized high temperatures exceeding the intrinsic temperature limit of silicon causes silicon/metal fusion and device failure.

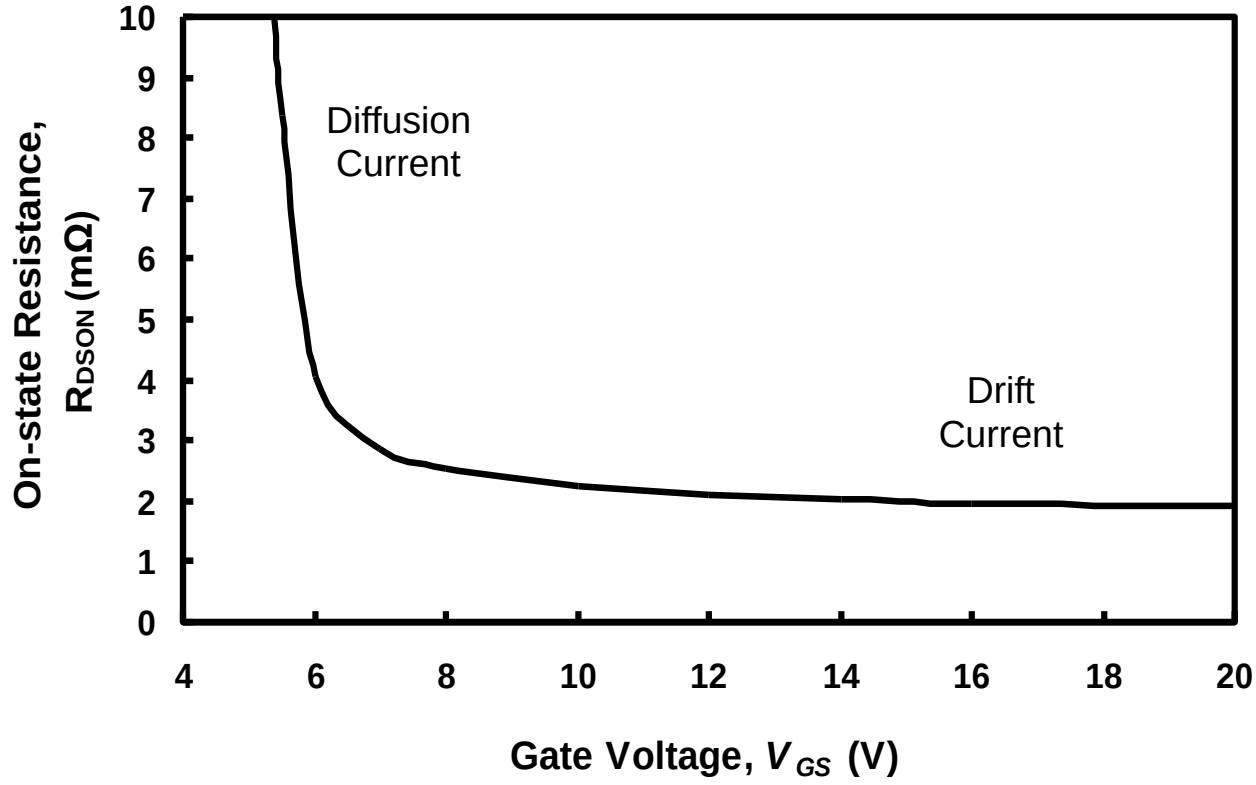

Fig. 6. R_{DSON} as a function of the V_{GS} showing the rapid change in R_{DSON} as the device switches from weak inversion to strong inversion. R_{DSON} changes very rapidly with V_{GS} in weak inversion because the diffusion current is exponentially related to V_{GS}. Small differences in V_{GS} between different trenches in subthreshold can cause very large differences in R_{DSON} when the MOSFET is in subthreshold. Thermal runaway in this region is very likely.

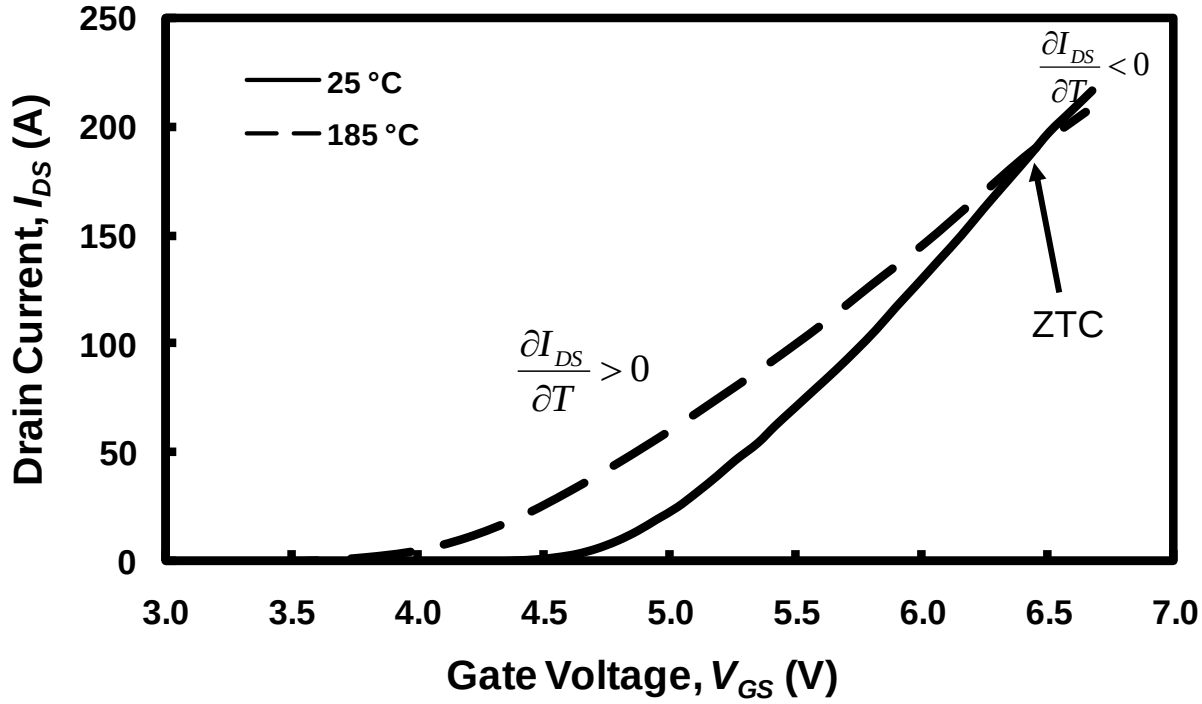

Fig. 7. The gate transfer characteristics of the 4 μm pitch 25 mm^2 power MOSFETs at 25 °C and 185 °C showing the ZTC. For bias points below the ZTC, $dI_{DS}/dT > 0$ (thermal instability) and for bias points above the ZTC, $dI_{DS}/dT < 0$ (thermal stability).

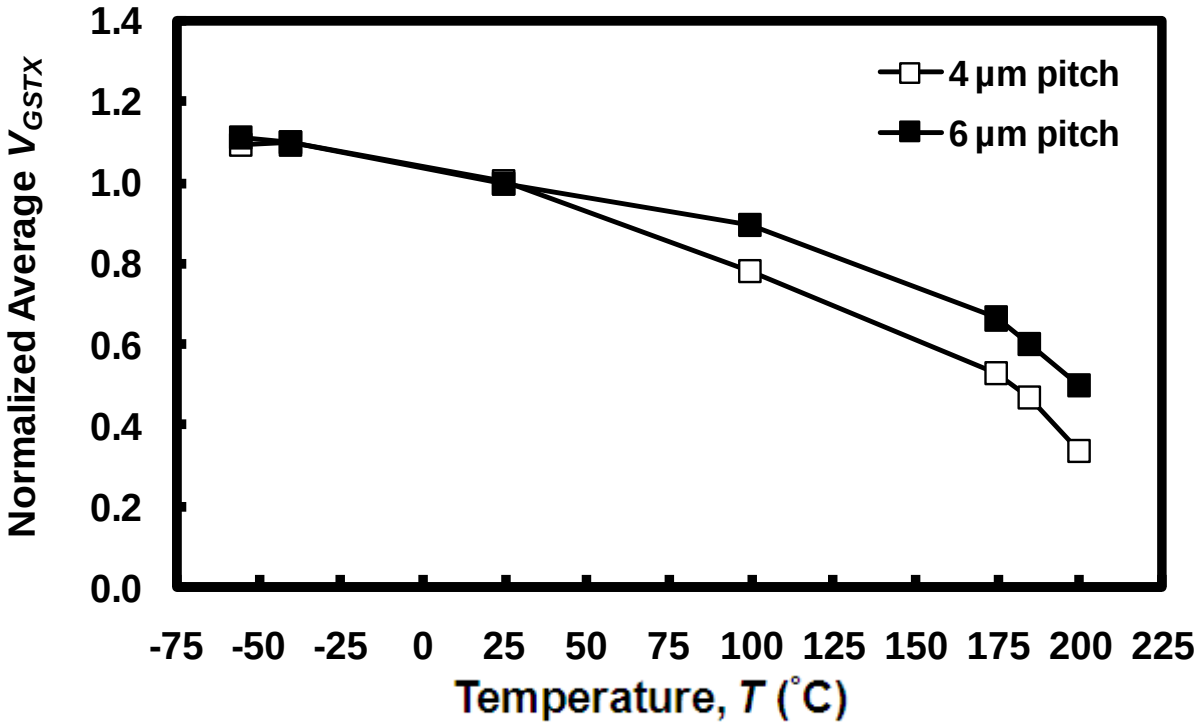

Fig. 8. The threshold voltage as a function of the temperature for 4 µm and 6 µm trench pitch power MOSFETs. The temperature threshold coefficient of the 4 µm pitch power MOSFET is 25% larger in magnitude than that of the 6 µm pitch power MOSFET thereby indicating less linear mode ruggedness with reducing trench pitch.

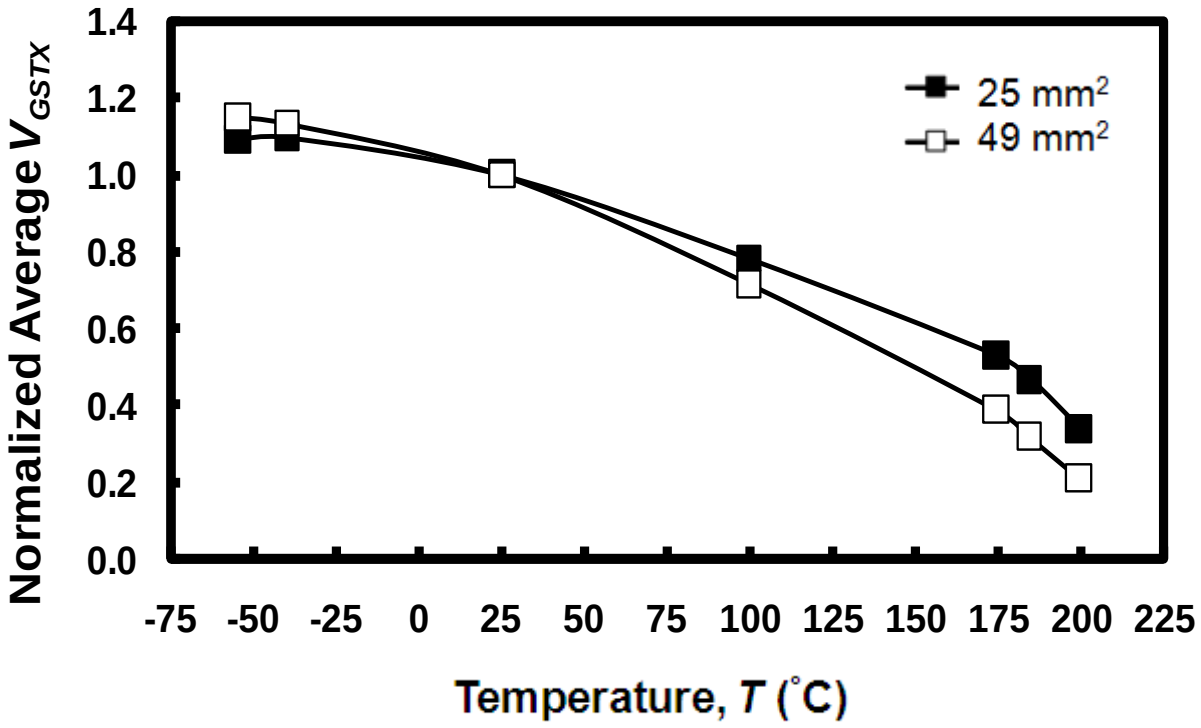

Fig. 9. The threshold voltage as a function of the temperature for 25 mm^2 and 49 mm^2 power MOSFETs. The temperature threshold coefficient of the 49 mm^2 MOSFET is 25% larger in magnitude than that of the 25 mm^2 MOSFET thereby indicating less linear mode ruggedness with increasing active area.

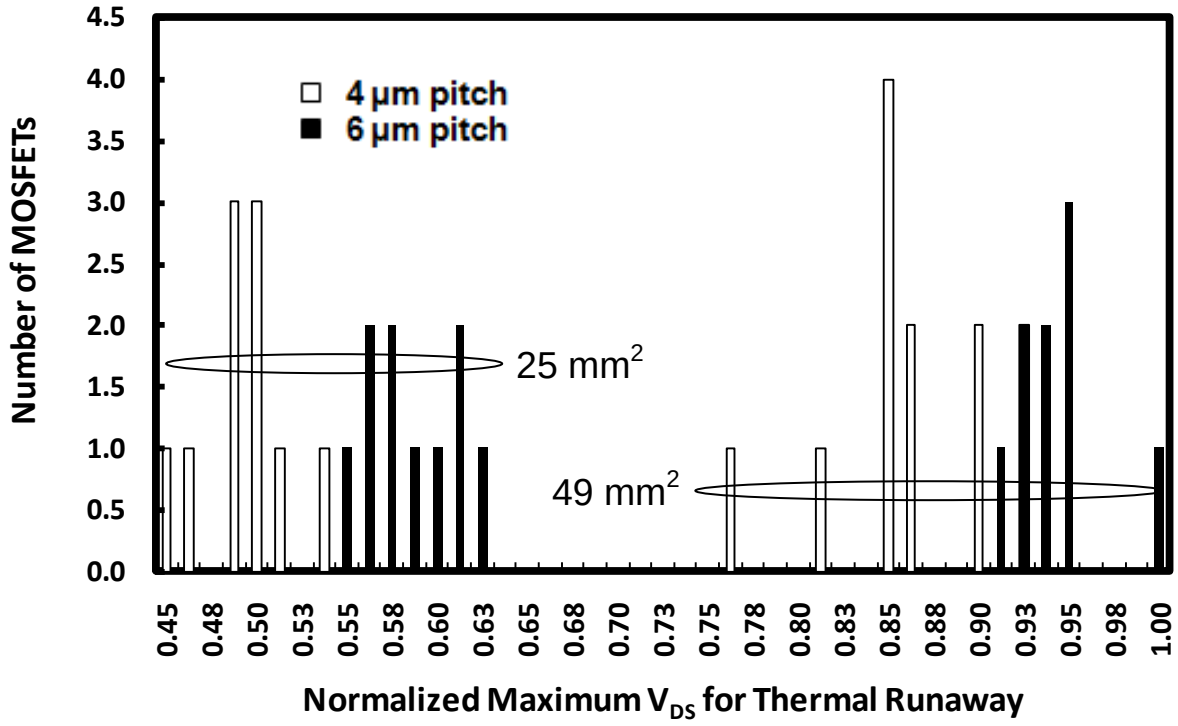

Fig. 10. Histogram distributions showing the maximum V_{DS} at the onset of thermal runaway for 25 mm^2 and 49 mm^2 MOSFETs with 4 µm and 6 µm cell pitch. The results show that the V_{DS} at the onset of thermal runaway is higher for the 6 µm cell pitch MOSFETs compared with the 4 µm cell pitch for the same MOSFET size.

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Fig. 1. 25 mm^2 power MOSFETs with 3 source wires and a gate bond wire. The back side contact acts as the drain terminal.

Fig. 2. Cross-sectional SEM image of the discrete trench power MOSFETs showing the polysilicon gate, the passivation and source metalisation.

Fig. 3. The MOSFET drain current as a function of the drain voltage showing avalanche breakdown at 25 V.

Fig. 4. The drain current as a function of the drain voltage for the 25 mm^2 4 µm pitch MOSFETs showing the bias regions prone to thermal runaway.

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