THE MBE GROWTH

AND

ELECTRICAL CHARACTERISATION

OF

HIGH RESOLUTION DOPED Si/GeSi

STRUCTURES

by

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ABSTRACT

Exploring the properties and physical limits of nanometer scale structures and devices, emerged with the advent of epitaxial techniques such as Molecular Beam Epitaxy (MBE). This has correspondingly created challenges to the available characterisation techniques. Determination of carrier concentration profiles in semiconductor structures is of vital importance since the operation of devices depends on it. Of the commonly used techniques, conventional capacitance-voltage (CV) has a major drawback due to the breakdown voltage at high reverse bias particularly at highly doped structures. The most competitive techniques for carrier concentration profiling are the electrochemical CV (ECV) which does not suffer from this limitation, Spreading Resistance Profiling (SRP) and Hall combined with stripped measurement.

This thesis reports experimental investigations of the capability and limitations of the ECV technique through comparisons with Secondary Ion Mass Spectroscopy (SIMS) and SRP on hitherto difficult profiling conditions in Si and, for the first time, carrier profiling in Si/SiGe structures. The ECV technique is shown to be well capable of profiling Si structures doped with boron up to the solid solubility limits. It is also demonstrated for the first time that ECV is better suited to profiling ultra thin boron layers including delta-layers in Si than the SRP technique. The first attempts to profile boron doped Si/SiGe structures have revealed that this material system can be depth-profiled with the electrolytes used to profile Si under optimised conditions, providing that the Ge concentration is kept below 25%. The importance of the electrolytes, leakage current, and the models used are also discussed with specific samples. Also the changes in etch current density between Si and SiGe enabled Ge profiles to be obtained in Si/SiGe heterostructures.

World record mobilities in strained SiGe channel MBE-grown normal structures are obtained through the use of very high substrate temperatures during growth whilst reducing the Ge concentration below 13% and limiting the thickness of the alloy layer. The theoretical calculations related to scattering mechanisms suggested that utilising high substrate temperatures results in reduction of both interface charge and interface roughness scattering, these being the dominant scattering mechanisms in the present material system.

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DECLARATION

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It contains an account of my own research work carried out in the Department of Physics at the University of Warwick.

The work presented in this thesis is the result of my own research except where specifically stated in the text and preceding acknowledgement.

Much of this work has been published or is in the process of being published and includes:

E Basaran, R A Kubiak, C P Parry, S M Newstead, E H C Parker and T E Whall, 'Ge content profiling in Si/GeSi structures grown by MBE', Semiconductor Science and Technology 6 (1991) 1175.

E Basaran, R A Kubiak, T E Whall and E H C Parker, 'Very high two-dimensional hole gas mobilities in strained silicon germanium', Applied Physics Letters 64 (1994) 3470.

E Basaran, C P Parry, R A Kubiak, T E Whall and E H C Parker, 'Electrochemical capacitance-voltage depth profiling of heavily boron doped silicon', in preparation.

E Basaran, R A Kubiak, R B Barlow, M Dowsett, T E Whall and E H C Parker, 'A comparison of electrical and chemical profiling of ultra thin boron layers in silicon', in preparation.

E Basaran, R A Kubiak, T E Whall and E H C Parker, 'Investigations into the depth profiling possibility of carrier concentration in *p*-Si/GeSi MBE materials', in preparation.

CHAPTER ONE

INTRODUCTION

1.1 SiGe MBE

MBE provides a powerful tool for basic research into the physics and device potential of modern semiconductor materials. The control capability over the deposition process particularly allows many considerations of both the material system and future devices to be fine tuned and investigated.

Contaminations from residual gas in the deposition chamber caused poor morphology at early stages of the development of Si MBE. With the advent of oil-free pumping techniques, UHV technology provided a vacuum quality better than 10^{-10} mbar after a bake-out enabling this method to be used at low growth temperatures (Kubiak and Parker, 1988). An unattractive feature of solid source MBE is that, due to the need to replenish the solid sources, the vacuum needs to be reestablished on a regular basis. As far as device processing is concerned, first of all the wafers have to reach the standard technology requirements for thickness, uniformity, metallic contamination, defect densities, particulates, etc. These required high quality substrates are available typically 3 inch or 10 cm in diameter. The substrate

is rotated during deposition to ensure a uniform distribution across the entire wafer. Although MBE is currently restricted to single wafer processing, a load lock enables the use of a multi-wafer cassette. The growth temperature (from room temperature to 1000°C) is controlled using a heater placed just behind the substrate holder. The flexibility of MBE allows arbitrary control over growth parameters such as growth temperature, growth rate and dopant flux. MBE growth occurs by surface adsorption and spontaneous incorporation of Si, Ge and dopant atoms and it does not depend to first order on any surface chemistry as do chemical vapour deposition (CVD) and related techniques.

Si devices have an overwhelming share in the world-wide electronic market. However in some areas, Si technology has been driven close to its physical limits. Both new and fast growing markets, such as telecommunication require increasingly more efforts to be addressed by Si devices. Intense investigations on III-V heterostructures have certainly produced superior devices. Nevertheless the potential market for these heterosystems are restricted because they lack compatibility with Si VLSI technologies.

A fundamental factor controlling the capability of electronics is the operating speed of their component devices (Singh, 1994). For some decades miniaturisation has become the key element for faster performance since function of a transistor, the most basic device in modern electronic circuits, can be improved by shrinking (Ferry and Grondin, 1991). Standard techniques used to introduce dopants into a semiconductor include thermal diffusion or implantation of energetic ions (Jones, 1991). Therefore the

dopant profiles with these methods have fundamental limits prohibiting the preparation of extremely sharp dopant profiles. Development of epitaxial techniques allowed us to grow such structures with vertical dimensions down to atomic scale so that the physical limits of the performance of devices can be explored (El-Kareh, 1993). Therefore the size-reduction process cannot be extended indefinitely, so an alternative material will have to be introduced. Because of the steady demand in the market, chip designers have naturally looked for alternative approaches to boost the speed of electronic devices. However industry has already invested tens of billions of pounds in tools and facilities for fabricating Si-based devices. Whilst other semiconductor materials such as GaAs are under current investigation, it would be clearly quite advantageous to find a path to faster performance that does not abandon Si (Meyerson, 1994). Therefore it seems very attractive to introduce Si/GeSi heterosystems with their basic compatibility with Si substrates and technologies, allowing the exploitation of band structure engineering and access to electronic and optical properties not hitherto possible. Basic properties of the Si/GeSi heterosystem have been studied for some time and device quality standards have been reached within the last few years.

SiGe MBE enables us to grow Si and SiGe alloy layers epitaxially with or without dopants on Si substrates (Kasper *et al.*, 1975 and Joyce, 1989). Because Si and Ge have the same crystal structure, a layer of one material can be deposited on the other, maintaining a consistent atomic order. An atomic flux of elemental Si and/or Ge are provided by coevaporation from electron beam evaporators. In an electron beam evaporator, the material to be grown is heated by an intense electron beam to the temperature which

provides the desired flux of atoms. The dopants typically Boron for *p*-type and Antimony for *n*-type can be evaporated from effusion cells where temperature is accurately controlled resulting in a well-controlled flux. Dopants are simultaneously incorporated during growth. The flux of the different constituents can be controlled by using mechanical shutters in front of the evaporation sources during growth. Typical growth rates range from 0.01 to 0.3 nms^{-1}. More details about Si MBE and related materials are given by Kubiak and Parker (1988).

In epitaxy, layers of atoms are deposited onto an existing crystalline material namely substrate which provides the same atomic arrangement for the newly accumulated layers as the crystal itself. Since the dopants are added during growth, a variety of doping profiles can be obtained. However there is a 4% mismatch between Si and Ge. Hence, SiGe layer growth of device quality requires both a low-temperature growth (to minimise diffusion, islanding and strain relaxation), and an oxygen-free surface passivation method (to reduce the oxygen incorporated at the interface causing crystalline defects and degradation of the electrical characteristics) (Maurizio *et al.*, 1991). Epitaxial growth techniques such as MBE (Parker, 1985; Tsao, 1993) and CVD (Meyerson, 1986) are essential for the growth of metastable alloys and for the preservation of sharp doping profiles. For successful epitaxial growth, atomically clean starting surface must be provided and preserved during growth. As opposed to CVD, MBE is a physical vapour deposition method.

Si and $Si_{1-x}Ge_x$ ($0<x<1$) heterojunctions were proposed to enable improvements in existing Si device technology but maintaining compatibility with existing processes lines (People and Bean, 1985).

1.2 DOPING CAPABILITY AND GROWTH OF SiGe MBE

The simplest method of doping during Si MBE is by coevaporation of dopant from a thermal effusion source, relying on spontaneous surface incorporation (Parry, 1991). The choice within the groups III and V elements for *n*- and *p*-type doping in SiGe MBE is a compromise between their physical, chemical and electrical properties (Kubiak and Parry, 1991). Coevaporation of the element is preferred to reduce contamination (Parry, 1991). In MBE, because the dopants are added during growth of the structure, a far better control and a variety of the dopant profiles can be obtained than with conventional techniques such as thermal diffusion or ion implantation. Extremely sharp and thin the so-called δ-doping profiles have been fabricated by the MBE growth (for example see Gossmann and Schubert, 1993).

The optimum choice of dopant and methodology depends on the most appropriate growth conditions for a given structure. For *p*-type doping, boron can readily be achieved by coevaporation of compounds or, the element to avoid oxygen incorporation at low temperatures whereas Sb is used as a favoured *n*-type coevaporation dopant.

Si and Ge can be mixed at any required ratio. However if the Ge content is increased, the lattice constant increases and the band gap narrows. Since the lattice parameter of Ge is about 4% larger than that of Si, Ge atoms would normally expand to their natural spacing; but if deposited on a much thicker Si layer, they are locked in place by the underlying Si; such that either strained or relaxed epitaxial growth of SiGe is possible on a Si substrate. Strained growth is in demand due to the lack of interfacial dislocations which could give rise to interface states and unwanted electrical effects. The interest in strained growth is also to the fact that the presence of tetragonal strain in the alloy produces a further reduction in the bandgaps with respect to the bulk alloy layer due to the splitting of degenerate valence and conduction bands (Baslev, 1966).

In order to grow high-quality layers, growth temperature is kept within a certain range and the layers do not exceed a maximum thickness (People and Bean, 1985). The maximum thickness so called metastable critical thickness for strained growth of SiGe alloys is simply defined as the thickness at which strain relaxation occurs due to the onset of misfit dislocation formation (see Iyer *et al.*, 1989). This quantity is clearly a function of the Ge fraction as shown in Fig. 1.1 and it is an important parameter for device designers since it is necessary to prevent strain relaxation and dislocation generation. It is one of the complications that the electrical activity of the dislocations is not well understood and very dependent on the interaction with impurities (Maurizio *et al.*, 1991). Whilst it is quantitatively not easy to correlate the electrical measurements to relaxation, they serve as a very sensitive measure of the heterojunction quality.

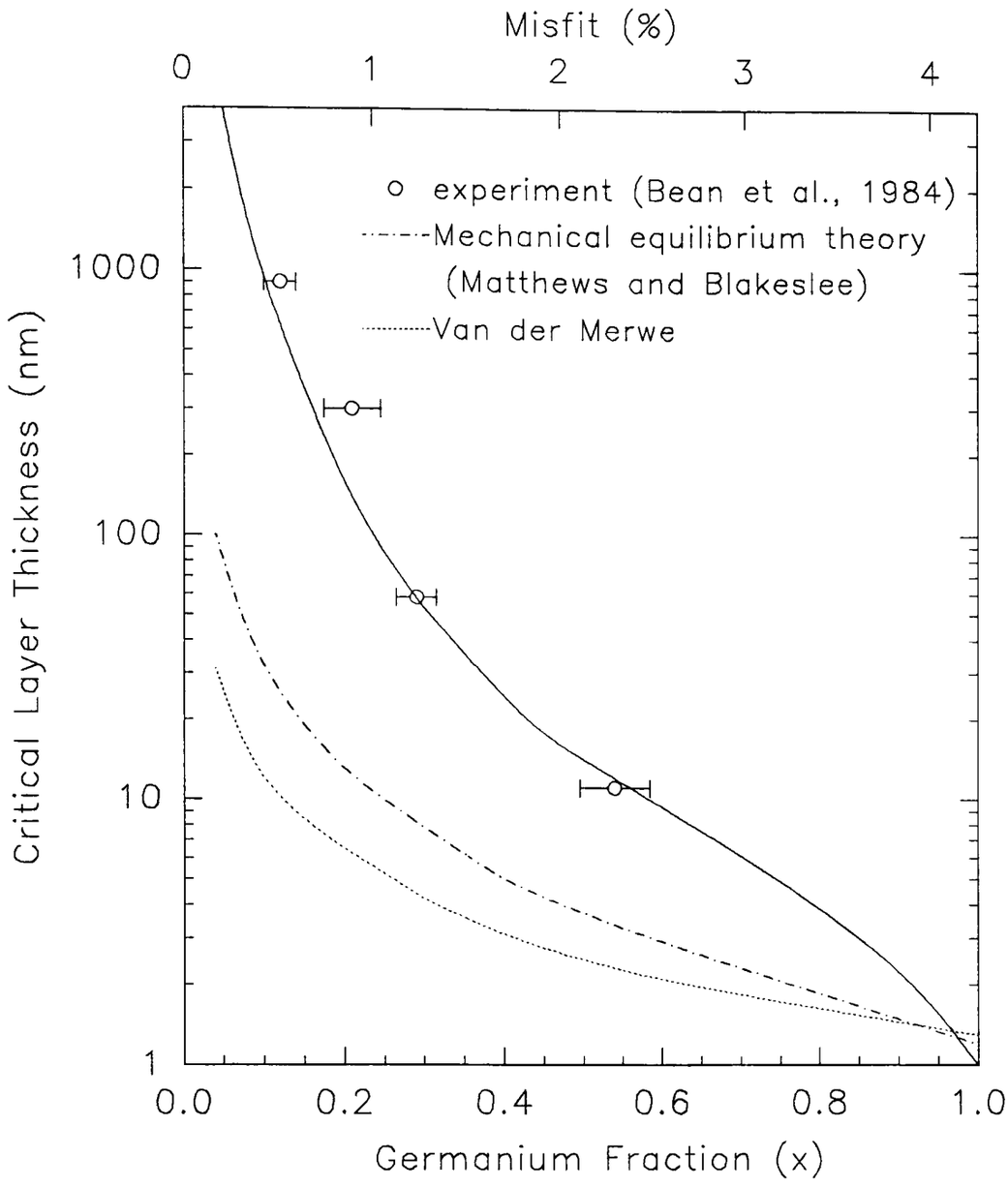

Fig. 1.1. Critical thickness as a function of Ge fraction for strained $Si_{1-x}Ge_x$ layers (After People, 1986).

As far as growth is concerned, the background doping level must be well-controlled and preferably very low (Gravesteijn, 1991). The production of high quality heterointerfaces requires the growth of buffer layers to reduce the effects of defects and dislocations arising at the substrate (Kearney, 1993). Growth temperatures have also limits due to a tendency towards Ge islanding at higher temperatures. There is a maximum growth temperature at a given Ge fraction depicted in Fig. 1.2.

With epitaxial growth techniques now maturing, ultra thin semiconductor structures can be grown routinely, leading research in semiconductor materials and devices into new era. A 'grower friendly' computer control system for accurate fabrication and reproducibility of structures facilitates the capability of the system at Warwick (Kubiak *et al.*, 1991). For example at Warwick, a boron delta layer was fabricated realising a thickness of < 1 nm and fully activated with a sheet carrier density of 3.5×10^{14} cm^{-2} (Powell *et al.*, 1991). Understanding the properties of such profiles have been in fact more a test of the resolution of the various analytical techniques than of the steepness of the carrier profile (Slijkerman*et al.*, 1989 and 1990). During the past decade, heterostructures have been extensively studied, enabling the design of a new generation of heterostructural devices (see section 1.3). However, fabrication of these structures requires very precise control of layer thickness, its uniformity and junction abruptness at heterointerfaces which depend on effective control of growth parameters such as growth temperature, fluxes of source material, and growth time. Nevertheless, reproducibility in the growth of ultra thin heterostructures is difficult to achieve due to the variations in growth

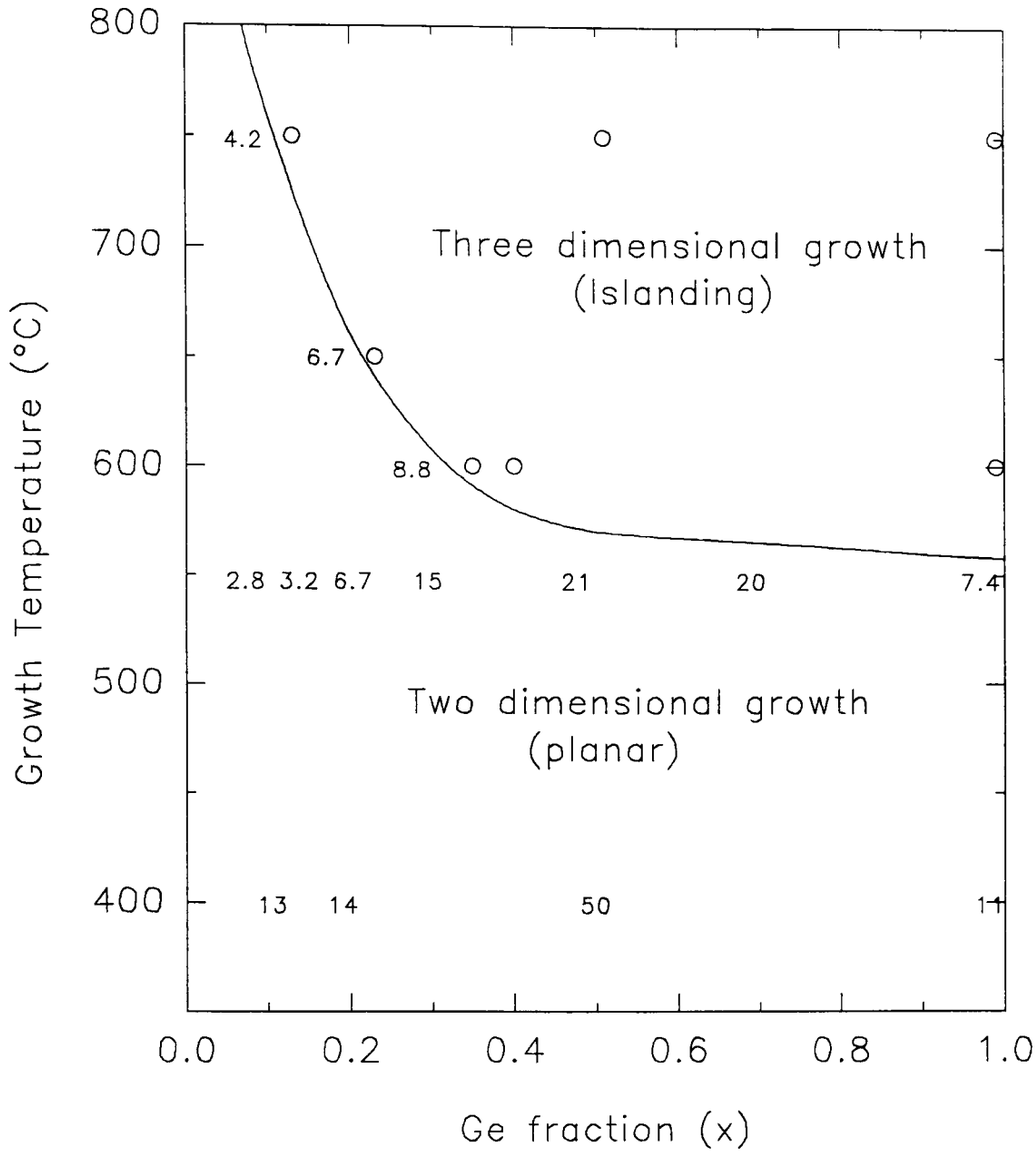

Fig. 1.2. Ideal growth morphology for $Si_{1-x}Ge_x$ on Si. Degree of crystallinity are indicated by numerical values as percentage (0, high; 100, low) determined by RBS.

parameters. Getting good short and long term stability of the matrix and dopant fluxes is particularly difficult and ±10% is regarded as good flux stability.

An *in-house* modified VG Semicon V90S MBE system having a larger chamber size and improved geometry is in use at Warwick where the epilayers in the present work were grown, except for a couple of samples which were grown by V80 MBE system as stated in the text. A schematic diagram of the V90S MBE system is given in Fig. 1.3. Flux uniformities were found to be better than ±5% across the 100 mm wafer used in the system. A report on a variety of growth factors leading to remarkable improvements in material quality and reproducibility is of significance (see chapter 5) (Kubiak *et al.*, 1993). Further details can be found in Kubiak *et al.* (1988), Powell *et al.* (1990) and Parry (1991).

1.3 THE POTENTIAL OF GeSi

Structures based on GeSi strained layers play an important role in improving existing devices and in developing new devices (Jain and Hayes, 1991). Properties of bulk crystalline SiGe alloys have been under investigation for some decades (for example see Glickman 1955, 1958 and Alonso *et al.*, 1989). By changing the composition, the band gap of the SiGe alloy varies from 1.1 eV to 0.7 eV corresponding to the wavelength range of about 1 μm to 1.5 μm providing a useful range for discrete opto-electronic devices and for integrated opto-electronic on Si.

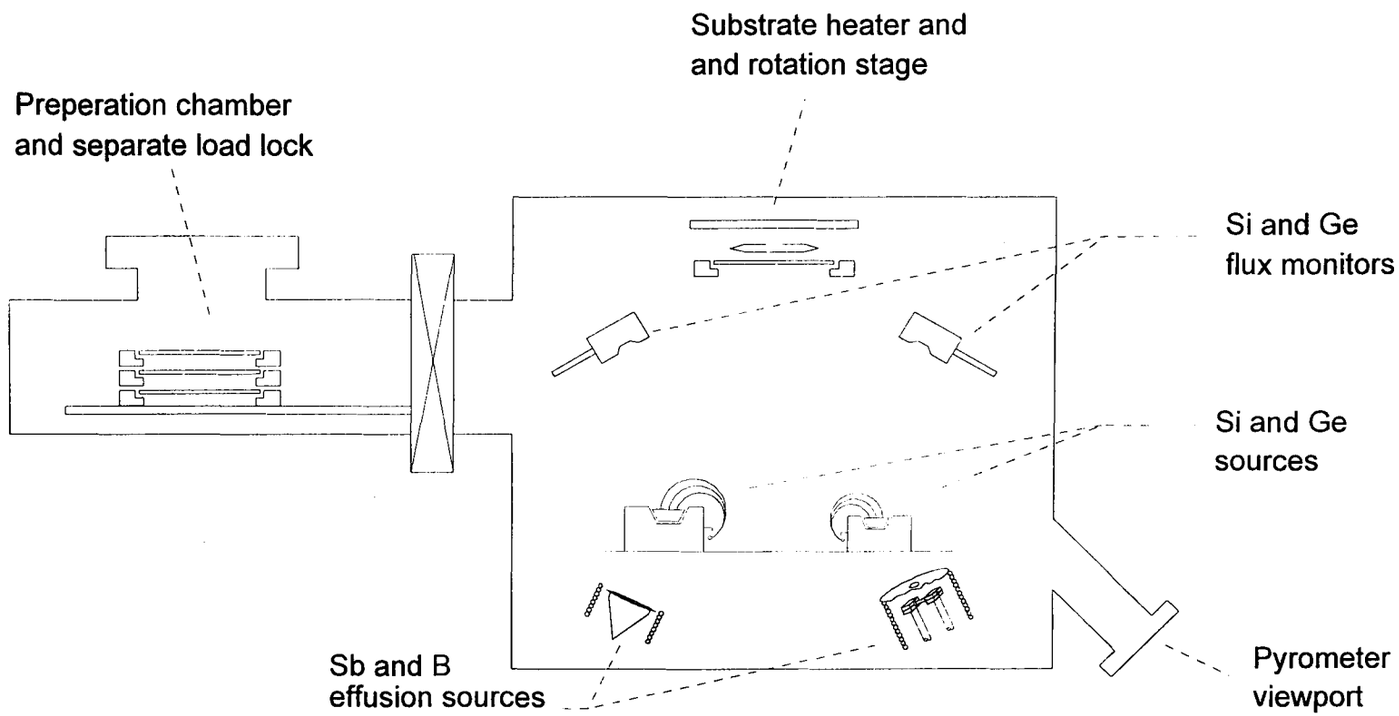

Fig. 1.3. Schematic of V90S MBE system used for the present work.

As an important application of strained SiGe layers, SiGe-HBT was first demonstrated by Iyer *et al.*, (1987). Like AlGaAs/GaAs, SiGe HBTs have an advantage over the conventional Si homojunction bipolar transistors stem mainly from that the energy band gap of the emitter is larger than that of the SiGe-base. Today, higher free carrier mobility in GaAs results in higher speed in HBTs of AlGaAs/GaAs than that of SiGe. On the other hand Si/GeSi HBT is less expensive and compatible to the existing Si technology and, show promise for improving the speed and gain of bipolar circuits (King *et al.*, 1989a,b). In a recent study, the fabrication of 100 GHz SiGe-HBT was obtained beyond the Si transistor limits by a systematic decrease of the SiGe layer thickness to 25 nm with a high boron doping level of $6x10^{19}$ cm^{-3} grown in a single run by a Si-MBE process (Kasper *et al.*, 1994). In another recent study it was reported that the features of SiGe HBTs make them particularly suitable for cryogenic operations (Cressler, 1994). The fabrication of the first SiGe:B δ-FET is also reported (Carns *et al.*, 1994).

GeSi strained layer MODFETs have been fabricated for *p*- and *n*-channel devices by Pearsall *et al.* (1986) and by Daembkes (1988) respectively. Several research groups proposed MOSFETs possessing two dimensional carrier gas systems (for example see Nayak *et al.*, 1991). MOSFETs based on selectively doped superlattices have shown improved performance. High mobility *p*-channel SiGe-MOSFETs have very recently been introduced exhibiting higher current drive compared to a bulk*p*-channel Si-MOSFET (Nayak *et al.*, 1994; Verdonckt-Vandebroek *et al.*, 1994; Scott *et al.*, 1994). More details about potential applications of Si/GeSi structures to

novel devices may be found in recent reviews (Schäffler, 1994; Miyao and Nakagawa, 1994).

1.4 STRENGTH AND LIMITATIONS OF CARRIER PROFILING TECHNIQUES USED

The simulation, fabrication and characterisation of ultra-thin impurity layers is critical and important to optimising *nanometer* range devices. The need to characterise ultra-thin doped layers (films) stems from the trend toward device miniaturisation which is expected to continue during next decade, resulting in improved circuit performance and higher circuit density (Dennard *et al.*, 1974 and Brews *et al.*, 1980). Scaling devices to smaller vertical dimensions implies lower voltages, thinner dielectrics and more abrupt and shallow profiles (Osburn *et al.*, 1980; Jiang *et al.*, 1992 and Hong *et al.*, 1991). Thus it makes scientists more and more limited by the lack of precise direct characterisation of the impurity profiles. This increases the tendency to use extrapolations from characterised and simulated profiles and to compare measured and simulated electrical results to arrive at the most probable vertical and horizontal dimensions. The increased complexity with scaling direction tends to three dimensional structures and dopant distributions for which more novel and sophisticated analysis and characterisation techniques are needed. Eventually, the challenge of reducing device dimensions below ~ 0.15 μm causes the difficulties arising from limitations, not only tool limitations, such as lithography, doping techniques, and control of impurity profiles but also inadequacy of process

and device simulators as well as limitations of profiling techniques. Furthermore, there is a lack of understanding of the physics underlying some of the device behaviours, such as quantum effects in the channel, and the breakdown of the classical drift-diffusion model (El-Kareh, 1993).

The Capacitance Voltage (CV) profiling methods have been employed with Schottky barrier junctions using metal and liquid electrolyte contacts, abrupt asymmetric *p-n* junctions, MOS capacitors and MOSFETs (Blood and Orton, 1992). Analysis of the variation of capacitance with applied voltage is the basis of several techniques for determining the net doping density and its depth profile. Studies of capacitance associated with the depletion region of a Schottky barrier on a metal-semiconductor junction provide extensive information on the concentrations and characteristics of electrically active centres in epitaxial layers and the near surface region of bulk semiconductors. Conventional depletion capacitance measurements are particularly powerful in giving information about the depth distribution of both shallow and deep impurity levels without the need for physical removal of layers of the material. However one disadvantage of conventional CV method is that the maximum depth which can be profiled is limited by electrical breakdown corresponding to a total space charge of about $2x10^{12}$ cm^{-2}. Electrochemical CV (ECV) method overcomes this limitation by chemical etch/measure cycle (Ambridge and Faktor, 1974). Unlike conventional depletion capacitance measurements, ECV method uses a fixed bias for measurements of the doping density and requires removal of the material from the semiconductor as a destructive technique. In ECV the maximum profile depth is restricted by roughening of the etched crater and

not by electrical breakdown. This feature makes ECV very attractive for the use in highly doped material. Nevertheless since the edge of the depletion region is actually smeared out by free carrier diffusion, the depth resolution is limited to a few Debye Lengths for both conventional and electrochemical CV methods. In ECV method, there is great demand for a convenient electrolyte which must provide both a satisfactory Schottky barrier and controllable electrochemical etching of the material. However it is a fast, straightforward technique and easy to interpret. Whilst conventional CV allows low temperature measurements ECV runs only at room temperature. However transport measurements via Hall technique can be carried out to determine a mobility profile, although physical removal of layers of the material is required. Generally speaking, these capacitance and transport measurements give complementary information about the semiconductor, though under the appropriate conditions the net shallow donor density obtained from the depletion capacitance is equal to the free carrier density obtain from a Hall experiment (Blood and Orton, 1992). Measurements of carrier transport phenomena relate to the properties of free carriers, chiefly the carrier density and mobility. Several methods of layer stripping are available such as (electro-) chemical etching and anodisation. Care is needed with experimental procedures such as non-uniform etching, *p-n* junction isolation, leakage currents and photo-effects and, correction of the raw data such as depletion layer and Hall scattering factor. Spreading Resistance (SR) profiling is the commonly employed technique using a small angle bevel (Pawlik, 1984). The SR method provides raw spreading resistance data which can be converted into the desired resistivity and hence carrier concentration profiles. It is destructive but allows repeat measurements,

however this is not advisable because of the inevitable surface damage caused by the probes. SR measurements are usually applied to Si. The limited application of the technique to wider gap materials such as GaAs stems from domination by barrier resistance (practical contacts show metal-semiconductor barrier effects). Each probe must be individually calibrated against standard samples whose surfaces have been prepared as nearly as possible like those of the material to be profiled. A profile involves three factors, becoming more critical if the carrier distributions vary sharply, the preparation of the bevel [small bevel angles (<0.1°) is required for sharper profiles such as by MBE growth], the choice of probe and the sequence of measurements. Some other concerns are noise, complex correction factors needed for converting and carrier spilling for steeply varying profiles. Certain prior knowledge of sample is also required.

1.5 STRUCTURE OF THESIS

The work presented in this thesis was targeted in two areas concerned with the MBE growth and characterisation of Si and Si/SiGe structures. The first was to improve the capability of the ECV technique to profile boron doped Si, for which SR profiling has been the first common choice, with the first demonstrations of profiling up to dopant solubility limits and through ultra thin doping spikes. The possibility of boron and Ge depth profilings in SiGe heterostructures employing an ECV profiler are also presented for the first time. The second objective was to enhance 2DHG mobilities by optimising growth conditions via growth parameters such as growth temperature, spacer

thickness and Ge content and lead to the world record mobilities in strained Si/GeSi system reported to date.

Following this introductory chapter, chapter 2 involves theoretical and experimental aspects presented with an emphasis on characterisation techniques used either by author or on behalf of author. It is divided into three sections; in the first, conventional and electrochemical CV profiling techniques are roughly surveyed; the second section deals with Hall measurements including mechanisms involved in 2DHG structures and in the final section, other techniques carried out on behalf of author and used for comparison reasons are given. Experimental details are also presented in each section.

Chapter 3 is concerned with the capability and limitations of ECV technique to profile *p*-type carrier concentration in Si. Profiles obtained by ECV technique are compared with conventional CV, Hall measurements and particularly SIMS profiles. Emphasis is put especially on heavily boron doped samples and ultra thin boron layers in Si, previously thought impossible to measure by ECV.

In chapter 4, the first systematic study of ECV profiling of GeSi layers are presented for Ge contents below 25%. First section is concerned with obtaining true carrier concentrations in GeSi structures with a discussion on the choice of electrolyte. Second section investigates Ge concentration-depth profiling via etch current density variations, which has already been published by the author (Basaran *et al.*, 1991).

Chapter 5 reports growth aspects of two dimensional hole gases in strained GeSi leading to the world record mobilities to date (Basaran *et al.*, 1994). A great number of structures are explored through Hall measurements at low fields and temperatures of 4-300 K. Ge content behaviour and diffusion effects is also given.

Finally, chapter 6 presents conclusions.

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CHAPTER TWO

THEORETICAL AND EXPERIMENTAL ASPECTS

This chapter provides an overview of the techniques used by the author or on behalf of the author and the experimental aspects related to the research. Growth details of the test samples grown by V90S MBE system on Si substrates at Warwick University are given in the following chapters where it is of interest.

2.1 METAL-SEMICONDUCTOR SCHOTTKY BARRIERS

2.1.1 INTRODUCTION

Electrical contacts to semiconductors are critical elements in a number of important technologies. The key electrical property of semiconductor contacts is the value of the ratio of forward and reverse current densities which will determine whether the junction acts as a rectifier, an ohmic contact or as a mixture of these limiting cases over the current density range of

experimental interest. (Sze, 1981). The current-voltage relationship for most semiconductors can be described by

$$J = J_0\left[\exp\left(-\frac{qV}{nkT}\right)-1\right] \qquad (2.1)$$

where J is the total current density, J_0 is the reverse saturation current density, V is the applied voltage, n is the diode ideality factor, k is the Boltzmann constant, T is the absolute temperature and q is the electronic charge. *I-V* characteristics can thus provide useful information on a diode for subsequent capacitance measurements, since the net doping density may be obtained from measurements of the depletion capacitance (see section 2.1.2) associated with the band bending region of a metal Schottky contact (Fig. 2.1). When a *p*-type semiconductor is brought into contact with a metal, holes will flow from semiconductor into the metal leaving a negative charge of the ionised shallow acceptor dopants within the semiconductor. This initial charge transfer will produce Fermi levels coincident creating a step between the Fermi level in the metal and the semiconductor valence band edge such that barrier height can be calculated as (Schottky, 1939)

$$\phi_b = E_g + \chi_s - \phi_m \qquad (2.2)$$

where E_g is the band-gap of the semiconductor, ϕ_m is the metal work function and χ_s is the electron affinity of the semiconductor. For zero applied bias, the band bending or built-in potential which occurs in the semiconductor depends on the doping level:

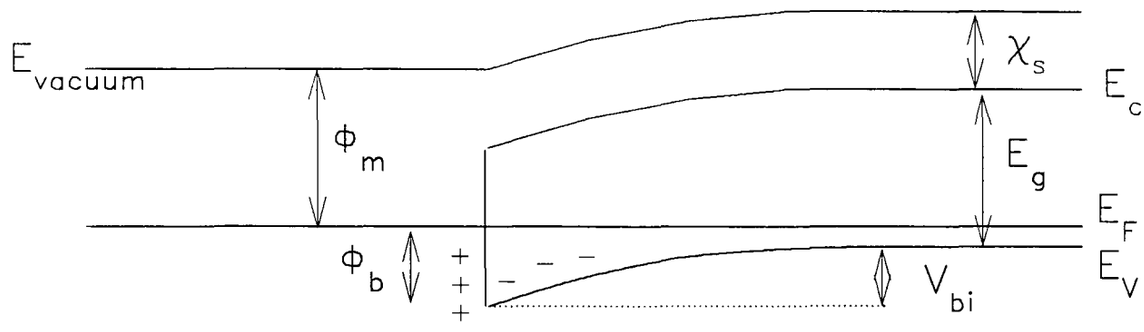

Fig. 2.1. Schematic of Metal–Semiconductor Schottky barrier formation.

$$V_{bi} = \phi_b - \frac{E_F - E_V}{q} \qquad (2.3)$$

where E_F is the Fermi energy and E_V is the valence band edge.

It has been determined experimentally that most semiconductor metal contacts do not conform to the predictions of the ideal Schottky limit as given above (Rhoderick and Williams, 1988). Surface states are among the proposed explanations. In our case, for example a few nm thick native oxide is formed on the semiconductor surface on removal from the MBE system. Furthermore deposition of metal (e.g. using sputtering) may result in a non-abrupt interface influencing the electronic band structure.

2.1.2 CONVENTIONAL CV PROFILING

The CV technique relies upon the fact that the width of a reverse-biased space-charge region of a semiconductor junction depends on the applied voltage. The band bending across the depletion layer is defined by the sum of the built-in potential and the applied bias, so Poisson's equation relates the electrostatic potential Ψ to the space-charge density $\rho(x)$ such that (Blood and Orton, 1992)

$$\frac{d^2\psi}{dx^2} = -\frac{1}{\varepsilon\varepsilon_0}\rho(x) \qquad (2.4)$$

where ε is the dielectric constant and ε_0 is the absolute permittivity. From this expression and using the band bending, the depletion width which describes the transition between the depletion and the neutral regions may be determined as

$$x_d = \left(\frac{2\varepsilon\varepsilon_0}{qN_A} V \right)^{1/2} \qquad (2.5)$$

where N_A is the acceptor dopant concentration.

The depletion layer of a Schottky barrier of *p*-type semiconductor contains a distributed fixed space charge due to ionised acceptors. A small increment dV of the bias results in an increment of the depletion width and this causes an increase in fixed charge per unit area dQ so that a small signal capacitance associated with the depletion region can be defined as

$$C = A \frac{dQ}{dV} \qquad (2.6)$$

where A is the diode area. Calculation of the total charge Q stored in the depletion region in terms of the total band bending V is calculated by integrating Poisson's equation to give the electric field applying Gauss' theorem to obtain Q(V). Differentiation of Q(V) gives the exact expression for the capacitance in terms of the total voltage across the depletion region for uniformly doped material. If the expression is simplified for room temperature and common semiconductors one may obtain (Blood and Orton, 1992)

$$C = A\left(\frac{q\varepsilon\varepsilon_0 N_A}{2}\right)^{1/2}\left(V - \frac{kT}{q}\right)^{-1/2} \qquad (2.7)$$

With assumption V>>kT/q, the equations (2.5) and (2.7) yield :

$$C = \frac{\varepsilon\varepsilon_0 A}{x_d} \qquad (2.8)$$

i.e. similar to the expression for a parallel plate capacitor.

An indication of the magnitudes of the quantities associated with the depletion capacitance for V=1 v as a function of N_A is given in Fig. 2.2. The doping profile N_A can now be determined at the edge of depletion layer by the dependence of the capacitance on reverse bias (Schroder, 1990)

$$N_A = \frac{1}{q\varepsilon\varepsilon_0 A^2}\,\frac{C^3}{dC/dV} \qquad (2.9)$$

The assumptions made for the depletion approximation explicitly state that the semiconductor can be divided into two distinct regions (a space charge region and a neutral bulk region) which is sharp and which defines the depletion depth. Because carrier diffusion will occur, the depletion edge is non-abrupt and the carrier distribution into the depletion region is given by (Blood, 1986).

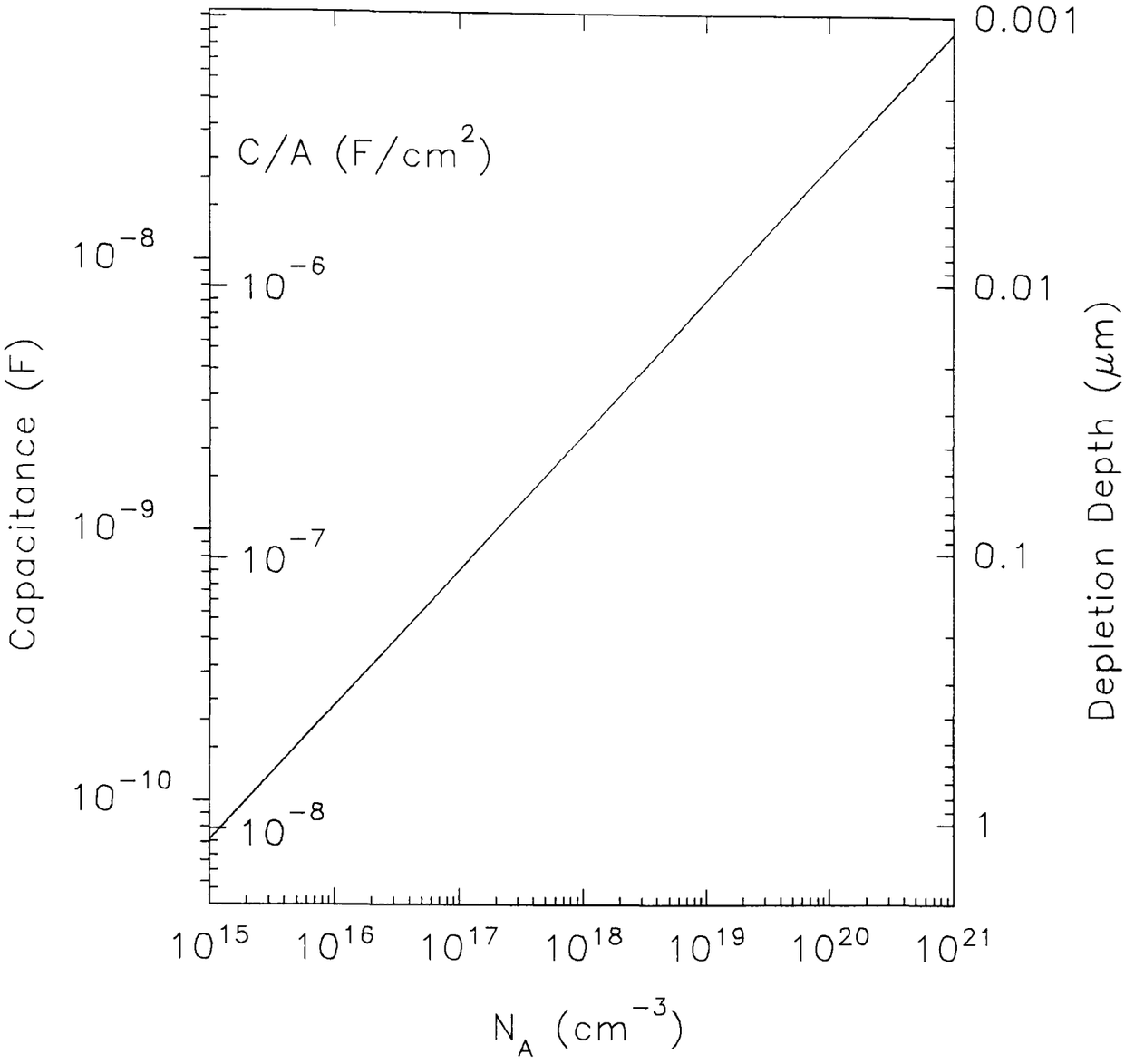

Fig. 2.2. Graph of capacitance per unit area and depletion depth for V=1 V given as a function of N_A for ϵ=12, and capacitance for 1 mm diameter contact.

$$p(x) = N_A \exp\left[\frac{1}{2}\left(\frac{x_d - x}{L_D}\right)^{1/2}\right] \qquad \text{for } x < x_d \qquad (2.10)$$

Carrier spilling occurs into the depletion region according to the characteristic Debye Length L_D given by

$$L_D = \left(\frac{\varepsilon\varepsilon_0 kT}{q^2 N_A}\right)^{1/2} \qquad (2.11)$$

The Debye Length is indicative of the abruptness of the space charge distribution near X_d and represents the distance over which free holes redistribute themselves in the vicinity of a fixed charge. A plot of L_D versus N_A for silicon at 300 K is given in Fig.2.3. The requirement of the depletion approximation that the depletion layer edge is abrupt is satisfied when the depletion depth is very much greater than L_D. Therefore CV profiling can only measure the free carrier density rather than the doping density, particularly for non-uniform doping steps (Kennedy and O'Brien, 1969).

2.1.3 EXPERIMENTAL ASPECTS

For conventional CV measurements, samples were cleaved into ~1 cm^2 sections and 1mm diameter Ti Schottky contacts sputtered onto the surface. Ohmic contacts to the p^{++} substrate were made using Al deposited on the wafer backside. No precleaning was used before contacts were

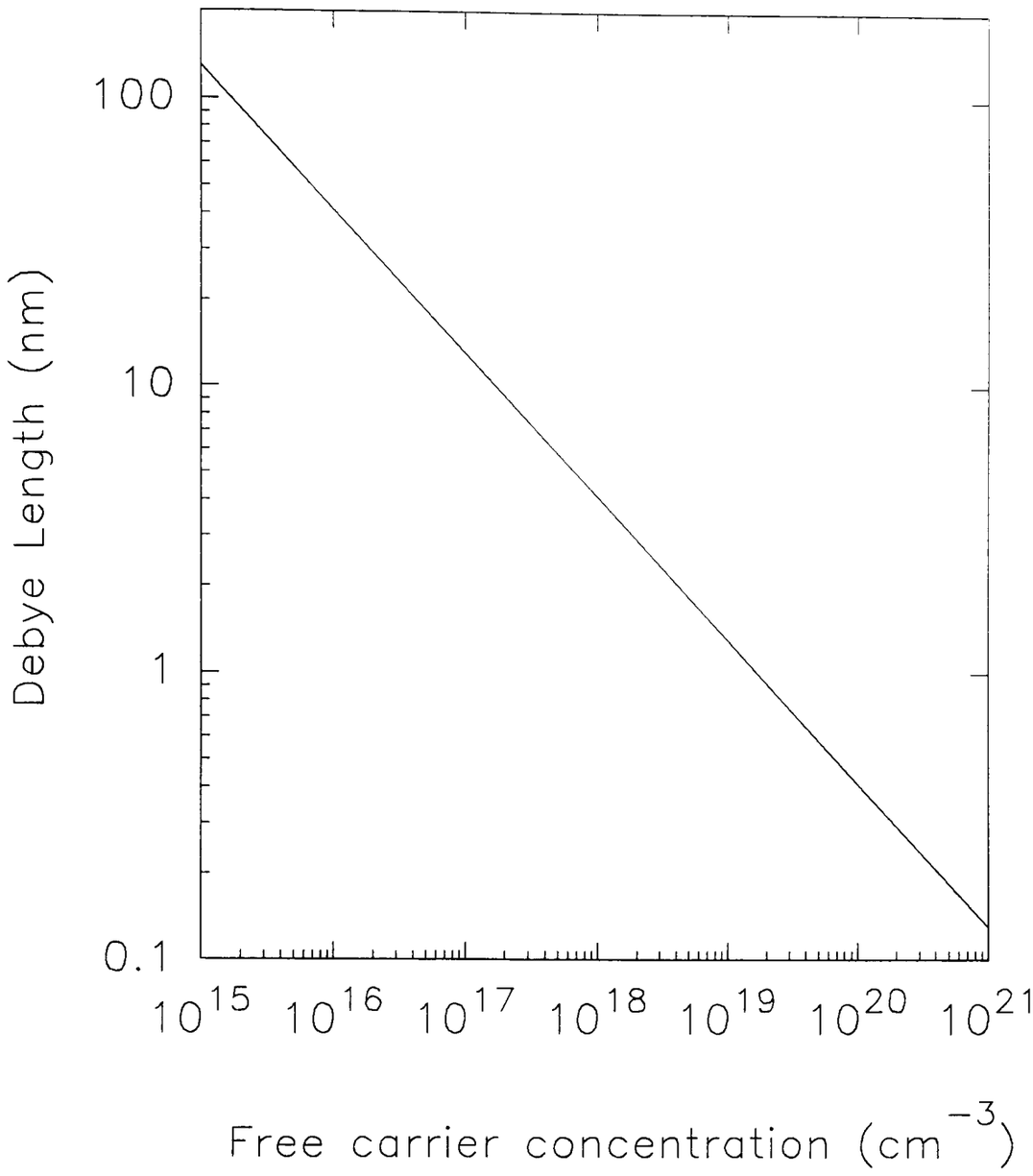

Fig. 2.3. Debye Length as a function of the free carrier concentration in Si at 300 K.

deposited. An in-*house* made sample holder was employed. *I-V* measurements were made using an HP 4140A DC voltage source. Dual frequency measurements (Lonnum and Johannessen, 1986) were then carried out to obtain carrier concentration profile using an HP 4192A impedance analyser with control and data acquisition to a PC through an IEEE bus.

2.2 ELECTROLYTE-SEMICONDUCTOR SCHOTTKY BARRIERS

2.2.1 INTRODUCTION

Both conventional and electrochemical profiling methods are based on the results developed in section 2.1 and are therefore limited by the assumptions of the depletion approximation. A suitable electrolyte in contact with a semiconductor, as in the case of the metallic contact in conventional CV, permits electrostatic potential changes to penetrate into the semiconductor due to charge carrier density levels of semiconductors.

Considering a *p*-type semiconductor, the dominant charged species are free holes and fixed negatively charged acceptor centres. The electrolyte used for ECV contains mobile negative and positive ions. On contact the electrochemical potential for holes is equalised (the Fermi level is continuous and is flat). If a positive ion is held at the interface, holes within the semiconductor near-surface region will be repelled creating a depletion region

within the semiconductor. On the other hand, if negative electrolyte ions predominate at the interface, free holes in the semiconductor will be attracted towards the surface, creating an accumulation region. Generally speaking the depth distribution of potential must be considered on both the electrolyte and the semiconductor sides of the interface. As the depletion region is of interest for this work, we shall concentrate on the semiconductor behaviour and assume negligible field penetration into the electrolyte by working with concentrated solutions ($\geq$ 0.1M). In considering the electrolyte-semiconductor interface providing that the electrolyte is concentrated, the expressions developed by Schottky (1939) can be employed to describe space charge for the depletion layers at metal-semiconductor interfaces. The measured capacitance will be that of the depletion layer and the electrolyte in series. For concentrated electrolyte the latter will be large (~10 μFcm^{-2}), thus the measured capacitance will closely approximate to the depletion layer capacitance. Excellent agreement with theory has been obtained by Dewald (1960) for a ZnO semiconductor electrolyte interface.

2.2.2 ELECTROCHEMICAL C-V PROFILING

The principles of ECV profiling have been extensively documented (for example see Blood and Orton, 1992). In ECV, an electrolyte is chosen which can both replace the metal to form a Schottky barrier, as well as etch the semiconductor controllably under appropriate bias conditions. By sequentially etching the semiconductor material electrochemically in forward bias and measuring the necessary parameters in reverse bias a depth profile of doping

level can be produced. A computer controlled instrument embodying these principles has been developed (Ambridge and Factor, 1975) and is manufactured commercially by Bio-Rad (BioRad, 1989). The Bio-Rad PN4300 was employed in this study.

2.2.2a ANODIC DISSOLUTION OF Si AND SiGe

One of the requirements of electrochemical C-V profiling is to obtain smooth and flat dissolution of semiconductor under investigation. If this criterion is not satisfied, an error will be introduced not only in etch depth but also in carrier concentration particularly in the region of junctions. Holes are needed to promote the anodic dissolution. In the case of *p*-type material, these are already available in the structure but for *n*-type material a 150 W halogen lamp light of photon energy greater than the band gap (Palmer, 1990) is employed to create electron-hole pairs. It is also important that the electrolyte should provide a dissolution rate sufficiently fast for practical use, however, this should also be controllable since it determines the depth resolution. The etch depth is obtained by integrating the dissolution current (i.e. the current flowing through the cell under forward bias) using Faraday's law

$$x_r = \frac{M}{zF\rho A}\int_0^t I\,dt \qquad (2.12)$$

where M molecular weight of the semiconductor

ρ density

z Dissolution valence number

F Faraday's constant

A major problem encountered during anodic dissolution of both *n*- and *p*-type Si is the gas evolution (H_2) from the semiconductor surface under anodic bias, reaching a maximum at or near the current peak (Sharpe and Lilley, 1980). Although reduced at higher voltages, bubbles are noticeable on the surface after a period of several minutes. A solution for this problem is to jet (pulse) the electrolyte near the Si electrode at regular intervals to remove bubbles. A second solution is to employ a wetting agent such as Triton X-100 (BioRad, ECV PN4200 profiler manual).

Effective dissolution valence number, which is a measure of the number of holes that are required to remove one molecule of the semiconductor, needs to be determined experimentally. It has been shown that for HF electrolyte/silicon the dissolution valence is dependent on carrier concentration and type as well as illumination and current levels, varying over a range of $2<N<4$ (Arita, 1978). Sharpe and Lilley (1980) have found the dissolution valence number as 3.5 ± 0.3 for *n*-type Si.

2.2.2b THE ELECTROCHEMICAL CELL

One of the most important parts of the ECV instrument is the electrochemical cell depicted in Fig.2.4. The cell has a sealing ring on which the sample is mounted and by which the contact area is defined. Initially

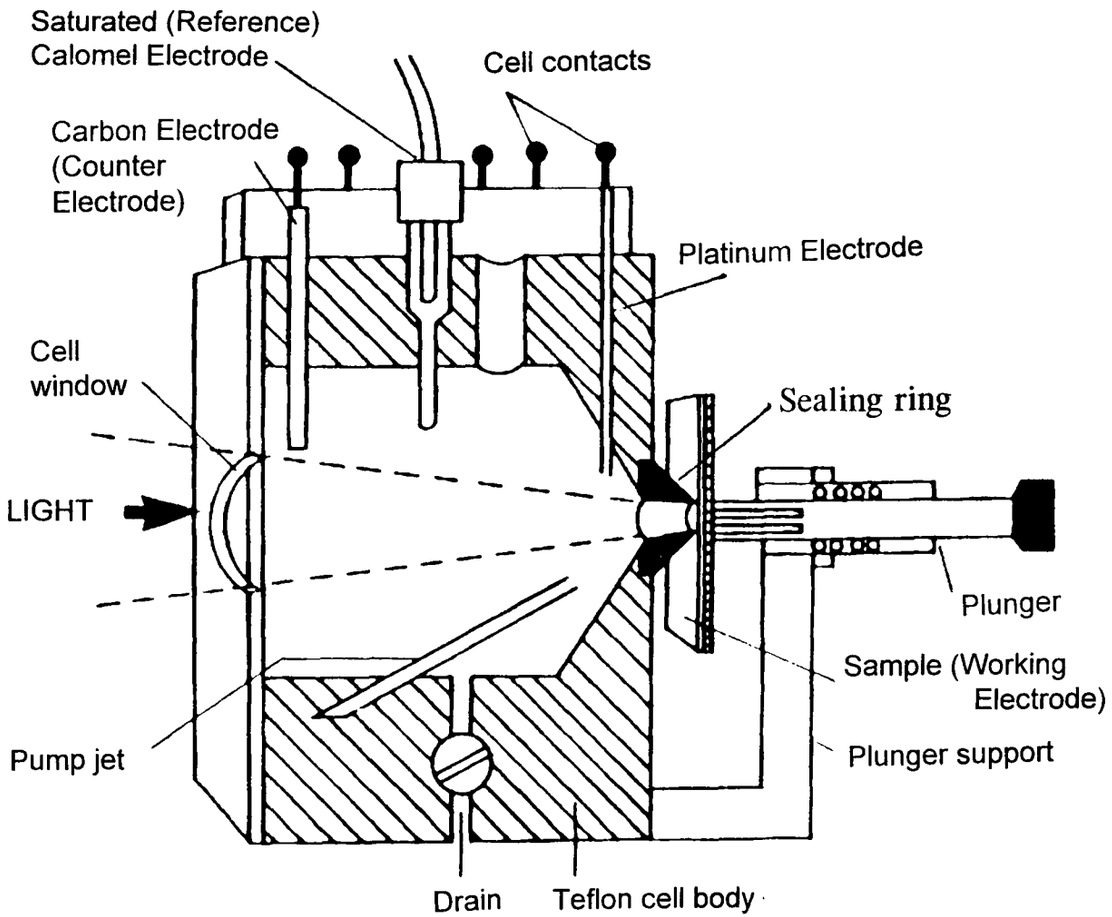

Fig. 2.4. The Electrochemical Cell for the ECV Profiler.

prepared electrolyte is poured into the cell with a syringe after the semiconductor is mounted onto the sealing ring. Since the semiconductor also acts as a working electrode for the dissolution, InGa eutectic is usually applied onto the back of the semiconductor to form good ohmic contacts which should be checked prior to etch profiling. A carbon (counter) electrode in the cell is used to complete the current circuit for etching the working electrode (sample). A saturated calomel electrode is used as a reference against which the equilibrium (rest) and overpotential can be measured. The correct conditions are ensured by monitoring the potential difference and reference electrode. With the counter and working electrodes open circuit (zero current) the measured potential is referred to as the rest potential and is the equilibrium or reference point for the system. From the measurements of the rest potential with and without illumination the semiconductor type can be ascertained. During illumination, electron-hole pairs are created in the depletion region and swept out in opposite directions by the electric field. As *p*- and *n*-type materials will produce photovoltages of opposite sign, they can be differentiated. For *p*-type material the electrode potential will become positive and conversely for *n*-type material it will become more negative.

2.2.2c THE IMPORTANT PARAMETERS

Information on the following parameters is crucial in ECV profiling:

Diode area should be determined as accurately as possible since it affects both depth and carrier concentration (see equations 2.8, 2.9 and

2.12). Accurate measurements of etch depth and capacitance also depend on a well defined area, with minimum leakage of electrolyte under the sealing ring. Sealing rings of 1 and 3mm diameter are available with the commercial instrument. The larger area is usually the choice since this increases the value of C, decreases the series resistance and reduces the fractional error in A (Blood, 1986). Although the area must be entered prior to profiling, the profile can be recalculated by using the raw data saved, after the area is measured. Determination of the area becomes rather complicated for *n*-type materials where illumination of the samples is needed for etching reasons (for details see Blood and Orton, 1992).

Dissipation factor (D) gives an indication of the quality of the Schottky diode at the semiconductor/electrolyte interface and is defined as the cotangent of the phase angle of the capacitor. In the parallel model, it is given by

$$D = \frac{\mathrm{Re}\, Y}{\mathrm{Im}\, Y} \qquad (2.13)$$

and in the series model

$$D = \frac{\mathrm{Re}\, Z}{\mathrm{Im}\, Z} \qquad (2.14)$$

where Y and Z are admittance and impedance respectively.

The **flatband** or **built-in potential** (V_{bi}) of a Schottky diode is measured with the assumption of uniformly doped material

$$V_{bi} = \frac{C}{2\left(dC/dV\right)} + V \qquad (2.15)$$

This value indicates how closely the measurements of C and dC/dV conform to the Schottky equation and hence how closely the junction approximates to a Schottky diode. This factor is also used to choose the most appropriate measurement voltage as discussed in chs. 3 and 4.

The depletion depth W_d is determined by measuring C and using equation (2.8). The measurement depth is the sum of the depletion depth and the etch depth as obtained from equation (2.12). The parameters C and dC/dV in the ECV method are obtained by using a slowly modulated high frequency voltage. The electrochemical cell along with the reference (termination) resistor and various stray admittances form a potential divider. For the purposes of analysis, this is taken to be of the form shown in Fig. 2.5. In the potential divider circuit used by the PN4300, the semiconductor/electrolyte interface is represented by an equivalent circuit of a capacitor and a resistor which are the depletion capacitance and the leakage current. A composite drive voltage (carrier+modulation+DC bias) is applied across the potential divider (Y1+Y2) and the output signal is measured across Y1. In order to get a good signal/noise ratio, the termination resistor is chosen so that Y1 is approximately equal to Y2. The various stray admittances are determined initially in the cable compensation

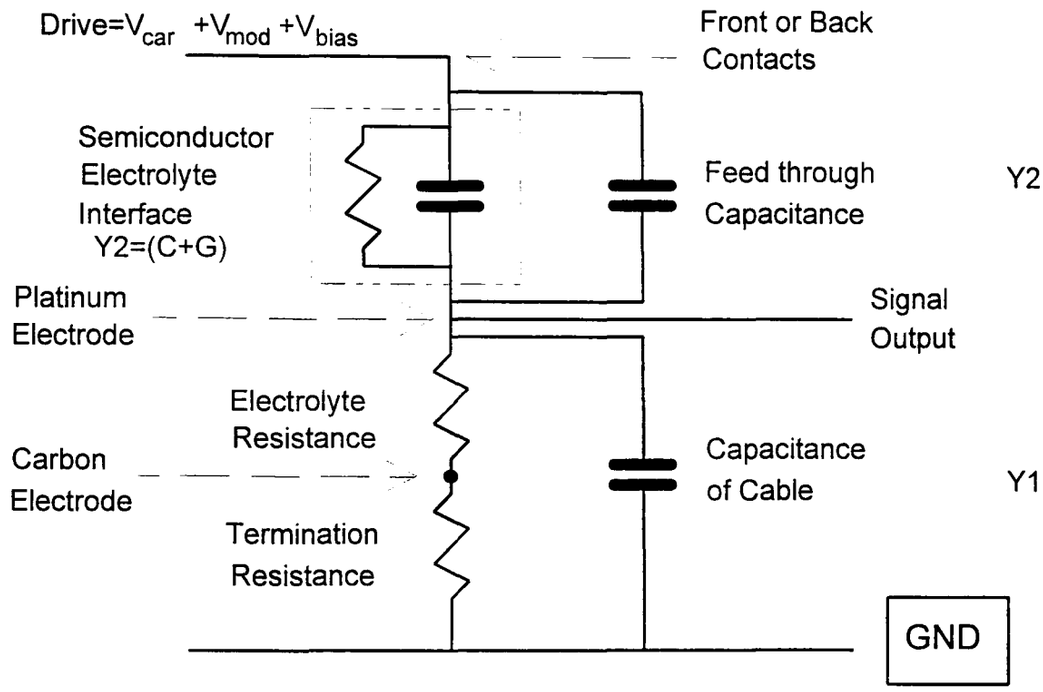

Fig. 2.5. Potential divider used by the ECV profiler (PN4300)

section of the program and C and G are determined as acquired by application of vector analysis. Because all the admittances in the network apart from C and G are independent of potential, dC/dV can be extracted from the amplitude and phase of the modulated component of the waveform and hence N can readily be calculated from eq. (2.9).

2.2.2d MODELS USED

In reality, the Schottky diode has a leakage current and a series resistance, as shown in Fig. 2.6 (a). It has been demonstrated that the influence of a series resistance in electrochemical profiling may lead a large measurement error (Hager, 1988). It has been suggested that if a dual frequency measurement is applied to the equivalent circuit, true capacitance can be correctly measured from the series resistance representing the sum of the resistances of the electrolyte between sample surface and platinum electrode, of the bulk semiconductor and of the contacts to the semiconductor surface. However in practise the analysis is not straightforward and involves small differences in measured values which tend to magnify errors.

The software (V.2.1) with the ECV profiler used in this work employs two models, parallel and series as shown in Fig. 2.6 (b) (Briggs and Stagg, 1988). Calculations for both models can be carried out after experiment by using the raw data. In the parallel model, capacitance is given by

$$C_p = -\frac{\mathrm{Im}\, Y}{2\pi f} \qquad (2.16)$$

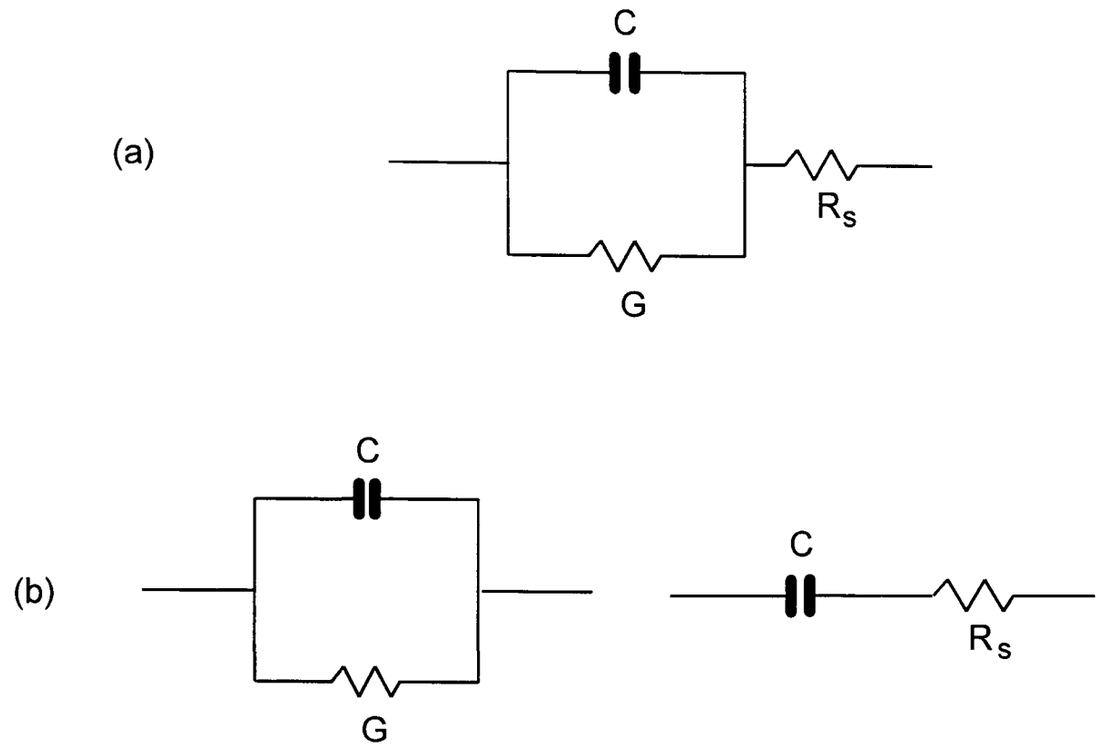

Fig. 2.6 (a) Equivalent circuit for a Schottky barrier,
(b) Equivalent circuits that ECV uses.

and differential capacitance is

$$\frac{dC_p}{dV} = -\frac{1}{2\pi f}\mathrm{Im}\left(\frac{dY}{dV}\right) \qquad (2.17)$$

By using conversion equations, one can determine the values in the series model as

$$C_s = \frac{\mathrm{Re}\,Y^2 + \mathrm{Im}\,Y^2}{2\pi f\,\mathrm{Im}\,Y} \qquad (2.18)$$

and

$$\frac{d}{dV}\left(\frac{1}{C_s}\right) = -2\pi f\,\mathrm{Im}\left(-\frac{1}{Y^2}\frac{dY}{dV}\right) \qquad (2.19)$$

The use of these conversion expressions allows the carrier density-depth profiles to be obtained for both models.

2.2.3 EXPERIMENTAL ASPECTS

The ECV profiler was commercially manufactured by BioRad (BioRad, 1989) after that described by Ambridge and Factor (1975). The Computer controlled profile plotter (model PN4300 with software version 2.1) employed here can use test frequencies of 1 to 25.5 kHz and of 0.01 to 2.55 kHz to

measure capacitance and differential capacitance respectively. Two different sealing rings are available to define the area at approximately 1 and 3 mm of contact diameters fitted onto the electrochemical cell (see section 2.2.2b). The sample is held against a PVC sealing ring using spring loaded sharp pins producing an essential ohmic back contact. The circuit connection to the electrolyte is made with a platinum (Pt) electrode to monitor the *C-V* behaviour. Electrolytes employed for ECV profiles are given in next chapter. Static *I-V* and *C-V* measurements were made prior to profiling to establish ohmic contact integrity (<3 ohms), to examine the behaviour of the sample/electrolyte barrier, and to select optimum bias conditions. After each profile, the actual etched area was established and investigated using a travelling microscope, and the crater depth was measured by a surface profilemeter (Talystep). To obtain the carrier concentration-depth profile, these measurements were then combined with the *C-V* and integrated etching current data. A complete profile takes between 1 and 4 hours, depending on such parameters as etch steps, etch current, settling time, and required etch depth. It is important to realise that all voltages are given with respect to saturated calomel electrode (SCE). In all ECV profiles, unless specified, the conditions employed are an etch voltage of 2 V, settling time of 10 s, measurement frequency of 3.2 kHz and modulation frequency of 40 Hz.

The program with the profiler allows interruptions to any profile under etch/measure cycle at any time and the performance of any other measurement at a particular etch point, such as *I-V* and *C-V* behaviours and, depletion profiling. Also, spot measurements for both models can be carried out for different measurement voltages to investigate the resultant parameters

to allow the user to judge whether a profile is running properly. Raw data was transferred to a PC, including name of material, specimen description, frequency (w) used (rads/s), both wetted and illuminated areas (cm^2), etch constant (=z ρ / M) (V mol cm^{-3}) and data in the pattern of Q_{tot} (μC) (total integrated current), Yr (S) (=ReY), Yi (S) (=ImY), dYr (S), dYi (S). Area and etch depth may then be measured and used to recalculate the carrier concentration-depth values in both models as well as other parameters may be calculated such as series and parallel resistances, FBP and dissipation factor.

2.3 HALL EFFECT

2.3.1 INTRODUCTION

Hall Measurements provide a direct measure of free carrier type and density, and yield a value for the appropriate carrier mobility. Information on Hall effect and resistivity over wide temperature range (e.g. 4-300 K) can be analysed to give information regarding impurities, imperfections, uniformity, scattering mechanisms, etc. which is unique to the technique.

The technique is destructive and involves etching a sample cross and forming electrical contacts with an InGa eutectic and gold pads. In the method used errors due to sample geometry and non-ideal contacts can be compensated (Van der Pauw, 1958) (ASTM F76-73, 1976). Theoretical

analysis of the experimental results on MBE-grown remote doped Si/SiGe 2DHG structures is given in detail in the work by Emeleus (1993).

2.3.2 THEORETICAL CONSIDERATIONS

2.3.2a REMOTE DOPING

With the advent of the mature epitaxial growth techniques, sequential deposition has become possible to form thin sandwich-type semiconducting structures in which potential steps in the valence and conduction bands are formed at the heterointerfaces. By restricting the thickness of individual layers to a few atomic spacing, charged carriers can be quantum mechanically confined to two dimensions. Moreover it is possible to vary the shape of the confining potential and the carrier population in the quantum well by changing the layer thickness or the material composition. By doping remotely from the well, spatial separation of charge carriers and impurity sites reduces ionised impurity scattering leading to higher mobilities (Dingle *et al.*, 1978).

2.3.2b SCATTERING MECHANISMS

Whilst scattering by lattice imperfections is relatively insensitive to temperature variations, phonon scattering decreases dramatically with reducing temperature. The latter becomes negligible below 20K which

enables the experimentalist to investigate the role of imperfections in limiting the carrier mobility. However in very high mobility (8.5×10^6 $cm^2V^{-1}s^{-1}$ at 1.5K) $GaAs/Al_xGa_{1-x}As$ heterojunction samples, the electron-phonon interaction dominates even at low temperatures (Foxon *et al.*, 1989). Theoretical calculations of hole mobility were carried out for strained SiGe quantum well considering specific scattering mechanisms (Laikhtman and Kiehl, 1993). Specific scattering mechanisms were also formulated and discussed by Emeleus *et al.* (1993) and Monroe *et al.* (1993) for Si/GeSi heterostructures.

The setback between the dopant layer and the nearest edge of the channel is one of the parameters controlling the effectiveness of remote doping which may be determined by estimating the mobility for **remote impurity scattering**. By treating screening in the 2D Thomas-Fermi approximation Emeleus *et al.* (1993a) have shown that mobility for the theoretical remote impurity is over 1×10^7 cm^2 V^{-1} s^{-1} for sheet densities below 2×10^{11} cm^{-2} which is the case for experimental data presented in chapter 5. For this reason the theoretical remote impurity contribution to the mobility is ignored.

For two dimensional systems, the relaxation time in the Born approximation at T=0K for wave number q is given by (Gold and Dolgopolov, 1986)

$$\frac{1}{\tau} = \frac{1}{2\pi E_F} \int_0^{2k_F} dq \frac{q^2}{(4k_F^2 - q^2)^{1/2}} \frac{\left\langle |U(q)|^2 \right\rangle}{\varepsilon(q)^2} \qquad (2.20)$$

where E_F is the Fermi energy, k_F is the Fermi wave number and $\langle |U(q)|^2 \rangle$ represents the presence of disorder. Planck constant is set equal to 1. The dielectric function is given by

$$\varepsilon(q) = 1 + \frac{2\pi e^2}{\varepsilon q} F(q) [1 - G(q)] g^o(q) \qquad (2.21)$$

where F(q) is the form factor accounting for the thickness of the gas and G(q) is the Hubbard form of the local field correction and evaluated as $1/\sqrt{5}$ for $q=2k_F$, $g^o(q)$ is the polarizability of the 2DHG and ε is the dielectric constant of the host material.

Interface roughness scattering stems from a nonplaner interface between the Si and SiGe layers. One or two monolayers at the heterojunction is a transition region due to random distribution of the Ge atoms in the alloy. Also growth may result in 3D islanding which is dependent on a number of factors such as growth temperature, deposition rate and high Ge content (see chapter 1). The random potential for the scattering by the interface roughness is expressed as

$$\langle |U_{IR}(q)|^2 \rangle = \pi(\Delta\Lambda q_s E_F)^2 \left(1 + \frac{2N_{Depl}}{n_s}\right)^2 e^{-q^2\Lambda^2/4} \qquad (2.22)$$

where Δ and Λ are the height and length parameters of the interface roughness scattering, q_s is the Fermi screening wave number at T=0K and

N_{depl} is the depletion density. Using the equation (2.22) in (2.20), Emeleus (1993) simplifies the relaxation time for maximum scattering rate ($k_F\Lambda$~1).

Interface impurity scattering is caused by contamination of the heterointerface with impurities during growth in a metallic environment. The scattering potential by charged impurity density n_i is given as

$$\left\langle \left| U_{CI}(q) \right|^2 \right\rangle = \frac{4n_i}{q^2}\left(\frac{\pi e^2}{\varepsilon}\right)\left[1+\frac{q}{b}\right]^{-6} \qquad (2.23)$$

where

$$b = \left[\frac{12m^* e^2}{\varepsilon}\left(N_{Depl}+\frac{11}{32}n_s\right)\right]^{1/3}$$

The random distribution of Ge atoms in MBE-grown SiGe alloys results in potential fluctuations giving rise to **alloy scattering** of mobile carriers. Using the random potential for alloy scattering (Gold, 1988)

$$\left\langle \left| U_{AL}(q) \right|^2 \right\rangle = x(1-x)\frac{3a^3 b}{2^7}(\delta V)^2 \qquad (2.24)$$

one can obtain the relaxation rate as

$$\tau = \frac{9m^*}{64}\left(\frac{k_F}{q_s}\right)^2 \frac{x(1-x)ba^3(\delta V)^2}{F(2k_F)}\left[1-G(2k_F)+\frac{2k_F}{q_s}\right]^{-2} \qquad (2.25)$$

where x is the Ge content, a is the alloy unit cell and δV is the spatial average of the fluctuating alloy potential over the alloy unit cell.

2.3.3 EXPERIMENTAL ASPECTS

For uniformly and heavily boron doped samples, Hall measurements provided an independent assessment of electrical activation (to an accuracy of ±10%) made on cross-shaped samples, applying the van der Pauw technique (Van der Pauw, 1958), and using the scattering factor appropriate to heavily boron doped Si of 0.7 (Sasaki *et al.*, 1988). These samples were grown on n^--Si substrates for junction isolation. Experimental details on 2DHG structures are given below.

2.3.3a STRUCTURE DESIGN

The major requirements to achieve high 2DHG mobilities are abrupt heterointerfaces between Si and SiGe negligible interface charge and no impurity or dopant contamination in the electrically active region. Beyond these, an effective remote doping mechanism has to be provided with the considerations of a suitable band offset, dopant concentration and spacer width. To provide commensurate growth it is also important to consider for a given Ge concentration, the maximum SiGe channel width and growth temperature along with diffusion and segregation effects. The structures to study growth aspects and electrical transport properties of 2DHG(s) in the

SiGe/Si system may be of three types, namely symmetrical, inverted or normal (Fig. 2.7). The symmetrical type in which 2DHGs formed at both junctions was first studied showed good carrier confinement and low temperature mobilities (People *et al.*, 1984). However two different superimposed oscillation periods in this study suggested different two dimensional hole densities at each heterointerface. Similar structures grown by UHV-CVD and RT-CVD provided apparently similar interface quality between Si/SiGe and SiGe/Si heterointerfaces (Wang *et al.*, 1989a; Wang *et al.*, 1989b; Venkataraman *et al.*, 1991). Further investigations on MBE grown single heterostructures (normal and inverted types in which a 2DHG formed at the upper and lower heterojunction respectively) by SIMS indicated surface segregation of boron in inverted structure resulting in different carrier mobilities (Mishima *et al.*, 1990). To avoid these problems, the present study employed normal structures (see Fig. 2.7).

2.3.3b STRUCTURE GROWTH

All the structures for this research were grown in a computer controlled VG V90S Si/MBE machine, fitted with a 180cc (AP & T) electron beam evaporator for silicon, a 40cc (Edwards Temescal) electron beam evaporator for Ge, and a special graphite element substrate heater. All sources have shutters located above them so that deposition may be commenced and terminated in <0.5 s. Commercial substrates used in the study were 3" or mostly 4" in diameter, cut and polished in the (100) direction. Total growth rates of between 0.1 and 0.3 nm s^{-1} were controlled using an Inficon Sentinel

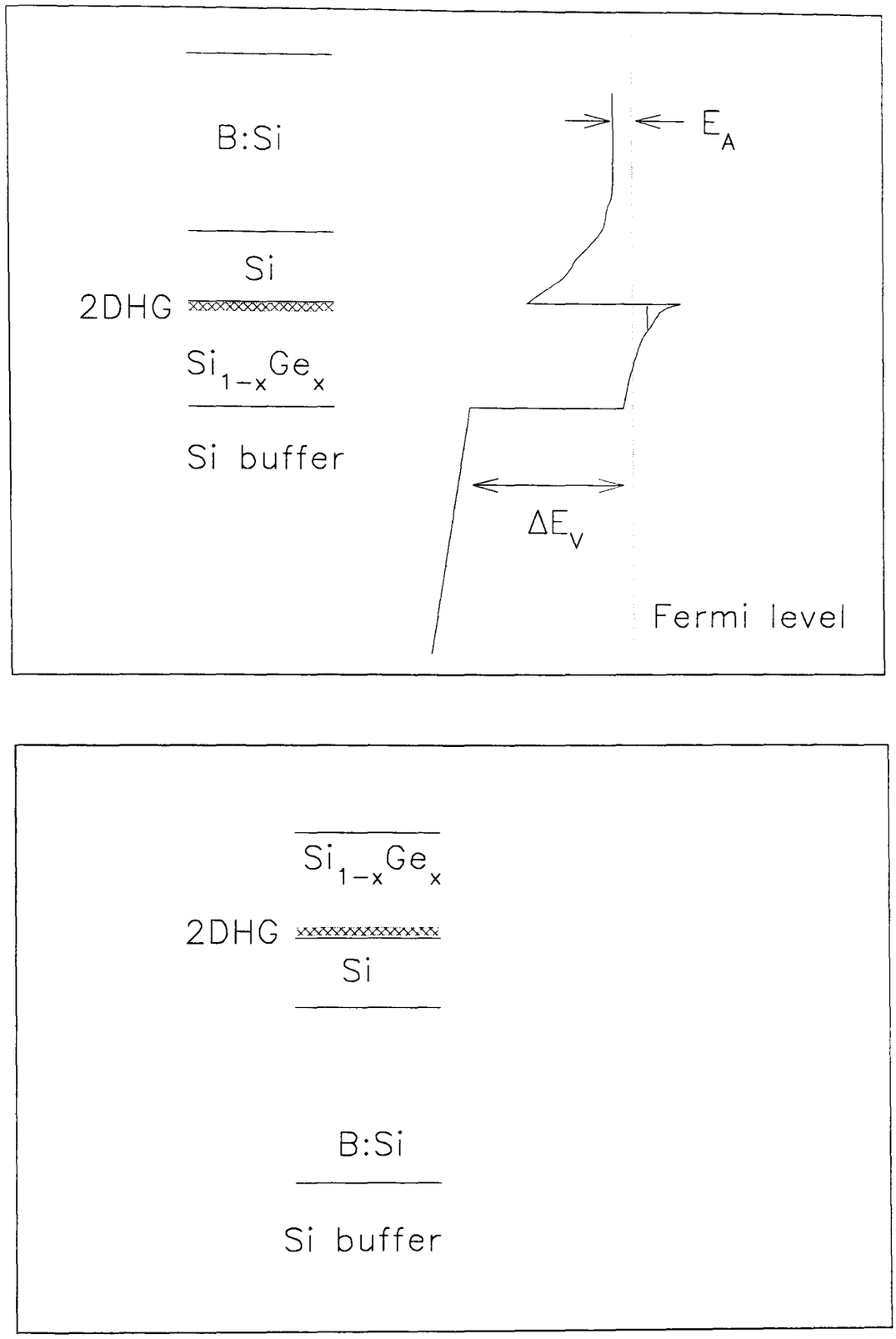

Fig. 2.7. Normal 2DHG structure and its schematic band alignment (upper part), Inverted 2DHG structure (lower part).

III system (Kubiak *et al.*, 1991). Elemental boron doping was achieved using an in-house designed source. Substrate temperatures between 550 and 950° C were monitored using an Ircon pyrometer and the reproducibility between growth runs was better than ±10°C. After machining to shape, all source materials were degreased, and subjected to a CP4A etch to remove gross contamination and then a full RCA cleaning procedure just prior to insertion into the copper electron beam evaporator hearths.

The studies were carried out on single quantum well SiGe/Si structures grown on 0.1 to 0.4 μm thick buffer layers on n^- (100) substrates. Elemental boron doping of the cap layer at a concentration of 1-5x10^{18} cm^{-3} was initiated 20 to 60 nm after completing the alloy layer growth, thus forming a spacer layer and producing a 2DHG at the upper Si/SiGe interface, (i.e. a 'normal' structure). The Ge concentrations in the alloy were in the range 5 to 20% and alloy thicknesses were between 30-74 nm. An exception to this specification was sample #33/56 where the spacer layer was ~63 nm (producing a correspondingly lower 2DHG sheet density). The equilibrium critical thickness according to Matthew and Blakeslee (1974) for these structures is in the range 20 to 70 nm so that all of the layers were close to or in the equilibrium regime.

2.3.3c SAMPLE PREPARATION

By using a mask having 1 mm diameter holes, aluminium was sputtered on the corners of a square sample with a side length of 6-7 mm

(Magnetron sputterer, Ion Tech.). To form the ohmic contacts with the 2DHG, diffusion of Al was then carried out by annealing the samples under Oxygen free N_2 gas ambient for 3 min. Crosses, painted with black wax, were used as masks to define of Hall crosses. Samples were etched for 10 s (about 10 μm) in CP4A, an acidic mixture of HNO_3, CH_3COOH and HF in the ratio of 5:3:3 and the wax was then removed by xylene.

2.3.3d CRYOGENICS AND MEASUREMENTS

A continuous flow cryostat (CFC) was employed in this study providing a measurement temperature range of 3.4 - 300 K. Cooling was achieved by using liquid ^4He with a pumping facility. This Oxford instrument cryostat uses a RhFe thermocouple as sensor for an Oxford ITC4 temperature controller. Magnetic fields of $\leq$0.51 T in strength were provided by a water-cooled electro-magnet. Schematic of the flow diagram for temperature measurements is shown in Fig. 2.8. A Si diode thermometer, calibrated in the range 1.5 - 300 K with an uncertainty of $\pm$30 mK, was used in constant current mode for temperature measurements (thermometer was supplied and calibrated by Institute of Cryogenics, Southampton University). Low temperature Hall measurements down to 3.4 K were carried out on cross-shaped samples using the van der Pauw (1958) methodology. 'f' factor is employed to examine the symmetry of samples for each measurement and any data with 'f' < 0.95 are omitted. Hall mobilities and sheet hole densities of the present 2DHG structures are reported in chapter 5.

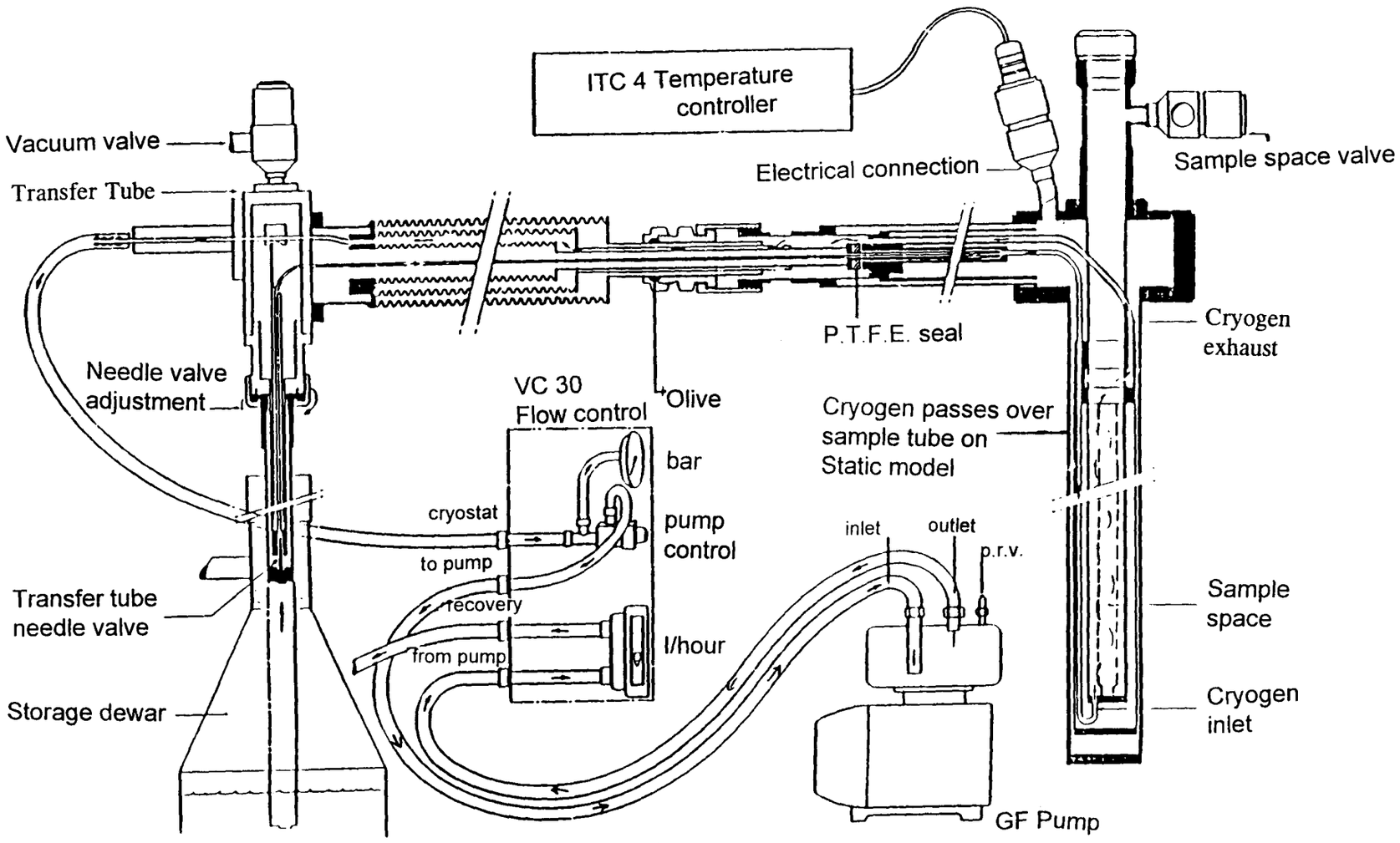

Fig.2.8. The schematic flow diagram for Hall measurements.

2.4 COMPARATIVE TECHNIQUES

2.4.1 SECONDARY ION MASS SPECTROSCOPY

In this technique the sample surface is bombarded under UHV conditions by an energetic beam of primary ions in the range of 500 eV to 30 keV. This causes sputtering of the particles from the sample surface as well as incorporation of the incident ions. Some of the sputtered particles are in the form of secondary ions which are extracted into mass spectrometer and separated according to their mass to charge ratio. Primary ions raster the sample surface in a very controlled way causing a crater the size of which is generally in the range 5x5 μm^2 to 500x500 μm^2. The counts of one or more mass peaks as a function of bombardment time are monitored. In order to obtain a dopant concentration-depth profile, counts are converted into concentration by running standards (usually ion implanted material) and, erosion time is converted into depth after measuring the crater with a surface profilemeter by assuming a constant erosion rate. A full description of SIMS and its applications can be found in the book by Benninghoven *et al.* (1987).

With respect to the Sigmund's cascade theory, the most successful explanation of the primary-target interactions, the primary ion shares its energy with target atoms. When the primary ion collides the target, a series of binary collisions create fast recoils. A collision cascade is developed until the transferable energies become less than the displacement energy and the primary ions comes to rest in the target host lattice resulting in ion implantation. The life time of the cascade is about 10^{-12} s and its dimensions are of the order of 10 nm (Clegg, 1990). The most striking feature of the

primary-target interactions are that the target atoms are intermixed in the region of penetration depth of the primary ion. These effects are responsible for the broadening of the depth profile of ultra-thin layers (see section 3.5) and may be minimised by employing low beam energies and oblique bombardment.

For high sensitivity, oxygen and caesium beams are employed. This causes the formation of an oxidised layer in the near surface region. Oxygen primary ion beam bombardment of Si results in an altered layer with a composition of SiO_x, where x depends on analysis conditions (Augustus *et al.*, 1988). 20 nm thick altered layer for 4 keV normal incident O_2^+ bombardment suggests that some of the implanted oxygen diffuses deeper into target since it is thicker than expected from ion implantation theory.

SIMS profiles were measured in either the Cameca IMS 4f machine at Cascade Scientific (Uxbridge) or the EVA 2000 machine at Warwick. The latter was fitted with a high linearity programmable beam scanning system to eliminate macrotopography effects. The investigations were carried out using $^{16}O_2^+$ primary ions, at different energies and incident angles as given in the text. Ion implanted boron standards in Si were used to calibrate SIMS profiles. Because boron standards in $Si_{1-x}Ge_x$ are not yet available, boron in Si implants were employed to calibrate doping levels in $Si_{1-x}Ge_x$, the validity of which is discussed in chapter four. The sputter rates were established by measuring all SIMS craters with a surface profilemeter (Slone Dektak Auto II).

2.4.2 SPREADING RESISTANCE PROFILING

Spreading resistance profiling (SRP) is in principle a very simple method, which determines the spreading resistance between two probes. Two carefully aligned probes are stepped along the surface and, the resistance between the probes is measured at each location (ASTM Standard F672) such that eventually the spreading resistance profile as a function of depth is obtained. Before the measurements, the sample is bevelled by mounting on a bevel block with melted wax and typical bevel angles of 15' to 5° are employed. Technical details regarding the preparation of the samples can be found in ref. (Schroder, 1990). After early poor irreproducible results, the importance of the mechanical design, the quality of probe and substrate preparation problems were recognised and overcome. Thus the SRP method has been developed to give rapid and reliable results on a wide range of silicon samples, though only to a very limited extent on III-V materials where high contact resistance limits the carrier concentration range which can be profiled (Pawlik, 1987a). The depth resolution is determined by the step size of the probe tips, typically 1 to 2.5 μm, and the magnification provided by the bevel angles ranging from 2 to 35. Therefore a resolution of a few nanometers should be feasible.

Complex results arise since SRP not only measures the top layers but also everything which is underneath. Therefore elaborate correction factors based upon Laplace's equation are presently used routinely to deconvolute the experimental data (Schumann and Gardner, 1969). Furthermore, apparent peak position of junctions strongly depend on the probe weight and

on the actual probe conditioning (Pawlik, 1992). Nevertheless for the probes having the same nominal pressure, variations in junction depths were found for probe tips which were conditioned slightly differently. These effects cannot be explained by probe penetration which was shown to be very small (Vandervorst and Maes, 1984), but are related with the exact probe-semiconductor characteristics (Clarysse and Vandervorst, 1992).

Relationship between measured resistance and the resistivity of the semiconductor under investigation depends upon the homogeneity of the material. This relationship is (Pawlik, 1987a)

$$R_M = CF\frac{\rho}{2a(\rho)} + R_B(\rho) \qquad (2.26)$$

where R_M is the total measured resistance, ρ is the resistivity, R_B is a resistivity dependent barrier term and a is the effective probe radius. The correction factor, CF in homogeneous materials is unity and, its importance in inhomogeneous materials is discussed by Pawlik (1987b). The attractiveness of SRP is that it provides unchallenged sensitivity (down to 10^{11} level) for every dopant which is electrically active. For samples containing *p-n* or high-low junctions, additional corrections are required. In application of very shallow profiles, SRP always produces junction depths shallower than SIMS and ECV. Multilayer corrections have evolved over the years and today very sophisticated correction schemes are used (for example see, Vandervorst and Maes, 1984; Schumann and Gardner, 1969; Choo*et al.*, 1978; Berkowitz and Lux, 1981; Piessens *et al.*, 1983; Choo *et al.*, 1983; Pawlik, 1986b).

Discrepancies can be understood in terms of the concept of carrier spilling. The latter refers to the redistribution of mobile carriers away from the steep dopant distributions (Hu, 1982). As a consequence the spreading resistance measured reflects the redistributed carrier profile and not the dopant profile. Since carrier concentrations in SR profiles are extracted from resistivity data, some assumptions must be made about carrier mobilities. Furthermore because the carriers are partially separated from their parent donor atoms when carrier spilling occurs, their mobilities may be significantly changed. Therefore carrier spilling effects dominating SR profiles and are therefore the principle limitation in thin structures. The SR profiles used in this work were obtained by M. Pawlik at Semiconductor Assessment Services Ltd.

2.4.3 CROSS-SECTIONAL TRANSMISSION ELECTRON MICROSCOPY

Transmission electron microscopy (TEM) has played an important role for many years in materials research and recently in the study of thin film multilayered structures such as those encountered on integrated circuits (Sheng, 1988). It provides a direct way of imaging defects in Si layers. In the TEM, high-energy electrons are accelerated to potentials of between 100 and 2000 kV and are focused by magnetic condenser lenses to form a spot from 0.1 to 100 μm in diameter (Pawlik, 1988). If there is any deviation in atomic positions, diffraction will occur and image contrast will result. For example Kasper *et al.* (1985) used the TEM to examine Si/Ge superlattice growth. The usefulness of TEM as an analytical tool for layered structures resulted

largely from the development of the technique for preparing cross sections of samples. In the past several years, a great deal of cross-sectional TEM (XTEM) work has been reported on the direct observation of buried features in semiconductor multilayer structures. The major obstacle to applying XTEM to Si device analysis has been sample preparation which, is nevertheless easier compared to III-V devices, and overcome by using an epoxy-embedding technique combined with large-area ion milling (Sheng and Chang, 1976). It is more time-consuming and expensive than other analytical techniques (Auger, SIMS, RBS, etc.) and considerable development and refinements of preparation techniques will occur. However, XTEM observations of structures offer excellent lateral and depth resolution not available by other techniques. The XTEM technique has helped us determine the exact geometry, physical state, interface characterisation and *p-n* junctions localisation, etc., of important structures. This has allowed extensive studies including MBE grown samples providing invaluable information for example relaxation study of SiGe thin films (LeGoues *et al.*, 1992) and strained layer GeSi/Si *p-n* junction diodes (Ross *et al.*, 1992). Because of the continued demand for better reliability and the need to monitor processes and inspection procedures, XTEM has become an indispensable analytical technique.

2.4.4 X-RAY DIFFRACTION

Double crystal diffraction allows the epitaxial layer to be compared to the substrate and hence its plane spacings can be obtained. Since the plane

spacings of Si are known, the true structure of the epitaxial layer can be found. This non-destructive technique provides very high resolution with easy sample preparation. At Warwick, double crystal x-ray diffraction method is routinely used to calibrate the Si and Ge rate in Si/GeSi superlattices. Detailed information may be found in the work of Powell (1992).

2.4.5 DEFECT ETCHING

Preferential etching is a simple and fast evaluation technique to explore the structural perfection of a single crystal. This technique is widely used for Si crystals to delineate process-induced defects which are inherent to the all growth methods although they are at low levels for epitaxial techniques. The effect of MBE growth conditions on defect levels and on the nature of defects has been discussed by Pindoria *et al.* (1990).

There are several preferential etches currently available for Si crystals (for example: Hu, 1977; Jenkins, 1977; Schimmel, 1979; Yang, 1984). The sample under investigation is immersed in the etchant to dissolve the material at a controlled rate. Defects and impurities are preferentially etched defining contours on the surface.

In this work, the dilute Schimmel etch (1.5 H_2O: 1 CrO_3 (0.75 M): 2 HF) was employed to dissolve boron doped Si and Ge_xSi_{1-x} layers at a controlled rate. Defect levels were quantified by counting the number of defects under an optical microscope and their areal density was determined.

It is important to note that for thin layers, the process of identification becomes difficult and hence defect count can be in error.

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CHAPTER THREE

BORON DEPTH PROFILING IN Si

3.1 INTRODUCTION

This chapter focuses on the determination of the free carrier distributions in Si MBE materials as measured using a commercial ECV profiler (PN4300). Assessment of the ECV profiles was carried out by comparison with SIMS, Hall measurements, conventional CV and SR profiles. The main advantage of the ECV over static CV is that the restriction of the electrical breakdown to the maximum profilable depth can be overcome by replacing metal of a Schottky barrier with a convenient electrolyte which additionally provides controllable etching of the semiconductor sample (see chapter 2).

The electrochemical CV technique for determining the carrier concentration was first proposed by T. Ambridge and co-workers (Ambridge *et al.*, 1973 and, Ambridge and Faktor, 1974) and, an automatic carrier concentration profile plotter was described (Ambridge and Faktor, 1975) for characterisation of *n*-type gallium arsenide. The demand for such a method

was due to the shortcomings of the established techniques for the measurement of the electrical properties of grown layers which suffer from important practical limitations as discussed in chapter 2. The technique was also applied to InP, where difficulties in forming high-quality metal Schottky contacts had been encountered (Ambridge and Ashen, 1979). Further development followed for the case of InP by utilising a more convenient electrolyte and improved sample mounting techniques (Green *et al.*, 1986).

The capability of ECV has already been adequately demonstrated for the III-V materials (Blood, 1986). However, profiling of Si is more difficult due to the problem of hydrogen (H_2) bubble evolution at the semiconductor surface during anodic dissolution, poorer understanding of the etch chemistry and of the conditions needed for optimal measurements. Reported results for profiling Si (see for example Sharpe and Lilley, 1980) usually concentrated on comparison with either the intended schedule or that obtained by SR profiles, which in many respects, is as poorly developed as ECV (see section 2.7.2). This has led to a neglect of using ECV for Si-based structures. For example, Sieber and Wulf (1991) concluded that the ECV technique is *not* able to estimate the carrier concentration above 10^{19} cm^{-3} because of the discrepancy of the maximum doping values between ECV and SR curves they observed. By comparison, Mogul *et al.*, (1992) reported profiling of heavily Ga^+ implanted Si, showing that ECV provided significantly *better* agreement with SIMS profiles than did SR.

It is the purpose of this work to clarify the capability of ECV in the field of Si-based materials particularly by recourse to the complex doping

structures that can be realised by MBE. In this chapter, the author first makes a comparison between a SIMS profile and ECV profiles for various electrolytes using a boron-doped staircase test structure and then reports the first systematic study of ECV profiling of boron doped Si at doping levels in the range of $1x10^{19}$ to $3x10^{20}$ cm^{-3}, and assess the accuracy of the technique by comparison with Hall measurements and SIMS profiles. Furthermore ECV profiling of ultra thin layers down to delta doping spikes is reported for the first time.

3.2 PREVIOUS WORK

Three different etches have been employed and are used in this study. They are designated E1, E2 and E3 in this thesis, and their constitution is given in Table 3.1.

Abbreviation	Electrolyte	reference
E1	0.1 M $NH_4F.HF$	BioRad, 1989
E2	1M/0.05 M NaF/H_2SO_4	Sharpe *et al.*, 1979 Leong *et al.*, 1985
E3	0.1 M/0.25 M NaF/Na_2SO_4 (with a pH of 4.7 by adding 2M H_2SO_4)	Horányi and Tüttö, 1993

Table 3.1. Electrolytes used for ECV profiling with symbols called in this thesis.

As discussed in section 2.2, 3.1 and 4.3 successful applications of ECV depends on availability of a convenient electrolyte for a particular semiconductor material. It has long been recognised that a number of reactions can be involved in the electrochemical dissolution of Si depending on anodic potential applied. It has been reported that the effective valence z (number of electronic charges transferred per atom of Si dissolved) may vary in the range 2 to 4 where a porous silicon film was formed by anodic reaction in aqueous hydrofluoric acid (HF) (Arita, 1978). The dependence of this valence number on HF concentration, carrier concentration of semiconductor, electrode potential and illumination was shown. This indicates that in electrochemical profiling, effective dissolution valence number must be determined for a given electrolyte-Si interface and be as reproducible as possible since it determines the accuracy of the depth scale (see section 2.2).

Sharpe *et al.*, (1979) first applied the ECV technique to thick (15 μm) epitaxial staircase structures with doping levels in the range of about $1x10^{15}$ to $5x10^{18}$ cm^{-3}. They employed NaF/H_2SO_4 electrolyte in aqueous solution with a composition of 1M/0.05M and a pH ~5 (E2). A smooth uniform dissolution at a potential of approximately 2.5V more anodic than the dark rest potential resulted in about 4 mA cm^{-2} on illuminated *n*-Si whilst employing a simple electrolyte agitation device to preclude the retention of gas bubbles at the Si electrode. For this electrolyte-Si system, the dissolution valence was found to be in the range 3.3 to 3.8. The measurement potential used was 1.5 V more anodic than the dark rest potential on *n*-Si and about 0.2 V more cathodic for *p*-Si, these conditions giving the best agreement

between ECV and SR profiles. Sharpe and Lilley (1980) delineated the effect of increasing fluoride content on the *I-V* characteristics of *p*-type Si-NaF/H_2SO_4 system. As expected, illumination of the *p*-type electrode caused virtually no change in current but for low doped *n*-type Si caused a large increase in current. They noticed that the behaviour of highly doped *n*-type Si was characterised by a large dark current. They also observed that gas evolution at both *n*- and *p*-type Si electrodes under anodic bias reached a maximum at or near the current peak and diminished at higher voltage but continued at a slow rate even at 2V overpotential (Sharpe and Lilley, 1980). In the case of highly doped *n*-type Si, carrier concentration doping level of ECV profile was slightly lower than obtained by SR in contrast to the situation at low doping levels. Ambridge and Faktor (1974) also noted a difference between ECV and SR profiles on low doped GaAs but they attributed the difference to the presence of deep levels.

Routine use of the ECV profiling technique for the characterisation of both *p*- and *n*-type Si-MBE materials was reported by Leong *et al.*, (1985). Provided carefully selected profiling parameters were chosen, acceptable agreement between ECV and SR profiles were obtained in the range of $1x10^{15}$ to $1x10^{19}$ cm^{-3}, using the NaF/H_2SO_4 electrolyte-Si system. They also observed that whenever effective dissolution valence number falls below 3.5, the resultant etch surface became badly pitted and covered with a brown deposit. In both *n*- and *p*-type Si materials, an etch voltage of 4 V introduced no effect on z but in the case of less than 1 V the surface is generally left covered with a layer of brown deposit affecting the subsequent carrier concentration measurement. They studied dilution of the electrolyte to avoid

the formation of brown deposit. Highly diluted electrolytes lead to an improvement in the uniformity with a cost of decrease in the dissolution rate which limits the practical use of the technique. They also showed the dependence of the dissolution number z of *n*-Si in the electrolyte on the dilution factor and illumination level under an anodic potential of 2 V. They found no effect of dilution of the electrolyte on carrier concentration profiles. They also noted that at higher doping levels, the (dark) leakage current during the measurement increased rapidly giving erroneous results indicating the effect of leakage current on carrier concentration profiles. In another study of profiling Si, the capabilities and limitations of ECV and SR profiling techniques were compared with attention paid to samples grown by MBE incorporating sharp doping transitions with broad doping spikes (Pawlik*et al.*, 1987). For reliable ECV measurements, they found that the leakage current must be low for doping levels above 10^{18} cm^{-3}. They also concluded that the maximum carrier concentration level that could be realistically measured by ECV was 2-3x10^{19} cm^{-3}. Despite the agreement on the location of the doping spikes, doping levels were up to a factor of 4 lower. High noise level in the SR profile was attributed to heavily defected samples, although ECV profile seemed not to be affected.

In a comparison between SIMS and ECV depth profiles of MBE-grown doped Si layers, the emphasis was put on technical aspects rather than on the physical interpretation of the results (Kechang *et al.*, 1990). They also reduced the concentration of the electrolyte (E2) by the dilution factor (Df) to control the dissolution speed and therefore the resolution of etch thickness. They found that z varies inversely with the dilution factor, and observed

variations in the etch depth W_r of the order of 10% in the range 3.5<Df<2. In contrast no dependency was observed on Df for 1.5<Df<2.5 over the doping level range 10^{15} - 10^{19} cm^{-3}. Carrier and modulation frequencies were 1 kHz and 40 Hz respectively and an etching potential of 3 - 4 V. It was also emphasised that the V_{meas} had to be checked and changed during the profile to retain optimum measurement/etch conditions.

Implanted and homogeneously low doped Si samples were investigated to deal with the problems arising from the technique and from the imperfections of the investigated materials (Sieber and Wulf, 1991). They observed considerable difference between SR and ECV profiles particularly in the vicinity of high doping gradients. They also added a small quantity of dodecylamin ($C_{12}H_{25}$-NH_2) to the ammonium bifluoride solution to avoid the influence of the bubbles generated by the anodic dissolution process (Sieber *et al.*, 1991). Effective valence numbers of 2.3, 2.7 and 2.4 were obtained for a structure containing epitaxial *n*-Si, Sb-implanted layer and bulk *n*-Si respectively. The study involved doping levels between $1x10^{16}$ and $1x10^{18}$ cm^{-3} and resulted in agreement in doping levels (within ~50%) between ECV and SIMS profiles. Using a contact area of 0.0025 cm^2 with the profiler PN4300, Ga implanted Si samples at various doses were used to compare ECV with SR (Mogul *et al.*, 1992). While ECV matched reasonably well the Ga atomic concentration obtained by SIMS, SR indicated almost an order of magnitude lower doping levels. ECV was also superior in its ability to profile shallow structures.

Tuppen *et al.*, (1987) studied an additional feature of the electrochemical technique namely defect revealing in Si-MBE materials. By using the standard Polaron semiconductor profiler (PN4200) and employing 0.1M solution of $NH_4F.HF$, they compared the sample surfaces after etching using the ECV and after using a standard Schimmel etch (Ota, 1983). Optimum conditions for revealing defects in the Si specimen were found to occur at a cell current density of 1.5 $mAcm^{-2}$, compared with typical profiling conditions used (~5 $mAcm^{-2}$) which yield non-defect revealed surfaces. The dissolution of Si was varied under different chemical reactions depending on applied potential. Therefore using a suitable combination of the high voltage non-revealing etch provided the removal of porous Si formed, and the low voltage revealing etch mode, it was possible to measure defect densities at various depths into the material to provide a defect (etch pit) profile.

3.3 BORON STAIRCASE IN SILICON

One of the routine uses of the ECV at Warwick is to provide rapid calibration of doping levels in the MBE system. To calibrate dopant sources (boron and antimony for *p*- and *n*-type doping respectively), ECV provides an inexpensive and rapid depth profiling which is conveniently carried out on 'staircase' type test structure. In this way, typically four different doping levels can be evaluated from the same structure. A SIMS profile of a typical boron staircase in Si (#32/4) grown on p^{++} substrate was obtained using normal incidence 11 keV O_2^+ primary ions is shown in Fig. 3.1. As is explained below, the ECV profiles resulted in good agreement with the SIMS except the

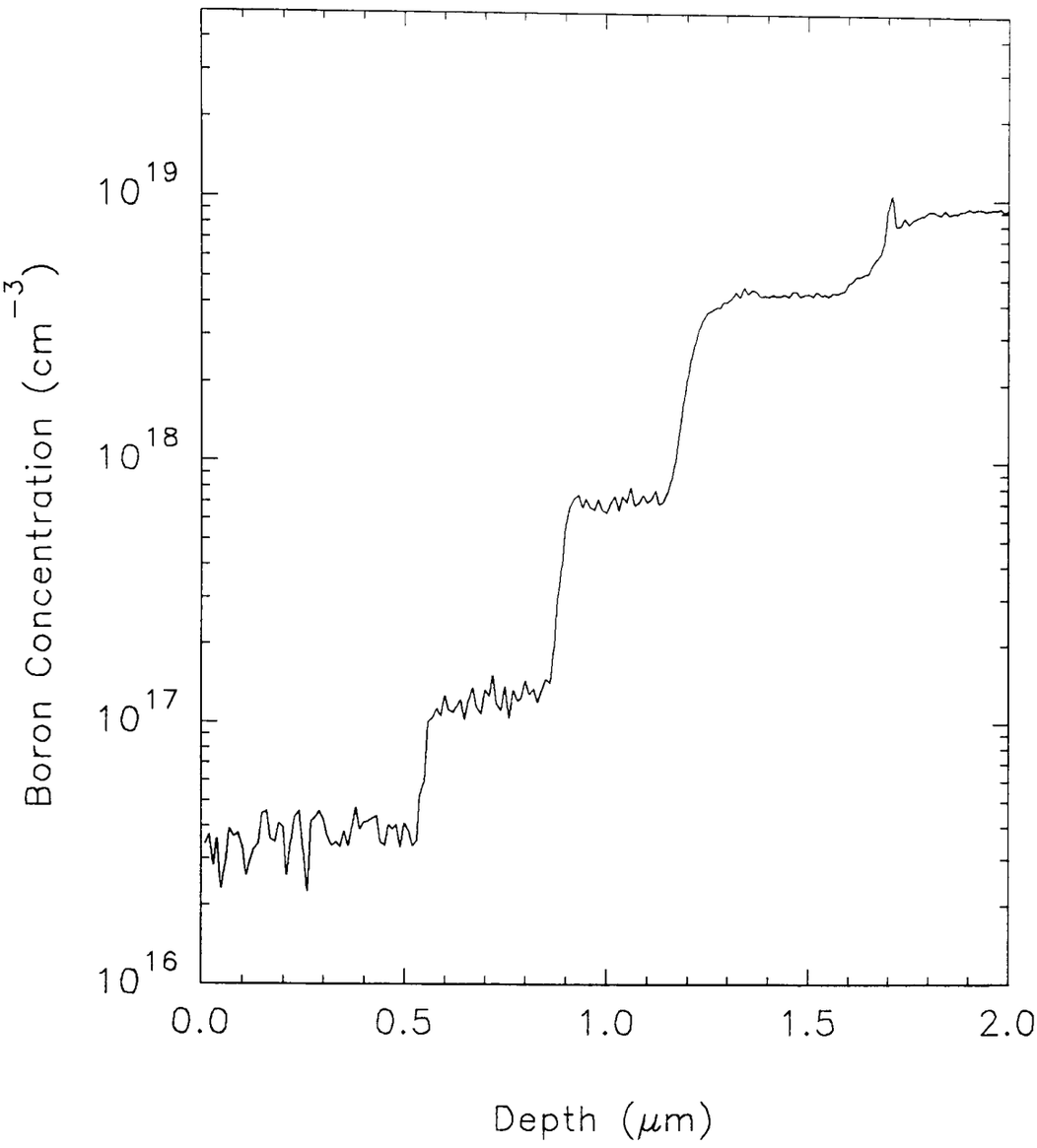

Fig. 3.1. SIMS depth profile of a boron staircase in Si grown by MBE (#32/4).

doping level of the first (nearest surface) step. Although the detection limit of the SIMS instrument for boron in Si is generally about $1x10^{16}$ cm^{-3}, the noise of the first doping level suggests that for this profile, the true boron concentration may be lower than indicated by the SIMS profile. Conventional CV measurements provided a third comparison for this doping level. As indicated in Fig. 3.2, the doping level of about $2x10^{16}$ cm^{-3} obtained by CV is in good agreement with the ECV result (see below - Figs. 3.4 a,b,c). Good uniformity of the substrates allows us to employ this as a fifth step to provide a check of lateral uniformity across the wafers. This was below the ECV measurement errors encountered here. In order to optimise the parameters, the electrolytes given in the literature to profile Si were employed as outlined in section 3.2. It is pertinent to note that the growth temperature used for this structure was 700°C, where previous work had indicated complete electrical activity for the doping level used (Parry *et al.*, 1991).

Before embarking on an ECV etch profile, it is important to establish the *I-V* behaviour of the contact to confirm satisfactory Schottky behaviour. Fig. 3.3a depicts the behaviour of the static *I-V* of the structure using the electrolytes E1 and E2 given in the Table 3.1 at ~0.4 μm into the first step. This behaviour is typical. The inset is an enlargement of the voltage range from -2 to 0V. Under reverse bias, no leakage current was observed for electrolyte E2 (although not the limit at this doping level for this electrolyte) but E1 shows leaky behaviour above -1.5 V. Similar *I-V* characteristics were observed for the second and third steps. From these *I-V* analyses, one may conclude that the measurement voltage range is more restrictive for electrolyte E1 than for E2, but both provide sufficiently large range from which

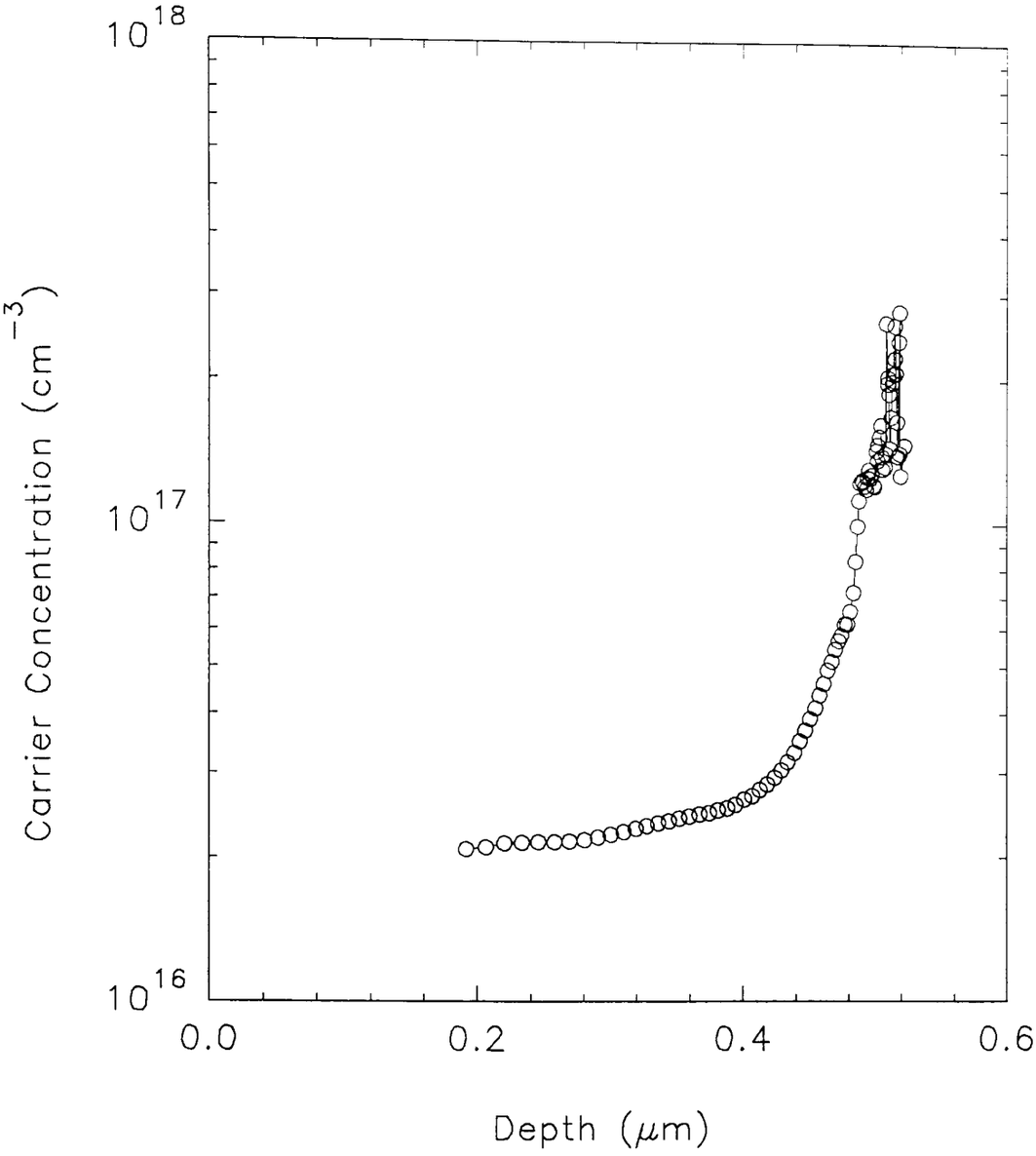

Fig. 3.2. Conventional CV profile of the first step of the boron staircase (#32/4).

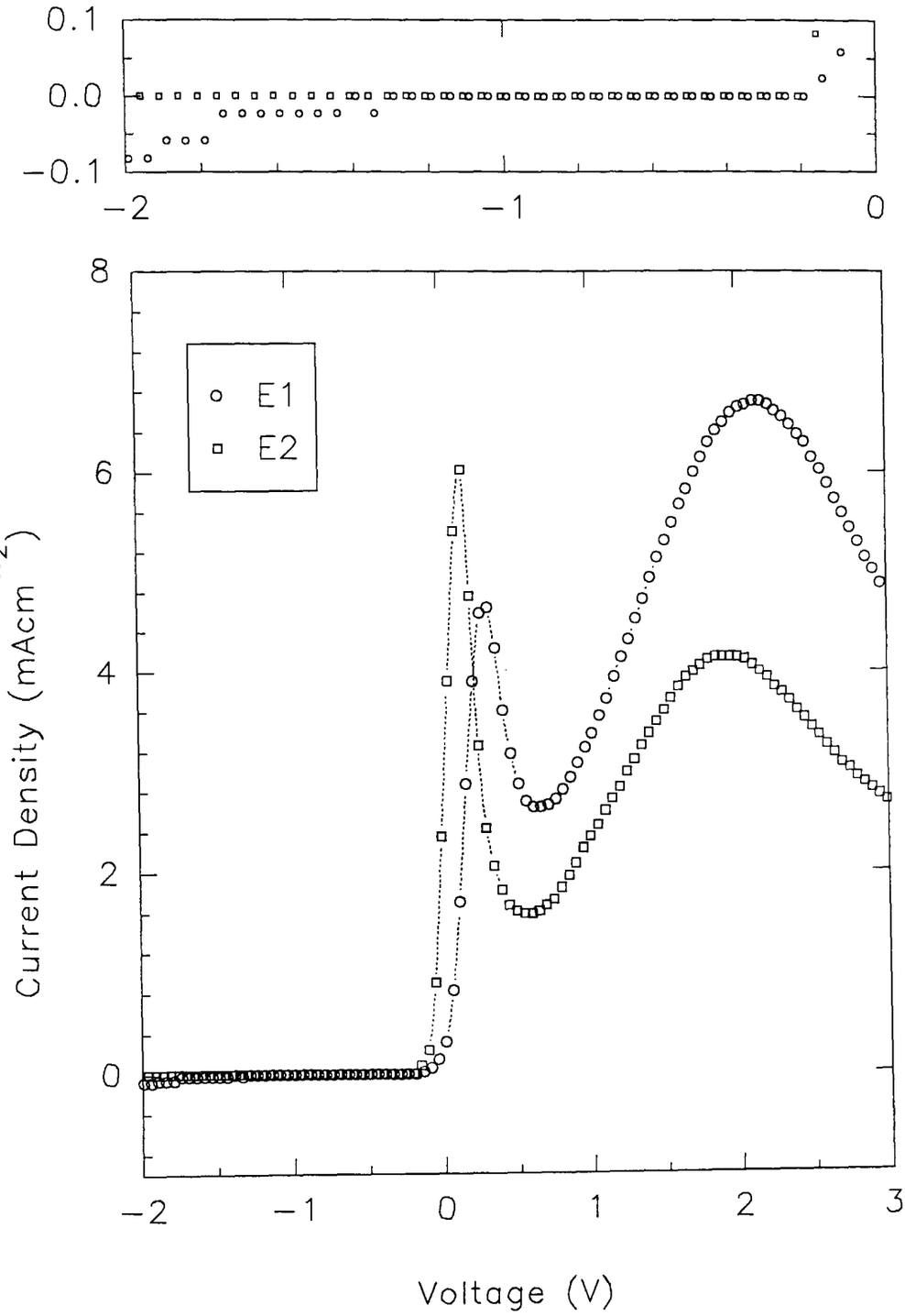

Fig. 3.3a. I–V behaviour of the staircase sample at 0.4μm for electrolytes E1, E2.

to choose. Using electrolyte E2, the *I-V* behaviours are compared at the first and fourth steps between -2 V and 0 V in Fig. 3.3b. For the fourth step, leakage current appears from about -0.8 V for this electrolyte (and from about -0.7 V for electrolyte E1).

From the above, it may be concluded that E2 provides a wider measurement bias range. For a staircase with a range of doping levels, a measurement bias in the range -0.3 to -0.9 V would provide the most appropriate condition. Figs. 3.4 a,b,c show complete profiles obtained with E2, under different conditions. One criterion to use as to the 'quality' of a profile is an agreement between the carrier concentration profiles obtained using the series and parallel models (see chapter 2), since this indicates that Rs and Rp are sufficiently small and large respectively as to have negligible effect. In Fig. 3.4a carrier concentration depth profile of the structure is given with a measurement voltage of -0.3V where discrepancy between the two models is evident. The discrepancy between the two models was worse with a measurement voltage of -0.2V; nevertheless better agreement with SIMS profile was observed from the series model at the highest doping level and from the parallel model at the lowest doping level at -0.2 V. From -0.4V to -0.9V, the two models matched each other well as observed in Fig. 3.4b where the measurement voltage was -0.5V. The profiling conditions employed for the profile in Fig. 3.4b are summarised in Table 3.2.

Meas. voltage	Etch voltage	Etch steps	Light	settling time	pump
-0.5V	2V	20 nm	off	10 s	on

Table 3.2. The profiling conditions for the Fig. 3.4b.

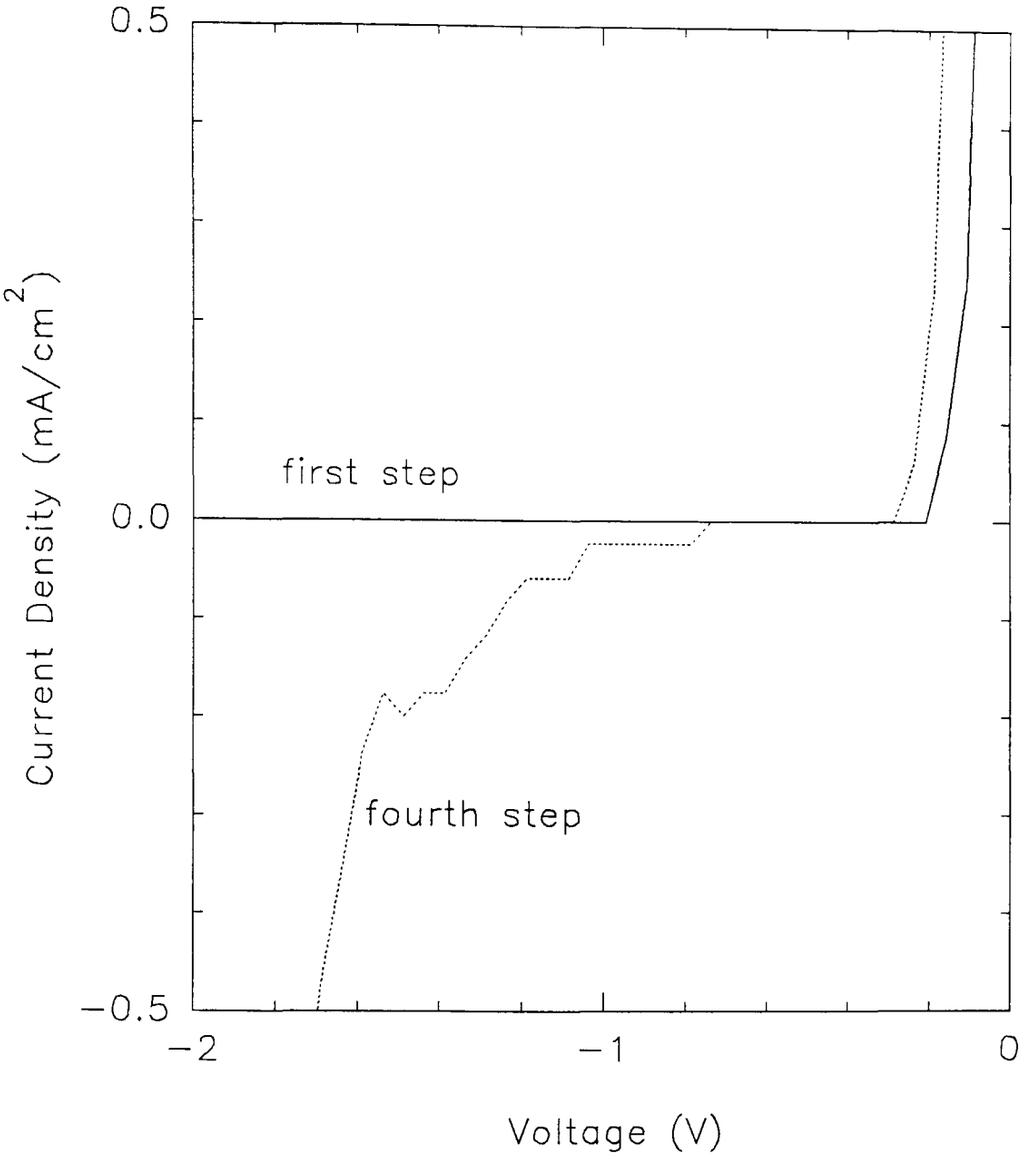

Fig.3.3b. I–V behaviour of the staircase sample at the first and fourth steps using the electrolyte E2.

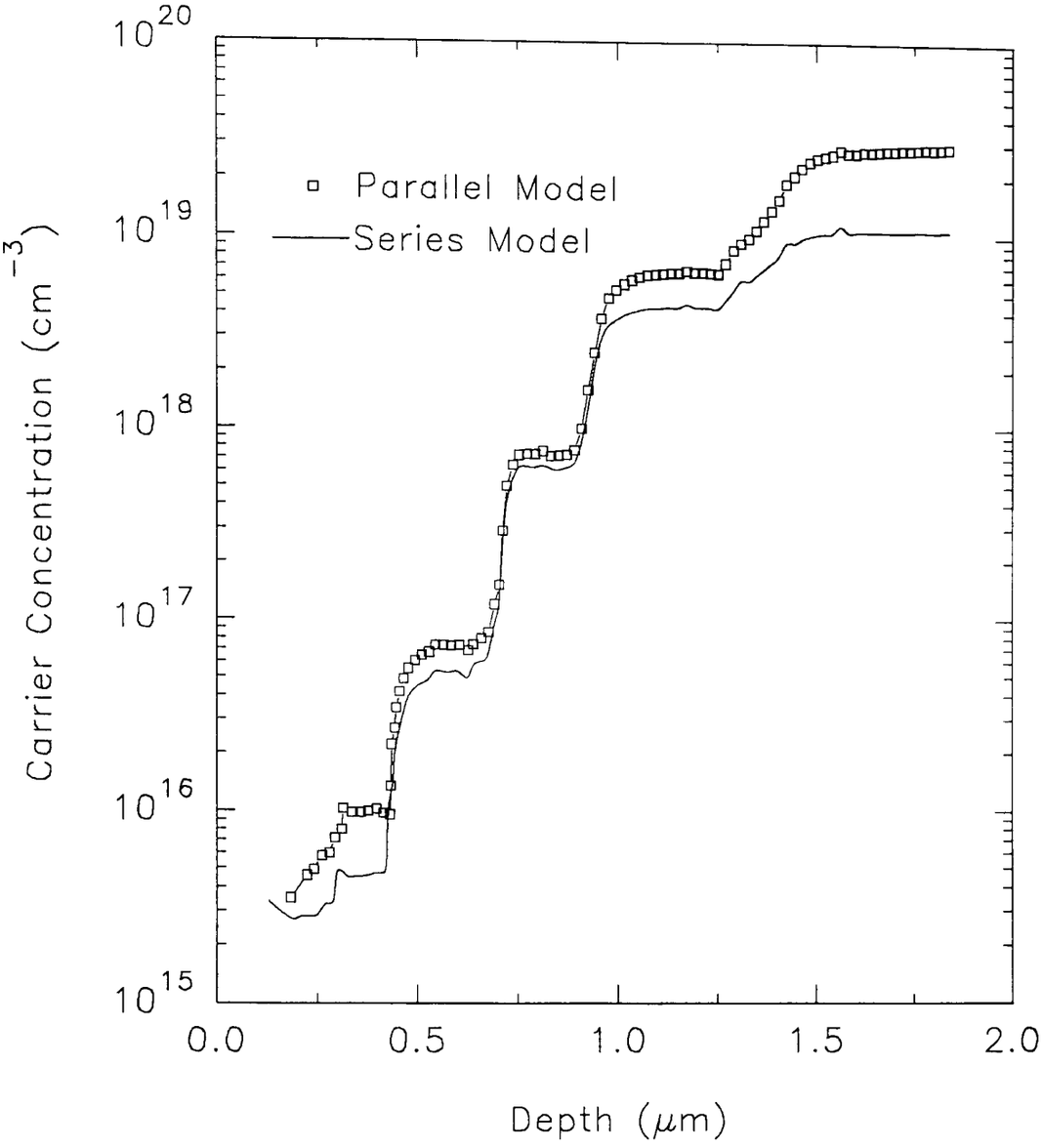

Fig. 3.4a. Carrier concentration–depth profile of the staircase using E2 and V_{meas}=−0.3V.

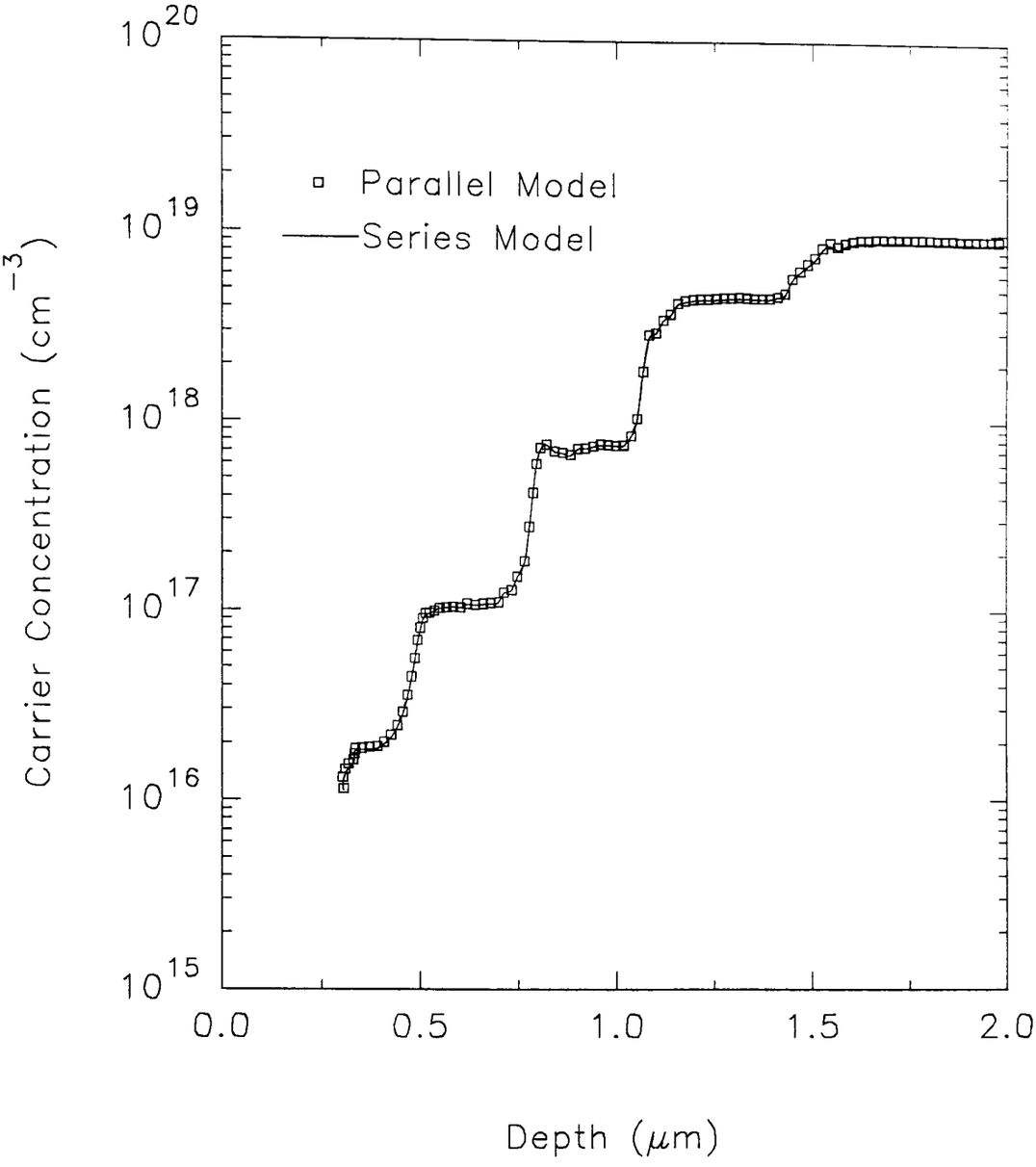

Fig. 3.4b. Carrier concentration–depth profile of the staircase using E2 and V_{meas}=−0.5V.

In the light of these analyses, any effects of measurement voltage on carrier concentration profiles were explored using the same conditions summarised in the Table 3.2 but changing the measurement voltage in the range -0.2 to -0.9V. In Fig. 3.4c, the same conditions were employed as in Fig. 3.4b but a small amount of a wetting agent Triton X-100 was added to the electrolyte to suppress bubble formation (instead of using the pump). However the doping levels appear to be affected by the wetting agent at higher doping level. This is the case particularly for the fourth step where doping level was lowered from ~4.5×10^{18} to ~2.5×10^{18} cm^{-3} with the use of wetting agent. Although leakage current was not detectable (<0.005 $mAcm^{-2}$), the dissipation factor rose with the wetting agent. It was increased to 0.24; three times higher than without wetting agent for the fourth step.

Another important parameter to examine along with leakage current is Flat Band Potential (FBP) behaviour (see chapter 2). Fig. 3.5 shows depth profiles of the staircase structure for FBP using both electrolytes and using profiling conditions in Table 3.2. When uniformly doped regions were profiled, FBP remained constant, an increase in doping corresponded to an increase in FBP which then returned to stabilised value. In the case of rather unreliable profiles, distortions and variations at uniformly doped regions in FBP were observed. The FBP could therefore be used as a figure of merit on the profile quality without having to stop profiling to perform *I-V* measurements.

Fig. 3.6 shows the quality of the Schottky barrier established between both electrolytes and the semiconductor under the same profiling conditions

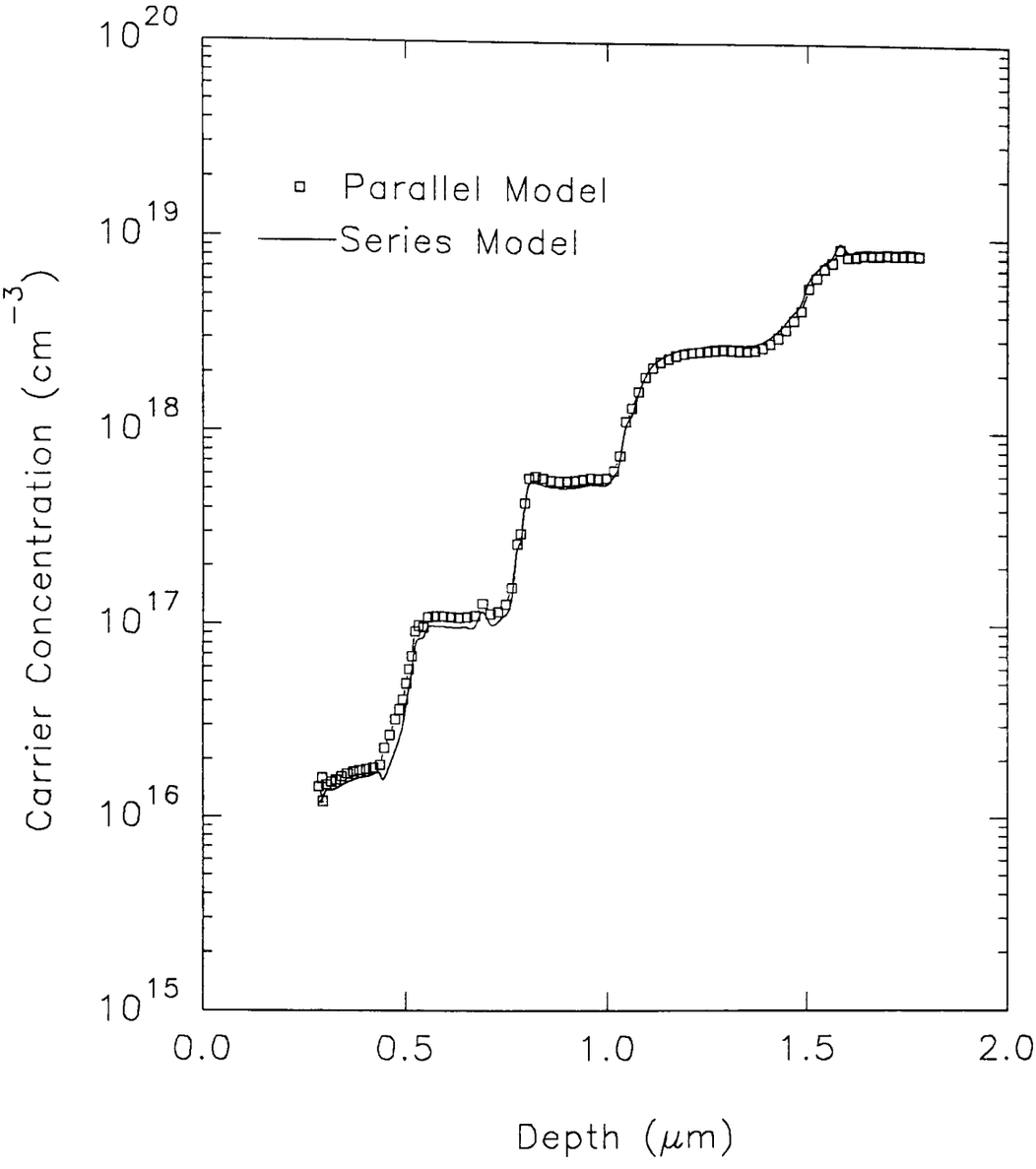

Fig. 3.4c. Carrier concentration–depth profile of the staicase using E2 with Triton X–100 and V_{meas}=–0.5V.

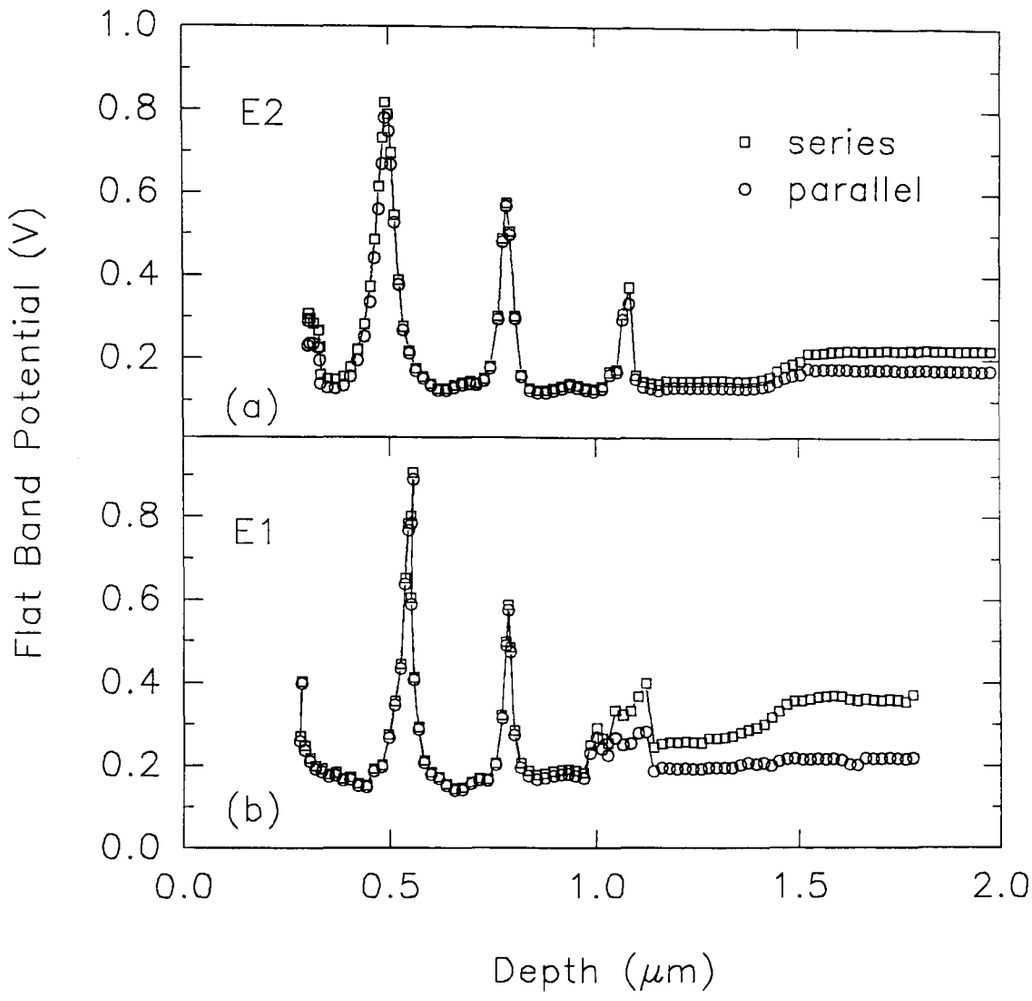

Fig. 3.5. FBP–depth profiles for both series and parallel models: (a) electrolyte E2 (see Fig. 3.4b) (b) electrolyte E1.

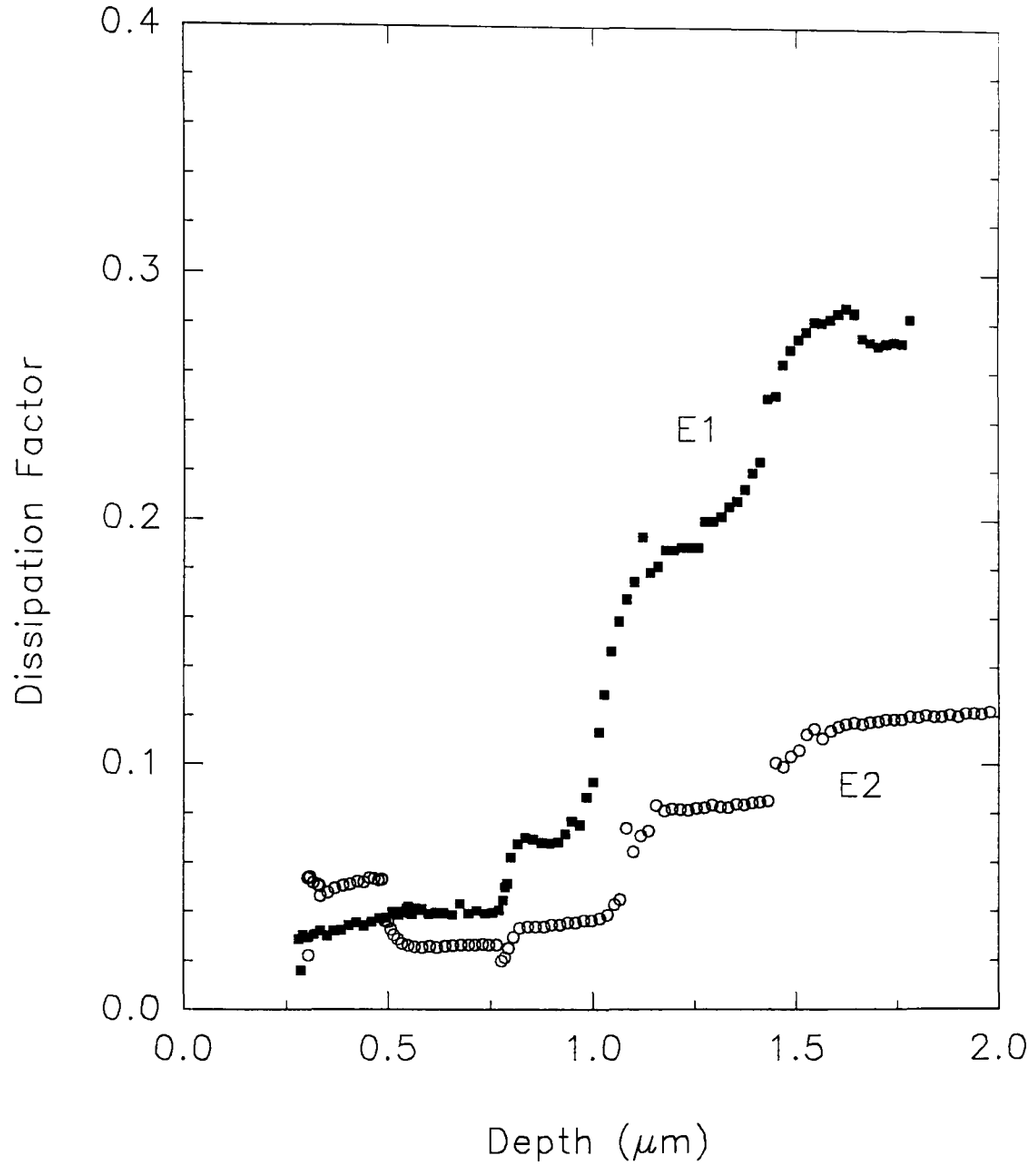

Fig. 3.6. Dissipation Factor–depth profiles for both electrolytes for the staircase structure obtained under the same conditions.

given in Table 3.2 as indicated by the dissipation factor. Both electrolytes provide sufficiently good Schottky behaviour at all doping levels, but a sharp increase in dissipation factor for electrolyte E1 at higher doping levels degrades the reliability of the results. This indicates that for doping levels higher than $1x10^{19}$ cm^{-3}, the electrolyte E1 may not be suitable to provide a satisfactory near-ideal Schottky barrier necessary for a reliable carrier concentration. In Fig. 3.7, the doping levels obtained as a function of measurement voltages by the ECV are shown, compared with the SIMS and conventional CV measurements for five doping levels in the epilayer and substrate. The figure also contains values obtained from electrolyte E1 at different measurement voltages of -0.3, -0.5 and -0.8V. This graph confirms reasonably good profiling by the ECV technique for a large measurement range for the doping levels between $2x10^{16}$ and $1x10^{19}$ cm^{-3} using both electrolytes, but indicates that E2 provides a more versatile range of conditions.

Electrolyte E3 (see Table 3.1) has been recently suggested as an alternative for electrochemical etching and profiling of Si (Horányi and Tüttö, 1993). Using a different electrochemical profiler (MCS-90 SEMILAB) they delineated the dependence of effective dissolution valence number on the dissolution potential, the pH of the electrolyte and the carrier concentration. They adjusted the pH of the electrolyte using 2 mol dm^{-3} concentration sulphuric acid solution. We have found that a few drops of sulphuric acid solution into 200 ml $NaF+Na_2SO_4$ affects the pH of the solution significantly. It has also been observed that the *measurable voltage range* with no leakage current was reduced compared with E1 and E2, restricting profiling to a very

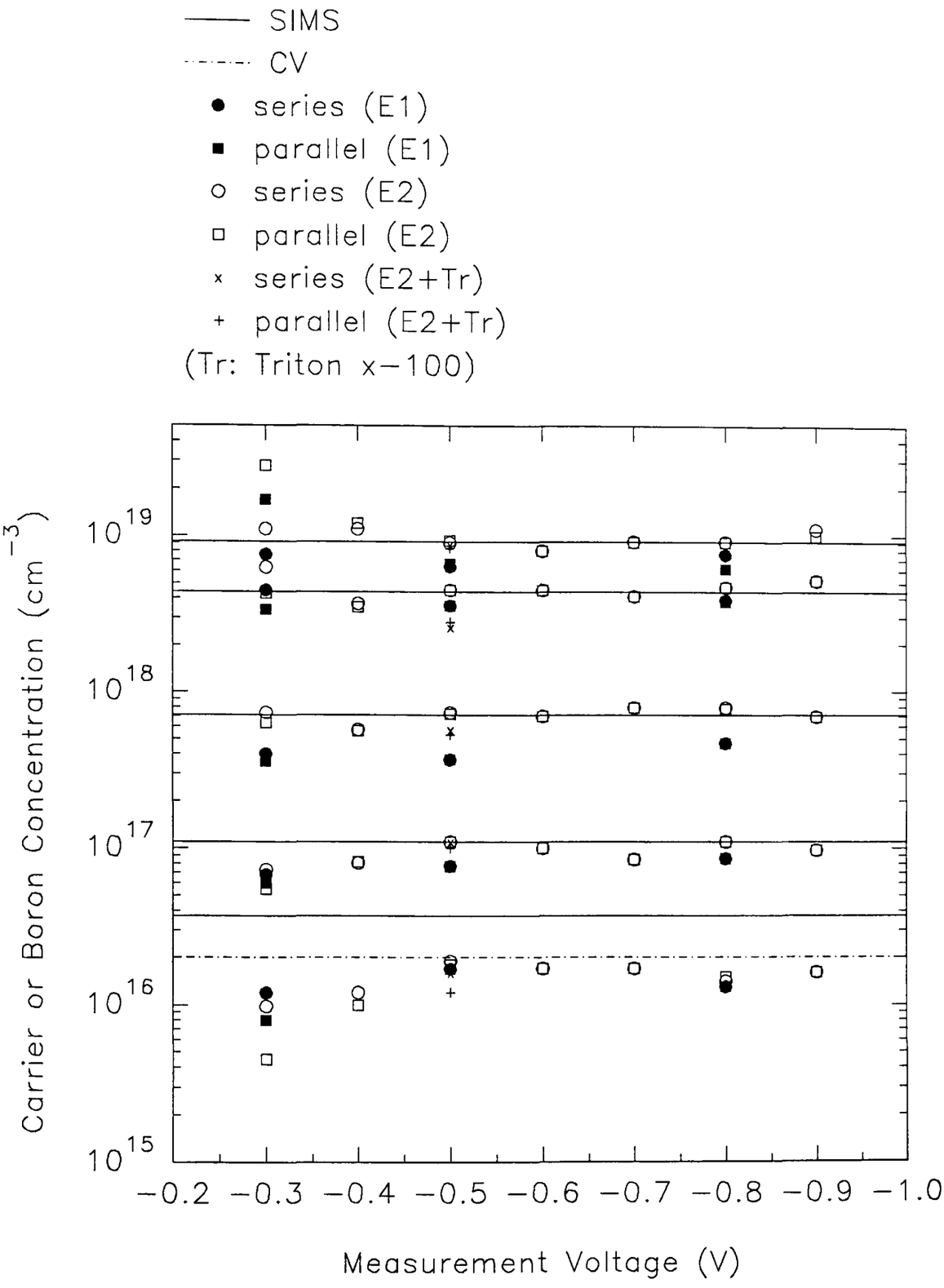

Fig. 3.7. Comparisons of the doping levels obtained from SIMS, conventional CV and ECV measurements.

limited doping range. The Schottky barrier formed between the electrolyte and semiconductor is less satisfactory compared with electrolytes E1 and E2. Also, the etch current density of about 0.3 $mAcm^{-2}$ with this electrolyte is about 15 times smaller than E1 and about 7 times smaller than E2, making profiling rather more time consuming. Conversely, such a slow etch rate may be useful in profiling of ultra-thin layers (see section 3.5).

3.4 HEAVILY BORON DOPED SILICON

3.4.1 UNIFORMLY DOPED STRUCTURES

A comparison between SIMS and ECV profiles of heavily doped structures can provide useful information about boron doping and electrically active doping level limits. However, as discussed in section 3.2, there has been a question mark over the capability of ECV to profile doping levels above 10^{19} cm^{-3}. The above analysis of the boron staircase structure implies that a pre-requisite to obtaining ECV profiles is optimisation of the measurement conditions. This entails choosing a measurement potential which minimises leakage and dissipation factor, and thereby maximises phase angle. In order to optimise parameters in heavily boron doped Si, a few uniformly doped structures were grown at different growth temperatures and growth rates. The *n*-type Si substrates used provided junction isolation to allow van der Pauw measurements to be carried out to obtain an independent assessment of carrier concentration. These structures were previously used to find out electrical activation levels (Parry *et al.*, 1992) and

boron doping induced strain by X-ray diffraction (Powell *et al.*, 1991b) since the growth conditions employed resulted in incomplete electrical activation (Parry *et al.*, 1992) in some cases. Growth details and results are summarised in Table 3.3. A SIMS profile of one of these structures (#10/7) is given in Fig. 3.8. This sample was grown at a growth temperature of 600°C, at a growth rate of 0.10 nms^{-1} and to a thickness of 300 nm. The SIMS profile reveals a doping level of $1.3x10^{20}$ cm^{-3} and Hall measurement confirms that the boron is completely activated.

Sample ID	Growth Temperature °C	Growth Rate nm/s	Thickness nm	**SIMS** $x10^{19}$ cm^{-3} ±%5	**Hall** $x10^{19}$ cm^{-3} ±10%	**ECV** $x10^{19}$ cm^{-3} ±30%
#111/9	800	0.28	840	20	3.5	4.5
#10/6	500	0.10	300	5.6	5.6	5.6
#10/7	600	0.10	300	13	13	15
#10/8	670	0.10	300	14	4.1	4.5
#10/9	760	0.10	300	13	2.8	3.0
#11/13	450	0.01	20	35	36	33
#11/14	600	0.01	20	2.8	2.8	2.2

Table 3.3. Growth details and results of uniformly boron doped samples grown by MBE. The electrolyte E2 with Triton X-100 were used in the ECV results.

An ECV depth profile of this structure for both models using electrolyte E2+Triton X-100 is also given in Fig. 3.8 by keeping the other conditions constant (as given in the experimental section). A measurement voltage of -0.44 V was employed to keep the leakage current to a minimum. A discrepancy between the two models was observed when the leakage current was allowed to increase.

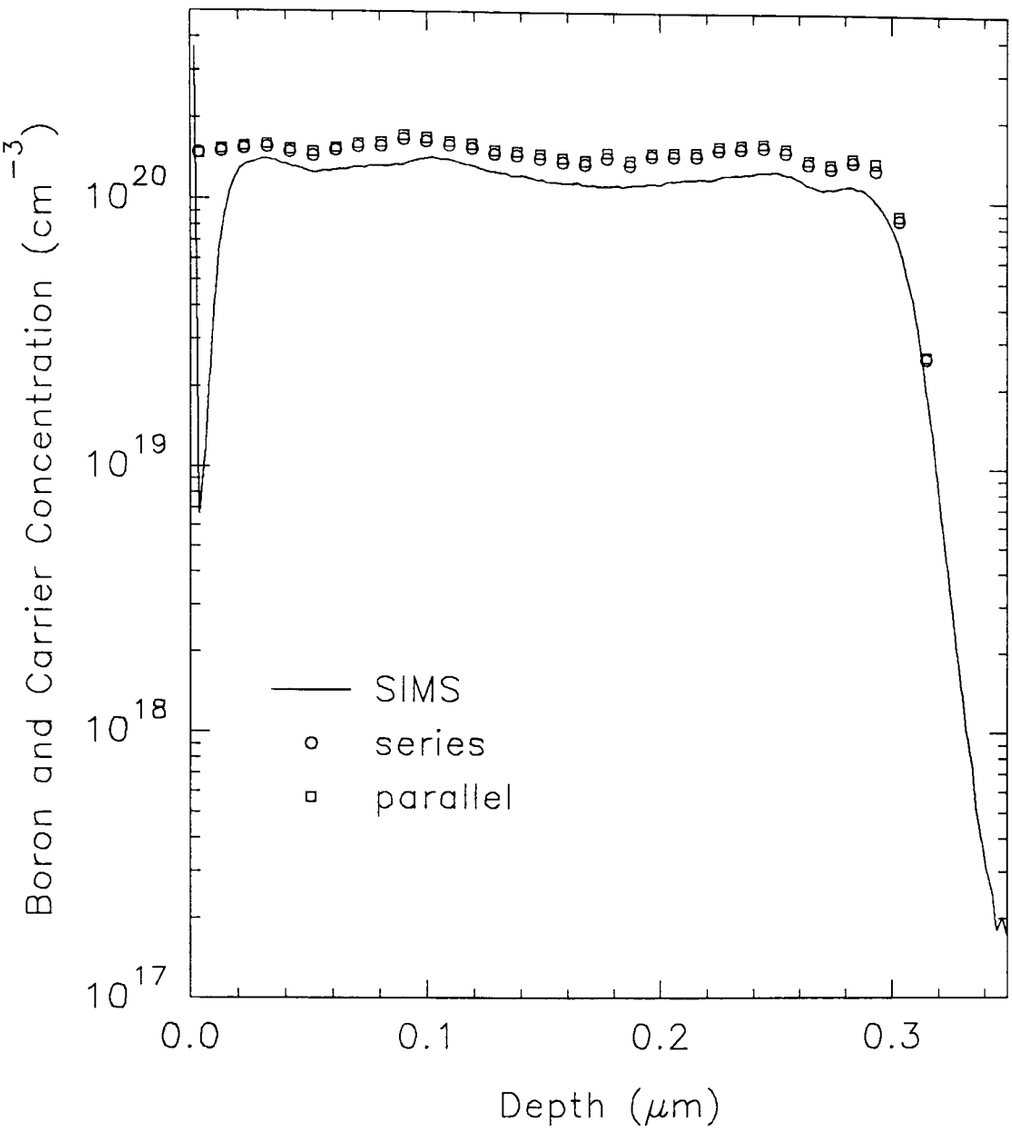

Fig. 3.8. SIMS and ECV depth profiles of uniformly boron doped structure (#10/7).

A SIMS depth profile of another sample (#10/8) is shown in Fig. 3.9a. This sample was also grown at a growth rate of 0.10 nms^{-1} to a thickness of 300 nm, but at a growth temperature of 670°C. Boron concentration from SIMS profile indicates $1.4x10^{20}$ cm^{-3} and Hall measurements indicated only 30% activation of boron (at $4.1x10^{19}$ cm^{-3}) for these growth conditions. When there is no leakage current, ECV depth profile of the structure using electrolyte E2+Triton X-100 provided an average doping level of $4.5x10^{19}$ cm^{-3}. When a measurement voltage of -0.5 V was employed the leakage current was less than 0.025 $mAcm^{-2}$, but this still led to the discrepancy between two models as shown in Fig. 3.9a. Another ECV profile of the structure was obtained using electrolyte E1+Triton X-100 shown in Fig. 3.9b. Discrepancy between the two models occurred despite minimum leakage current (less than 0.005 $mAcm^{-2}$). It can be seen that the series model is successful in obtaining the correct profile for this electrolyte. In Fig. 3.10, *I-V* curves indicated a slightly higher *no leakage measurement voltage range* for the electrolyte E2, although they both started showing a breakdown at about -0.6 V. However the dissipation factor was higher for E1 compared with E2 under the same conditions. It was also realised that when Triton X-100 (wetting agent) is added to both electrolytes E1 and E2, an extended minimum leakage interval for measurement voltage was obtained as also shown in Fig. 3.10. Despite no leakage up to -1.1 V, a sharp change in flat band potential was observed at higher voltages. Also the addition of Triton X-100 provided slightly lower carrier concentrations in all samples.

From Table 3.3, it is seen that the largest discrepancy between Hall measurements and ECV occurred for the sample #111/9 and this sample was

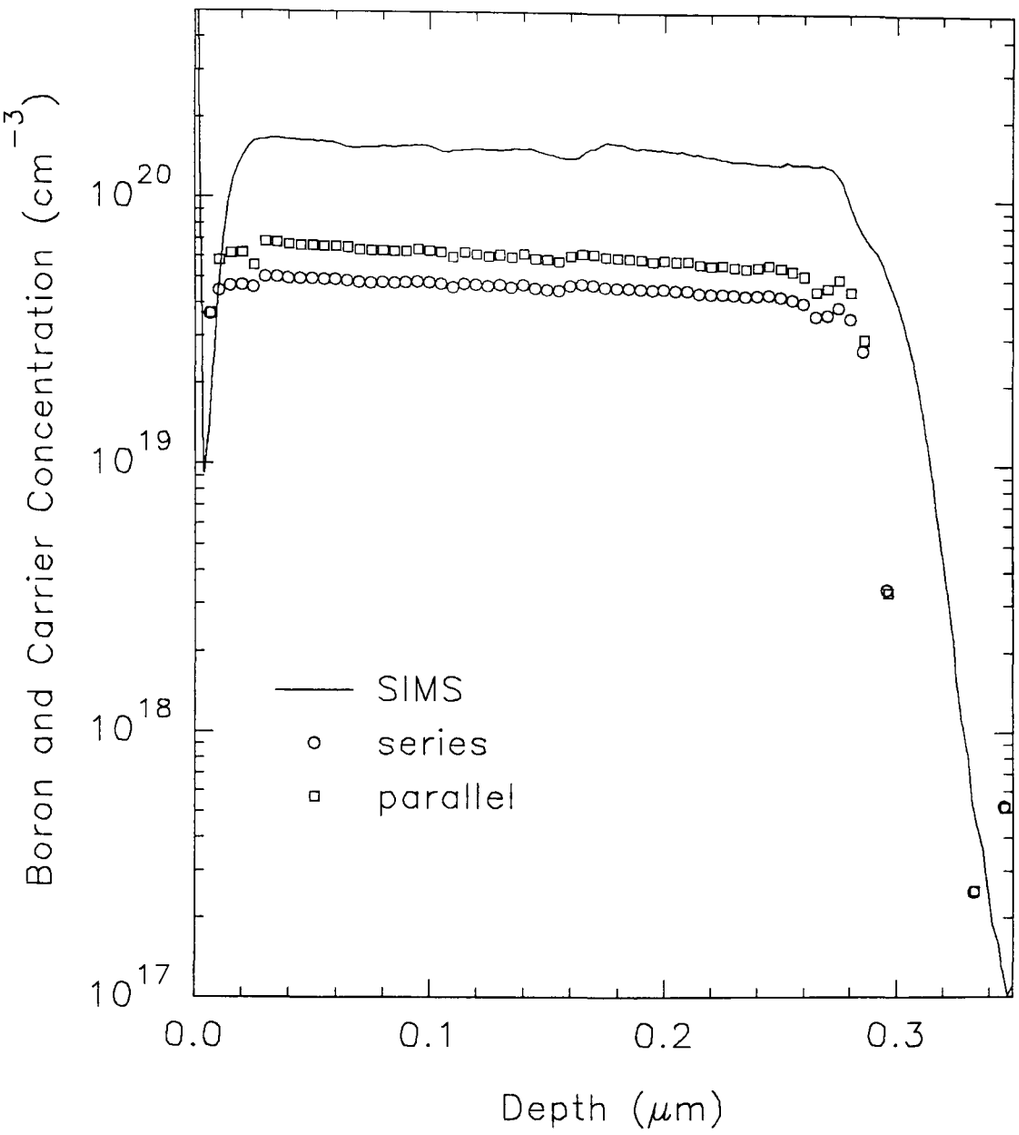

Fig. 3.9a. SIMS and ECV depth profiles of uniformly boron doped structure (#10/8).

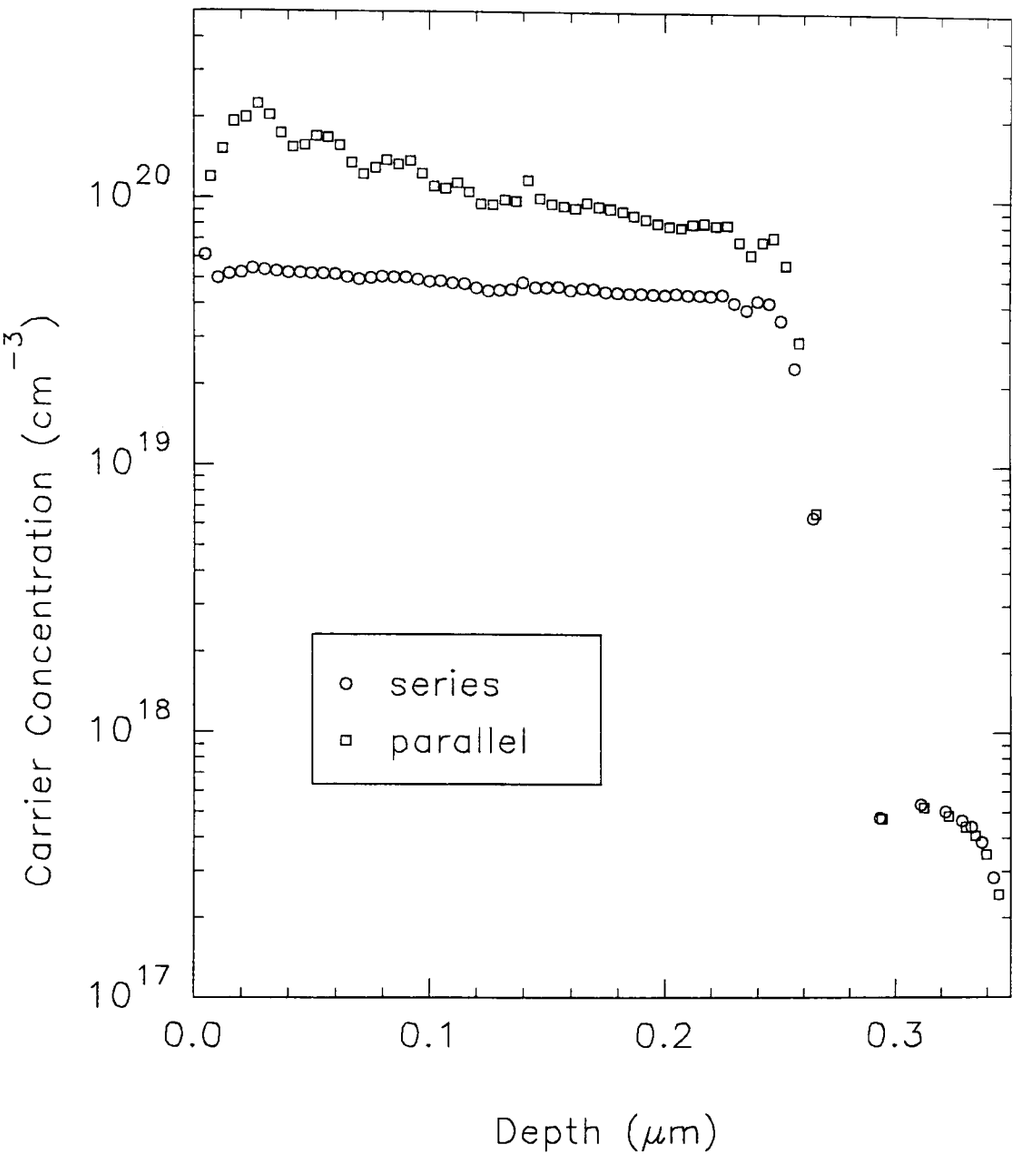

Fig. 3.9b. ECV depth profile of structure (#10/8) using E1+Triton X−100.

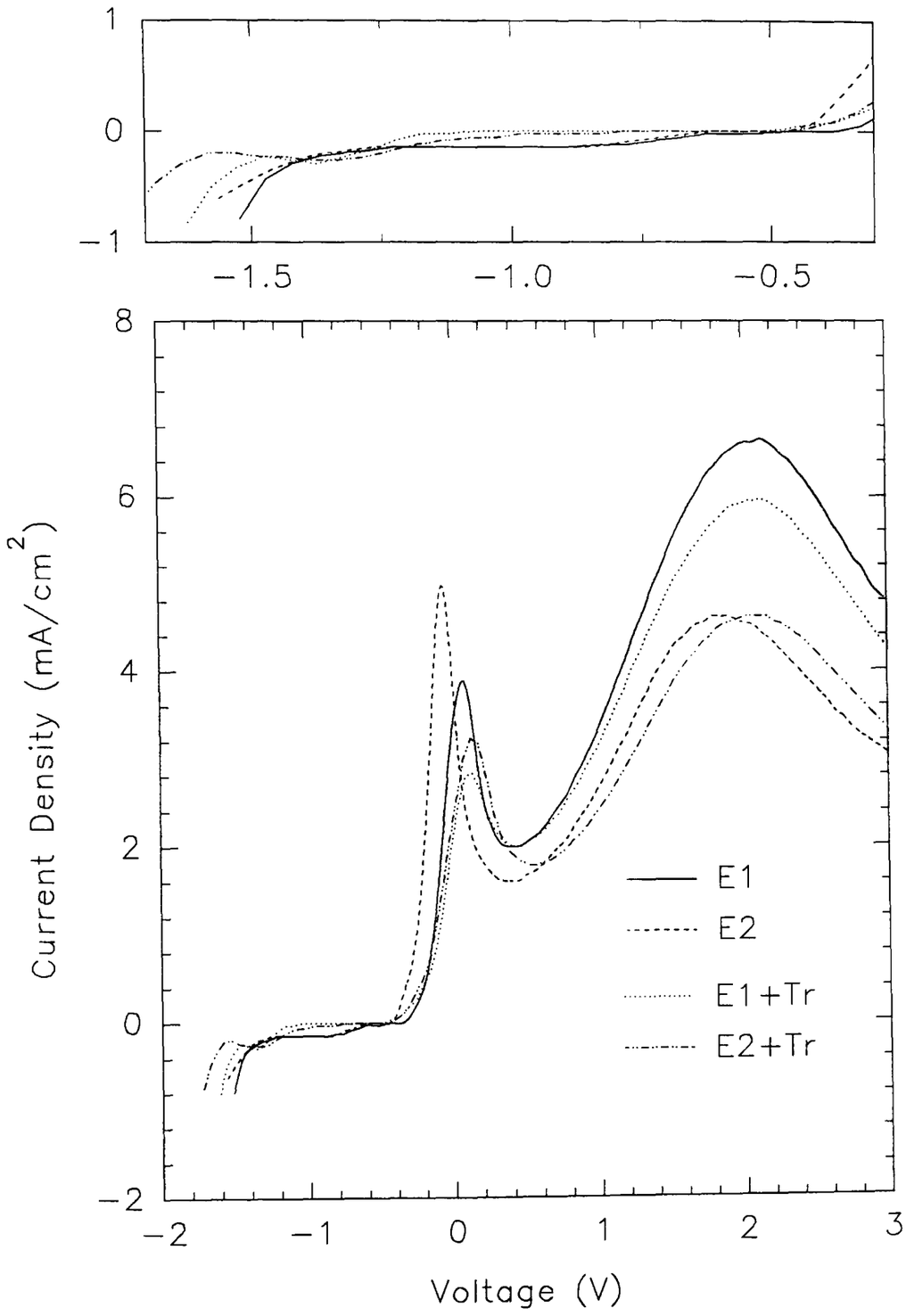

Fig. 3.10. I–V behaviours for structure (#10/8) using electrolytes E1, E2 and with wetting agent.

therefore used to investigate the behaviour of dissipation factor and leakage current. This uniformly boron doped structure was grown at 800°C at 0.28 nms^{-1} and 840 nm thick. The electrolyte E2 with Triton was employed for the ECV profiles of this structure. Fig. 3.11a illustrates how leakage and the dissipation factor vary as a function of measurement potential (reverse bias) during profiling of the uniformly doped sample #111/9 given in Table 3.3, and Fig. 3.11b presents the carrier concentration values obtained using the two available models. Below -0.2V, high leakage is observed (low parallel resistance), which, as can be seen in Fig. 3.11b invalidates the use of the parallel model. Between -0.2 and -0.7V, low leakage with an acceptable dissipation factor was obtained, and the absence of leakage resulted in convergence of the carrier concentration values for the two models negligible contribution from parallel and series resistances. Finally, leakage, and the first signs of breakdown were observed above -0.7V. Similar results were obtained for the other structures in Table 3.3, indicating that optimum measurement conditions for heavily boron doped material correspond to a reverse bias of between -0.2 and -0.7V and we generally use between -0.3 and -0.5V. Table 3.3 shows that the carrier concentrations obtained under the optimised conditions from ECV measurements agree with values obtained from Hall measurements, within the previously stated measurement accuracies. The presence of inactive boron appears not to affect the measurement.

Finally, a 20 nm thick boron epilayer (#11/23) grown on n^- substrate at 450°C with an active doping level in the mid-10^{20} cm^{-3} range was used to test for the upper limit for carrier concentration by ECV. Doping level of boron

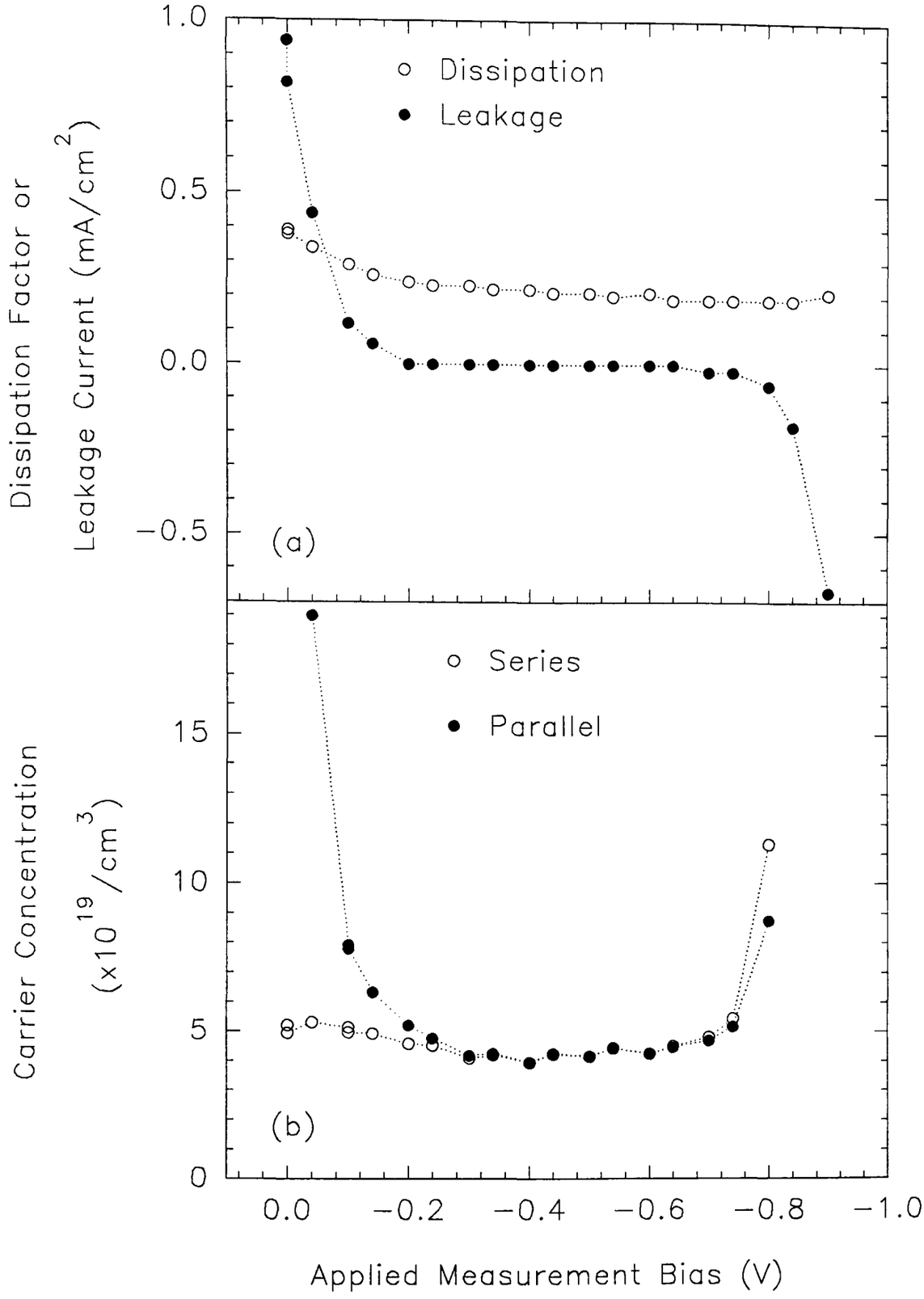

Fig. 3.11. ECV profiling of the uniformly doped structure #111/9, showing the measurement voltage dependency.

concentration was obtained by measuring the areal density in SIMS profile. Hall measurements and ECV results are given in Fig. 3.12.

3.4.2 DOPING TRANSIENTS

The second set of samples included complex doping profiles, to test not only the concentration level, but also the profiling capability of the ECV technique for high-low structures. The first modulation doped structure (#10/15) was grown at 700°C and 0.10 nms^{-1} on p^- substrate. Fig. 3.13 shows the intended boron profile (broken line) based on the boron shutter operation, and SIMS results (solid line). It is evident from the SIMS profile that under the growth conditions used severe surface accumulation occurred during the growth of regions B and A leading to "shoulders" denoted regions D and C respectively. There is also a time delay before equilibrium doping is achieved; these effects are discussed in more detail elsewhere (Parry*et al.*, 1991). The ECV profile shown in Fig. 3.13, obtained under optimised profiling conditions shows firstly that the dopant in regions A and B was incompletely activated. Indeed, the measured doping level ($1.5x10^{19}$ cm^{-3}) agreed well with that expected for boron doping at ~$6x10^{19}$ cm^{-3} under the growth conditions employed from our study on uniformly doped structures assessed by Hall measurements (section 3.5.1). Secondly, the ECV profile of the shoulders in regions C and D agreed extremely well with SIMS over the first part of the shoulder, indicating complete electrical activation as would be expected at these doping levels. However, an apparent discrepancy occurs at points X and Y at doping level of ~$8x10^{18}$ cm^{-3}. This transition in the doping level

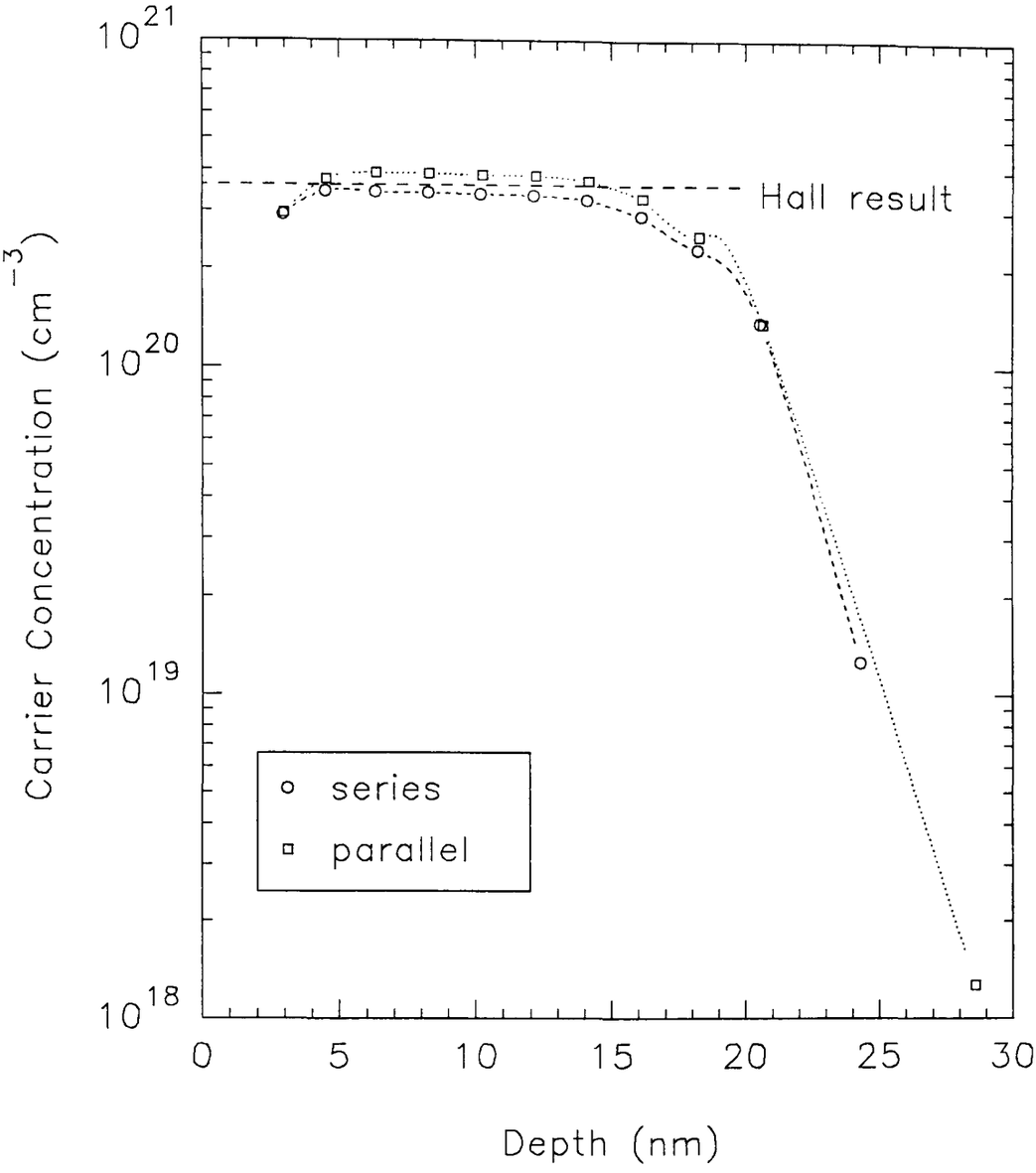

Fig. 3.12. ECV profiles and Hall result of a shallow and heavily doped Si structure (#11/13).

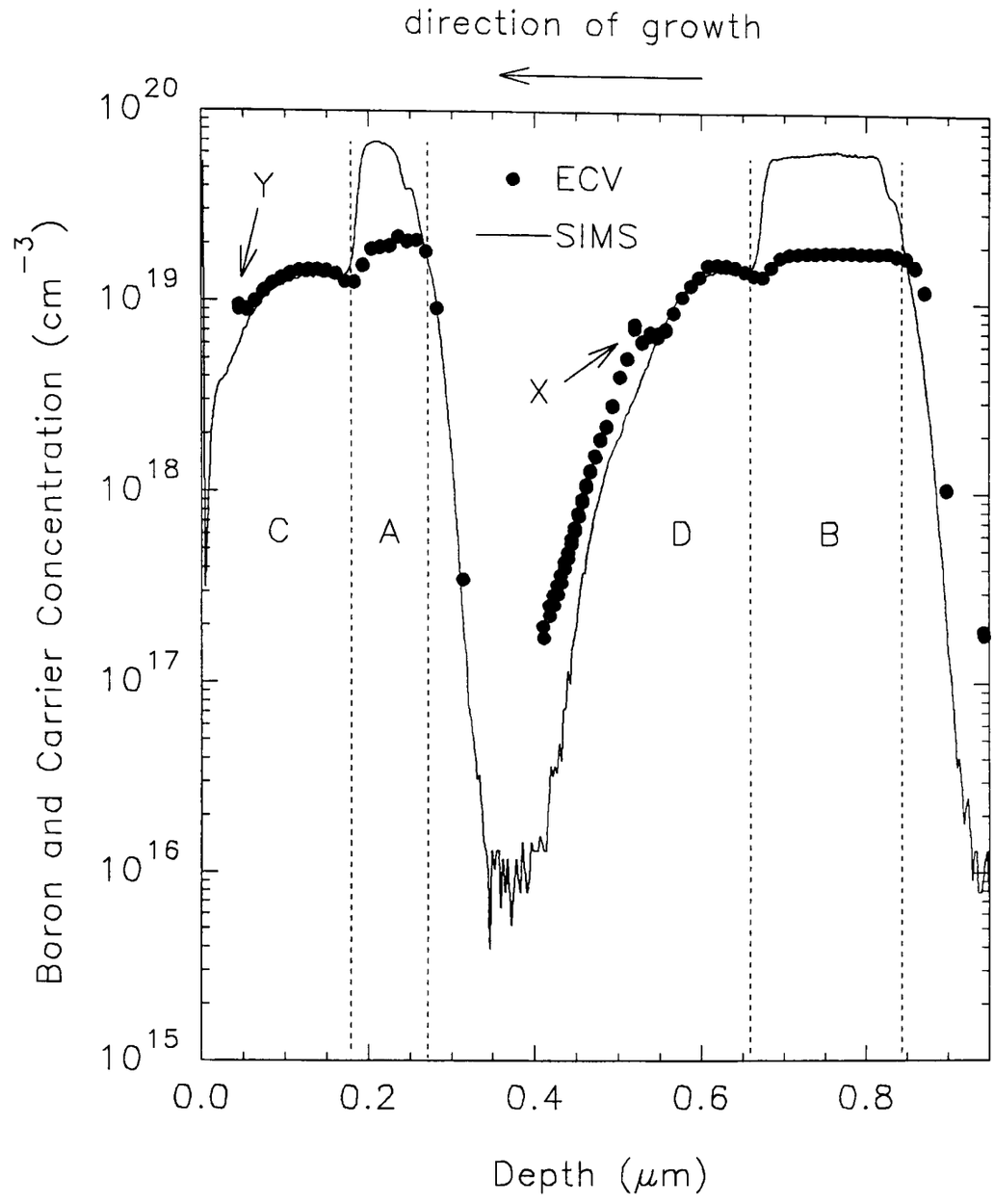

Fig. 3.13. SIMS and ECV depth profiles of a modulation structure grown at 700^{0}C and 0.1 nms^{-1} (#10/15).

varies with measurement bias, suggesting that the effect is associated with the transition of etching from the undoped to the high boron doped regions.

Fig. 3.14 shows another profile structure; grown at 700°C and 0.15 nms^{-1} on p^- substrate, again grown under conditions leading to incomplete activation (B and C) and accumulation induced shoulders (D and E). In this case, the correspondence in regions D and E with SIMS was improved, although the occurrence of the transition at points X and Y is again apparent.

It should be noted that these structures represent extremes of surface accumulation due to the specific growth conditions used. One can note from Table 3.3 that ECV indicates slightly higher results than the Hall measurements for the thick samples, although these results for uniformly doped structures and the graphs for modulation structures have indeed been optimised. The use of electrolyte E2 without wetting agent under optimised conditions resulted usually in slightly higher carrier concentration levels for both uniformly and modulation doped structures. The use of electrolyte E1 on the other hand resulted in a discrepancy between models where the series model appeared in good agreement although again slightly higher but, parallel model was unable to estimate the correct level. The electrolyte resistance for E1 is about 3 times higher than the electrolyte E2, thus the series model is expected to be more appropriate to electrolyte E1.

Although comparisons between Hall measurements and ECV results confirms good agreement, clearly data indicating a *higher* carrier concentration than the real boron concentration (e.g. obtained by SIMS) must

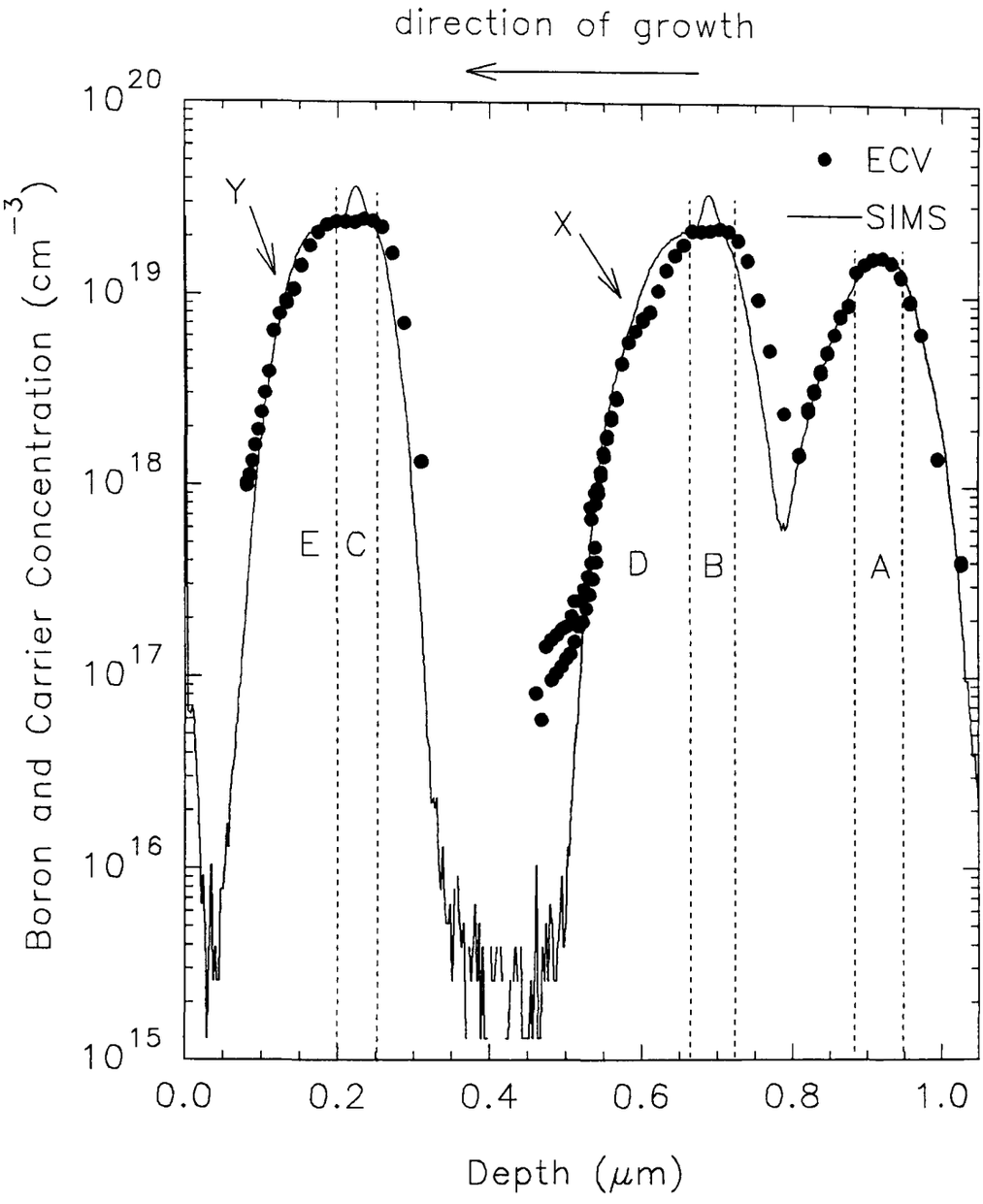

Fig. 3.14. SIMS and ECV depth profiles of a modulation doped structure grown at 700^{0}C and 0.15 nms^{-1} (#10/16).

be treated as suspect. Although good agreement was obtained between SIMS and ECV profiles for MBE grown *n*-type Si (Horányi and Tüttö, 1993), a flat and smooth etch crater was shown employing electrolyte E3, the ECV profile was significantly higher than the corresponding SIMS profile ($3x10^{20}$ cm^{-3}). Kechang *et al.* (1990) also observed a discrepancy in absolute doping levels measured with the two techniques (ECV was higher than SIMS result) in the samples grown to investigate the temperature dependency of boron redistribution.

3.5 PROFILING OF ULTRA THIN BORON LAYERS IN Si

Since the performance and speed of semiconductor devices increase as the spatial dimensions of the device structure decrease, narrower doping distributions are a natural consequence of the spatial scaling process (Gossmann and Schubert, 1993). The routine growth of ultra thin layers (such as delta doping spikes) has become possible with the advent of novel low-temperature growth techniques such as MBE. Characterisation of such ultra thin layers is a challenging analytical task for all techniques each of which has its own capabilities and limitations. Indeed, a *multi*-technique approach is often necessary to fully characterise the structure. For example, TEM images may provide useful information about lateral dopant distribution in a structure, but the relationship between intensity and concentration cannot be quantified. X-ray diffraction provides a fast, non-destructive and high resolution method to assess the spatial localisation of dopants, but it is

necessary to consider and model the strain induced by the dopant (Powell *et al.*, 1991b). In principle some information about the dopant distribution function may be extracted from the position and relative intensity (Powell *et al.*, 1991c) however, as with TEM, sensitivity is poor. With respect to direct dopant profiling, SIMS provides the most reliable assessment, but only of the chemical concentration (Dowsett *et al.*, 1992). In order to use the Hall technique, assumptions have to be made about the Hall factor, typically 0.75 for holes (Lin *et al.*, 1981) and anyway uniformly doped or simple structures are needed. To obtain a carrier concentration profile, conventional CV technique is employed successfully. However the major drawback of the technique is that it is restricted to the profiling of delta layers with a sheet density of less than $1x10^{13}$ cm^{-2} due to avalanche breakdown at higher sheet densities (for example see Gossmann and Schubert, 1993). Here we consider the application of ECV to such structures. Its advantages are discussed in chapters 1 and 2.

The boron-doped sample employed for this study was grown at 480°C to minimise diffusion during growth and, ensure full activation and minimal surface accumulation. It had an intentional (*p*-type) background doping level of $2\text{-}3x10^{16}$ cm^{-3}. A cap layer was also grown at a thickness of 50 nm and doped at $2x10^{18}$ cm^{-3} to allow the ECV technique to resolve the first layer fully. The intended structure is shown in Fig. 3.15a. Fig 3.15b shows a SIMS profile of the structure. The areal densities and thicknesses at FWHMs obtained from SIMS profile along intended thicknesses are given in Table 3.4. It can be seen that thicknesses of the layers as indicated by the FWHMs are

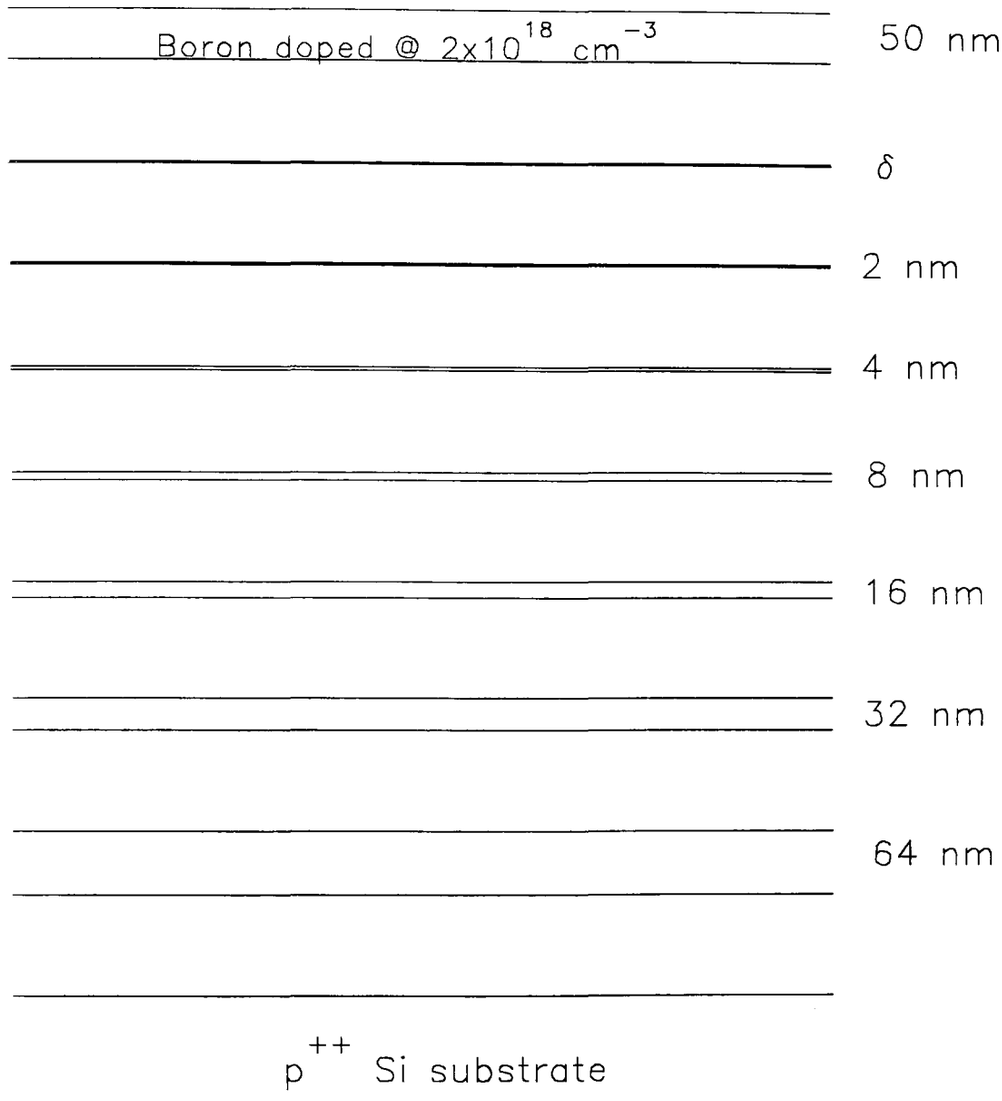

Fig. 3.15a. Intended structure of ultra-thin boron layers in Si (#33/9). Spikes were doped at $2x10^{19}$ cm^{-3} and seperated with 100 nm thick Si layers with a background doping of $2x10^{16}$ cm^{-3}.

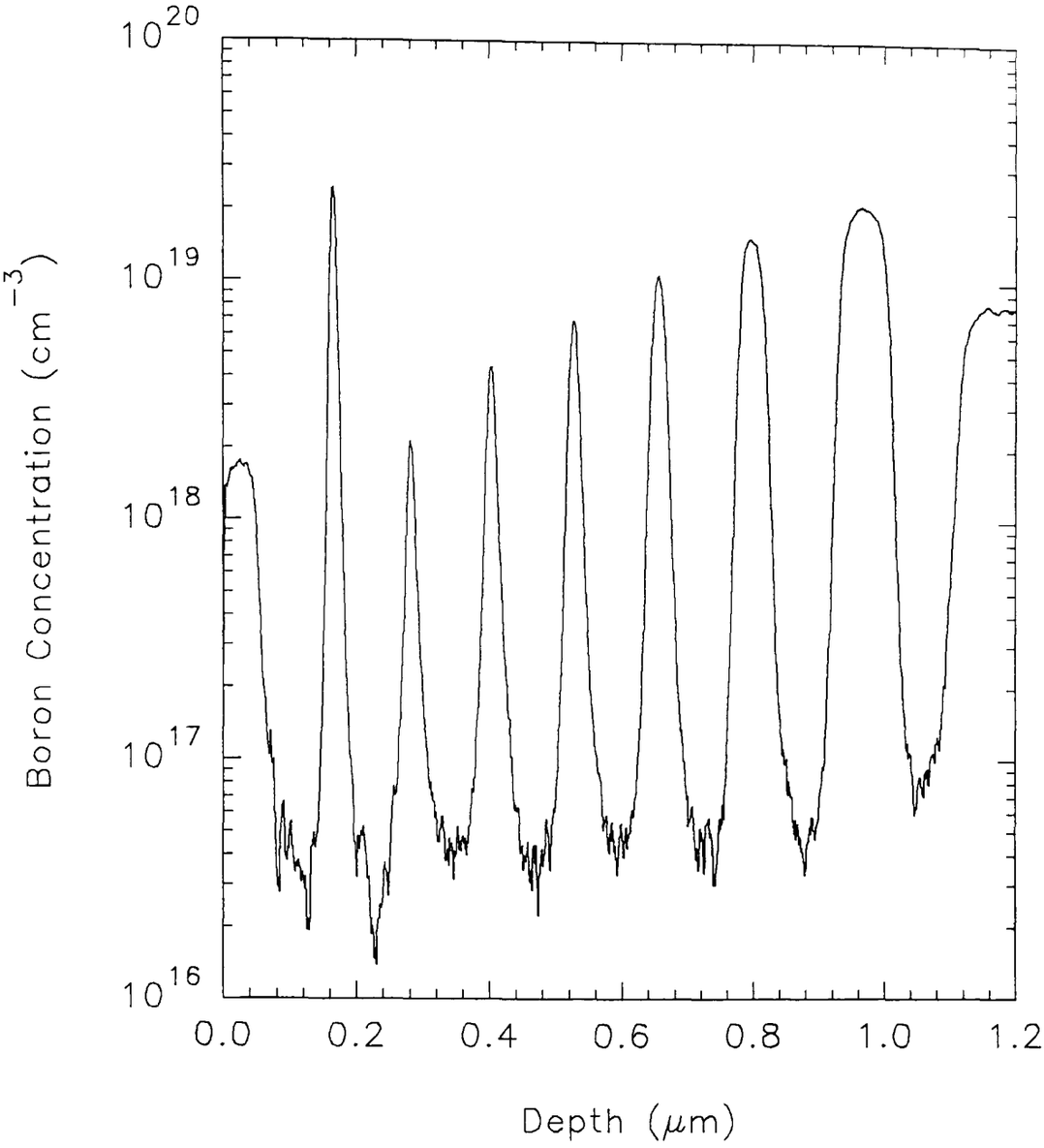

Fig. 3.15b. SIMS profile of ultra-thin boron spikes in Si (#33/9). Primary ions 4 keV O_2^+ normal incidence.

close to the intended values for the thick layers but are overestimated for the narrower features due to intermixing effects (Dowsett *et al.*, 1992).

	Intended thicknesses (nm)	FWHM (nm) SIMS	sheet densities (cm^{-2}) $x10^{13}$		
			SIMS	ECV	SR
Delta		9.6	2.67	2.5	11
1st	2	12.1	0.321	0.34	0.04
2nd	4	13.6	0.734	0.91	0.11
3rd	8	15.4	1.23	1.4	0.19
4th	16	20.3	2.37	2.1	0.88
5th	32	32.3	5.55	5.9	19
6th	64	68.0	13.8	15	48

Table 3.4. Intended thicknesses and FWHMs obtained from the SIMS profile and, sheet densities obtained from SIMS, ECV and SR profiles.

Another feature observed from the SIMS profile was that the peak height of the spikes doped @$2x10^{19}$ cm^{-3} apparently decreased with decreasing spike width. By using the sheet densities obtained from SIMS and intended thicknesses, one can determine that peak heights are in the range of $1.8\pm 0.3x10^{19}$ cm^{-3}, confirming that the decrease in the peak heights with spike width is associated with the limitation in depth resolution of SIMS.

In Fig. 3.15c, a SR profile of the structure is given where depth increment between data points was 6.6 nm. SR profiles of MBE-grown delta layers by other groups have not been realised, so SR profile of such ultra thin

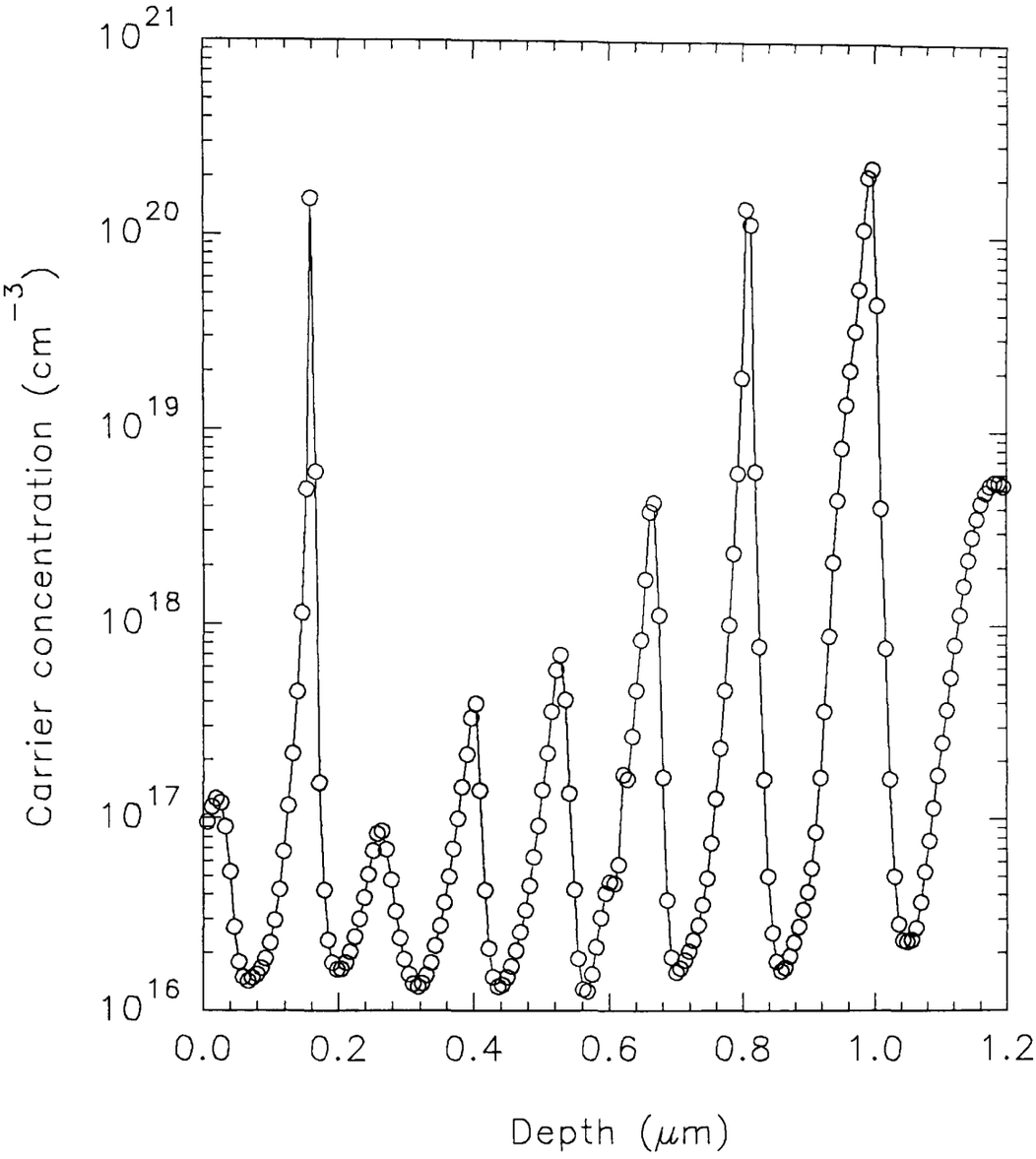

Fig. 3.15c. SR profile of structure #33/9.

layers is reported here for the first time (Pawlik, 1993). The reason to this may well be crystalline quality as crystalline imperfections increases the noise level significantly in SR profiles (Pawlik *et al.*, 1987). It must however be appreciated that all the features are broader in the SR profile than they are in reality due to carrier spilling, which for SR occurs in the opposite direction to that in bulk material due to the presence of a bevel. Carrier spilling effects are therefore the principle limitation in such ultra thin structures. It is also clear that the doping levels are inaccurate by up to a factor of 10 times, probably indicating the limitations of existing algorithms when applied to this layer. Sheet densities obtained from SR profile are also given in Table 3.4 indicating SR is not capable of determining sheet densities correctly for such ultra thin layers. However the locations of the layers are reasonable well determined.

Fig. 3.15d shows an ECV depth profile of the structure. The measurement conditions are given in the Table 3.5. One feature is that background level is not reached due to the Debye Length exceeding the spacing between spikes.

Meas. voltage	Etch voltage	Etch steps	electrolyte	frequency
-0.6 V	2 V	5 nm	E2	3.2 kHz

Table 3.5. Profiling conditions of Fig. 3.15d.

A distortion on the leading edge was observed which increased at higher measurement voltages. This is believed to be due to transition of etching through the change in doping level - as discussed in section 3.4.2. Using

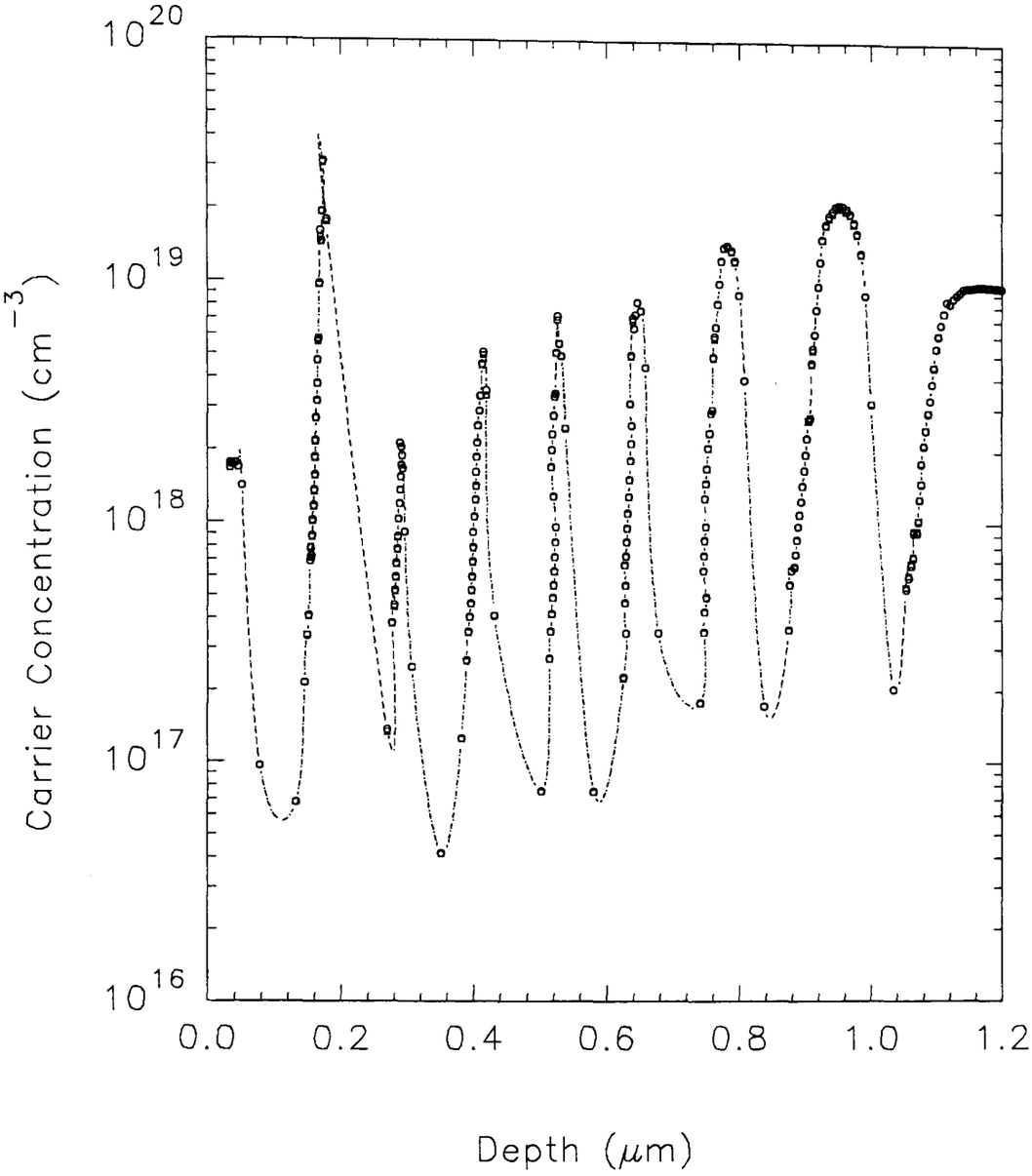

Fig. 3.15d. ECV depth profile of the structure #33/9 using E2 with V_{meas}=−0.6V.

lower measurement voltages again indicated a discrepancy between two models which was discussed for thicker layers in section 3.2. Although all true doping levels (except for the delta layer) are about $2x10^{19}$ cm^{-3}, doping heights in the ECV profile are close to those of the SIMS profile, which as with SIMS, due to limited depth resolution.

Sheet densities obtained from this profile are presented in Table 3.4. Due to the high etch current it is not possible to employ electrolyte E1 for small etch steps. For etch steps smaller than 5 nm, even electrolyte E2 is not practical due to very short etch times (<1 sec) which are not well controlled. In order to obtain smaller etch steps, as Leong *et al.*, (1985) successfully used for rather thick and lower doping levels, the use of diluted electrolyte E2 caused enormous distortions, with increased loss of Schottky barrier quality with dilution. Electrolyte E3 was therefore employed because its lower current rates allow access to smaller etch steps by providing practical etch times. As depicted in Fig. 3.15e (where the conditions given in Table 3.5 were used to provide 2.5 nm etch steps), this lead to the doping levels being largely overestimated. This was due to poor Schottky characteristics as indicated by high dissipation factor.

3.6 CONCLUSIONS

It is apparent that in order to employ ECV, the measurement conditions must be optimised. The choice of electrolyte and measurement voltage play a critical role.

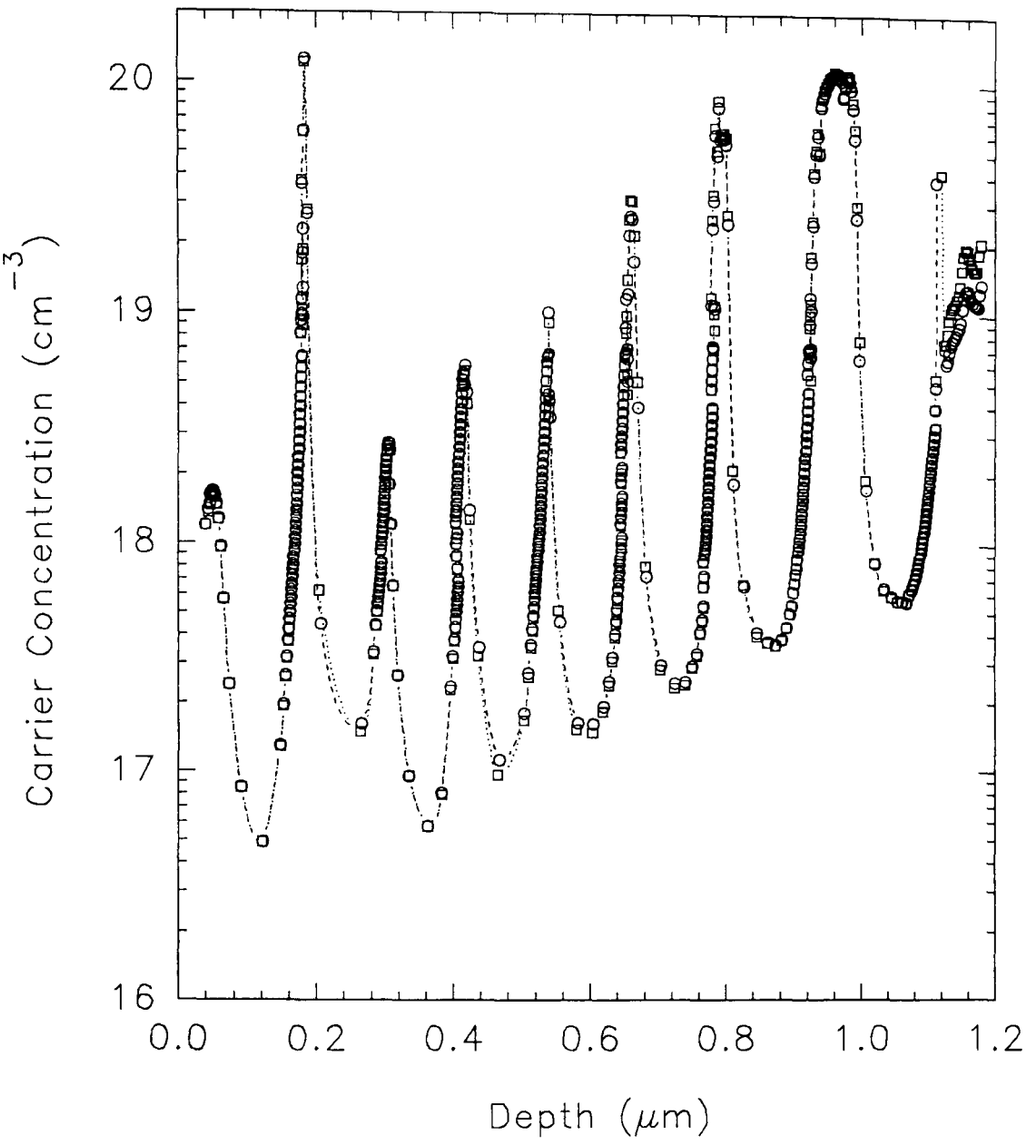

Fig. 3.15e. ECV depth profile of the structure #33/9 employing E3 with V_{meas}=−0.6V.

The first systematic investigation is reported to explore the effectiveness of the ECV technique for profiling heavily boron-doped (exceeding $1x10^{20}$ cm^{-3}) Si. By comparison with SIMS and Hall (as appropriate), an accuracy of 30% was achieved. Despite anecdotal scepticism regarding the capability of ECV applied to Si, it is apparent that the technique is capable of profiling heavily doped layers of both uniformly doped and complex doping structures. Optimisation of the measurement conditions to ensure minimum leakage current as well as acceptably low series resistance lead to a meaningful and reproducible measurement of the doping levels. Incomplete activation of boron under particular growth conditions did not affect the ECV measurements. ECV profiles carried out under optimal conditions showed higher dissipation factor at higher doping levels resulting in slightly higher implied concentrations compared with SIMS and Hall data.

The electrolyte E1 provides a rather fast and unstable etch current density, (3-5 $mAcm^{-2}$) compared with electrolyte E2 which was constant at about 2 $mAcm^{-2}$. E3 gave the slowest etch rate, but less satisfactory Schottky barriers were obtained. As a result, electrolyte E2 is the best choice to profile ultra thin layers. Although electrolyte E1 is less hazardous and easy to prepare, it is not recommended for use at doping levels above $1x10^{19}$ cm^{-3}. Handling E2 needs more caution and 1M NaF needs more time to prepare, but is more convenient to profile very large range of doping concentrations from $1x10^{15}$ to $3x10^{20}$ cm^{-3}. Based on the accuracies of the various steps as performed at present, a measurement accuracy under optimised profiling

conditions (as explained in the text) was ±30% in doping level and in the depth scale of ±10% was achieved.

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CHAPTER FOUR

BORON AND GERMANIUM DEPTH PROFILING IN Si/GeSi STRUCTURES

4.1 INTRODUCTION

The aim of this chapter is two fold. The first part relates to optimising the etching and profiling conditions to achieve the accurate doping determination of free carrier distributions in SiGe/Si layers. The second part is concerned with Ge concentration-depth profiling through monitoring of the etch current variations in SiGe/Si structures. With the combination of these features, the ECV profiling technique is shown to be a rapid and powerful tool for depth profiling both boron and Ge in the Si/GeSi heterostructures. Evaluation of the ECV technique for doping and compositional profiling is performed by comparison with other techniques, such as SIMS and SR profiles.

Strained Si/GeSi based devices grown by MBE have been fabricated since 1984 and used as a route to achieving advanced devices (see for

example Jain and Hayes, 1991; MRS, 1991; Schäffler, 1994). In particular, the unique band-gap engineering possibilities and compatibility of strained Ge_xSi_{1-x} layers with current Si technology have made this materials system attractive for various applications. For example heterostructure bipolar transistors (HBT), which benefit from using a heavily-doped, strained Ge_xSi_{1-x} layer in the base have stimulated extensive research in this material system (King *et al.*, 1989). Further details are given in chapter 1.

Of critical importance is the electrical behaviour of epitaxial materials, particularly when correlated with relevant material parameters such as information on carrier concentration and incorporation of the dopants in the crystalline configuration. Current interest in epitaxial Ge_xSi_{1-x} structures not only requires accurate, fast and reproducible structural characterisation (Jain and Hayes, 1991) but also requires high resolution profiling methods because, increasingly, very thin layers have to be grown.

4.2 RELATED WORK

The capability of ECV technique has been demonstrated for carrier concentration profiling of III-V materials where it has become one of the most commonly used electrical evaluation techniques (Blood and Orton, 1992). The ECV technique has been shown to be better suited to the observation of accumulation spikes in moderately high doped materials than for those of the conventional CV technique (Blood, 1986). Experimental measurements on different doping densities have shown that carrier accumulation features only

become apparent for densities above about $1x10^{17}$ cm^{-3} (Blood and Orton, 1992). Furtado *et al.* (1987) have shown that ECV profiling can be used to obtain the conduction band offset of a single *n-n* AlGaAs heterojunction. Zhao *et al.* (1988) have applied this technique to the study of single *n-n* GaAsSb/GaAs heterojunctions. A successful first attempt was made to compare ECV measurements and simulations on multiple junction device structures (Seabaugh *et al.*, 1989). To optimise Zn dopant profiles in a *pin*-diode/FET, ECV was also employed as a comparison technique (Bauer*et al.*, 1991).

Profiling of Si involved some difficulties and, a large systematic study was presented to show the capability and limitations of the technique for *p*-type profiling of Si in the previous chapter which discusses the optimising of parameters to profile boron doped Si materials. In this chapter we consider use of ECV to extend it further to the Si-based materials; such as Si/GeSi systems.

4.3 THE CHOICE OF ELECTROLYTE

As discussed in Section 2.4, successful applications of ECV depends on availability of a convenient electrolyte for a particular semiconductor material. For any given semiconductor, a convenient electrolyte basically must provide two conditions;

1)- a near-ideal Schottky barrier with the semiconductor

2)- anodic dissolution of the semiconductor.

To profile $Si_{1-x}Ge_x$ layers, an electrolyte should be convenient for various Ge contents. If Si/SiGe heterosutructures are to be profiled, the electrolyte should also allow profiling of Si. Anodic dissolution should provide uniformly even etching for both layers. This condition becomes particularly important for profiling thin layers. Small etch currents are needed for small etch steps, hence high resolution, however too small an etch current makes profiling time consuming. Above all, reproducibility is extremely important for reliable profiles. A non-hazardous and easily prepared chemical solution is always preferred. A low series resistance (which depends on the electrolyte) is another important aspect, particularly for higher doping levels as explained in the section 3.4.

In this study, the electrolytes used in the literature for Si as outlined in the previous chapter are also employed for SiGe. So far no attempt has been traced in the literature for dopant profiling of Ge.

4.4 ECV PROFILING OF BORON DOPED Si/GeSi STRUCTURES

As an example of the profiles encountered with profiling Si/SiGe superlattices, a 12 period uniformly boron doped $Si/Ge_{0.4}Si_{0.6}$ superlattice was grown on an n^- substrate. X-ray diffraction confirmed that Ge content was 40% with 5.6 nm GeSi and 19.6 nm Si layers. Fig. 4.1 shows an ECV

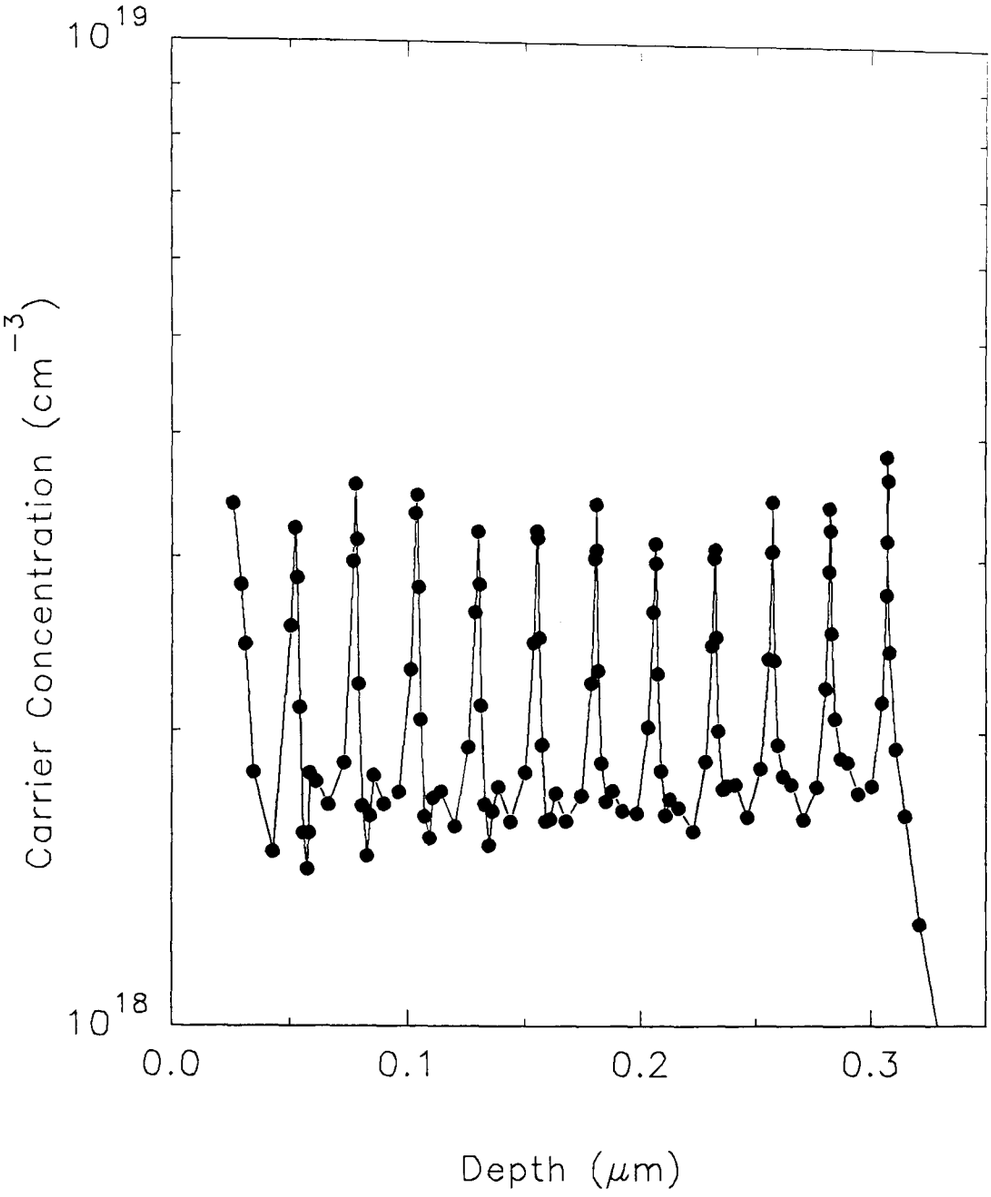

Fig. 4.1. An ECV profile of uniformly boron doped 12 period $Si/Ge_{0.4}Si_{0.6}$ superlattice.

depth profile of this structure obtained by employing electrolyte E2 (1M NaF/ 0.05M H_2SO_4 as given in section 3.2) with a 1.25 nm etch steps. This electrolyte was chosen to obtain higher resolution as discussed in the previous chapter. The etched depth in the profile has been corrected. When the epilayer was etched, the profiler gave about 160 nm etching, however as expected Talystep measurement confirmed 300 nm etching. This indicates that maximum resolution to profile such structure with electrolyte E2 is about 2.5 nm. Experimental measurements on samples of different doping densities was reported that carrier accumulation features only become apparent for densities above $1x10^{17}$ cm^{-3} (Blood, 1986). The profile in Fig. 4.1 shows resolved spikes and dips confirming 12 period; one spike per well. Because SIMS profile of the structure employing boron standards in Si also showed spikes and dips of boron, the spikes and dips could be indicative of the variations in the density of fixed dopant impurities in Si and GeSi layers. However far larger variations in the ECV profile might suggest that it could be due to the accumulation and depletion of free charge at the interfaces.

Structures given below were employed to investigate boron incorporation in SiGe MBE (Parry *et al.*, 1991). As these structures present dopant behaviour in Si and GeSi, they may provide better understanding of capabilities and limitations of the ECV profiling technique for the Si/GeSi system.

Fig. 4.2a shows a SIMS depth profile of a modulation doped $Si/Ge_{0.2}Si_{0.8}$ multilayer structure (#11/25). The structure features 50 nm thick boron layers grown in Si and GeSi at growth temperatures of 650, 600 and

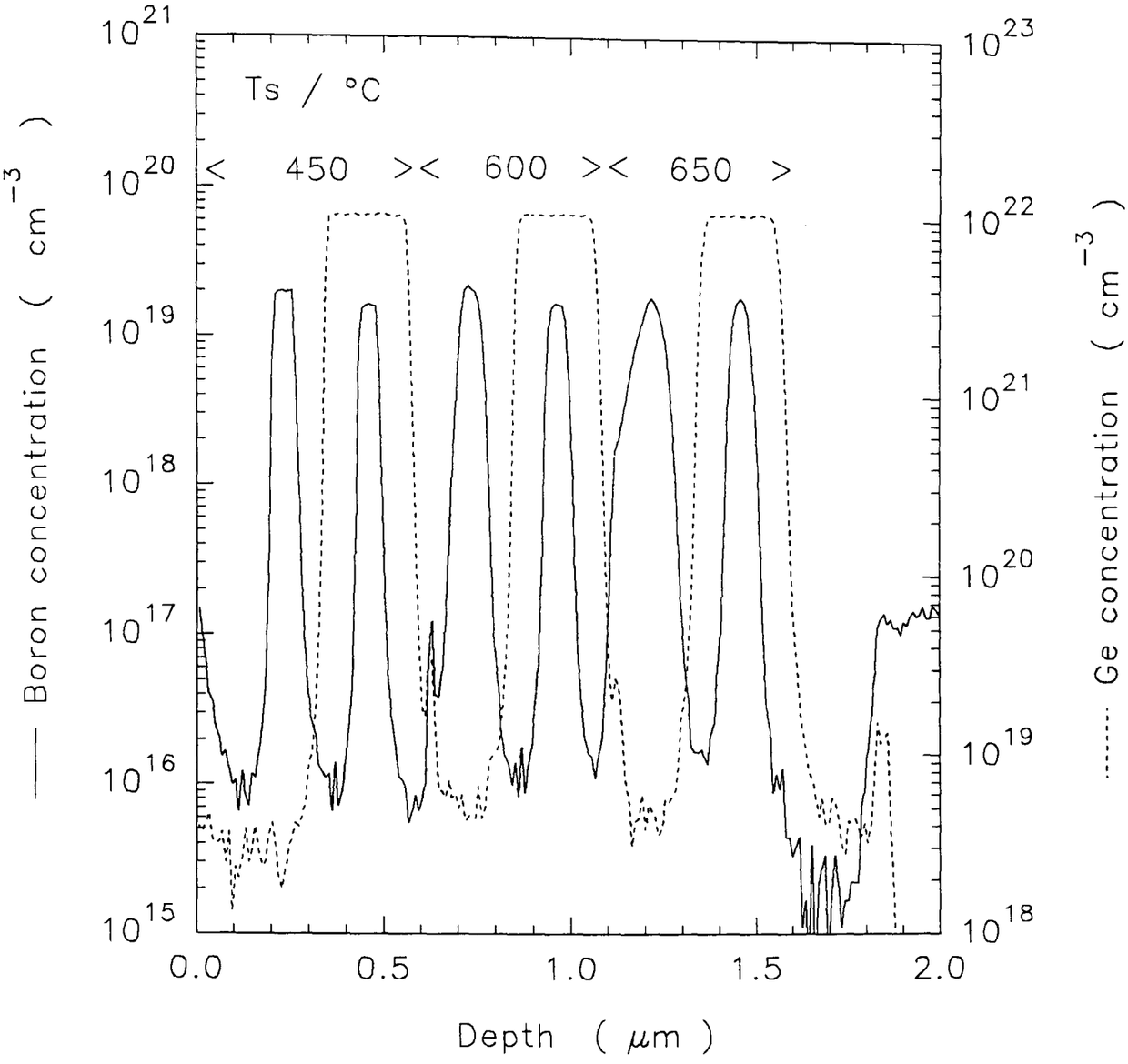

Fig. 4.2a. SIMS Depth profile of modulation doped $Si/Ge_{0.2}Si_{0.8}$ multilayer structure (#11/25).

450°C, and at a rate of 0.10 nms^{-1} as shown in Fig. 4.2a. Growth was interrupted for 10 min during the change of substrate temperature with a 75 nm Si layer grown before starting the next alloy layer. A 100 nm thick Si cap was finally grown. During the growth of boron layers in GeSi, boron flux was increased by 20% to compensate for the increased growth rate. The total thickness of this structure exceeds the metastable critical thickness achievable at 20% Ge. Indeed defect etch measurements revealed dislocations threading throughout the layer confirming that this structure had relaxed. In Fig. 4.2b, corresponding SR profile is depicted. It features rather sharp top ends and the features of the individual layers are lost; for example the boron layers grown at 450 and 650°C provide information from SIMS on boron incorporation which cannot be obtained from SR profile. Nevertheless, the profile shows that the technique is capable of handling Si/GeSi heterostructures with reasonable good doping level and depth resolution. For the ECV depth profiles, both electrolytes E1 (0.1M $NH_4F.HF$ as given in section 3.2) and E2 were employed to optimise the parameters (see section 2.2.2c). Experience has provided information that leakage current is a cause of discrepancy between the models (see section 2.2.2). However the series model was successful in each attempt to profile the structure where dissipation factor was below about 0.4. One example is shown in Fig. 4.2c of which profiling conditions are as given in Table 4.1. As opposed to SR result, the ECV profile revealed the features of boron both in Si and $Si_{0.8}Ge_{0.2}$ layers. Doping levels in the ECV profile appeared about 50% higher for each spike compared with the SIMS profile, whilst in SR profile doping levels were varied. The dissipation factor and leakage current behaviours are also given in the Fig. 4.2d. The dissipation factor as an indication of Schottky formation

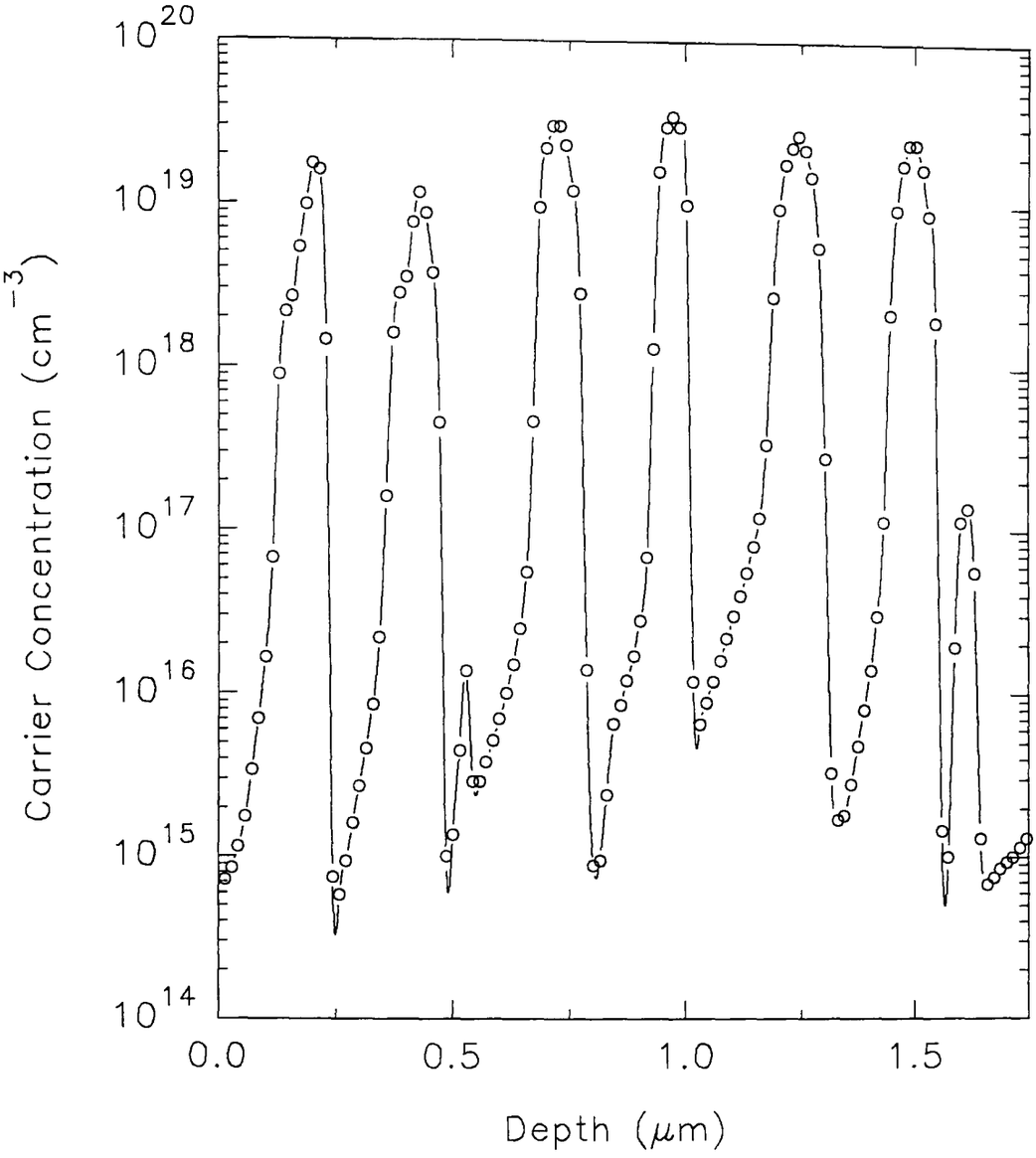

Fig. 4.2b. SR depth profile of boron doped $Si/Ge_{0.2}Si_{0.8}$ heterostructure (#11/25).

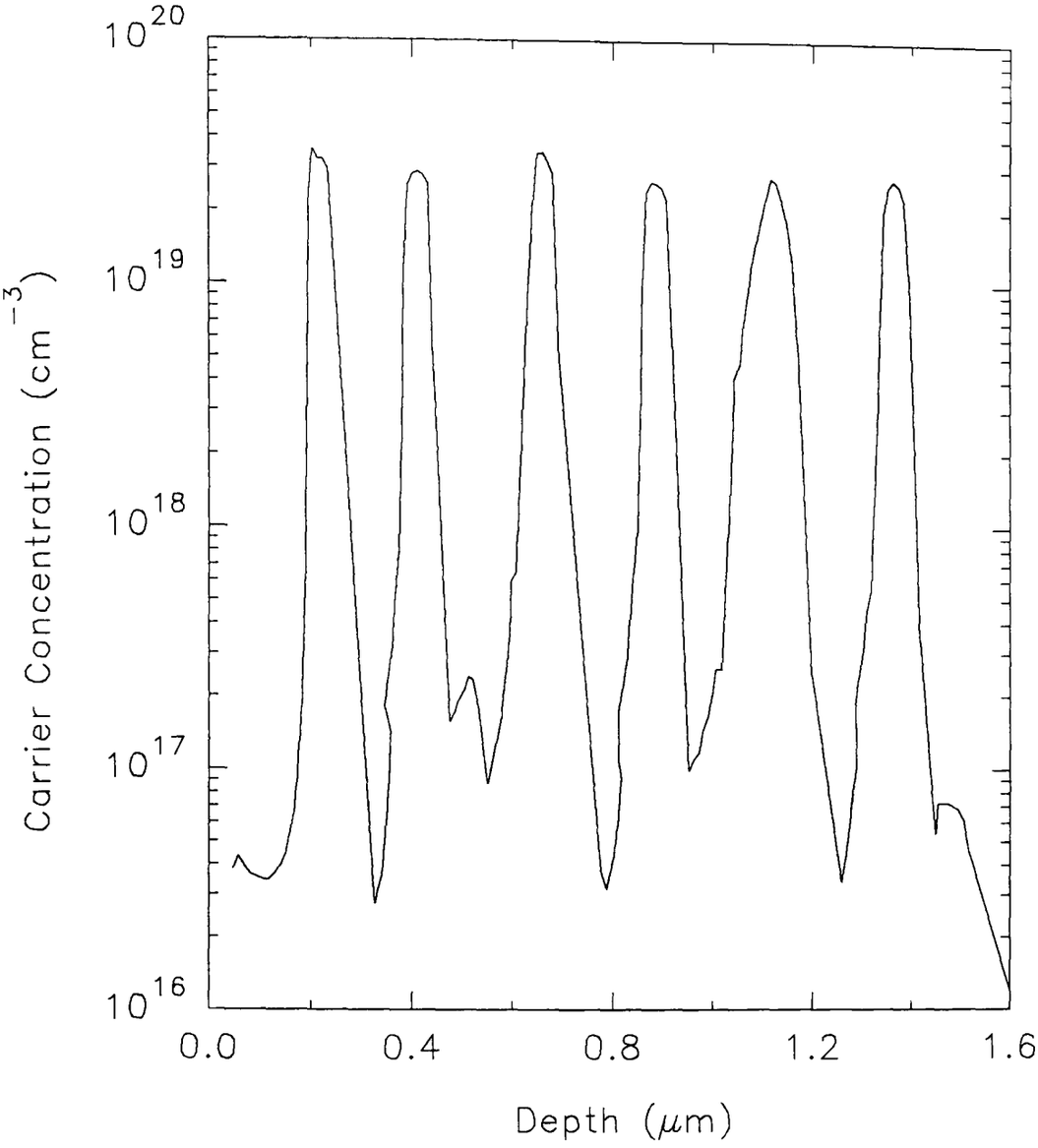

Fig. 4.2c. An ECV depth profile of modulation doped $Si/Ge_{0.2}Si_{0.8}$ multilayer structure (#11/25).

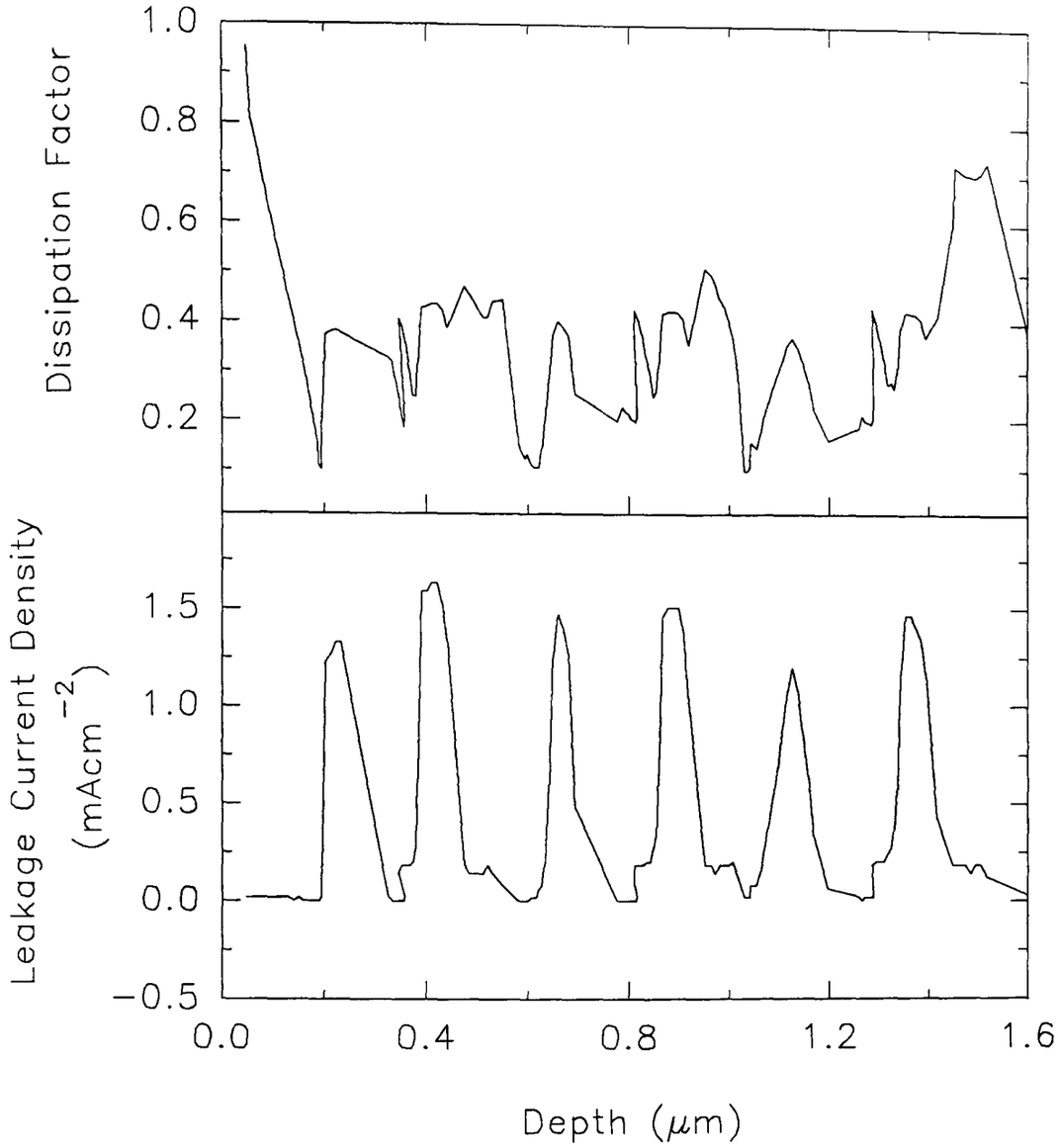

Fig. 4.2d. Dissipation Factor and Leakage Current Density behaviours resulted from Fig. 4.2c.

showed rather random variations. The overestimation of the doping levels can be explained by such relatively high dissipation factor. From this, one can conclude that dissipation factor should be below 0.4 for reasonable Schottky barriers. On the other hand, the leakage current rose with doping spikes which explains the failure of the parallel model. The parallel model however is in excellent agreement with the series model at the leading and trailing edges of the spikes on location but overestimates the doping levels at around $1x10^{20}$ cm^{-3}.

Electrolyte	V_{meas}	V_{etch}	frequency	Etch depth	Settl. time
E2	-0.4 V	2 V	3.2 kHz	10 nm	10 s

Table 4.1. Profiling conditions of Fig. 4.2c.

By utilising the higher reverse bias, the dissipation factor could be slightly lowered and leakage current minimised, resulting in good agreement of both models as shown for the profile depicted in Fig. 4.2c. However as in the case for heavily doped Si structures, high reverse bias disturbs the FBP resulting in a distortion on the leading edges of carrier concentration profiles (see section 3.4). This has been observed for both models sometimes realising small artificial spikes just before the leading edges. These spikes can be identified whether they are real or not, by simply applying various measurement voltages in various profiles for the same structure. This would also provide information about correct doping levels as well as behaviour of the dopant in the semiconductor.

To determine any dependency of Ge fraction on the correct determination of carrier densities, a fully strained Si/Ge_xSi_{1-x} heterostructure was employed (#14/4). The structure features 30 nm thick boron spikes in both Si and Ge_xSi_{1-x} layers. These are indeed thin layers to make an optimisation study but necessary for a fully strain structure. The structure was grown at a growth temperature of 550°C and at a growth rate of 0.10 nms^{-1}. Ge contents were varied from 1% to 20%. Fig. 4.3a shows boron and Ge SIMS profile of the structure indicating the Ge contents. Strong profile smearing under the growth conditions made the thin boron spikes ill defined. Despite this, all boron spikes were resolved in the ECV profiles one of which is shown in Fig. 4.3b. Profiling conditions are given in Table 4.2. Very similar results were obtained by using the small ring and the usual frequency of 3.2 kHz as expected for such doping levels. Nevertheless under the profiling conditions given in Table 4.2 for Fig. 4.3b, a very small leakage current (0.01 $mAcm^{-2}$) was observed only in the region of 20% Ge suggesting a shift in *I-V* behaviour in Si and GeSi regions. This feature will be of great importance to study Ge depth profiles as outlined in the section 4.5.

Electrolyte	V_{meas}	V_{etch}	frequency	Etch depth	Area
E2	-0.4 V	2 V	1 kHz	5 nm	0.1 cm^{-2}

Table 4.2. Profiling conditions of Fig. 4.3b.

In Fig. 4.3c, dissipation factor and leakage current density as a function of depth are given where the measurement voltage -0.3V was employed. Although all spikes were resolved in both models, some small

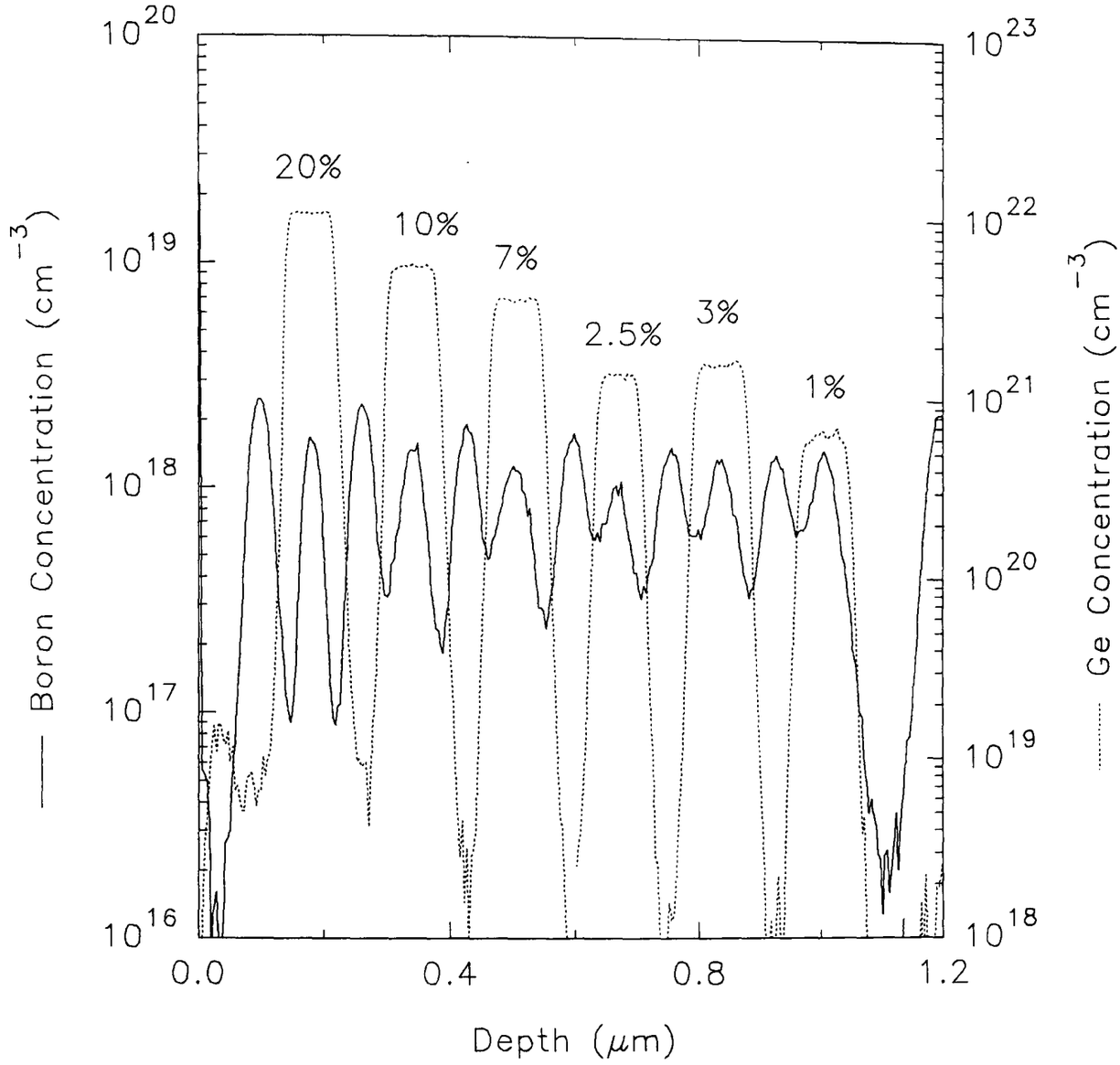

Fig. 4.3a. SIMS Depth profile of a boron doped Si/Ge_xSi_{1-x} structure grown at various Ge fractions (#14/4).

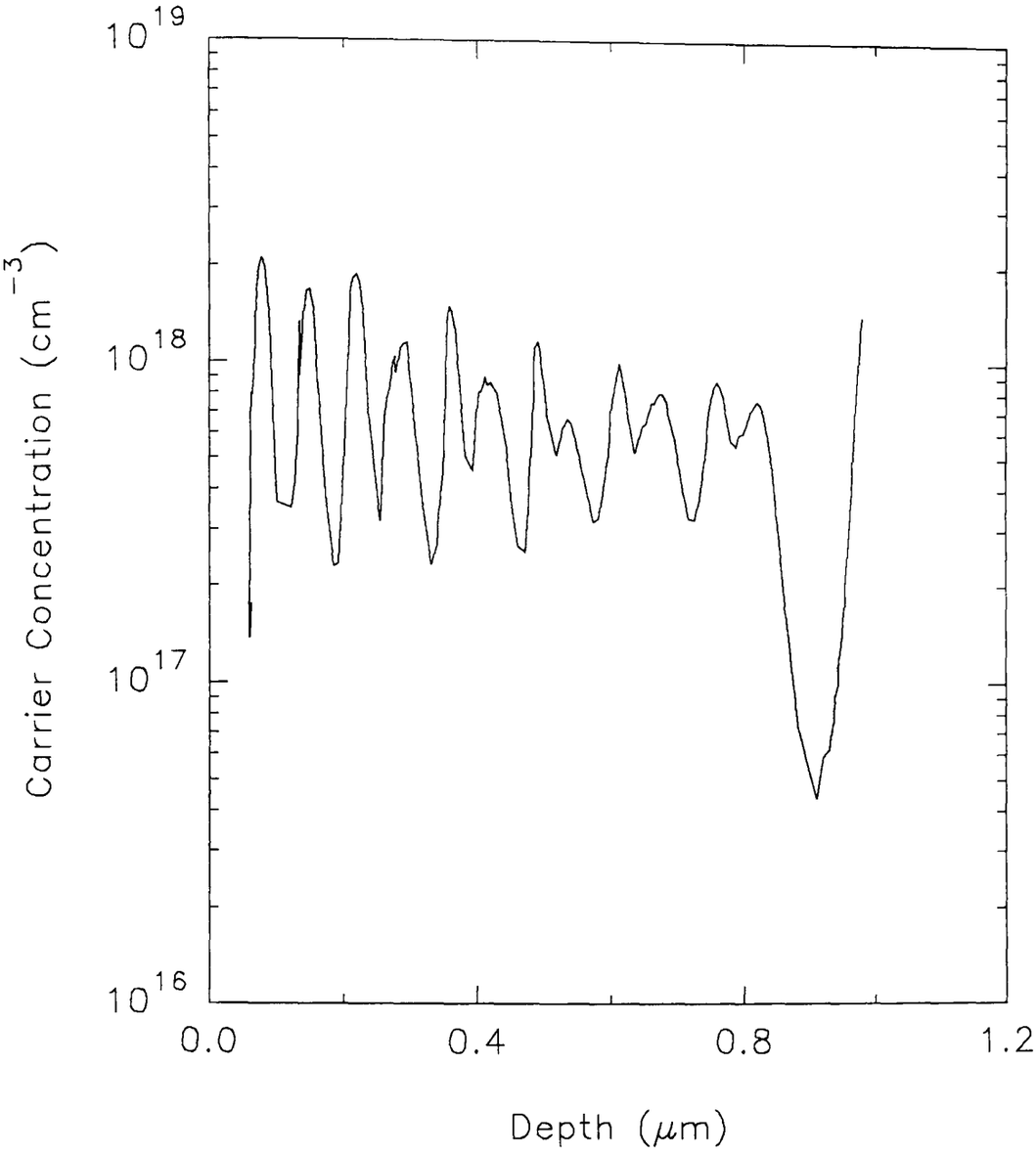

Fig. 4.3b. An ECV profile of thin boron spikes grown in Si/Ge_xSi_{1-x} at various Ge rates.

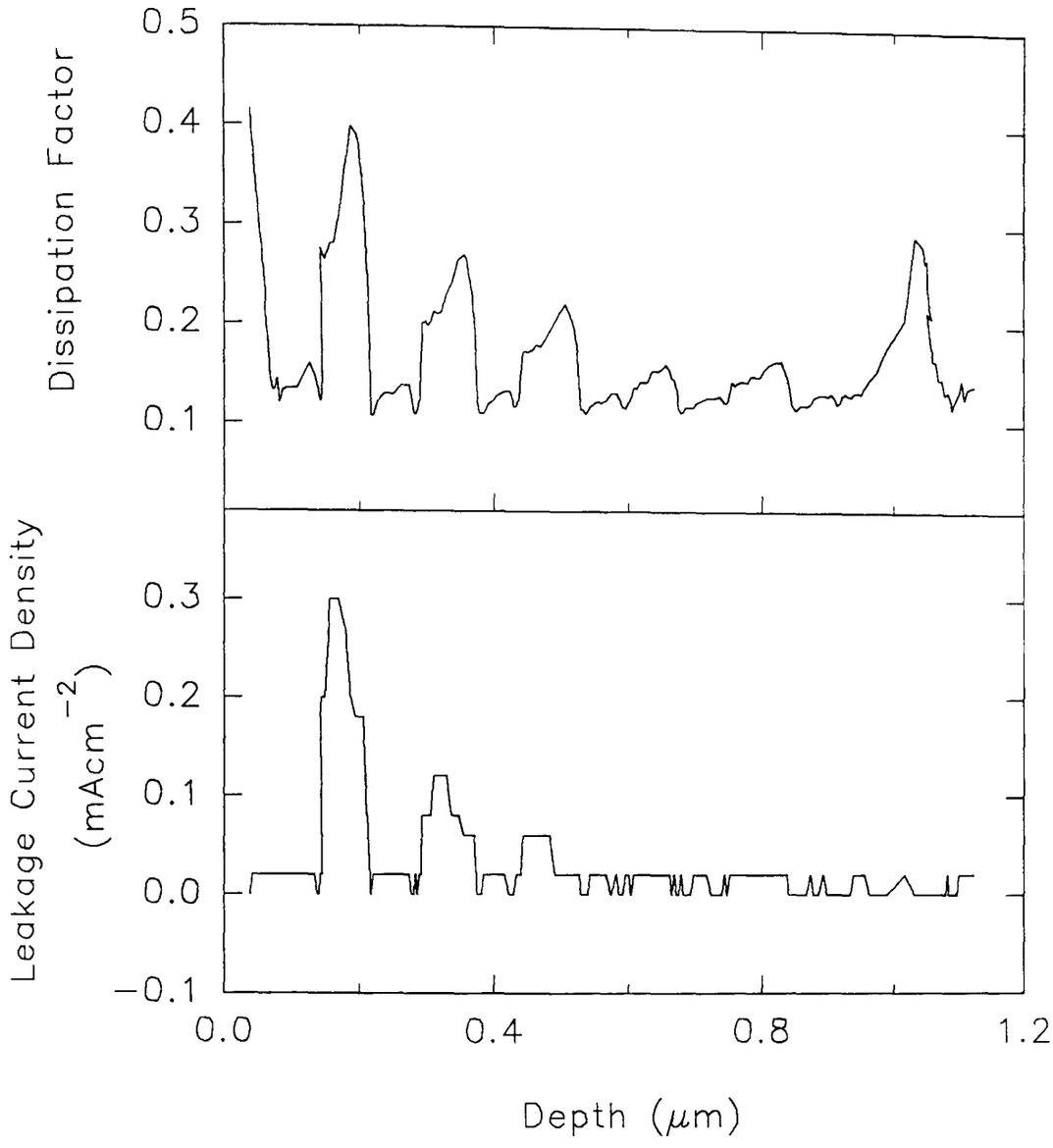

Fig. 4.3c. Dissipation Factor and Leakage Current Density behaviours resulted from V_{meas}=−0.3 V for the structure #14/4.

discrepancy was observed due to leakage current effect. For this measurement it is clear that a deterioration in Schottky barrier formation of GeSi regions have become apparent as shown in Fig. 4.3c (upper part). Again the leakage current density was highest in the SiGe layer of the highest Ge concentration.

Another structure (#17/14) containing boron spikes in Si and GeSi at a Ge staircase was grown at 510°C and 0.10 nms^{-1}. Boron and Ge SIMS depth profile of the structure is given in Fig. 4.4a indicating the Ge fractions. This structure has obviously been relaxed. Fig. 4.4b indicates ECV profiles of this structure where both electrolytes E1 and E2 were employed. Profiling conditions were as given in Table 4.1 for both electrolytes, but an etch depth of 5 nm was used for the electrolyte E1. In general using same etch steps, very similar boron doping levels were obtained for the two electrolytes within the experimental error. This suggests that using small etch steps provided higher resolution hence enabling to reach correct doping levels. With the profiling conditions applied in Fig. 4.4b, leakage current was not detectable and, series and parallel models were matched exactly for both electrolytes. At the first glance the diagram exhibits an overshooting of boron spikes at higher Ge contents. However boron doping concentrations from the SIMS profile indicate ~$4x10^{18}$ cm^{-3}. This suggests that doping levels were not reached at least for boron spikes in Si regions, since both SIMS and ECV instruments were setup for boron profiling in Si throughout the experiments. Quantifications of the SIMS and ECV profiles are given in the following sections where SIMS estimated boron less and ECV higher in increasing Ge content layers. This discrepancy between boron spikes in Si and GeSi layers

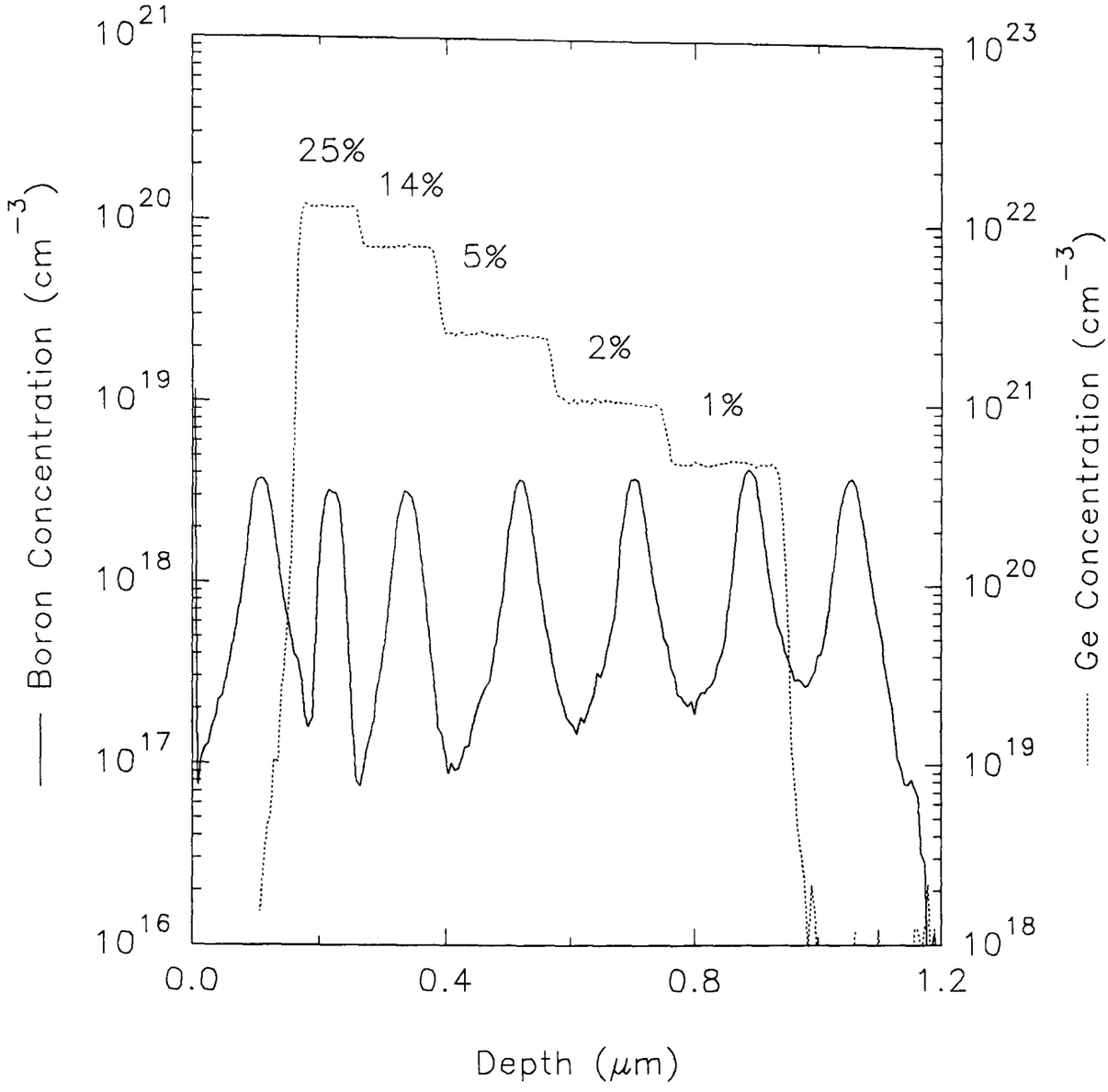

Fig. 4.4a. SIMS depth profile of a boron doped $Si/Ge_xSi_{1-x}/Si$ structure (#17/14).

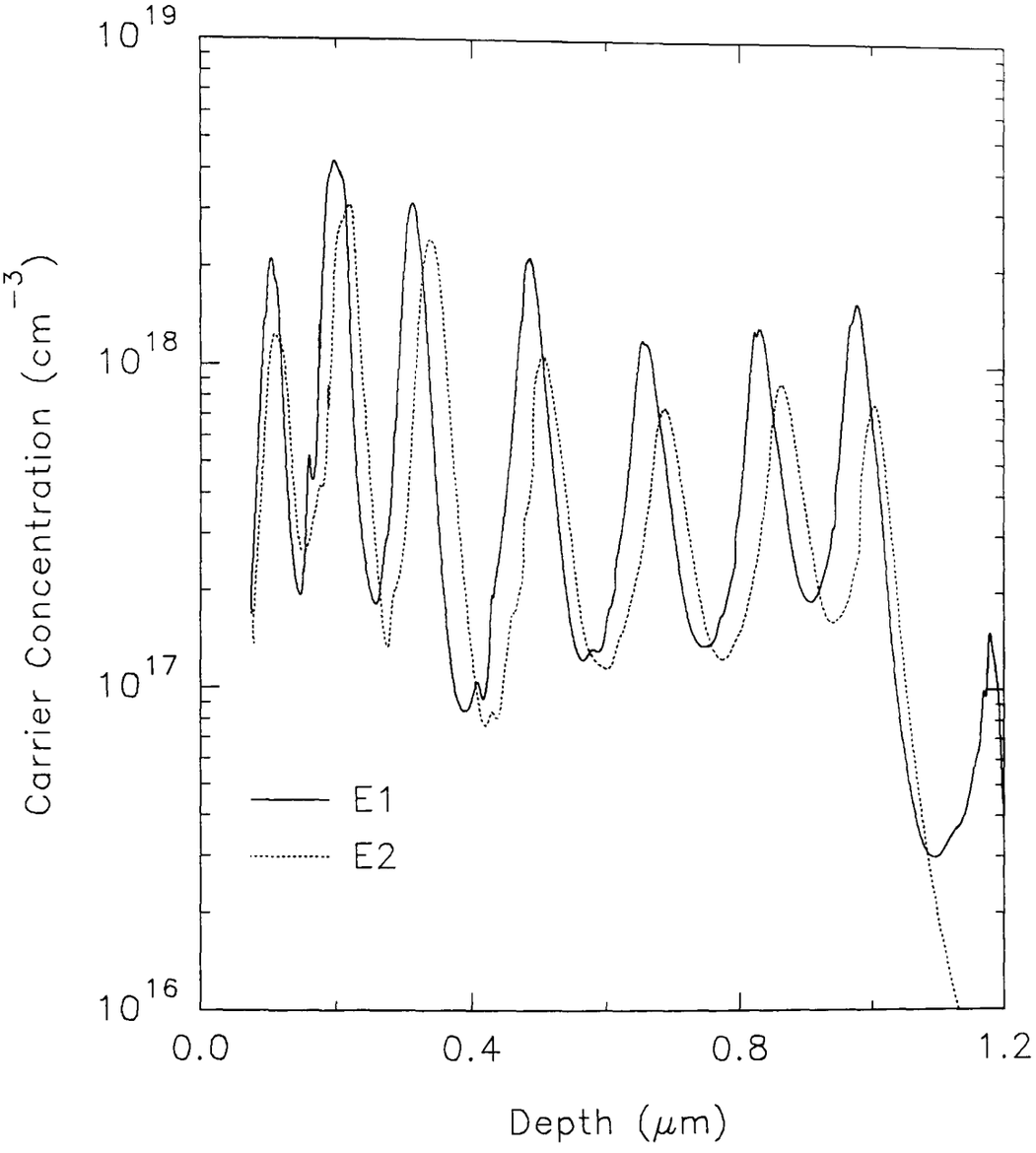

Fig. 4.4b. ECV depth profiles of structure #17/14 under the same conditions but different etch steps.

was not seen between SIMS profile in Fig. 4.3a and ECV profile in Fig. 4.3b even at 20% Ge region. This may either be related to the incorporation behaviour of boron under different growth conditions or to the relaxation of the structure. In the use of low frequency of 1 kHz and higher setting time of 60 s, very similar graphs were obtained.

Finally for both electrolytes E1 and E2, overbiasing (-0.6 V for this case) resulted in better Schottky barrier formation through monitoring dissipation factor, nevertheless distortions with positive and negative mixed data were observed on carrier concentration profiles.

4.4.1 QUANTIFICATION IN SIMS PROFILES

As explained in second chapter, only a fraction of the species of interest in the sample will actually be collected as useful data often described as 'ion' yield. Using a standard, the error in the determination of the atomic concentration profiled under the same set of conditions is less than 5%.

A difference in boron yields was observed in layers grown containing different Ge fractions. However comparative boron yields can be established by measuring the sheet density of boron spikes in Si against those obtained in identical spikes in Ge_xSi_{1-x} for $0< \mathbf{x} <0.25$ (Parry, 1991). As can be seen in Fig. 4.5, the boron yield decreases with increasing Ge fraction resulting in a boron yield in $Ge_{0.2}Si_{0.8}$ ~60% of that in Si. This plot is to be used to obtain

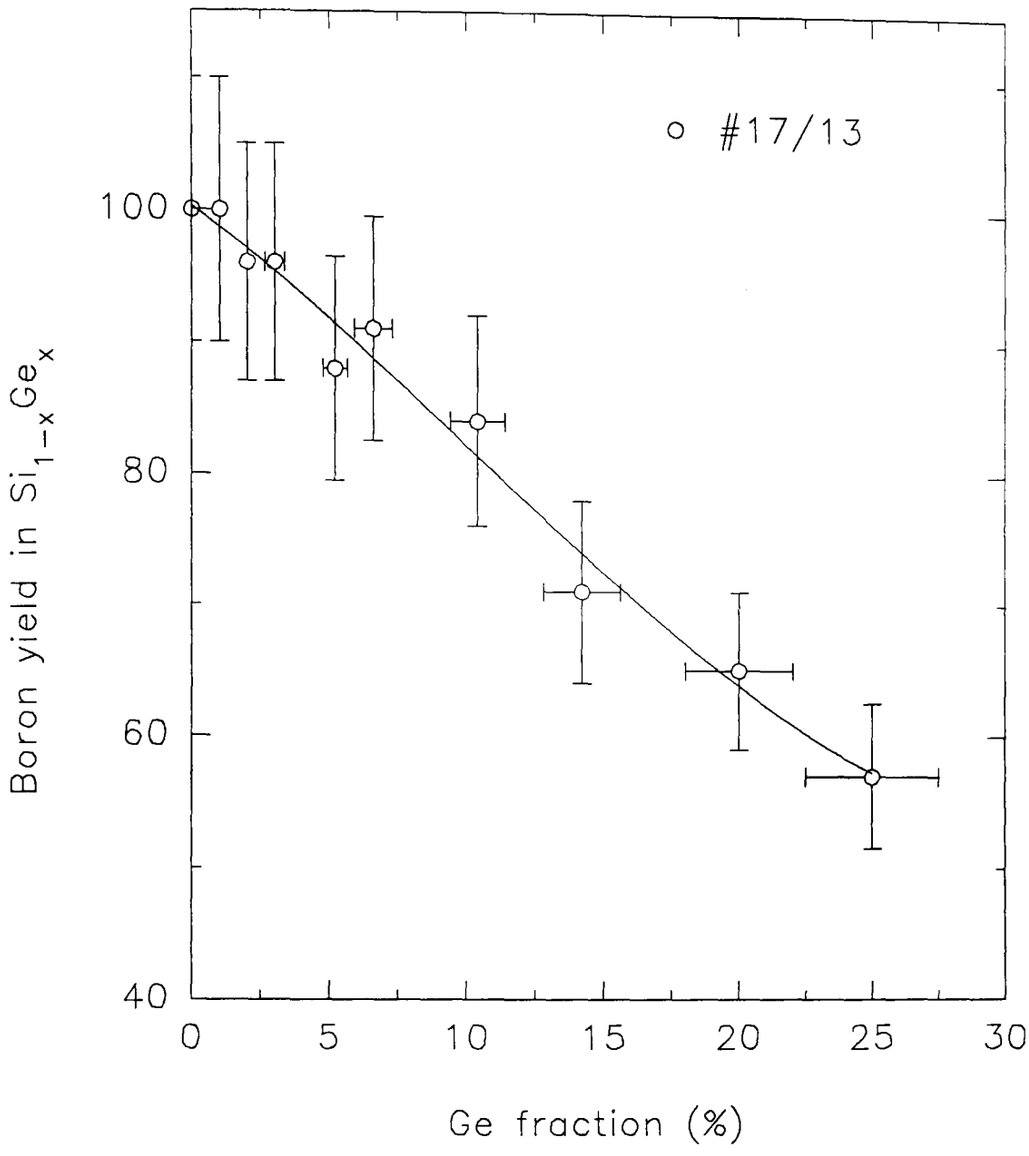

Fig. 4.5. Plot of percentage boron yield against Ge fraction for profiling under identical conditions (After Parry, 1990).

boron doping levels in Ge_xSi_{1-x}, within a 20% error, provided a boron in Si standard is profiled under identical conditions.

The factors affecting depth resolution in SIMS profiles are discussed in the second chapter. The assumption of uniform etch rate during primary ion beam bombardment may not be valid for multilayer structures. If this is the case during profiling of Si/Ge_xSi_{1-x} structures, then the measured Si and GeSi layer thicknesses will contain a systematic error. The error in depth calibration for the structures used in this work is ±5% for Ge fractions up to 25%.

4.4.2 QUANTIFICATION IN ECV PROFILES

An error has been introduced in the calculations of both carrier concentration and depletion depth, due to the different dielectric constants of Si and Ge. Assuming a linear interpolation, the dielectric constant for $Si_{0.75}Ge_{0.25}$ is 13. This implies that boron doping levels in $Ge_{0.25}Si_{0.75}$ layers will be ~9% less than those shown in the diagrams since the dielectric constant of Si has been employed in the ECV graphs.

The depletion depth will be 9% higher in a $Si_{0.75}Ge_{0.25}$ region (see expression 2.5). Removed depth, however, is affected by the presence of Ge which has larger density and molecular weight. On the assumption of linear interpolation, this will contribute about 2.5% error in depth for a $Ge_{0.25}Si_{0.75}$ layer. The effective valence number for GeSi layers remains to be

established and assumed to be same as Si, however results suggest that it is smaller in SiGe compared to Si.

It is possible to make the corrections by reprocessing the raw data (see section 3.3). However in the case of small **x** (Ge content), it can be ignored compared to error in measurements of capacitance and etch current.

4.5 Ge CONTENT PROFILING IN Si/SiGe HETEROSTRUCTURES

Anodic dissolution characterisation of Si/GeSi superlattices was introduced in terms of electrochemical cell potential-depth profiles (Gibbings *et al.*, 1990). During anodic dissolution of Si/GeSi structures, Tuppen *et al.* (1988) reported variations in etch current which corresponded with regions of different composition. The present author has developed this further. In this section, the present author demonstrates that under appropriate conditions, the anodic etch current scales with Ge content, opening the possibility to a simple and rapid method of Ge profiling of arbitrary structures (Basaran *et al.*, 1991).

In addition to the sample preparation in Section 3.3, all etches were freshly prepared as required. It is also found that use of the mechanical pump to remove H_2 bubbles (a by-product of the etching reaction) resulted in excessive noise in the measured etch current, reducing sensitivity to Ge content. Adding a drop of Triton X-100 to the electrolyte suppressed bubble

formation sufficiently to obviate the need for use of a pump, resulting in reduced noise and acceptable crater depth uniformity (±5%).

During the investigation of ECV profiling of Si and Si/GeSi structures, several electrolytes were studied to evaluate their performance for both electrical and Ge concentration profiling as explained in the previous section. Although less reliable for dopant profiling, a mixture of 1M NaF/0.2M $NH_4F.HF$ provided the best choice for Ge concentration profiling, since defect revealing (Tuppen *et al.*, 1988) (which would lead to loss of depth resolution and sensitivity) was avoided, and measurable etch currents could be achieved over the entire composition range of interest.

Fig. 4.6(a) shows a boron and Ge SIMS profile through a typical Si/GeSi structure grown on a *p*-type substrate (denoted structure A) used in a study of the boron doping kinetics of GeSi (Parry *et al.*, 1992). Fig. 4.6(b) shows the corresponding variation in etch current during anodic dissolution of the structure under two different etch conditions (discussed below). To characterise the sensitivity of the electrolyte to Ge content and optimise the etching conditions, the *I-V* characteristic was measured in the middle of the Si and GeSi regions in structure A, as shown in Fig. 4.7. In Si, the *I-V* curve shows an initial rise to 0.7 V, followed by a negative resistance region, consistent with the previous results for *p*-type Si (Memming and Schwandt, 1966 and section 3.4), with a trough at about 1 V. Finally, a rapid rise is observed which exceeds the current measuring capability of the profiler at about 2.5 V. The usable etching voltage for Si is thus between 1.0 and 2.5 volts. The effect of Ge composition on *I-V* characteristic is apparent in Fig.

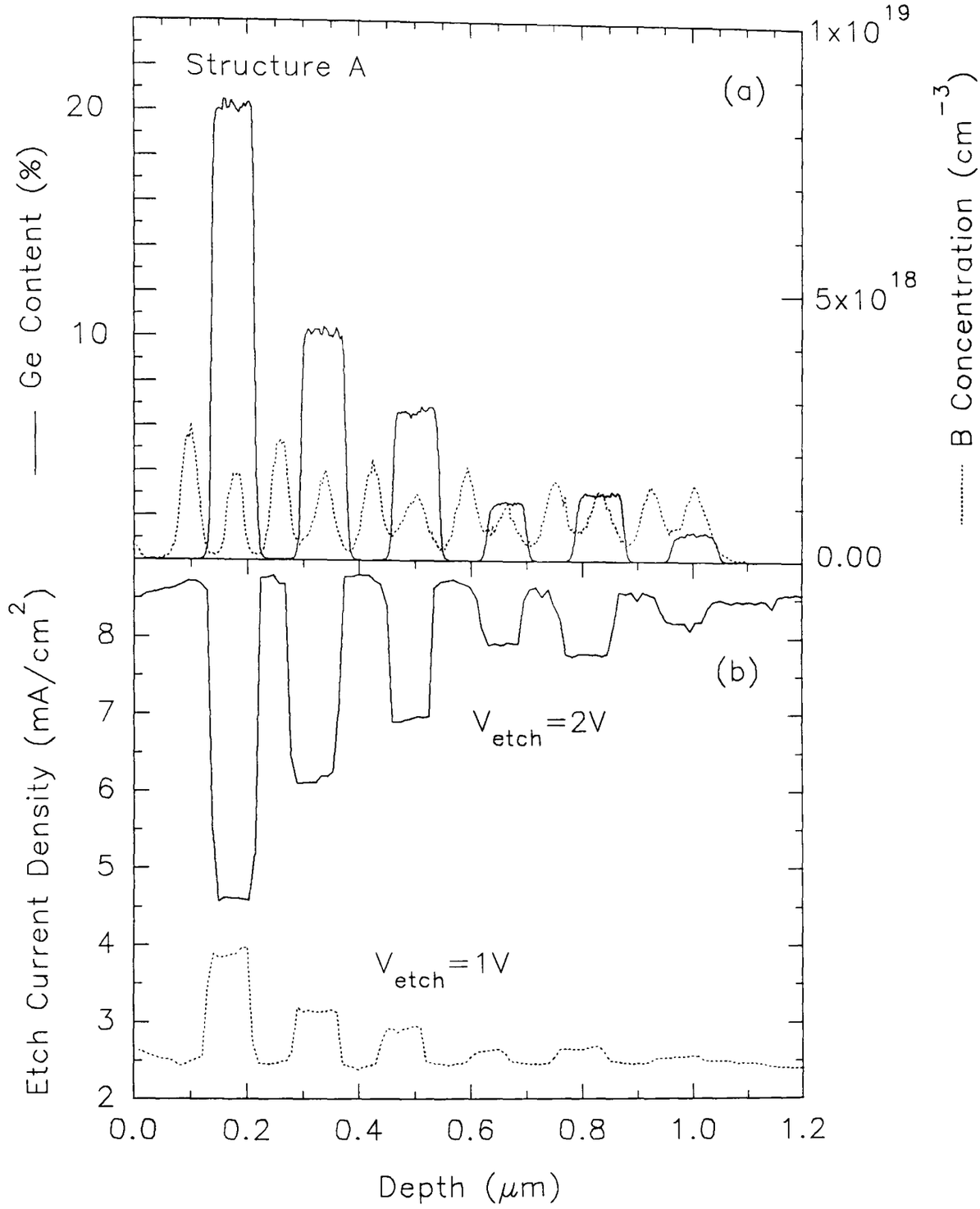

Fig. 4.6. (a) Boron and Ge SIMS depth profiles of #14/4, (b) Etch current density vs depth profile at V_{etch}=2V and V_{etch}=1V.

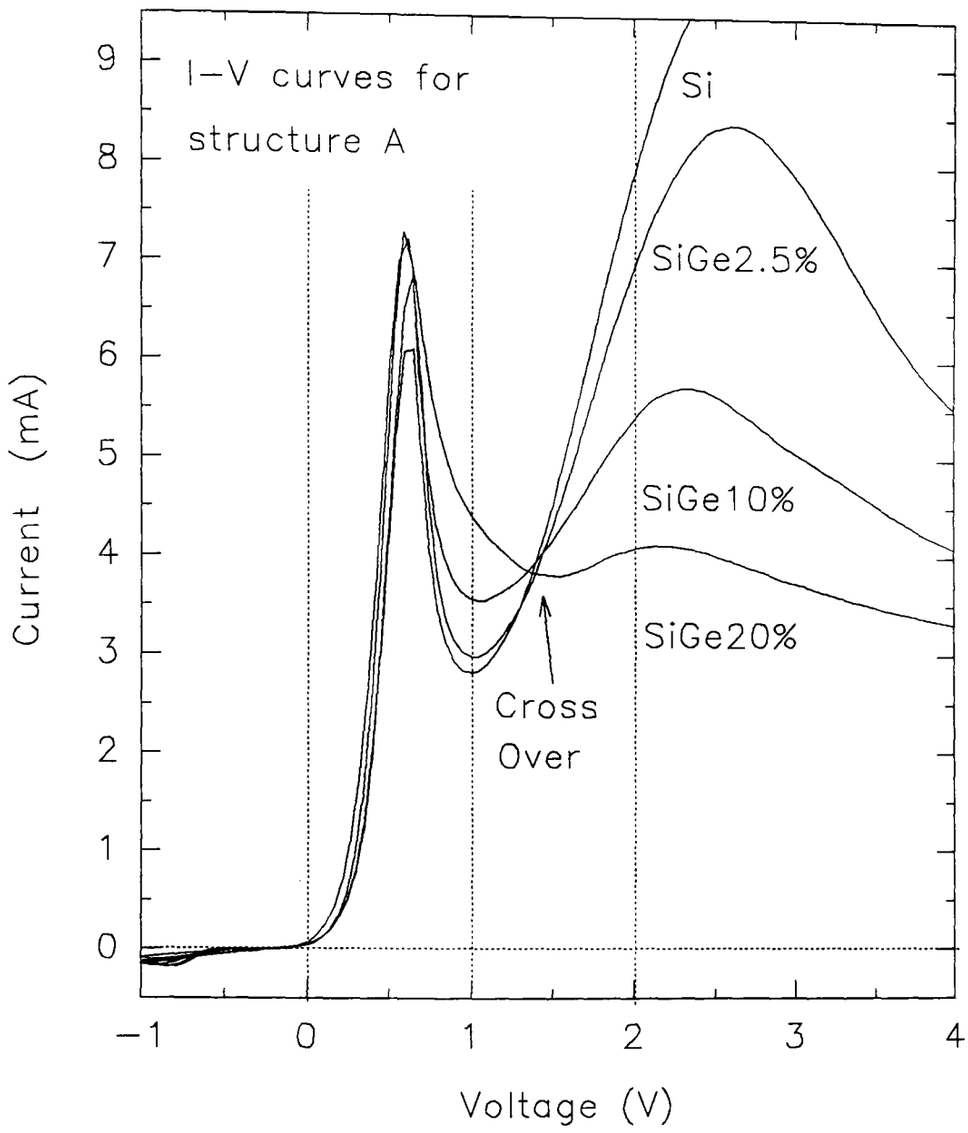

Fig. 4.7. I–V behaviour obtained from structure #14/4.

4.7. Below 1.4 V, the etch current increases slightly with Ge composition, although the dynamic range is small, and thus subject to measurement noise (see the dotted curve in Fig. 4.6(b)). Above 1.4 volts, the etch current decreases with Ge content, with an increasing dynamic range up to a voltage of 2.5 V, where a second peak is revealed through addition of Ge. Optimum dynamic range for Ge_xSi_{1-x} alloys for $x<20\%$ is thus obtained at around 2 V, as shown by the solid curve in Fig. 4.6(b).

The duration of each etch step is calculated on the basis of Faraday's law of electrolysis which integrates the charge passing through the circuit until the required total charge is attained. At an etch potential of 2 V, the etch current density shown in Fig. 4.6(b) for structure A was 8.6 mA cm^{-2} corresponding to an etch rate of 3.3 nms^{-1}. All the reported experiments were performed with an etch step of 10 nm requiring 3 secs per etch step in Si (and correspondingly longer in SiGe). Attempts to achieve higher depth resolution (<5 nm) led to increased noise due to the short duration of the etch steps which became dominated by an apparent initial current pulse at the start of each etch step. Conversely, some improvement in the stability of the Si etch current could be obtained at the expense of depth resolution. An etching potential of 2 V and etch step of 10 nm also provided good depth measurement accuracy; the indicated profile depth agreed with that measured with a surface profilometer to within ±10%.

Holes are required to promote the etching reaction. In structure A, these are provided by boron doping. In *n*-type material, holes are produced by strong illumination during etching to create electron/hole pairs. Although

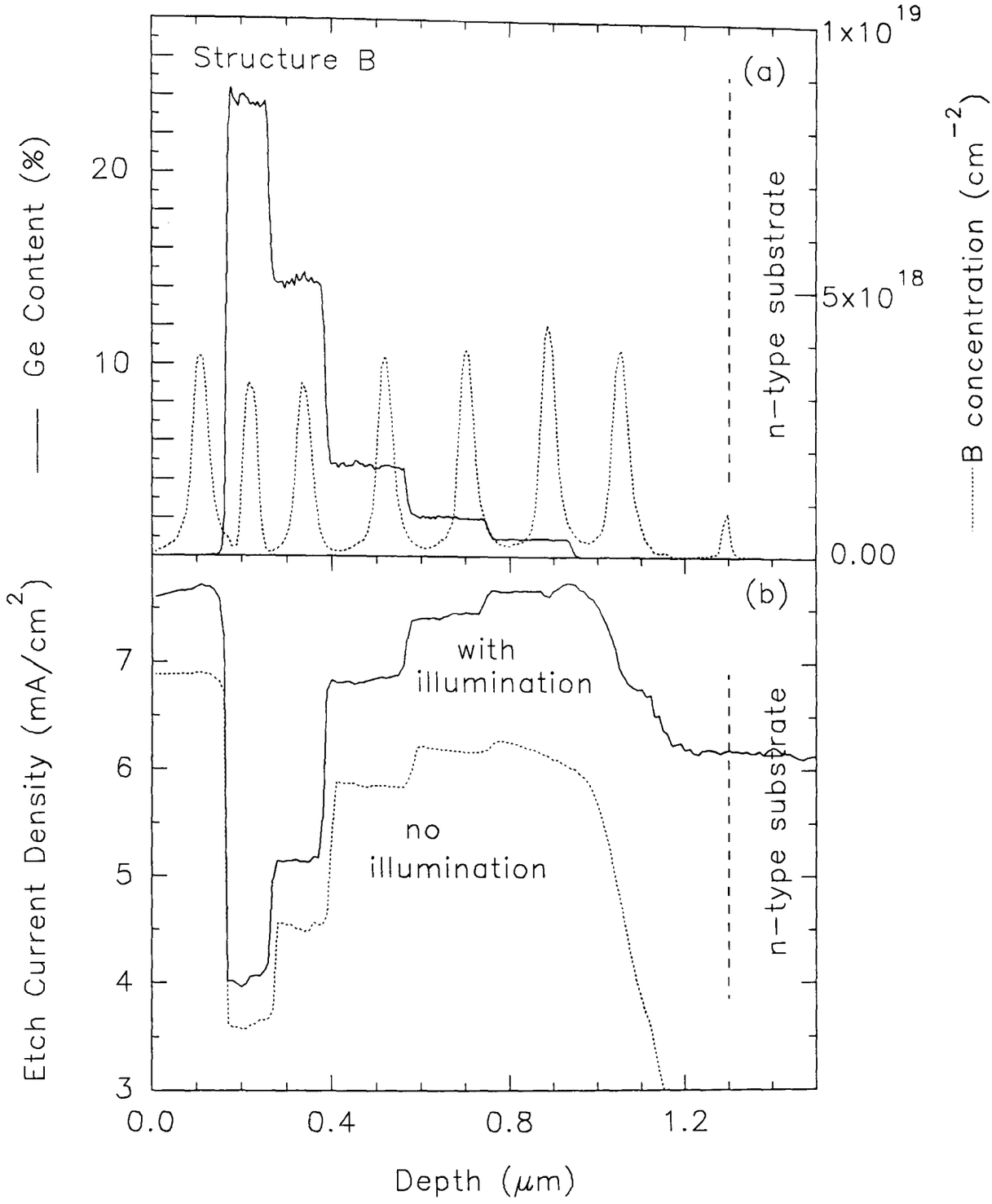

Fig. 4.8. (a) Boron and Ge SIMS depth profiles (#17/14) (b) Etch current density vs depth profiles with and without illumination at 2V.

no *n*-type material was investigated, Fig. 4.8(a) shows the SIMS Ge and boron profile for a structure (denoted structure B) grown onto an n^{++} substrate, thus including an *p-n* junction at the substrate/epilayer interface. Fig. 4.8(b) shows the etch current profile which illustrates the importance of illumination to promote sufficient hole density to maintain etching as the *p-n* junction is approached.

In addition to structures A and B, four other *p*-on-*p* (doping levels in the range $2x10^{17}$ to $2x10^{18}$ cm^{-3}), and an undoped-on-*p* Si/GeSi structures were investigated. Fig. 4.9 summarises the results as the measured change in etch current (δI_e) with Ge content over the range $0 \leq \mathbf{x} \leq 24\%$. Although all the *p*-on-*p* and undoped-on-*p* structures follow a common curve (solid line in Fig. 4.9), the *p*-on-*n* structure B (dotted line in Fig. 4.9) yields a different behaviour, even remote from the *p-n* junction and at the high Ge concentrations. It is likely that this difference is due to differences in equivalent circuit parameters measured for *n*- and *p*-type material, and is clearly illustrated in Fig. 4.8(b) in the difference in etch current in *p*-type Si (8.7 mA cm^{-2}) and n^{++} Si (6.2 mA cm^{-2}) in the substrate.

For the *p*-on-*p* and undoped-on-*p* structures, the correlation between δI_e and **x** lies within the indicated error bars, determined by the SIMS-assessment of **x**, as discussed above, and the spread in δI_e as measured from the profiles (see Figs. 4.6(b) and 4.8(b)). Other factors may also influence δI_e, most notably doping level. In Si structures, we observed a difference in δI_e of 0.5mA cm^{-2} between $2x10^{17}$ and $1x10^{19}$ cm^{-3}. However, in this work, the effect of the doping concentrations (up to $2x10^{18}$ cm^{-3}) is not

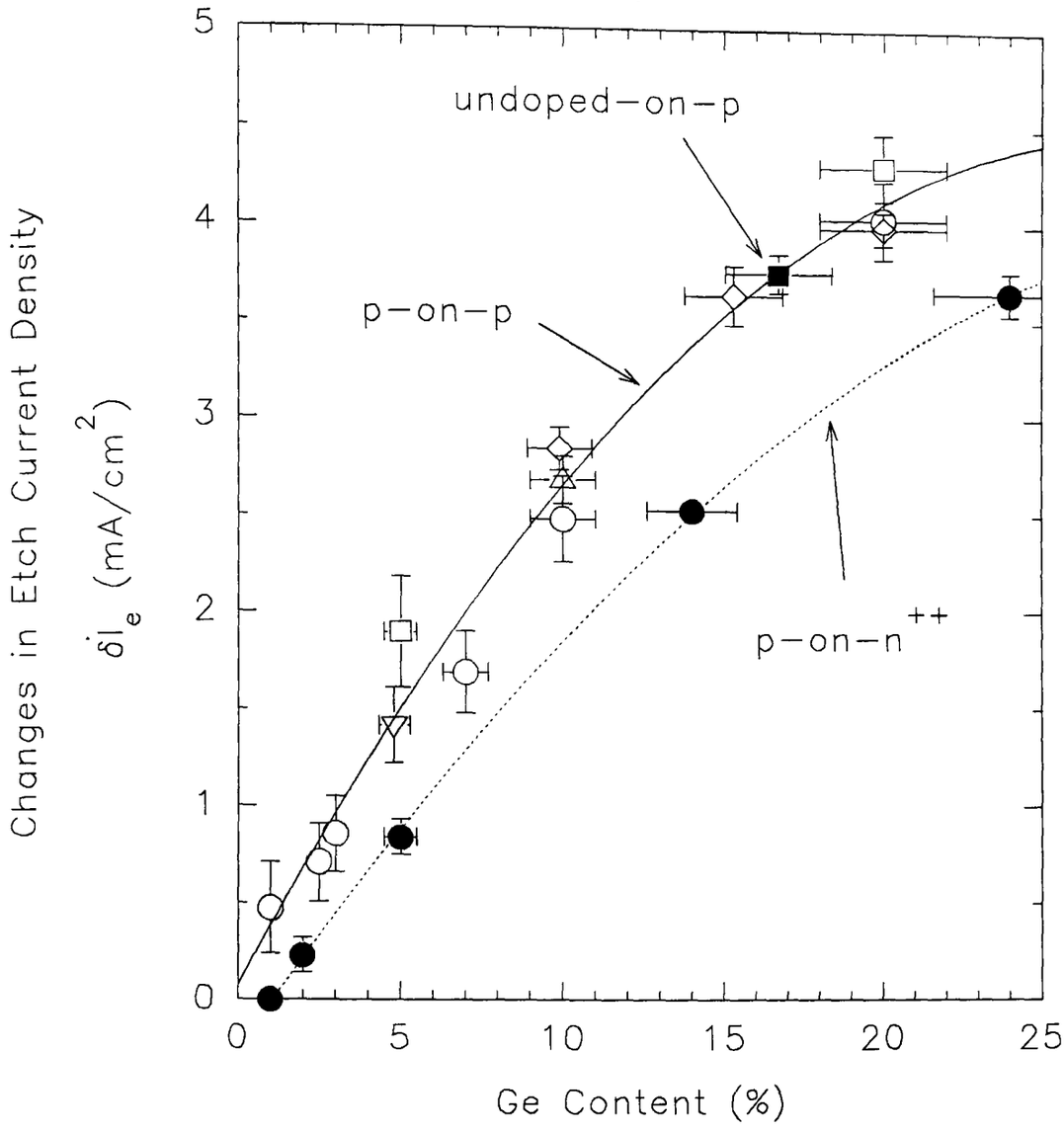

Fig. 4.9. Changes in etch current density as a function of Ge content obtained from various structures.

discernible, as indicated by the consistency of the undoped GeSi structure (filled square in Fig. 4.9), and the absence of modulation of etch current in Figs. 4.6(b) and 4.8(b) with Boron doping profile. Further evaluation of the influence of doping and other experimental factors (reproducibility of etch, measurement temperature etc.) is required. Nevertheless, these preliminary experiments indicate that the Ge content can be determined by anodic dissolution to an accuracy of ±15% of measured x. The solid line given in Fig. 4.9 was obtained by a second order regression of all the data on *p*-type substrates and gives measured change in etch current as

$$\delta I_e = aX^2 + bX + c \qquad \text{(mA cm}^{-2}\text{)}$$

where X is the Ge fraction as percentage (below 25%), $a=-5.59\times10^{-3}$, $b=3.14\times10^{-1}$ and $c=7.57\times10^{-2}$.

4.6 CONCLUSIONS

ECV investigations were carried out on Si/GeSi heterostructures containing boron spikes at fairly high doping levels with Ge concentrations below 25%. Because structures also involved Si, the electrolytes E1 and E2 were employed. The ECV profiles were compared with the SIMS profiles and a SR profile and good agreements were obtained. The structures chosen had doping levels below 2×10^{19} cm^{-3} to enable comparisons. For example at highest doping levels, ECV measurements indicated complete activation of boron in Si and $Ge_{0.2}Si_{0.8}$ layers consistent with the earlier work given in the

previous chapter. It was also shown that ECV profile were more quantitative than SR profile particularly with regard dopant incorporation behaviour. Minimum etch steps that can be achieved are 2.5 and 5 nm for the electrolytes E2 and E1 respectively. No particular difference between two electrolytes was observed for profiling SiGe, nevertheless electrolyte E2 gave higher resolution compared to the electrolyte E1 which has a higher etch rate.

ECV showed that the areal density of boron spikes in GeSi as determined by SIMS needs to take into account significantly different boron ion yield between Si and the GeSi alloy since boron levels were calibrated in both Si and GeSi using boron implanted Si standards under the same conditions.

Schottky barrier *I-V* behaviours of Si and GeSi layers reveal a small shift suggesting that the measurement voltage for Si is not ideally suited for GeSi layers. The increased leakage current leads to an error in carrier concentration. This small shift can be increased by choosing a mixture of electrolytes and this enabled Ge concentration depth profiles to be carried out using etch current density changes. It was found that a mixture of 1M NaF/0.2M $NH_4F.HF$ fulfils the criteria for composition profiling by exhibiting uniform etching characteristics and high sensitivity to Ge content. Optimal dynamic range in etch current for $0< \mathbf{x} <25\%$ was obtained at an etch voltage of 2V. The technique may also be applicable to III-V materials.

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CHAPTER FIVE

GROWTH ASPECTS AND ANALYSIS OF 2DHG SYSTEM

5.1 INTRODUCTION

Materials and growth-related phenomena can have a large impact on the physics of semiconductor heterostructures. This chapter reports experimental optimisation studies of the growth methodology carried out by the author to obtain high mobility two dimensional hole gases (2DHGs) formed at SiGe/Si heterojunctions. The factors which affect the quality of Si and GeSi grown by solid source MBE and characterisation of remote doped strained Si/SiGe/Si 2DHG structures are reported on.

There have been dramatic improvements in 4K two dimensional *electron* gas (2DEG) mobilities in Si grown on relaxed GeSi buffer layers in recent years with values up to $8x10^5$ $cm^2V^{-1}s^{-1}$ have been reported (Meyerson, 1995). With the observation of the fractional quantum Hall effect in *n*-channel material (Nelson *et al*, 1992, Monroe *et al.*, 1992), modulation-doped field effect transistors (MODFETs) of high transconductance (König *et al.*, 1992,

Ismail *et al.*, 1992) and electron resonant tunnelling diodes (Ismail *et al.*, 1991) utilising such high mobility $Si/Si_{1-x}Ge_x$ *n*-channels have been demonstrated and show considerable promise as Si-based heterostructure devices for high-speed digital and analogue applications.

By comparison, the best 2D *hole* gas mobilities in coherent low Ge content (≤20%) structures have for some years remained at around $4x10^3$ $cm^2V^{-1}s^{-1}$ (Smith *et al.*, 1992). This thesis reports on work performed which realises 2DHG mobilities as high as 19820 $cm^2V^{-1}s^{-1}$ at 7K. It was found that Ge concentrations ≤13% were needed to ensure minimal strain relaxation at the highest growth temperatures, with alloy layer thicknesses comparable to the equilibrium critical thicknesses. The influence of the growth temperature and development of suitable growth schedules was primarily responsible for these improvements. Analysis indicated that a reduction of interface charge scattering has resulted in achieving the high mobility in the 2DHG material. The structural effect on growth at high growth temperatures (T_s) is also examined.

5.2 PREVIOUS WORK

The achievement of the 2DHG at the interface of a $Si/Ge_{0.2}Si_{0.8}$ strained layer heterojunction was reported first by People *et al.* (1984) with the effective use of remote doping resulting in increased mobility values compared to uniformly doped SiGe epilayer material as depicted in Fig. 5.1. The structure grown on *n*-type Si (100) substrate was boron doped on both

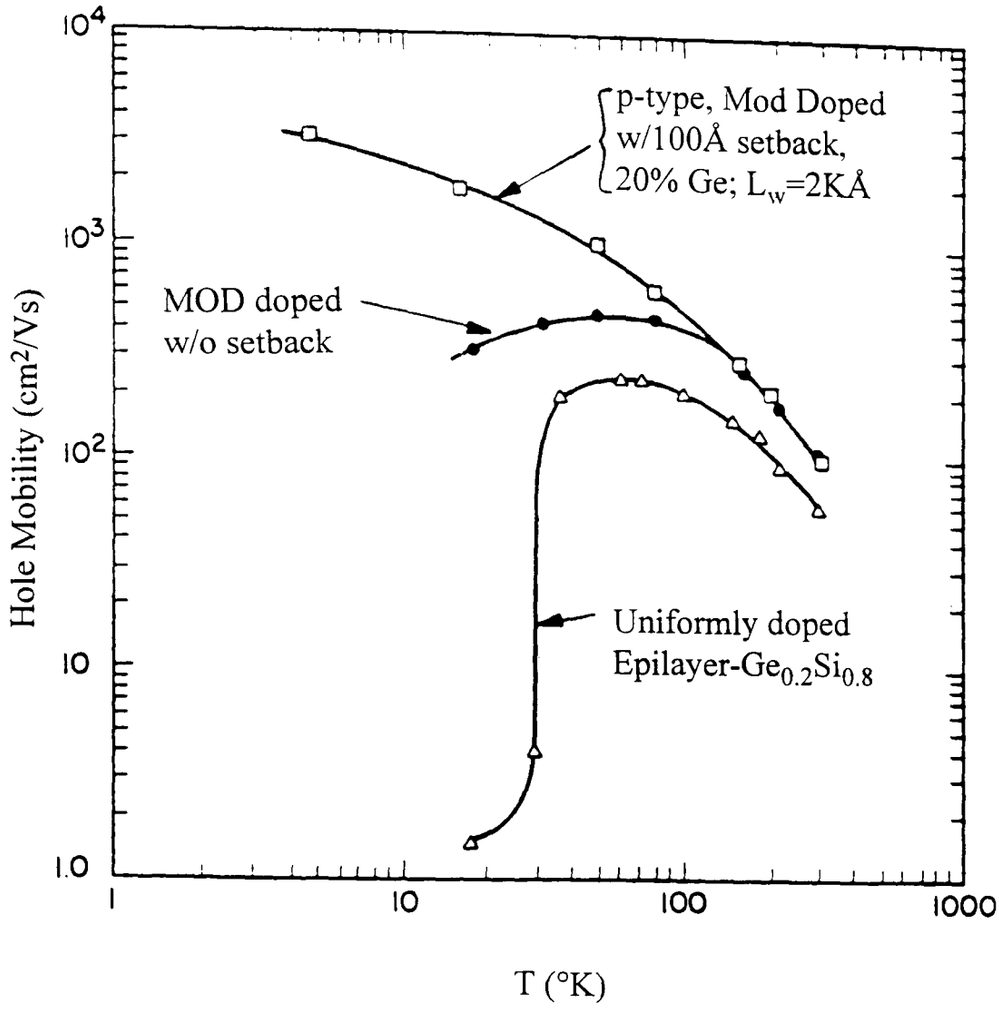

Fig. 5.1. Mobility enhancement for a 2DHG in a remote doped SiGe.

sides of the SiGe layer with undoped spacer layers of 10 nm, forming two quantum wells for holes, one at each heterointerface. The strained SiGe layers were kept below the critical thickness for the composition. Peak hole mobilities of 3300 $cm^2V^{-1}s^{-1}$ were observed at 4.2K. The effects of varying alloy thickness, doping setback and boron concentration on the low temperature hole mobility for 2DHG systems in $Ge_{0.2}Si_{0.8}$/Si selectively doped double heterostructures were also investigated (People *et al.*, 1985). Measurements on identical *n*-type structures (Ge20%) failed to provide enhanced mobility 2DEGs, which was taken as an indication that bandgap difference is mostly accommodated as a valence band offset. With the first successful fabrication of the 2D electron gas systems in $Si/Si_{1-x}Ge_x$ strained-layer superlattices, Abstreiter *et al.* (1985) reported enhanced low temperature mobilities of ~1000 $cm^2V^{-1}s^{-1}$ when the $Ge_{0.5}Si_{0.5}$ layers were doped with *n*-type impurities. They investigated a multilayer consisting of a periodic sequence of equally thick Si and $Ge_{0.5}Si_{0.5}$ layers grown on a $Ge_{0.25}Si_{0.75}$ relaxed buffer layer.

To confine the much higher mobility electrons in a 2DEG, Ge_xSi_{1-x}/Si structures must be grown such that a tensile strain exist in the Si layers. Along with a significant conduction band offset, such structures will have a high threading dislocation density due to the relaxed buffer layer. Introducing a graded Ge concentration buffer layer provided dramatically reduced density of dislocations in the 2DEG regions (Mii *et al.*, 1991). Using this technique, a two decade increase in electron mobility to $1.7x10^5$ $cm^2V^{-1}s^{-1}$ at 1.5 K was reported by Schäffler *et al.* (1992). A different strain relief method has been recently suggested for the SiGe layer to be relaxed without the generation of

threading dislocations within the layer by depositing SiGe on an ultra thin Si on insulator substrate with a superficial Si thickness less than the SiGe layer thickness (Powell *et al.*, 1994).

Until now, the improvements in 2DEG structures have not been repeated on 2DHG structures. Studies on SiGe 2DHGs with rather low mobilities have been reported by a number of groups, using different growth techniques. In these studies, no significant Ge segregation was reported. However, using solid source MBE Mishima *et al.* (1990) observed boron surface accumulation affecting the undoped spacer layer thickness and hence hole densities in the well. 'Normal' structures would not be influenced by such effects whereas 'inverted' ones would be.

Wang *et al.* (1989 a,b) grew *p*-type double modulation-doped heterostructures with x=0.12 and 0.15 by UHV-CVD technique and a hole mobility 3700 $cm^2V^{-1}s^{-1}$ at 14 K was obtained for heterostructures with x=0.12 at a sheet carrier concentration of $8x10^{11}$ cm^{-2}. Investigations of single modulation-doped heterostructures (x=0.2) by SIMS indicated that boron segregation degrades the symmetry of the normal and inverted interfaces resulting in a higher carrier mobility in the normal structure than in an inverted structure. The MBE samples doped *p*-type using a heavily boron doped Si slug. Hole mobilities of 6000 $cm^2V^{-1}s^{-1}$ at 2 K and 3800 $cm^2V^{-1}s^{-1}$ at 6 K were realised in normal structures with a sheet density of $1x10^{12}$ cm^{-2}. Single and symmetrical double 2DHG heterojunctions were also investigated on RT-CVD grown structures obtaining similar peak mobilities of about 2500 $cm^2V^{-1}s^{-1}$ with a sheet density of $5x10^{11}$ cm^{-2} at liquid helium temperatures

(Venkataraman and Sturm, 1991). The normal and inverted modulation doped interfaces in this case showed similar characteristics, indicating negligible dopant segregation. In an MBE-grown normal structure, a hole mobility up to 4300 $cm^2V^{-1}s^{-1}$ at a carrier concentration of $3x10^{11}$ cm^{-2} at 1.5 K (x=0.23) was reported (Nützel *et al.*, 1992). They also showed a dependency of mobility on growth temperature over the range of investigation (300 - 450°C) for the superlattice structures but no influence for the single alloy layers. (See also Fang *et al.*, 1992).

Initial investigations on normal and inverted structures at Warwick resulted in poor mobilities behaving quite differently at low temperatures from those reported by the previous groups. Analysis showed that the vanishing mobility on approaching T=0 K could be due to strong localisation of the holes as a result of excessive levels of interface charge and roughness (Emeleus, 1993). In general it was not possible to obtain reproducible transport results from nominally identical samples, which was taken to indicate the presence of some randomly varying parameter in the growth. Growth interrupts of a few minutes duration before and/or after growing the spacer layer were then introduced aimed at reducing background doping in the quantum well region. Transport properties showed that the sample with a single growth interrupt, sited 8 nm from the edge of the 2DHG in the spacer layer, had a non-vanishing mobility at low temperatures. Nevertheless 2DHG mobilities at liquid helium temperatures were less than $1x10^3$ $cm^2V^{-1}s^{-1}$.

SIMS analysis demonstrated that Cu was present in the SiGe channel for the sample with no growth interrupt but it was gettered from the channel

and resided mainly in the boron doped Si region if an interrupt was used (Smith *et al.*, 1992). Introducing a Si liner for the 2-in. Ge charge in a water-cooled Cu hearth provided further improvements with reproducible higher mobilities and SIMS profiles indicated Cu levels below the detection limit ($1x10^{17}$ cm^{-3}) throughout the structure. It was also found that increasing growth temperature from 520°C to 640°C resulted in an enhancement of mobility from 1250 $cm^2V^{-1}s^{-1}$ to 3650 $cm^2V^{-1}s^{-1}$ at 4 K. Post growth annealing showed no change in transport behaviour which indicated that growth temperature dependence is associated with growth processes, and not to solid state diffusion processes. Subsequent studies on growth temperature dependence at Warwick provided a peak mobility of 9300 $cm^2V^{-1}s^{-1}$ at a growth temperature of 850°C (Whall *et al.*, 1993). The best 2DHG mobility measured for hole gases was $1.8x10^4$ $cm^2V^{-1}s^{-1}$ at 4.2 K in pure Ge channel (Xie *et al.*, 1993). In this study, modulation doped GeSi/Si heterostructures were grown by MBE incorporating relaxed, compositionally graded Ge_xSi_{1-x} buffer layers with low threading dislocation densities (~10^6 cm^{-2}). A 2DHG mobility as high as $5.5x10^4$ $cm^2V^{-1}s^{-1}$ was also claimed, however no details were given.

5.3 INITIAL STUDIES

A variation in the quality of Si and GeSi grown at Warwick has been observed in common with other laboratories. This has been evident not only in the structural, electrical and optical properties (for example, low mobilities with poor reproducibility in 2DHG structures), but also in the material response

to processing and to characterisation and measurement methods (for example, allowing reliable, high quality Schottky barrier formation). Significant improvements in material quality and reproducibility have been obtained in the present study which was influenced by a variety of growth-related factors, including the use of liners for source materials evaporated from electron beam evaporators, the purity of source material and growth methodology (Kubiak*et al.*, 1993).

In the earlier studies, the presence of Cu in 2DHG structures was detected exhibiting very poor and non-reproducible 4K mobilities (typically ~100 $cm^2V^{-1}s^{-1}$, whereas Cu was below the SIMS detection limit of $1x10^{17}$ cm^{-3} for structures containing Si only (Smith *et al.*, 1992). The presence of Cu can be readily attributed to the use of Cu hearth of the electron beam evaporator. By replacing the Ge source with a smaller volume charge contained within a machined Si 'liner' and thereby eliminating the possibility of molten Ge coming into contact with the Cu hearth, Cu levels fell below the detection limits of SIMS and mobilities in comparable structures grown under the identical conditions increased to ~2000 $cm^2V^{-1}s^{-1}$. In the present work, to increase the volume of Ge available the use of a Si liner has recently been superseded by a pyrolytic graphite crucibles for both Si and Ge charges which acted as liners in the electron beam hearth. Adopting this procedure mobilities retained their improved values. SIMS analysis was used to measure the C levels in such structures (see Fig. 5.2). It is concluded that no additional C was introduced by the use of the liners and Cu levels remained below SIMS detection. Further work is however needed at better detection limit. However, although not affecting the 2DHG mobilities, the use of a

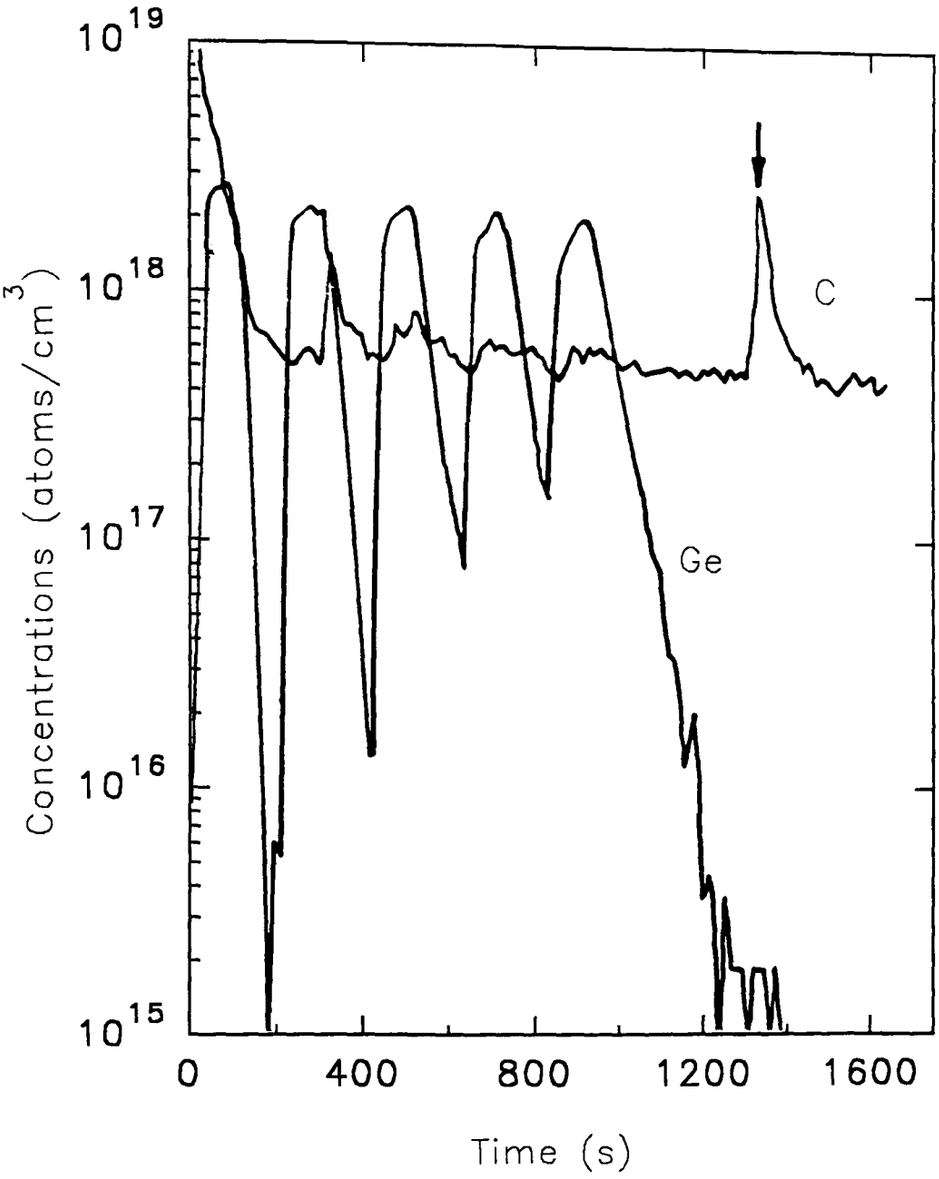

Fig. 5.2a. SIMS profiles of C and Ge in a $SiGe_{0.1}$ multilayer structure before the use of liners.

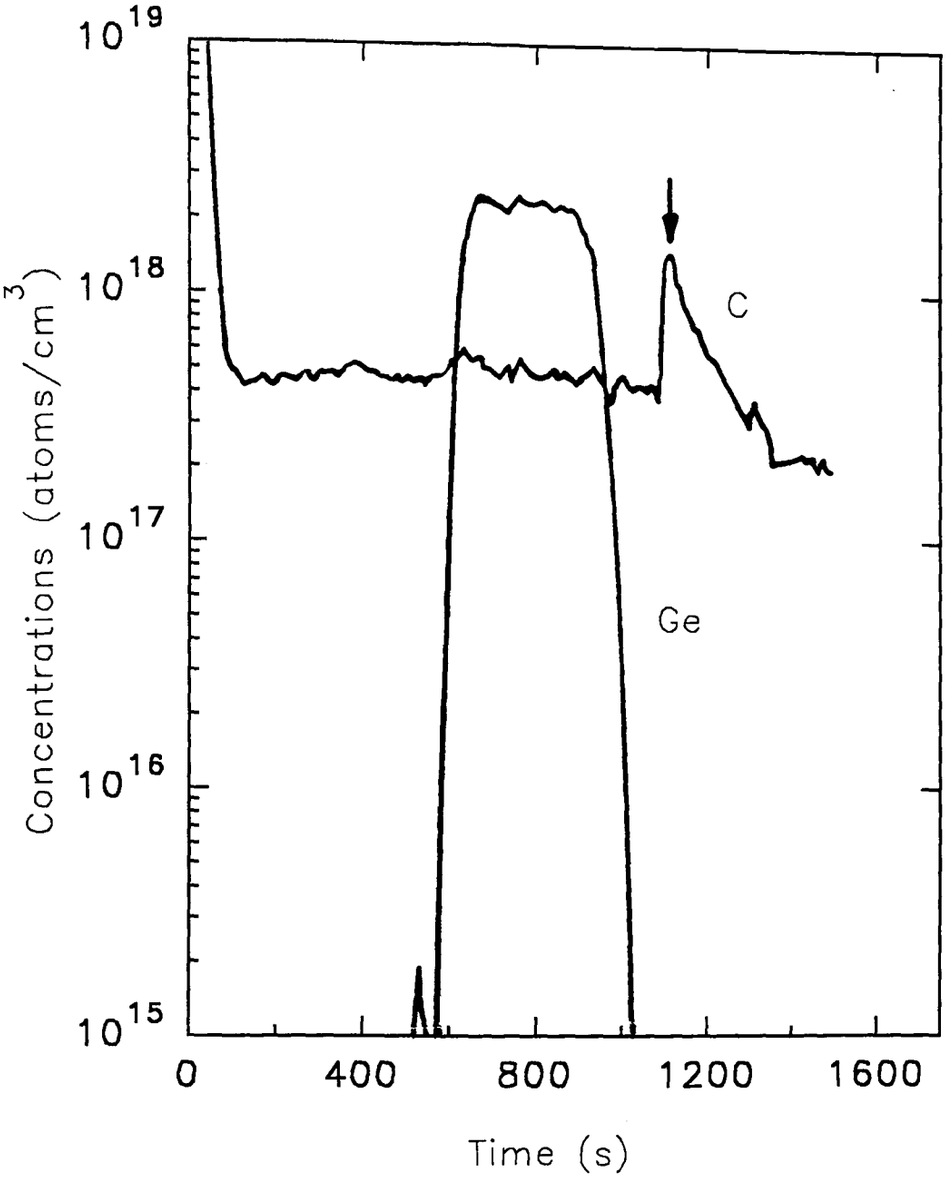

Fig. 5.2b. SIMS profiles of Ge and C in a $SiGe_{0.1}$ 2DHG structure after the use of liners.

crucible for the Si source does appear to reduce contamination levels in the Si, as was evident by the improved reliability of Ti Schottky barrier contacts (Brighton, 1993).

In this work which carried out by the present author, the resistivity and Hall measurements were performed on 56 normal Si/GeSi/Si 2DHG structures. Initial Hall measurements were carried out to elucidate the effect of growth interruptions, since these had had a dramatic effect in early studies where mobilities were poor (<1000 $cm^2V^{-1}s^{-1}$). The structures were grown at 875°C, except for the cap which was grown whilst the temperature decreased to 750°C to reduce boron diffusion. The Ge content was between 10.2% and 11.4%, SiGe layer thickness (L_{well}) was 28-33 nm, spacer layer thickness (L_{spac}) was 20-23 nm and doped capping layer thickness (L_{cap}) was 50-58 nm. Fig. 5.3 shows temperature behaviour of the hole mobility and sheet carrier concentration which demonstrates that growth interrupts now had no effect on the transport properties. It is believed that the elimination of Cu contamination has removed the need for growth interruption.

XTEM analysis of some of the structures revealed the absence of threading or misfit dislocations and that they were of high crystallographic quality with abrupt interfaces. Defect etching also confirmed very low misfit dislocation densities. X-ray rocking curves obtained using the symmetric [004] reflection were used to determine the Ge concentration in some of the alloy layers assuming the layers were fully strained. Preliminary analysis using both the symmetric [004] and asymmetric [115] reflections indicated the alloy layer in the sample #33/56 (8% Ge) was >92% strained. Although

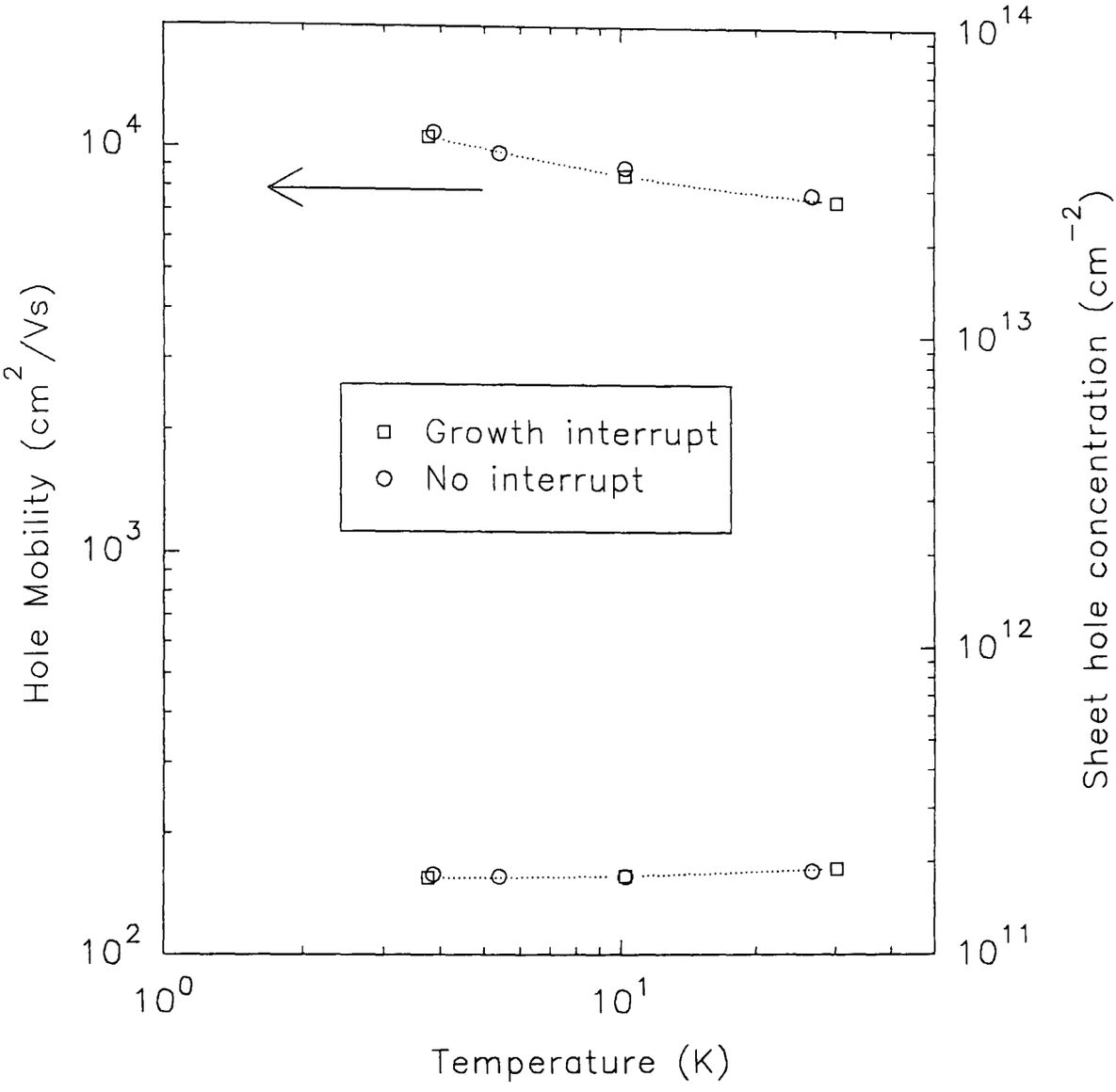

Fig. 5.3. Mobility and hole concentration data for two identical samples but one with growth interupt.

Pendellosung thickness fringes were evident in nearly all of the X-ray rocking curves, indicating sharp planar interfaces, XTEM on certain samples revealed that the upper Si/SiGe interface to be undulating with a period of between 500-1000 nm and the depth of the undulation varied up to a maximum of 20 nm. These observations are consistent with strain-related surface diffusion effects studied by Pidduck *et al.* (1992).

5.4 Ge CONTENT DEPENDENCE

Fig. 5.4 shows that mobility-temperature data exhibits a peak for the Ge concentrations below ~11% at a temperature between 5 and 20 K. The Ge concentration in the samples were 7.4% (#32/12), 13.8% (#32/13), 5% (#32/14), 10% (#32/15), 3% (#32/16) and 17.5% (#32/17) as given in the Fig. 5.4. The growth temperature was 875°C and after growing the alloy layer it was set to 750°C during the growth of the cap layer. For these structures, the intended value of L_{well} was 30 nm, L_{spac} was 20 nm and L_{cap} was 50 nm. For the samples with Ge concentrations below 11%, the mobility increased with decreasing temperature reaching a maximum and then mobility decreased monotonically down to 4 K. This kink is greater at low Ge alloys as can be seen from the Fig.5.4. The relationship between 4K mobility and sheet density was investigated by varying the Ge concentration and by keeping all other parameters constant as given in Fig. 5.5 (Ts=870°C but cap was grown at 750°C). As expected sheet hole concentration increases with increasing Ge content. For the sample containing 17.5% Ge, the unexpected poor mobility would be due to the onset of 3D growth processes or strain relaxation

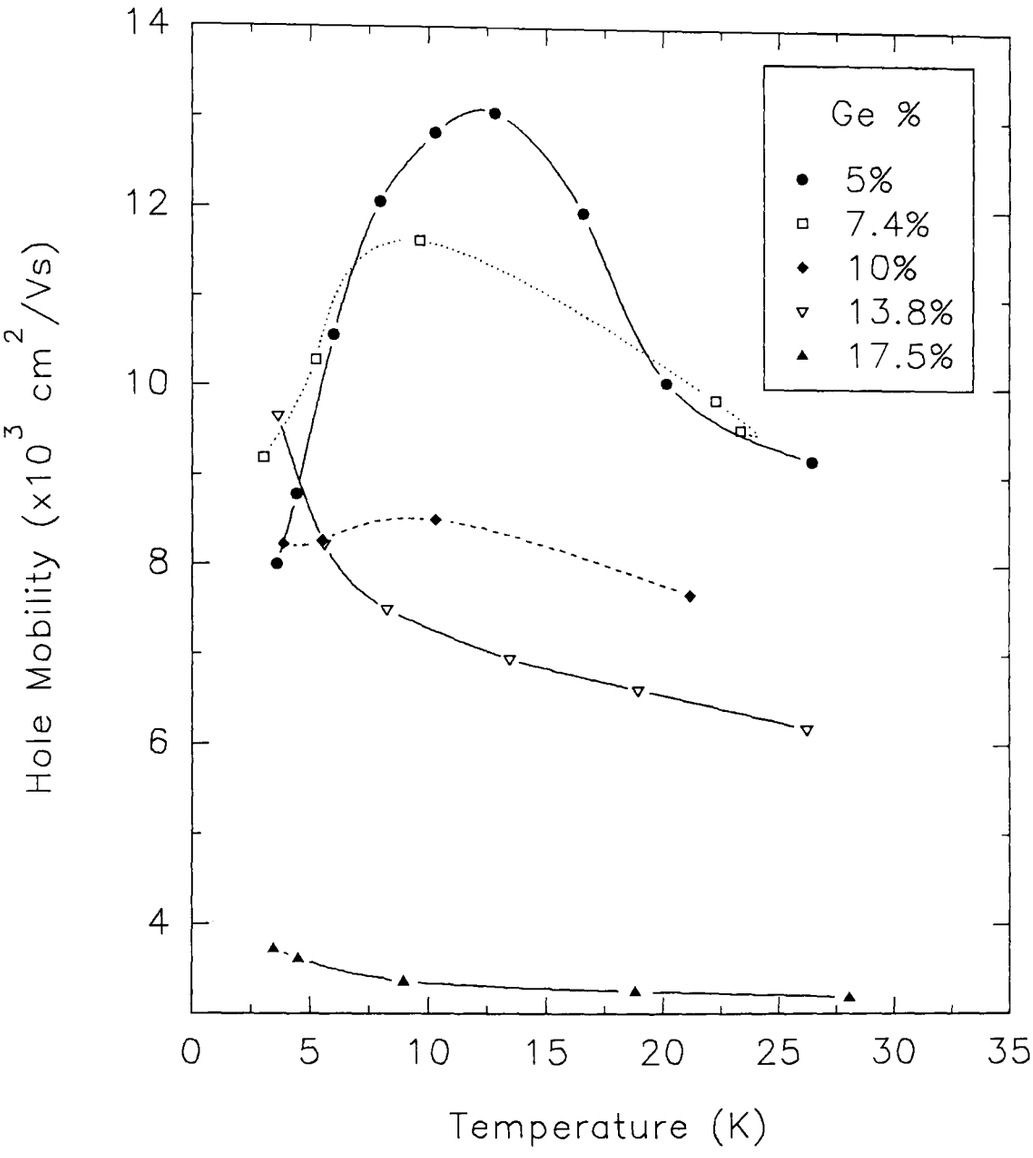

Fig. 5.4. Mobility data behaviour as a function of temperature for various Ge concentrations. All samples are nominally identical but Ge contents. (T_s=870°C but cap layer was grown at 750°C)

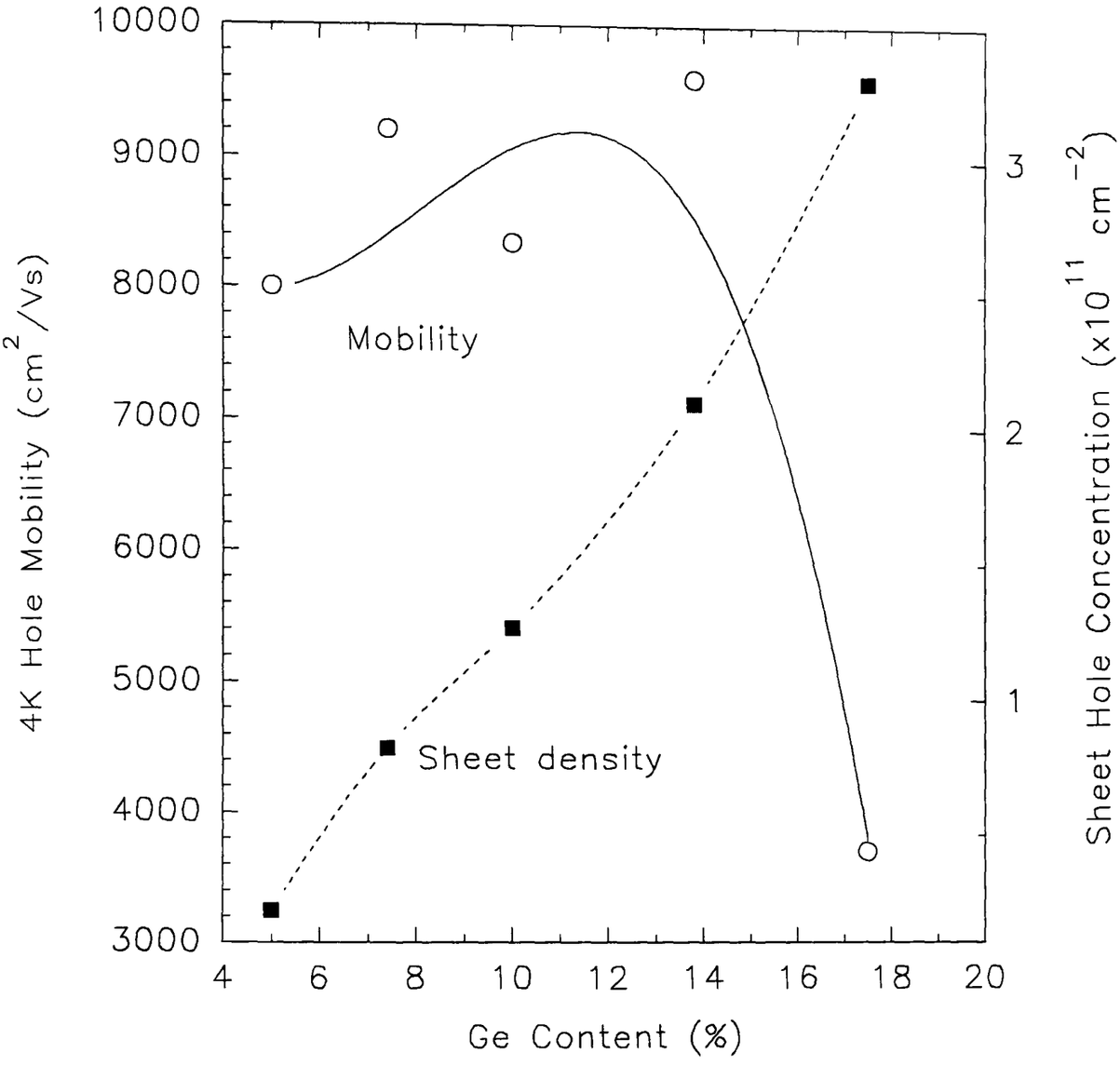

Fig. 5.5. 4K mobility and sheet density as a function of Ge concentration.

effects, but no analysis has been carried out (see Fig.1.2 in chapter 1). For this reason in the subsequent studies, the Ge concentration in the structures was kept below 14% because of the need for high substrate temperatures as explained in the following section.

5.5 GROWTH TEMPERATURE DEPENDENCE

Investigation of growth temperature dependency was carried out together with the other parameters being varied such as Ge content (but keeping this less than 14%), spacer layer thickness, alloy layer thickness and boron doping concentration. It has also been found that the cap layer temperature has implications for transport behaviour. Fig. 5.6 shows mobility dependence on temperature (in the range 3.5 to 40 K), with boron doping of $2x10^{18}$ cm^{-3} kept constant. Other parameters are given in Table 5.1. The structures (#33/15) and (#33/16) are identical but in the latter substrate temperature was set to 710°C after growing the alloy layer which resulted in enhanced mobility. When comparing with other results, it is evident that the cap temperature cannot alone explain the mobility enhancement, it is very clear that increasing the substrate temperature produces enhanced mobilities. Sheet densities for these samples at low temperatures were between $1.3x10^{11}$ and $1.9x10^{11}$ cm^{-2}. Another set of low temperature measurements are shown in Fig. 5.7 for which growth details of the samples are given in Table 5.2. The basic difference from the previous set (Table 5.1) is that the alloy layer thicknesses are reduced to half to enable retention of fully strained layer growth at higher substrate temperatures. Boron doping level for these

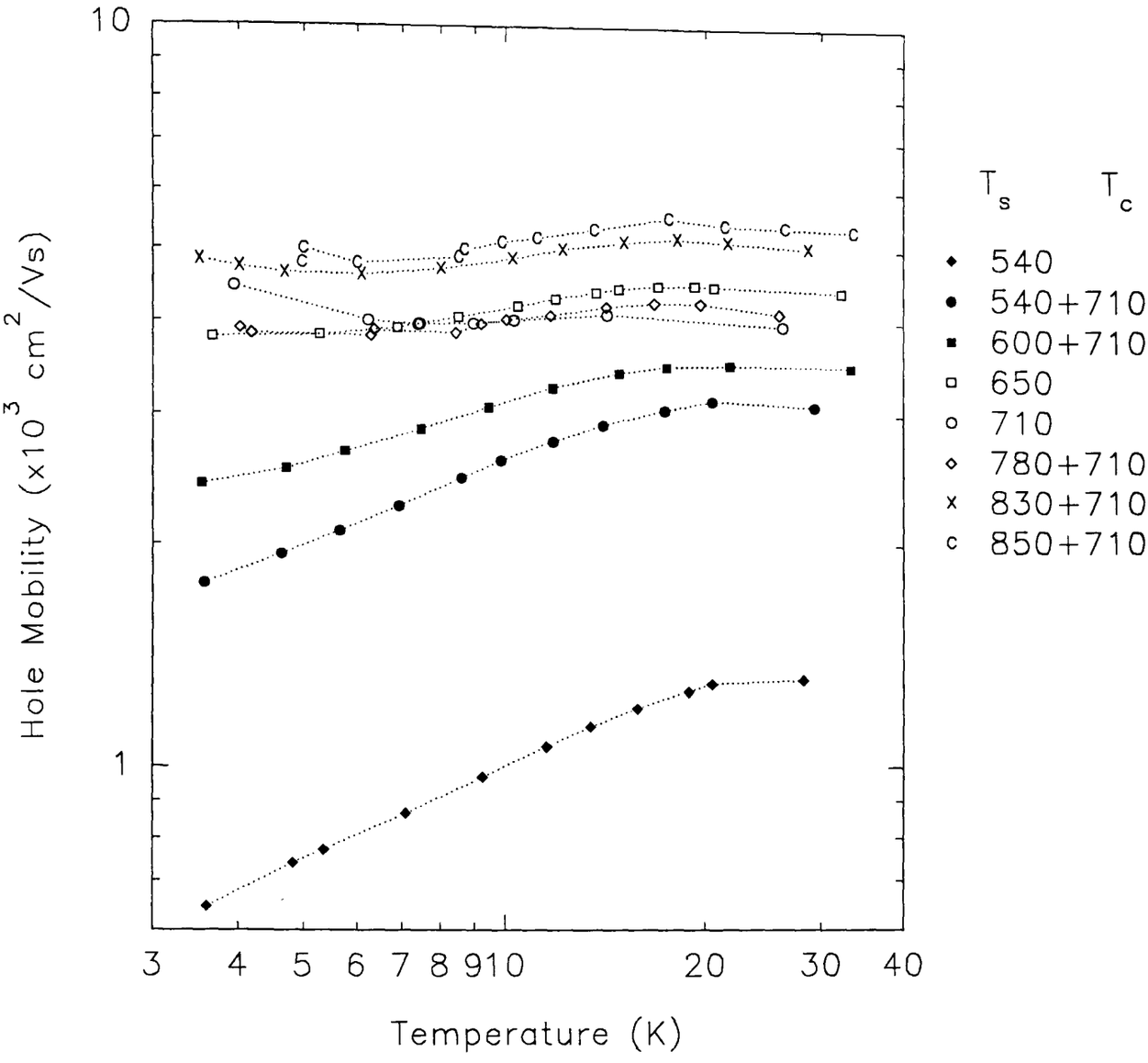

Fig. 5.6. Hole mobility dependence on temperature for the samples grown at various substrate temperatures. Details of the samples are given in Table 5.1.

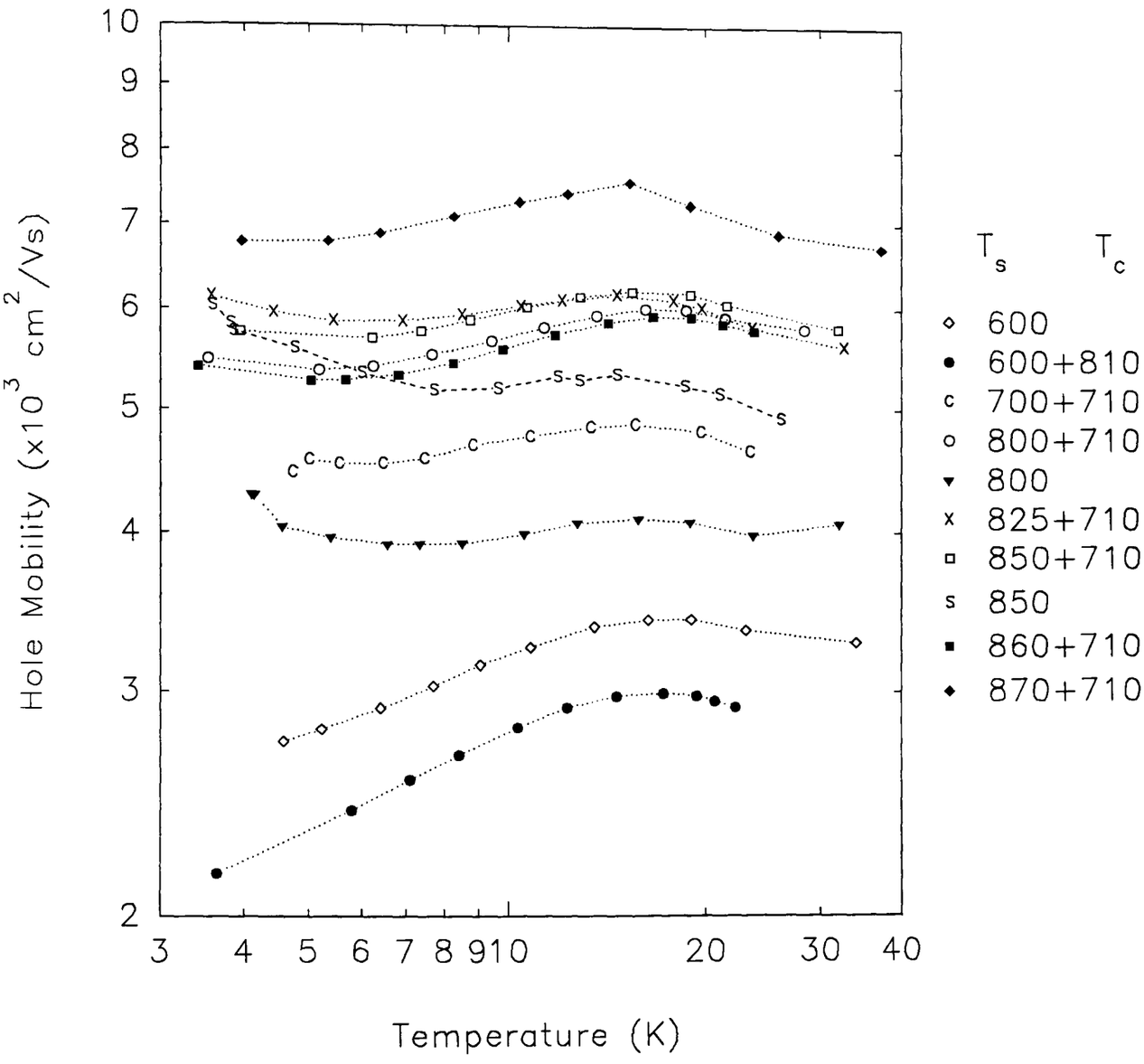

Fig. 5.7. Hole mobility behaviour of the samples grown at various substrate temperatures. Growth details are given in Table 5.2.

samples was also $2x10^{18}$ cm^{-3} except for the #33/28 and #33/29 where $5x10^{18}$ cm^{-3}. Comparisons between samples #33/21 and #33/27 (where the

ID	T_{well} °C	T_{cap} °C	Ge% ±0.5	L_{well} ±5 (nm)	L_{spac} ±2 (nm)	L_{cap} ±5 (nm)
33/5	710	710	10.8	55	22	55
33/6	650	650	10.8	55	22	55
33/7	780	710	10.8	55	22	55
33/12	830	710	10.3	61	24	62
33/13	600	710	10.3	61	24	62
33/14	850	710	10.3	61	24	62
33/15	540	540	10.3	61	24	62
33/16	540	710	10.3	61	24	62

Table 5.1. Growth details of the samples given in Fig. 5.6.

only difference is the cap temperature which increased to 810°C for the latter one) in terms of mobility resulted in opposing behaviour to that seen in the comparison between samples #33/15 and #33/16 made in the previous set. This suggests that there is a compromise for the substrate temperature of the cap layer. However an increase in the substrate temperature for the alloy layer provided enhanced mobilities as suggested for example for the samples #33/19 and #33/25 with similar sheet densities (where the only difference is the alloy layer growth temperature). Sheet densities at low temperatures varied between $1.1x10^{11}$ and $1.7x10^{11}$ cm^{-2} except for #33/28 and #33/29 where $2.3x10^{11}$ and $2.7x10^{11}$ cm^{-2} were respectively obtained.

ID	T_{well} °C	T_{cap} °C	Ge% ±0.5	L_{well} ±3 (nm)	L_{spac} ±2 (nm)	L_{cap} ±5 (nm)
33/19	800	710	10.3	30	24	62
33/20	850	710	10.3	30	24	62
33/21	600	600	10.3	30	24	62
33/22	825	710	10.3	30	24	62
33/24	860	710	10.3	30	24	62
33/25	700	710	10.3	30	24	62
33/26	870	710	10.3	30	24	62
33/27	600	810	10.3	30	24	62
33/28	850	850	10.3	30	24	62
33/29	800	800	10.3	30	24	62

Table 5.2. Growth details of samples given in Fig. 5.7.

The 2DHG 4K Hall mobilities are shown in Fig. 5.8 plotted against growth temperature (T_s). The mobility increased from 4000 $cm^2V^{-1}s^{-1}$ for a 13% alloy grown at 650°C to 17650 $cm^2V^{-1}s^{-1}$ for a 6.5% alloy grown at 900° C. To achieve the highest mobilities it was found necessary to access growth temperatures ≥890°C and to reduce the growth temperature immediately after termination of the alloy layer growth in order that the doped part of the Si cap was deposited whilst the wafer was cooling to 750°C (though it rarely achieved this temperature by the end of growth). The mobility seemed to peak sharply at growth temperatures around 900°C. The reduction in mobility for T_s > 900°C could be associated with the reduction in the effective spacer width due to the propensity of Si to planarise an undulating surface following growth of SiGe at a higher temperature, by filling in the depressions, or due to

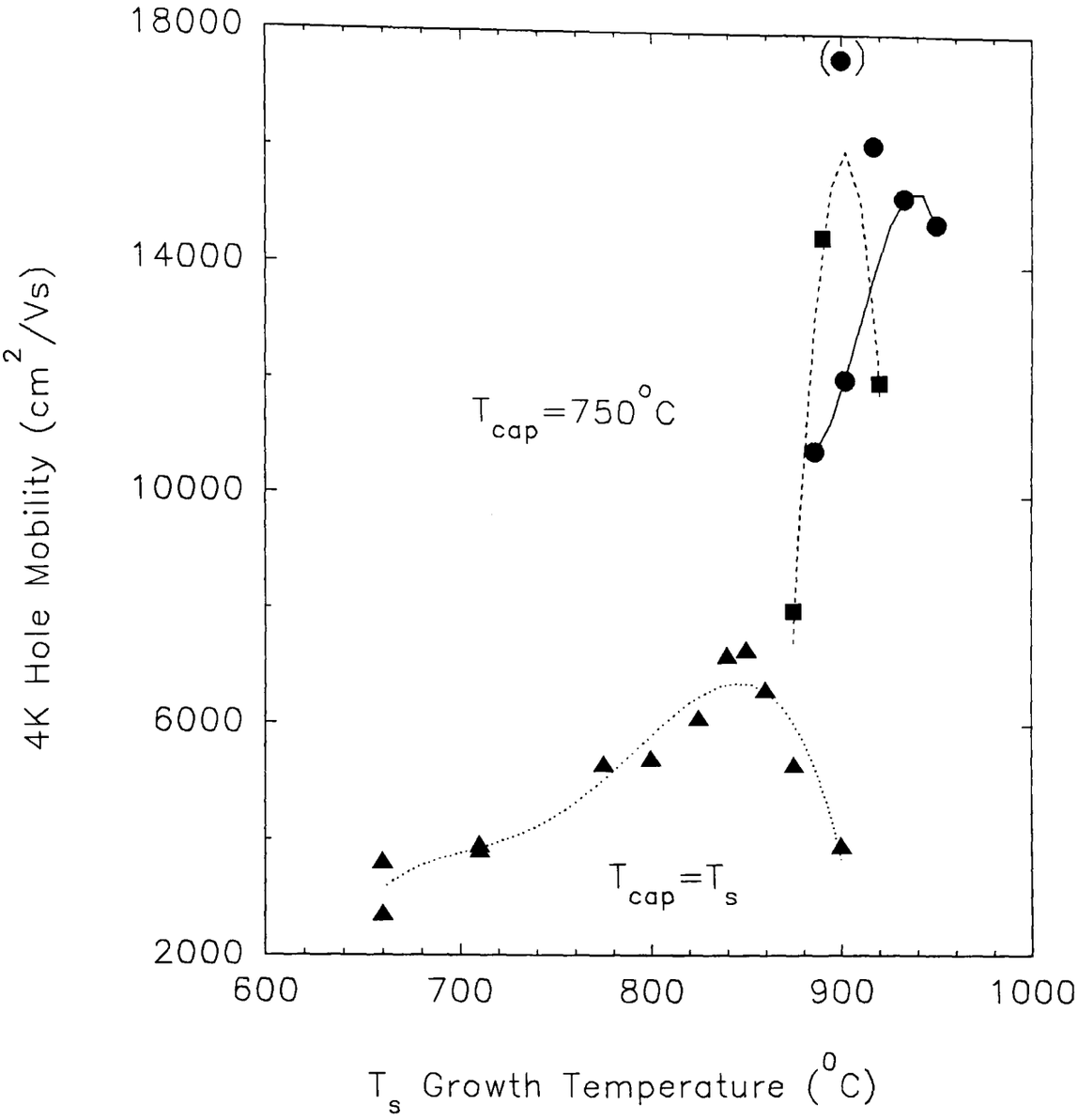

Fig. 5.8. 4K 2DHG mobilities in $Si_{1-x}Ge_x$. T_{cap} is the set temperature at which the cap layer was grown. ▲ x=0.11−0.14, L_w=50 nm, L_s=20 nm, N_s=2−4x10^{11} cm^{-2}, ● x=0.06−0.09, L_w=30 nm, L_s=20−40 nm, N_s=4−10x10^{10} cm^{-2}, ● x=0.065, L_w=74 nm, L_s=63 nm, N_s=4x10^{10} cm^{-2}, ■ x=0.05−0.06, L_w=30 nm, L_s=30 nm, N_s=4−12x10^{10} cm^{-2}.

boron diffusion during growth of the doped cap layer both causing onset of dominant ionised impurity scattering or due to relaxation of strain. Higher sheet densities observed in samples grown at temperatures above 900°C provide evidence to support the latter view. Diffusion and segregation are discussed in the next section.

Table 5.3 shows the measured properties of some of the layers. The highest mobility was 19820 $cm^2V^{-1}s^{-1}$ at 7K obtained for sample #33/56, which had a Ge concentration of 6.5% and a sheet density of $4x10^{10}$ cm^{-2}. Hall data obtained from an 8% alloy layer over the temperature range 4-300 K are shown in Fig. 5.9, indicating a 2DHG density of $7x10^{10}$ cm^{-2}, a 4 K mobility of 14200 $cm^2V^{-1}s^{-1}$ and a peak mobility of 16200 $cm^2V^{-1}s^{-1}$ at 9 K. Shubnikov de Haas oscillations obtained from some of the samples confirmed the 2D confinement of the carriers and gave sheet densities similar to those obtained

Sample ID	Ge Conc. %	μ (4K) $cm^2V^{-1}s^{-1}$	μ_{peak}(K) $cm^2V^{-1}s^{-1}$	μ (0.35K) $cm^2V^{-1}s^{-1}$	N_s (Hall) cm^{-2}	N_s (SdH) cm^{-2}
#31/17	13*	11100		15000	$1.8x10^{11}$	$2.05x10^{11}$
#33/55	9.1	11000			$6.8x10^{10}$	
#33/56	6.5	17580	19820 (7K)		$3.9x10^{10}$	
#34/45	8.3	16100			$6x10^{10}$	

Table 5.3. Measured properties of some 2DHG structures. * indicates uncalibrated data.

from the Hall measurements. Measurements down to lower temperatures on some of the samples show that the mobility goes through a minimum at

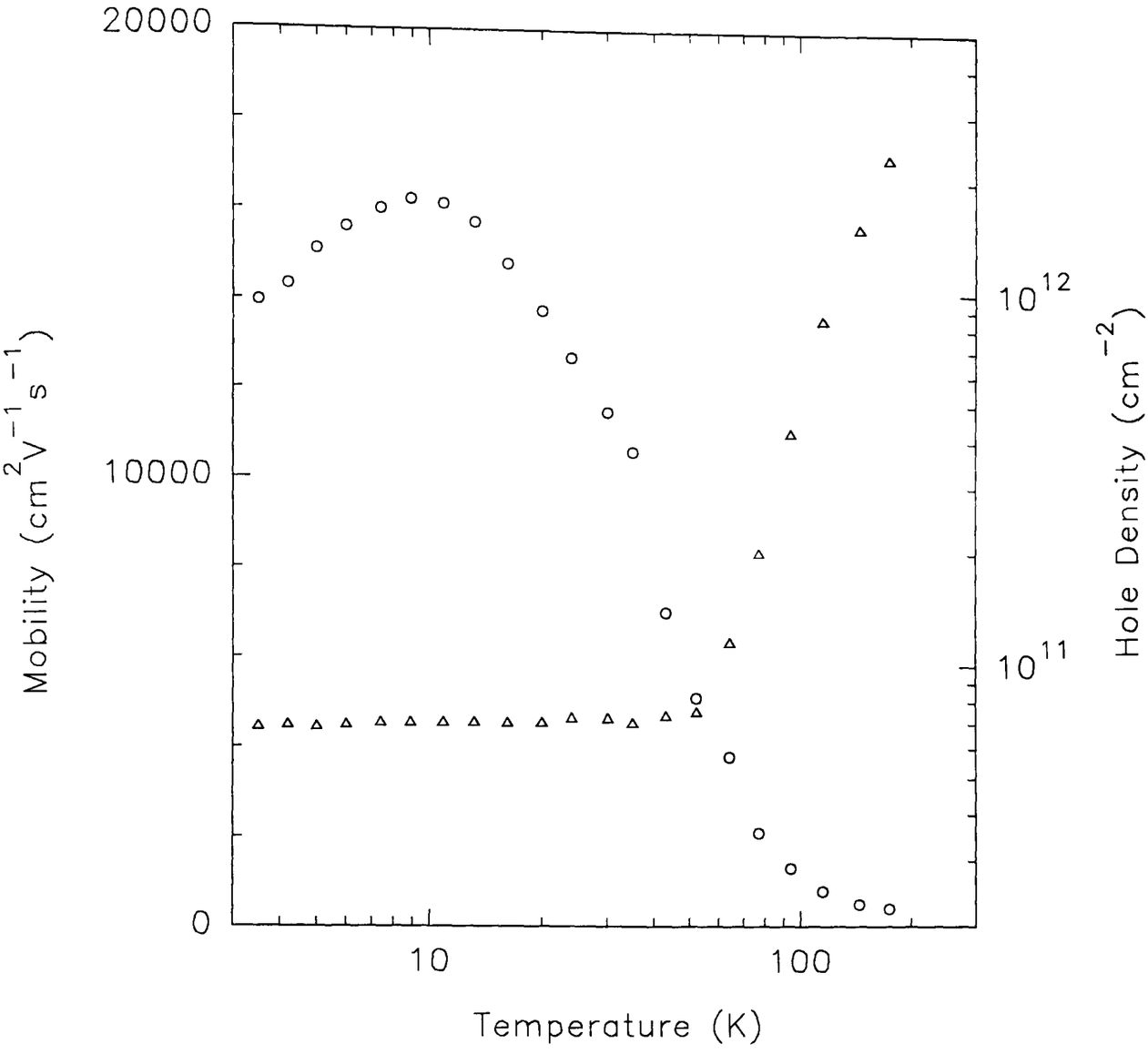

Fig. 5.9. Hall mobility (∘) and carrier sheet density (▵) vs temperature for a $Si/Si_{0.92}Ge_{0.08}$ structure.

around 3K and increases with reducing temperature to the lowest temperature (0.3 K). This temperature dependence of the mobility is similar to that which has been seen previously in GaAs/AlAs quantum wells (Sasaki *et al.*, 1987). The increase in mobility as the temperature is decreased below 3 K is attributed to an increase in screening (Emeleus *et al.*, 1993b). A relaxation time which increases with energy can account for the minimum at 3 K, followed by a maximum at around 10 K as phonon scattering becomes dominant.

5.6 DIFFUSION AND SEGREGATION EFFECTS

As explained in the previous section, samples giving higher mobilities were grown at higher substrate temperatures. However, high substrate temperatures introduces the possibility of diffusion from both sides of the spacer layer; boron diffusion from the boron doped Si cap layer and Ge diffusion from the alloy layer into the spacer layer. Both would cause a reduction in effective thickness of the spacer layer. As given in the previous section, one of the samples grown at a substrate temperature of 900°C throughout the sample resulted in a poor mobility being 3900 $cm^2V^{-1}s^{-1}$ at 4K. However, the sample grown at a substrate temperature of 950°C where substrate temperature set to 750°C after growing the alloy layer resulted in a high mobility of 14750 $cm^2V^{-1}s^{-1}$ at 4K.

At temperatures above 800°C, the primary diffusion path for boron in Si is through the positively charged point defect state (Clapper *et al.*, 1990).

Hence the boron dependence of the diffusivity can be expressed as (Loechelt *et al.*, 1993)

$$D = D_p \left(\frac{p}{n_i} \right) \qquad (5.1)$$

where p is the hole concentration, n_i is the intrinsic carrier concentration, and D_p represents the positively charged defects such that

$$D_p = F_f \, e^{-E/kT} \qquad (5.2)$$

with k is the Boltzmann constant, E is the activation energy, T is the absolute temperature and F_f is the frequency factor. By using the Arrhenius behaviour given by Loechelt *et al.* (1993), one can obtain a boron diffusion length as high as 10 nm at 900°C for 500 s (the time used to grow 50 nm boron doped Si cap at a growth rate of 0.1 nm/s). It should be remembered that some samples used in the present study contain 20 nm thick spacer layers. This suggests that boron diffuses into the spacer layer, and reducing the substrate temperature to 750°C was essential for obtaining the best mobilities.

As deposition of SiGe under normal circumstances takes place at relatively low temperatures (say 550°C), diffusion of Ge in the alloy at high growth temperatures would smear the Si/SiGe interface and reduce the mean Ge composition with the possibility of relaxation of the strain by diffusion or dislocation formation. Below 1050°C, there exists a controversy about the diffusion mechanisms (Dorner *et al.*, 1984 and Fahey *et al.*, 1989). McVay

and Ducharme (1974) reported that the effect of strain for Ge diffusion in the alloy is insignificant. However LeGoues *et al.* (1988) has found a strongly enhanced diffusion in strained layers than relaxed ones and there is theoretical support for this (Bean *et al.*, 1985). Holländer *et al.* (1989) reported that thermal annealing above 800°C results in strain relaxation and mixing due to the diffusion of Ge. The results of Holländer *et al.* (1989) indicated that the strain relaxation is due to Ge diffusion instead of generation of misfit dislocations. Strong composition dependence of the Ge diffusion coefficient in strained SiGe was reported (Baribeau, 1993). However, Karasawa *et al.* (1993) reported that the strain in the SiGe layers remain almost constant during annealing at up to 950°C for 30 min, while some misfit dislocations are formed above 800°C in samples with x>10%. Ge diffusion is negligible up to 950°C, but boron atoms diffuse considerably even for 30 min anneals at 850°C.

The literature suggests that the Ge diffusion in SiGe depends on defect density, strain and Ge concentration. Therefore, the analysis of diffusion profiles is not straightforward and different diffusion behaviour can be expected in the centre of the SiGe layer from that in the tails of the profile (Van de Walle *et al.*, 1989).

The author employed the SIMS technique to investigate Ge diffusion in a $Si_{0.75}Ge_{0.25}$/Si heterostructure (Basaran, 1990). Assuming straight Arrhenius behaviour, the diffusion coefficient was derived as

$$D = 51.2 \exp\left(-\frac{4.33}{kT}\right) \quad cm^2 / s \qquad (5.3)$$

The highest growth temperature used for the samples in this study was 900°C where the alloy layer growth took 1200s (120 nm thick with a growth rate of 0.1 nms^{-1}). The calculated diffusion length over this period evaluated from the above expression is about 1.2 nm, whilst about 1.1 nm from Holländer *et al.* (1989) and about 1 nm from Van de Walle *et al.* (1989) indicating good agreement. The highest substrate temperature used in this work was 950°C for alloy growth (with back off to 750°C during the spacer layer growth) but because the growth rate was 0.3 nm/s, a diffusion length can be estimated to be less than 1 nm.

The segregation of Ge during the growth of SiGe heterostructures by MBE has been reported by several groups over recent several years (for example see Zalm *et al.*, 1989). In order to suppress the Ge segregation, a novel growth technique was developed referred to as segregation assisted growth (or surfactant mediated epitaxy) using As (or Sb) adlayers alike (Ohta *et al.*, 1994 and references therein). The strain stability may depend on the interface abruptness and crystallinity of the SiGe layer, which varies according to the choice of epitaxial growth techniques (Karasawa *et al.*, 1993).

An important study for the present work related to the growth temperature rather than annealing was reported by Nakagawa and Miyao (1991) who studied growth temperature dependence on Ge surface segregation of MBE grown samples on Si (100) and Si (111) substrates by using X-ray photoelectron spectroscopy. The Ge segregation phenomena increased to a maxima at around 450°C in the case of the Si (100) substrates and decreased above this temperature, up to 750°C as studied. Such a

decrease in Ge segregation should enable abrupt interface for the structure as was thought to be the case in the present study. A decrease in the Ge segregation was also reported with the decrease in deposition rate.

5.7 MOBILITY LIMITING SCATTERING MECHANISMS

The interpretation of the mobility data for a range of structures with various sheet densities is shown in Fig. 5.10. Fig. 5.10 includes data on structures where the maximum 4 K mobilities were approximately 2500 $cm^2V^{-1}s^{-1}$ (Emeleus *et al.*, 1993a) and 9300 $cm^2V^{-1}s^{-1}$ (Whall *et al.*, 1993). Theoretical calculations for various scattering mechanisms as a function of carrier sheet density as represented in Fig. 5.10 have been carried out at T=0K for a 2DHG in a Si/SiGe heterostructure using the relevant expressions given in chapter 2. Calculations showed that remote impurity scattering for the mobility is completely negligible as compared with the experimental Hall mobility data. Calculations of screened alloy scattering at 0 K for 6% and 20% alloy have been made as shown in Fig. 5.10. These calculations differ from those carried out previously (Emeleus *et al.*, 1993a) in that a more accurate value of the effective mass has been used as deduced from Shubnikov de Haas measurements (Whall *et al.*, 1994a). The new calculations also employ a more accurate treatment of screening based on the work of Gold (1988). However, both the present and previous methods of calculations indicate that alloy scattering is not an important factor in any of the samples considered here. The two scattering processes which seem to be most dominant in the material, and which can account for observed dependence of mobility on

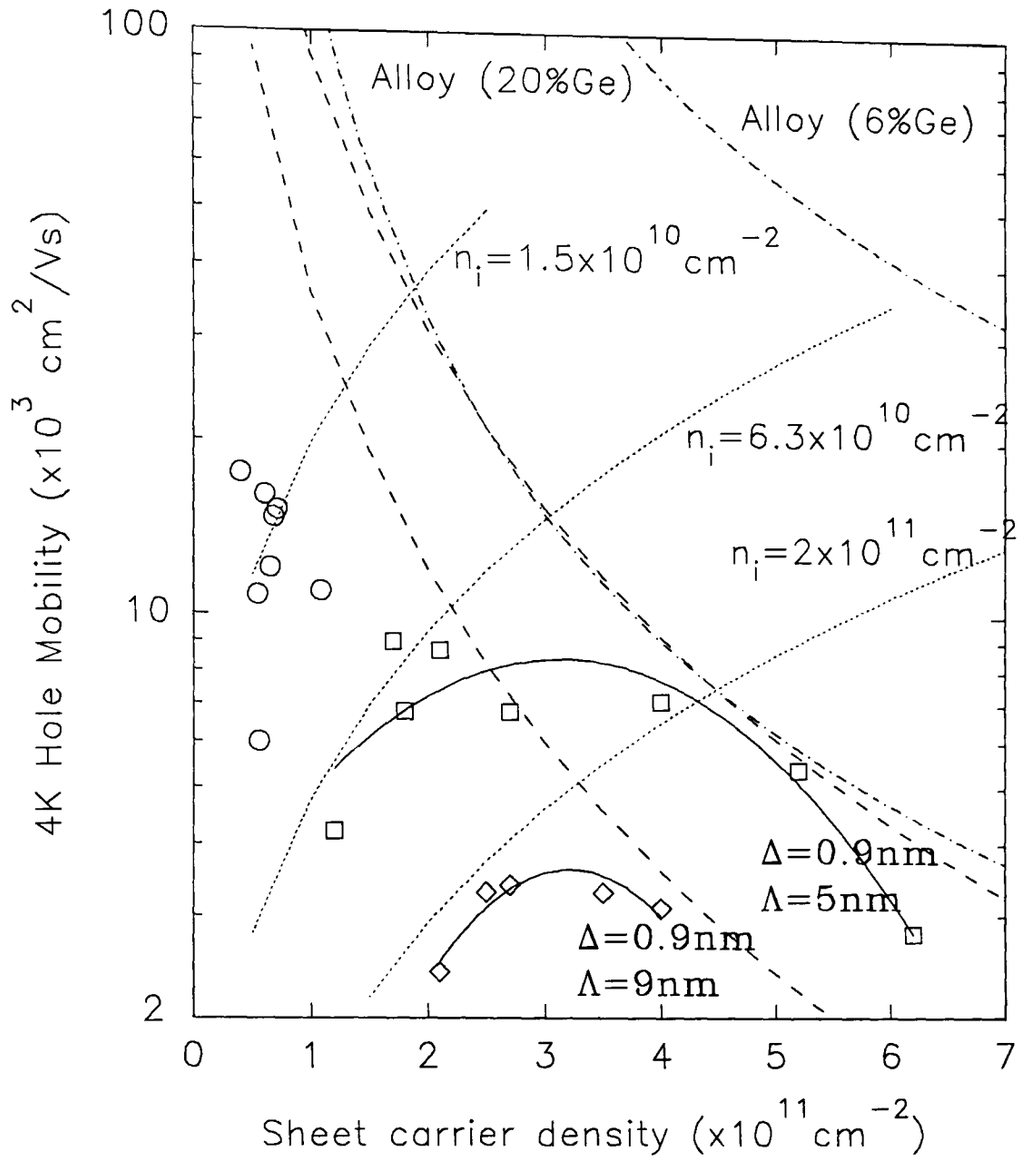

Fig. 5.10. 4K $Si_{1-x}Ge_x$ 2DHG mobility vs sheet density.

·-·-·- screened alloy scattering for x=0.06 and x=0.20 (theory),

---- short range interface roughness scattering for different correlation lengths Λ and roughness depths Δ (theory) and

····· interface charge scattering for different interface charge densities, n_i (theory).

◇ x=0.20, T_s=550–710°C (experiment),

□ x=0.13, T_s=875°C (experiment) and

○ x=0.06–0.13, T_s=890–950°C (experiment).

sheet density, are interface charge and interface roughness scattering - the former dominating at low sheet densities and the latter at high sheet densities. The interface roughness scattering calculations depend on the correlation length Λ and the depth Δ of the interface roughness and the values chosen are those which give the best fits to the data in Fig. 5.10. It should be noted that since this is a two parameter fit the choice of these parameters must be regarded as somewhat arbitrary. Insufficient XTEM analysis were carried out to deduce reliable values of Λ and Δ for the present structures. The mobility analysis indicates that for low sheet densities in the present structures ($\leq$ $1x10^{11}$ cm^{-2}) interface charge scattering is prevalent and that the primary effect of increasing growth temperatures is to reduce the density of this charge to ~$2x10^{10}$ cm^{-2}. Additional confirmation that such short range scattering was prevalent in these structures at low temperatures has been obtained from measurements of the quantum lifetime in the $Si_{0.87}Ge_{0.13}$ 2DHGs (Whall *et al.*, 1994a) (Whall *et al.*, 1994b). Considerably higher mobilities can be expected with further improvements in material quality.

5.8 CONCLUSIONS

By using the results obtained in the present work a few points may be outlined with the combination of the literature data:

Early experiments showed that the dominant mechanism was charged interface impurities at about $2x10^{11}$ cm^{-2}. The experimental studies in the present work indicated that very high 2DHG mobilities (leading to the record

mobility of 19820 $cm^2V^{-1}s^{-1}$ at 7 K) can be obtained in strained SiGe channel MBE-grown normal structures, through the use of very high substrate temperatures. It has been found that by reducing the Ge composition below 13% and limiting the thickness of alloy layer, growth temperatures can be increased up to ~890°C providing that growth temperature is reduced immediately after termination of the alloy layer growth.

The theoretical calculations related to the scattering mechanisms suggest that interface charge and interface roughness scattering limited the mobility and that utilising high substrate temperatures results in reduction of interface charge scattering.

It was found that Ge concentrations $\leq$13% were needed to ensure minimal strain relaxation with alloy layer thicknesses comparable to the equilibrium critical thicknesses and also to prevent any 3D islanding occurrence such that high growth temperatures can be employed.

The reduction in the mobility for substrate temperatures above 900°C could be associated with a reduction in the effective spacer width due to the propensity of Si to planarise an undulating surface following growth of SiGe at higher temperature by filling in the depression, and/or due to boron diffusion during growth of the doped cap layer. At the high temperatures, significant boron diffusion occurs in Si and higher sheet densities observed in samples grown at temperatures above 900°C provide evidence to support this view, whereas Ge diffusion was found to be insignificant in SiGe.

XTEM analysis of some of the structures revealed no dislocations and that they were of high crystallographic quality with sharp interfaces. Defect etching showing very low misfit dislocation densities, and X-ray rocking curve analysis indicated that layers were nearly fully strained. It seems likely that Ge segregation was not a significant factor in the growth of these layers especially for the high temperature growth, and sharp Si/SiGe interfaces were evident along with a reduction in interface charge density.

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CHAPTER SIX

CONCLUSIONS

Experimental investigations have been undertaken to determine the capability and limitations of the ECV profiling technique for carrier concentration profiling in Si and Si/SiGe heterostructures. The technique was shown to be well capable of profiling Si structures doped with boron up to the solid solubility limits, which is a new observation. Optimisation of the parameters was carried out on variety of uniformly doped structures via comparisons with Hall measurements and SIMS profiles, which differ if boron is not completely activated. Profiles of complex doping structures with severe boron accumulation were made, which suggested that incomplete activation of boron did not affect the ECV measurements. The highest concentration levels were found to influence dissipation factor. By comparison with SIMS and Hall measurements, accuracies of 30% in doping levels and 10% in depth were achieved.

Profiling of ultra thin layers including a boron delta layer was undertaken for the first time, and showed better agreement with quantitative SIMS profile than did the SR profile on both doping levels and areal densities.

All measurement conditions were optimised by a careful choice of the measurement voltage prior to etch profiles. It was found that leakage current had a significant effect on deduced doping levels and should be kept minimum. Deduction of the profile for both models after measuring the etched area and investigating the dissipation factor and flat band potential provided the necessary information on reliability of the profiles obtained. Comparisons of the electrolytes suggested that the electrolyte E2 was better suited for profiles both heavily doped Si layers due to its comparatively low series resistance, and ultra thin layers due to its slow etch rate hence providing higher depth resolution. The electrolyte E1 was successfully employed up to relatively high doping levels, however the electrolyte E3 was abandoned due to its less satisfactory Schottky behaviour.

Investigations with the electrolytes E1 and E2 enabled, for the first time, carrier concentration profile in Si/SiGe heterostructures for Ge contents below 25%. There showed better agreement with SIMS profile compared with the SR profile; for example ECV was able to detect important anomalies in depth profiles under the growth conditions for which the SR profile failed. For the structures used in this work, no difference between electrolytes E1 and E2 were realised. I-V behaviours causing a small shift between Si and SiGe layers suggested that care should be taken to choose a measurement voltage to prevent any leakage current occurring during profiling.

This shift in etching current was increased and made sensitive even to 1% Ge using an electrolyte of 1M NaF/0.2M $NH_4F.HF$, fulfilling the criteria for Ge compositional profiling. It exhibited uniform etching characteristics such

that Ge content can be obtained through changes in anodic dissolution current for 0 <x< 25%.

MBE growth optimisation studies of Si/SiGe heterostructures were undertaken through measurements of 4K mobility in 2DHG, produced by remote boron doping of the Si/SiGe heterointerface. It was shown that very high 2DHG mobilities can be obtained in the strained SiGe channel through the use of high substrate temperatures. World record mobilities were obtained up to 19820 $cm^2V^{-1}s^{-1}$ at 7K. It was found that by reducing the Ge composition to below 13% and limiting the thickness of the alloy layer, alloy layer growth temperatures can be beneficially increased up to ~900°C. Restriction of Ge and alloy layer thicknesses were needed to ensure minimal strain relaxation with alloy layer thicknesses comparable to the equilibrium critical thicknesses, and also to minimise the tendency towards 3D growth at such high temperatures. It was shown that boron diffuses faster than Ge in Si. Whilst alloy layer can be grown at such high temperatures with insignificant Ge diffusion interface smearing, it was necessary to reduce the substrate temperature during cap layer growth to prevent any significant boron diffusion. The reduction in the mobility at T>900°C was attributed to a reduction in the effective spacer width due to boron and Ge diffusion. The higher sheet densities observed in these structures provided evidence to support this view.

XTEM analysis of some of the structures revealed absence of threading or misfit dislocations and that they were of high crystallographic

quality with abrupt interfaces. Defect etching also confirmed very low misfit dislocations.

The theoretical calculations of hole scattering mechanisms suggested that the higher mobility can be attributed to a reduction in the interface charge at the Si/SiGe interface typically from $2x10^{11}$ to ~$2x10^{10}$ cm^{-2} for low sheet densities ($\leq 1x10^{11}$ cm^{-2}) and, interface charge limited mobility for $<3x10^{11}$ cm^{-2} and interface roughness scattering for $>3x10^{11}$ cm^{-2} are the most dominant mechanisms.