Analysis of Power Device Failure Under Avalanche Mode Conduction

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***Abstract*-- This paper investigates the physics of device failure during avalanche for 1.2 kV SiC MOSFETs, silicon MOSFETs and silicon IGBTs. The impact of ambient temperature, initial conditions of the device prior to avalanche breakdown and the avalanche duration is explored for the different technologies. Two types of tests were conducted namely (i) constant avalanche duration with different peak avalanche currents and (ii) constant peak avalanche current with different avalanche durations. SiC MOSFETs are shown to be the most rugged technology followed by the silicon IGBT and the silicon MOSFET. The material properties of SiC suppress the triggering of the parasitic BJT that causes thermal runaway during avalanche.**

***Index Terms*—Avalanche Conduction, MOSFET, Reliability, Silicon Carbide,**

I. INTRODUCTION

It is important for power devices to be able to conduct current in avalanche reliably without suffering thermal destruction. Some applications such as the Integrated-Starter-Alternator in automotive systems use low on-state resistance MOSFETs in avalanche mode, hence, device reliability under these conditions is critical [1, 2]. There are two avalanche conduction modes, namely static and dynamic. In the static avalanche case, the device is in the normal forward conduction mode, hence, the voltage across the device is low while the current is high. In the case of dynamic latching, both the voltage and current are high which can happen during linear mode operation and unclamped inductive switching. The current density for dynamic avalanche to occur is less than that of the static [3-5]. The ambient temperature is critical in determining the avalanche capability of the device and largely causes the device to operate less reliably as it is increased [6]. Depending on the peak avalanche current and the avalanche duration (size of the inductor storing energy), the power device will dissipate different amounts of avalanche energy reliably [7]. The avalanche capabilities of power devices will also depend on the transistor technology type as well as the fabrication material. In this paper the avalanche capabilities of 1.2 kV SiC MOSFETs, Si IGBTs and Si MOSFETs is examined. Two different circuits were used for conducting the experiments as well as several avalanche energies and ambient temperatures. In section II the experimental set up is described and the measurements are presented. In Section III, the junction temperatures are calculated and the conclusions are presented in section IV.

II. EXPERIMENTAL SETUP UP AND MEASUREMENTS

The experiments were conducted using the equipment shown in Fig.1.

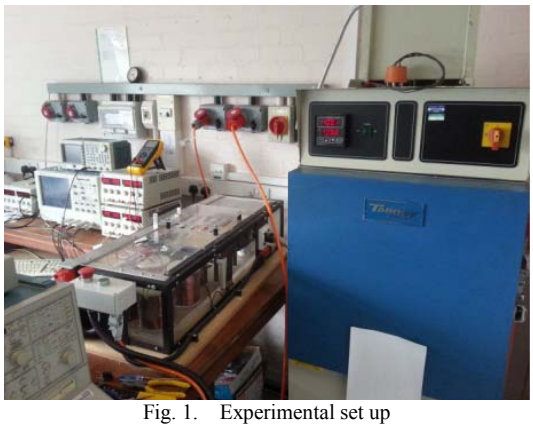

Fig. 1. Experimental set up

The experiments were undertaken using CREEs SiC MOSFET (CMF10120D), Fairchild's silicon IGBT (FGA15N120ANTD) and IXYS silicon MOSFET (IXFX20N120). All of the devices are rated at 1.2 kV and similar current ratings. The avalanche durations were modulated using 4 different inductor sizes namely 1.2 mH, 2.2 mH, 4.8 mH and 9.5 mH. The devices were placed in an environmental chamber in order to modulate different ambient temperatures and observe the impact of temperature. The tests were conducted at -25˚C, 0 ˚C, 25˚C, 50 ˚C, 75 ˚C and 125 ˚C.

Two different circuit configurations were used in the avalanche experiments. In one configuration shown in Fig. 2(a), the DUT is used to charge the inductor which means there is some initial current through the device when it is set into avalanche. In the second configuration shown in Fig. 2(b), a different higher voltage device is used to charge the inductor meaning the DUT is never switched on. In the tests conducted using the circuit in Fig. 2(a), there will be some initial junction temperature rise in the DUT due to the fact that there is some initial current in the channel of the device, hence, some conduction losses. In the experiments in Fig. 2(b), the initial junction temperature will be the ambient temperature

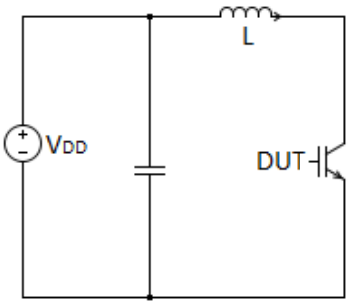

Fig. 2(a). Circuit with DUT charging the inductor

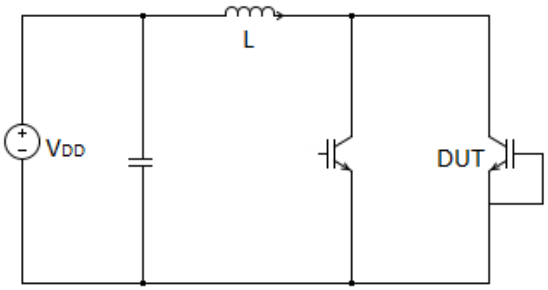

Fig. 2(b). Circuit with DUT not charging the inductor

Fig. 3 shows a typical measurement of the avalanche characteristics using the circuit in Fig. 2(a), where it can be seen that there is simultaneously high voltage across and current through the device while the inductor dissipates current into the DUT. This voltage is the breakdown voltage of the device.

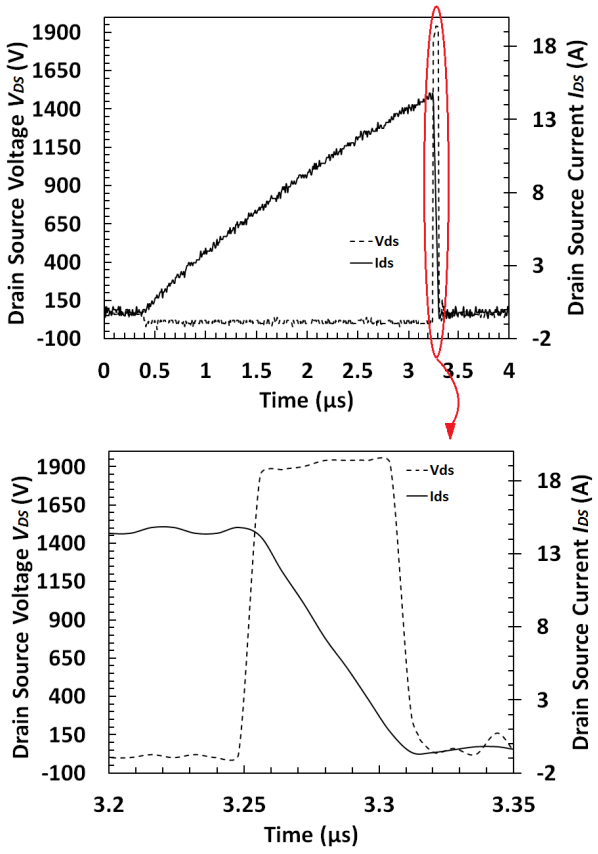

Fig. 3. Device Charging Inductor and going into avalanche

A. DUT charging the inductor (Test circuit in Fig. 2(a) i.e. DUT gate is ungrounded)

The first test was conducted using the circuit of Fig. 2 (a). The results presented in the following figures are for both the MOSFETS and the IGBTs for all the inductances and all the temperatures used. To calculate avalanche energy, the following formula was used:

$$E_{AV} = \frac{1}{2} L I_{AV}^{\ 2}$$

where E_{AV} is the avalanche energy, L is the inductance and I_{AV} is the peak avalanche current. Fig. 4 shows the calculated peak avalanche energy (prior to device failure) as a function of temperature for different avalanche durations (inductances) for the SiC MOSFET. Similar results for the IGBT are presented in Fig. 5. It can be seen that the peak avalanche energy decreases with temperature as expected because the initial junction temperature sets the headroom for the amount of energy to be dissipated.

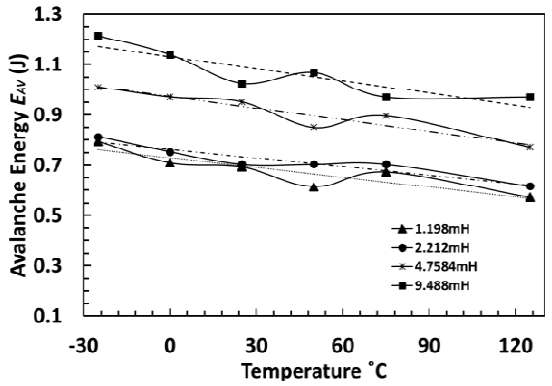

Fig. 4. Peak avalanche energy as a function of temperature for different inductances for the SiC MOSFET

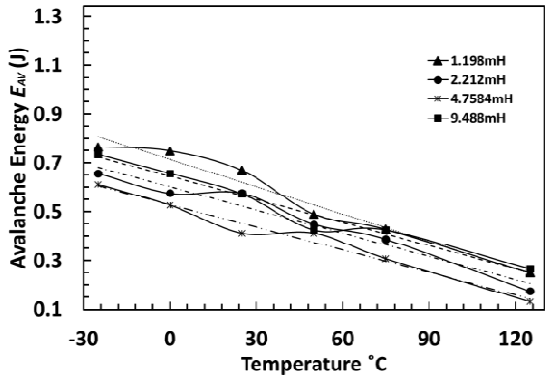

Fig. 5. Peak avalanche energy as a function of temperature for different inductances for the Silicon IGBT

From Fig. 4 and Fig. 5, it can be seen that the SiC MOSFET is capable of withstanding higher peak avalanche energy compared to the silicon IGBT and that the difference between them increases with the avalanche duration. In the case of the SiC MOSFET, the maximum avalanche energy conducted by the device increases with the avalanche duration whereas for the IGBT, the

maximum avalanche energy is somewhat less dependent on the inductances used.

There are 2 failure modes explored in the experiments. The first failure mode is low avalanche duration with higher avalanche currents while the second failure mode is low avalanche currents with higher avalanche durations. Although both tests are designed to evaluate the electrothermal ruggedness of the devices, the first test evaluates the resistance of the device to latch-up (BJT latch-up for the MOSFET and Thyristor latch-up for the IGBT) while the second test evaluates the maximum intrinsic temperature that the device is capable of sustaining. Parasitic BJT latch-up is also influenced by an unequal temperature distribution across the chip resulting from parametric variability between the cells in the power device. In the 1st failure mode, since the avalanche duration is short and there is insufficient time for the chip temperature to rise uniformly, hot-spotting will contribute significantly to device failure via BJT latch-up. In other words, the electrical time constant of the chip is much smaller than the thermal time constant so the failure mode is primarily an electrical switching mode. Hence, devices with manufacturing defects will fail this test rapidly before the chip has a chance to reach its thermal limits. In the 2nd failure mode, the avalanche duration is long enough and the initial power is small enough to allow uniform temperature rise across the chip. Hence, the thermal time constant of the chip is comparable to the electrical time constant of the switching event and the temperature limits of the device are tested. It is known that the intrinsic temperature limit of the device is reached when the thermally generated carriers due to temperature induced bandgap narrowing becomes equal to the background doping of the device. Fig. 6 to Fig. 9 shows the maximum avalanche energy dissipated prior to device failure for both the SiC MOSFET and the silicon IGBTs with different avalanche durations (inductances). The inductance used in Fig. 6 is the 1.2 mH, in Fig. 7 is 2.2 mH, in Fig. 8 is 4.8 mH and in Fig. 9 is 9.5 mH.

It can be seen that for the measurements made with the smaller inductances (Fig. 6 and Fig. 7), the difference in electro-thermal ruggedness (maximum avalanche energy prior to device failure) between the two technologies is smaller compared to the measurements made using the larger inductances. As the avalanche duration (inductor) is increased, the failure mode changes from latch-up to intrinsic temperature limitations, hence, the performance of the SiC MOSFET relative to the silicon IGBT improves. It can be seen from the measurements made using the larger inductances (Fig. 8 and Fig. 9) that the SiC MOSFET is significantly more avalanche rugged as the avalanche duration is increased. This is due to the higher intrinsic temperature capability of the device owing to its larger bandgap i.e. due to the larger bandgap, the rate of carrier generation with temperature is less for the SiC device hence, the device is more resistant to thermal runaway.

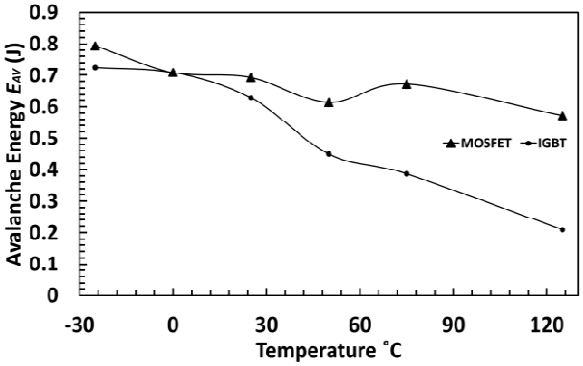

Fig. 6. Energy Comparison between MOSFET IGBT using L=1.2 mH

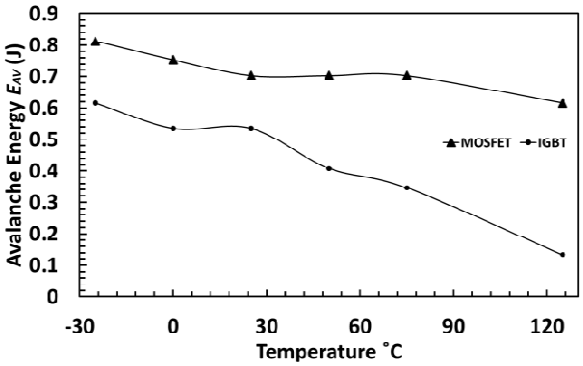

Fig. 7. Energy Comparison between MOSFET IGBT using L=2.2 mH

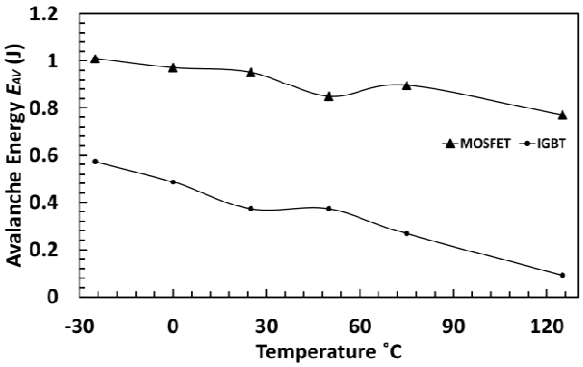

Fig. 8. Energy Comparison between MOSFET IGBT using L=4.8 mH

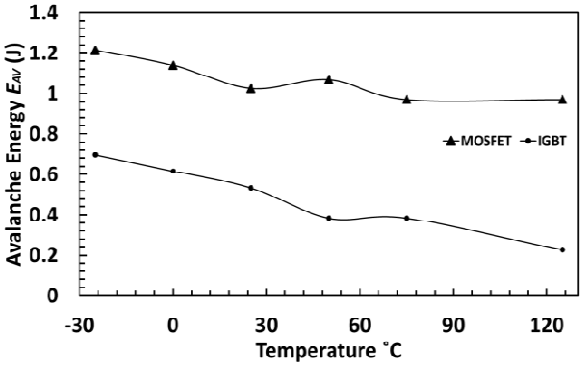

Fig. 9. Energy Comparison between MOSFET IGBT using L=9.5 mH

B. DUT not charging the inductor (Test circuit in Fig. 2(b)i.e. DUT gate is grounded)

In the second part of the experiment, the avalanche inductor was charged using a high breakdown voltage device while the gate of the DUT was grounded to the source. In other words, the DUT is never switched on. The circuit diagram used is shown in Fig. 2b. The high voltage device used was IXEL 40N400-N with a breakdown voltage of 4 kV and current capability of 90 A. Since the avalanche current will always flow through the device with the lower breakdown voltage rating, the high voltage device would not interfere with the avalanche measurements. The breakdown voltage of the device was not affected by grounding the gate. Also, the breakdown voltage difference between the silicon IGBT and the SiC MOSFET remained the same [8]. The results for the avalanche current and the avalanche energy for the MOSFET are shown in Fig. 10 and for the IGBT in Fig. 11. Fig. 10(a) shows the maximum avalanche current as a function of temperature for the SiC MOSFET using the 1.2 mH inductance. Fig. 10(a) compares the electrothermal ruggedness for the case of the DUT used to charge the inductor (circuit in Fig. 2a where the gate is ungrounded) and the case where the gate of the DUT is grounded (circuit in Fig. 2b where the DUT is grounded and never switched on). Fig. 10(b) shows a similar plot for the SiC MOSFET with the avalanche energy shown as a function of the ambient temperature. It can be seen, as expected, that the electrothermal ruggedness is higher using the circuit configuration in Fig. 2(b) where the gate of the DUT is grounded. In fact, when the gate of the DUT is grounded, the SiC MOSFET never fails so the points shown in Fig. 10(a) and Fig. 10(b) represent the limits of the test equipment as shown in the figure.

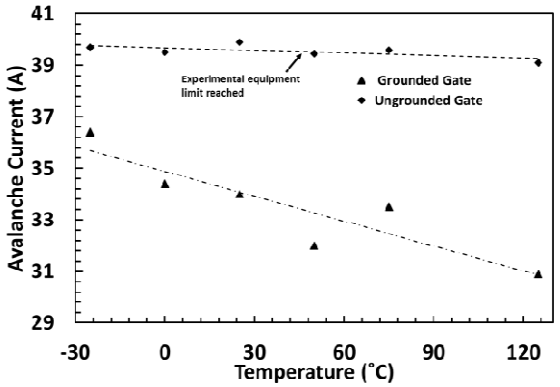

Fig. 10(a). Comparison of maximum avalanche current I_{AV} between grounded and non-grounded gate for the SiC MOSFET

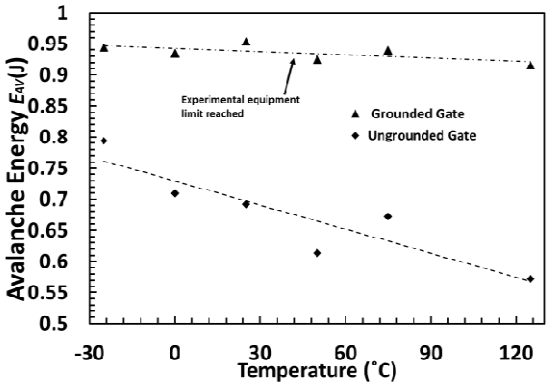

Fig. 10(b). Comparison of maximum avalanche energy E_{AV} between grounded and non-grounded gate for the SiC MOSFET

For the SiC MOSFET, it is clear that there is a major difference between the two configurations. With the gate of the SiC MOSFET grounded, there was insufficient energy to trigger BJT latch-up and thermal runaway in the device hence, the maximum avalanche energy the SiC MOSFET is capable of reliably dissipating is unknown for that particular test configuration. The limits of the test equipment were reached.

Similar results are shown for the silicon IGBT in Fig.11(a) where the peak avalanche current is shown as a function of temperature and in Fig. 11(b) where the peak avalanche energy is shown as a function of temperature. As was done for the SiC MOSFET in Fig. 10, comparisons have been made for the silicon IGBT between measurements with the ungrounded gate (using the circuit in Fig. 2a where the DUT charges the inductor) and grounded gate where DUT is never switched (Fig. 2b where another device charges the inductor). As expected, higher temperatures reduce the avalanche ruggedness performance of the DUTs. However, unlike the case of the SiC MOSFETs, there is not a substantial difference between the 2 tests (grounded gate vs ungrounded gate). In other words, using the DUT to charge the inductor does not yield avalanche ruggedness capability results that are significantly less than using a higher voltage transistor to charge the inductor.

Hence, Fig. 10 and Fig. 11 show that grounding the gate for the SiC MOSFET completely suppressed the mechanism of BJT latch-up and the devices were indestructible using the experimental set-up. However, for the silicon IGBT, grounding the gate had no impact on the mechanism of thyristor latch-up. It is thought that the material properties of SiC were key to this observation since similar measurements on 1.2 kV silicon MOSFETs showed significantly less electrothermal ruggedness for all test conditions.

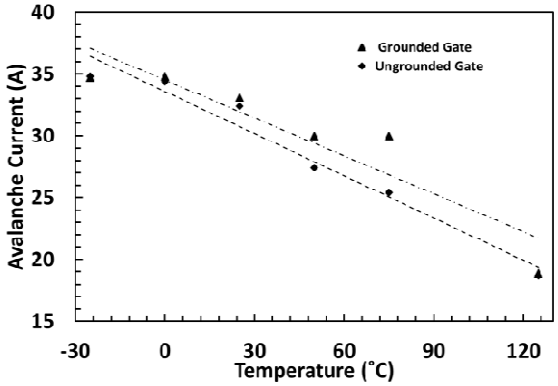

Fig. 11(a). Comparison of the maximum avalanche current I_{AV} between grounded and non-grounded gate for the silicon IGBT

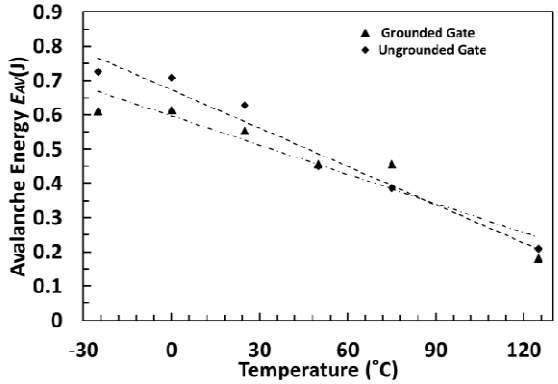

Fig. 11(b). Comparison of the maximum avalanche energy E_{AV} between grounded and non-grounded gate for the silicon IGBT

To ensure that the breakdown voltage characteristics of the DUT have been unaffected by the addition of the charging transistor, the drain-source characteristics of the DUT were monitored during avalanche for the case of the grounded and non-grounded gate measurements. The drain-source voltage characteristics during avalanche are shown in Fig. 12(a) for SiC MOSFET under both test conditions where it can be seen that the breakdown voltage does not change. Fig. 12(b) shows a similar plot for the silicon IGBT. Fig. 12(c) shows the drain-source voltage characteristics for the silicon IGBT and SiC MOSFET during avalanche where it can be seen that the breakdown voltage is higher for the SiC MOSFET and the avalanche duration is shorter. It should be noted that all the measurements are with the same inductor. The longer avalanche duration in the SiC MOSFET is due to the higher breakdown voltage.

Similar avalanche ruggedness tests have been carried out on the 1.2 kV silicon MOSFETs. Fig. 13 shows the maximum avalanche current as a function of temperature for the 3 technologies namely, the SiC MOSFET, the silicon IGBT and the silicon MOSFET all rated a 1.2 kV. In Fig. 13, all of the measurements have been carried out on the 9.5 mH inductor with the DUT not used to charge the inductor i.e. the gate of the DUT is grounded and a high voltage transistor is used to charge the inductor. From Fig.13 it is evident that the most resilient device is the SiC MOSFET followed by the silicon IGBT and the Si MOSFET. The dependency of the avalanche ruggedness capability on temperature is more or less similar between the two MOSFETs probably due to the same architecture. The silicon IGBT exhibits a higher temperature dependency with the maximum avalanche current decreasing much more rapidly as the temperature is increased. The differentiating factor between the MOSFETs capability is the superior electrothermal capability of silicon carbide.

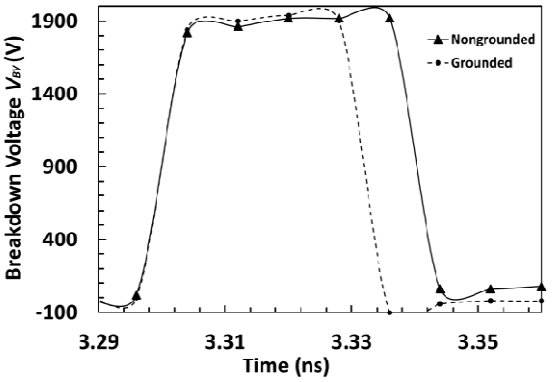

Fig. 12(a). Drain-source voltage characteristics of the SiC MOSFET during avalanche with both circuit configurations

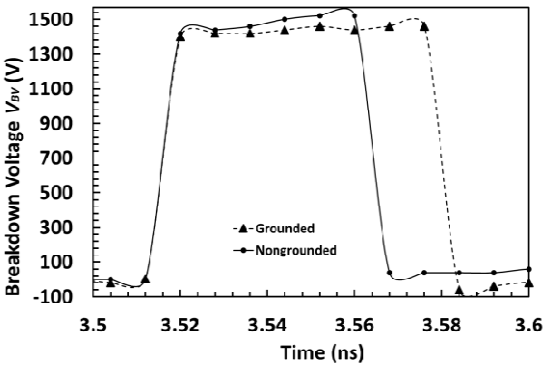

Fig. 12(b). Drain-source voltage characteristics of the silicon IGBT during avalanche with both circuit configurations

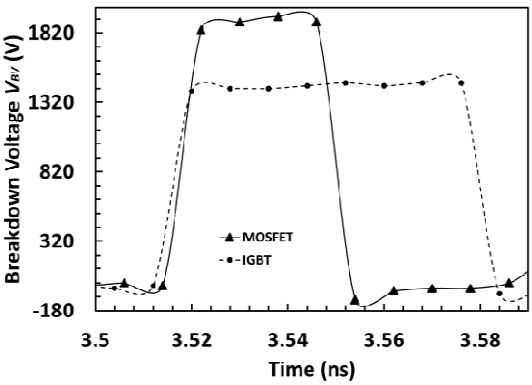

Fig. 12(c). Breakdown voltage of IGBT and MOSFET with grounded gates on both devices

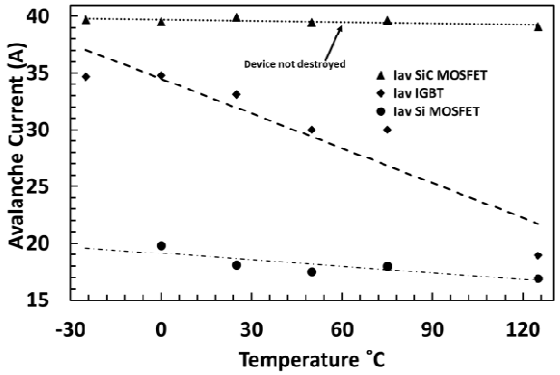

Fig. 13. Avalanche current for SiC MOSFET, Si IGBT, Si MOSFET with grounded gates

III. JUNCTION TEMPERATURE CALCULATION

Due to the nature of the test, it is very difficult to measure the junction temperature of the device using temperature sensitive electrical parameters during avalanche. However, the temperature can be calculated using electro-thermal equations that have been calibrated by finite element models. Using [9] it is possible to calculate the junction temperature when the device is in avalanche. The temperature is calculated using

$$T_J@n*\frac{t_{AV}}{10} = \begin{cases} \frac{P_O*K}{10}*\sqrt{\frac{t_{AV}}{10}}*\left[10*\sqrt{n}-\sum_{1}^{n}\sqrt{n}\right], n \le 10 \\ \frac{P_O*K}{10}*\sqrt{\frac{t_{AV}}{10}}*\left[10*\sqrt{n}-\sum_{n-9}^{n}\sqrt{n}\right], n > 10 \end{cases}$$

Where T_J is the junction temperature, t_{AV} is the duration of the avalanche which is extrapolated from the measurements, P_O is the peak power also calculated from the measurements, K refers to the device thermal response and is calculated from the transient thermal impedance characteristic provided in the data sheet, n is the time step of the calculated temperature. The transient thermal characteristics for different ambient temperatures during avalanche for the SiC MOSFET are presented in Fig.14. The inductor used for the measurements in Fig. 14 was 9.5 mH. Fig. 15 shows the temperature transient characteristics for the SiC MOSFET during avalanche with different inductors (i.e. different avalanche durations). The ambient temperature used in the calculations of Fig. 15 was 25˚C. Fig. 16 and Fig. 17 show similar calculated thermal transients for the silicon IGBT.

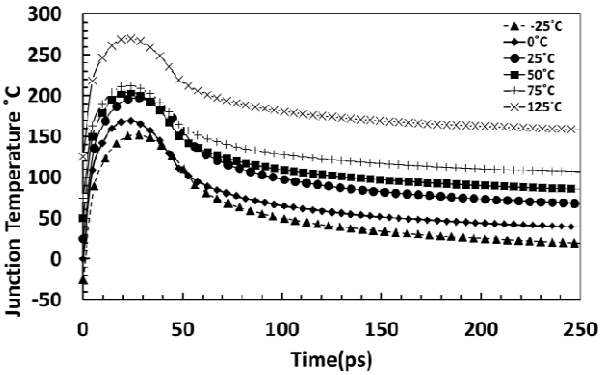

Fig. 14. Junction Temperature for SiC MOSFET for different ambient temperatures

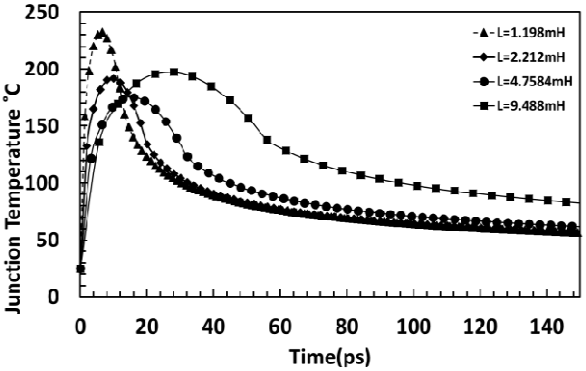

Fig. 15. Junction Temperature for SiC MOSFET for different inductors

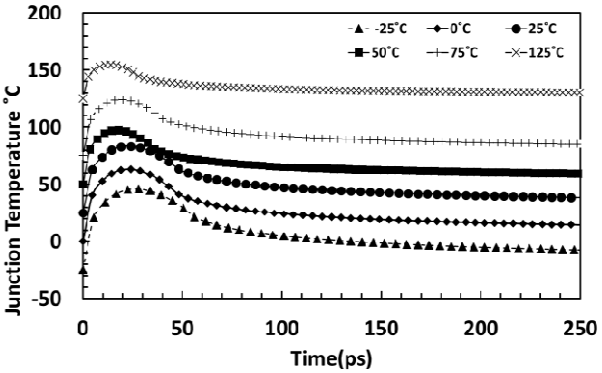

Fig. 16. Junction Temperature for Si IGBT for different ambient temperatures

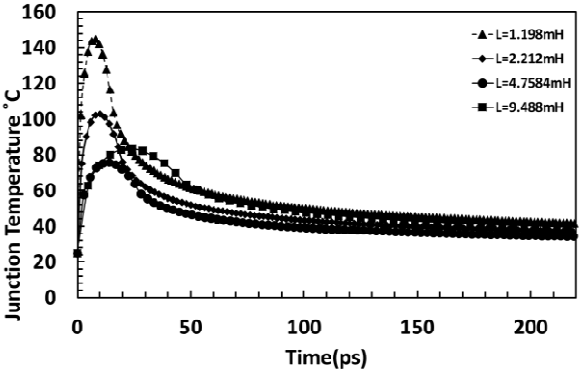

Fig. 17. Junction Temperature for Si IGBT for different inductors

Fig. 18 shows the peak calculated junction temperature for the SiC MOSFET and silicon IGBT at different ambient temperatures where a linear relationship can be

observed. Fig. 19 shows the peak junction temperature for both technologies with different inductors at 25 C.

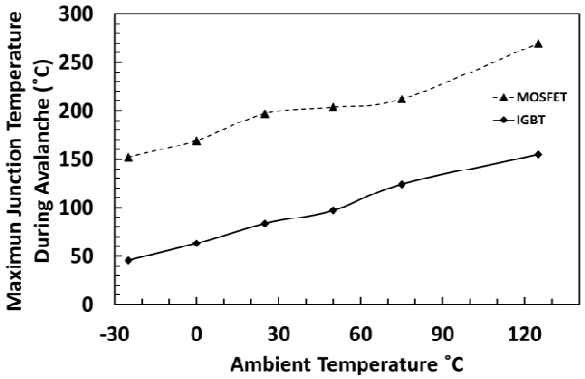

Fig. 18. Comparison of peak junction temperatures for different ambient temperatures

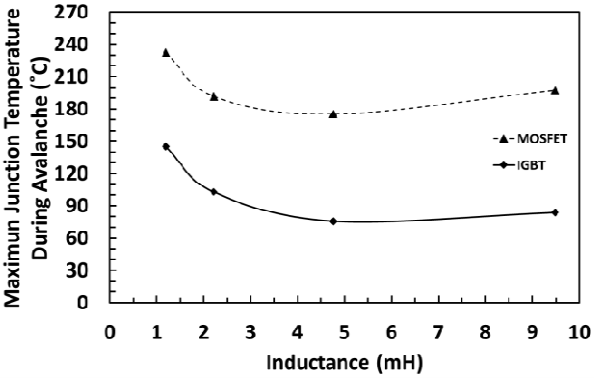

Fig. 19. Comparison of peek junction temperatures for different inductances

Regardless that the junction temperature of the SiC MOSFET is higher than that of the Si IGBT the MOSFET is more resilient to avalanche. The thermal capabilities of SiC are the dominant factor for the avalanche capabilities of the device

IV. Conclusions

Power device failure under unclamped inductive switching can be triggered under two conditions namely, high avalanche current with a short avalanche duration (condition A) and a low avalanche current with a long avalanche duration (condition B). Under condition A, parasitic BJT latch-up due to hot-spotting resulting from an unequal temperature distribution and inter-cell parametric variation within the power device, is known to be the trigger mechanism. Whereas under condition B, the intrinsic semiconductor temperature limitation resulting from thermally induced bandgap narrowing is thought to be the trigger mechanism. In this paper, SiC power MOSFETs are shown to be more avalanche rugged under condition B for the same avalanche energy compared to condition A. In the case of IGBTs, there is not a significant difference between the two conditions as far as the maximum avalanche energy is concerned. UIS tests have also been performed when the DUT is used to pre-charge the inductor (condition C) and when another device is used to pre-charge the inductor while the gate of the DUT is clamped to its source (condition D). SiC power MOSFETs are shown to be significantly more rugged in condition D compared to condition C. The results show that the material property of the semiconductor is more critical for determining avalanche mode ruggedness than the device type.

V. Acknowledgment

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VI. References

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