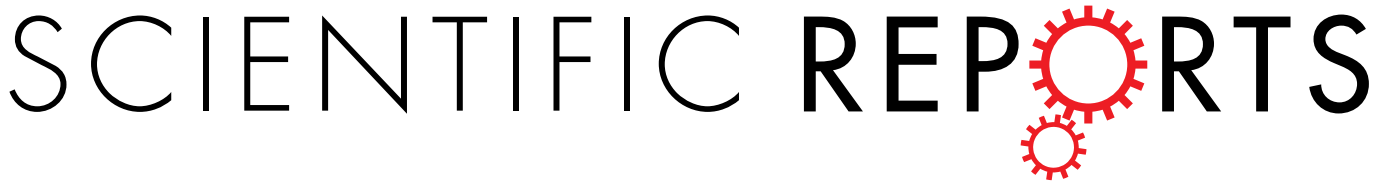

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# Interfacial Engineering of Semiconductor–Superconductor Junctions for High Performance Micro-Coolers

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**The control of electronic and thermal transport through material interfaces is crucial for numerous micro and nanoelectronics applications and quantum devices. Here we report on the engineering of the electro-thermal properties of semiconductor-superconductor (Sm-S) electronic cooler junctions by a nanoscale insulating tunnel barrier introduced between the Sm and S electrodes. Unexpectedly, such an interface barrier does not increase the junction resistance but strongly reduces the detrimental sub-gap leakage current. These features are key to achieving high cooling power tunnel junction refrigerators, and we demonstrate unparalleled performance in silicon-based Sm-S electron cooler devices with orders of magnitudes improvement in the cooling power in comparison to previous works. By adapting the junctions in strain-engineered silicon coolers we also demonstrate efficient electron temperature reduction from 300 mK to below 100 mK. Investigations on junctions with different interface quality indicate that the previously unexplained sub-gap leakage current is strongly influenced by the Sm-S interface states. These states often dictate the junction electrical resistance through the well-known Fermi level pinning effect and, therefore, superconductivity could be generally used to probe and optimize metal-semiconductor contact behaviour.**

The quality of the electrical contact between a semiconductor and a metal electrode is one of the key process elements in building high performance microelectronic circuits[1,2]. For transistors, the specific contact resistance needs to be sufficiently low to maximize drive currents and extensive efforts have been devoted to this topic since the dawn of semiconductor physics and integrated circuits. New materials (like 2D materials (graphene) and nanotubes) that are contenders to replace canonical semiconductors bring in new challenges to this field[3–5]. For example, one of the major obstacles, before graphene electronics becomes truly a viable high speed technology, is how to produce reliable low resistance contacts between 3D metal electrodes and 2D graphene.

Metal-semiconductor junctions can also have an active function, the classic example being the Schottky diode, which relies on the rectifying properties of the metal-semiconductor junction in the thermionic emission limit. Involving a similar physical process they can also be used as electro-thermal elements which allow a cooling heat flux due to electron energy filtering. One example is a Schottky junction in the tunnelling limit with temperature below the superconducting critical temperature of the metal electrode (see Fig. 1a,b). Such a semiconductor-superconductor (Sm-S) cooler junction introduces strong energy filtering for the tunnelling electrons due to the superconducting gap and the sharp peaks in the quasiparticle density-of-states (DOS) around the gap (see Fig. 1b). The Sm-S cooler junction[6] is the

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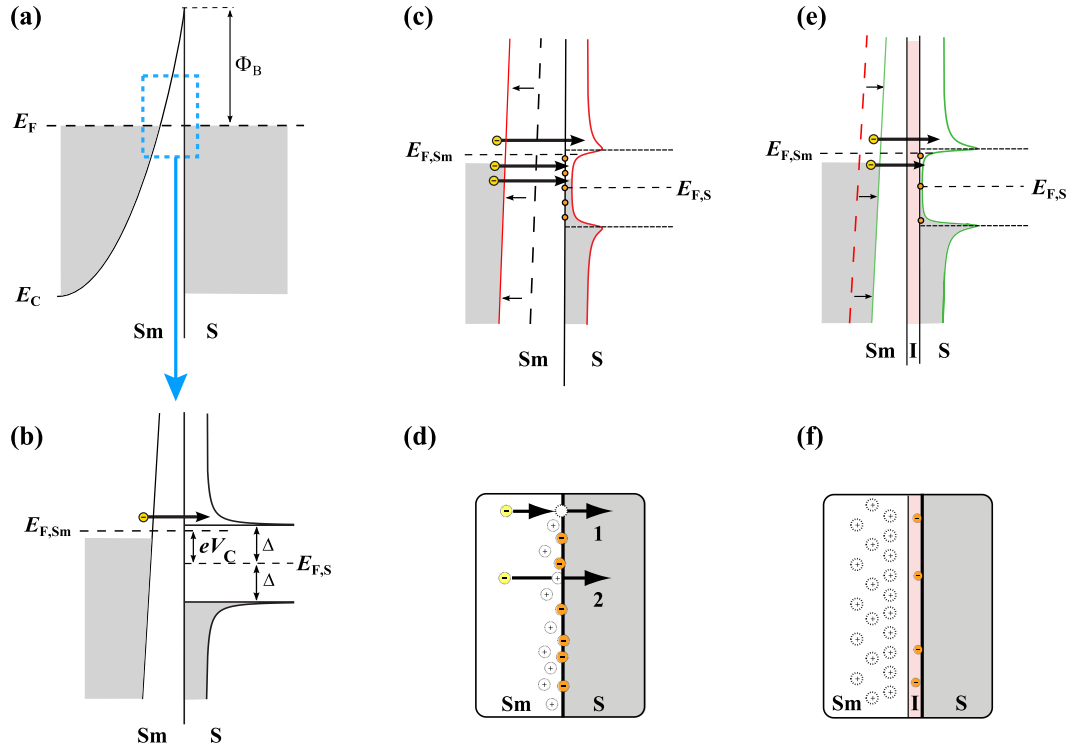


**Figure 1. Energy bands and electronic transport at the interface.** (**a**) Energy band diagram showing an ideal Sm-S Schottky barrier, where the barrier height is defined as $\Phi_B = E_c - E_F$, the difference between the semiconductor conduction band edge $E_c$ and Fermi level $E_F$ at the interface. (**b**) A blow-up of (**a**) around the Fermi level revealing the ideal superconductor density of states (DOS) and superconducting gap $\Delta$. Hot electron tunnelling from semiconductor to the superconductor is also illustrated. (**c**) Non-ideal Sm-S junction with negatively charged surface states at the interface (orange filled circles), which cause a shift of the conduction band and broaden the effective superconductor DOS by introducing sub-gap leakage channels due to unoccupied trap states close to the Fermi level. (**d**) Real space illustration of the leakage channels. Channel 1 illustrates the leakage through the interface trap states [the same as in (c)] and channel 2 the donor induced leakage channels. (**e**) Energy band diagram and (**f**) real-space illustration of the passivation effect of the insulating layer I. Leakage paths are diminished and Schottky barrier thickness is reduced. The latter being equivalent to Fermi-level depinning.

counterpart of the fully metallic device based on normal metal-insulator-superconductor (NIS) tunnel junctions[7,8]. Sm-S and NIS junctions provide an effective laboratory to study non-linear electro-thermal effects, and they are envisioned to be utilized in high sensitivity bolometer devices and electronic cooler platforms[9–12]. The silicon-based Sm-S cooler junctions, with the Schottky tunnel barrier replacing the insulator tunnel barrier, were originally introduced to improve certain features of NIS based devices[6]. It was anticipated that the Schottky barrier could be free from the unwanted leakage and pinhole effects that were present in large scale, high transparency NIS junctions. Another advantage over the NIS devices, is that the unwanted parasitic phonons-to-electrons heat back-flow in Sm-S cooler devices is significantly smaller than in NIS coolers, due to the weaker electron-phonon coupling in semiconductors[13–15]. Coupled with the advanced processing infrastructure of Si-based devices the Sm-S junctions were anticipated to take superconductive junction coolers to a whole new technological level, with the capability to build large scale integrated cooler platforms for low temperature sensors and devices.

However, it turned out that the high transparency (low resistance) Sm-S junctions that are needed for efficient coolers, did not behave according to the expectations[16,17]. They suffered from significant sub-gap leakage, which can be described phenomenologically by smearing of the ideally sharp density of states in the superconductor (see Fig. 1c). Due to this, the field of Sm-S coolers did not flourish and the problems with leakage remained neither understood nor solved. In this work, we successfully tackle both of these items. We demonstrate the first high transparency and low leakage Sm-S junctions and provide an explanation of the physics behind the sub-gap leakage effect in Sm-S junctions. A low leakage junction is achieved by introducing an additional insulator tunnel barrier between the S (Al) and Sm (n+ Si) electrodes and, thereby, creating a superconductor-insulator-semiconductor (SISm) cooler junction. Despite the introduction of the insulating barrier ($SiO_2$) the junction resistance remains low, which is attributed to Fermi level de-pinning and dopant segregation effects. Our results indicate that the sub-gap leakage is due to dopants in the tunnel Schottky barrier and, especially, due to surface states present at the Si-Al

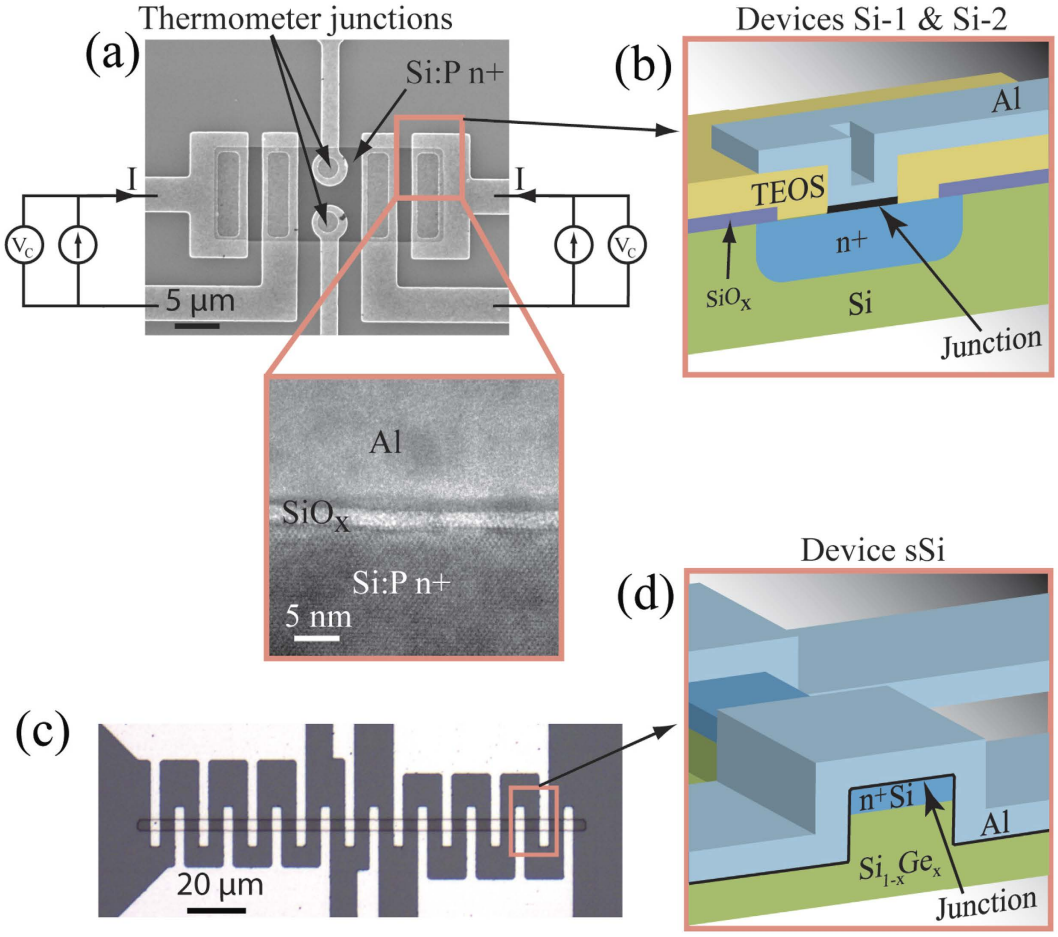


**Figure 2. Cooler devices.** (**a**) SEM and TEM micrographs of unstrained doped well samples. The Si:P island is visible as a darker shade under the junctions and electrodes in the SEM picture. The high resolution TEM micrograph shows the $SiO_x$ layer at the junction interface for sample Si-2. (**b**) Schematic cross-section of unstrained doped well samples Si-1 and Si-2. (**c**) Optical microscope image of the strained epi-layer sample sSi and (**d**) schematic cross-section. For all devices the semiconductor (Sm) is doped silicon and the superconductor (S) is aluminium.

interface (Fig. 1c,d). The added $SiO_2$ barrier effectively passivates the junction, removing both leakage channels (Fig. 1e,f). The main outcome of this work is the demonstration of low leakage high cooling power Sm-S devices, which can be utilized in large scale microcooler platforms and bolometers. Sm-S hybrids are also important for the emerging field of Majorana fermion quantum circuits[18]. In broader scope, our results are strongly linked to the physics of semiconductor-metal junctions and one of the key observations is that a metal electrode in the superconducting state acts as a sensitive probe to the metal-semiconductor surface states, which often dictate the junction resistance through the Fermi level pinning effect.

## Results

**Tunnel junction devices.** To improve the Sm-S junction quality, we have investigated different junction processing methods, with and without *in-situ* oxidation. The processes have been used for two different types of Sm-S cooler devices: unstrained with implanted wells in bulk Si and strained silicon (sSi) with degenerately doped epi-layer. The unstrained bulk Si cooler samples, Si-1 and Si-2, consist of degenerately doped Si:P wells in a Si substrate, which define the active Si island, see Fig. 2a for sample layout. The junctions were defined by opening contact vias through an isolating oxide layer, see Fig. 2b. The sSi cooler consists of a 30 nm thick strained Si layer grown on a relaxed $Si_{1-x}Ge_x$ alloy buffer layer. A biaxial tensile strain is induced via the lattice mismatch between the silicon and the SiGe alloy. The degenerately doped layer is etched to form an isolated mesa structure and the strained Si island is contacted with Al electrodes to form the junction, see Fig. 2c,d.

For all samples, the Si was treated using Hydrofluoric (HF) acid to remove the native oxide and hydrogenate the Si surface. Sample Si-1 is used as the unstrained control, with Al deposition after the HF treatment to form Sm-S junctions. The unstrained sample Si-2 and the strained sample sSi were annealed

| Ref. | $R_c$ (kΩμm²) | $\Gamma/\Delta$ | $P_c$ @ 0.3 K (pW/μm²) | $P_c$@ 0.1 K (pW/μm²) |
|---|---|---|---|---|
| 6 | 36 | — | 0.03 | Heat |
| 16 | 2000 | $3.5 \times 10^{-2}$ | ~0 | Heat |
| 19 | 100 | $1.0 \times 10^{-2}$ | 0.02 | Heat |
| 19 | 10 | $1.5 \times 10^{-2}$ | 0.14 | Heat |
| sSi | 31 | $1.0 \times 10^{-3}$ | 0.04 | 0.006 |
| Si-1 | 1.1 | $2.5 \times 10^{-3}$ | 1 | 0.13 |
| Si-2 | 1.35 | $8 \times 10^{-4}$ | 0.86 | 0.14 |

**Table 1. Sample parameters and comparison with previous works on Sm-S junctions.** See Supplementary Table 1 for all parameters of devices Si-1, Si-2, and sSi. The Ref. 19 strained sample in Fig. 3 is the one with $Rc = 100\,\mathbf{k}\Omega\mu m^2$. Heat means that the junctions introduce heating instead of cooling.

and oxidized at 550 °C *in-situ* in the sputtering system, before the Al deposition, which is intended to create a controlled oxide barrier in the interface, creating semiconductor-insulator-superconductor (SmIS) junctions. As a control for the sSi cooler we refer to earlier work[19], where device geometry was the same, but the junctions were not subjected to our *in-situ* oxidation technique. In order to generate a sample with a high interface state density, we prepared one set of devices by damaging the Si surface with Ar plasma before the Al deposition. Fabrication details and sample parameters can be found from the Supplementary Material. The most relevant junction parameters together with earlier literature are listed in Table 1.

**Electronic properties.** The current $I$ through the superconducting tunnel junction is commonly described by the relation[9,10]

$$I = \frac{G_T}{e}\int_{-\infty}^{\infty} dE\, g(E)\, F, \tag{1}$$

where $G_T = (R_c/A)^{-1}$ is the tunnel conductance, $e$ is the elementary charge, $E$ is the energy and $g(E)$ is the superconducting density-of-states (DOS). Here $R_c$ is the characteristic junction resistance and $A$ is the area of the junction. The function $F$ is the combined Fermi-Dirac distribution of the superconducting and semiconducting materials

$$F = f\,(E - eV_C,\, T_e) - f\,(E,\, T_b), \tag{2}$$

where $V_c$ is the voltage over the junction, $T_e$ is the electron temperature of the semiconductor, $T_b$ is the bath temperature and $f(E, T)$ is the Fermi-Dirac distribution (at temperature $T$). Throughout the analysis $T_b$ is also assumed to be the temperature of the superconducting electrodes. We use the differential conductance $G$ to represent the transport properties, which is given by

$$G = \frac{dI}{dV_c} = G_T\int_{-\infty}^{\infty} dE\, g(E)\,\frac{\partial f\,(E - eV_C,\, T_e)}{\partial\,(eV_C)}. \tag{3}$$

The sub-gap leakage is empirically described by the Dynes parameter $\Gamma$, which is introduced in the Dynes model[20]. In the Dynes model the superconducting DOS is described by

$$g\,(E) = \left| Re\left[\frac{E + i\Gamma}{\sqrt{(E + i\Gamma)^2 - \Delta^2}}\right]\right|. \tag{4}$$

By setting $\Gamma = 0$ we obtain the ideal sharp BCS (Bardeen-Cooper-Schrieffer) DOS without any states in the superconducting gap (see Fig. 1b). Non-zero $\Gamma$ smears the DOS around the gap edges and produces finite amount of states in the superconducting gap $\Delta$ (see Fig. 1c).

We determine the device parameters $G_T$ and $\Delta$ from the electrical measurements described in the Supplementary Material. We evaluate the quality of the tunnel junction interfaces using the ratio $G_0/G_T$, where $G_0$ is the zero bias conductance of the junction. $G_0$ is temperature dependent and should be investigated at sufficiently low-temperature, well below the superconductor critical temperature so that the sub-gap current is not dominated by thermally excited quasiparticles. Note that at $k_BT \ll \Delta$ the $G_0/G_T$ -ratio is numerically equivalent to the Dynes parameter $\Gamma/\Delta$. In this work, we refer to the low temperature saturated $G_0/G_T$ as the junction leakage.

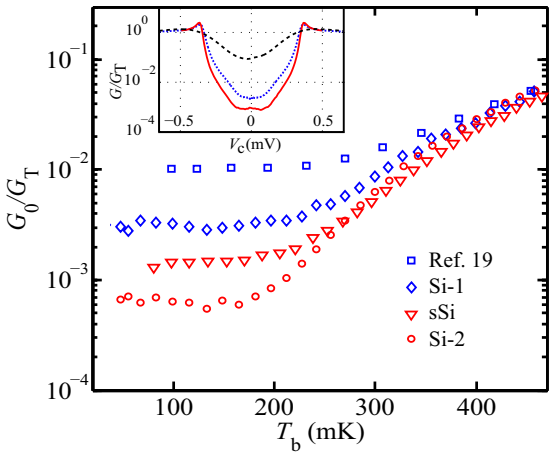


**Figure 3. Differential conductance.** Temperature dependence of the normalized differential zero-bias conductance $G_0/G_T$ measured from different samples. Inset: Normalized conductance curves $G/G_T$ as a function of voltage bias measured from samples Si-1 (blue dotted line) and Si-2 (red line) at $T_b = 30$ mK. The black dashed curve shows the conductance curve of the Ar plasma degraded junction.

Figure 3 main shows $G_0/G_T$ as a function of temperature. The oxide junction sample Si-2 shows clear reduction in the sub-gap conductance in comparison to the un-oxidized control sample Si-1. For the strained epitaxial sample we can observe a similar trend: the un-oxidized strained sample originally reported in ref. 19 has significantly larger sub-gap leakage than the oxidized strained sample sSi. Conductance as a function of junction bias is shown in Fig. 3 inset. In addition of the data from samples Si-1 and Si-2 the inset also shows data measured from the Ar plasma treated sample. The small local maxima in the conductance at zero voltage bias for the oxidized sample Si-2 is a common indication of Andreev tunnelling[21–23], also seen in high transparency high quality NIS tunnel junctions[24].

**Cooling performance.** The cooling power of superconducting tunnel junction degrades as a function of the sub-gap leakage. This degradation arises from the low energy tunnelling within the gap, which, as stated above, is empirically described using the Dynes density of states. Operated as a cooler, the degenerately doped Si island was cooled through two pairs of symmetric SmIS (Si-$SiO_x$-Al) junctions or Sm-S junctions biased in parallel and the island temperature $T_e$ was measured with an independent pair of high resistance junctions used as a thermometer as illustrated in Fig. 2a. The thermometer was calibrated at zero cooler bias, where $P_c = 0$ and $T_e = T_b$ and was then used to determine $T_e$ at non-zero bias resulting in Fig. 4a,c,d for samples Si-1, Si-2 and sSi, respectively. The measurement setup and thermometry calibration is described in the Supplementary Material.

The cooling power of a tunnel junction can be expressed as[10]

$$P_C = \frac{G_T}{e^2}\int_{-\infty}^{\infty} dE\, g(E)\,(E - eV_C)\,F. \tag{5}$$

The cooling power $P_c$ opposes inherent thermal coupling and heating mechanisms which need to be included in a heat balance equation to determine the resultant electron temperature. To model our experimental results we have adopted the thermal model utilized in ref. 19, and the results are shown as dashed and full lines in Fig. 4a–f. A full model description together with the fit parameters can also be found from the Supplementary Material.

The electron temperatures obtained from the thermometer and model are in good agreement for all devices, other than minor deviations for the measurements taken at low $T_b$. These deviations we attribute to leakage currents in the thermometer junctions, not included in the thermal model. We also compare the conductance curves with those of the model, as shown in Fig. 4b,d,f, which show that our model compares well to the experimental conductance characteristics of the coolers.

For the sSi cooler we get an impressive cooling down to $T_e = 90$ mK from $T_b = 300$ mK. The total power load for the sSi cooler is lower when compared to our unstrained Si devices due to factor of ~40 lower electron-phonon coupling[15,19] and reduced Joule heating. Compared to previous results on sSi devices with the same geometry and Joule heating[19], our new oxide junction device shows a large improvement in cooling performance attributed to both the reduced sub-gap leakage and the comparably higher $G_T$ (see Table 1).

To determine how our tunnel junction cooling performance compares to that of an ideal tunnel junction, we have studied the ratio $P_c(\Gamma)/P_{max}$ which can be considered as a cooler junction figure of merit. $P_{max}$ is the maximum cooling power obtained at optimal $V_C$ and $\Gamma = 0$, i.e, $P_{max}$ is linked to the ideal BCS

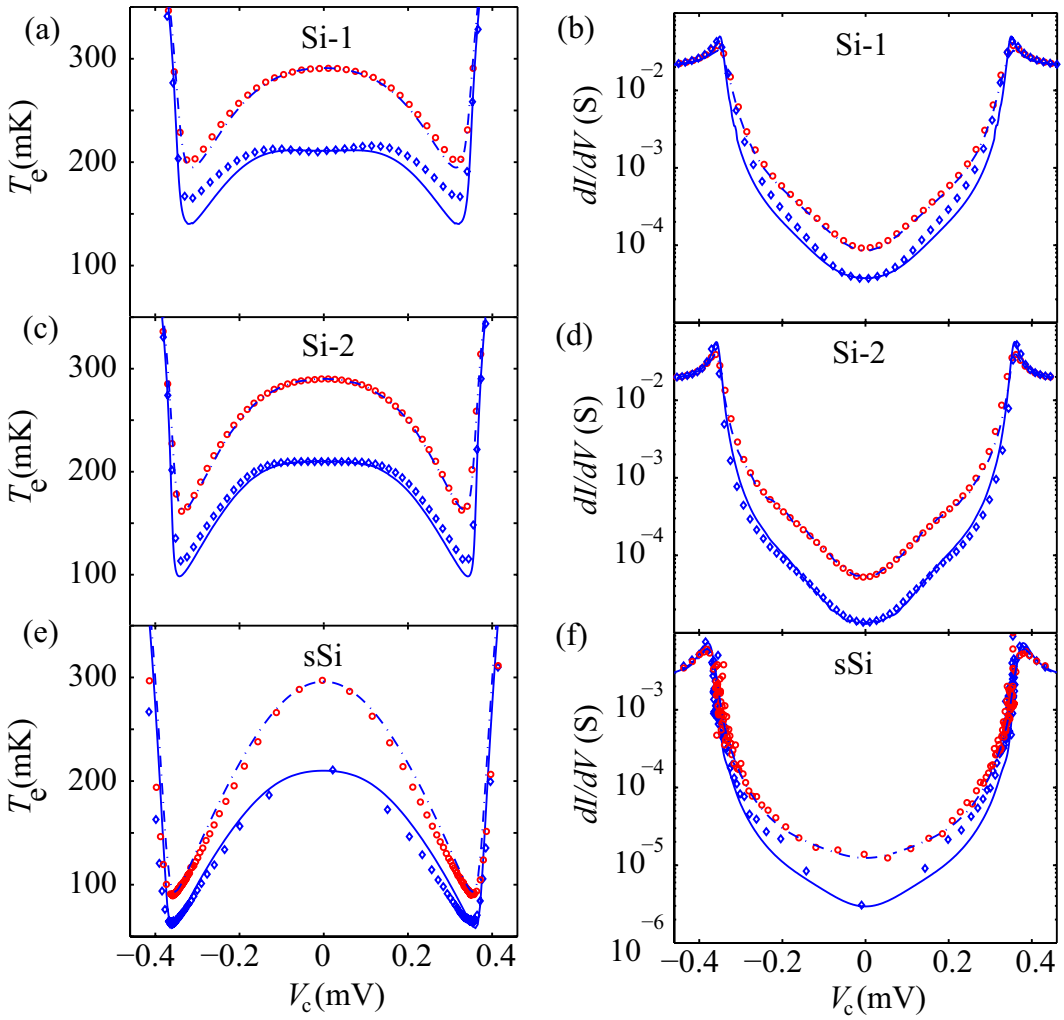


**Figure 4. Cooling and electronic properties.** (**a,c,e**) Electron temperature and (**b,d,f**) differential conductance of different samples as function of junction bias voltage. Symbols are experimental data and the solid and dashed curves are fits to the model. Electron temperature equals to the bath temperature at $V_C = 0$.

DOS. Optimal bias and $P_{max}$ have closed form from analytical approximations, $V_C \sim (\Delta - 0.66 k_B T_e)/e$ and $P_{max} \sim \frac{G_T \Delta^2}{e^2}\left[0.59\left(\frac{k_B T_e}{\Delta}\right)^{3/2} - \sqrt{\frac{2\pi k_B T_b}{\Delta}} e^{-\Delta/k_B T_b}\right]$, but here these parameters were determined numerically.

In Fig. 5, we have plotted $P_c(\Gamma)/P_{max}$ as a function of $\Gamma/\Delta$ and temperature $T_e$ (with $T_e = T_b$). This plot illustrates that, for a given $\Gamma/\Delta$, there is a minimum temperature where one can expect cooling, which serves as an indication of the tunnel junction quality required for cooling applications. As the electron temperature is reduced, for a given junction leakage $\Gamma/\Delta$, the cooling drops to zero (black line) at a temperature given by the relation $T_e \simeq T_c\, 2.5\, (\Gamma/\Delta)^{2/3}$ [25]. For poor quality junctions (high $\Gamma/\Delta$) the zero figure of merit is reached at higher temperatures. Therefore, to reach low electron temperatures, the figure of merit must remain high at low temperatures and this can only be achieved with high quality junctions (low $\Gamma/\Delta$). The cooler junction figure of merit drops with temperature because the useful cooling power depends on the spread of the Fermi distribution, which reduces with lowering the temperature, whereas the sub-gap leakage provides a heating component to the power integral in equation (5), which is nearly constant with temperature. Thus, leakage quickly becomes dominant at low temperature unless $\Gamma$ is low.

## Discussion

The similar $R_c$ for samples Si-1 and Si-2, with 1.1 kΩμm$^2$ and 1.35 kΩμm$^2$ respectively, seems at a first glance a counter intuitive result, since in addition to the Schottky barrier sample Si-2 also has the oxide barrier, which should significantly increase the tunnel resistance between Si and Al in comparison to sample Si-1. Firstly, we suggest that the oxide layer passivates the surface causing reduction in the

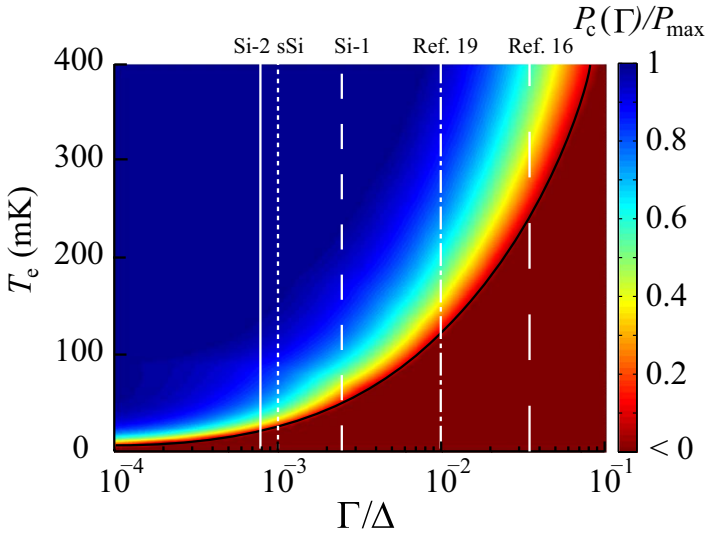


**Figure 5. Figure of merit of junction coolers.** Contour plot of figure of merit $P_c(\Gamma)/P_{max}$ as a function of Dynes parameter $\Gamma/\Delta$ and electron temperature $T_e$. $P_c(\Gamma)/P_{max} < 0$ corresponds to heating. For $\Gamma/\Delta > 6 \times 10^{-3}$ there is no cooling power at $T_b < 100$ mK, which also is observed for the earlier work listed in Table 1. The white vertical lines indicate the $\Gamma/\Delta$ for Sample Si-1, Sample Si-2, Sample sSi, ref. 19 and 16.

interface state density and, thereby, reduction of the negative charge at the interface, which leads to lowering (and thinning) of the Schottky barrier. This is equivalent to the Fermi-level de-pinning effect that such thin insulator layers have been shown to enable[26]. Note that sample Si-1 has higher sub-gap leakage than sample Si-2 (Fig. 3) and, therefore, we postulate that the opening of the superconducting gap creates a sensitive instrument to probe the interface states giving access to information that is hidden when investigating the contact resistance between semiconductor and metal only in the normal non-superconducting state. Similar interfacial effects have been also investigated in fully metallic junctions[27,28]. In addition to the interface state effect the oxide can create a high density donor layer in Si just next to the oxide (see Fig. 1f). This occurs because the low solubility of phosphorous in $SiO_x$ causes repelling of the dopants into the Si during the oxidation step. The effect is known as the dopant segregation effect[29] and it has been utilized in many nano-device fabrication recipes[30,31]. As the oxidation temperature (550 °C) is too low for strong phosphorous diffusion the high density donor region forms and this further reduces the Schottky barrier. The combination of the Fermi-level de-pinning and the segregation effects virtually offset the impact of the oxide barrier, leading to only a small increase in the tunnel resistance - from 1.1 kΩμm$^2$ (sample Si-1) to 1.35 kΩμm$^2$ (sample Si-2). Without these effects, the oxidation would create very high tunnel resistance and the junction would be relatively useless as a cooler or bolometer element. Because of this expectation, it has taken 14 years from the first studies on the Sm-S cooler[6] to realize a truly effective cooling performance in a silicon-based tunnelling junction.

Note that the behaviour of the Ar plasma-treated sample fully supports the above interpretation with regard to the interface traps and the superconductor being a useful probe of such states. The Ar treatment damages the semiconductor surface and increases the number of the traps, so for this sample $R_c$ and sub-gap leakage should be high. Indeed, this is precisely what we observe: we get a very large $R_c$ of 10 kΩμm$^2$ and sub-gap leakage is almost one order of magnitude higher compared to the process without Ar plasma (see the inset of Fig. 3).

The oxide barrier also confers other enhancements on the tunnelling cooling process. Our experimental results are well explained using the Dynes DOS, and the reduced sub-gap leakage clearly improves the junction performance. We infer that low-energy sub-gap tunnelling processes in Sm-S junctions occur through the interface states and dopant induced channels (Fig. 1c,d). Their proximity to the superconductor may create gap states in the superconductor or local high transparency channels, which results in increased single particle or 2-particle tunnelling (Andreev reflection)[21]. Adding an oxide barrier effectively reduces the number of these local channels, both through the reduction of interface states and the retraction of dopants at the interface, Fig. 1f. Compared to previous works[6,16,17,19] (see also Table 1), our findings clearly show that with our interface engineering we have significantly reduced both the high contact/tunnel resistance and high sub-gap leakage of Sm-S tunnel junctions – results that guarantee high cooling power.

A closer study of the results in Fig. 5 reveals that the cooling power, $P_c$, for the oxide junction sample Si-2 is ~90% of the ideal cooling power at $T_b \sim 100$ mK, based on the value of $\Gamma/\Delta = 8 \times 10^{-4}$ that we extracted from the transport measurements. The Sm-S device Si-1 is further from the ideal maximum performance with ~55% of the ideal cooling power at the same temperature (with $\Gamma/\Delta = 2.5 \times 10^{-3}$).

Both of these results are significant improvements compared to previous work on Sm-S coolers[6,16,17,19], where no cooling power was available at these temperatures (for $\Gamma/\Delta \geq 10^{-2}$, see also Table 1). For the sSi sample, the oxide junction quality showed a sub-gap leakage of $\Gamma/\Delta = 1 \times 10^{-3}$, which is an order of magnitude better than obtained from previous sSi devices[19], indicated in Table 1 and Fig. 5. From the comparison in Fig. 5, this device would be expected to have a useful cooling power $P_c$ down to $T_b \sim 35$ mK, however here the load from electron-phonon (e-ph) coupling and Joule heating in this particular device limits the observed cooling.

The origin of the larger sub-gap leakage and significantly higher characteristic resistance $R_c$ in the sSi device in comparison to the devices Si-1 and Si-2 is not known. We speculate that dislocations and mesa type structure can introduce more leakage paths. The dopant density is slightly lower in device sSi ($2.7 \times 10^{19}\,cm^{-3}$) than in devices Si-1 and Si-2 ($4 \times 10^{19}\,cm^{-3}$), but this alone cannot explain the order of magnitude difference in $R_c$. On the other hand, once again we can observe correlation between the magnitude of $R_c$ and sub-gap leakage. If we can obtain similar junctions for sSi as in device Si-1, on the basis of our simulations, we would observe cooling from 300 mK to 46 mK.

It should be noted that another potential contribution to the sub-gap leakage comes from coupling to environmental noise[32], which can also be empirically described by the Dynes model. Note also that doped semiconductors have significantly higher resistance than metals do and, therefore, noise coupling can be more serious issue in Sm-S devices than in NIS devices. This can be observed as a direct heating which can lead to a saturation of the low-temperature sub-gap conductance, as observed in Fig. 3. Therefore, the $\Gamma$-values found in this work must be considered as the upper limit values.

Large resistivity and low e-ph coupling of doped Si also provides the possibility for extremely high sensitivity THz detection. This is especially true for strained Si where ultra-low e-ph coupling values can be achieved[15] and very recently the first strained Si-based S-Sm-S THz bolometer has been demonstrated[33]. The junction technology introduced here can be directly adapted to such device to create a bolometer with improved characteristics.

Si-based cooler technology has an advantage of allowing a wider selection of superconductor materials, since in contrast to metal-based NIS coolers the quality of the junction interface is mainly determined by the cleaning/oxidation process of the normal (semiconductor) island. It is therefore plausible that larger gap superconductors (e.g. Nb, V) could be employed to initiate cooling in doped Si from temperatures as high as 1.5 K. Critically, the lower electron-phonon coupling in silicon than in metals, with further very large reductions possible with increased strain[14,15], could make silicon-based cooling technology superior to its all-metal counterparts.

In summary, we have demonstrated high transparency and low sub-gap leakage Sm-S cooler junctions by engineering the Sm-S interface by an insulator tunnel barrier between the S and Sm electrodes. Despite the introduction of the insulator barrier layer to the Schottky junction, the resistance of the superconductor-insulator-semiconductor cooler junction remains low. This unanticipated result was linked to the Fermi level de-pinning and dopant segregation effects that strongly affect the junction properties at the nanoscale. The insulator barrier layer significantly reduced the sub-gap leakage channels associated with interface states and dopants in non-oxidized Schottky barrier devices. By investigating a damaged surface sample we showed that the interface states at the Sm-S interface give a large contribution to the sub-gap leakage current. Therefore, a superconducting electrode can act as a sensitive probe to the metal-semiconductor surface states. Due to high transparency and low leakage the present junctions show unparalleled cooling power performance, in comparison to previous works on Sm-S coolers. Indeed, the demonstrated performance is comparable to that of high power NIS coolers[34], and the prospects posed by the first Sm-S cooler investigations 14 years ago[6] are accessible in practical devices. By adapting the new junctions in strain-engineered silicon coolers, where electron-phonon coupling is strongly reduced by strain, we also demonstrated efficient electron temperature reduction from 300 mK to below 100 mK by the electronic cooling process. In this work we utilized Al as the superconductor, which limits the operation to sub-1 K temperatures. The demonstrated Si-based cooler technology can enable cooling from above 1 K by the utilization of higher gap superconductors, with transition temperatures above 1 K.

## Methods

The samples in this study were fabricated on Si substrates utilizing UV lithography, dopant implantation, wet and plasma etching, epitaxial growth and different film deposition techniques. The details of the processes are described in the sample fabrication section of the Supplementary Material.

The transport measurements at low temperature have been performed in a dilution refrigerator down to a temperature of $T_b = 30$ mK. The refrigerator was equipped with measurement lines containing a combination of shunting and dissipative filters.

The *I-V* characteristics of both cooler and thermometer junctions were measured with a standard four-point measurement scheme. The tunnel junction resistance $R_T$ of our devices is given by the asymptotic resistance at voltages $V \gg \Delta/e$ and the superconducting gap $\Delta$ is defined by the threshold voltage $\Delta/e$ from the *I-V* characteristics at $T \ll T_c$. The conductance curves were obtained through differentiating the measured *I-V* data.

Hall bar measurements at 10 K provide values for the mobility, carrier density and sheet resistance of the sample under test. The carrier density $N$ is calculated using the measured sheet density and an estimated implant layer thickness of 150 nm. From the sheet resistance we can obtain the Si island resistance $R_{sm}$ of the samples in this work.

## References


1. Raymond, T. T. The physics and chemistry of the Schottky barrier height. *Appl. Phys. Rev.* **1,** 011304 (2014).
2. Sze, S. M. *Semiconductor Devices: Physics and Technology*. Wiley: New York, USA, (2001).
3. Landman, U., Barnett, R. N., Scherbakov, A. G. & Avouris, P. Metal-semiconductor nanocontacts: silicon nanowires. *Phys. Rev. Lett.* **85,** 1958–1961 (2000).
4. Suyatin, D. B. *et al.* Strong Schottky barrier reduction at Au-catalyst/GaAs-nanowire interfaces by electric dipole formation and Fermi-level unpinning. *Nature Commun.* **5,** 3221 (2014).
5. Chen, C., Aykol, M., Chang, C., Levi, A. F. J. & Cronin S. B. Graphene-Silicon Schottky Diodes. *Nano Lett.* **11,** (5) 1863–1867 (2011).
6. Savin, A. *et al.* Efficient electronic cooling in heavily doped silicon by quasiparticle tunnelling. *Appl. Phys. Lett.* **79,** 1471–1473 (2001).
7. Nahum, M., Eiles, T. M. & Martinis, J. M. Electronic microrefrigerator based on a normal-insulator-superconductor tunnel junction. *Appl. Phys. Lett.* **65,** 3123–3125 (1994).
8. Leivo, M. M., Pekola, J. P. & Averin, D. V. Efficient Peltier refrigeration by a pair of normal metal/insulator/superconductor junctions. *Appl. Phys. Lett.* **68,** 1996–1998 (1996).
9. Giazotto, F., Heikkila, T. T., Luukanen, A., Savin, A. M. & Pekola, J. P. Opportunities for mesoscopics in thermometry and electronics. *Rev. Mod. Phys.* **78,** 217–274 (2006).
10. Muhonen, J. T., Meschke, M. & Pekola, J. P. Micrometre-scale refrigerators. *Rep. Prog. Phys.* **75,** 046501 (2012).
11. Lowell, P. J., O'Neil, G. C., Underwood, J. M. & Ullom, J. N. Macroscale refrigeration by nanoscale electron transport. *Appl. Phys. Lett.* **102,** 082601 (2013).
12. Nguyen, H. Q., Meschke, M. & Pekola, J. P. A robust platform cooled by superconducting electronic refrigerators. *Appl. Phys. Lett.* **106,** 012601 (2015).
13. Prunnila, M. *et al.* Intervalley-Scattering-Induced Electron-Phonon Energy Relaxation in Many-Valley Semiconductors at Low Temperatures. *Phys. Rev. Lett.* **95,** 206602 (2005).
14. Prunnila, M. Electron–acoustic-phonon energy-loss rate in multicomponent electron systems with symmetric and asymmetric coupling constants. *Phys. Rev. B* **75,** 165322 (2007).
15. Muhonen, J. T. *et al.* Strain dependence of electron-phonon energy loss rate in many-valley semiconductors. *Appl. Phys. Lett.* **98,** 182103 (2011).
16. Buonomo, B. *et al.* Electron thermometry and refrigeration with doped silicon and superconducting electrodes. *J. Appl. Phys.* **94,** 7784 (2003).
17. Savin, A. *et al.* Application of superconductor–semiconductor Schottky barrier for electron cooling. *Physica :Condensed Matter B* **329-333,** 1481–1484 (2003).
18. Mourik, V. *et al.* Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices. *Science* **336** 1003–1007 (2012).
19. Prest, M. J. *et al.* Strain enhanced electron cooling in a degenerately doped semiconductor. *Appl. Phys. Lett.* **99,** 251908 (2011).
20. Dynes, R. C., Narayanamurti, V. & Garno, J. P. Direct measurements of quaiparticle-lifetime broadening in a srong-coupled superconductor. *Phys. Rev. Lett.* **41,** 1509–1512 (1978).
21. Blonder, G. E., Tinkham, M. & Klapwijk, T. M. Transition from metallic tunneling regimes in superconducting microconstrictions: Excess current, charge imbalance, and supercurrent conversion. *Phys. Rev. B* **25,** 4515–4532 (1982).
22. Hekking, F. W. J. & Nazarov, Yu. V. Interference of two electrons entering a superconductor. *Phys. Rev. Lett.* **71,** 1625–1628 (1993).
23. Hekking, F. W. J. & Nazarov, Yu.V. Subgap conductivity of a superconductor-normal-metal tunnel interface. *Phys. Rev. B* **49,** 6847–6852 (1994).
24. Rajauria, S. *et al.* Current-Induced Dissipation in a Hybrid Superconducting Tunnel Junction. *Phys. Rev. Lett.* **100,** 207002 (2008).
25. Camarasa-Gomez, M. *et al.* Superconducting cascade electron refrigerator. *App. Phys. Lett.* **104,** 192601 (2014).
26. Connelly, D., Faulkner, C., Grupp, D. E. & Harris, J. S. A New Route to Zero-Barrier Metal Source/Drain MOSFETs. *IEEE T. Nanotechnol.* **1,** 3 (2004).
27. Jung, H. *et al.* Potential barrier modification and interface states formation in metal-oxide-metal tunnel junctions, *Phys. Rev. B.* **80,** 125413 (2009).
28. Im, H., *et al.* Subgap leakage and interface states in superconductor-insulator-superconductor tunnel junctions, *Physica C* **470,** S832 (2010).
29. Knoch, J. & Appenzeller, J. Impact of the channel thickness on the performance of Schottky barrier metal–oxide–semiconductor field-effect transistors. *Appl. Phys. Lett.* **81,** 3082–3084 (2002).
30. Kinoshita, A., Tsuchiya, Y., Yagishita, A. & Uchida, K. Solution for high-performance Schottky-source/drain MOSFETs: Schottky barrier height engineering with dopant segregation technique. *2004 Symp. VLSI Technol.* **168** doi: 10.1109/VLSIT.2004.1345459 (2004).
31. Ahopelto, J., Prunnila, M. & Pursula, E. Self-aligned doping profiles in nanoscale silicon structures. *Physica E* **32,** 547 (2006).
32. Pekola, J. P. *et al.* Environment-Assisted Tunneling as an Origin of the Dynes Density of States. *Phys. Rev. Lett.* **105,** 026803 (2010).
33. Brien, T. L. R. *et al.* A strained silicon cold electron bolometer using Schottky contacts. *Appl. Phys. Lett.* **105,** 043509 (2014).
34. Fisher, P. A., Ullom, J. N. & Nahum, M. High-power on-chip microrefrigerator based on a normalmetal/insulator/superconductor tunnel junction. *Appl. Phys. Lett.* **74,** 2705 (1999).


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## Author Contributions

D.G., J.S.R., M.J.P., A.V.T. and H.Q.N. performed the electrical characterization and electron cooling and electron-phonon coupling measurements and modelling under the supervision of D.R.L. and M.P. D.G. and M.P. are the principal authors of the manuscript with contributions from M.J.P., E.H.C.P. and T.E.W. J.S.R., M.J.P. and D.G. prepared the supplementary information. M.P. designed the well devices and their fabrication process, with feedback from D.G., E.H.C.P. and T.E.W. D.G. was responsible for the fabrication of the well devices. E.H.C.P., T.E.W., M.M., M.J.P. and D.R.L. designed the strained samples and their fabrication process with feedback from J.S.R., D.G. and M.P. M.M. and V.A.S. were responsible for the epitaxial growth of the strained Si and M.J.P. and D.G. on the further processing to devices. The overall project was supervised by E.H.C.P., T.E.W., D.R.L. and M.P. All authors participated in interpreting the data and discussions on the manuscript.

## Additional Information

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