Reliability Assessment and Modelling of Power Electronic Devices for Automotive Application and Design

By

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Declaration

This thesis is submitted to the University of Warwick in support of the application for the degree of Doctor of Philosophy. It has not been submitted in part, or in whole, for a degree or other qualification at any other University. Parts of this thesis are published by the author in peer-reviewed research papers listed. Apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work described in this thesis is carried out by the author in School of Engineering of the University of Warwick.

Roozbeh Bonyadi

2012-2016

To mum and dad.

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Publication List

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2. Jahdi, S.; Alatise, O.; **Bonyadi, R.**; Alexakis, P.; Fisher, C.A.; Ortiz Gonzalez, J.A.; Li Ran; Mawby, P., "An Analysis of the Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation," *Power Electronics, IEEE Transactions on* , vol.30, no.5, pp.2383,2394, May 2015.

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4. Hu, J.; Alatise, O.; Ortiz Gonzalez, J.; **Bonyadi, R.**; Ran, L.; Mawby, P.A., "The Effect of Electrothermal Non-Uniformities on Parallel Connected SiC Power Devices under Unclamped and Clamped Inductive Switching," in *Power Electronics, IEEE Transaction on*, vol. 31, no. 6, pp. 4526-4535, June 2016.

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Abstract

The emergence of the hybrid electric vehicle and electric vehicles (HEV and EV) requires the reliability assessment of power electronic devices used in the inverters. This includes the electro-thermal reliability of bipolar devices such as IGBTs and PiN diodes and more recently, the SiC MOSFETs since the SiC technology is not as mature as their bipolar counterparts. This research, in its own capacity, through the use of accurate compact models, investigates the switching performance and characteristics of silicon IGBTs, PiN diodes and SiC MOSFETs. The need for higher power densities and fast device switching causes certain concerns in the performance and terminal characteristics of the converter.

SiC MOSFET is a potential power device for implementing EV drivetrain inverters. One of the major advantages of SiC MOSFET is the possibility of using their body diodes for reverse current conduction, thereby obviating the need for lossy silicon PiN diodes. The primary goal of using SiC MOSFETs is to enable high frequency switching since the significantly lower switching losses coupled with the high dI/dt and dV/dt can increase the power density. This research has investigated and modelled the use of the SiC body diode for current commutation under high dV/dt conditions. Since the body diode is not designed to operate under such conditions, the electrothermal robustness of SiC body diode is investigated by simulating parasitic BJT latch-up that results from hard current commutation under high dV/dt. In a power MOSFET, high switching rates coupled with the drain-body capacitance brings about a displacement current passing through the resistive path of the P-body in the MOSFET structure which creates a voltage at the base of the parasitic BJT within the device. This BJT latch-up under certain thermal conditions is capable of destruction of the device.

Another problem induced by high switching speed is that of the electrical coupling between complementing devices in the same leg of the inverter which is known as cross-talk or parasitic gate turn-on. In this research, the unintentional switching of IGBTs and the resulting short circuit current surge passing through the devices as a consequence of reducing the dead-time as well as increasing the switching rate is investigated and modelled. This is due to the discharge of the Miller capacitance which feeds back a current into the gate of the transistor. The result is that both transistors are switching on in the same phase leg.

The other problem which is addressed in this research is modelling the switching transients of parallel connected IGBTs for the purpose of delivering high current conduction capability. The electrothermal energy balancing between the parallel connected IGBTs is important as the electrothermal variation between the parallel connected devices can cause temperature imbalance, thereby, accelerating the degradation of the power module. This research investigates the variations in the electrical time constants and the thermal time constants between the parallel connected devices and models the switching behaviours.

Lastly, this research has focused on designing and fabricating power modules suitable for EV application and has tried to address methods to improve the electrothermal performance of the device and has investigated the impact of parasitic inductance of the layout on the electrothermal performance of the power module.

List of Abbreviations

ADE	Ambipolar diffusion equation
BJT	Bipolar Junction Transistor
CAE	Computer Aided Engineering
CFD	Computational Fluid Dynamic
CMOS	Complementary Metal Oxide Semiconductor
CSR	Charge Storage Region
CTE	Coefficient of Thermal Expansion
UAC	Undepleted accumulation layer capacitance
DUT	Devices under test
ECCE	Energy Conversion Congress and Exposition
EDU	Electric drive units
EMC	Epoxy moulding compound
EV	Electric Vehicle
EVB	Electric vehicle battery
FEM	Finite Element Models
FMEA	Failure Mode and Effect Analysis
GaN	Gallium Nitride
GTO	Gate Turn-Off
HEV	Hybrid Electric Vehicle
HV	High Voltage
ICE	Internal combustion engine
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistors
KVL	Kirchhoff's current and voltage laws
LED	Light Emitting Diodes
MOS	Metal Oxide Semiconductor

MOSFET	Metal Oxide Semiconductor Field Effect Transistors
NPT	Non-Punch Through
PHEV	Plug-in Hybrid Electric Vehicle
PMSM	Permanent magnet synchronous machine
PT	Punch Through
RTA	Rapid thermal annealing
SiC	Silicon Carbide
SOA	Safe Operating Area
SPWM	Sinusoidal Pulse Width Modulation
SRM	Switched reluctance motor
SSM	Six Step Mode
SVM	Space Vector Modulation
THIPWM	Third Harmonic Injection Pulse Width Modulation
VSC	Voltage source converters
VSI	Voltage source inverter

List of Symbols

A Active die area (cm^2)

A_B BJT base area (cm^2)

a_i Ratio of intercell area to active die area

C_B Drain-base capacitance of BJT (F)

C_{DIC} Depleted intercell drift region capacitance (F)

C_{GD} Gate-drain capacitance (F)

C_{ox} Oxide capacitance per unit area (Fcm^{-2})

C_p Specific heat ($W.kg^{-1}.K^{-1}$)

C_{th} Thermal capacitance (J/K)

C_{UAC} Undepleted accumulation layer capacitance (F)

D Ambipolar diffusivity (cm^2s^{-1})

D_b Diffusion coefficient in the emitter (cm^2s^{-1})

D_e Diffusion coefficient in the base (cm^2s^{-1})

D_n Electron diffusivity (cm^2s^{-1})

D_p Hole diffusivity (cm^2s^{-1})

D_{pH} Hole diffusivity in IGBT buffer layer (cm^2s^{-1})

E Electric field (Vcm^{-1})

E_0 Impact ionisation coefficient for Göhler/Sigg model (Vcm^{-1})

E_{01} Electric field at anode junction (Vcm^{-1})

E_{02} Electric field at cathode junction (Vcm^{-1})

E_1' Electric field gradient of anode depletion layer (Vcm^{-2})

E_2' Electric field gradient of cathode depletion layer (Vcm^{-2})

E_m Electric field at centre boundary during diode punch-through (Vcm^{-1})

G_p Hole generation rate ($cm^{-3}s^{-1}$)

h_n N+ emitter recombination parameter (cm^4s^{-1})

h_p P emitter recombination parameter (cm^4s^{-1})

I_{AK} Anode-cathode current (A)

I_{CE} Collector-emitter current (A)

I_{disp1} Displacement current at anode boundary of charge storage region (A)

I_{disp2} Displacement current at cathode boundary of charge storage region (A)

I_{DS} Drain-source current (A)

I_g Gate terminal current (A)

I_{GD} Gate-drain current (A)

I_{mos} MOS channel current (A)

I_n Electron current (A)

I_{n1} Electron current at P emitter (anode) boundary of charge storage region (A)

I_{n2} Electron current at cathode end of charge storage region (A)

I_p Hole current (A)

I_{p1} Hole current at P emitter (anode) boundary of charge storage region (A)

I_{p2} Hole current at cathode end of charge storage region (A)

J Current density due to electrons and holes ($cm^2V^{-1}s^{-1}$)

J_{CE} Collector-emitter current density (Acm^{-2})

J_n Electron current density ($A.cm^{-2}$)

J_p Hole current density ($A.cm^{-2}$)

k Harmonic index for charge storage region carrier density Fourier series representation

K_{FV} Feedback gain relating depletion layer voltage to boundary carrier density (Vcm^3)

K_p MOS transconductance (AV^{-2})

K_{p0} MOS Transconductance at room temperature (AV^{-2})

K_{th} Thermal conductivity ($Wm^{-1}K^{-1}$)

L Length of inversion layer (cm)

L_E Emitter length (cm)

l_m MOSFET/IGBT intercell half-width (μm)

M Total number of segments in calculation of drift region voltage drop

n Electron concentration (cm^{-3})

N_A Acceptor (P-type) doping concentration (cm^{-3})

N_B Drift region doping N-type concentration (cm^{-3})

N_D Donor (N-type) doping concentration (cm^{-3})

N_E Emitter doping (cm^{-3})

N_{eff} Effective depletion layer carrier density (cm^{-3})

N_H Buffer layer doping (cm^{-3})

n_i Intrinsic carrier concentration (cm^{-3})

p Free hole concentration (cm^{-3})

p_{b1} Carrier concentration at the P-emitter junction

p_k k-th Fourier series component of charge storage region carrier density profile (cm^{-3})

p_{x1} Ambipolar carrier density at anode end of CSR (cm^{-3})

p_{x2} Ambipolar carrier density at cathode end of charge storage region (cm^{-3})

q Unit electron charge (≈1.6×10-19C)

$Q_{channel}$ Charge in the inversion layer (C)

Q_H Buffer layer stored hole charge (C)

R_p Hole recombination rate ($cm^{-3}s^{-1}$)

R_{pb} P-body resistance (Ω)

R_{th} Thermal resistance (K/W)

T Temperature (K)

T_0 Reference temperature (≈300K)

t_{ox} Oxide thickness (nm)

t_r Travel time for electrons in the channel (s)

V Volume (m^3)

V_{ak} Anode-Cathode voltage (V)

V_B Drift region voltage drop (V)

V_d Depletion voltage (V)

V_{d1} Depletion voltage at anode end of the charge storage region (V)

V_{d2} Voltage across depletion layer at cathode end of charge storage region (V)

V_{DS} Drain-source voltage (V)

V_{GS} Gate-source voltage (V)

V_{j2} Forward N^-N^+ junction voltage at cathode end of charge storage region (V)

v_{sat} Carrier saturation velocity (cms^{-1})

V_T Thermal voltage (V)

V_{th} Threshold voltage (V)

V_{th0} Threshold voltage at room temperature (V)

W Width of inversion layer (cm)

W_B Carrier storage region width (μm)

W_{cell} MOS cell width (μm)

W_{d1} Width of the depletion layer at anode end of the charge storage region (μm)

W_{dg} Width of the depletion region (μm)

W_H IGBT buffer layer width (μm)

x_1 Boundary position at anode end of charge storage region (μm)

x_2 Boundary position at cathode end of charge storage region (μm)

x_d Total depletion width (cm)

x_n Depletion width in N-type (cm)

x_p Depletion width in P-type (cm)

Z_{th} Thermal impedance (K/W)

α_F Forward transfer ratio (typically ≈0.98)

$\mu_{i,\max}$ Maximum mobility of electron/hole ($cm^2V\text{-}1s\text{-}1$)

μ_n Electron mobility ($cm^2V\text{-}1s\text{-}1$)

μ_p Free hole mobility ($cm^2V^{-1}s^{-1}$)

$\frac{\partial p}{\partial x}$ Gradient of free hole carrier density (cm^{-4})

ρ Density ($kg.m^{-3}$)

τ High-level carrier lifetime (s)

τ_{HL} High-level carrier lifetime (s)

τ_{HL0} High-level carrier lifetime at room temperature (s)

τ_n Electron lifetime (s)

τ_p Hole lifetime (s)

ε Permittivity (Fcm^{-1})

ε_{ox} Silicon oxide permittivity (Fcm^{-1})

ε_s Semiconductor permittivity (Fcm^{-1})

ε_{si} Silicon permittivity (Fcm^{-1})

Φ_{bi} Built-in potential (V)

ϕ_F Bulk reference potential (V)

Chapter

1 Introduction

In the recent years, due to the significant increase of the greenhouse gas emission, global warming has become a major concern with governments across the world. This is expected to cause a rise of the sea level and cause the glaciers melt which will have huge impact on the life and habitat of all animals and human beings. Most of the technologically advanced countries around the globe have started to pay a close attention to this environmental problem and recently president Obama, of the United States, has addressed this issue by proposing an action plan to mitigate the worst effects of global warming [1, 2]. Consequently, the United States has developed a challenging plan to address the threat of climate change and are taking a leading role in combating CO_2 emissions especially from power plants [3]. The UK government established the world's first legally binding climate change target in 2008 with the Climate Change Act and aims to reduce the UK's greenhouse gas emissions by at least 80% by 2050 [4, 5].

The European parliament has also voted to revise EU rules on greenhouse gas emissions in general. Specifically, for the automotive sector, CO_2 emission limits for passenger cars for 2020 aim to ensure that the average new car produced will emit no more than 95 g CO_2/km [6]. This means that the average reduction in fuel consumption needs to be reduced by 27 per cent which is the toughest challenge that the major car manufacturers are facing. The electrification of transportation is widely recognised as a critical step in decarbonisation of modern industrial societies for the purpose of mitigating green-house gas emissions as well as ensuring energy security. Replacing the internal combustion engine with an electrical machine is a critical step in this direction.

The reduction of CO_2 emission is a challenging task as the demand for energy is increasing rapidly and the electricity sector is the major responsible source of total global CO_2 emissions. One of the ways to meet the UK greenhouse emission reduction targets is using renewable energy in form of wind turbine energy harvesting and PV solar cells. Moreover, building HVDC lines between UK and EU enables transcontinental energy exchange in a more efficient way and hence, can reduce the CO_2 emissions. The second responsible source after electricity sector is transportation sector and specifically automotive industry which is the main focus of this thesis.

The EU has introduced the new fuel economy test which is called “World Harmonised Light Duty Vehicle Test Procedure”, also known as WLTP, which aims to represent real-world driving conditions and has been developed from a database of

460,000 miles of global driving data. In order for a car to be able to pass the WLTP drive cycle, it needs to have a high peak power and quick acceleration for short periods of time and at the same time the size of the internal combustion engine (ICE) needs to be reduced in order to reduce the CO_2 emission [7]. Moreover, to be able to save fuel and increase the efficiency of the car, the engine needs to work at optimal operating points and the engine needs to operate at low speed. One of the methods that contributes in the reduction of the CO_2 emissions is deploying a regenerative braking system. The regenerative braking system will increase the fuel efficiency of a vehicle, however, these are not enough to satisfy the new WLTP fuel economy test and new technologies that show potential for decreasing energy use and carbon emission needs to be assessed. Among these new technologies which can be used in transportation, Hybrid Electric Vehicle (HEV), Plug-in Hybrid Electric Vehicle (PHEV) and Electric Vehicle (EV may also referred to as BEV or battery electric vehicles) can be named.

An electric power train increases the efficiency of the system and reduces the need of larger internal combustion engine (ICE). It also can provide high peaks of power and quick acceleration from zero speed which significantly contributes to reduction of fuel consumption. Consequently, due to the presence of the electric powertrain, these vehicles have better fuel economy and better overall performance than the conventional vehicles [8]. The Toyota Prius is an example and is the world's best-selling HEV and Toyota has over seven million global hybrid sales. PHEVs are the next generation of HEVs which can offer advantages over HEV including lower fuel consumption and the ability to charge the batteries from electric gird from any typical home outlet. This can

significantly extend the electrical range of the car and reduce the emissions as well. In general, the larger the battery pack, the further these vehicles will run in electric mode, after which the vehicle swaps to the ICE. If PHEVs are adapted by a large population, additional benefits will arise: for example, the batteries of these cars when they are plugged into the gird can be used as local energy storage when power demand at the grid is high.

1.1 Introduction to the EV Power Converter

Electrical machines convert electrical energy into mechanical energy using a rotating electromagnetic field that generates torque. This rotating electromagnetic field is generated by a 3-phase DC-to-AC voltage source inverter (VSI) powered by a DC link. Using a vector control, the torque and speed characteristics of the machine can be controlled from a user interface determined by the drive cycle.

Modern electric vehicle architectures are comprised of a DC battery (which is typically a lithium ion battery), a DC-DC boost converter required to step the battery voltage up, a 3 phase voltage source inverter and an electric machine for traction. Modern electric drivetrains are also capable of regenerative breaking, which simply means that vehicle retardation is initiated not by converting mechanical energy into heat via friction, but instead by running the motor as a generator. The AC power generated by the traction motor is then rectified by the converter and used to re-charge

the battery thereby improving the energy efficiency of the overall system. Fig. 1.1 shows a typical example of such a drivetrain from Toyota. In this drivetrain schematic, the battery voltage is 200V, the boost-converter output voltage is 650V and the maximum power deliverable by the machine is 50kW motoring and 30kW generating.

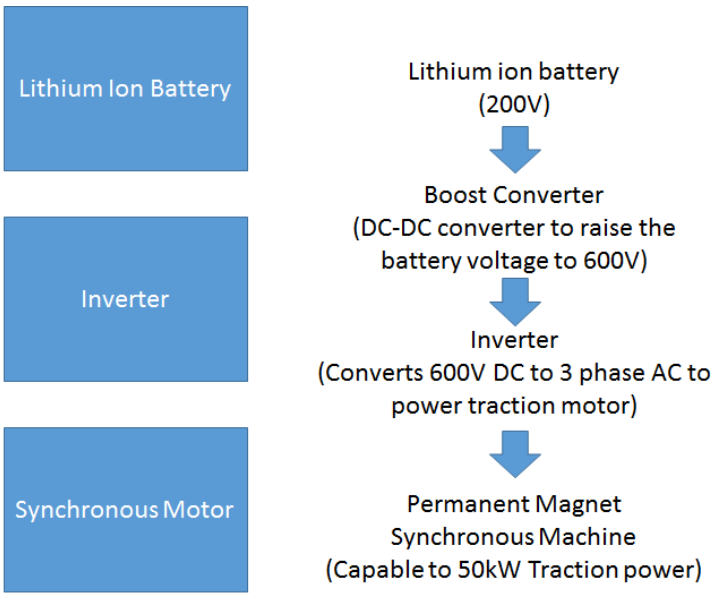


Fig. 1.1 Power conversion system for Hybrid Electric and Electric Vehicles from Toyota Prius.

The power electronic converter is critical to the efficiency and power density of the electric drivetrain system. The converter is voltage sourced since the DC side voltage is constant and the DC side current determines the direction of power flow. It is also a self-commutated converter since the phase-to-phase commutation of the current within the converter is determined by the switching of the power electronic devices. The simplest VSI is a 2 level converter comprised of 6 power devices each with an anti-parallel diode. This converter has 8 possible switching states with 2 being redundant

and 6 being active. The control strategy of the converter can be optimised to enable reduced power conversion losses. A typical power module is shown in Fig. 1.2 where a number of transistors and diodes can be seen on a DBC substrate.

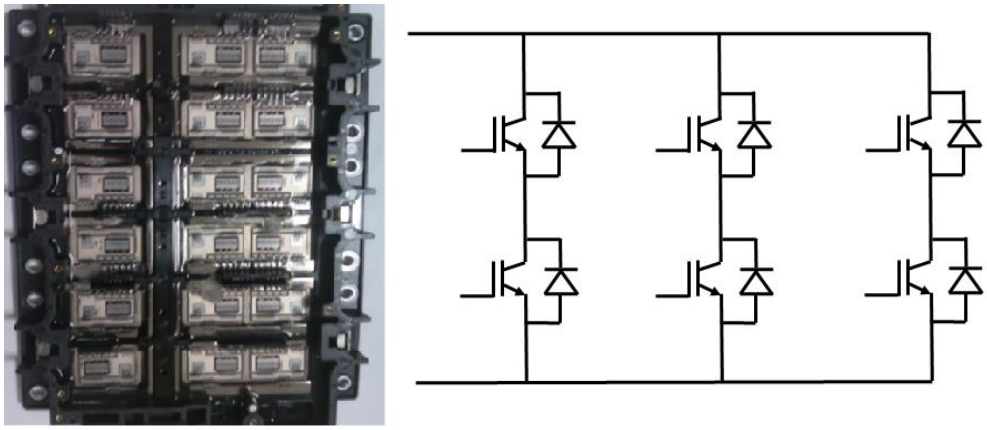


Fig. 1.2 Picture of Toyota Prius IGBT inverter module and a circuit schematic taken at Warwick.

1.2 Power Devices for EV Drivetrains

Currently, these power electronic converters are implemented using silicon insulated gate bipolar transistors (IGBTs) for electrical power inversion (DC to AC) and silicon PiN diodes for rectification (AC to DC). Silicon IGBTs are the technology of choice because the voltage levels required for power conversion are too high for silicon power MOSFETs. MOSFETs have more desirable characteristics than IGBTs; however, the on-state losses are prohibitive in silicon at voltages exceeding 200V.

The power electronic devices are not only limited to the motor control and electric vehicles, they are also used in a very wide range of applications such as wind turbine

and photovoltaic solar cells, high voltage DC transmission lines (HVDC), traction of trains and propulsion system of marine and in aviation sector.

To date, all major EV and HEV manufacturers use silicon IGBT and PiN diodes in their power electronic converters; however, the blocking voltage, switching frequency and current rating of these devices are reaching their limits and emergence of SiC power devices has generated interest for their use in EV drivetrains. Toyota has announced that they will start using this material by 2020. The reason is predicted on the need for high power densities for energy efficient ultra-compact drivetrains. Increasing the switching frequency of the power converter can enable this by reducing the size of the passive components that accompany the power converters. However, the recombination and reverse recovery currents of IGBTs and PiN diodes limit the maximum switching frequency. Hence, as a result, the use of wide bandgap unipolar devices like SiC MOSFETs and Schottky diodes is an attractive proposition for EV manufacturers.

1.3 Rationale for Current Work

The work presented in this thesis is mainly focused on modelling and parameterising electro-thermal failure modes in power electronic devices within an inverter which may cause thermal runaway and destruction of the devices or can cause long term reliability issues such as solder delamination or wire bond lift-off which can reduce the lifetime of the power inverter. Also, SiC devices are going to be adopted by

the automotive industry, this work additionally studies some of the reliability aspects of these devices in an inverter.

Physics-based modelling of bipolar power electronic devices such as IGBTs and PiN diodes have been carried out in several works [9]. The focus of previous research was the creation of fast modelling tools to simulate the switching transient of power electronic devices. However, these models lack the transient thermal behaviour of the device and assume a quasi-static temperature throughout the simulation. Moreover, these models were often used to simulate single turn-on and turn-off transients of the devices. 3D heat flow models which can accurately predict the temperature of the packaging of the device has been developed which are based on Fourier series reconstruction of ambipolar diffusion equation of heat transfer in the material [10]. However, these models are very complicated and they cannot be integrated with fast converter simulator such as PLECS which consider ideal switching of the devices and can supply the heat losses from the defined power losses look up tables.

In this work we employ accurate compact models, which describe the switching performance and characteristics of silicon IGBTs and PiN diodes, as well as SiC MOSFETs for EV drivetrains. The desire for higher power densities makes device switching much more critical. The models developed here are a key tool in investigating the associated problems which will be described later in this thesis.

Increasing the power density means that switching speeds will need to increase, allowing passive component sizes to be reduced. This places much higher strain on the power devices, which will lead to reliability issues. Hence, it is critical to be able to

accurately model both the electrical and thermal behaviour of the full converter including the power devices and the cooling system and understand the failure mechanisms.

The failure modes studied in this thesis may occur during the operation of the power inverter in an automotive application. As power electronics is a key component in an electric drive of the vehicle and concept of HEV/BEV, it is very important to be able to systematically study the failure modes and track the cause of the problem at the early stage in the design phase of development of the vehicle. This technique is also known as Failure Mode and Effect Analysis (FMEA) which is one of the steps during the design phase of any new component in advanced vehicle manufacturing industry. A functional design FMEA can pinpoint the failure mode at early stages during the design phase and helps to structure mitigation methods to reduce the risk and probability of failure occurrence and it should be carried out at system level and also on each and every component within the system. Hence, the introduced electro-thermal models in this work can be used by reliability engineers to show and parameterise these failures and prevent them from happening by understanding the root cause of the failure and by controlling the operation of the inverter and preventing it from operating under certain conditions such as hard commutation or high temperatures which may trigger these failures. Also, these analyses can be used by the engineers to estimate the peak achievable performance before the failure happens.

1.4 Contribution to Knowledge

In order to be able to characterise and model the failure mode, accurate compact electro-thermal models for IGBTs, PiN diodes and SiC MOSFETs were developed based on physics of semiconductors and then the developed models were used to explain the failure modes and the key parameters which were triggering the failures were identified and characterised. The temperature modelling is based on RC thermal networks. The models were used in different circuit configurations in order to model the known failure modes and compares and validates the models by comparing the results with the experiments.

The reliability issues investigated in this work are:

(i) BJT (Bipolar Junction Transistor) latch-up triggered by body diode reverse recovery under hard commutation with high *dV/dt.* The parasitic BJT model has been developed and implemented as a parasitic component in the compact electro-thermal model and the parasitic BJT latch-up phenomenon on MOSFETs during the reverse recovery of SiC MOSFET or CoolMOS body diode were investigated and parameterised. The results show that the current needed to trigger the parasitic BJT within the SiC MOSFET and CoolMOS can be provided by high *dI/dt* in the power electronic device. Moreover, at high temperatures and with higher current densities, thermal runaway due to parasitic BJT latch-up is exacerbated and the model can predict this accurately.

(ii) Parasitic gate switching of IGBTs under hard commutation and high temperatures. The unintentional parasitic gate turn-on of the device leads to a failure mode due to passing a surge of current through the devices (also known as shoot-through current) and may lead to catastrophic breakdown of the semiconductor devices. This phenomenon has been modelled and characterised in this work. In addition to parasitic gate turn-on phenomenon, reverse recovery induced parasitic turn-off phenomenon specific to SiC MOSFET has been modelled and validated through experiments. The results and experiments carried out to investigate this phenomenon indicated that this phenomenon can have destructive consequences on the SiC MOSFET due to the resulting oscillations of current between the diode and the transistor. The probability of the occurrence increases with the supply voltage, forward current, temperature and switching rate. The critical parameter is the snappiness of the diode recombination current and the dI/dt slope of the diode current during the reverse recovery, especially, the positive slope of the current. This slope coupled with the stray inductance of the MOSFET can result in a voltage which can bring down the gate voltage of the MOSFET and cause gate ringing. The impact of the four abovementioned parameters on the snappiness of the diode recombination current was investigated through experiments and modelled accurately using SiC MOSFET/PiN diode compact models.

(iii) Characterising the current sharing between paralleled IGBTs. Paralleling devices to develop a high current capability power module is very important in automotive industry where the demand for higher performance is required from the

powertrain. The electric motors with higher power are required for better performance and hence, power inverters with higher current handling capability are required. In this work, accurate current sharing between the devices has been studied and the thermal aspects of having unbalanced current sharing between the devices which can lead to thermal runaway of one of the devices has been studied.

Each of these failure modes were investigated by designing appropriate experimental setup to capture the failure modes. In order to understand the physics behind these failure modes, key parameters which can trigger them were identified and varied and the impact of combination of each parameter were investigated in the experiments and models were also validated for each case scenario.

1.5 Overview of Dissertation

This chapter gave an introduction to the global warming and challenges in reducing the CO_2 emissions. Moreover, it provided a brief rationale into the thesis. Chapter 2 gives a brief introduction into the electric drive and powertrain within a HEV/BEV. It also introduces different subsystem in an electric vehicle, as well as power inverters basics. Different types of device and circuit modelling tools will be introduced and importance of modelling the reliability of power electronic devices will be discussed. This thesis is divided into two parts. Part I is dedicated to modelling of power electronic devices and reliability modelling of power devices under certain conditions and Part II is dedicated to design and fabrication of an automotive power inverter.

Chapter 3 will give an introduction to the physics of operation of power electronic devices and physics of the semiconductor. It introduces the scientific framework of the device models and reviews the contribution of other researchers in the development of these models. The trade-off between finite element models and compact models is investigated. Then, development of modelling tools for power electronic devices will be explained in detail in this chapter. This includes modelling IGBTs, PiN diodes using Fourier series based reconstruction of the ambipolar diffusion equation which models the drift/diffusion of minority carriers in the voltage blocking drift region. Moreover, MOSFET model developed and equations are introduced in this chapter. Then the thermal aspect of the modelling will be explained and the compact electro-thermal model developed to model the reliability of power electronic devices will be explained in details. The model introduced in this chapter is used in subsequent chapters to investigate anomalous IGBT/PiN diode and SiC MOSFET characteristics under hard commutation with high dV/dt and dI/dt.

Chapter 4 introduces the SiC MOSFET as a potential power device for implementing EV drivetrain inverters. One of the major advantages of SiC MOSFET is the possibility of using their body diodes for reverse current conduction thereby obviating the need for lossy silicon PiN diodes and their problematic reverse recovery characteristic. This is attractive for EV manufacturers that would like to reduce their component count and improve the energy conversion efficiency of the power inverter. SiC Schottky diodes are well recognised to be susceptible to electromagnetic oscillations and instability (ringing) in their output characteristics. This ringing can be transmitted

back to the DC link and thus undesirable for applications like EV drivetrains. The ringing results from RLC resonance between the output capacitance of the diode/transistors and the parasitic inductance from the packaging. The primary goal of using SiC MOSFETs is to enable high frequency switching since the significantly lower switching losses coupled with the high *dI/dt* and *dV/dt* can enable increased power density for EV drivetrains. However, the ringing in the Schottky diode presents an impediment toward the realisation of these benefits. However, the body diode of the SiC MOSFET presents itself as a good comprise between the high speed low-loss switching of the Schottky diode and the soft recovery characteristics of the PiN diode. This is because the body diode is actually a SiC PiN diode, however, the very low minority carrier lifetime resulting from the wide bandgap means there is very little stored charge and reverse recovery. In this chapter, the use of the SiC body diode for current commutation under high *dV/dt* conditions is investigated and modelled. Since the body diode is not designed to operate under these conditions, the reliability is investigated by simulating parasitic BJT latch-up that results from hard current commutation under high *dV/dt*. The phenomenon is explained in details using the experimental observation to demonstrate the failure modes. Next, the device models developed in Chapter 3 will be used to model this failure mode and to give in depth understanding of the physics behind the thermal runaway due to parasitic BJT latch-up. The model is validated and the results are discussed in this chapter.

Chapter 5 investigates another anomalous IGBT characteristic that occurs under the high *dV/dt* and *dI/dt* conditions required for high power densities in EV drivetrains.

This is cross-talk or parasitic turn-ON. As the current and voltage commutation rate is increased in the EV inverter module, unintentional short circuits may occur as a result of reduced dead-time as well as unintentional turn-ON of devices thereby leading to repetitive short circuits. This un-intentional switching results from the discharge of the Miller capacitance feedback a current into the gate of the transistor. The result is that both transistors are switching ON in the same phase leg thereby resulting in a discharge of the DC link capacitance and short circuit current. The mitigation technique in IGBTs is to turn-OFF the power devices with large negative gate voltages and/or reducing the switching rates using different turn-ON and turn-OFF gate drive impedances. However, both techniques limit the maximum switching frequency that can be used to drive the converter. Tackling this problem will require advanced compact models that can predict the occurrence of parasitic turn-ON as well as correctly estimate the power dissipation that results from it. This chapter addresses this modelling requirement by using the modelling framework introduced in chapter 3 to investigate parasitic turn-ON or cross-talk in IGBTs and SiC power devices. The parasitic induced parasitic gate turn-off in SiC MOSFETs is also another anomalous characteristic introduced in Chapter 5 of this dissertation. This phenomenon is due to the very high dI/dt of the reverse recovery current of the complementing PiN diode under hard commutation condition coupled with the parasitic components of the circuit. The observations during the experiments are discussed and both phenomena are modelled. The key parameters are introduced and mitigation methods are explained.

Chapter 6 addresses the modelling requirements for paralleling multiple power devices for the purpose of delivering high current conduction capability. Future EV drivetrains are expected to have higher voltage blocking and current conduction capability. The need for series connected power devices for higher voltage blocking will not emerge in EV drivetrain applications since DC link voltages are not expected to rise beyond the voltage blocking capability of commercially available IGBTs. However, higher current modules will be needed in the future. To deliver this, more power devices will be required for parallel connection, hence, the electro-thermal energy balancing between them is important to model and understand. Chapter 6 extends the modelling framework in chapter 3 to address this problem. Electro-thermal variations between the power electronic devices connected in parallel, can cause temperature imbalances thereby accelerating the degradation of the power module. These electro-thermal variations can come in the form of variations in the electrical time constants and/or thermal time constants between the parallel connected devices. The model developed in this chapter can predict the impact of different junction temperature of the devices or having different gate resistance on the current sharing between the devices. These differences can happen due to non-uniform degradation of the devices during the lifetime of the power module. The model in this section decouples the thermal time constant from the electrical time constant to produce a computationally inexpensive modelling tool which can be used by the reliability power electronic engineers to model the current sharing between parallel IGBTs in a power module.

Chapter 7 shows packaging process of power inverter and shows a double side cooling power inverter suitable for automotive application that is designed at Warwick University's packaging cleanroom.

Finally, the last chapter (Chapter 8) concludes the dissertation and addresses possible future development and research opportunities in this field.

Chapter

2 Introduction to Electrical Drive System

2.1 Overview

Conceptually, in hybrid electric vehicles power and torque is transmitted to the wheels from combination of a fossil fuel powered internal combustion engine and an electric power source. The power flow is bidirectional between the battery and the powertrain and it can also be bidirectional between the load and the electrical powertrain. Fig. 2.1 below shows the conceptual schematic of a hypothetical hybrid electric vehicle [8, 11].

The main types of HEV are listed as below [8, 12]:

(a) Mild hybrid electric vehicles

(b) Series hybrid electric vehicles

(c) Parallel hybrid electric vehicles

(d) Series-parallel hybrid electric vehicles

(e) Plug-in hybrid electric vehicles

All these different types of HEV systems are introduced in detail in Appendix A.

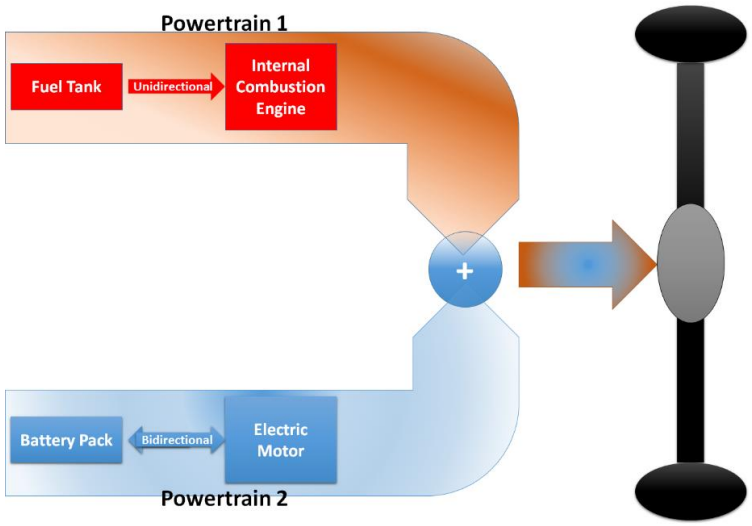


Fig. 2.1 Schematic of a hypothetical hybrid electric vehicle with two powertrains.

In the case of BMW i3 the power is only taken from the battery and the ICE is an option to charge the battery through a generator to extend the vehicle range.

2.2 Electric Powertrain

The biggest difference between a conventional vehicle and EV comes down to the electric powertrain system. An electric powertrain consists an electric machine, a battery and a power converter with a controller.

2.2.1 eMachines

There are several different types of electric machines. One of the most attractive eMachines for automotive industry is the permanent magnet synchronous machine (PMSM) due to its high power and torque density of this type of motor. PMSMs were invented in the mid-19th century and they were used at a fixed frequency mainly for single phase power generation. Advances in power electronics have led to the invention of variable frequency drives and has opened new doors for PMSM in a wide range of applications.

The high torque profile and low maintenance cost of PMSM makes this type of motor desirable for premium electric vehicles. Although, the rare-earth materials used in these motors increases the raw material cost and therefore makes them less attractive, however they are the most common type of motor in use today in HEV application. Other types of common motors used are induction motors, switched reluctance as well as DC motors. Each of these machines have their own pros and cons in terms of torque ripple, power density, ease of manufacturing, ease of maintenance, cost and ease of rotor cooling.

2.2.2 EV Battery

The traction battery which is used to power the eMachine is known as electric vehicle battery (EVB). These batteries are different from the conventional vehicle battery packs used for ignition and lighting of the vehicle as they need to deliver power

for a longer periods of time according to the anticipated range of the vehicle. Moreover, the propulsion system of the vehicle requires a significantly higher current. Consequently, the EVB for PHEV/BEVs are required to have a very large capacity. Batteries are predominantly rechargeable lead-acid, NiCd, nickel metal hydride, lithium ion or Li-ion polymer.

2.2.3 Power Inverter

Depending on the type of the motor and the direction of power flow between the motor and the battery, the electrical power needs to be converted into a suitable form; i.e. conversion between AC or DC voltages, adjustment of current and voltage level, varying frequency or combination of these might be needed during the operation of the vehicle. The subsystem responsible for power conversion is known as power inverter (converter). At the heart of these inverters there are several semiconductor power switches. The bidirectional power flow between the eMachine and the battery pack, enables regenerative braking.

In a nutshell, semiconductor power devices try to emulate an ideal electrical switch which is controlled by a gate terminal. The most common power inverter used in the automotive industry is the three phase, 2 level power inverter (Fig. 2.2). This circuit topology converts DC power from the battery to 3-phase sinusoidal current which excites the electric motor. This circuit is also known as a three phase full-bridge built-up from three half bridges which are the core unit of the majority of topologies and consists two devices in series.

Fig. 2.3 shows such a half bridge topology which consists two switching devices connected in series. A full bridge power bridge is made from three half-bridges connected in parallel and is used for driving a single phase motors or a DC motor.

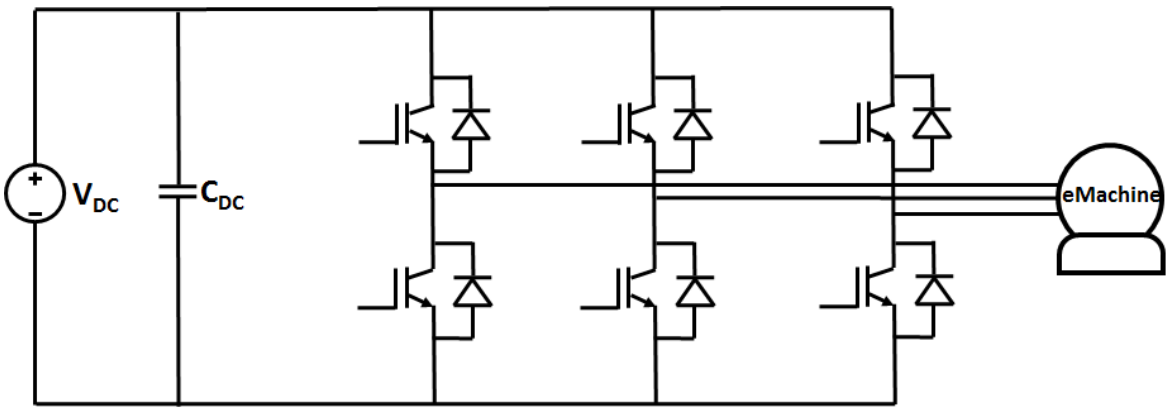


Fig. 2.2 Circuit diagram of a 3-phase full bridge inverter.

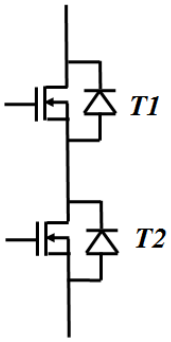


Fig. 2.3 A half bridge topology.

The two diagonal active devices in each two consecutive legs of the inverter are switched at the same time and the current that flows through these devices energises the windings of the stator. Different control strategies can be used to drive the motor

using a three phase inverter such as Sinusoidal Pulse Width Modulation (SPWM), Third Harmonic Injection Pulse Width Modulation (THIPWM), Space Vector Modulation (SVM), Over Modulation (OVM), Six Step Mode (SSM) and etc. It is worthwhile mentioning that in order to control the torque feedbacks from the motor are required which can be via current transducers measuring currents from the cables going from the phase output of the inverter into the motor (LEM hall effect current transducer) and position sensors which are typically resolvers in case of permanent magnet motors.

Fig. 2.4 shows an example of commercially available HEV and BEV inverters for Toyota Prius and Nissan Leaf respectively. As can be seen, the power module consists of several IGBTs and diodes connected in parallel to form the three phase power inverter. Fig. 2.5 illustrates Nissan Leaf power inverter as a complete system. This includes the power stage, DC-link capacitors, gate driver and controller, filters, cooling system, bus-bars and interfaces with the motor and wiring harness of the resolver. Power inverter of a switched reluctance motor (SRM) is introduced in Appendix B.

2.2.4 Power Devices

At the heart of each power inverter are several different power electronic switches. The very first power electronic devices were mercury-arc valves also known as mercury-vapor rectifier which was a type of a rectifier used to rectify the high AC current and high AC voltage into DC form. This device was invented in 1902 by Peter Cooper Hewitt and were used to drive industrial motors and high voltage DC (HVDC)

lines as well as the electric railways in London. The advancement of solid-state semiconductor technology led to invention of semiconductor devices such as diodes, thryristors and transistors in the early 1950s and this improved the current and voltage handling capability of such devices.

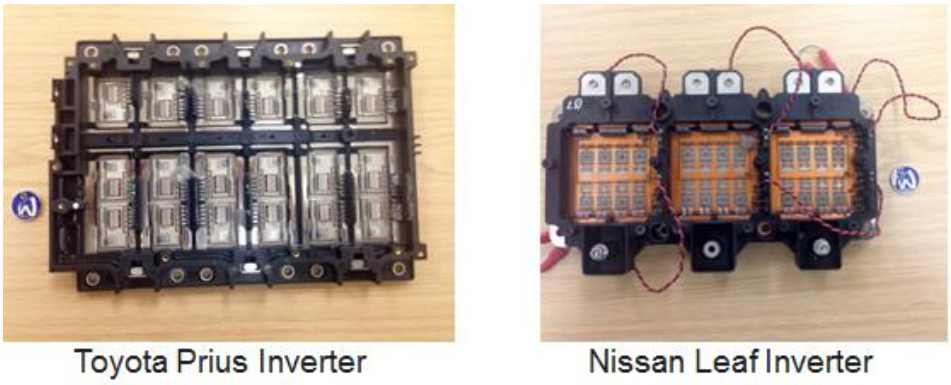


Fig. 2.4 Commercially available power inverter of (Left) Toyota Prius (HEV) and (Right) Nissan Leaf (BEV).

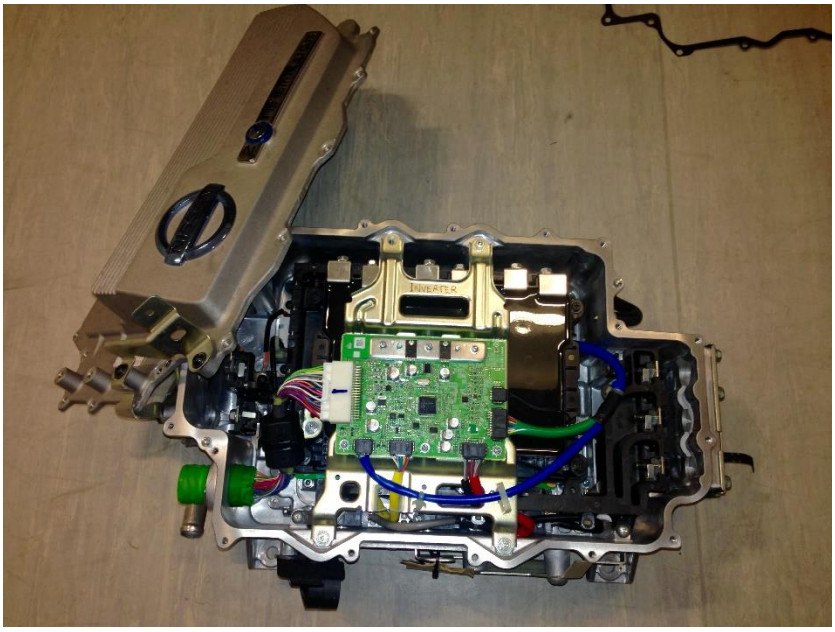


Fig. 2.5 Power inverter of Nissan Leaf including the gate driver, DC link capacitors, power bridge, filters and cooling system.

Power engineers designed devices with control capability such as Bipolar Junction Transistors (BJT), Metal Oxide Semiconductor Field Effect Transistors (MOSFET), Junction Field Effect Transistors (JFET), Gate Turn-Off Thyristors (GTO), and Insulated Gate Bipolar Transistor (IGBT). The basic operation of these devices are similar to valves and the control of the current through these devices can be achieved by applying a small signal to the gate (control terminal) of these devices. Hence, unlike line commutation devices such as thyristors, the operational frequency of these devices were not limited to the periodical change of the current and they could be switched at higher frequencies which enabled a new era in the field of power electronics where the current and voltage waveforms could be shaped based on the switching topology of the solid-state power electronics used in circuits.

The most commonly used power electronic devices in automotive application are IGBTs, PiN diodes, MOSFETs and Schottky diodes. In this section a brief history of the power devices is reviewed.

2.2.4.1 Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

The MOSFET was invented by Dawon Kahng and Martin M. Atalla at Bell Labs in 1959. MOS structure has been used widely in small signal integrated and digital circuits. Invention of Complementary Metal Oxide Semiconductor (CMOS) and using them in microprocessors and digital circuits by Fairchild Semiconductor was one of the

most important steps in the field of computer engineering and was the basis of modern digital circuits.

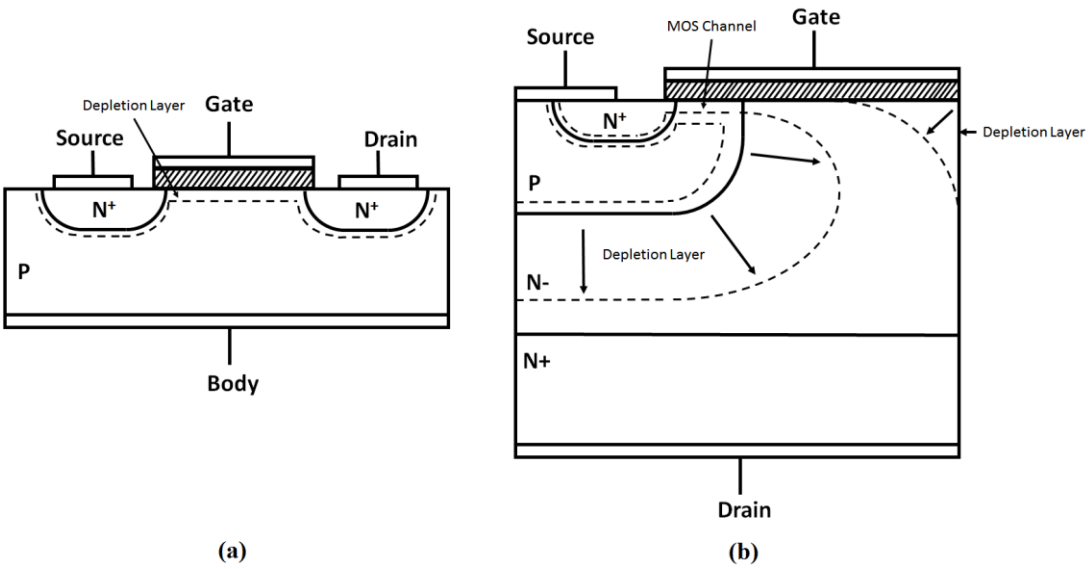


Fig. 2.6 Cross-section view of (a) a lateral MOSFET and (b) a vertical power MOSFET.

Early MOSFETs were lateral devices and could not carry high currents and were not capable of blocking high voltages. Advancement in manufacturing CMOS devices, enabled design of vertical MOSFET devices. Vertical MOSFETs can block higher voltages than their counterpart lateral devices and they are capable of handling higher current density. Power MOSFETs can switch at faster rate than thyristors or IGBTs. However, the blocking voltage of Silicon-based MOSFETs are limited to several hundreds of Volts. Hence, they are not a suitable candidate for applications where higher blocking voltages are needed.

Fig. 2.6 shows a cross-section view of (a) a lateral MOSFET and (b) a vertical MOSFET. In principle, both devices operate similarly and the when an inversion layer

forms under the gate of the device and channel is formed, electrons start to flow from source towards the drain. The difference between these two is the existence of the N^- type drift layer which provides higher blocking voltage for the vertical structure.

When a power device is operating, during the time that the device is conducting current, the device has an on-state voltage drop which is due to the resistive behaviour of the device. The losses associated to the on-state resistance of the device is known as conduction losses. Moreover, when the device is switching from the off-state to on-state or vice versa, at the onset of switching, both current and voltage exist which exhibits a power loss generated in the form of heat in the device. This is known as switching losses which can be categorised into turn-on losses or turn-off losses. In case of MOSFETs, these devices have a very low switching losses and this is due to the fact that the device is a unipolar device and only electrons (in case of n-channel) or holes (in case of p-channel) are the carriers. Hence, there is no extra charge stored in the device and the device can switch fast (a few ns to a few hundreds of ns depending on the voltage rating and the operating voltage). However, due to existence of the vertical low doped drift layer in the device, the on-state voltage drop is slightly higher in comparison to the bipolar devices such as IGBTs.

2.2.4.2 Insulated Gate Bipolar Transistors (IGBT)

IGBTs are semiconductor devices which their switching operation are controlled similar to MOS gate structure and the drift region of this device operate based on conductivity modulation. Some of the early versions of this transistors in 1983 were

referred to as COMFET due to this reason [13]. The operation mode of this transistor was discovered in an experiment and patented by Yamagami in 1968 and later on it was reported by Scharf and Plummer in 1978. The vertical operation mode of this transistor was experimentally discovered by B. J. Baliga in 1979. A vertical IGBT which is now being widely used in a very wide range of applications in power electronics has a very similar structure to a vertical MOSFET. The only difference is existence of a P-type anode at the back-side of the device which enables flow of electrons and holes into the drift region. Hence, these type of devices are known as bipolar devices.

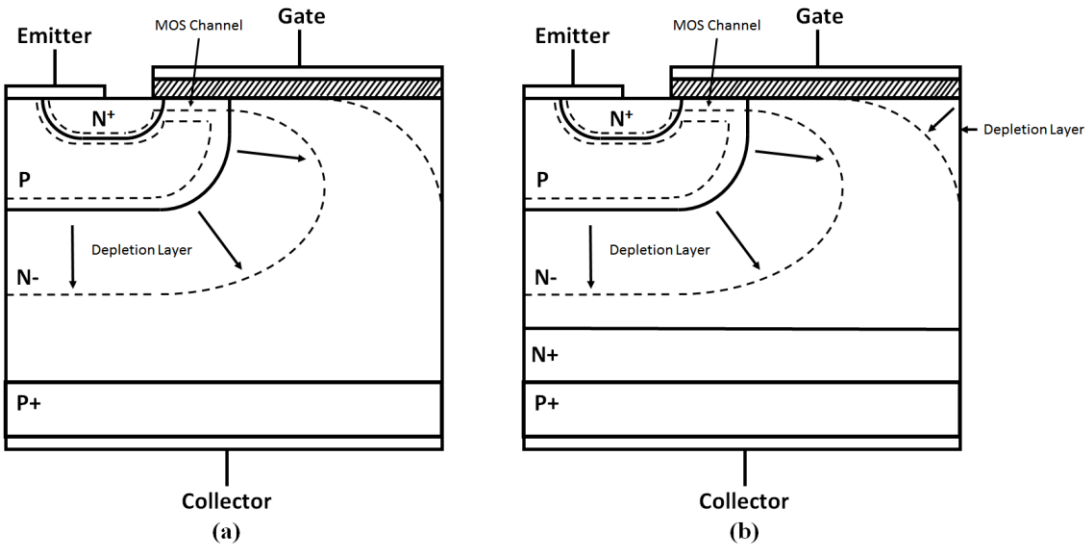


Fig. 2.7 Cross section view of a vertical (a) NPT IGBT and (b) PT IGBT.

Fig. 2.7 illustrates the cross section view of structure of two different types of IGBT known as Punch Through (PT) IGBT and Non-Punch Through (NPT) IGBTs. The difference between these two are in the N+ Buffer layer added to the P-substrate layer

in PT IGBTs. This extra buffer layer is used to avoid the failure of the device by controlling the expansion of the depletion region at high voltages using this added layer. By vertically shrinking the drift layer of the NPT IGBT to create a thin drift layer and a low doped field stop layer, a new IGBT structure was reported by Laska et al. which is known as Field Stop Non-Punch Through (FSNPT) IGBT [14]. This type of device has a very low on-state resistance and low switching energy was achieved by optimising the carrier concentration in the Charge Storage Region (CSR) [14].

Due to the conductivity modulation phenomenon and the fact that IGBTs are minority carrier devices, they exhibit a superior conduction characteristic which makes these devices a better candidate for high current power electronics applications [15]. Fig. 2.8 can be used as a guideline for choosing a suitable power switching device based on the application (i.e. Switching frequency and required power rating) [16]. As can be seen, both power MOSFETs and IGBTs are suitable for automotive application.

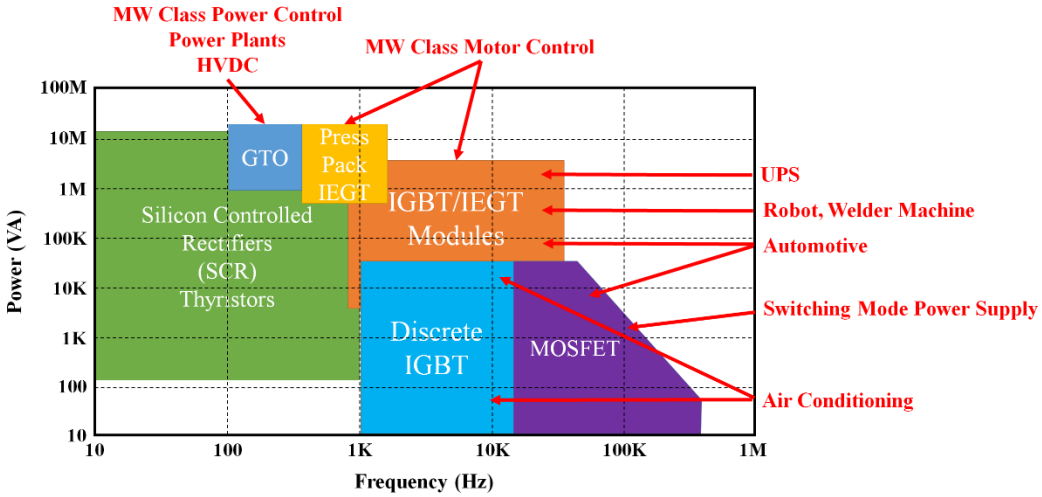


Fig. 2.8 Power vs. Frequency graph for different power switching devices.

2.2.4.3 PiN Diodes

PiN diodes are diodes with two junctions: P^+N^- and N^-N^+. A schematic of structure of a PiN diode is shown in Fig. 2.9. As can be seen, the structure of a PiN diode has an extra low N-type doped or alternately an intrinsic semiconductor layer between the conventional low power PN junction diode. This added layer is known as intrinsic region and it is responsible to block high voltage by supporting the reverse electric field across the device when it is reverse biased.

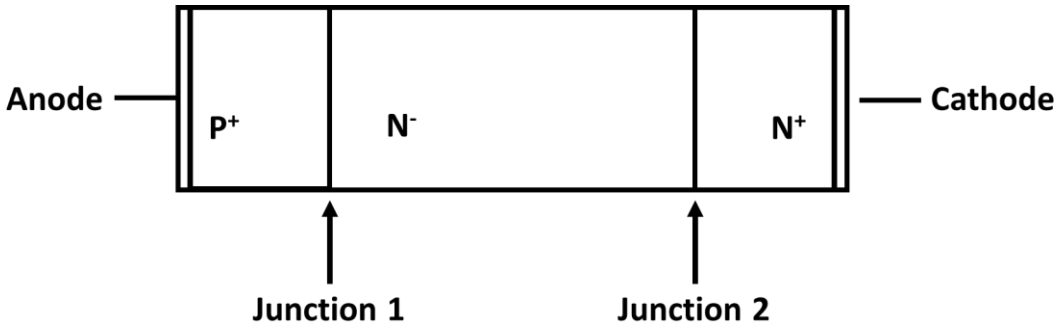


Fig. 2.9 A schematic of PiN diode structure.

In addition, during the forward operation of the device, electrons and holes diffuse from the highly doped P^+ and N^+ regions into this region and conductivity modulation phenomenon due to existence of excessive minority carriers reduces the on-state resistance of this region. PiN diodes are very popular as anti-parallel diodes in power electronic applications. The switch-off of these devices are affected by the high carrier lifetime in the drift region of the device. Consequently, in order for the device to start blocking the current, the extra charge needs to be extracted from the drift region. During the charge extraction, the direction of the current is reversed. This is known as

reverse recovery of PiN diode. The majority of losses in PiN diodes occur during the switch-off of the device. Hence, some optimisation needs to be carried out on these devices to reduce the carrier lifetime and increase the switching speed of these devices. However, these changes can affect the on-state resistance of the device and hence, there is a trade-off between the switching speed (reverse recovery time) and the on-state resistance of the device. As a result, based on the application, depending on the switching frequency and the amount forward conduction current of the device, a device with low switching loss or low conduction loss can be chosen to optimise the performance of the system and reduce the losses.

Similarly, the device starts conducting when enough charge is formed in the drift region and the depletion region disappears due to the forward voltage across the device.

2.2.4.4 Future of Power Electronic Devices

The demand for power electronics with lower losses, higher current capacity, higher blocking voltage, higher switching frequency and overall enhanced performance is rapidly increasing in all the power electronic applications from very low milliwatt level used in mobile electronics (phones, tablets and laptops) to very high voltage, high power applications such as transmission lines between countries and traction of electric trains.

A typical power switching chip, is made from several thousands of paralleled transistor cells. Increasing the number of parallel connected transistors, can potentially increase the current handling capability of the device and increase the power rating of

the device for a given blocking voltage. Increase of power capability of a power device requires heat extraction from the device. Silicon is reaching its theoretical limits in delivering high power and higher efficiency while reducing the size of the system to meet the market demand. Consequently, engineers started investigating alternative materials to replace the conventional Silicon chips with high performance materials [17-19].

Two potential candidates to be utilized in power electronics applications are SiC and GaN wide bandgap semiconductors. These materials have a wider bandgap than Silicon and hence, they have lower leakage currents at higher voltages and they can block a significantly larger voltage; this means that vertical devices made from SiC can handle higher critical electric field and hence the drift region of these devices can be significantly thinner than that of silicon devices [20]. This reduces the on-state electrical resistance of the device as well. The electrical bandgap is the energy gap difference between the conduction band in the solid material and the valence band. Fig. 2.10 shows the energy bandgap diagram for different materials [17].

Due to the superior material properties, devices made from these materials inherently have lower on-state resistance (better forward conduction) and they can switch at significantly faster switching frequencies. All in all, material properties of these wide bandgap semiconductors make them suitable for high power and high temperature applications [18, 21]. Table 2.1 compares the electro-thermal material properties of different wide bandgap semiconductors with conventional Silicon. As

explained earlier, the wide bandgap of the materials in this table, increases the electric breakdown field of the device .

All wide bandgap semiconductors show a better property in every aspect. However, there are several issues with respect to crystal growth of these materials. SiC devices can be fabricated by epitaxial growing of SiC on top of a SiC substrate. However, the technology is not as mature as Silicon crystal growth and some defects can be found in the material which reduces the reliability of the devices and reduces the mobility of the carriers and hence the performance of the device. Moreover, growing a reliable oxide layer on top of SiC devices is challenging. Fairchild Semiconductor International Inc. introduced a new SiC Bipolar Junction Transistor (BJT) which have relatively lower switching losses in all range of on resistance ($R_{(on)}$) in comparison to the other semiconductor power switching devices from the same technology. In addition, they do not have any tail current like IGBTs and hence they are able to operate fast (20 ns turn-on time and 30 ns turn-off time). Moreover, Infineon, started introducing SiC BJTs, however, they decided not to continue with these devices due to their drawbacks: The gate biasing of these devices are more complex than devices with MOS gate structure as they require current at the gate in order to conduct current in the forward bias mode [22-24].

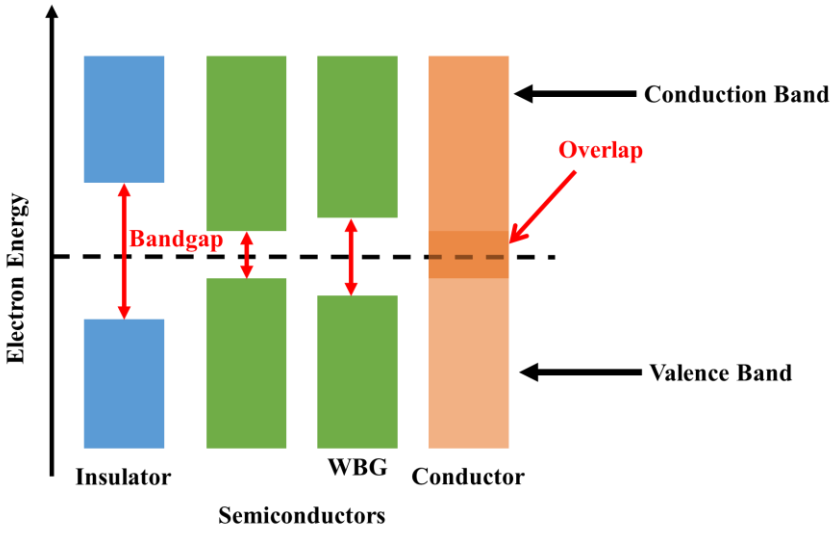


Fig. 2.10 Energy bandgap in insulators, semiconductors and conductors.

GaN devices use Silicon, SiC or sapphire substrate. Hence, GaN devices cannot be designed to be vertical and they cannot have high current density. Also, Silicon thermal resistance is significantly higher and this reduces the cooling and thermal performance of GaN device. Consequently, SiC devices are more desirable for high current, high voltage applications and GaN devices target the market of low power RF applications or lighting where highs switching frequency is required. GaN semiconductor is being used to provide energy saving, durable, long-life alternative to conventional light bulbs in form of Light Emitting Diodes (LED).

In the automotive industry, use of wide bandgap semiconductors especially SiC, promises extra power density, solves the range anxiety by offering lower losses/increased efficiency and it offers a better thermal management by reducing the size of the cooling system and hence reduction of the overall size of the inverter. Consequently, automotive industry shows strong interest in the utilisation of wide

bandgap semiconductors in the near future. One of the main factors prohibiting industry from wide scale adaption of SiC devices are high cost associated with the fabrication of SiC device. Another reason is associated with the packaging of SiC devices. Use of conventional materials to package SiC devices reduces the heat exchange and hence the thermal performance of these devices and does not allow the device to work at its maximum rating.

SiC devices can be used in vehicles with high DC voltage system; i.e. battery voltage of 800V DC to benefit from the high blocking voltage and low losses of the device. Toyota has announced that from 2020, they will commercialise their SiC-base power inverter in their EVs. Also high performance vehicles such as McLaren sports series and Formula 1 cars are using SiC power devices to benefit from the very high power to weight ratio achieved from these high performance devices.

Table 2.1 Material properties of different semiconductors.

	Material						
Property	**Si**	**GaAs**	**3C-SiC**	**6H-SiC**	**4H-SiC**	**GaN**	**Diamond**
Bandgap, E_g (eV)	1.12	1.43	2.4	3.03	3.26	3.45	5.45
Dielectric constant, ε_r^a	11.9	13.1	9.72	9.66	10.1	9	5.5
Electric breakdown field, E_c (kV/cm)	300	400	8000	2500	2200	2000	10000
Electron mobility, μ_n ($cm^2/V.s$)	1500	8500	750	500 80	1000	1250	2200
Hole mobility, μ_p ($cm^2/V.s$)	600	400	40	101	115	850	850
Thermal conductivity, λ (W/cm.K)	1.5	0.46	5	4.9	4.9	1.3	22
Saturated electron drift velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2.5	2	2	2.2	2.7

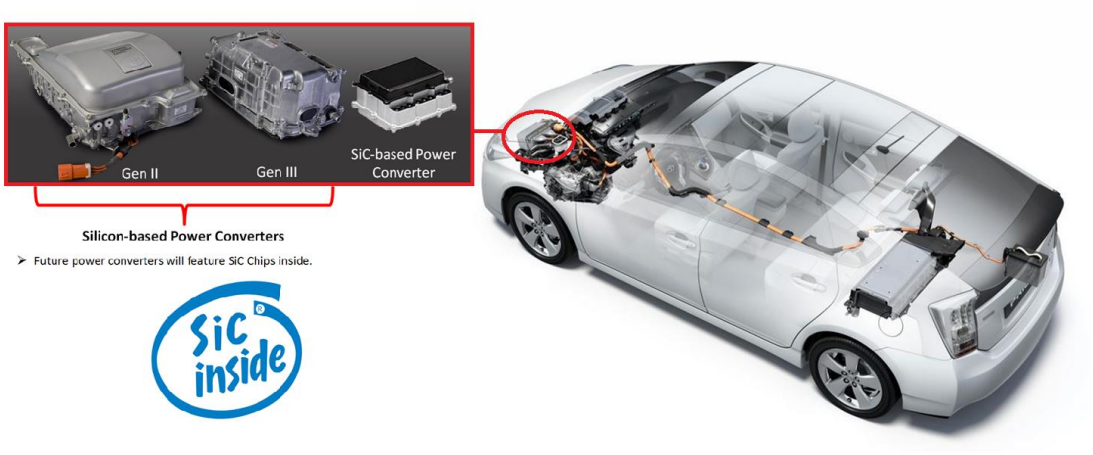


Fig. 2.11 Evolution of Toyota Prius hybrid traction power inverter and reduction of inverter size over time and the future of commercial SiC-based power inverter.

Fig. 2.11 compares the power evolution of power inverters and decreasing of the size and increasing of the power density of the inverter by using wind bandgap SiC MOSFETs in the automotive application.

2.3 Power Device Modelling

Computer Aided Engineering (CAE) tools are vital in automotive industry and this is due to the fact that using computer to model each component in a system and investigating the integrity of the whole system and subsystems can reduces the product development time and cost and reduce the risk by increasing the safety. In addition, CAE tools are being used as a method to verify the product before prototyping and they

are being used to investigate the reliability and lifetime of each component without even building and testing the device [9].

EVs and PHEV are new topics to the automotive industry and hence, the nature of the business requires vehicle manufacturing companies to be confident that products will meet all the requirements and standards and at the same time, the product is cost efficient and reliable with low failure probability according to the expected bathtub curve of the vehicle. Power electronics in electric vehicle is one of the most important parts of the electric drive and design of a power inverter is not only limited to the electrical analysis. The design phase rather requires a multi-physics approach. Modelling power electronic devices is essential to validate the electro-thermal behaviour of the device under certain drive cycles and also to validate the reliability and robustness of the devices under various conditions. This becomes more important when the integration of power electronics into the electric motor for the future vehicles is required. Also, by moving towards High Voltage (HV) systems and switching the devices under high commutation conditions at elevated switching frequencies brings about some reliability constraints for the switching power electronic devices used in automotive applications. Hence, it is very important for power electronic engineers to be able to model the operation of the device under different switching and conducting conditions and being able to predict the failure modes of the devices under such conditions. Also, accurate switching loss and conduction loss calculations helps the engineers to design an appropriate heatsink and cooling systems with correct thermal resistance and thermal capacitances.

Hence, models for power electronic devices need to consider the electro-thermal aspect of the device as well as taking the parasitic inductances of the circuit into consideration. The parasitic inductances are due to the current paths within the electrical circuit which is not desirable, but they are inevitable. The compact electro-thermal modelling tool needs to provide an accurate device behaviour and also it requires to simulate the operation of the device for a long duration of time to provide information about the temperature rise and thermal losses of each device and the whole power bridge.

There are several ways to model power electronic devices. Some of the most common way to model a power electronic device is by using behavioural models, lumped-value physics-based, detailed physics-based models, and Finite Element Models (FEM). The difference between these models are explained in Appendix C.

A combination of physics-based device model and the lumped parameter models can be used to provide information about the reliability of the device under different operational conditions. In order to take into account the impact of device modifications (such as die area, base thickness, doping, local carrier lifetime, electron/hole recombination rate, oxide thickness, MOS transconductance, etc.) in the overall performance of the power inverter, device models based on fundamental semiconductor physics are preferred. In addition, lumped component models of thermal networks can be added to make an accurate, compact and fast electro-thermal model.

A key issue in power module design is the incorporation of the inductance and capacitive coupling. Multi physics finite element modelling tools such as COMSOL can

be used to determine the parasitic inductance and resistance of the current paths within the power module. The values of lumped parasitic resistance and inductance of the layout calculated using electromagnetic finite element modelling tool can be extracted and incorporated into a circuit simulator in order to produce the current and voltage waveforms including the overshoot and undershoots arising from interaction of the device with the parasitic inductances. The capacitive coupling between the bus bar and the power module becomes of more importance in fast switching systems using SiC devices which is not explained in this work.

2.4 Reliability of Power Inverters

The reliability of power inverter is one of the key concerns in the automotive industry. In this industry safe operation of each component in a vehicle and quality of the final product requires all the components to comply with the standards and design rules. Consequently, it is important for the design engineer to be able to understand the failure mechanism and reliability constraints of the inverter and the sub-system components; such as power electronic devices used in the inverter and be able to model and predict the failure modes in the design phase. The reliability of the power inverter requires understanding of electro-thermal behaviour of the power electronic device and thermo-mechanical behaviour of the inverter. The electro-thermal behaviour of the device considers the coupling of electrical behaviour of the device with the thermal behaviour. The mechanical stress which ultimately leads to device failure can be coupled with the mechanical wear-out model to predict lifetime performance. Hence,

study of reliability of power electronic devices in an inverter is a multidisciplinary area of study which requires a comprehensive understanding of electrical operation of each device and understanding the mechanical and thermal aspect of the system.

2.4.1 Electro-Thermal Reliability

As the heat capacity of a power device is very small due to the small dimensions of the device, a rapid temperature rise within the device is imminent. Reliability of power module, requires the heat to be extracted from the device in such a way that the amount of heat generated within the device due to the conduction and switching losses does not allow the junction temperature of the device increase beyond the maximum operating temperature of the device.

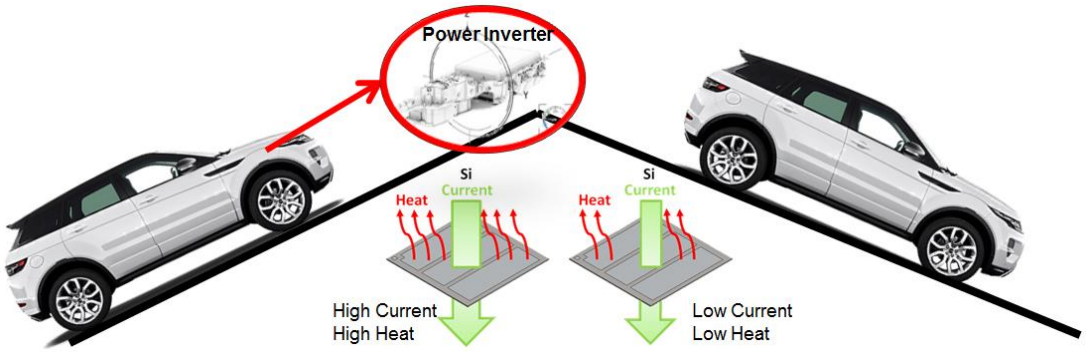


Fig. 2.12 The impact of road and driving conditions on the heat generated in power electronic devices in a hypothetical HEV.

From a system point of view, in an automotive applications where the electric motor is driven through the power inverter, the mission profile can have a significant impact on the temperature and hence stress placed on the inverter; Fig. 2.12 shows an

example of input of power losses due to higher current passing through the device, when the vehicle is going uphill versus lower current and consequently lower heat dissipation during the time that the vehicle is going downhill. This shows importance of electro-thermal modelling of power devices within the system for a given mission cycle and being able to model the electro-thermal reliability of the devices under hard switching conditions.

Up until this point we have considered only IGBTs as a switching device, however in the future higher voltage SiC-MOSFETs may become an attractive alternative, hence it is worth spending time considering the reliability aspects of these devices.

2.4.2 Thermo-Mechanical Reliability

The performance and reliability of the device is affected as the device is stressed under a particular mission profile. Power cycling is a term that is used when the device is switched on and off for a long period of time and the temperature of the device is changed actively due to the conduction and switching losses of the device. The temperature change due to power cycling leads to mechanical stress which can consequently result in device failure. Thermal cycling is a term that is used when the device is heated passively by putting the device in an environmental chamber and the temperature of the chamber is varied between two values (ΔT). The change in the temperature causes thermo-mechanical stress in the structure of the device and causes the device to degrade. Hence, it is important to understand the structure and packaging techniques used to manufacture power modules and in general power inverters in order

to understand the thermo-mechanical reliability and failure modes of power devices [25]. The power module mechanical failure due to thermal cycling are wire bond lift-off and the solder delamination. Wire bond lift-off happens when the frequency of temperature change is high and because the heat capacity of the wire bond is smaller than the rest of the package, the wire bonds degrade more rapidly. In contrast, when the temperature change is larger, but the frequency of changing is smaller, the solder layer is degraded more.

2.4.2.1 Power Electronic Packaging

As described earlier, power electronic devices are usually vertical devices; i.e. current flows vertically inside the device. Hence, an electric and thermal path needs to be prepared for the device to form the circuit as well as provide a path to extract heat from the device under operation. The process which is used to prepare the device to be used in an application (e.g. making a power inverter for automotive application) is known as packaging of power electronic devices. By having one or more power devices packaged in the same housing, a power module is created. A power module can compromise several different dies connected in parallel and series in the same package.

Typically a power module is made from a ceramic substrate which provides mechanical support for the module as well as providing a good heat path with low thermal resistance and at the same time, providing a good electrical insulation between different parts of the circuit and the high voltage side of the power module from the cooling system. The ceramic substrate is a thin layer of ceramic which is typically

sandwiched between two layers of copper. The ceramic material is usually Aluminium Oxide, also known as Alumina (Al_2O_3), Aluminium Nitride (AlN) or Silicon Nitride (Si_3N_4). Fig. 2.13 shows a SiC MOSFET power module packaged on an AlN DBC substrate.

Table 2.2 illustrates some electrical and thermal material properties of these different ceramic materials. Based on the application, cost consideration, heat and vibration that the inverter is subjected to during the application and the blocking voltage of the devices used in the application, different types of ceramic materials might be used. The thickness of the Copper at the top side depends on the current rating of the device and the power module and the amount of continuous current that the devices need to conduct under operation.

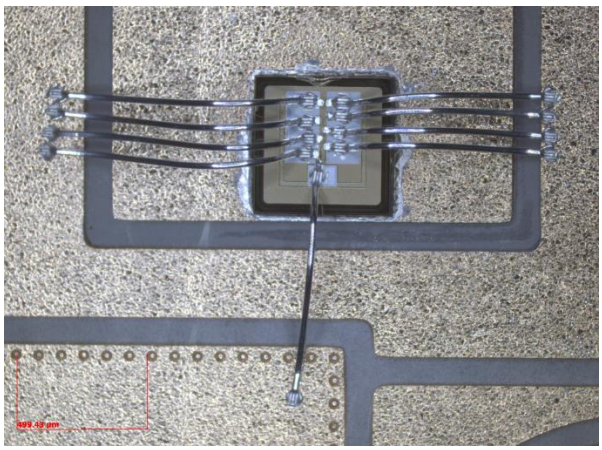


Fig. 2.13 A SiC MOSFET die packaged on AlN DBC substrate with electroless NiPdAu surface coating assembled at Warwick.

For automotive application where the required current is in the range of 400-1000A, the minimum thickness of the top side Cu is 0.3 mm. The bottom side Cu is

usually soldered to a baseplate which conducts heat from the device to the cold plate and the coolant. The Cu at top and bottom of the DBC substrate can be electro-less plated with Ni, Au or Pd or an alloy made from these three metals. This can prevent the Cu from corrosion and it can enhance the wetting and soldering profile depending on the type of solder and thickness of the coating layer.

The baseplate may be eliminated in some cases and the power module can be mounted on a single layer directly cooled by the coolant. The baseplate is usually made from a Cu which has a good thermal conductivity. Recently, Aluminium Silicon Carbide (AlSiC) is being used as an alternative to Cu which is lighter and has a better thermal conductivity.

Table 2.2 Ceramic DBC substrate material properties

Properties	AlN	Al_2O_3	Si_3N_4	Si
Bending Strength/Flexural Strength (MPa)	350	320	689	
Dielectric Constant (@ 1MHz)	8.8	9.8	4.5~7.4	
Coefficient of Thermal Expansion ($\times 10^{-6}$/°C)	4.6	7.6	3.3	2.6
Thermal Conductivity (W/m.K)	180~200	18	29	
Breakdown Voltage (kV/mm)	14	15	100	

During the fabrication of power electronic devices, a metallic contact is needed for the semiconductor in order to create an electric path for electrons and holes to flow into the device. The metallization is usually carried out by deposition of Nickel and Aluminium/Titanium Ohmic contact metals on top of the semiconductor followed by

rapid thermal annealing of the contact in inert ambient (Ar) to form the Ohmic contact [26]. Next, an additional layer of Aluminium is formed on top (metal overlay) to prepare the device for packaging process [27]. At the bottom side of the device, a layer of Ti/Ni is deposited followed by deposition of a layer of silver (Ag) to prepare the device for the back side packaging process[28]. The device is mounted on top of the DBC substrate by solder reflow process.

In order to connect the top side of the device to other parts of the circuit, wire bonds are used. Wire bonds are thin wires, typically Aluminium (Al), which are connected to the top side of the device using ultrasonic welding process.

As can be seen, a power module is made from stack of different layers of materials on top of each other. Fig. 2.14 shows a cross section view of a hypothetical power inverter. As can be seen, different materials are bonded on top of each other.

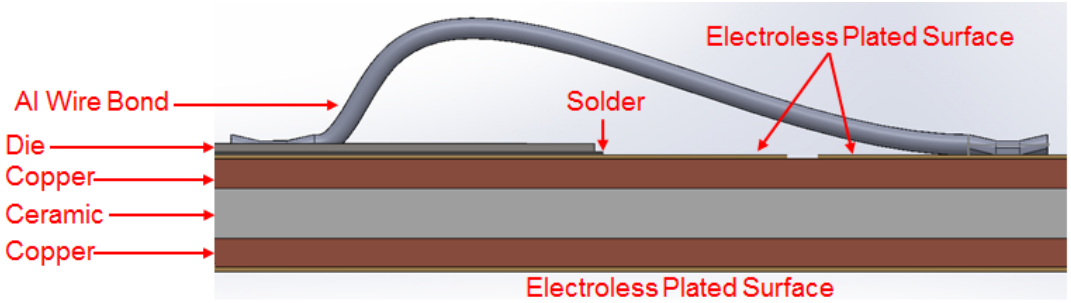


Fig. 2.14 A cross section view of a conventional power module packaging showing stack of different materials on top of each other.

One of the most important material properties which needs to be considered during the design of an inverter, is the Coefficient of Thermal Expansion (CTE) of different materials. CTE is the parameter that determines how much an object will

expand when the temperature of the object subjected to heat changes for one degree Celsius in a constant pressure. If the materials stack on top of each other in a power module have different CTE, then when the temperature of the inverter increases, different layers tend to expand at different rates. This can lead to solder delamination and/or wire bond lift-off which are two main common thermo-mechanical failure modes in power modules [29]. Repeated stress cycles below the tensile strength of the material is known as fatigue and both electro-thermal failure modes mentioned above are as a consequence of thermal fatigue.

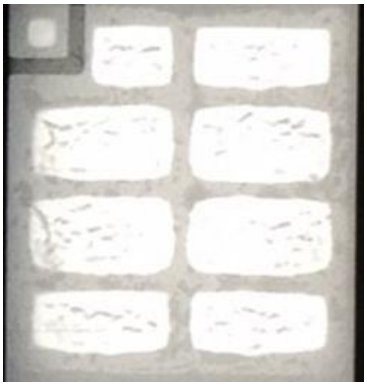


Fig. 2.15 Solder voids at zero power cycling.

Bond wire lift-off usually happens when a crack propagates at the junction between the bond wires and the die and this crack electrically disconnects the wire from the surface of the device.

During the solder reflowing process, the flux inside the solder paste and also the trapped air inside the solder between the die and the DBC substrate results in existence of voids which are hollow spaces under the die in the solder area to form under the device. This reduces the contact between the device and the substrate and if the

percentage of voids under the device becomes high, this can result in poor electrical performance and in long term it can cause reduce the lifetime and result in reliability issues. Fig. 2.15 shows an X-Ray image of a solder layer processed using ATV reflow oven at the University of Warwick at zero power cycling. In this image, the white colour indicates solder layer and the narrow grey lines in the solder layer indicates the voids formed during the soldering process.

Table 2.3 shows thermal properties of several different materials that are used in power electronics. As can be seen, the CTE of Cu, Al and solder layers are significantly higher than the other layers of materials. Hence, the expansion rate at these layers are greater than the expansion rate at the die and hence, stress builds up at the junctions between these materials.

Table 2.3 Thermal properties of different materials used in power electronics packaging [30].

	AlN	Al_2O_3	Si_3N_4	Si	SiC	AlSiC	Al	Cu	Solder
Coefficient of Thermal Expansion ($\times 10^{-6}$/°C)	4.6	7.6	3.3	2.6	4	6.9	22.2	16.6	21.4
Thermal Conductivity (W/m.K)	180~200	18	29	130	120	150	205	385	61.1

As explained earlier, the change in the junction temperature of the power devices in an inverter under operation is the main cause of thermal fatigue and hence the abovementioned failure modes of the power inverters. Consequently, it is important to be able to model and accurately calculate the temperature rise of the device under

different conditions to be able to predict the changes in the junction temperature of an automotive power inverter.

Part I

Chapter

3 Introduction to Modelling

3.1 Compact Device Models

Physics-based power device models based on fundamental semiconductor physics can accurately predict both the transient and static performance of power devices and allow the evaluation of the device performance at the system level. This chapter introduces the essential semiconductor physics used to model devices such as IGBTs, PiN diodes and SiC MOSFETs. In addition, the temperature dependent parameters for each of the devices are explained thoroughly in this chapter.

3.2 Semiconductor Physics

The crystal structure and resulting band diagrams of a semiconductor are the basis for calculating the fixed and mobile carrier densities in a semiconductor and can

be found in text books [31, 32]. A brief explanation of these fundamentals can be found in Appendix D.

3.3 Power Electronic Devices

This section introduces the structure of the physics behind the models used in this thesis.

3.3.1 P-N Junction

One of the basic building blocks in semiconductor devices is the P-N junction. This junction consists a P-type doped region of semiconductor in contact with an N-type doped region of semiconductor. Such a junction, allows current to flow in one direction and blocks the current in another direction. It is a constituent part of virtually all power devices and so it is important to understand how this operates in detail.

Fig. 3.1 illustrates a simplified One-dimensioned view of an abrupt P-N junction structure. As shown in the diagram, the doping in the P and N regions are assumed to be uniformed and the transition between the two regions is abrupt. This assumption serves as well in understanding the operation of the structure. The metal contacts are assumed to be Ohmic.

Depending on the applied bias, three different operating regions need to be considered: (a) equilibrium $V_{ak} = 0$V, (b) Forward bias $V_{ak} > 0$V and (c) Reverse bias $V_{ak} < 0$V.

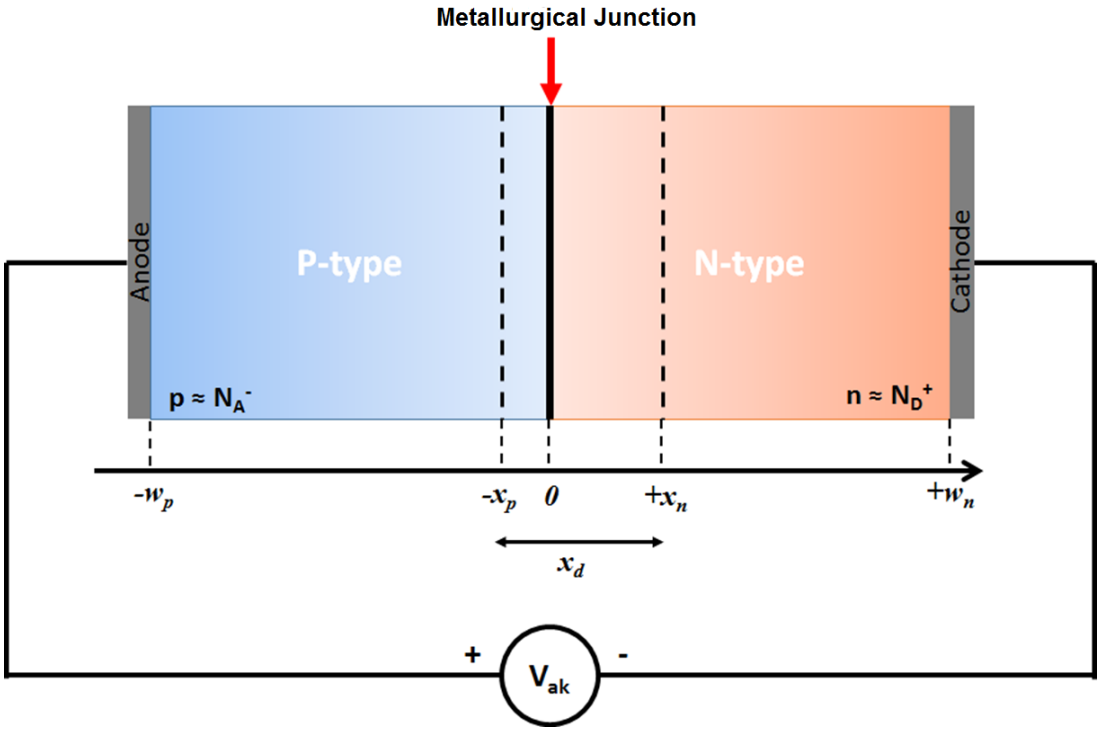


Fig. 3.1 A diagram of P-N junction structure.

When two opposite doped regions are connected together, in thermal equilibrium, electrons in the N-doped region diffuse to the P-type doped region and vice versa. This leaves a region depleted of carriers in the region close to the junction. The regions empty from carriers at the junction are referred to as depletion region which establishes an electric field in the opposite direction, which prevents further depletion. Eventually, an equilibrium is established and at that point the field develops a potential drop defined by equation (3.1).

$$\Phi_{bi} = V_T \ln \frac{N_A N_D}{n_i^2} \tag{3.1}$$

In this equation N_A and N_D are the doping level of the acceptor and donor type semiconductors respectively. Both thermal voltage ($V_T = kT/q$) and intrinsic carrier concentration (n_i) are temperature dependent and so Φ_{bi} is temperature dependent, and consequently, the in-built voltage reduces with increasing temperature. Fig. 3.2 shows the built in voltage and the electric field across a P-N junction when there is no voltage applied. The depletion width (x_d) can be calculated based on the doping of the P and N region and Poisson's equation. E_0 is the peak electric field at the metallurgical junction.

$$E_0 = -\frac{qN_D x_n}{\varepsilon_s} = -\frac{qN_A x_p}{\varepsilon_s} \tag{3.2}$$

$$x_d = x_n + x_p = -\frac{\varepsilon_s E_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right) \tag{3.3}$$

If the P-type is highly doped and the N-type is lightly doped, then the depletion width on the P-type (x_p) will be significantly smaller than the depletion on the N-type side (x_n) and the junction is said to be asymmetrically doped. The electro-static potential is related to the area under the electric field curve, hence, by integrating the electric field across the P-N junction, the depletion voltage is obtained:

$$V_d = -\frac{E_0 x_d}{2} = \frac{q x_d^2}{2\varepsilon_s}\left(\frac{N_A N_D}{N_A + N_D}\right) \tag{3.4}$$

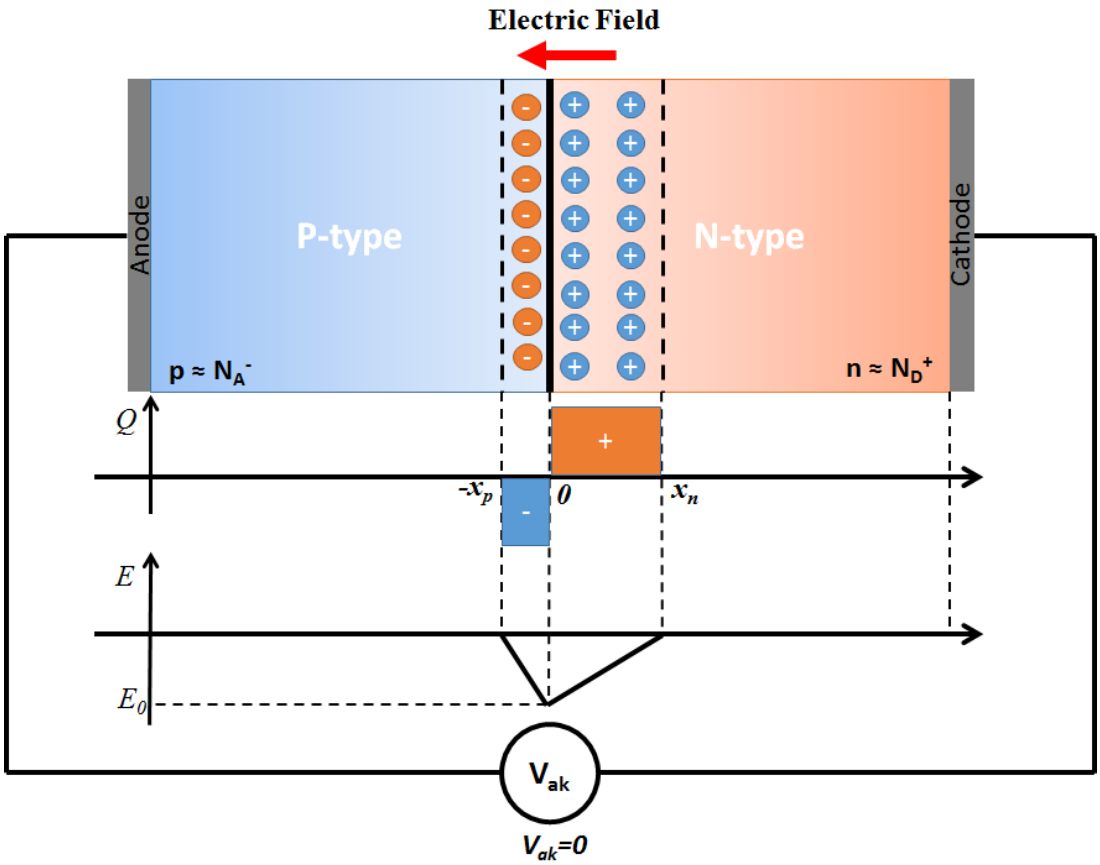


Fig. 3.2 Built-in potential at P-N junction when no voltage is applied to the ends of the structure.

In case scenario (b), when positive voltage is applied to the P-N junction; a positive voltage to is applied to the Anode with respect to the Cathode, current will flow and it is said to be forward bias. By applying a forward bias, the depletion region starts shrinking until the depletion disappears and the carriers can flow easily through the device. The voltage dependent depletion widths can be calculated as:

$$x_d = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\cdot|V_d|} \qquad (3.5)$$

In this equation V_d is the voltage drop across the junction and is equal to the external voltage applied to the structure minus the built-in voltage of the PN junction ($V_d = |V_{ak} - \Phi_{bi}|$). When a negative voltage is applied to Anode with respect to the Cathode terminals (c), the depletion width expands and the device blocks the flow of current. The maximum voltage that the device can withstand depends on the doping of the P and N regions, width of these regions and the breakdown field of the semiconductor. In power electronic applications, a wide N-type doping region is generally used to provide the required blocking voltage. This forms the blocking region which supports the high voltage in reverse bias for all power devices and is usually referred to as the drift region.

3.3.2 PiN Diode

The asymmetric junction described above, is the structure used in PiN diodes to block the reverse bias. Fig. 3.3 shows a typical PiN diode structure along with the electric field across the device. In forward bias the PiN diode operates using the high level injection of carriers into the lightly doped drift region of the device (which without high level injection will have a high resistivity). In high power, high current applications, it is clearly not desirable to have high on-state resistance. High level injection of carriers in the PiN diode brings about a phenomenon that is referred to as conductivity modulation which is specific to bipolar power devices such as PiN diode, BJT, IGBT, and thyristors and vastly reduces the on-state resistance.

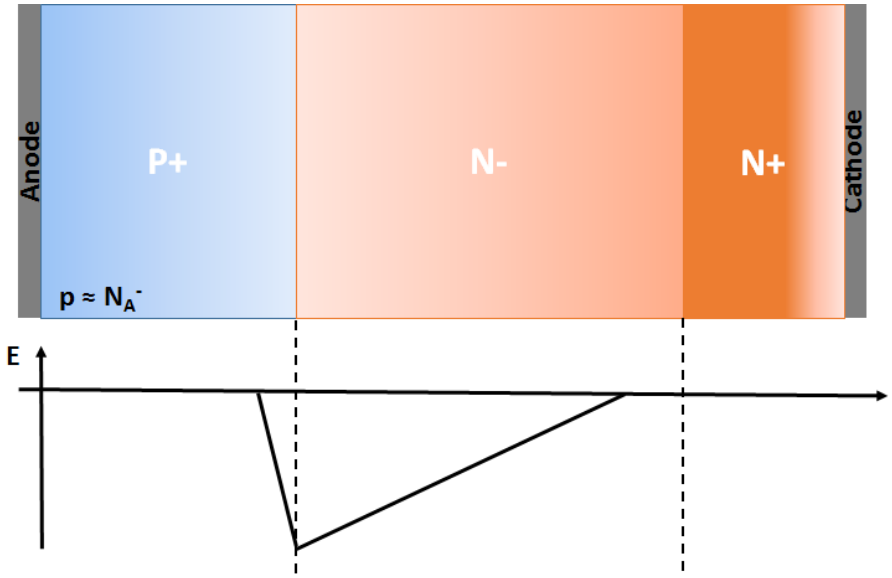


Fig. 3.3 PiN diode structure and the electric field across the device.

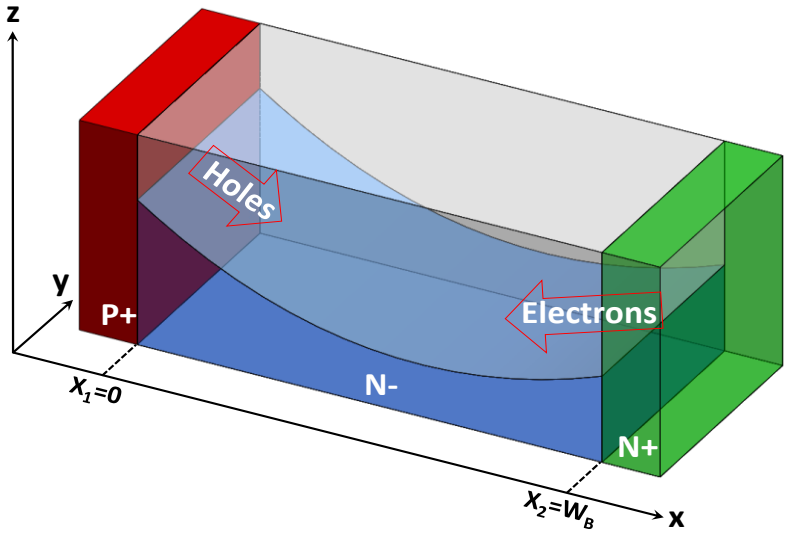


Fig. 3.4 3D diagram of a PiN diode with formation of charge storage region.

Under forward bias, electrons are injected to the N-drift region from the N^-N^+ junction and holes are injected to the drift region from P^+N^- junction. High level of carrier injection in the drift region, means that mobile charge is stored in the drift

region of the device. At very high current densities, the concentration of the carriers stored in the drift region becomes much greater than the background doping of the drift region. The charge stored in the drift region of the PiN diode is in form of catenary shape and is shown in Fig. 3.4.

Charge neutrality requires that the concentration of electrons and holes in the drift region be equal to each other. Hence, the electron and hole drift and diffusion currents shown in Appendix D, equations (D.19) and (D.20), can be re-written as below:

$$\frac{J_n}{q\mu_n} = pE + V_T \frac{\partial p}{\partial x} \tag{3.6}$$

$$\frac{J_p}{q\mu_p} = pE - V_T \frac{\partial p}{\partial x} \tag{3.7}$$

The total current is sum of electron and hole currents in equations (3.6) and (3.7) and by combining these two:

$$J_p = \frac{J}{q}\left(\frac{\mu_p}{\mu_n + \mu_p}\right) - \left(\frac{2\mu_n\mu_p V_T}{\mu_n + \mu_p}\right)\frac{\partial p}{\partial x} \tag{3.8}$$

Replacing the current density of holes in equation (3.8) into continuity equation which is one of the basic semiconductor physics equation and is shown (D.24) results:

$$\left(\frac{2\mu_n\mu_p V_T}{\mu_n + \mu_p}\right)\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{\partial p(x,t)}{\partial t} + (G_p(x,t) - R_p(x,t)) \tag{3.9}$$

$$D = \frac{2\mu_n \mu_p V_T}{\mu_n + \mu_p} = \frac{2D_n D_p}{D_n + D_p} \tag{3.10}$$

Where D is known as the ambipolar diffusion constant. In this equation, G_p and R_p denote the hole generation and recombination mechanisms which are function of time and space. Shockley-Read-Hall recombination is the most dominant recombination mechanism in Silicon with Auger recombination dominating at high injection levels, and can be written as:

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{\partial p(x,t)}{\partial t} + \left(\frac{np - n_i^2}{\tau_n(p + n_i) + \tau_p(n + n_i)}\right) \tag{3.11}$$

Assuming the concentration of injected carriers are significantly higher than the background doping level due to high level injection and charge neutrality, this equation can be expressed as:

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{\partial p(x,t)}{\partial t} + \frac{p(x,t)}{\tau_n + \tau_p} \tag{3.12}$$

In which τ_n and τ_p are carrier electron and hole lifetime in seconds respectively. Sum of these two lifetimes is high-level carrier lifetime in seconds.

$$\tau = \tau_n + \tau_p \tag{3.13}$$

Replacing the high level carrier lifetime in equation (3.12) results in the ambipolar diffusion equation which explains the concentration of minority carriers in the drift region of the device in time in one dimension (x).

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t} \tag{3.14}$$

This determines the diffusion of the mobile carriers in the drift region and it determines the carrier concentration throughout the plasma region in the drift region. This equation does not have an analytical solution (except in steady state) as it requires boundary conditions and the boundary conditions are time and space dependant. However, the equation may be reconstructed and solved using numerical techniques. In this work we use a Fourier series to approximate the evolution of the plasma as the device switches.

As shown in Fig. 3.4, the concentration of carriers near to the PN^- and N^-N^+ junctions are higher than the centre of the drift region. Due to this high level of carrier concentration at these junctions, the minority carriers flow into the P^+ and N^+ regions and they recombine with holes and electrons respectively. The current flow due to the emitter recombination can be expressed as:

$$J_{n(PN^-)} = qh_p(p_{(PN^-)})^2 \tag{3.15}$$

$$J_{p(N^-N^+)} = qh_n(p_{(N^-N^+)})^2 \tag{3.16}$$

In these equations, h_n and h_p are the recombination rates of electrons and holes at the emitter respectively and they can be expressed as a function of diffusivity and carrier lifetime and the carrier concentration (basically doping). The emitter recombination equations are equivalent to the minority carrier saturation currents [9, 33-35].

$$h_p = \frac{1}{p_{(P^+)}} \sqrt{\frac{D_{n(P^+)}}{\tau_{n(P^+)}}} \tag{3.17}$$

$$h_n = \frac{1}{p_{(N^+)}} \sqrt{\frac{D_{p(N^+)}}{\tau_{p(N^+)}}} \tag{3.18}$$

During the switch-off of the device, the charge stored in the drift region will need to be extracted and the depletion regions need to form in order for the PiN diode in order to block current and the reverse voltage be blocked across the width of the device.

Fig. 3.5 shows the measured turn-off switching waveform of a PiN diode. As can be seen, during the turn-off of the diode, the current becomes negative which results from stored charge being extracted from the device. This negative current passing through the device is known as reverse recovery. Fig. 3.5 is obtained from a clamped inductive switching test, which is carried out to characterise the switching of diodes and IGBT/MOSFETs (body diode).

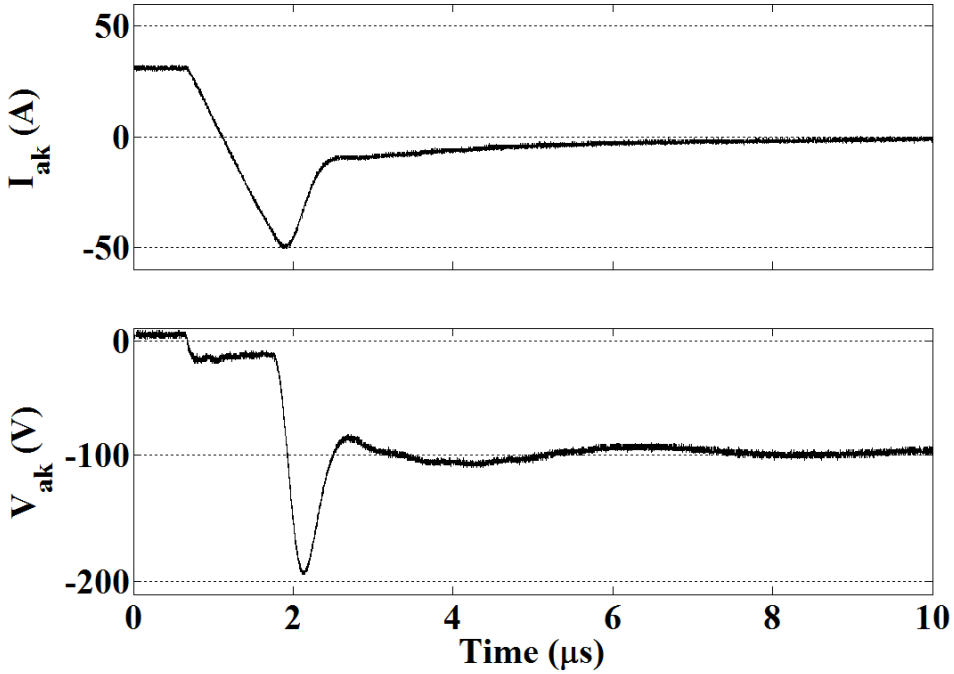


Fig. 3.5 A typical PiN diode (IRF HF50D120ACE) current and voltage turn-off switching waveforms measured at Warwick.

Fig. 3.6 shows a schematic of a clamped inductive switching circuit. During this test a double pulse is applied to the gate of the switching device. During the first pulse, the inductive load is charged and during the second pulse, the turn-off behaviour of the device under test (diode) is captured. The negative current of the PiN diode during this test is consequence of commutation of the current from the PiN diode to the switching device. The rate of current commutation depends on the rate of voltage drop across the stray inductance of the switching device and the switching rate of the bottom side device (determined by the gate resistance of the switching device, R_G). The area underneath the current curve in the negative section is equal to the amount of charge which is stored in the device and needs to be extracted in order for the device to fully switch-off.

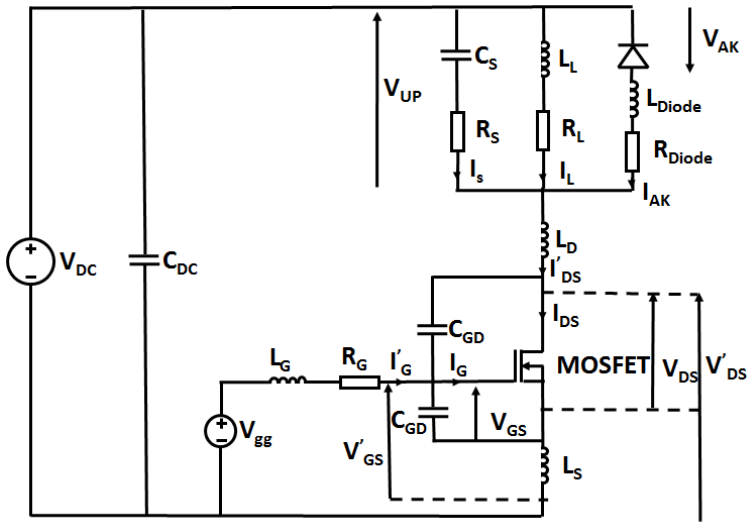


Fig. 3.6 Clamped inductive switching circuit.

The charge stored in the drift region of the PiN diode defines the switching speed of the device and as can be seen, during the switching of the device both current and voltage exist. Consequently, the power loss of the device which is voltage multiplied by the current, is high. Moreover, although the losses in diode is smaller than the transistor in the same circuit, but the turn-off losses of the PiN diode have the largest contribution in the losses and heat generation of the anti-parallel diode under operation. This further demonstrates the importance of modelling the transient behaviour of the plasma in bipolar devices.

When the switching device is turned on, the voltage across it starts to fall down and the current commutes from the diode to the switching device. When the direction of the current changes from positive to negative, the depletion region(s) at P^+N^- (and N^-N^+) junction(s) start forming and the electric field at the edges of the drift region starts to increase and drift region expands until the device becomes fully depleted and the

depletion regions join in the drift region. When the switching device turns on the current transfers from the diode. This causes a reduction in the voltage drop across the stray inductance (L_D) in circuit schematic of Fig. 3.6. Hence, the switching device current stops increasing and this results in the peak of the reverse recovery current waveform. After this peak, the current in the diode returns to zero. During this period of time when the current is returning to zero from the peak reverse current, the depletion regions are formed and the remaining charge stored in the drift region is annihilated by recombination in the drift region and the rate of change of the current is determined by the recombination rate and carrier lifetime in the diode. During this time, as the depletion region expands and charge is extracted and annihilated, the voltage across the diode decreases towards the off-state voltage which is determined by the DC link voltage of the circuit. Any oscillation in the voltage waveform is due to the reduction of the device capacitance as the charge in the drift region is disappearing. This coupled with the stray inductance of the circuit brings about this oscillations.

Fig. 3.7 shows the calculated extraction of charge the PiN diode at different points in time during the switch-off of the diode. As can be seen, the carrier concentration is high initially and the carrier concentration has a catenary shape. Once, the switching device turns-on, the charge is extracted from both ends of the device until the charge storage region shrinks and the remaining charge is recombined in the drift region.

The opposite of this happens during the turn-on of the diode. The voltage across the diode reduces the electric field and the depletion layer retract until they disappear

the edges of the drift region and then the carriers start flowing to the device from both ends to form the charge storage region.

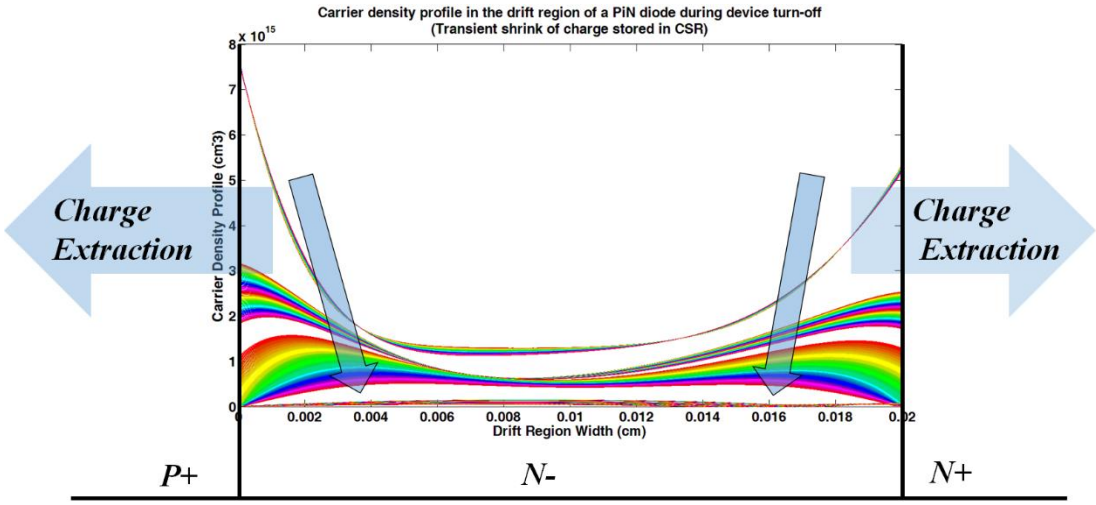


Fig. 3.7 Extraction of charge from the drift region during turn-off of PiN diode.

In order to model these transients, as well as the static behaviour of a PiN diode, the ambipolar diffusion equation needs to be solved, subject to the constraints imposed by the external circuit. The ambipolar diffusion equation is a parabolic partial differential equation identical to the heat diffusion equation which can be reconstructed using Fourier series. Similarly, the ambipolar diffusion equation may be reconstructed using Fourier series if boundary conditions for this equation are defined. Fig. 3.8 shows the charge storage region and x_1 and x_2 are the points where the excess carrier concentrations fall to zero and thus define the extent of the depletion region. When in forward bias, they are located at the ends of the drift region and they start moving towards the middle of the drift region as the depletion region starts to grow.

Here, we are using a one-dimensional representation of the plasma, however, the technique can be extended to multiple dimensions. By multiplying each side of equation (3.14) in $\cos(\pi k(x-x_1)/(x_2-x_1))$ and integrating with respect to x, the space between x_1 and x_2 the following equations are obtained:

$$D\int_{x_1}^{x_2}\frac{\partial^2 p(x,t)}{\partial x^2}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx = \int_{x_1}^{x_2}\frac{p(x,t)}{\tau}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx + \int_{x_1}^{x_2}\frac{\partial p(x,t)}{\partial t}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx \tag{3.19}$$

$$D\left(\frac{\partial p(x,t)}{\partial x}\Big|_{x_2}(-1)^k - \frac{\partial p(x,t)}{\partial x}\Big|_{x_1}\right) - D\left(\frac{\pi k}{x_2-x_1}\right)^2\frac{x_2-x_1}{2}p_k(t) = \frac{x_2-x_1}{2\tau}p_k(t) + \int_{x_1}^{x_2}\frac{\partial p(x,t)}{\partial t}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx \tag{3.20}$$

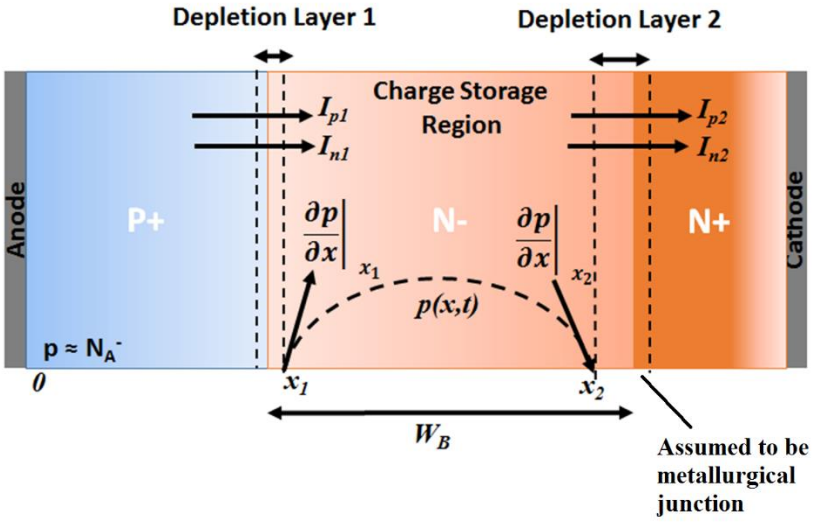


Fig. 3.8 Charge storage region in a hypothetical PiN diode.

By expanding the carrier concentration profile in the drift region in time and space domain using Fourier series we have:

$$
\begin{aligned}
&p(x,t) = p_0(t) + \sum_{n=1}^{\infty} p_n(t)\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)\\
&where:\\
&p_0(t) = \frac{1}{(x_2-x_1)}\int_{x_1}^{x_2} p(x,t)dx\\
&p_k(t) = \frac{2}{(x_2-x_1)}\int_{x_1}^{x_2} p(x,t)\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)dx
\end{aligned}
\tag{3.21}
$$

By differentiating the abovementioned expansion of the carrier concentration profile to time, we have:

$$
\begin{aligned}
&\frac{\partial p(x,t)}{\partial t} =\\
&\frac{dp_0}{dt} + \sum_{\substack{n=1\\ n\neq}}^{\infty}\left[\frac{dp_n}{dt}\cos\left(\frac{\pi n(x-x_1)}{x_2-x_1}\right) + p_n\frac{d}{dt}\left[\cos\left(\frac{\pi n(x-x_1)}{x_2-x_1}\right)\right]\right]\\
&+\frac{dp_k}{dt}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right) + p_k\frac{d}{dt}\left[\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)\right]
\end{aligned}
\tag{3.22}
$$

$$
\begin{aligned}
&\frac{\partial p(x,t)}{\partial t} =\\
&\frac{dp_0}{dt} + \sum_{\substack{n=1\\ n\neq}}^{\infty}\left[\frac{dp_n}{dt}\cos\left(\frac{\pi n(x-x_1)}{x_2-x_1}\right)\right.\\
&\left.+ p_n\left[\frac{n\pi}{x_2-x_1}\sin\left(\frac{\pi n(x-x_1)}{x_2-x_1}\right)\left[(x_2-x)\frac{dx_1}{dt} + (x-x_1)\frac{dx_2}{dt}\right]\right]\right]\\
&+\frac{dp_k}{dt}\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right) + p_k\frac{d}{dt}\left[\cos\left(\frac{\pi k(x-x_1)}{x_2-x_1}\right)\right]
\end{aligned}
\tag{3.23}
$$

By replacing equation (3.23) in (3.20) the following expression is obtained:

$$D\left(\frac{\partial p(x,t)}{\partial x}\Big|_{x_2}(-1)^k-\frac{\partial p(x,t)}{\partial x}\Big|_{x_1}\right)-D\left(\frac{\pi k}{x_2-x_1}\right)^2\frac{x_2-x_1}{2}p_k(t)=$$
$$\frac{x_2-x_1}{2\tau}p_k(t)+\sum_{\substack{n=1\\n\neq k}}^{\infty}\frac{n^2p_n}{n^2-k^2}\left[\frac{dx_1}{dt}-(-1)^{n+k}\frac{dx_2}{dt}\right] \tag{3.24}$$
$$+\frac{x_2-x_1}{2}\frac{dp_k}{dt}+\frac{p_k}{4}\left[\frac{dx_1}{dt}-\frac{dx_2}{dt}\right]$$

The final form of the solution to the ambipolar diffusion equation using Fourier series can be written as below:

$$k=0:$$
$$\frac{D}{(x_2-x_1)}\left[\frac{\partial p}{\partial x}\Big|_{x_2}-\frac{\partial p}{\partial x}\Big|_{x1}\right]=\frac{dp_0}{dt}+\frac{p_0}{\tau}+\frac{1}{(x_2-x_1)}\sum_{n=1}^{\infty}p_n\left[\frac{dx_1}{dt}-(-1)^n\frac{dx_2}{dt}\right]$$

$$k>0:$$
$$\frac{2D}{(x_2-x_1)}\left[\frac{\partial p}{\partial x}\Big|_{x_2}(-1)^k-\frac{\partial p}{\partial x}\Big|_{x1}\right]=\frac{dp_k}{dt}+p_k\left[\frac{1}{\tau}+\frac{D\pi^2k^2}{(x_2-x_1)^2}\right] \tag{3.25}$$
$$+\frac{2}{(x_2-x_1)}\left[\sum_{\substack{n=1\\n\neq k}}^{\infty}\frac{n^2p_n}{n^2-k^2}\left[\frac{dx_1}{dt}-(-1)^{n+k}\frac{dx_2}{dt}\right]+\frac{p_k}{4}\left[\frac{dx_1}{dt}-\frac{dx_2}{dt}\right]\right]$$

The carrier lifetime and doping of the drift region is assumed to be constant through-out the drift region of PiN diode in this equation. However, device manufacturers control the carrier doping and also they control the carrier lifetime. A PiN diode model based on Fourier series reconstruction of carriers in the drift region with a variable carrier lifetime is modelled in [33, 35].

As can be seen from equation (3.25), solution of the ambipolar diffusion equation requires the carrier density gradient at the edges of the Charge Storage Region (CSR) ($\partial p/\partial x$ at x_1 and x_2), the position of which (x_1 and x_2), the differential of the boundary positions which shows the rate of expansion or shrinkage of the carrier storage region, and the carrier concentration at x_1 and x_2 when there is no depletion region (CSR exists). The boundary condition for the carrier density gradient at the two depletion regions can be obtained using equation (3.26):

$$\frac{\partial p}{\partial x} = \frac{1}{2qA}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right) \tag{3.26}$$

Now that the transients of the carrier concentration in the drift region is obtained using the Fourier series, the voltage drop across the drift region can be calculated. The current equations (3.6) and (3.7) are used and it is assumed that due to conductivity modulation phenomenon, the free carriers in the lightly doped plasma region is equal to the number of holes plus the background doping of the drift region ($n = p + N_B$).

$$J = qE\left(p\left(\mu_n + \mu_p\right) + \mu_n N_B\right) + qV_T\left(\mu_n - \mu_p\right)\frac{\partial p}{\partial x} \tag{3.27}$$

By integrating the electric field (E) in the equation above between x_1 and x_2 the voltage drop equation can be achieved.

$$V_B = \frac{J}{q}\int_{x1}^{x2}\frac{dx}{p\left(\mu_n + \mu_p\right) + \mu_n N_B} - V_T\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\int_{p_{x1}}^{p_{x2}}\frac{dp}{p} \tag{3.28}$$

By knowing the carrier concentration profile based on the Fourier series solution to the ambipolar diffusion equation, integrating the charge by dividing the CSR into M finite number of segments with carrier distribution of p_T and assuming linear approximation in the integration of the charge, the voltage drop in the drift region can be approximated as below:

$$V_B \cong \frac{J}{q(\mu_n+\mu_p)}\frac{x_2-x_1}{M-1}\sum_{k=0}^{M-1}\left[\frac{1}{p_{T(k)}-p_{T(k-1)}}\ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right)\right] - V_T\left(\frac{\mu_n-\mu_p}{\mu_n+\mu_p}\right)\ln\left(\frac{p_{x2}}{p_{x1}}\right) \tag{3.29}$$

$$p_{T(k)} = p\left(x_1+\frac{k(x_2-x_1)}{M-1}\right)+\frac{\mu_n N_B}{\mu_n+\mu_p} \tag{3.30}$$

The depletion widths at the two junctions can be written using equations (3.31) and (3.32). As shown in Fig. 3.8, the current due to electrons and holes at P^+N^- junction are I_{n1} and I_{p1} respectively and the current due to electrons and holes at N^-N^+ junction are I_{n2} and I_{p2} respectively. The total current passing through the diode is equal to sum of current components passing through junction 1 and this is also equal to the sum of electron and hole currents passing through junction 2. As explained earlier, the current due to movement of carriers can be due to drift, diffusion and displacement currents.

$$W_{d1} = \sqrt{\frac{2\varepsilon V_{d1}}{qN_B + \frac{|I_{p1}|}{Av_{sat}}}} \tag{3.31}$$

$$W_{d2} = \sqrt{\frac{2\varepsilon V_{d2}}{qN_B + \frac{|I_{n2}|}{Av_{sat}}}} \tag{3.32}$$

The currents due to movement of carriers at the two abovementioned junctions are as below:

$$I_{n1} = qAh_p p_{x1}^2 \tag{3.33}$$

$$I_{p2} = qAh_n p_{x2}^2 \tag{3.34}$$

$$I_{p1} = I_{AK} - I_{n1} - I_{disp1} \tag{3.35}$$

$$I_{n2} = I_{AK} - I_{p2} - I_{disp2} \tag{3.36}$$

The displacement current during the changes in the depletion regions are calculated using equations (3.37) and (3.38) as below:

$$I_{disp1} = \frac{\varepsilon A}{W_{d1}} \frac{dV_{d1}}{dt} \tag{3.37}$$

$$I_{disp2} = \frac{\varepsilon A}{W_{d2}} \frac{dV_{d2}}{dt} \tag{3.38}$$

The depletion layer voltages are obtained using a proportional control and are a function of the carrier concentration at the boundaries of the depletion layer. The feedback gain for the proportional control is K_{FV}. The depletion regions form when the carrier concentration crosses zero. Using a similar technique as in op-amp circuit application for zero crossing detection is used to determine if the depletion region is active and next using the high proportional gain, the voltages at the depletion layers are approximated. Moreover, this feedback loop helps the convergence and stability of the model (Appendix D) [9].

$$V_{d1} = \begin{cases} 0 & p_{x1} > 0 \\ -K_{FV}\, p_{x1} & otherwise \end{cases} \tag{3.39}$$

$$V_{d2} = \begin{cases} 0 & p_{x2} > 0 \\ -K_{FV}\, p_{x2} & otherwise \end{cases} \tag{3.40}$$

The boundaries of the depletion layer are defined using the depletion region widths at the two junctions of the PiN diode and are expressed using equations (3.41) and (3.42). As shown in Fig. 3.8, W_B is the width of the intrinsic layer of the PiN diode and is in *cm*.

$$x_1 = W_{d1} \tag{3.41}$$

$$x_2 = W_B - W_{d1} \tag{3.42}$$

Using equation (3.26), the depletion layer boundary condition for the derivative of the carrier concentration at the edges of the CSR can be written using the current equations (3.33) to (3.37) as below:

$$\left.\frac{\partial p}{\partial x}\right|_{x1} = \frac{1}{2qA}\left(\frac{I_{n1}}{D_n} - \frac{I_{p1}}{D_p}\right)$$

$$\left.\frac{\partial p}{\partial x}\right|_{x2} = \frac{1}{2qA}\left(\frac{I_{n2}}{D_n} - \frac{I_{p2}}{D_p}\right) \tag{3.43}$$

Using equation (3.1) in the P-N junction section, the inbuilt voltages of junctions can be calculated using two equations below:

$$V_{j1} = V_T \ln\left(\frac{p_{x1} N_B}{n_i^2}\right) \tag{3.44}$$

$$V_{j2} = V_T \ln\left(\frac{p_{x2}}{N_B}\right) \quad \text{assuming low doped N-drift region} \tag{3.45}$$

The total voltage across the PiN diode can be calculated by adding all the voltages together.

$$V_{AK} = V_{j1} + V_{j2} + V_B - V_{d1} - V_{d2} \tag{3.46}$$

The electric field at the edges of the depletion regions can be calculated using the displacement currents in equations (3.37) and (3.38). The electric field and the derivative of the electric field at the edges of the depletion region are then used to

determine whether or not punch-through has occurred. Punch-through happens when the two depletion regions meet each other somewhere in the drift region of the device. Using the electric field at the boundaries and the gradient of the electric field, the electric field at the centre boundary can be calculated as below.

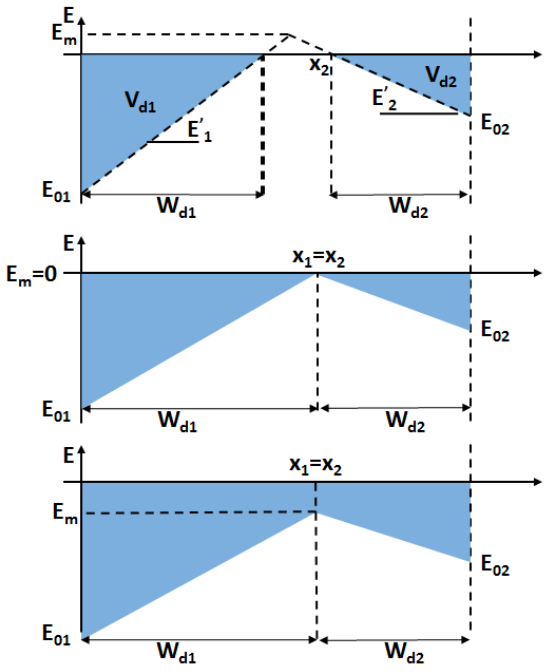


Fig. 3.9 Electric field at the boundaries of the depletion region under normal operation and punch-through

Fig. 3.9 shows the electric field at the boundaries of the depletion region under normal operation and when the punch-through happens. As can be seen, the electric field at the centre of the drift region where two edges of the depletion region meet can be calculated using the electric field gradient and the electric field values at the junctions. If the calculated electric field at the centre is positive, then punch-through has not happened. When the two depletion regions meet, this electric field is equal to

zero. When the electric field at the centre of the drift region is negative, this means that the punch-through has happened. Equation (3.47) below can be used to calculate the electric field at the centre of the drift region (E_m).

$$\begin{cases} E_1' = \dfrac{E_m - E_{01}}{x_m} \\ E_2' = \dfrac{E_m - E_{02}}{x_m - W_B} \end{cases} \rightarrow \frac{E_m - E_{01}}{E_1'} E_2' = E_m - E_{02} + W_B E_2'$$

$$E_m = \frac{E_{01}\left|E_2{}'\right| + E_{02}E_1{}' + W_B E_1{}'\left|E_2{}'\right|}{E_1{}' + \left|E_2{}'\right|} \tag{3.47}$$

The absolute values applied to the slopes of electric fields are purely due to mathematical explanation and the fact that the electric field on one side has a positive slope and on the other side has a negative slope.

3.3.3 MOSFET

The principle operation and the equations used to model a MOSFET are explained in this section. The base structure of a MOSFET is the Metal Oxide Semiconductor (MOS) capacitor. A MOS capacitor is made from a metal layer deposited on a layer of silicon dioxide (SiO_2) grown/deposited on top of the semiconductor. This structure is used at the gate of the device to control the flow of the current through the device. The MOS capacitor can be either made on top of N-type semiconductor (p-MOS) or on top of a P-type semiconductor which is referred to as n-MOS. In n-MOS, when a positive

voltage applied to the gate terminal, it attracts electrons to the interface between the oxide dielectric and the semiconductor substrate and forms a channel between the drain and source which is referred to as inversion layer. The dimensions of the inversion layer determine the amount of current that can pass through the inversion layer (also known as MOS channel).

The voltage that is applied to the top metal of a MOS capacitor, creates an electric field that penetrates through the semiconductor substrate. In case of P-type semiconductor, the electric field repels the majority holes from the surface of the semiconductor close to the oxide layer. Existence of the oxide layer, creates an insulation between the metal and the semiconductor, preventing the electrons from moving towards the metal. Repulsion of holes from the surface of the P-type semiconductor in presence of electric field, creates a depletion region under the oxide. During the formation of the depletion region (depletion operation), minority carriers move to the surface. The formation of depletion region for a P-type MOS capacitor substrates is shown in Fig. 3.10. By increasing the V_{GS} bias voltage, the depletion width increases. The depletion region is essentially a voltage dependent capacitor which can be charged or discharged depending on the voltage that is applied to it.

The potential at which the inversion layer forms is referred to as threshold voltage (V_{th}). Threshold voltage of is approximately calculated using equation below [31, 32]:

$$V_{th} = \frac{2}{C_{ox}}\sqrt{\varepsilon_{si} V_T N_A \ln\left(\frac{N_A}{n_i}\right)} + 2V_T \ln\left(\frac{N_A}{n_i}\right) \tag{3.48}$$

As can be seen, threshold voltage is voltage dependent and it also depends on the doping of the semiconductor substrate. In this equation, N_A is doping of the semiconductor and ε is permittivity of Si. C_{ox} in equation above is the oxide capacitance per unit area (F). Oxide capacitance can be calculated using equation below in which ε_{ox} is permittivity of oxide and for SiO_2 is equal to 3.9 times of free space permittivity:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.49}$$

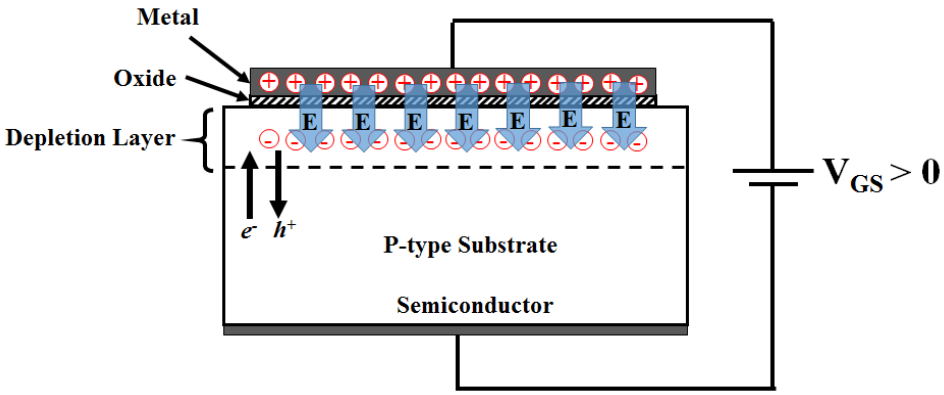


Fig. 3.10 P-type substrate MOS capacitor under forward bias and formation of depletion region.

The MOSFET shown in Fig. 3.11 is a three terminal device that is controlled by the application of a gate bias resulting in a current passing through the device. The majority of the power MOSFETs have a P-type semiconductor under the gate oxide. Hence, they work based on movement of electrons in the channel. Fig. 3.11 shows the structure of an N-channel vertical power MOSFET and the formation of the channel when the device is conducting. When positive gate bias with respect to the source (V_{GS}) is applied to the gate terminal, a channel starts to form which initially extends from

the N^+ source region to the N^- drift region. The channel is depleted from holes and a current path is provided via the electrons to transport current from source to drain and due to electrons, the direction of current flow is from drain to source. The current only flows, if a positive voltage is applied to the drain with respect to the source, and V_{GS} is larger than the threshold voltage (V_{th}).

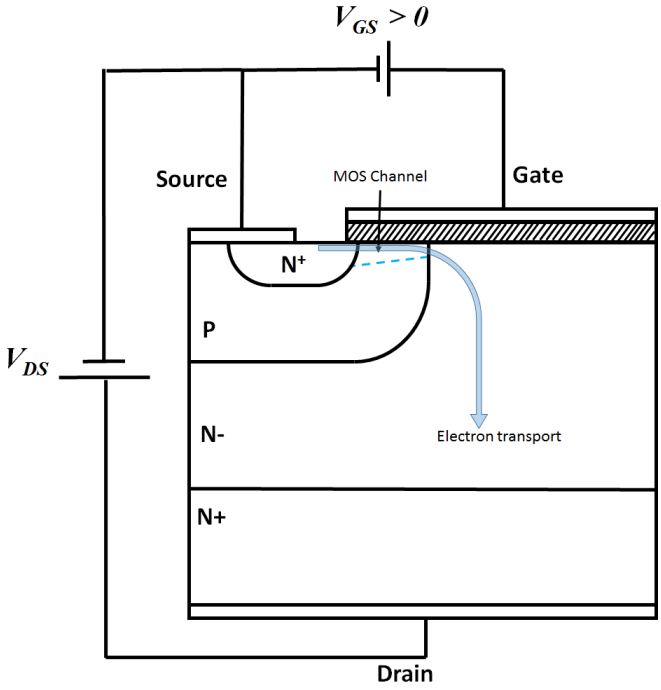


Fig. 3.11 Formation of channel when the MOSFET is biased and is conducting.

Fig. 3.12 illustrates the typical forward characteristic of a power MOSFET. The MOSFET on-state current can be controlled by the amount of V_{GS} voltage that is applied to the gate of the device. The output characteristics, the region in which the MOSFET shows similar characteristic as a resistor, is referred to as linear or Ohmic region. Occurs at below V_{DS} ($V_{GS} - V_{th} > V_{DS}$). This region is usually used in operation of low

voltage digital circuits. The amount of current that can pass through the channel in this operation area is calculated using equation below (gradual channel approximation):

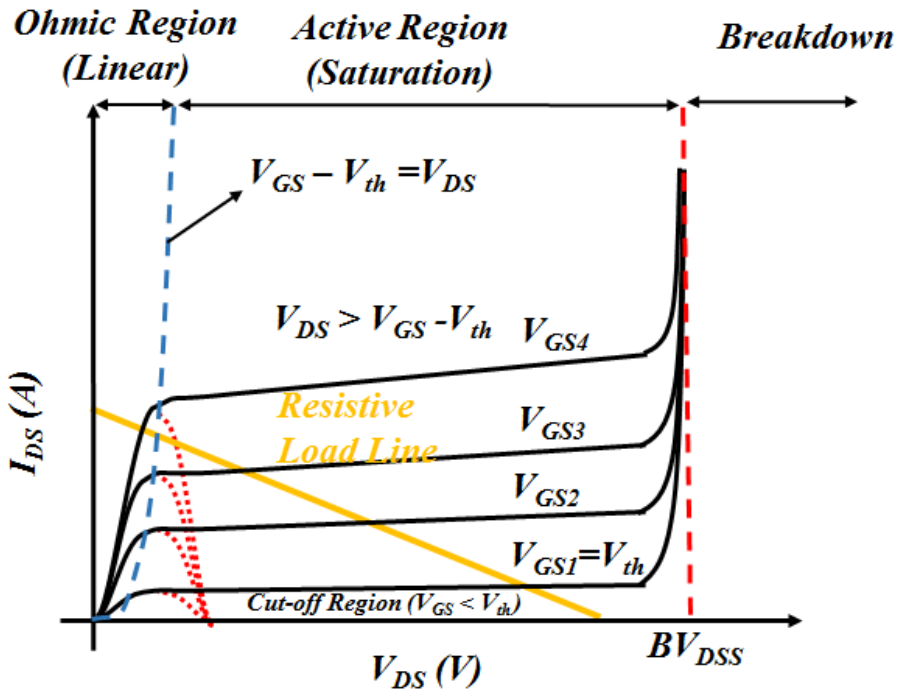


Fig. 3.12 Static forward characteristic of a MOSFET at different gate-source voltages.

$$I_{mos} = \frac{-Q_{channel} WL}{t_r} \tag{3.50}$$

This equation is basically the charge flow rate equation and it specifies the charge density existing in the inversion layer ($Q_{channel}$) divided by the amount of time it takes for the carriers to flow from the source to the N^- drift region. W is the gate width, L is

the gate length and t_r denotes the travel time for the electron and is calculated simply by dividing the length of the gate divided by the velocity of electron which is simply product of mobility in electric field.

$$t_r = \frac{L}{v} \tag{3.51}$$

$$v = \mu E = \mu \frac{V_{DS}}{L} \tag{3.52}$$

Hence, the current equation at the linear region can be calculated as below:

$$I_{mos} = -\mu Q_{channel} \frac{W}{L} V_{DS} \tag{3.53}$$

The inversion charge is proportional to the voltage applied to the gate of the device and the oxide capacitance per unit area explained in equation (3.49). Hence, the current in the linear region can be written as below:

$$Q_{channel} = -C_{ox}(V_{GS} - V_{th}) \quad for \quad V_{GS} > V_{th} \tag{3.54}$$

$$I_{mos} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})V_{DS} \quad for \quad V_{GS} - V_{th} > |V_{DS}| \tag{3.55}$$

For drain-source voltages below the threshold voltage, the current can be assumed to be equal to zero and this is shown as "*Cut-off Region*" in Fig. 3.12. However, in reality there exist a sub-threshold current which determines the amount of leakage current in

the device when a voltage below the threshold voltage is applied to it. The sub-threshold current may be calculated by the equation below:

$$I_{mos} \propto e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)} \tag{3.56}$$

$$n = 1 + \frac{\sqrt{\frac{q\varepsilon N_a}{\phi_F}}}{2C_{ox}} \tag{3.57}$$

In this equation ϕ_F is the bulk reference potential which quantifies the distance between the Fermi energy and the intrinsic energy of the semiconductor bulk.

If we assume that the charge in the inversion layer varies with the drain-source voltage, then the quadratic model for MOSFET is resulted with the following equation:

$$I_{mos} = \mu C_{ox} \frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \quad for \quad V_{GS} - V_{th} > V_{DS} \tag{3.58}$$

In the saturation region of the MOSFET, current is independent of the drain-source voltage it does increase as significant as it does in the linear region. The dotted line shown in blue colour in Fig. 3.12 is the on-set of the saturation region and follows this quadratic equation:

$$I_{mos} = \mu C_{ox} \frac{W}{L} V_{DS}^2 \tag{3.59}$$

The equation showing the current in the saturation region is as below:

$$I_{mos} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \quad for \quad V_{DS} > V_{GS} - V_{th} \tag{3.60}$$

The current in the saturation may increase with a small slope and this due to a phenomenon known as channel length modulation, in which the MOSFET has a small footprint and is fabricated on a low doped substrate. As the drain-source voltage increases, the depletion width at the drain increases. Consequently, the length of the channel becomes shorter and hence, the current passing through the channel increases. This is illustrated with a slight slope in the current in the saturation region in Fig. 3.12. This impact may be reduced by increasing the size of the device, increasing the length of the channel and increasing the doping of the substrate. The impact of channel length modulation is taken into account by multiplying $\left(1+\lambda V_{DS}\right)$ term to the current equations in MOSFET. Hence, the MOSFET current equations can be written as below:

$$I_{mos} = \begin{cases} e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)} & for \quad V_{GS} < V_{th} \\ \mu C_{ox}\dfrac{W}{L}\left(\left(V_{GS}-V_{th}\right)V_{DS} - \dfrac{V_{DS}^2}{2}\right).\left(1+\lambda\left|V_{DS}\right|\right) & for \quad V_{GS}-V_{th} > V_{DS} > 0 \\ \dfrac{\mu C_{ox}}{2}\dfrac{W}{L}\left(V_{GS}-V_{th}\right)^2\left(1+\lambda\left|V_{DS}\right|\right) & for \quad V_{DS} > V_{GS}-V_{th} \end{cases} \tag{3.61}$$

In this equation $\mu C_{ox}\dfrac{W}{L}$ is known as MOS transconductance and it is denoted by K_p. During the operation of MOSFET, as the inversion layer forms and the voltage across the drain-source terminals is large enough for the current to start flowing, current passing through the device rises and at some point, the voltage across the device

falls and the depletion regions start to shrink. When the device is switching off, the depletion regions start forming and the inversion layer shrinks until the channel is cut-off and the current flow stops. At this point the depletion region across the device expand and they withstand the blocking voltage across the drain-source terminal of the device. In this equation, the MOS transconductance, the thermal voltage, and the threshold voltages of the device are temperature dependent and their temperature dependencies are explained in detail in Chapter 5.

The calculation of the voltage dependent parasitic capacitance of the MOSFET is shown in Appendix D. During the switching of the device, charge and discharge of this capacitor determines the displacement current and shape of the voltage waveform which is further discussed in Chapter 5.

The displacement current of the depletion layer may be obtained using equation below:

$$I_{disp} = \varepsilon A \sqrt{\frac{qN_B}{2\varepsilon V_{DS}}} \frac{dV_{DS}}{dt} \tag{3.62}$$

The voltage drop at the bulk of the drift region in MOSFET can be calculated using equation below:

$$V_B = \frac{I_{DS}}{qAa_i \mu_n N_B} \tag{3.63}$$

During the operation of the MOSFET, the drain-source current is sum of the MOS channel current, the displacement current and the gate-drain capacitance current. Hence, we have:

$$I_{DS} = I_{mos} + I_{disp} + I_{GD} \tag{3.64}$$

The gate-drain current is calculated by the following equation:

$$I_{GD} = C_{GD}\frac{dV_{DS}}{dt} - \frac{I_g + C_{GD}\dfrac{dV_{DS}}{dt}}{C_{GS} + C_{GD}}C_{GD} \tag{3.65}$$

The gate-source voltage can be calculated using equation below:

$$V_{GS} = \int \frac{I_g + C_{GD}\dfrac{dV_{DS}}{dt}}{C_{GS} + C_{GD}}dt \tag{3.66}$$

3.3.3.1 Drain-Source Voltage Calculation

The drain source voltage can be calculated using the MOS channel current. If the two current equations in the Ohmic and pinch-off region are compared together, the following condition can be used to decide whether the device is operating in the saturation region or in the linear region:

$$Condition: \quad (V_{GS} - V_{th})^2 - 2\left(\frac{I_{mos}}{K_p}\right) \geq 0 \tag{3.67}$$

If this condition is true, then the device is in the Ohmic region, hence, the second equation in (3.61) is used to calculate the drain-source voltage. As can be seen in Fig. 3.12, the MOS current equation in the Ohmic region is a quadratic equation which is shown in red colour for different values of gate-source voltages. The load line determines the value of the current during the operation of the device. For a single value of I_{mos} at a certain gate-source voltage, there may be 2, 1 or zero answers for the V_{DS} based on the quadratic equation of the current. These answers happen if the constant current line:

(a) Crosses the current equation at two points: In this case scenario I_{mos} is less than the peak of the quadratic equation. In this case scenario, only the smallest answer is valid as the larger value does not exists on the forward characteristic of the device.

(b) Crosses the equation at the peak of the waveform: this is the blue line shown in Fig. 3.12 which is the boundary between the Ohmic and saturation operation region.

(c) Or is higher than the peak value of the equation: this case scenario is not a valid operation point for the device.

Hence the drain-source voltage is calculated using equation below:

$$V_{DS} = \min\left\{\frac{2(V_{GS}-V_{th}) \pm \sqrt{(V_{GS}-V_{th})^2 - 2\left(\frac{I_{mos}}{K_p}\right)}}{2}\right\} \tag{3.68}$$

If the condition shown in (3.67) is not true, then the device is operating in the saturation region and the drain-source voltage may be calculated as below:

$$V_{DS} = \left(V_{GS} - V_{th}\right) + \frac{\frac{I_{mos}}{K_p\left(V_{GS} - V_{th}\right)^2} - 1}{\lambda} \tag{3.69}$$

3.3.4 IGBT

As explained in the previous chapter, IGBT cell has a very similar structure to MOSFET. The only difference is the added P^+ emitter added to the backside of the device and the collector terminal is at the bottom side of this structure (Refer to Fig. 2.7 for the cross section view of PT and NPT IGBTs). The added P-type layer at the back side of the device allows holes to be injected to the N^- drift region of the device, making this device a bipolar transistor which works based on conductivity modulation. Similar to PiN diode, during the on-state of the device, carriers are injected to the drift region of the device and the amount of electrons passing through the MOS channel of the device, determines the amount of current that passes through it. Similar to MOSFET, the gate voltage creates an inversion layer and creates a path for the electron current to pass through the channel. The positive collector-emitter voltage across the terminals of the device results in an electric field. This electric field causes the electrons to flow to the drift region from the N^+ emitter through the n-channel towards the collector. At the same time, holes flow from the P^+ emitter to the low doped drift region towards the P-well. Consequently a triangular shape charge is stored in the drift region of the device

which has a higher density closer to the bottom of the device. The charge density at closer to the P^+ region close to the emitter is lower which is due to the fact that depletion region exists close to this region. The charge storage region in an IGBT is shown in Fig. 3.13.

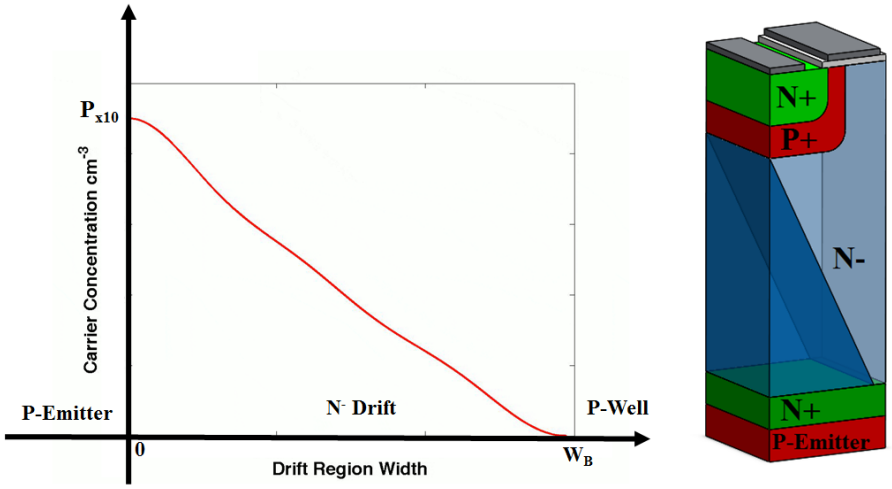


Fig. 3.13 Charge storage region in an IGBT with 3D view of the device cell structure.

The density of carrier concentration profile in shown in Fig. 3.13 can be obtained by knowing the carrier density at the edge of the P-emitter region shown in this graph.

$$\left.\frac{\partial p(x,t)}{\partial x}\right|_{t=0} = \frac{1}{2qA}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right) \cong \frac{-p_{x10}}{W_B} \qquad (3.70)$$

The transient operation of an IGBT is shown in Fig. 3.14. These waveforms are taken from clamped inductive switching tests carried out on a PiN diode/IGBT pairs. When the positive gate voltage is applied to the gate of the IGBT with respect to the emitter of the device, the inversion layer starts to form in the P-well underneath the

gate. When the gate-emitter voltage reaches the threshold voltage of the device, the MOS starts conducting and current starts rising. The gate capacitance at this point is mainly the gate-emitter capacitance as the Miller capacitance is small. The gate-emitter voltage that charges the gate-emitter capacitance charges exponentially with the time constant of $R_G C_{GE}$. As the MOS channel conducts, carriers are injected in the drift region through the inversion layer in the P-well underneath the gate of the device and they move towards the P^+ region close to the collector where they recombine.

The amount of current entering the P-emitter and recombine there is equal to:

$$I_n = qAh_p p_{x1}^2 \tag{3.71}$$

Hence, the holes are allowed to flow to the drift region. The initial fall of V_{CE} occurs due to reduction of the drift region resistance. The rate of change of collector-emitter voltage is determined by the rate of change of the depletion capacitance coupled with the back electromagnetic force produced due to the change of voltage across the parasitic stray inductance of the IGBT.

When the IGBT switches on, the complementing freewheeling PiN diode, is switching off. Hence, the PiN diode undergoes a negative current which consequently results in a peak overshoot current in the I_{CE} current waveform. Further decrease of the collector-emitter voltage after the peak of the IGBT forward current happens due to the complete switch-off of the complementing freewheeling diode. This causes the depletion

region in the drift region of the IGBT shrink towards the MOS located at the top of the device.

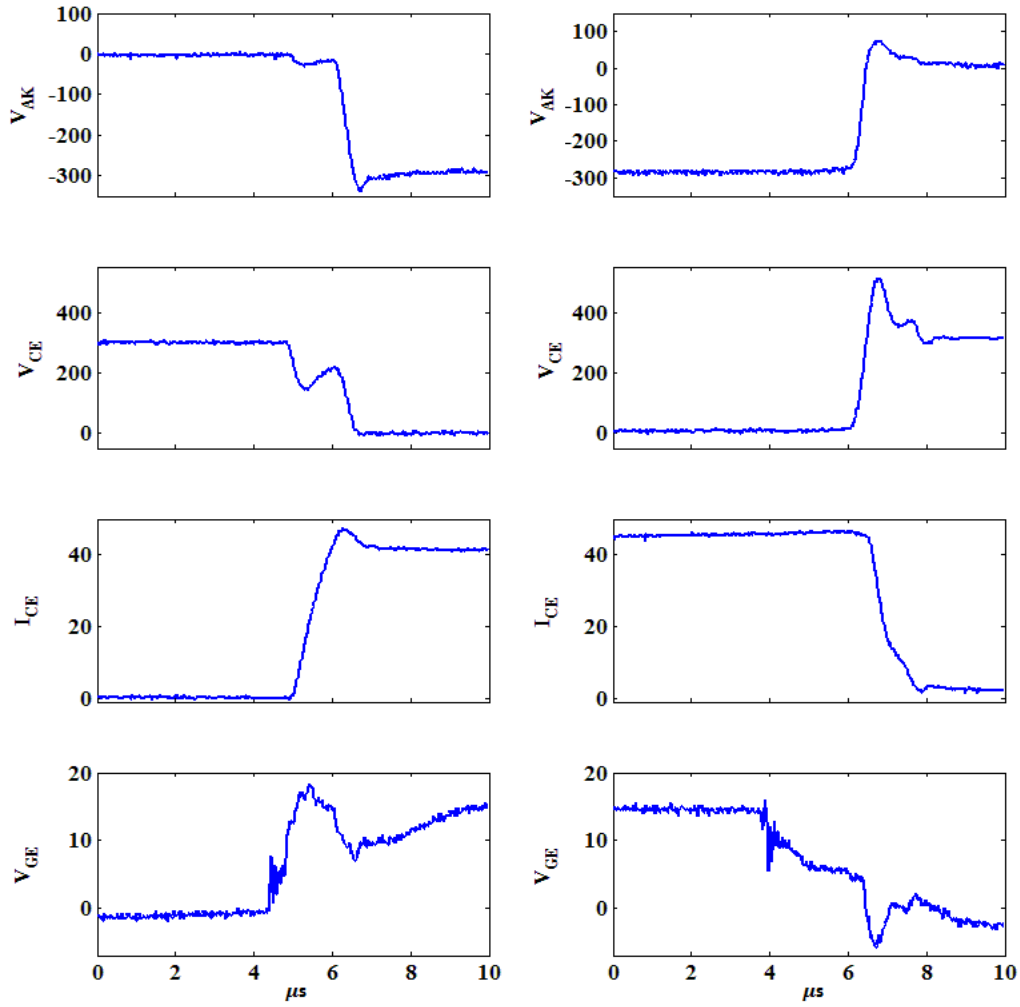


Fig. 3.14 Measured IGBT turn-on and turn-off switching waveforms.

As the charge gets stored in the drift region and the accumulation layer under the gate starts to form, the Miller capacitance increases. Sudden change of the miller capacitance can change the rate at which the depletion region shrinks and causes the gate voltage goes into the plateau region. The fast rate of change of the Miller

capacitance coupled with the parasitic gate inductance may rarely cause an overshoot in the gate-emitter voltage which is shown in Fig. 3.14. When the miller capacitance causes the plateau region in the gate-emitter of the IGBT, the collector-emitter voltage also experiences a plateau. Due to the high carrier lifetime, the diffusion length becomes greater than the drift region width of the device. Consequently, when the minority carriers are injected in the drift region, the charge storage region starts to form and the collector-emitter voltage of the IGBT starts falling down.

Similar to operation of PiN diode, when the device completely switches on and high level injection of carriers creates the charge storage region, due to conductivity modulation the on-state resistance of the IGBT reduces and hence, the on-state voltage drop reduces gradually. This is known as the IGBT tail voltage which occurs at the turn-on transient. At the time when the collector-emitter voltage drops significantly, the MOS channel voltage also decreases to the on-set of Ohmic region operation. Assuming that the load current is constant, any further decrease at the voltage across the MOS of the IGBT would results in the voltage rise across the gate-emitter of the device. At this time finally the gate-emitter voltage can reach the on-state voltage set by the gate driver circuitry.

In contrast, when the IGBT is switching off, the gate-emitter voltage starts falling down. This is due to the discharge of the gate-emitter capacitor through the gate resistance. This results in a negative current flow in the gate of the device that needs to flow to the Miller capacitance, during which the Miller capacitor starts charging creating the gate-emitter voltage plateau. At this point, the drain-source voltage of the

MOS structure within the IGBT cell exceeds the V_{GS}-V_{th}, and hence, the MOS goes to the saturation mode. At this plateau region, the gate-source voltage is held constant to support the constant MOS channel current. Consequently, the collector-emitter voltage increases. The Miller capacitance is a series connection of a voltage dependent depletion capacitance and a constant gate oxide capacitance. The depletion regions start forming and they create an electric field to withstand the blocking voltage across the device. The voltage dependent depletion width between the edge of the CSR and the gate can be calculated using the same equation as PiN diode, equation (3.32). This causes the collector-emitter voltage to rise. The rate of rise in the collector-emitter voltage is determined by the rate of extraction of the excessive carrier concentration in the drift region of the IGBT. When the gate-emitter voltage reaches the threshold voltage of the device, the MOS channel pinches-off and current falls down in the device and the current commutates in the complementing freewheeling diode. The collector-emitter voltage of the IGBT might experience a voltage overshoot due to existence of parasitic inductances and the diode turn-on voltage. Once, the depletion region is formed, the remaining current passing through the device needs to recombine and the CSR needs to be depleted completely. This brings about the IGBT tail current which has the main contribution in the power losses during the switch-off of the IGBT.

Similar to equation (3.28) of the PiN diode, during the operation of IGBT, the on-state voltage drop across the drift region can be calculated based on the amount of charge stored in the drift region of the device and the amount of current that is passing through the device. Due to conductivity modulation and high level injection of minority

carriers in the drift region, the base resistance in the IGBT is low during the conduction mode of the device. Relation below further demonstrates this:

$$V_B = \frac{J_{CE}}{q(\mu_n + \mu_p)} \int_{x=0}^{W_B} \frac{dx}{p(x)} \tag{3.72}$$

Now that the operation of an IGBT during the turn-on and turn-off is explained, equations related to the operation of the device, formation/shrinkage of the charge storage region and the depletion regions will be explained in the remaining of this section. These equations are used to model the behaviour of the IGBT.

During the on-state operation of IGBT when the CSR is formed, the collector-emitter current can be expressed as the sum of electrons and holes flowing to the drift region. The number of electrons entering the p-emitter to recombine is taken from equation (3.73).

$$I_{CE} = I_n + I_p = I_p + qAh_p p_{x10}^2 \tag{3.73}$$

The only difference between equation (3.73) and the similar current equation for PiN diode is that no displacement current exists due to the fact that during the conduction of the device, there is no depletion layer. Using this equation and equation

(3.70) results in the calculation of the carrier concentration at the edge of the P-emitter region.

$$p_{x10} = \frac{D}{2h_p W_B}\left(\sqrt{1+\frac{2h_p W_B^2 I_C}{qADD_P}}\right) \tag{3.74}$$

The carrier concentration in the drift region can be approximated by assuming large diffusion length and linear gradient approximation of the carrier concentration in the drift region of the IGBT.

$$p(x,t) = p_{x10}(t)\left(1-\frac{x(t)}{W_B}\right) \tag{3.75}$$

In which $x(t)$ is the position of the boundary of the depletion width in the drift region. As the drift region expands, $x(t)$ moves from W_B (drift region width) to 0.

The depletion width as mentioned earlier can be calculated by subtracting the drift region width from the voltage dependent depletion width in equation (3.32).

$$W = W_B - \sqrt{\frac{2\varepsilon V_d}{qN_{eff}}} \tag{3.76}$$

In this equation, N_{eff} is the effective carrier density of the drift region and may be calculated using the following equation:

$$N_{eff} = N_B + \frac{|J_p| - |J_n|}{qv_{sat}} \tag{3.77}$$

Similar to PiN diode, the boundary condition for the CSR requires the gradient of the carrier concentration at the edge of the CSR. This can be calculated using the electron and hole currents calculated in equation (3.73) (which is similar to equation (3.43) for the PiN diode). The boundary position of the charge storage region at the edge of the P-emitter region is equal to zero as there is no depletion region during the on-state of the IGBT. Consequently, similar to equation (3.44) the junction voltage between the P-emitter and the drift region can be calculated. This is based on the assumption that the IGBT is a punch-through IGBT and the heavily doped N type buffer layer does not exist. In case of NPT IGBT with a buffer layer sandwiched between the drift region and the P^+ emitter at the backside of the IGBT, the electron and hole currents are calculated using equations below:

$$I_p = \frac{2Q_H D_{pH}}{W_H^2} - \frac{2qAD_{pH} p_{x1}^2}{W_H N_H} \tag{3.78}$$

In this equation, Q_H is the amount of charge stored in the buffer layer of the device. This W_H denotes the width of the buffer layer and D_{pH} is the diffusivity of the holes in the buffer layer and N_H is the doping of the buffer layer. The amount of charge stored in the buffer layer can be calculated based on the continuity equation (D.23).

$$\frac{\partial Q_H}{\partial t} = I_{CE} - Q_H\left[\frac{1}{\tau_{pH}} + \frac{2h_p N_H}{W_H} + \frac{2D_{pH}}{W_H^2}\right] + qA\left[h_p + \frac{2D_{pH}}{W_H N_H}\right]p_{x1}^2 \qquad (3.79)$$

The P^+N_H junction voltage can be calculated by knowing the amount of carrier concentration at the P emitter junction (p_{b1}):

$$V_{j(P^+N_H)} = V_T \ln\left(\frac{p_{b1}N_H}{n_i^2}\right) \qquad (3.80)$$

And the voltage at the N_HN_B junction can be calculated by knowing the carrier concentration at the edge of the drift region (p_{x1}) adjacent to the buffer layer.

$$V_{j(N_H N_B)} = V_T \ln\left(\frac{N_B}{p_{x1}}\right) \qquad (3.81)$$

The MOSFET behaviour of the MOS structure in the IGBT uses the same MOSFET current equations explained in section 3.3.3, equation (3.61).

By writing the equation for the electron and hole current at the junction between the drift region and the P-well layer, the IGBT model can be completed. The equations are as below:

$$I_n = I_{mos} \qquad (3.82)$$

$$I_p = I_{CE} - I_{mos} - I_{CG} - I_{disp} \qquad (3.83)$$

The gate-collector current passing through the Miller capacitor is voltage dependent and can be calculated using the same equation as MOSFET shown in equation (3.71). The gate structure is stripe similar to MOSFET and together with the Miller capacitance, they follow the same equations as explained in section 3.3.3 for the MOSFET. The displacement current is due to the movement of carriers in to the P-well region and can be derived using equation below:

$$I_{disp} = \frac{\varepsilon A(1-a_i)}{W_{d2}} \frac{dV_{d2}}{dt} \tag{3.84}$$

The depletion width and the voltage at the depletion region are similar to equations (3.32) and (3.40) for the PiN diode. The ambipolar diffusion equation for the drift region is derived in the similar way as for the PiN diode explained in equation (3.14). By assuming the boundary conditions for the CSR, similar to equation (3.25) for PiN diode, the Ambipolar Diffusion Equation (ADE) can be reconstructed using Fourier series. In [34] the ambipolar diffusion equation is reconstructed using Fourier series in two dimensions which results in higher accuracy. The voltage drop across the IGBT can be calculated by summing the voltage drop on each junction and the voltage drop across the drift region.

$$V_{CE} = \begin{cases} V_{d2} + V_B + V_{j(P^+N_B)} & for\ NPT \\ V_{d2} + V_B + V_{j(P^+N_H)} + V_{j(N_H N_B)} & for\ PT \end{cases} \tag{3.85}$$

Chapter

4 Bipolar Latch-up in Power MOSFETs

In power electronics, vertical MOSFETs are designed to work beyond 1 kV. Therefore, many reliability concerns that might not be as important in microelectronics, become significantly important in power electronics. An example of this is the bipolar latch-up of the parasitic BJT of the power MOSFETs. Since SiC MOSFETs are aiming to replace Si IGBTs which do not have a body diode, this reliability concern needs to be revisited. In this chapter, a compact dynamic and fully-coupled electro-thermal model for parasitic BJT latch-up is presented and validated by measurements. The model can be used to enhance the reliability of the latest generation of commercially available power devices. BJT latch-up can be triggered by body-diode reverse-recovery during hard commutation with high *dV/dt* or from avalanche conduction during unclamped-inductive-switching. In the case of body-diode reverse-recovery, the base current that initiates BJT latch-up is calculated from the solution of the ambipolar diffusion equation describing the minority carrier distribution in the anti-parallel PiN body-diode. For hard commutation with high *dV/dt*, the displacement current of the drain-

body charging capacitance is critical for BJT latch-up whereas for avalanche conduction, the base current is calculated from impact ionization. The parasitic BJT is implemented in Simulink using the Ebers-Moll model and the temperature is calculated using a thermal network matched to the transient thermal impedance characteristic of the devices. This model has been applied to CoolMOS and SiC MOSFETs. Measurements show that the model correctly predicts BJT latch-up during reverse-recovery as a function of forward-current density and temperature. The model presented, when calibrated correctly by device manufacturers and applications engineers, is capable of bench-marking the robustness of power-MOSFETs. The work carried out in this chapter are presented in [36-38].

4.1 Introduction

Body diodes are often used as anti-parallel diodes in power MOSFET circuits. The drift layer between the p-body and the drain, is effectively a PiN diode known as the body diode. Body diodes can be used in applications such as DC-DC buck converters, bridge topology switching circuits, high performance PV converter cell and can also be employed in synchronous rectified brushless DC motor drive inverter circuits [39-44]. In such applications, diode snappiness and high reverse recovery charge of the body diode can impose a significant amount of electrical stress and power loss in the MOSFETs [45]. Reverse recovery charge is stored in the drift region as explained in the previous chapter. However, conventional lifetime control techniques (gold or platinum doping as well as irradiation) are not applicable in reducing the carrier lifetime as is

the case with discrete diodes, hence the body diode of the MOSFET can suffer from significant reverse charge. One of the main concerns regarding the usage of the body diode of power MOSFETs is the robustness of the device under hard commutation; e.g. in synchronous rectification, or in other circuits such as motor drives or primary side switching of switch mode power supplies [46, 47].

The high demand for high frequency and efficient power converters has triggered research into SiC devices including power MOSFETs [48]. SiC MOSFETs are more suitable for high voltage and high speed applications due to their higher breakdown voltage, lower on state resistance and faster switching. SiC has a significantly smaller minority carrier lifetime and as a result of the higher critical field, the thickness of the voltage blocking drift layer is approximately 10 times less than silicon devices. Consequently, they show smaller reverse recovery with a higher breakdown voltage. The effect of using SiC MOSFET in synchronous rectification has been studied in [40] which shows that the reverse recovery of SiC body diode is negligible as well as an improvement in the switching speed of the MOSFET. As shown in Fig. 4.1, MOSFETs have parasitic NPN BJTs that can latch-up under the right conditions; for instance, when the emitter-base voltage is forward biased, the base-collector voltage is reverse biased and there is sufficient body current in the base [49, 50]. For the BJTs to latch, there must be a body current sufficient to cause a voltage drop greater than the emitter base junction voltage of the parasitic BJT. To prevent this from happening, the source is usually grounded to the body by a high dose body implant and a common metal contact. However, at high temperatures a non-zero body resistance and a non-zero body

current can cause BJT latch-up. The high *dV/dt* of the body diode during reverse recovery coupled with the parasitic drain-to-body capacitance within the MOSFET can cause a body current (*CdV/dt*) sufficient to latch the parasitic BJT. This is particularly pertinent to SiC MOSFETs where *dV/dt* is high, minority carrier lifetime is low and the body diode is snappy.

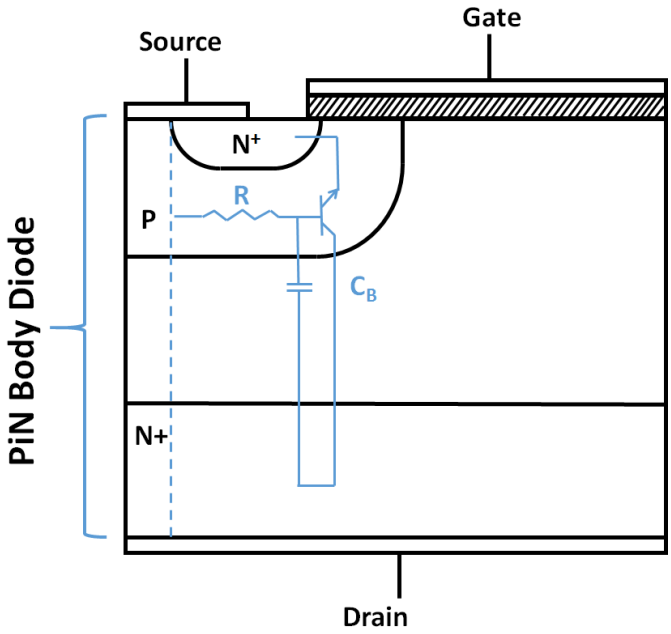


Fig. 4.1 Block diagram of a vertical MOSFET with parasitic components.

CoolMOS devices use the principle of the super-junction to achieve high blocking voltages while delivering low conduction losses. The alternate n and p columns in the drift region means that the body diode is not a conventional PiN diode and will therefore exhibit a different reverse recovery characteristic. In this chapter, the reliability of the SiC MOSFET and CoolMOS body diode under reverse recovery is investigated experimentally and by modelling. The body diode of the MOSFET has been modelled

using the Fourier series solution to the ADE explained in the previous chapter. In case of the CoolMOS model, it has been assumed that there is negligible carrier concentration gradient or electric field gradient across the lateral cross-section of the device in comparison to the vertical cross-section of the device. As a result, electrons flow from the cathode (the drain of the MOSFET) into the drift regions and holes flow from the anode (the p-body of the MOSFET) into the drift regions. Based on this, the 1-D solution of the Fourier series is applicable because of the assumption that the vertical concentration gradients are much higher than the lateral concentration gradients. This is coupled with electro-thermal model of the parasitic BJT and is used as a compact physics-based electro-thermal model for a SiC MOSFET and Si-based CoolMOS device. The impact of the temperature as well as current density on the diode recovery characteristics and failure mechanism of the MOSFET is investigated by the model and compared with experimental measurements. The proposed model can be used to investigate the conditions of device failure during purposeful or inadvertent reverse recovery of device body diode. The model is useful for estimating the reliability performance and giving deeper physical insight to the nature of bipolar latch-up. Section 4.2 describes the validation of the developed model and extending it to the SiC body diode. Section 4.3 describes the BJT electro-thermal model, and section 4.4 discusses the results while section 4.5 concludes the chapter.

4.2 Body Diode Model Validation

The model has been developed for a discrete PiN diode initially and in this chapter, has been extended to body-diodes for SiC MOSFETs and CoolMOS devices. The finite element models of super-junction devices in SILVACO was simulated and the lateral and vertical carrier concentrations and electric fields are extracted (Fig. 4.2). Depletion in CoolMOS is 2-dimensional instead of 1 dimensional. However, because the concentration gradients and electric fields in the direction under consideration (which is the vertical direction shown in Fig. 4.4 and Fig. 4.5 for PN^-N^+ and PP^-P^+ diodes respectively) are much higher than those in the lateral direction (shown in Fig. 4.3), carrier drift and diffusion, hence, the Fourier series reconstructed ADE is applied in the vertical direction only. Carrier dynamics in the lateral direction is assumed to be inconsequential because the electric fields and concentration gradients in the lateral PN junction are smaller.

The high level lifetime in the drift region (τ_{HL}) in the ADE (equation 3.46) is in order of $1\mu s$ for silicon devices and 0.1 ns for SiC and D_n (electron diffusion coefficient) for Silicon is 36.1798 cm^2/s and 34.3708 cm^2/s for SiC at room temperature and D_p (hole diffusion coefficient) is 11.6292 cm^2/s for Silicon and 2.3258 cm^2/s for SiC at room temperature. Diffusion coefficients in SiC is smaller in comparison with silicon.

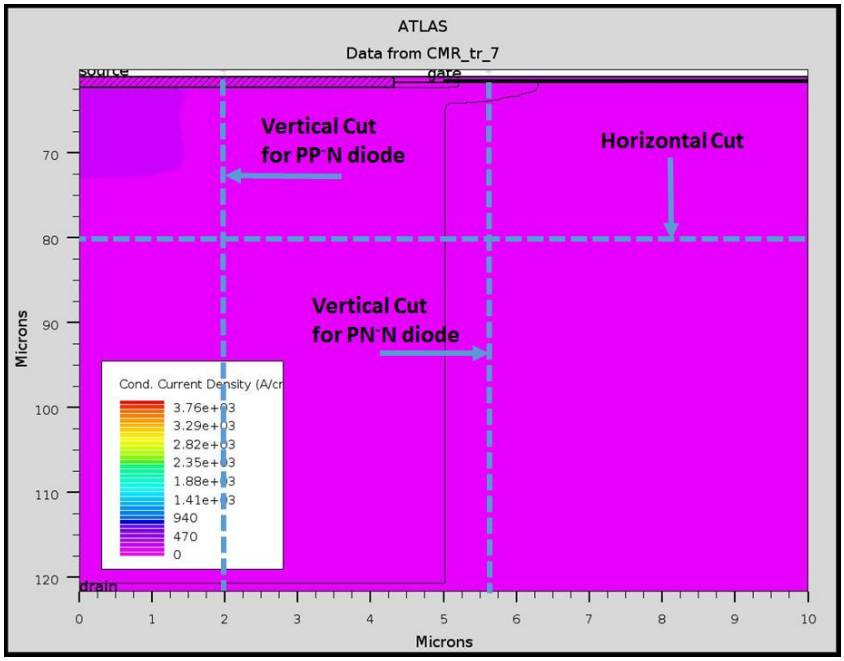


Fig. 4.2 A super-junction device structure built in Silvaco also with the cross section cuts which were used to show the carrier concentration gradient in the vertical and horizontal axis.

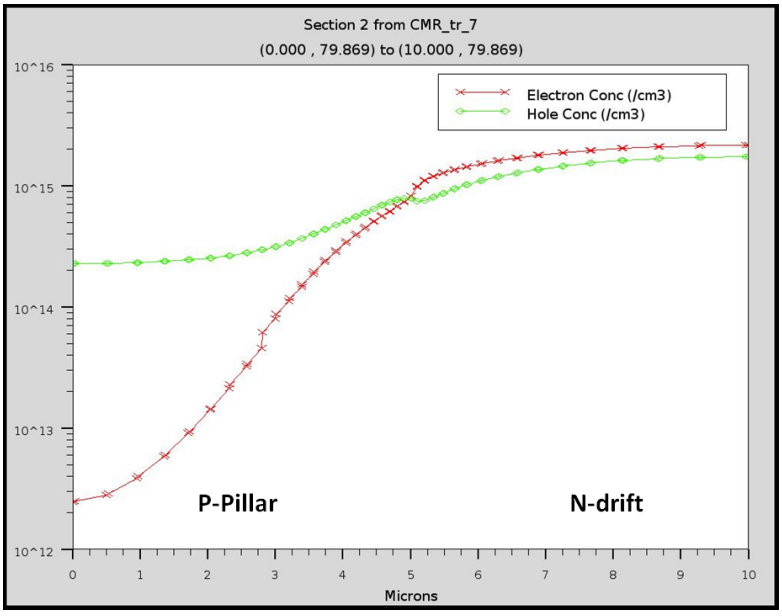


Fig. 4.3 Electrons and holes concentration in the horizontal axis of the device showing small lateral gradient for carrier concentration.

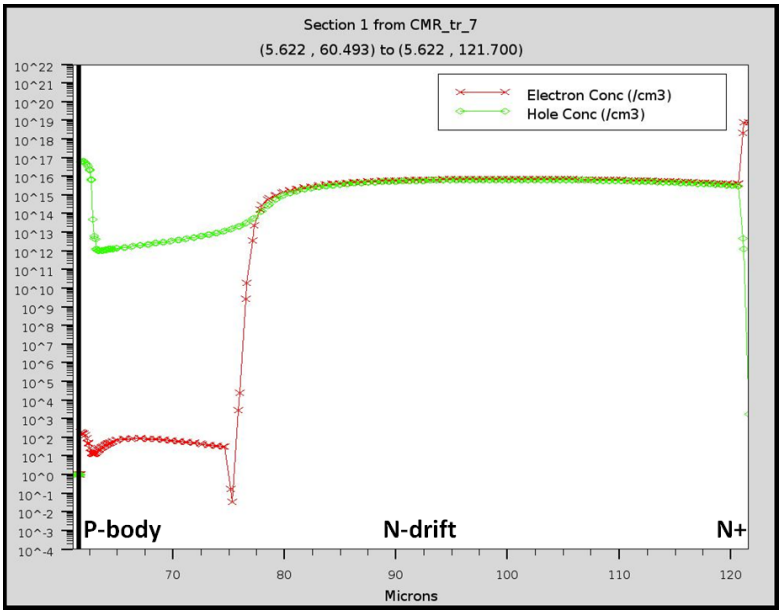


Fig. 4.4 Electrons and holes concentration in the PN-N diode showing high vertical gradient in the carrier concentration in comparison with the lateral cross section view.

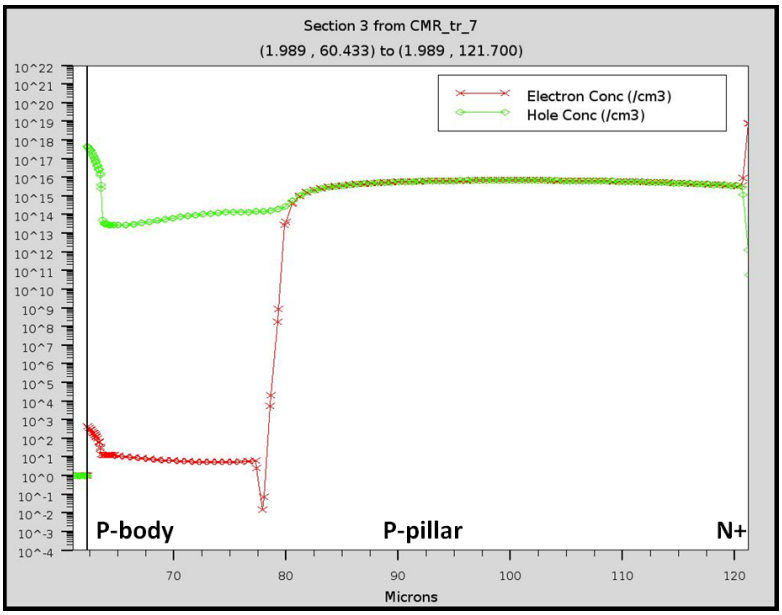


Fig. 4.5 Electrons and holes concentration in the PP-N diode showing high vertical gradient in the carrier concentration in comparison with the lateral cross section view.

To validate the model using experimental measurements, a clamped inductive switching test rig is used as shown in Fig. 4.6. As can be seen in Fig. 4.6, the low side transistor is used to commutate the current away from the high side free-wheeling diode, which in this case is the body diode of the MOSFET. The body diode of the MOSFETs under test is stressed by physically connecting the gate of the MOSFET to the source, thereby ensuring that the MOSFET never turns on and current flows through the body diode in the reverse direction. By using the double pulse method, the low side transistor is switched on charging the inductor to a pre-defined current after which it is switched off thereby commutating the current to the body diode. When the low side transistor is switched on again, the high side body diode goes into reverse recovery which can trigger device destruction depending on the commutation rate, temperature, forward current density etc. To validate the model, the results from the Fourier Series ADE (FS-ADE) solution are compared with experimental measurements on a discrete PiN diode as well as a finite element device modelled using a simulator (Silvaco). A 1.2kV/45A IXYS PiN diode (DSI45-12a) coupled with a low side transistor of suitable rating was tested. The choice of this low switching speed diode was purely based on the modelling aspect of the work and to verify the simulation and the device behaviour. All the terminal voltages and currents were captured on a Tektronix oscilloscope. The semiconductor devices were placed in a thermal chamber where the ambient temperature was varied in order to analyse the temperature dependencies of the switching transients [51-54]. Fig. 4.7 shows the experimental setup including the

test rig, chopper cell, the environmental chamber and the oscilloscope used to carry out the measurements on the power devices.

Fig. 4.8 (a) shows a comparison of the diode turn-off current for the experimental measurement, the FS-ADE (Fourier Series reconstruction of Ambipolar Diffusion Equation) model and a finite element simulation from Silvaco while Fig. 4.8 (b) shows a comparison of the voltage across the device during turn-off. Datasheet parameters were used together with known physical constants to obtain matching and the *dI/dt* of the current was varied by the gate resistance used to switch the low side transistor. As can be seen from Fig. 4.8 (a) and Fig. 4.8 (b), the FS-ADE model is capable of replicating the current and voltage waveforms of both the experimental measurements as well as finite element models.

Fig. 4.9 (a) shows the different reverse recovery waveforms of the discrete silicon PiN diode corresponding to different commutation rates modulated by the gate resistance of the switching transistor.

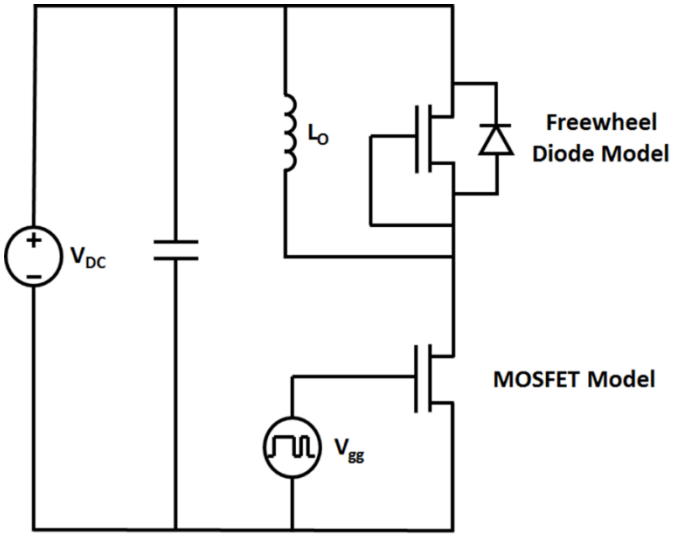


Fig. 4.6 Chopper cell circuit used to model the switching dynamics of body diode of a MOSFET and CoolMOS.

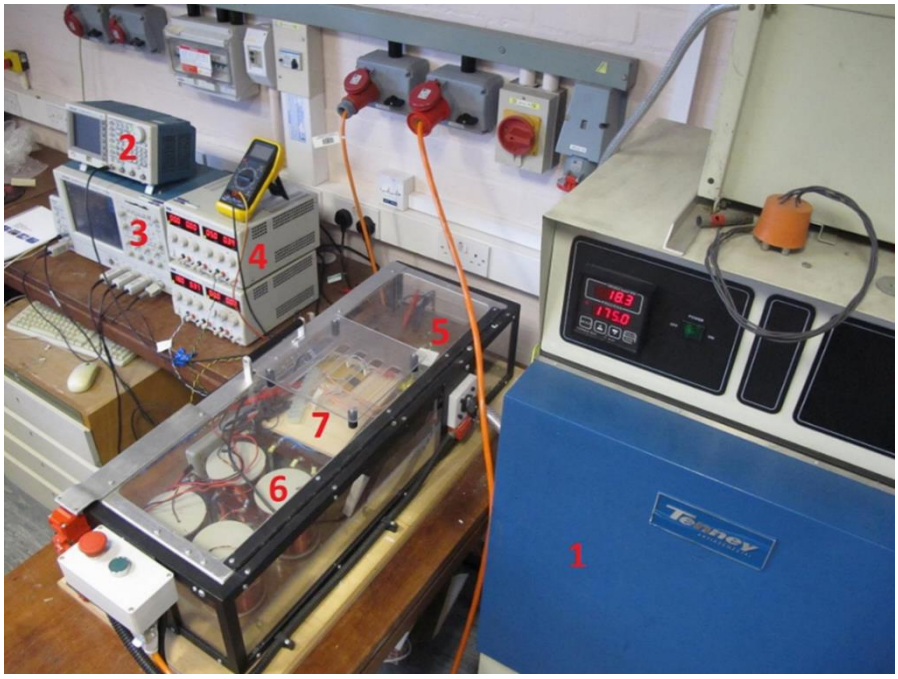


Fig. 4.7 Experimental setup. 1. The environmental chamber where the device temperature can be changed between -75°C to 175°C, 2. Function generator to produce double pulse, 3. Oscilloscope, 4. DC power supply for the gate driver and gate input signal, 5. DC link capacitor, 6. Inductive load, 7. Gate drive circuit.

The reverse recovery characteristic of the body diode of a SiC MOSFET from Cree (C2M0160120D) is also modelled using the FS-ADE solution and validated by experimental measurements. Fig. 4.9 (b) shows the results of the FS-ADE model together with the measurements of the reverse recovery characteristics of the SiC body diode. As can be seen in Fig. 4.9 (a) and Fig. 4.9 (b), there is good matching between the FS- ADE model and the experimental measurements. The material parameters were changed to match with the known material parameters of SiC and the size of the device was changed accordingly using the existing data available on the device datasheet.

Fig. 4.10 (a) shows the measured reverse recovery characteristics of the CoolMOS body diode at different temperatures whereas Fig. 4.10 (b) shows that of the SiC MOSFET body diode at different temperatures. As can be seen from the experimental measurements in Fig. 4.10 (b), there is very little reverse recovery charge in the SiC body diode compared with the CoolMOS body-diode shown in Fig. 4.10 (a) and the reverse characteristics of the SiC MOSFET body diode are temperature invariant. This is due to the very low minority carrier lifetime in SiC which means that the stored charge in the drift region very quickly recombines during the turn-off of the body diode.

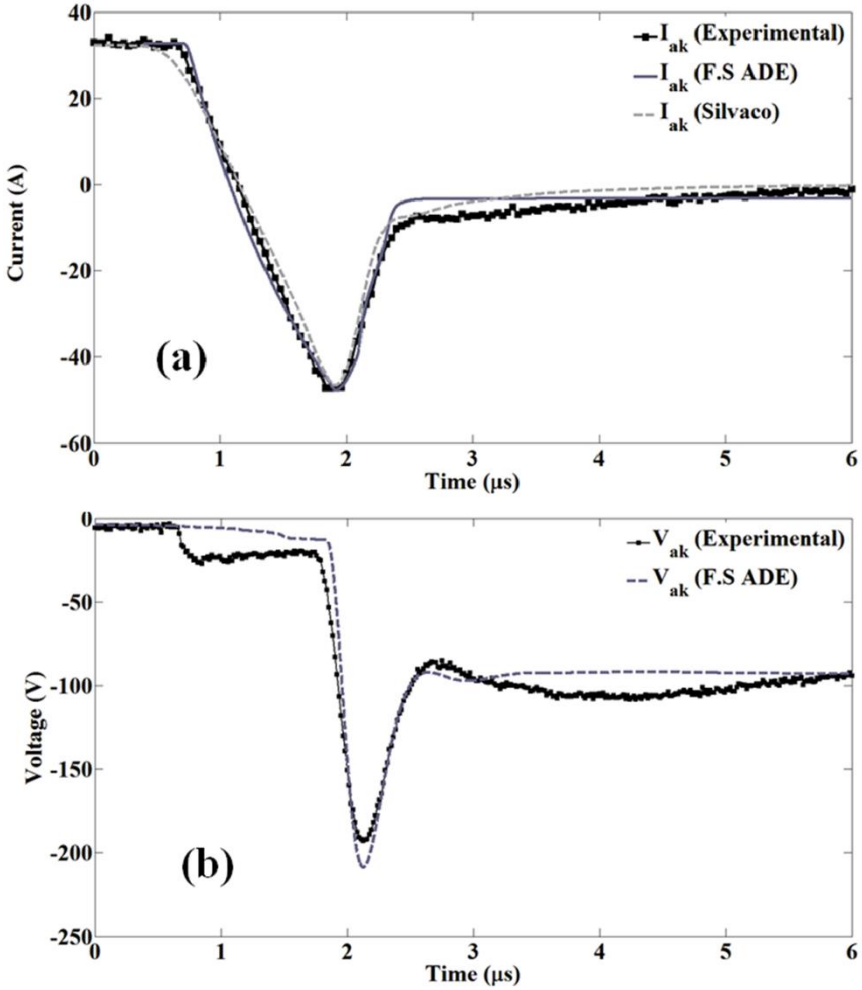


Fig. 4.8 Simulation validation: Diode reverse recovery current waveform (a) and voltage waveform (b) from the experimental results, Silvaco Finite Element device simulation and Fourier Series ADE reconstruction simulation at the room temperature using 22 Ω gate resistance.

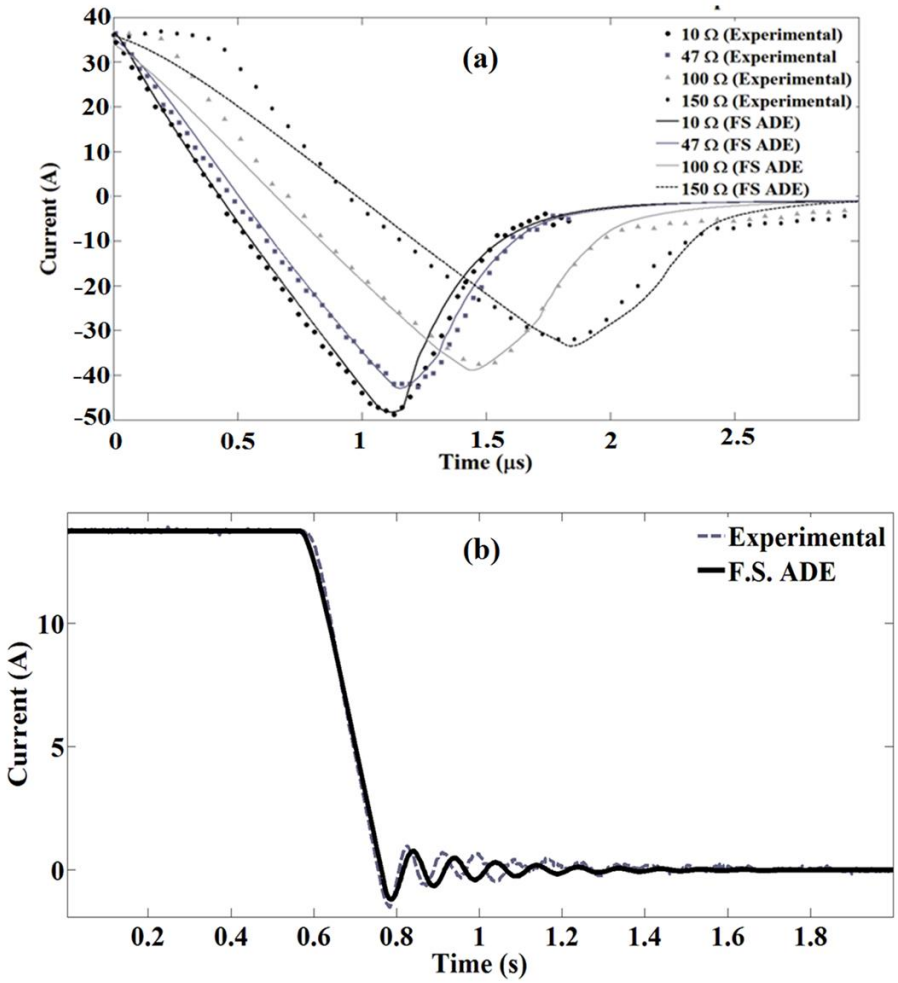


Fig. 4.9 (a) PiN diode reverse recovery waveform for different IGBT gate resistances (different *dI/dt*) - Comparison between the experimental results and the simulation results using the Fourier Series ADE reconstruction. Fig. 4.9 (b). Measured and modelled reverse recovery characteristics of the SiC MOSFET body-diode.

Furthermore, the epitaxial voltage blocking drift layers in SiC are significantly thinner compared to that of silicon or CoolMOS, hence, there is less charge to be extracted during turn-off. The model developed for the silicon CoolMOS body diodes also takes the temperature dependency of the reverse recovery characteristics into account. As can be seen in Fig. 4.10 (a), the CoolMOS device exhibits significant reverse

recovery charge that increases with temperature due to increased carrier lifetime. For CoolMOS devices, modifications have been made to the Fourier solution of the ADE to account for the fact that it is not the conventional body diode, but rather alternate PN-N and PP-N diodes due to the super-junction architecture.

Fig. 4.11 (a) shows the structure of the conventional power MOSFET while Fig. 4.11 (b) shows the structure of a CoolMOS device with the PP-N and PN-N diodes along with the parasitic BJT, body resistance and depletion capacitance. According to this structure, the device consists of a PN-N and PP-N diodes in parallel, due to the super-junction architecture, i.e. the minority carriers in the PN-N diodes are holes while the minority carriers in the PP-N diodes are electrons. Consequently, the minority carrier lifetime and mobility of these carriers are different in the drift regions of the two different diodes. The electrons in the PP-N diodes have a higher lifetime and larger diffusivity in comparison to holes in the PN-N diodes. The model takes account of the larger charge stored in the body diode of a CoolMOS by utilising these two parallel diodes. Basically, in order to model the PP-N diode structure in the body diode of a CoolMOS, the N type drift layer of a conventional PiN diode is replaced with a P-type material with a different background doping and the minority carriers are changed to electrons. This means that the diffusion coefficient (related to the mobility of carriers according to Einstein relationship for diffusion) and the carrier lifetime are changed (i.e. μ_n=1330 cm^2/Vs and μ_p=450 cm^2/Vs, τ_n (P-type)=10μs and τ_p (N-type)=1μs) [33, 35, 55-57].

Equation (3.57) for the ADE reconstruction of the ambipolar diffusion equation explained in section 3.3.2, is solved for PN$^-$N and PP$^-$N diodes keeping in mind that holes are the minority carriers in the former and electrons are the minority carriers in the latter. These modifications can account for a significantly higher reverse recovery charge in CoolMOS which is necessary for modelling the body diode failure during the reverse recovery.

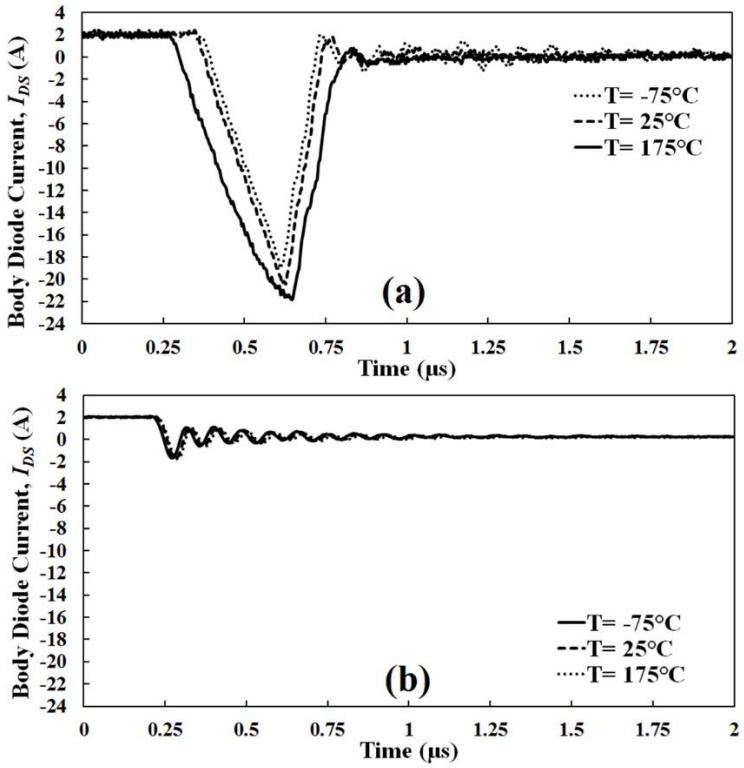


Fig. 4.10 (a) Measured reverse recovery current as a function of time for the CoolMOS body diode at different temperatures. Fig. 5(b) Measured reverse recovery current as a function of time for the SiC MOSFET body diode at different temperatures.

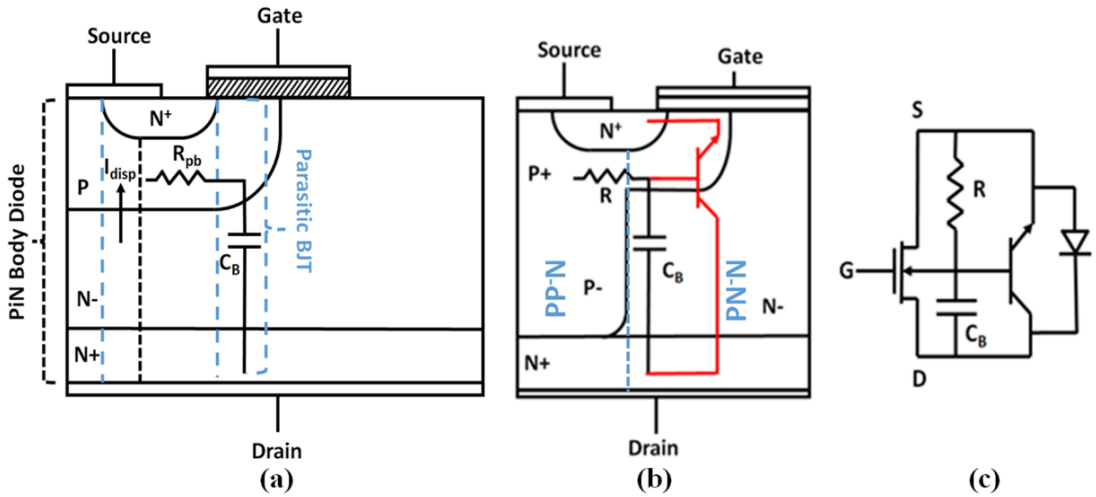


Fig. 4.11 (a) a vertical MOSFET structure, (b) CoolMOS structure including the parasitic BJT and a body diode. (c) Equivalent circuit of a MOSFET with the parasitic BJT and a body diode.

Fig. 4.12 (a) shows the simulated minority carrier concentration profiles of the CoolMOS device PP$^-$N and PN$^-$N body diodes in the drift region whereas Fig. 4.12 (b) shows the minority carrier concentration profile of the SiC PN$^-$N body diode. The minority carrier profile in the plasma region of the devices is extracted right at the point before the devices are switched off from high level injection mode during body diode conduction. As can be seen, the carrier concentration profile for PP$^-$N diode is higher than PN$^-$N diode and hence the reverse recovery waveform of CoolMOS is higher than a normal silicon or SiC based PiN diode. This is confirmed by the experimental measurements on reverse recovery in the body diodes shown in Fig. 4.10 (a) and Fig. 4.10 (b). The higher minority carrier concentration in the PP$^-$N relative to the PN$^-$N diode is due to increased electron lifetime and higher electron diffusivity. Fig. 4.12 (b) shows that the minority carrier concentration in the SiC PiN body diode is an order of magnitude lower than that in the CoolMOS.

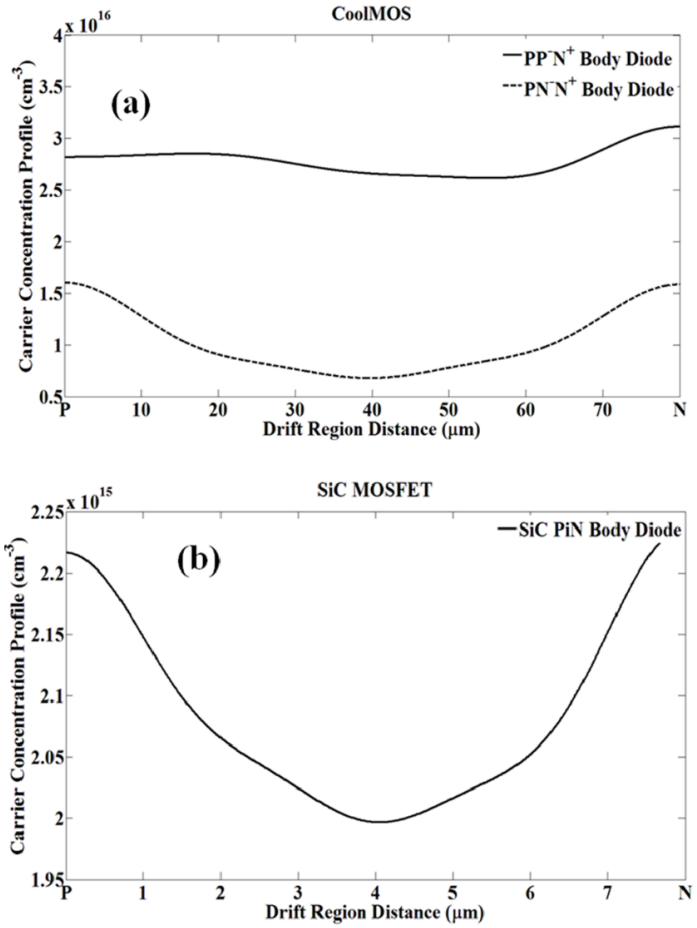


Fig. 4.12 Carrier concentration profile in the drift region of a PP-N and PN-N body diodes of a CoolMOS (a) and the carrier concentration profile of a SiC MOSFET body diode during the high level injection of these devices before switching off (b).

4.3 BJT Electro-Thermal Model

Fig. 4.11 (a) shows a typical vertical MOSFET illustrating the anti-parallel body diode and body resistance. Referring to Fig. 4.11 (a), the p-well resistance is shown as

R_{pb} and the drain-base capacitance is shown as C_B. The base current that triggers the BJT can come from the displacement current of the drain-to-body depletion capacitance during the body diode turn-off with high *dV/dt.* It can also be triggered by high *dV/dt* across the body diode during reverse recovery. As the reverse current reaches its peak, the depletion widths start to form across the junctions of the PiN diode and the remaining minority carriers in the drift region have to be recombined since carrier extraction is no longer possible. If the positive sloping recovery current (the recombination current between the peak reverse current and zero) is excessively high in the presence of parasitic inductance, large voltage overshoots coinciding with high peak reverse currents can cause very high instantaneous power dissipation across the device. This high instantaneous power causes high temperature excursions that can trigger the parasitic BJT and destroy the device.

Fig. 4.13 (a) shows the measured characteristics of a CoolMOS body diode in reverse recovery showing high reverse recovery current and simultaneously high peak voltage overshoot. Excessively snappy body diodes are known to be a reliability hazard under hard commutation [58]; hence, soft recovery diodes have been developed to mitigate this effect. The electro-thermal modelling of the BJT therefore requires an accurate physics based modelling of the diode's reverse recovery characteristics. To accurately model the electro-thermal BJT, the displacement current of the drain-to-body capacitance as a function of *dV/dt* during turn-off must first be calculated.

4.3.1 Drain-to-Body Capacitance Displacement Current

Fig. 4.14 (a) to Fig. 4.14 (d) shows the results of the FS-ADE simulations for 2 different switching rates (*dI/dt*). As the body diode is switched off, the low carrier lifetime in SiC results in a rapid extraction of the excess charge. The result of this is a fast rising voltage with a high *dV/dt* across the diode that is proportional to the switching rate. This can be seen in Fig. 4.14 (b) where the overshoot is due to stray inductance (approximately between 100-200 *nH*).

The peak overshoot increases with increasing *dI/dt*. As the diode begins to block, the electric fields at the junctions (PN^- and N^-N^+) cause the depletion width to start extending into the drift region. The result is that the drain-body capacitance decreases and there is a resulting displacement current associated with the charging of the capacitance. Fig. 4.14 (c) shows the simulated drain-base capacitance whereas Fig. 4.14 (d) shows the calculated displacement current.

The depletion width (W_{d1}) and the drain-base capacitance (C_B) can be calculated using equations (4.1) and (4.2) below:

$$W_{d1} = -\frac{\varepsilon E_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right) \tag{4.1}$$

$$C_B = \frac{\varepsilon_i}{W_{d1}} \tag{4.2}$$

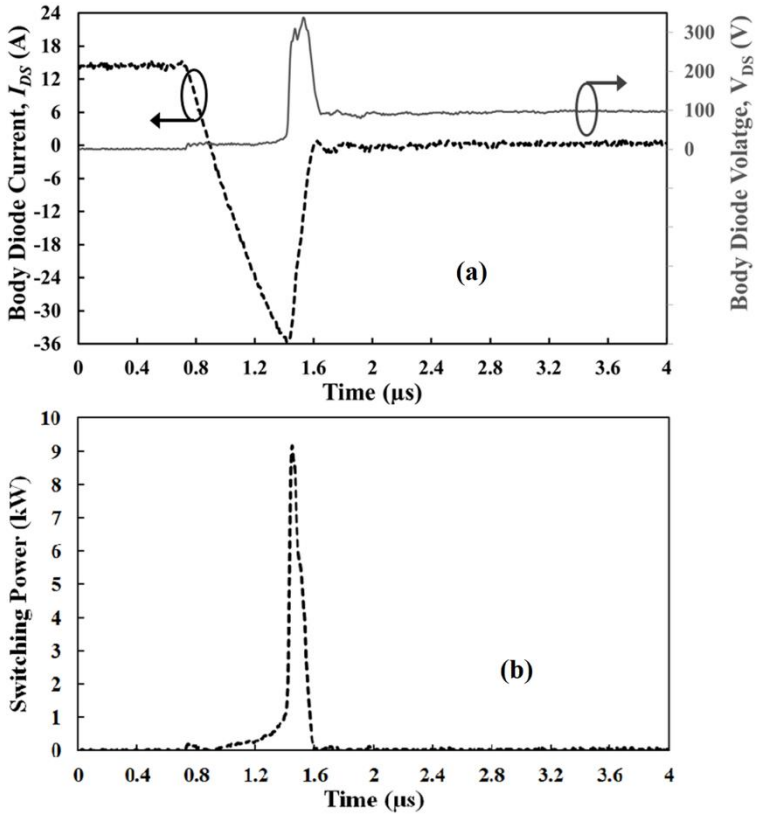


Fig. 4.13 (a) CoolMOS switching-off current and voltage waveform showing high dI/dt and dV/dt at the same instant of time (b) Instantaneous switching power of CoolMOS during the switching-off.

In these two equations, N_A (SiC: 2×10^{17} cm^{-3} and Si: 2×10^{19} cm^{-3}) and N_D (SiC: 1.5×10^{15} cm^{-3} and Si: 1×10^{13} cm^{-3}) are the donor and acceptor doping of the P and N^- region respectively; q is unit electron charge; ε is permittivity of SiC/Si (8.5845×10^{-13} F/cm and 1.05×10^{-12} F/cm respectively); and E_0 is the electric field at the metallurgical junction.

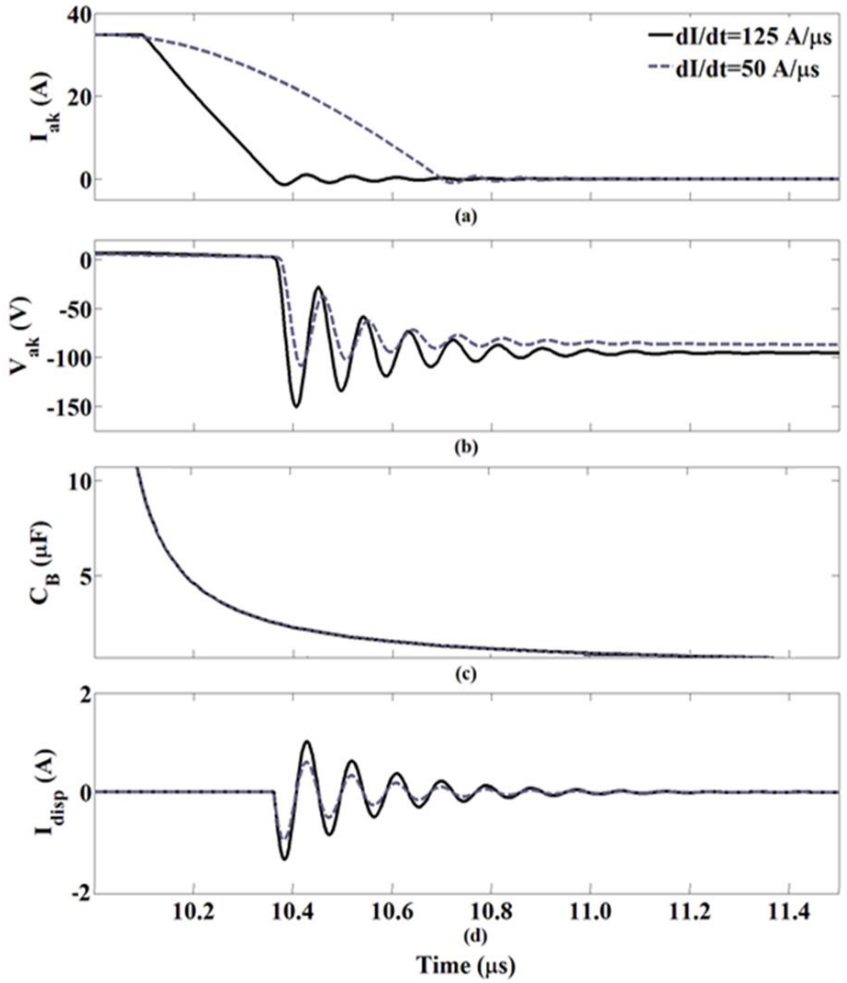


Fig. 4.14 Fourier series ADE simulation of the SiC MOSFET body diode displacement current, parasitic BJT base capacitance and electric field at P+N- junction during turn-off.

As the depletion region widens, the base capacitance of the BJT decreases as shown in Fig. 4.14 (c). The displacement current at the PN^- junction can cause the parasitic BJT to latch-up if there is sufficient body resistance to forward bias the parasitic BJT. This causes BJT latch-up of the device by causing a voltage drop across the emitter-base junction of the BJT greater than the in-built voltage (φ_{BE}). The displacement current shown in Fig. 4.14 (d) is calculated using equation (3.5) below. In this equation, A represents die area and a ratio between the cell size and the P-emitter

of the body diode is considered as the die area of the body diode (SiC MOSFET die area is approximately 10.24 mm^2 and CoolMOS is approximately 20 mm^2 and the body diode ratio is assumed to be in the range of 10-20%). N_{eff} is the effective doping of the depletion region, V_{CE} and V_{DS} are BJT's collector-emitter and MOSFET's drain-source voltages respectively.

$$I_{disp} = \frac{\varepsilon A}{W} \cdot \frac{dV_{DS}}{dt} = \left[\varepsilon A \sqrt{\frac{qN_{eff}}{2\varepsilon V_{CE}}} \right] \frac{dV_{DS}}{dt} \tag{4.3}$$

4.3.2 BJT Latch-up Mechanism

It can be seen from Fig. 4.14 (d) that the peak displacement current increases with the switching rate. This means that faster switching devices are more likely to undergo parasitic BJT latch-up. That displacement current flows through the body resistance (R_{pb}) of the MOSFET which is the resistance between the p-body and the n-source. This p-body resistance (R_{pb}) can be calculated using equation (4.6) where L is the length of the base (0.9×10^{-4} cm), N_B is the base doping (2×10^{17} cm^{-3}) and A_B is the area of the base:

$$R_{pb} = \frac{L}{q\mu_p N_B A_B} \tag{4.4}$$

The mobility of holes (μ_p) in the base of the BJT is temperature dependent. Consequently, increasing the temperature reduces the hole mobility, hence increasing the base resistance. This increases the base-emitter voltage of the BJT. This

temperature dependency for silicon-based devices are explained in Chapter 3 which can be applied directly for CoolMOS. The temperature dependence of μ_p [59] for SiC is shown in equation (4.5). The critical MOSFET parameter that contributes to avalanche breakdown is the body resistance, which must be minimized for a rugged MOSFET. In the equation below, index of *i*, indicates holes or electrons. *T* is temperature of the device, N_{pg}, γ_p, α_p, and β_p depends on type of the material and *N* is the dopant concentration.

$$\mu_i = \mu_{i,\max} \frac{B_{i(N)} \left(\frac{T}{300} \right) \beta_i}{1 + B_{i(N)} \left(\frac{T}{300} \right)^{(\beta_i + \alpha_i)}} \tag{4.5}$$

$$B_{i(N)} = \left(\frac{\mu_{p,\max}}{\mu_{p,\max} - \mu_{p,\min}} \right) \frac{\left[1 + \left(\frac{N}{N_{pg}} \right)^{\gamma_p} \right]}{\left(\frac{N}{N_{pg}} \right)^{\gamma_p}} - 1 \Bigg|_{T=300K}$$

$$\beta_p(4H - SiC) = 0.5$$

$$\alpha_p(4H - SiC) = 2.6$$

$$\gamma_p(4H - SiC) = 0.5$$

$$\mu_{p,\max}(4H - SiC) = 117 cm^2 V^{-1} s^{-1}$$

$$\mu_{p,\min}(4H - SiC) = 30 cm^2 V^{-1} s^{-1}$$

$$N_{pg}(4H - SiC) = 10^{19} cm^{-3}$$

$$N = N_B = 2 \times 10^{17} cm^{-3}$$

By multiplying the body-resistance in the displacement current induced by the P^+N^- junction of the PiN body diode, the base-emitter voltage (V_{BE}) of the BJT is calculated.

$$V_{BE} = I_{disp} \times R_{pb} \tag{4.6}$$

The built-in voltage φ_{bi} of the parasitic BJT can be calculated using equation (3.7) below:

$$\varphi_{bi} = \frac{KT}{q} \ln\left(\frac{N_B N_E}{n_i^2}\right) \tag{4.7}$$

In which K is Boltzmann constant, N_B and N_E (1.2×10^{19} cm^{-3}) are the base and emitter doping respectively and n_i is the intrinsic carrier concentration which is also temperature dependent and increases with temperature (T). Equation (4.8) shows this temperature dependency [60].

$$n_i(4H-SiC) = 1.7 \times 10^{16} T^{3/2} e^{-(2.08\times10^4)/T} \tag{4.8}$$

If the voltage drop across the base-emitter of the BJT becomes greater than the built-in voltage of the parasitic BJT, then the BJT switches on and a current starts flowing from the collector to the emitter of the BJT.

4.3.3 BJT Ebers-Moll Model

In the proposed electro-thermal model, the Ebers-Moll model is used to calculate the collector current. The applicability of Ebers-Moll model for large signal modelling is shown in [60-63].

$$I_C = \alpha_F I_{ES}\left(e^{\frac{(V_{BE}-\varphi_{bi})}{V_T}} - 1\right) \tag{4.9}$$

$$I_{ES} = qA\left(\frac{D_e n_i^2}{L_E N_E} + \frac{D_b n_i^2}{W_B N_B}\right) \tag{4.10}$$

D_e and D_b are diffusion coefficients which are related to the electron mobility in the emitter and base of the parasitic BJT using Einstein relation (kinetic theory). L_E is emitter length, N_E is emitter doping and W_B is the base width of the BJT. The electron mobility can be calculated using equation (4.11) in which N_D is donor doping. The interdependency of the two currents which explain the interaction between the junctions is α_F which is the forward transfer ratio and is typically 0.98.

$$D_e = \frac{KT}{q}\mu_{n,E} \tag{4.11}$$

$$D_b = \frac{KT}{q}\mu_{n,B}$$

$$\mu_{n,E}(4H-SiC)=\frac{4.05\times10^{13}+20\times N_D^{0.61}}{3.55\times10^{10}+N_D^{0.61}}$$

$$\mu_{n,B}: N_D = 2\times10^{17} cm^{-3}$$

$$\mu_{n,E}: N_D = 2\times10^{19} cm^{-3}$$

4.3.4 Electro-Thermal Model Positive Feedback Loop

As the BJT turns on, the current passing through the device generates heat and the device temperature starts rising which increases the base resistance and the body voltage. Consequently, the positive feedback loop increases the parasitic BJT forward current. This continues to generate more power until the temperature excursion due to the instantaneous power causes the device to latch-on and consequently causes the device to break down. The calculated power is inserted into Cauer-network to model the junction temperature of the chip. Fig. 4.15 illustrates the cross section view of a basic hypothetical power device mounted on top of a DBC and the equivalent Cauer-network of this power module.

The flow chart of the model developed in Simulink is shown in Fig. 4.16. As can be seen in this figure, the temperature calculated from the thermal network [64] is fed back in a closed loop to recalculate the temperature dependent parameters in the clamped inductive circuit, base resistance, intrinsic carrier concentration and the BJT base and collector currents. As can be seen in Fig. 4.16, if the BJT does not latch-up,

then the current continues to flow in the body diode until it reaches zero and the simulation model works in *Loop1* showed in the figure.

The values of thermal resistors and capacitors for the Cauer-network are calculated by taking these steps:

Step 1- finite sample points from the transient thermal impedance curve (junction to case) obtained from a single pulse power input of the power device was captured from the device datasheet (Cree SiC MOSFET and Infineon CoolMOS CE technology).

Step 2- Using curve fitting tool in MATLAB, a rational fitting method is used to reconstruct the curve (Fig. 4.17). Here Cauer-network impedance equation is considered to be the base of curve fitting as it can give physical meaning to each layer; however, Foster network may be used as well.

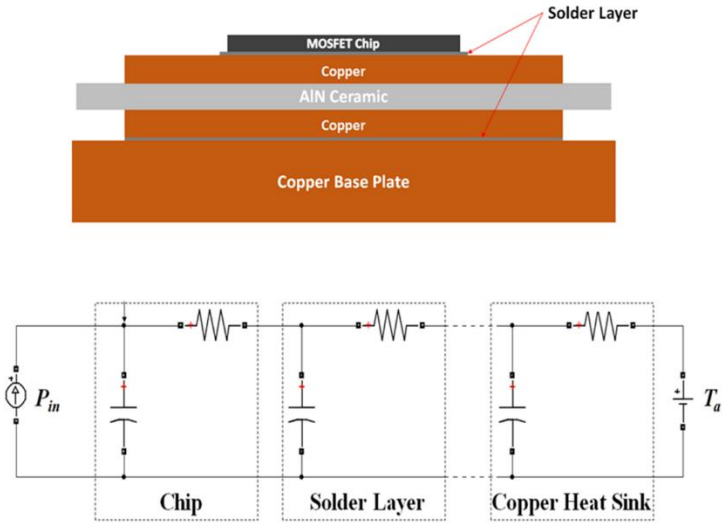


Fig. 4.15 Cross section view of a basic hypothetical die mounted on top of a DBC and soldered to a base plate and the corresponding Cauer-network of this power module.

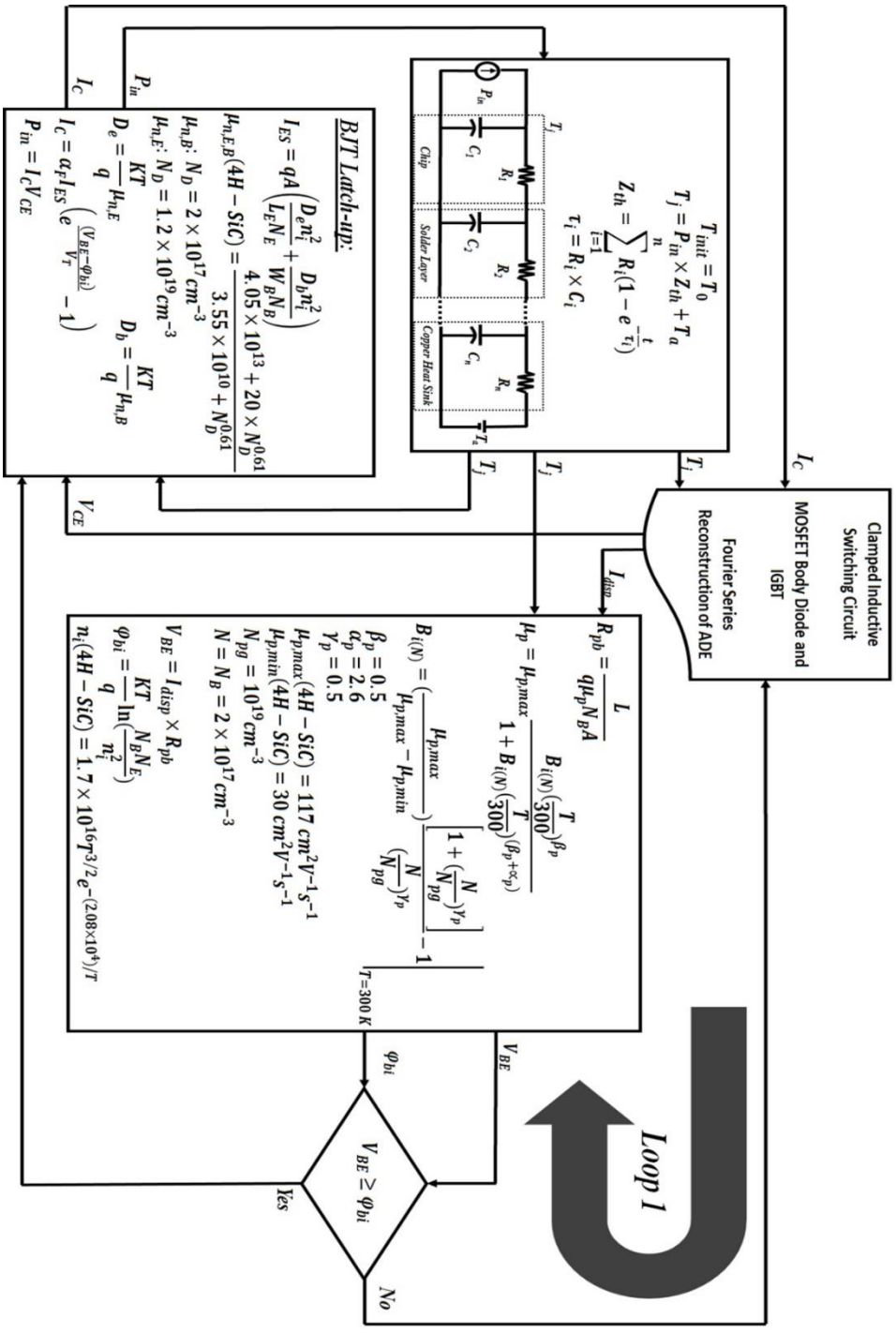


Fig. 4.16 Block diagram of the electro-thermal parasitic BJT latch-up coupled with the clamped inductive switching circuit model for a MOSFET body diode.

Each parameter in the curve fitting tool is set to have an upper and lower limits based on the geometry, specific heat capacity, density and thermal conductance of the material to achieve reasonable values for thermal resistance and thermal capacitance of the Cauer-network thermal chain. Note that based on the Cauer-network impedance equation, the numerator degree is one order smaller than the denominator degree. It is critical for this study to have an accurate curve fitting within the μs level as the transient occurs in μs. Consequently, 5th order Cauer network is considered for both SiC MOSFET and CoolMOS which in case of TO-247 may be interpreted as the die, solder layer, adhesive layer, the copper base plate, CTE-matched high flow EMC (epoxy moulding compound) packaging. Equation (4.14) shows the reconstruction of the thermal impedance using rational curve fitting for the device:

$$Z_{th} = \frac{p_1 s^4 + p_2 s^3 + p_3 s^2 + p_4 s + p_5}{s^5 + q_1 s^4 + q_2 s^3 + q_3 s^2 + q_4 s^1 + q_5} \tag{4.12}$$

Step 3- The impedance from the junction to case of a Cauer-network can be calculated using equation (4.15):

$$Z_{th}^{'} = \cfrac{1}{C_1 s + \cfrac{1}{R_1 + \cfrac{1}{\ldots + \cfrac{1}{C_i s + \cfrac{1}{R_i}}}}} \tag{4.13}$$

Step 4- Since the denominator of equation (4.14) is one order higher than the numerator, by calculating the admittance of equation (4.14), the value of C_1 can be

calculated. By inverting the remainder of this calculation, the impedance of the remainder can be calculated which will result in the value of R_1. By continuing this process, R_1, R_2, C_1, and C_2 are calculated. Table 4.1 shows the calculated values for SiC MOSFET and CoolMOS devices. The differences between the thermal parameters of the CoolMOS and SiC Power MOSFET arises from the difference in die sizes primarily. As a result of the wide bandgap and higher critical electric field, the SiC MOSFET is a smaller die compared to the CoolMOS hence it has a higher thermal resistance and a smaller thermal capacitance. The model with the Fourier series method of reconstructing the charge storage region is described in [57, 65] where the parameters are defined and techniques for extracting the values for these parameters are described in detail. The values for parameters come directly from measurements and datasheets information. The parameters for the electro-thermal model and parasitic BJT are obtained from the measurements and datasheet information and by comparing the simulation waveforms with the experimental results.

The Cauer-network is assumed to consist 5 levels (in case of TO-247 packaging is die, solder attach, standard copper base metal, CTE-matched high flow epoxy and conventional moulding compound encapsulation). In addition, the thermal resistances and capacitances have been restricted within pre-calculated physical limits based on the device geometry and physical constants like material density and heat capacity. This brings about a very good fit between the datasheet transient thermal impedance curve and the fitted curve using the method explained.

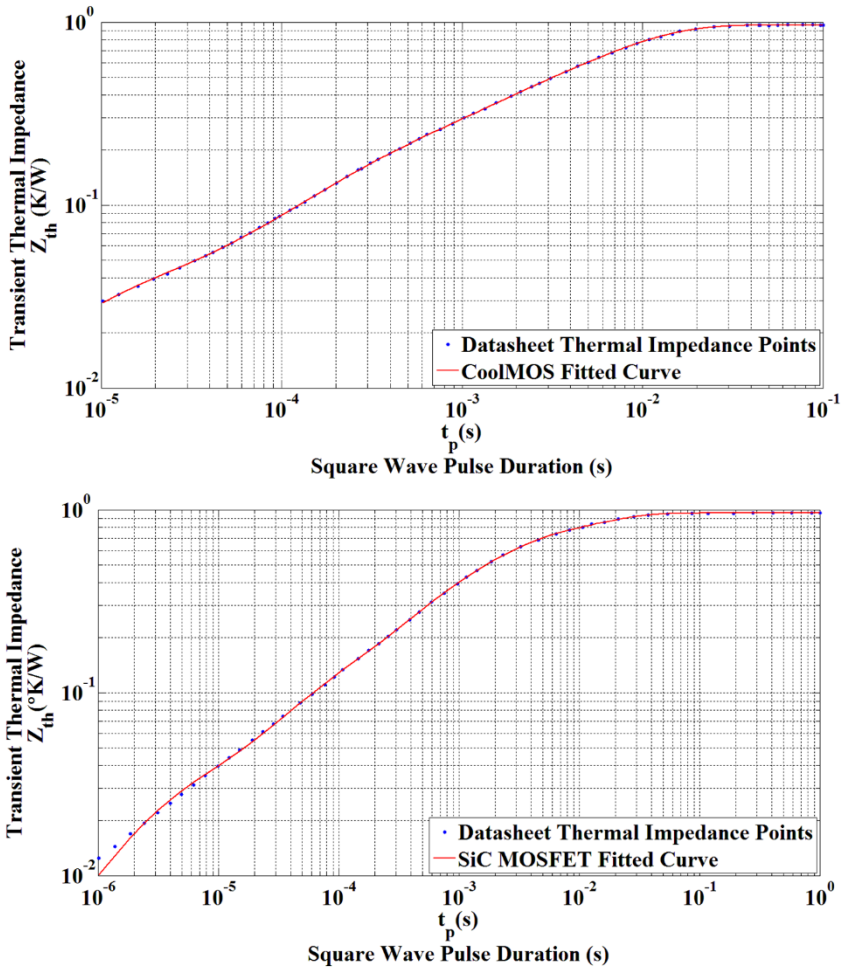


Fig. 4.17 Fitted curve of the transient thermal impedance of Infineon CoolMOS and Cree SiC MOSFET.

The goodness of the fit for the CoolMOS thermal transient curve is:

Goodness of fit:

SSE:	0.0001797
R-square:	1
Adjusted R-square:	1
RMSE:	0.001731

The goodness of the fit for the SiC thermal transient curve is:

Goodness of fit:

SSE:	0.001885
R-square:	0.9997
Adjusted R-square:	0.9997
RMSE:	0.006545

This shows a very good fit between the data available from the datasheet and the fitted curve. The upper and lower values of the parameters in curve fitting have been set to have the thermal resistance and capacitance of the die within the reasonable values in order to get a better calculated temperature. For instance, thermal resistance of the CoolMOS with die area of $5mm \times 5mm$ will be in the range of:

$$R_{th} = \frac{L}{K_{th} A} = \frac{140 \times 10^{-6}}{145 \times \left(5 \times 5 \times 10^{-6}\right)} = 0.0386 \left(m^2 \cdot °K / W\right) Lower \quad Limit \qquad (4.14)$$

$$R_{th} = \frac{L}{K_{th} A} = \frac{220 \times 10^{-6}}{145 \times \left(5 \times 5 \times 10^{-6}\right)} = 0.0607 \left(m^2 \cdot °K / W\right) Upper \quad Limit \qquad (4.15)$$

In the above equations, L is the thickness of the die and Kth is thermal conductivity which is the time rate of steady heat flow through a unit area of a homogenous material induced by a unit temperature gradient in a direction perpendicular to that unit area ($145 W / m.°K$ for Silicon).

Thermal resistance of the SiC MOSFET would be in the range of:

$$R_{th} = \frac{L}{K_{th}A} = \frac{140\times10^{-6}}{120\times\left(3.2\times3.2\times1^{-6}\right)} = 0.1139\left(m^2\cdot°K/W\right)Lower \quad Limit \quad (4.16)$$

$$R_{th} = \frac{L}{K_{th}A} = \frac{200\times10^{-6}}{120\times\left(3.2\times3.2\times10^{-6}\right)} = 0.1628\left(m^2\cdot°K/W\right)Upper \quad Limit \quad (4.17)$$

And the thermal capacitance of a CoolMOS is calculated as below:

$$C_{th} = V\rho C_p = 5\times5\times140\times10^{-12}\times2329\times712 = 0.0058\,Lower \quad Limit \quad (4.18)$$

$$C_{th} = V\rho C_p = 5\times5\times220\times10^{-12}\times2329\times712 = 0.0091Upper \quad Limit \quad (4.19)$$

In the above equation, V is the volume of the die in m^3, ρ is the density of Silicon in Kg/m^3 and C_p is specific heat of Silicon in $W/Kg.°K$. In the case of the thermal capacitance, the slightly higher values obtained from the experimental curve fitting can be attributed to the fact that the temperature dependency of thermal capacitances has not been incorporated into the pre-calculations.

Table 4.1 Thermal resistance and thermal capacitance for devices calculated from the transient thermal impedance curve of devices

CoolMOS		**SiC MOSFET**	
R_1	0.03867	**R_1**	0.1164
R_2	0.194	**R_2**	0.08321
R_3	0.3111	**R_3**	0.2618
R_4	0.4003	**R_4**	0.2845
R_5	0.02277	**R_5**	0.2136
C_1	1.99×10^{-4}	**C_1**	3.3381×10^{-4}
C_2	1.281×10^{-3}	**C_2**	9.084×10^{-4}
C_3	4.576×10^{-3}	**C_3**	7.875×10^{-4}
C_4	8.694×10^{-3}	**C_4**	5.281×10^{-3}
C_5	3.187×10^{-1}	**C_5**	5.874×10^{-2}

4.4 Results and Discussion

Using the clamped inductive switching circuit, two different failure modes were captured. The devices under test were a Si-based super-junction MOSFET (P/N: 726-IPW90R340C3) from Infineon and a Cree SiC power MOSFET (P/N: C2M0160120D). The gate and source of the MOSFETs were clamped and their body diodes were used as freewheeling diodes in the clamped inductive switching test rig. By increasing the first pulse duration during the inductor charging phase of the double pulse test, different forward currents were passed through the body diodes and the waveforms were captured. This current was increased until the device failed. The maximum forward current that triggers a fail during turn-off is defined as the latching current for each technology.

4.4.1 SiC and CoolMOS Latch-up Waveforms

Fig. 4.18 (a) shows the reverse recovery current waveform of the SiC MOSFET body diode at different forward currents. The SiC MOSFET has a very small carrier lifetime in the intrinsic region in comparison to Si-based devices and consequently, the reverse recovery of these devices is significantly shorter than silicon devices. As can be seen, the device failed at 42 A forward current as the parasitic BJT latched up. Fig. 4.18 (b) illustrates the reverse recovery waveform obtained from the CoolMOS device body diode during the reverse recovery. As can be seen, by increasing the forward current density, the reverse recovery increases as a result of higher stored charge which

is unlike the silicon carbide MOSFET where the reverse recovery current of the body diode was independent of the forward current. At the forward current of 44 A, there is sufficient rise in the junction temperature to cause failure in the device. It can also be noticed that the CoolMOS device typically fails during reverse recovery whereas the SiC device fails during the turn-off transient and that the *dI/dt* of the SiC body diode is higher than that of the CoolMOS. Due to a very high *dV/dt* and sudden fall of the voltage, the voltage waveform during the failure was not captured.

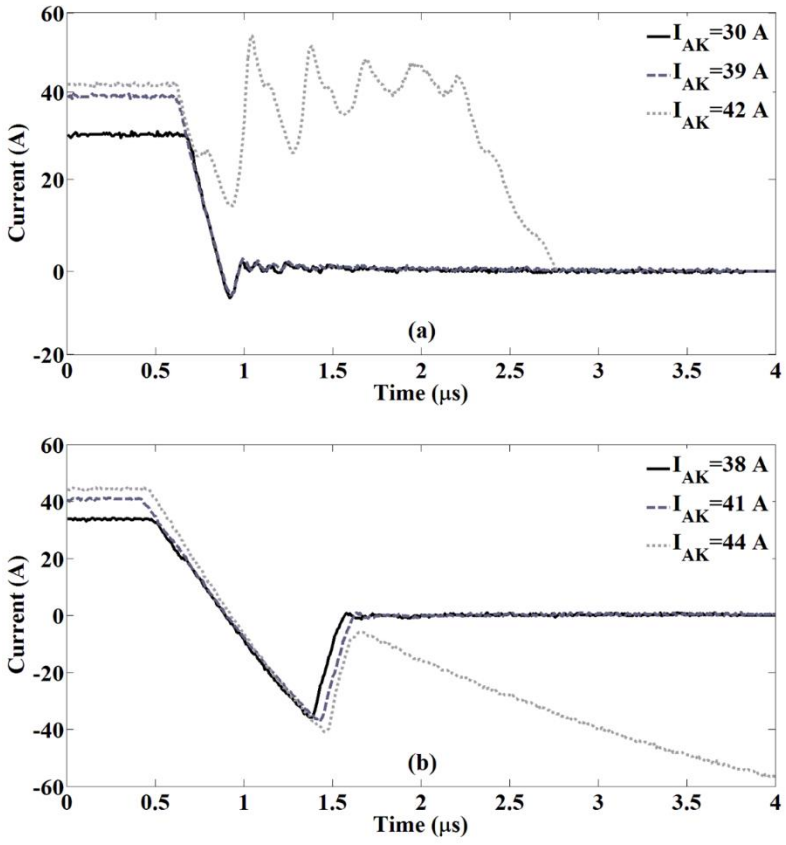


Fig. 4.18 (a) Experimental results showing SiC MOSFET body diode reverse recovery at varied forward currents. (b) Experimental results showing CoolMOS body diode reverse recovery at varied forward current.

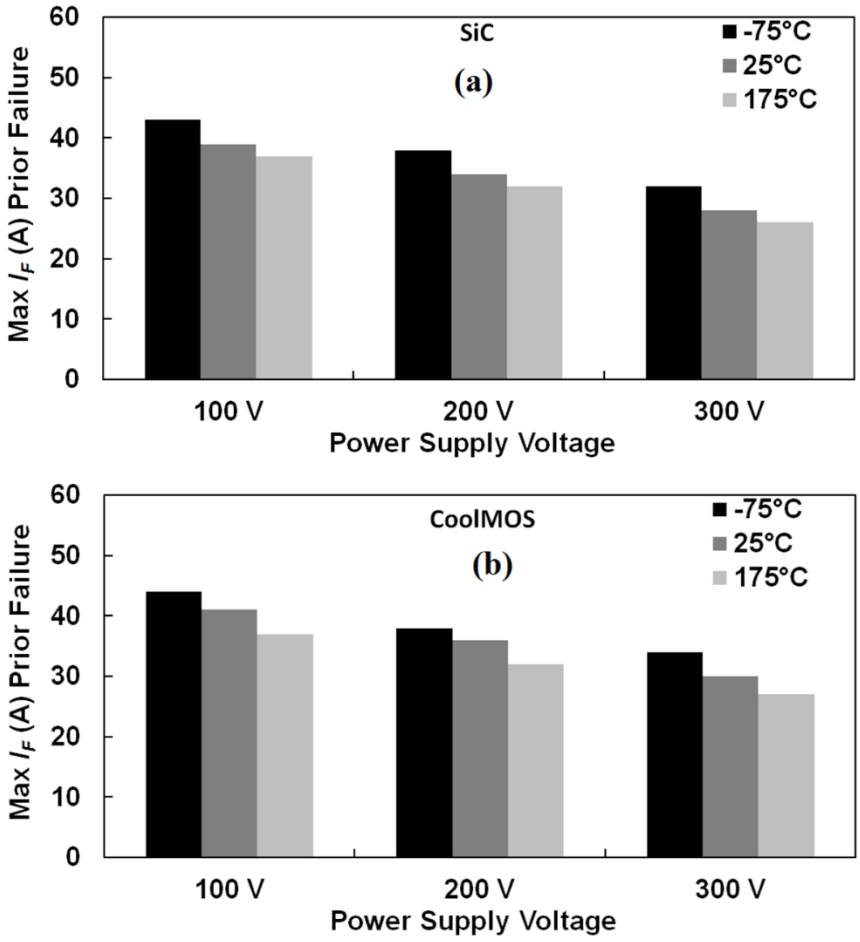


Fig. 4.19 (a) Parasitic BJT latch-up current at different temperatures (SiC MOSFET). (b) Parasitic BJT latch-up at different temperatures (CoolMOS).

4.4.2 Latch-up Temperature and Voltage Dependency

The impact of temperature and the supply voltage on the latching current was investigated for the SiC and CoolMOS devices. The temperature was varied from -75 °C to 175 °C and the supply voltage was also varied from 100 V to 300 V. Similar to the previous measurements, the forward current was increased until the device failed

during reverse recovery of the body diode. Fig. 4.19 (a) shows the parasitic latch-up current for SiC MOSFET at different temperatures while Fig. 4.19 (b) shows the same graph for CoolMOS power MOSFET. As the supply voltage and temperature are increased, the latching current for device failure decreases as is expected because both voltage and temperature contribute to BJT latch-up.

As explained earlier, if the parasitic BJT latches up the device might fail. There are different parameters that cause the parasitic BJT to latch up during the reverse recovery of the body diode such as high *dV/dt*, high current density and high temperature. Using the introduced electro-thermal model for the parasitic BJT, the impact of increasing the current density and temperature on the SiC MOSFET and CoolMOS body diode can be investigated.

4.4.3 BJT Latch-up Dynamics

Fig. 4.20 shows how the electro-thermal BJT latch-up model of the SiC MOSFET behaves under normal condition when there is no thermal runaway (normal), as well as when the device undergoes thermal runaway (latch-up). The condition that triggers thermal runaway in this case, is a higher forward current.

As can be seen from Fig. 4.20, as the body diode undergoes the switching transient in (a) for 2 different forward currents, the instantaneous power dissipated across the diode shown in (b) causes a temperature rise. The instantaneous power dissipation increases with the forward current.

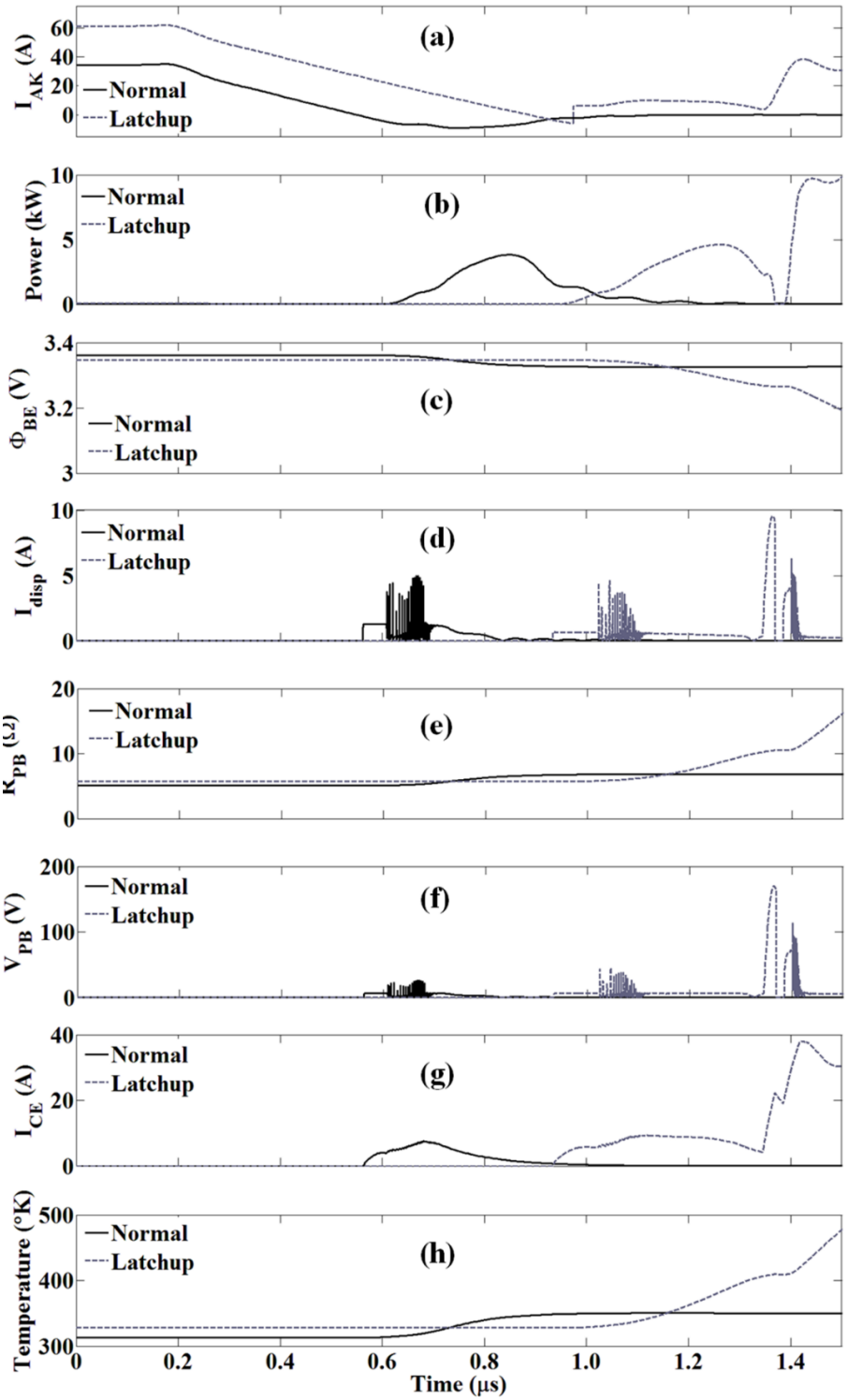


Fig. 4.20 Parasitic BJT transient electro-thermal behaviour; comparison between the SiC MOSFET PiN diode under normal switching condition and under BJT latch-up.

This temperature rise causes the in-built junction voltage (Φ_{BE}) to fall as shown in Fig. 4.20 (c). It can be seen from Fig. 4.20 (c), that the device with the higher forward current experiences a higher drop in Φ_{BE} due to higher dissipated power. The fall in Φ_{BE} is as a result of increased carrier concentration from bandgap narrowing shown in equation (4.7).

Fig. 4.20 (d) shows the displacement current (I_{dsip}) caused by the charging of the drain-body depletion capacitance and the impact of the dissipated power on the p-body resistance (R_{PB}) is shown in Fig. 4.20 (e). The rise in R_{PB} is due to the increasing temperature calculated from the thermal network and caused by the power dissipated during the turn-off of the body diode. It can be seen that the device with the higher forward current has a higher rise in R_{PB}.

Fig. 4.20 (f) shows the body voltage (V_{PB}) which is $I_{disp} \times R_{PB}$ and acts as the base-to-emitter voltage of the parasitic BJT. At the point where V_{PB} becomes greater than Φ_{BE}, the parasitic BJT turns on and produces a collector-to-emitter current (I_{CE}) calculated from the Ebers-Moll model in equation (4.9).

Fig. 4.20 (g) shows the calculated I_{CE} for the 2 parasitic BJTs where the device with the higher forward current can be seen to exhibit a more rapid increase in I_{CE} with no corresponding decrease. It can also be seen from Fig. 4.20 (g), that although the device with the smaller forward current has a parasitic BJT that turns on, however, the temperature rise is such that does not allow the positive electro-thermal feedback process to set in.

Fig. 4.20 (h) shows the respective temperature plots for each device. The model developed in Fig. 4.20 has been used to simulate the behaviour of the device under three different forward currents.

The results are shown in Fig. 4.21 for the SiC MOSFETs and Fig. 4.22 for the CoolMOS MOSFETs. Fig. 4.21 and Fig. 4.22 explain the experimental observations of Fig. 4.18 and Fig. 4.19 using the developed model. As can be seen from the results of the model, the predicted rise in temperature and the on-set of thermal runaway occurs at higher forward currents for both technologies. The model correctly predicts that the higher forward current causes higher instantaneous power dissipation as well as higher body diode reverse recovery charge (in the case of the CoolMOS) which triggers thermal runaway as a result of BJT latch-up.

Fig. 4.21 (a) shows the SiC MOSFET body diode turn-off characteristics at different forward currents whereas Fig. 4.21 (b) shows the calculated temperature from the flowchart shown in Fig. 4.16. For the normal operation mode the temperature rise was approximately estimated to rise around $1\,^{\circ}C$ and $1.5\,^{\circ}C$ for the normal operation of the devices at 33A and 42A respectively in the single switching event. This small temperature rise is due to the small reverse recovery of SiC MOSFET and small energy dissipation within the device for a single switching event.

Fig. 4.22 (a) and Fig. 4.22 (b) show similar plots for the CoolMOS device where it can be seen that the model is capable of predicting BJT latch-up at higher forward current densities. The model can also be used to accurately predict the impact of temperature on the thermal runaway during reverse recovery. Simulations have

therefore been performed at different ambient temperatures to investigate how well the model predicts latch-up at different temperatures. At higher temperature, the mobility of the hole is reduced and consequently, the p-body resistance increases. This brings about higher base-emitter voltage and causes the parasitic BJT's high current.

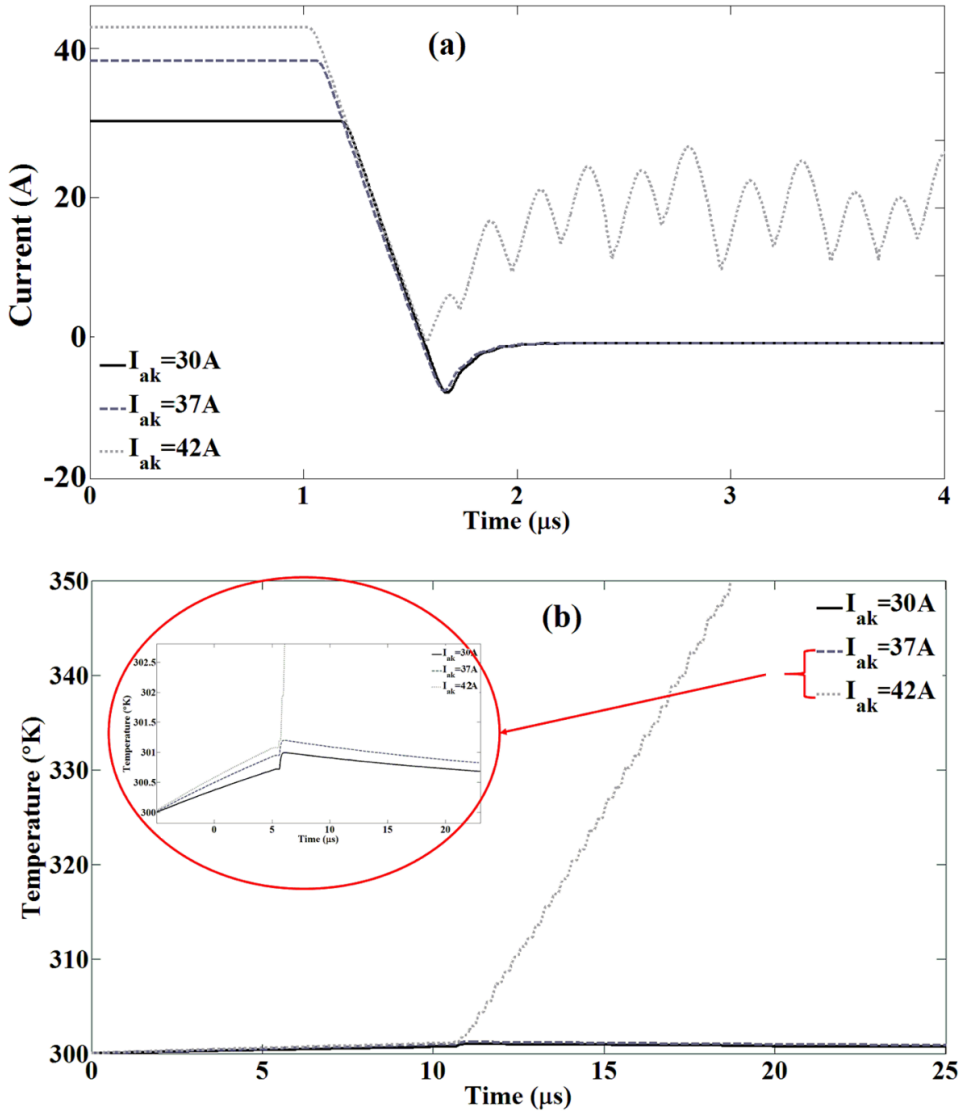


Fig. 4.21 (a) Simulation results showing reverse recovery waveform of SiC MOSFET body diode for varied forward current. (b) Temperature rise within the device during the body diode reverse recovery.

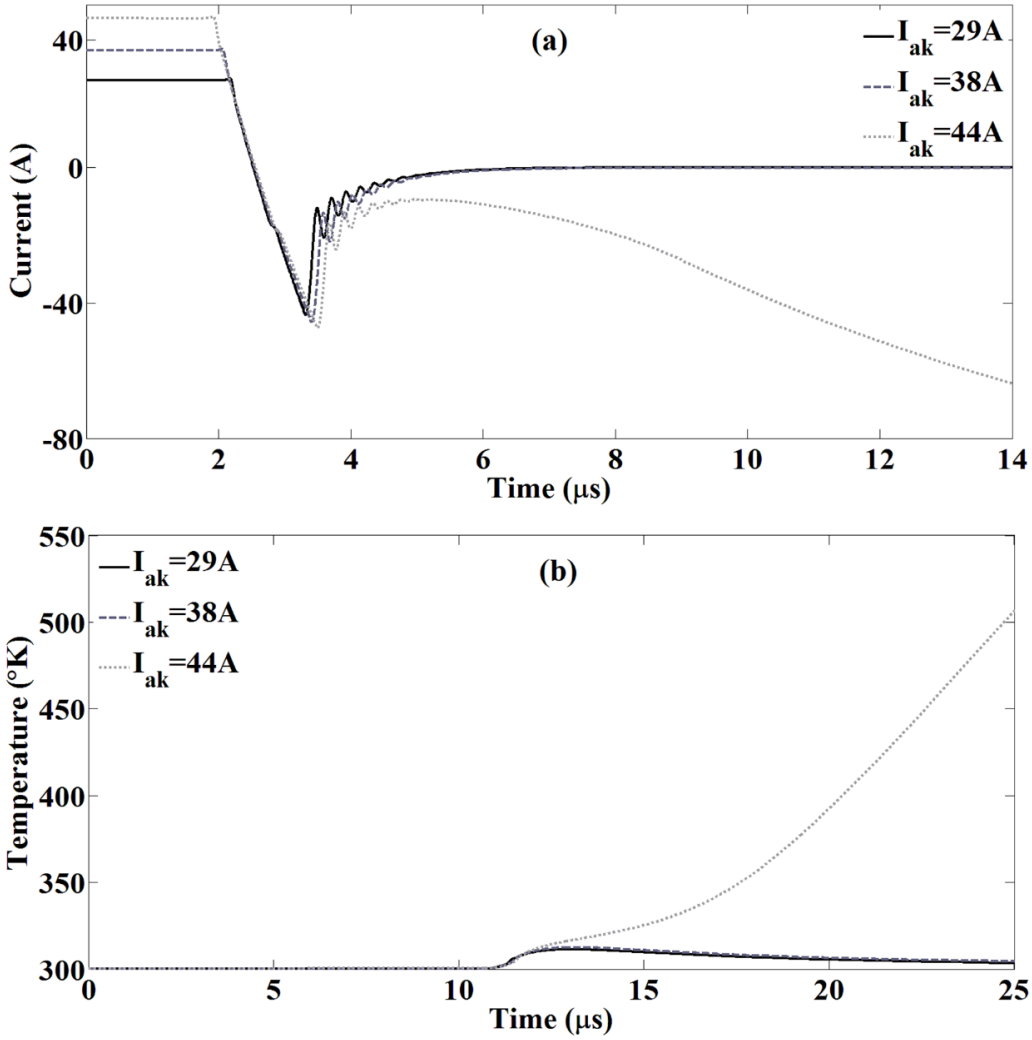


Fig. 4.22 (a) Simulation results showing reverse recovery waveform of CoolMOS body diode for varied forward current. (b) Temperature rise within the device during the body diode reverse recovery.

Fig. 4.23 (a) shows the body diode turn off current characteristics for the SiC MOSFET at three different temperatures (25°C, 75°C and 125°C). As can be seen, the device fails at 125°C due to thermal runaway. The calculated temperature is shown in

Fig. 4.23 (b) for the SiC MOSFET where it can be seen that thermal runaway results in an uncontrollable rise in temperature.

Fig. 4.24 (a) shows the body diode current turn off characteristics for the CoolMOS device at different temperatures similar to Fig. 4.23 (a) for the SiC MOSFET. Fig. 4.24 (b) shows the simulated temperature of the CoolMOS device corresponding to Fig. 4.24 (a). By comparing Fig. 4.24 (b) to Fig. 4.23 (b), it can be seen that the rate of temperature rise for the SiC MOSFET is larger than the CoolMOS. This is due to smaller thermal capacitance of the SiC die in comparison to the CoolMOS. The differences between the SiC MOSFET and the CoolMOS device arises from the difference between the thermal resistances (which is dependent on the die size), the semiconductor material and the device architecture. The SiC MOSFET is able to sustain a significantly larger avalanche current density in spite of having a higher thermal resistance. This is due to the wide bandgap which makes the device more temperature resilient.

The SiC device fails during turn-off before the zero crossing of the current because of the combination of high *dV/dt* and the drain-to-body depletion capacitance generating a displacement current which flows through the body resistance and triggers the parasitic BJT.

The high thermal resistance of the MOSFET coupled with the temperature sensitive body resistance means that the device can fail during turn-off as a result of high ambient temperature, high forward current density and higher commutation rates. In case of the CoolMOS device, the excessive reverse recovery charge causes high instantaneous power dissipation which raises the temperature of the device and

triggers the parasitic BJT. Hence, the device fails in reverse recovery after the zero crossing as opposed to the SiC MOSFET where the failure is before the zero crossing.

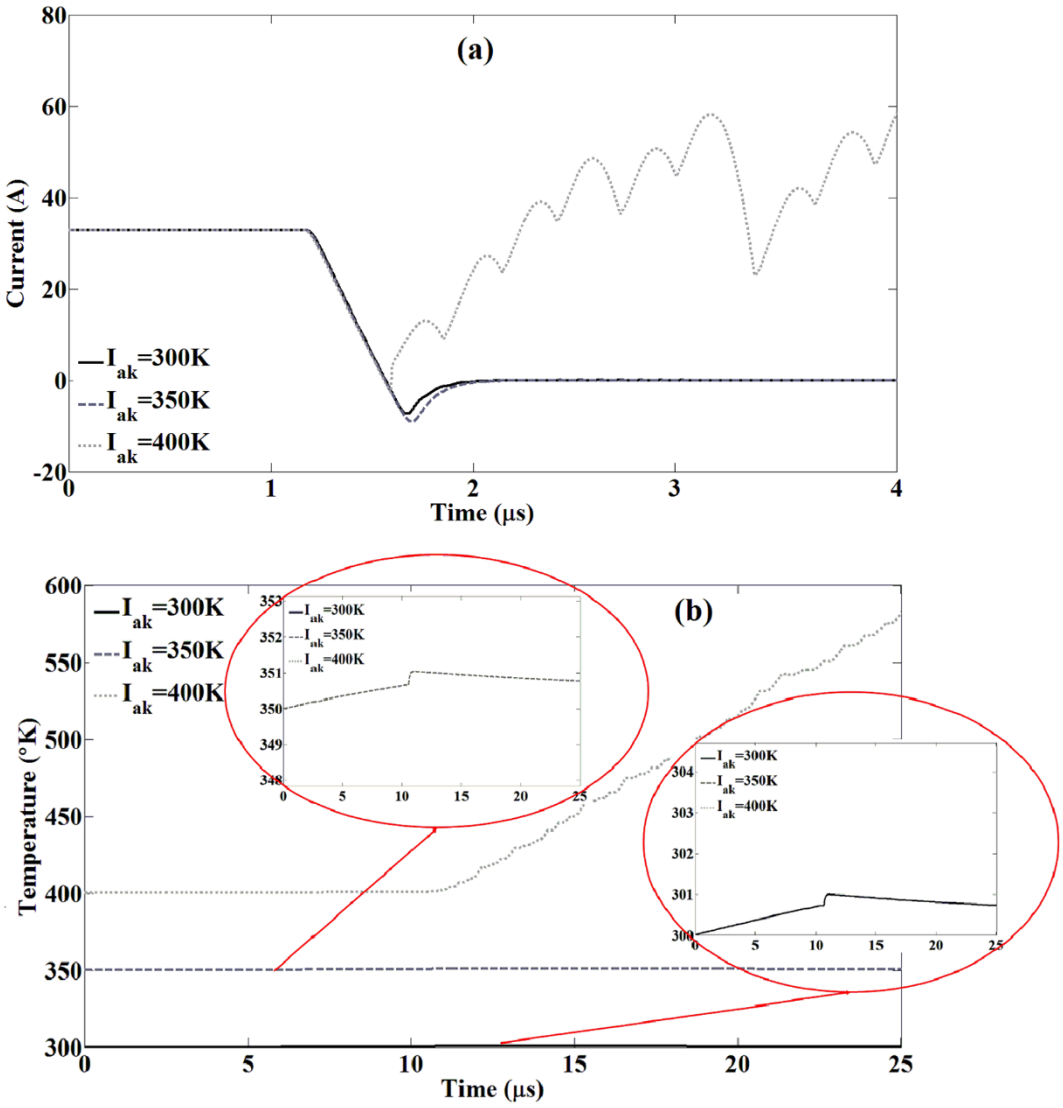


Fig. 4.23 (a) Simulation results showing reverse recovery waveform of SiC body diode for varied temperature. (b) Temperature rise within the device during the body diode reverse recovery.

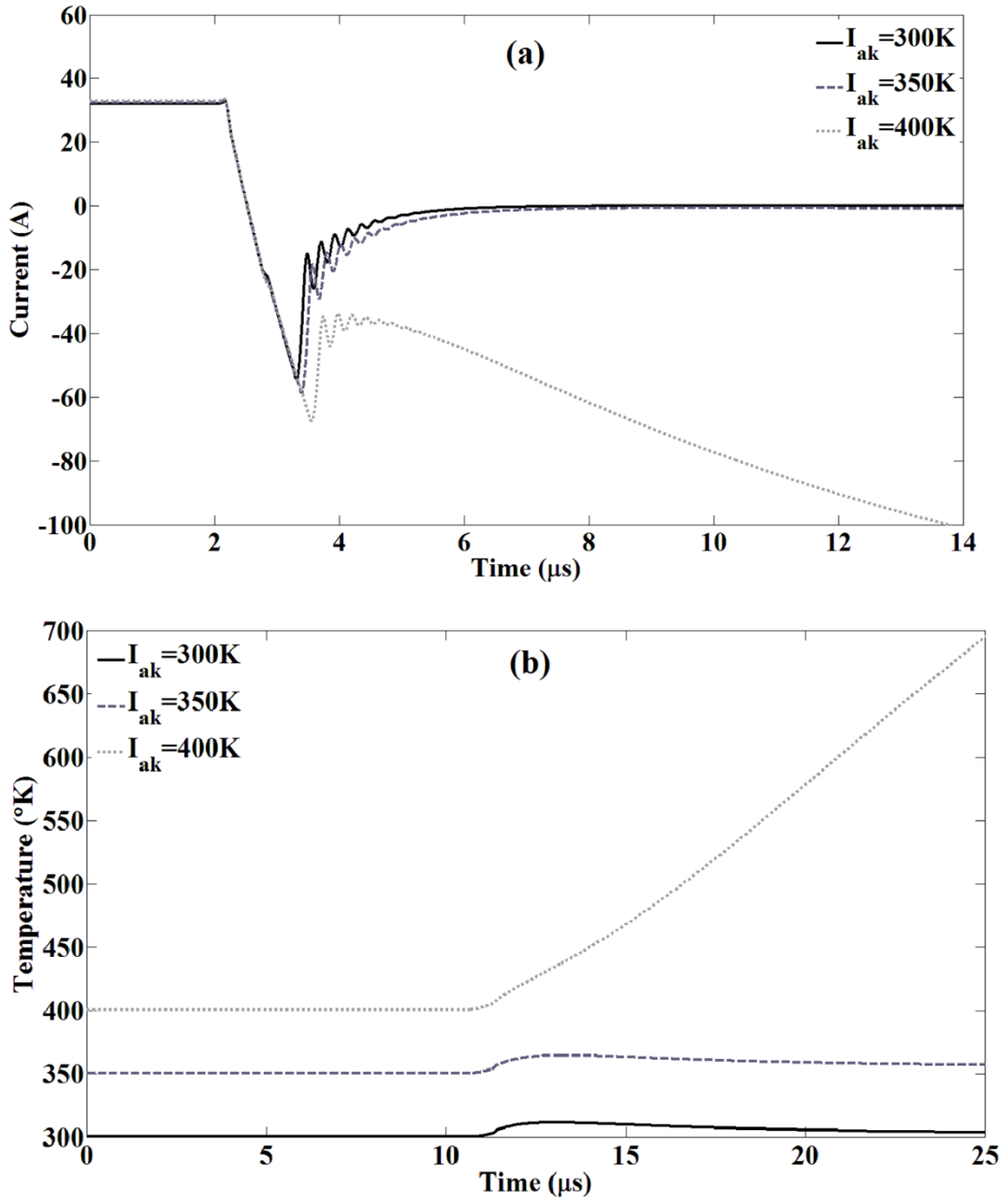


Fig. 4.24 (a) Simulation results showing reverse recovery waveform of CoolMOS body diode for varied temperature. (b) Temperature rise within the device during the body diode reverse recovery.

The difference between the SiC MOSFET and the CoolMOS device arises from the difference between the thermal resistances (which is dependent on the die size), the semiconductor material and the device architecture. The SiC MOSFET is able to sustain a significantly larger avalanche current density in spite of having a higher thermal resistance. This is due to the wide bandgap which makes the device more temperature resilient. The SiC device fails during turn-off before the zero crossing of the current because of the combination of high *dV/dt* and the drain-to-body depletion capacitance generating a displacement current which flows through the body resistance and triggers the parasitic BJT.

The actual die sizes of the destructed SiC and CoolMOS power devices are shown below:

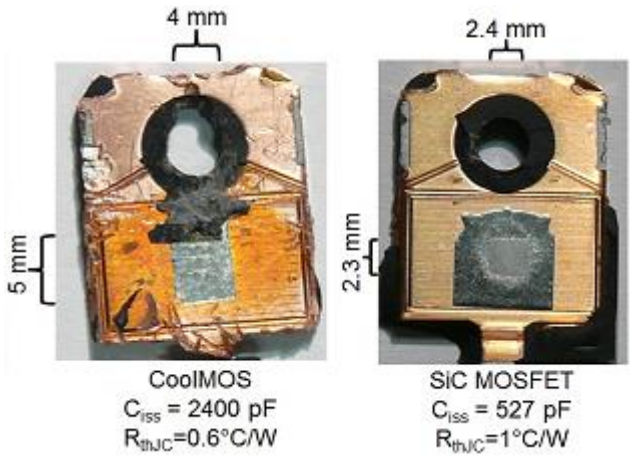


Fig. 4.25 Actual die sizes for SiC MOSFET and CoolMOS devices.

4.5 Conclusions

This chapter has introduced a computationally efficient and accurate compact model that can be used to predict and diagnose electro-thermal bipolar latch-up in power MOSFETs. The model was used to investigate the reliability of SiC MOSFET and super-junction MOSFET body diodes during reverse recovery. SiC Cree MOSFETs and Infineon CoolMOS were tested in a clamped inductive switching test rig and the body diode of the upper switch was used as a free-wheeling diode.

Moreover, the SiC MOSFET PiN body diode and CoolMOS were modelled using the Fourier series reconstruction of the ambipolar diffusion equation to calculate the excessive carrier stored in the drift region during the switching transition. In the case of the CoolMOS device, the ambipolar diffusion equation was modified to account for the fact that electrons will also be minority carriers in the p-pillars of the drift region.

An electro-thermal model of the BJT was developed alongside of the clamped inductive switching circuit to simulate the thermal runaway of these devices under the reverse recovery. The thermal resistance and capacitance for the packaged devices from Cree and Infineon were calculated and used in the Cauer thermal network. Moreover, the temperature of the device at each step of the simulation was fed back to the device and all the temperature dependent parameters were calculated after each step. The reverse recovery of the model was validated by comparing the results with the

experiments. Experiments show that thermal runaway is exacerbated by high current densities and temperatures which is well predicted and replicated by the model.

Chapter

5 Parasitic Induced Gate Switching in Power Devices

This chapter is divided into two sections: (1) A detailed physics-based analysis of parasitic gate turn-on and the resulting shoot-through currents in IGBT modules together with its dependency on switching rate, temperature and switching frequency; and (2) parasitic gate turn-off of SiC MOSFET and the resulting gate bouncing of the device under hard commutation condition and high *dV/dt*. Both of these phenomenon happen parasitically and as IGBTs and SiC MOSFETs are two active switching devices that can be used in automotive applications, these reliability constraints are studied together in this chapter.

Because the minority carrier distribution profile in the IGBT's drift region is simulated by solving the ADE, the dynamics of Miller capacitance discharge and how it shapes the V_{GE} and V_{CE} transients during the short circuit can be explained in detail. Unlike some SPICE models, this model is able to accurately account for non-linear Miller capacitance as well as the temperature dependency of the threshold voltage,

minority carrier lifetime, MOS-transconductance and carrier mobility. As a result, the shoot-through current and power dissipation is accurately predicted. The model has been calibrated by the measured shoot-through currents from 3 IGBT modules from different vendors at different temperatures and switching rates. Some power module manufacturers employ internal damping to avert shoot-through but this is at the cost of limiting the maximum dI/dt that the module can tolerate. In IGBT power modules with no internal damping (this is in form of an external gate-source capacitor and high frequency decoupling capacitors), the peak shoot-through current is shown to decrease with increasing switching frequency due to a low pass filter formed by the half-bridge parasitic elements.

Since the Miller-capacitance is a series combination of a fixed oxide capacitance and a voltage dependent depletion capacitance, the V_{GE} and V_{CE} transients are first dominated by the oxide capacitance at low depletion widths and then by the depletion capacitance as the increasing V_{CE} increases the depletion-width. The parasitic gate transient is typically characterized by 2 peaks; the first peak which is due to the transition of the Miller-capacitance from the oxide to the depletion capacitance and the 2nd peak which is due to the high negative dV_{CE}/dt caused by punch-through as the drift layer becomes fully depleted at high V_{CE}.

Moreover, in this chapter the parasitic gate turn-off in SiC power MOSFETs and the resulting gate bouncing due to rapid switching on and off of the gate drive under hard commutation is analysed and modelled. This phenomenon happens when a SiC MOSFET is used in conjunction with a fast recovery PiN diode as an antiparallel diode.

The reliability of power PiN diode and SiC MOSFET transistors under hard commutation conditions is modelled and experimentally investigated as a function of the commutation rate, supply voltage, forward current and junction temperature. When power PiN diodes are switched off at elevated junction temperatures and high commutation rates, the recombination of high *dI/dt* of the recombination current of the PiN diode and the parasitic source inductance of the bottom side transistor can cause source voltages capable of inadvertently turning off the complimenting transistor (if the parasitic source voltage is greater than the threshold voltage). This results in severe oscillation of current between the transistor and the dio0de with the devices turning on and off uncontrollably. The damping of these oscillation is shown to decrease with increasing temperature and the likelihood of thermal runaway increases with the transistor switching rate and supply voltage. Furthermore, the parasitic drain inductance of the MOSFET coupled with the *dI/dt* of the diode reverse recovery current can cause severe voltage overshoots that may exceed the breakdown voltage of the transistor. In this chapter this phenomenon which is referred to as parasitic gate turn-off is investigated and presented.

This chapter is presented in [66, 67].

5.1 Parasitic Gate Turn-On

By increasing the switching frequency of power devices in voltage source converters (VSC), the probability of unintentional turn-on of the complementing power

switching device in the same leg of the inverter increases. This is as a consequent of high *dV/dt* and *dI/dt* induced by the high switching frequency coupled with the Miller capacitance of the device. This phenomenon is known as cross-talk or parasitic turn-on. High *dV/dt* and *dI/dt* can coupled with the Miller capacitance of the device creates a current which passes through the gate resistance of the device. This can create a gate-emitter voltage greater than the threshold voltage of the device and causes parasitic switch-on of the device. This results in a short circuit occurring across the leg of the inverter [68-71]. The high instantaneous power dissipation caused by the short circuit can be a hazard in the operation of VSCs since this high surge of current is capable of destroying the device. This will degrade the reliability of the module and contribute significantly to the case temperature. This problem is exacerbated by increasing the switching speed of the devices. Hence, it is important to be able to accurately predict and model this shoot through current. The parasitic turn-on can be suppressed by applying negative off-set voltage to the gate-emitter of the device. This creates a larger margin from the off-state of the transistor to the threshold voltage of the device [72, 73]. If *dV/dt* and *dI/dt* are high enough to create a large enough voltage at the gate to turn-on the device through the mechanism explained above, then even the negative voltage might not be able to fully eliminate the gate parasitic turn-on. Applying negative voltage is useful at lower temperatures; however, the negative temperature coefficient of the threshold means that the reduced threshold voltages at elevated temperatures increases the likelihood of shoot-through currents. Consequently the margin between the off-state and the threshold voltage of the transistor reduces, thus,

sufficient high *dV/dt* across the device may create a high enough voltage across the gate-emitter of the IGBT and trigger the device. This is even more important in case of SiC MOSFETs as these devices have significantly smaller threshold voltage and the gate of these devices cannot withstand large negative voltages.

Consequently, it is important for the power electronics engineers to be able to predict the shoot through current as a function of switching rate and temperature. Compact circuit simulators such as PLECS are based on lumped parameters and switching happens instantaneously which means variations in the *dV/dt* cannot be simulated. The device models do not account for threshold voltage, hence, basic modelling the shoot-through phenomenon is not possible in such simulators. On the other hand, the dynamic macro-model of IGBT such as the one used in SPICE is described as a combination of the dc model and nonlinear input capacitance [74] and is predominantly a BJT which is driven using a gate of a MOSFET. The charge stored in the drift region of the IGBT is considered as a lumped charge thereby lacking the accuracy of physics-based models or the finite element simulators. Similarly, the physics-based Hefner device model is also based on lumped charge values [54, 75-79]. This model does not take account of the effect of the temperature on the carrier lifetime, threshold voltage, MOS transconductance and carrier mobility.

During the parasitic turn-on the nonlinear Miller capacitance is important in predicting the shape of the voltage and current waveforms. This is due to the fact that the Miller capacitance is made of two capacitors which are connected in series. One gate oxide capacitor which is constant and one voltage dependent depletion capacitor.

Moreover, the model introduced in chapter 3 is based on the physics of the device and the drift and diffusion equations and can accurately take account of the minority carrier distribution profile in the drift region of the IGBT. The device model solves the ambipolar diffusion equation to model the behaviour of minority carriers and the charge distribution in the charge storage region of the device hence it can predict the depletion widths and as a result the Miller capacitance.

5.2 Parasitic Gate Turn-On Model Development and Experimental Setup

The results obtained for this chapter are tested using an IGBT-based power module with power rating of 1200V/150A. This power module is from DAWIN Electronics Co, Ltd. with part number of DM2G100SH12AE and is 7DM-1 package with a half-bridge topology. The IGBT parameters of this power module is extracted using the methods explained in [34, 57, 65] and the forward characteristic obtained from the IGBT model is compared with the forward characteristic of the datasheet for validation. Fig. 5.1 shows the forward characteristic of the device for different values of V_{GE} and the forward characteristic obtained from the physics-based device model. The dotted lines in this graph are used to obtain the channel length modulation parameter (Lambda).

The shoot-through current is modelled using the physics-based IGBT model in a half-bridge cell. Fig. 5.2 illustrates the schematic of a half-bridge voltage source

inverter used in the test rig to investigate the effect of temperature and switching rate on the shoot-through current in a half-bridge topology.

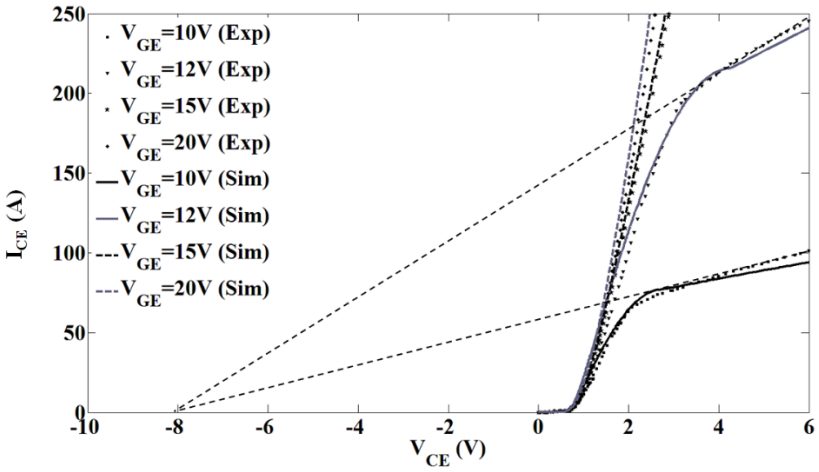


Fig. 5.1 Forward characteristic of DM2G100SH12AE power module and comparison of the datasheet forward characteristic with the device model results.

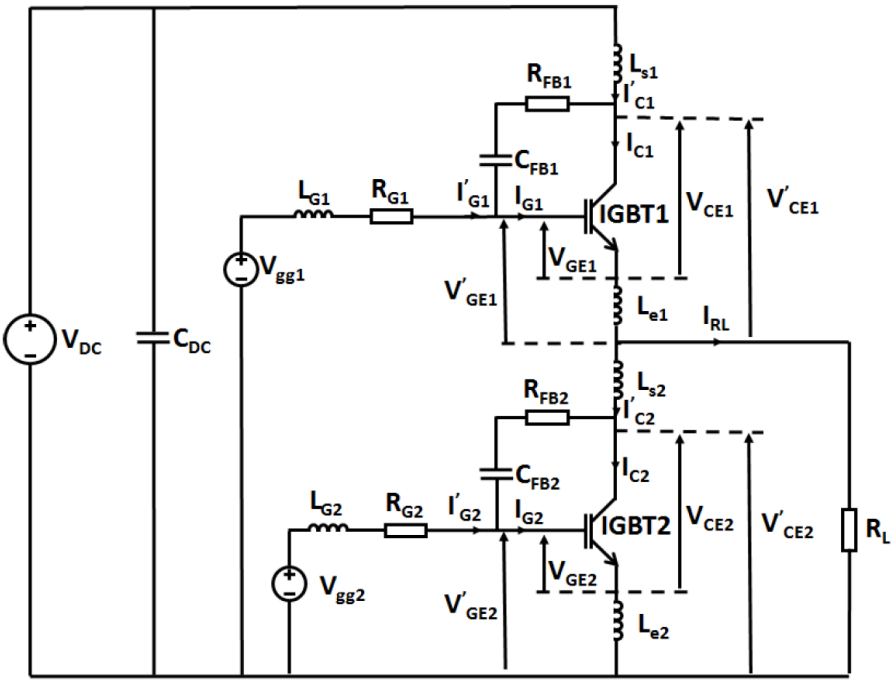


Fig. 5.2 Schematic of a half-bridge topology in a voltage source inverter used to investigate the parasitic turn-on effect.

The model takes account of the parasitic inductances and the gate resistors. In this schematic, L_{s1} and L_{s2} are parasitic stray inductance in the collector of the top and bottom IGBT, L_{e1} and L_{e2} are the Kelvin inductance of the top and bottom IGBT, and L_{G1} and L_{G2} gate inductances of the top and bottom IGBTs respectively. These can physically be interpreted as a combination of inductances from the layout of the power module and the cables connected to the device. The gate resistances at the gate drive for the top and bottom IGBTs are shown as R_{G1} and R_{G2} respectively. R_{FB1}, R_{FB2}, C_{FB1} and C_{FB2} are feedback resistors and capacitors which may be used in the model to improve convergence and they are not physical components but rather used as a numerical trick. The resistive load of R_L is between the collector and emitter of the bottom IGBT.

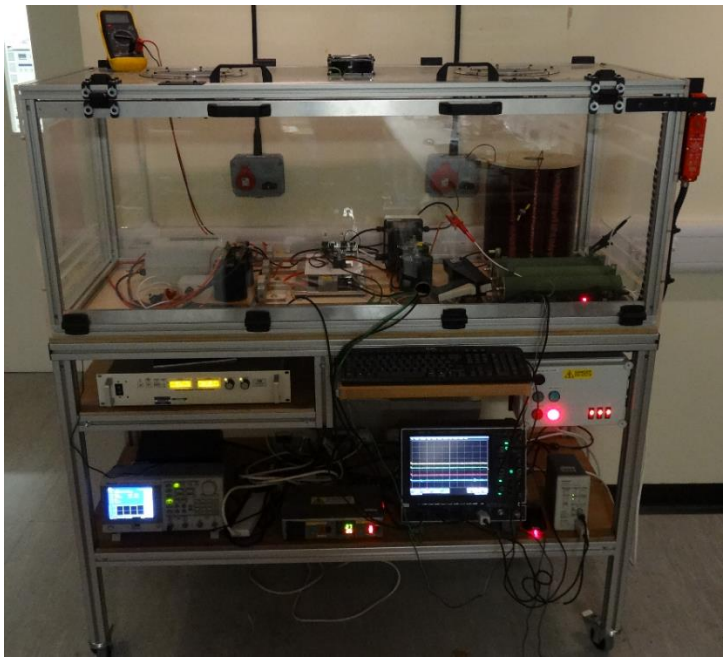


Fig. 5.3 Experimental setup for the parasitic turn-on.

The experimental setup uses the same circuit in the test rig shown in Fig. 5.3. In the model it has been assumed that the DC voltage source can supply infinite amount of current to the circuit to eliminate the oscillations on the DC link capacitor. The resistive load is 1 kΩ. The power module is placed on top a hotplate and the temperature of the device can be varied to investigate the effect of the temperature on the behaviour of the device during the parasitic turn-on.

By applying Kirchoff's voltage and current laws to the circuit shown in Fig. 5.2, the circuit equations used in conjunction with the model explained in Chapter 3 are derived. The complete equations are shown in Appendix E.

5.2.1 Results and Discussion

Cross-talk happens when the high dV/dt and dI/dt on one of the transistors in a half-bridge causes the gate of the complementing device in the same leg to switch-on. This is due to the voltage across the gate-collector capacitor (Miller capacitor) which induces a current at the gate of the transistor. In the experimental setup explained earlier, the top switch is constantly switching and the gate of the bottom switch is shorted to the emitter. When the bottom switch turns on parasitically, a short circuit happens at the leg of the inverter. By increasing the gate resistance of the bottom switch, the parasitic turn-on becomes more significant and the amplitude of the surge of current passing through the device increases.

This increases the junction temperature of both devices and consequently, the threshold voltage of the devices reduces. This causes the shoot-through current increase

and a positive loop can be formed. Hence, rapid switching of the inverter might cause device failure. To validate the behaviour of the model with experiments during the parasitic turn-on, the gate resistance of the top switch is set to be 10 Ω while the gate resistance of the bottom switch is set to 100 Ω. This causes a very large current surge to pass through both devices during the short circuit. In order to change the temperature of the device, the DUTs (devices under test) were mounted on a hot plate and the temperature of the hot plate was controlled. The cross-talk effect can be increased by using a larger gate resistance at the gate of the bottom IGBT which is not switching. In this study, the top gate resistance is kept at 10 Ω while the bottom gate drive is set to be 100 Ω. Under the same conditions, a physics-based model results are compared with the experimental results and SPICE simulation where the model is based on a Hefner model and the parameters are modified to get a match between the simulation and the model. Fig. 5.4 shows the current waveform during the parasitic switch-on. As can be seen, the shoot-through current goes as high as 80 A for a period of 1 μs.

Fig. 5.5 shows the voltage waveform for the same experiment and the comparison between the physics-based model, SPICE and experiments as can be seen, the voltage waveform has two distinct slopes. Both models can predict this behaviour. The SPICE model has been scaled in time to fit in the same window as the experimental result and the physics-based model. Moreover, the SPICE model cannot accurately predict the second slope. This slope is due to the formation of depletion region and depends on the depletion width. This shows the importance of accurately modelling the Miller

capacitance as this has a significant impact on the calculation of power losses during the parasitic turn-on.

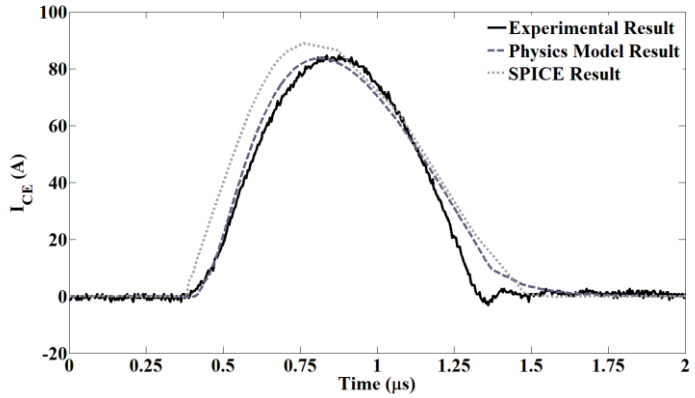


Fig. 5.4 I_{CE} current waveform of the bottom IGBT during the cross-talk, comparison between the experiment, the physics-based model and SPICE.

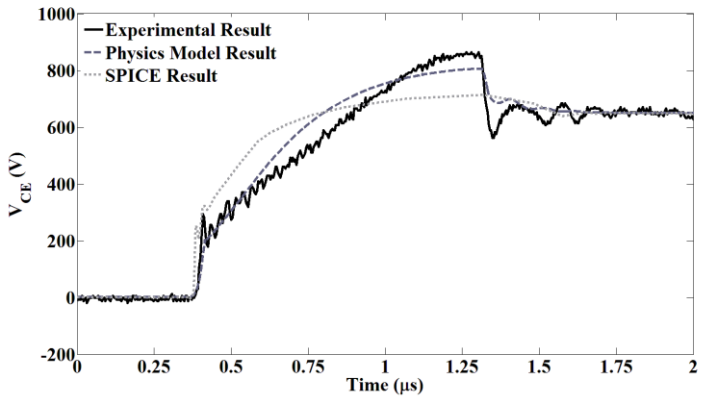


Fig. 5.5 V_{CE} voltage waveform of the bottom IGBT during the cross-talk, comparison between the experiment, the physics-based model and SPICE.

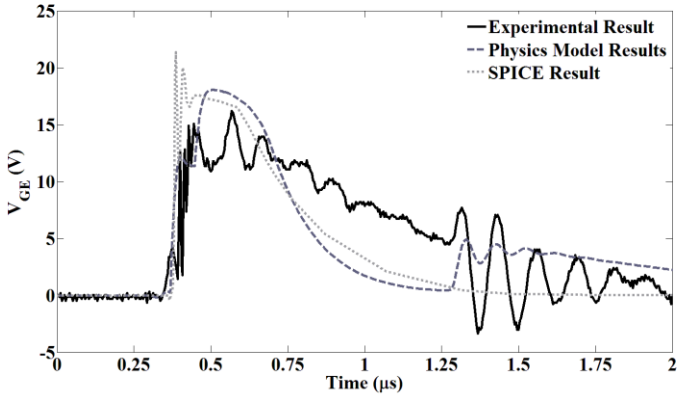


Fig. 5.6 V_{GE} voltage waveform of the bottom IGBT during the cross-talk, comparison between the experiment, the physics-based model and SPICE.

Fig. 5.6 shows the gate-emitter voltage of the device which switches on parasitically. As can be seen, this voltage can be characterized by two peaks. One larger peak at the beginning of the waveform which is due to the high *dV/dt* and *dI/dt* of the top device which is switching. The second smaller peak is due to the negative *dV/dt* in the collector-emitter voltage coupled with the parasitic stray inductance of the collector of the IGBT. This will be explained in detail in this section. As shown in Fig. 5.6, the SPICE model is unable to show the second pulse which is due to the fact that the displacement current due to the formation of the depletion layer in the device is not calculated in the model. In contrast, the physics-based device model can accurately show this behaviour. If the second spike of the gate-emitter voltage is larger than the threshold voltage of the device this phenomenon can repeat. Hence it is important to model this accurately.

Furthermore, to validate the behaviour of the physics-based model, the results obtained from the model for two different gate resistances of 10 Ω and 100 Ω are

compared with the experimental results and are shown in Fig. 5.7, Fig. 5.8 and Fig. 5.9. As can be seen, the model can accurately predict this phenomenon for different gate resistances. The peak current increases significantly by increasing the gate resistance. This is due to the fact that the high *dV/dt* imposed on the complementing device in the same phase leg results in charging the Miller capacitance. Consequently, a current flows into the gate resistance of this device and hence it can create a voltage across the gate-emitter of it. If the gate resistance is larger, the voltage created at the gate of the bottom switch increases and consequently, the current passing through the device increases.

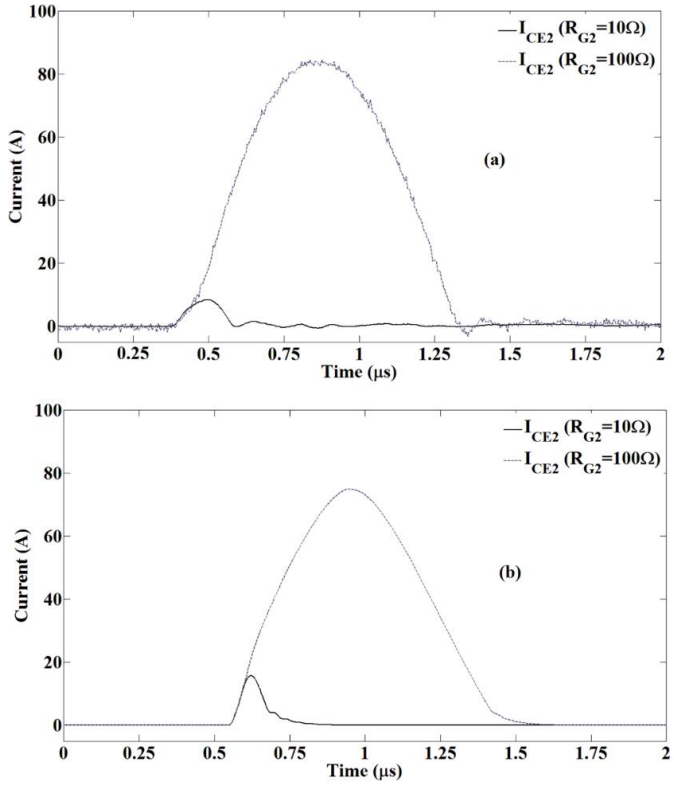


Fig. 5.7 I_{CE} current waveform of the bottom IGBT during the cross-talk for two different gate resistances; (a) Experimental results (b) Physics-based model results.

As explained earlier, the parasitic turn-on happens due to the high *dV/dt* and *dI/dt* of the top switch. This coupled with the Miller capacitance causes the bottom switch to turn-on. Consequently, it is important to investigate the behaviour of the Miller capacitance during the cross-talk. The Miller capacitance is a made of two capacitors. A fixed oxide capacitance and a voltage dependent depletion capacitance.

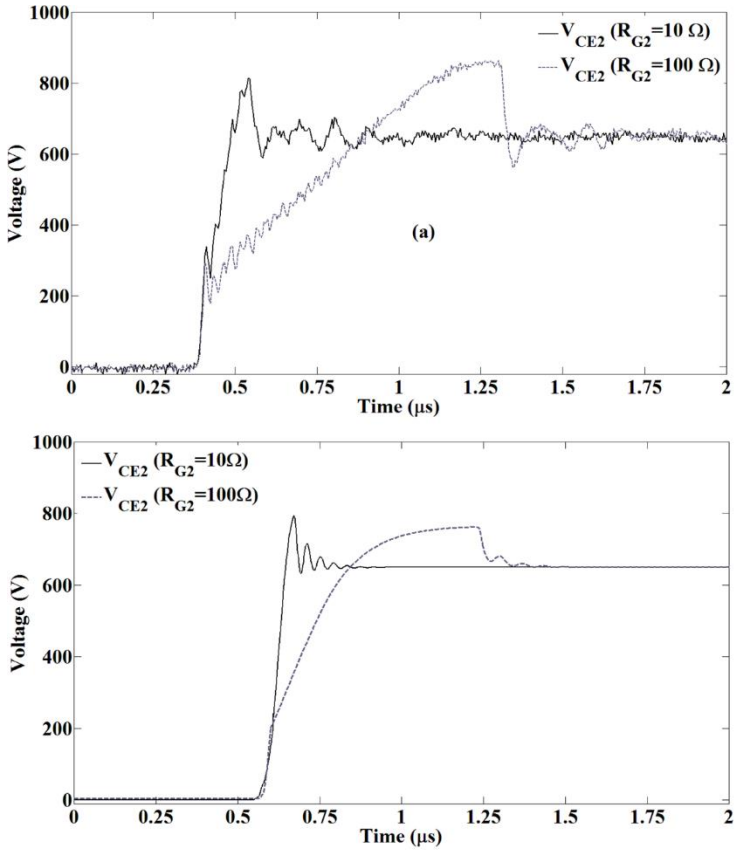


Fig. 5.8 V_{CE} voltage waveform of the bottom IGBT during the cross-talk for two different gate resistances; (a) Experimental results (b) Physics-based model results.

Fig. 5.10 shows a cross section view of a hypothetical IGBT structure during the parasitic turn-on. As can be seen, the channel still exists and the device is conducting. As the voltage across the device decreases, the gate-emitter voltage drops at the same

time; during which, the depletion region starts forming between the P-well and N- drift region. As the drift region grows, the charge stored in the device reduces and the device current decreases. When the device punches through and the depletion width meets at the edges of the drift region, the device current cuts-off. At this point, the device reaches the turn-off threshold.

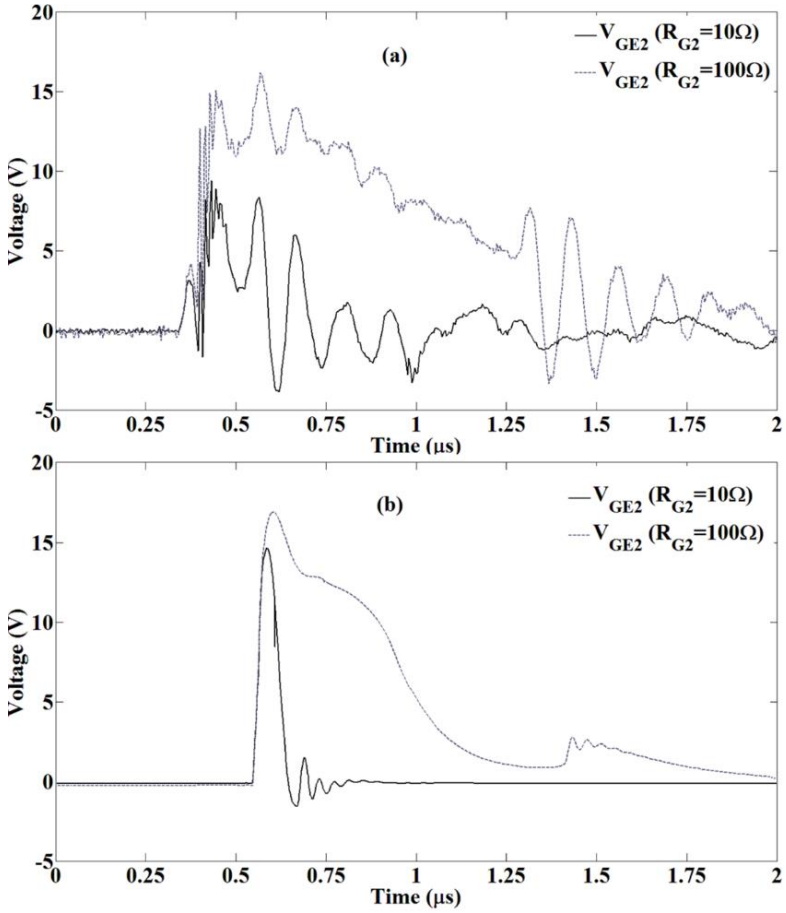


Fig. 5.9 V_{GE} voltage waveform of the bottom IGBT during the cross-talk for two different gate resistances; (a) Experimental results (b) Physics-based model results.

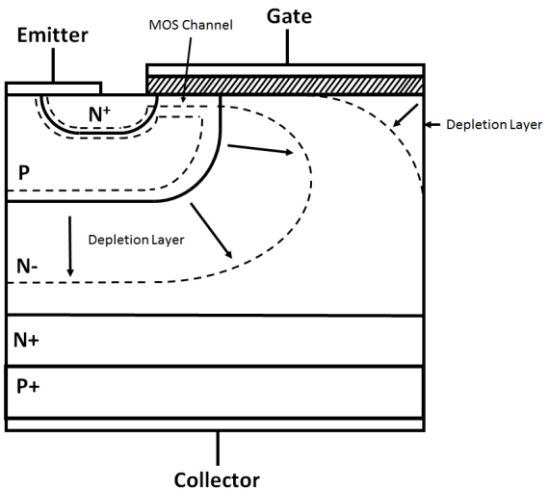


Fig. 5.10 Cross section view of an IGBT showing the process of depletion layer formation.

The Miller capacitance C_{gc} is that of the two dimensional depletion layer between the gate and N- plasma region underneath the gate. This capacitance of an IGBT with the die area of A (cm^2) and intercell area to active device area of a_i is calculated using equation (5.1) to (5.3) as below:

$$C_{gc} = Aa_i C'_{ox}\left(1+\frac{W'_{dg}}{l_m}\left[\frac{1}{\frac{C'_{ox}W_{dg}}{\varepsilon_{si}}+1}-1\right]\right) \tag{5.1}$$

$$W'_{dg} = \min\{W_{dg}, l_m\} \tag{5.2}$$

$$W_{dg} = \sqrt{\frac{2\varepsilon(V_{dg}-V_{ge})}{qN_B}} \tag{5.3}$$

In this equation, C'_{ox} is the oxide capacitance of the IGBT per unit area (Fcm^{-2}), ε_{si} is the permittivity of silicon (Fcm^{-1}), N_B is the base doping of the drift region (cm^{-3}), l_m is the IGBT intercell half-width (μm). V_{dg} determines the width of the gate depletion.

A sharp decrease in Miller capacitance happens when this voltage exceeds zero. This capacitance decrease determines the onset of the main rise in V_{CE}. The decrease in the collector-gate current cannot completely sustain the negative gate current, so the gate-emitter capacitor starts to discharge again consequently, V_{ge} drops slightly. This happens with a slight decrease in the MOS current and hence, the electron current into the drift region falls. This gives a steep negative current density gradient at the end of the plasma region and a faster rate of depletion layer expansion which consequently brings about a faster dV_{ce}/dt. This nonlinear behaviour of the Miller capacitance which depends on the depletion width between the gate oxide and charge storage region is accurately modelled in the physics-based model, helping this model to replicate the transient waveforms.

The cross-talk procedure is explained in details using Fig. 5.11. As can be seen, the process is characterized using three distinct time instances (t_1, t_2 and t_3). As can be seen in the V_{CE1} graph in Fig. 5.11, at t_1 the top device switches on and the voltage across this device starts falling down. This high dV/dt across the top switch results in a high dV/dt across the Miller capacitance of the bottom switch. This coupled with the gate resistance of the bottom switch, makes a peak in the gate voltage of the bottom switch.

As can be seen in V_{GE2} waveform in Fig. 5.11, at t_1 voltage across the gate-emitter becomes greater than the threshold voltage of the IGBT. Consequently, the bottom switch also turns on simultaneously with the turn-on of the top transistor. This brings about a high surge of current caused by the short circuit across the leg of the inverter.

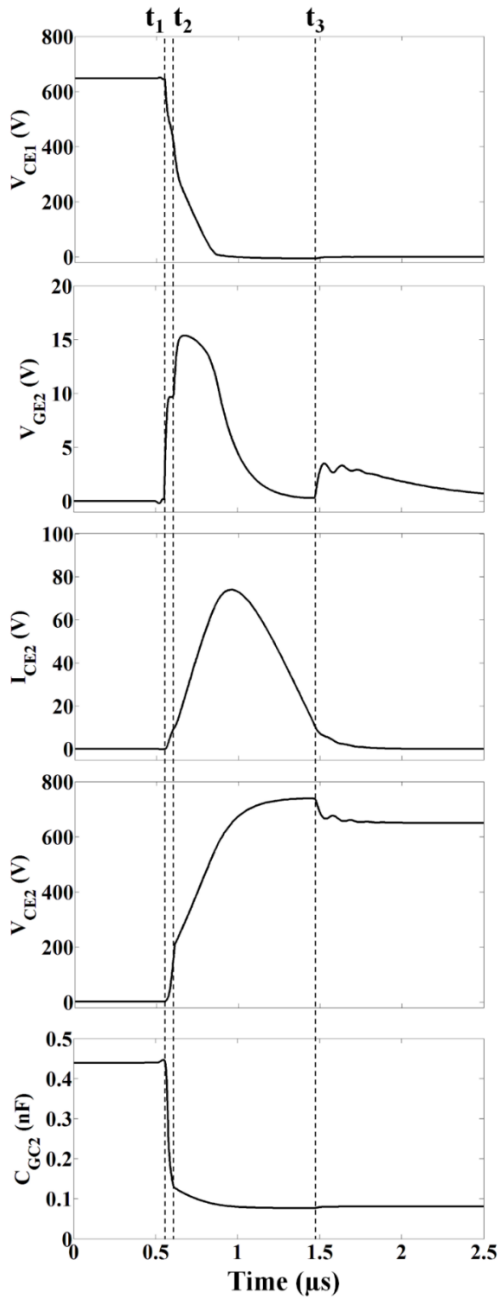


Fig. 5.11 Parasitic turn-on process.

As can be seen in I_{CE2} graph, the current passing through the IGBT starts rising at t_1. At the same time, the Miller capacitance starts falling down. Once the gate voltage of the top IGBT reaches the threshold voltage, the MOS channel starts to conduct and

allows electrons to flow into the drift region. This current flows through the depletion layer at saturation velocity and it runs through the drift region which has not been depleted towards the P-emitter at the bottom of the device.

The holes are also injected in the opposite direction. This causes the voltage to decrease across the device due to the decrease in the electric field slope arising from an extra electron carriers in the charge storage region which causes the decrease in V_{CE1} waveform at t_2. This also brings about the IGBT capacitance discharge. At the same time, the gate voltage of the bottom IGBT reaches a plateau. This plateau is due to the transition of the bottom device Miller capacitance from the oxide capacitance to the voltage dependent depletion capacitance. Between t_2 and t_3, the top switch completely switches on and consequently, dV/dt reduces to zero. This causes the gate of the bottom device start to decrease. Once the gate reaches the threshold voltage the bottom device switches off. At this point, bottom switch Miller capacitance depletes completely and punch-through happens. Consequently, the flow of current through the device is stopped and no current can be fed to the collector stray inductance of the bottom switch. This induces a negative dV/dt across the bottom IGBT at t_3. Coupled with the gate resistance of the bottom switch, the second peak occurs at the gate-emitter of the bottom switch at t_3.

As explained earlier, the two slopes appearing in the voltage waveform during the cross-talk is due to the Miller capacitor. Fig. 5.12 illustrates the effect of the miller capacitance on the two slopes of V_{ce} during the cross talk. Fig. 5.13 shows the effect of gate oxide on the slopes of the emitter-collector voltage.

The two slopes are due to the sudden reduction of the total Miller capacitance as the voltage dependant depletion capacitance starts to decrease as the depletion width expands due to the rising collector voltage. So the initially high dV_{CE}/dt, is due to a series combination of the oxide capacitance and the depletion capacitance whereas the lower dV_{CE}/dt is due to a reduction in the depletion capacitance. Fig. 5.14 shows the effect of the gate resistor on the switching behaviour of the device during the cross-talk.

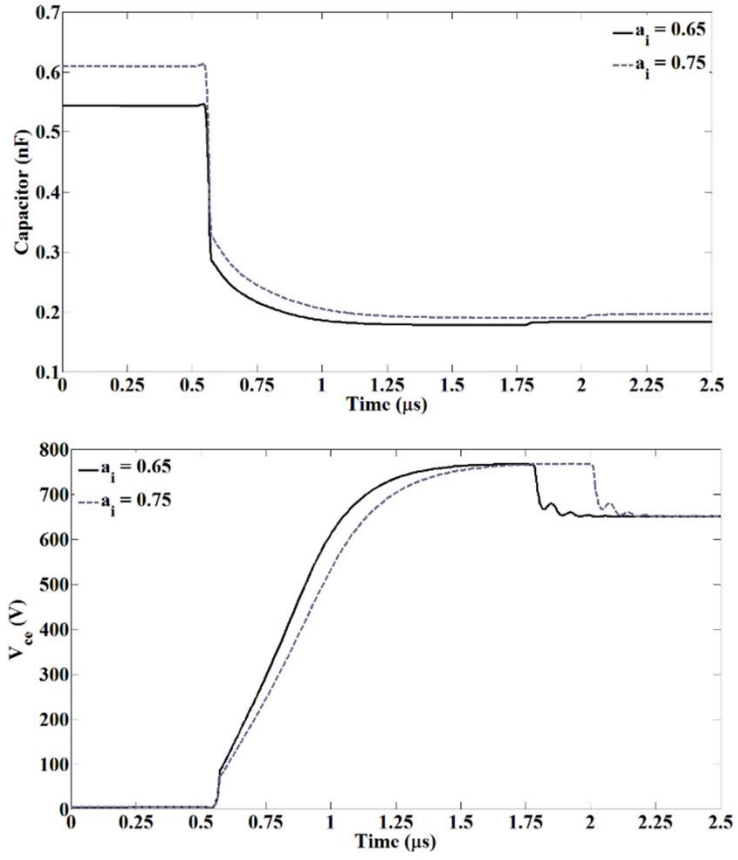


Fig. 5.12 Simulation result showing (a) time dependent gate-collector capacitance for two different values of ratio of intercell area and active die area (a_i) (b) collector-emitter voltage slope change for two different values of ratio of intercell area and active die area.

As can be seen, by increasing the gate resistance, the switching speed reduces (RC time constant increases) and consequently, the Miller capacitance drops more slowly which brings about a significantly smaller V_{CE} slope in comparison to the case that the gate resistance is smaller.

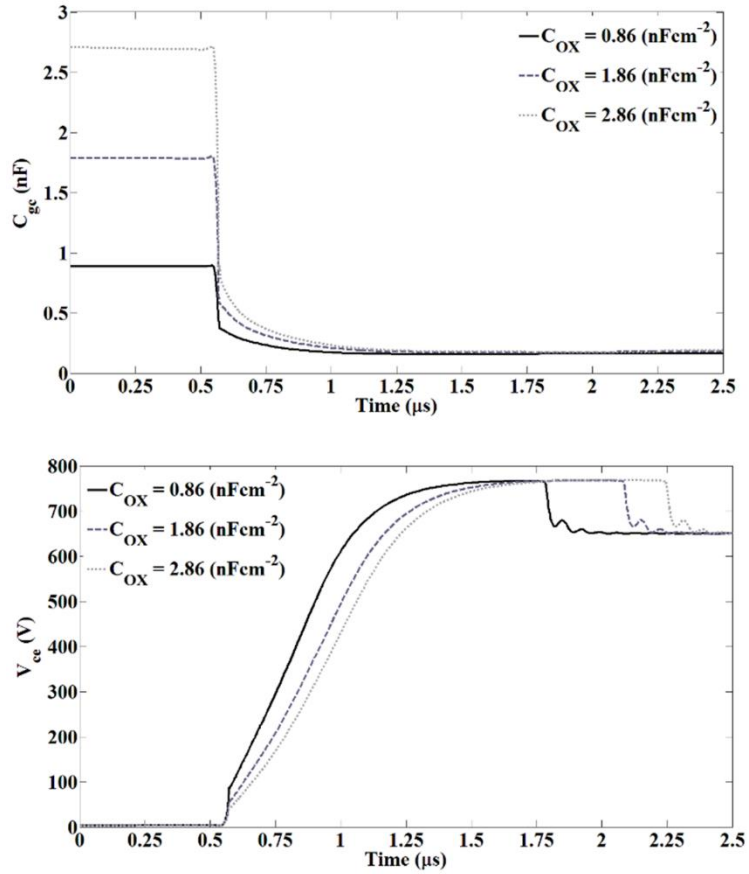


Fig. 5.13 Simulation result showing (a) time dependent gate-collector capacitance for three different values of C_{ox} (b) collector-emitter voltage slope change for three different values of C_{ox}.

Increase in the temperature of the device reduces the threshold voltage of the IGBT. This results in a large overshoot current throughout a larger period of time. Basically the turn-on of the device will be shifted earlier in time and the turn-off of the

device will be shifted later in time increasing the time of the shoot-through current. At the same time, the mobility of electrons and holes change with temperature which consequently has an effect on the transconductance. This effect is not as significant as the threshold voltage.

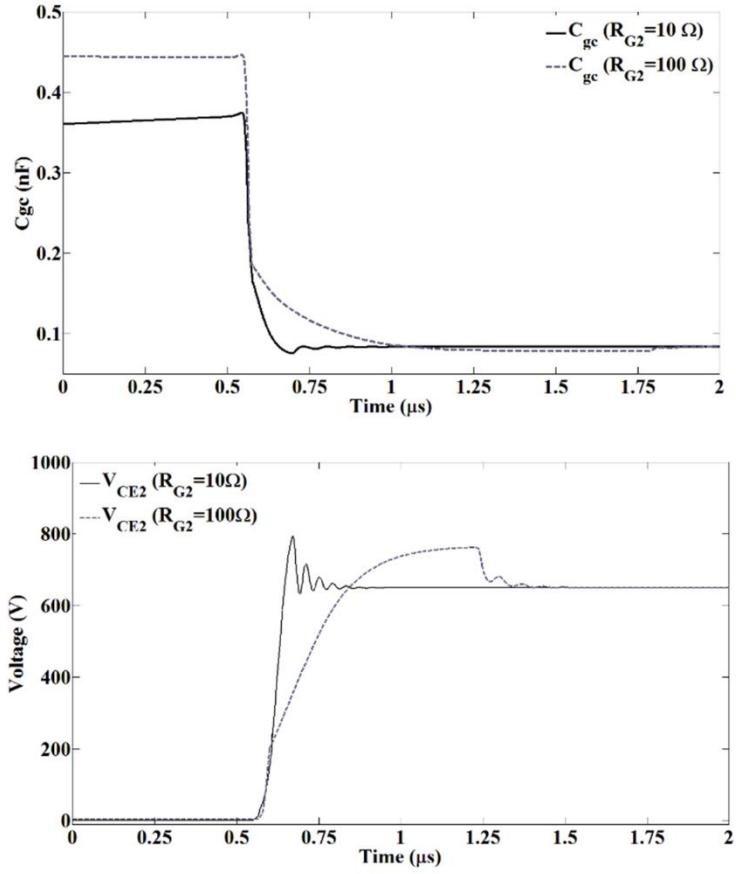


Fig. 5.14 Simulation result showing (a) time dependent gate-collector capacitance for two gate resistances (b) collector-emitter voltage slope change for two gate resistances.

The carrier lifetime in the charge storage region increases with temperature. This causes more charge to be stored in the drift region of the device. Consequently, the

shoot-through current can increase by increasing the carrier lifetime as the on-state resistance of the device is reduced. Equations below describe the effect of the temperature on these parameters. These equations are used in the quasi-static temperature dependent physics-based model to investigate the effect of temperature on the cross-talk phenomenon. The temperature dependency of the following equations have been described in detail in [80-84].

$$V_{th} = V_{th0} - 9\times10^{-3}\left(T - T_0\right) \tag{5.4}$$

$$K_p = K_{p0}\left(\frac{T_0}{T}\right)^{0.8} \tag{5.5}$$

$$\tau_{HL} = \tau_{HL0}\left(\frac{T}{T_0}\right)^{1.5} \tag{5.6}$$

$$\mu_{n,p} = \mu_{n0,p0}\left(\frac{T_0}{T}\right)^{2.5} \tag{5.7}$$

In these equations, T_0 is the room temperature, V_{th0} is the threshold voltage at room temperature. Similarly, K_{p0}, τ_{HL0} and $\mu_{n0,p0}$ are transconductance, high-level lifetime, mobility of electrons and holes at room temperature respectively.

To verify the behaviour of the model with the temperature, the same IGBT power module was tested at different temperatures. The device was placed on a hotplate and the temperature was varied from 25 degrees to 120 degrees and the collector-emitter

voltage and current waveforms and the gate voltage were captured. Fig. 5.15 illustrates the I_{CE} current waveform at different temperatures. As can be seen the peak of the current increases with temperature and the pulse is also longer with temperature as expected.

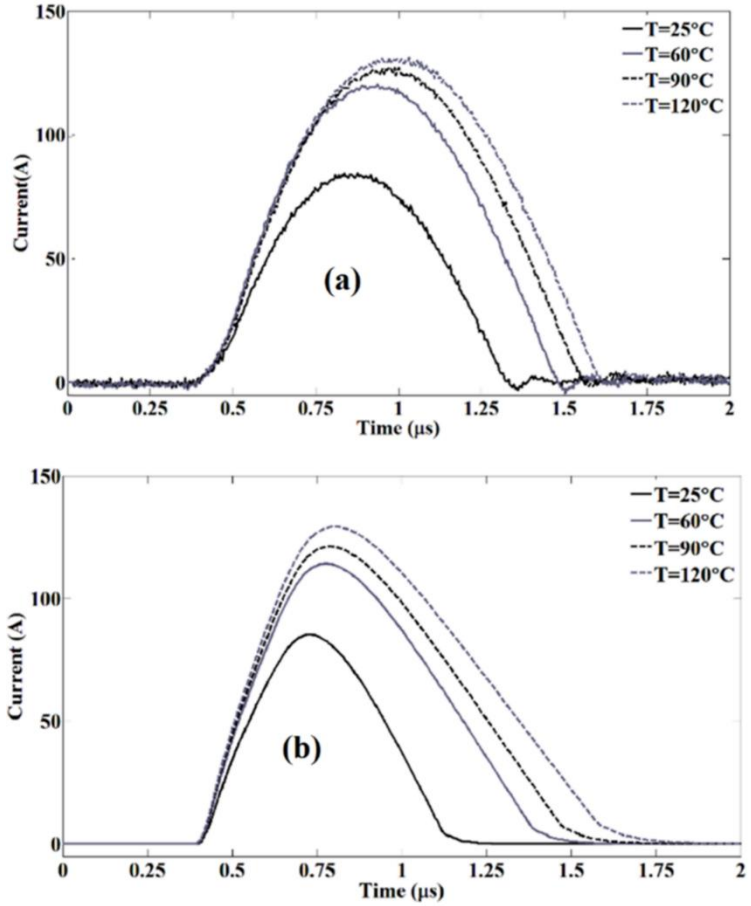


Fig. 5.15 Shoot-through current at different temperature; (a) Experimental result and (b) Simulation results.

Fig. 5.16 shows the V_{CE} voltage waveform obtained from the experiments and the simulation results under the same conditions. The observed *dV/dt* of the IGBT reduces

by increasing the temperature. Moreover, the depletion punch-through is delayed in time due to the increase in the carrier lifetime and reduction of the threshold voltage.

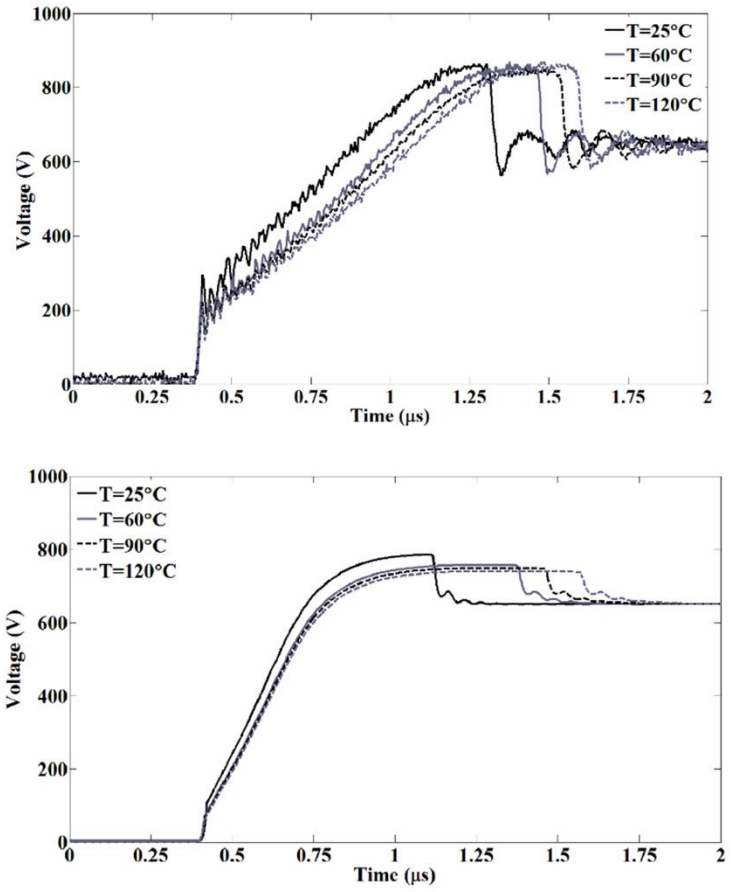


Fig. 5.16 Collector-emitter voltage at different temperature. (a) Experimental result and (b) Simulation results.

Fig. 5.17 shows the gate-emitter voltage waveform of the bottom IGBT at different temperature for the experiment and simulation. As can be seen, the peak voltage increases and due to the shift in the punch-through of the depletion layer in the device, the second peak of the gate voltage is delayed in time similar to Fig. 5.16.

As explained earlier, the short circuit happening at the leg of the inverter causes a large power dissipation to occur on the devices and this can be a hazard in the operation of the inverter. To quantify this power loss, the current and voltage waveform are shown on the same graph in Fig. 5.18.

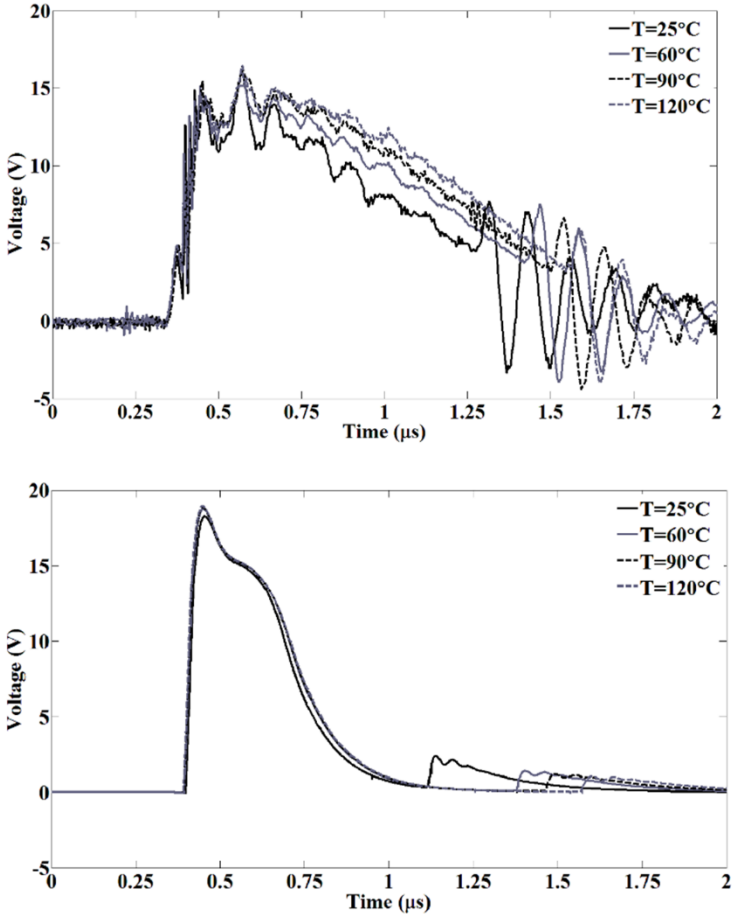


Fig. 5.17 Gate-emitter voltage at different temperature. (a) Experimental result and (b) Simulation results.

As can be seen, the power dissipation for this experiment where the bottom side gate resistance is higher than the top device, the shoot-through current increases significantly and there is an approximate 60 kW power loss in a period of 1 μs across

the bottom side device. By having a repetitive switching of the device, this creates a very high power loss which increases the temperature of the device in less than a minute and may cause the device to get destroyed.

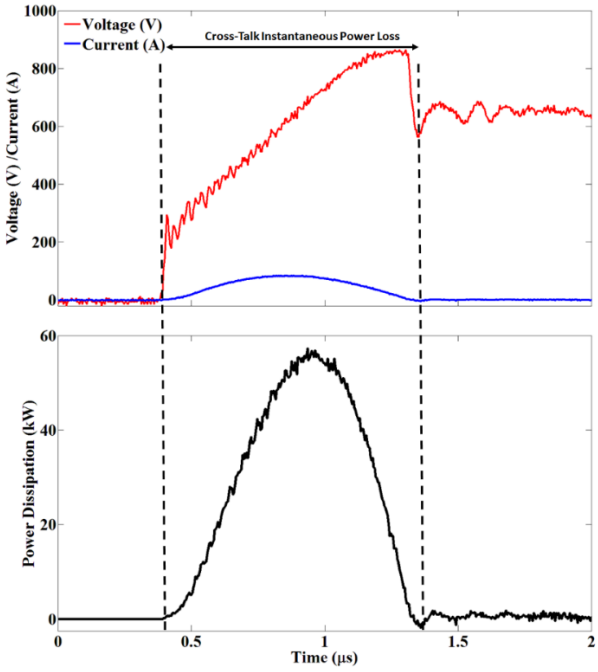


Fig. 5.18 Experimental result showing shoot-through current and voltage and switching power dissipation.

The model has been tested to calculate the power losses due to the cross-talk phenomenon on the bottom side switch at different temperatures. The results are shown in Fig. 5.19. As can be seen, the power losses increases significantly by increasing the temperature.

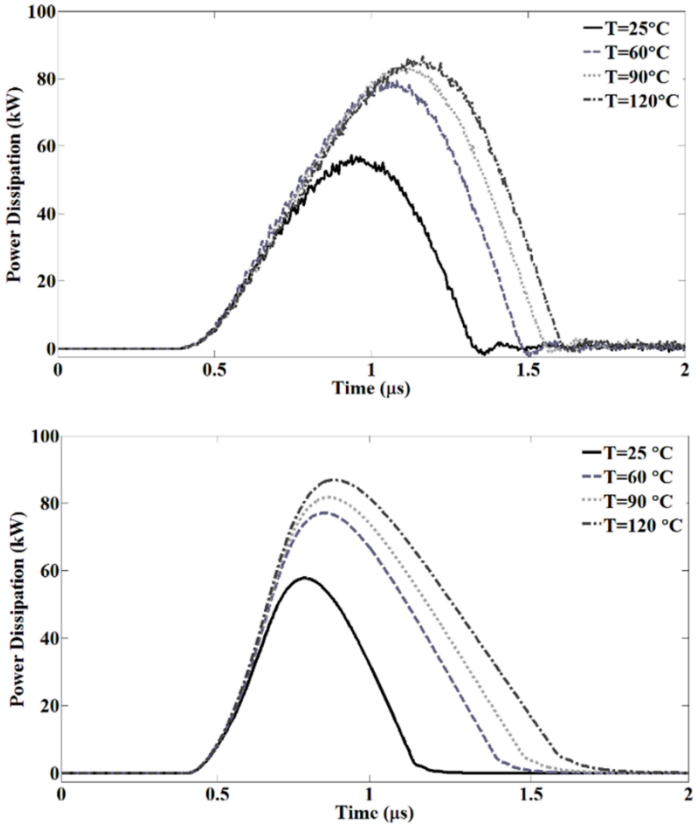


Fig. 5.19 Shoot-through switching power dissipation in (a) experiments and (b) simulation.

Fig. 5.20 illustrates the energy loss across the device for different temperatures and compares the experimental results with the simulation results obtained from the accurate physics-based device model. As can be seen, the energy losses almost becomes double when the temperature of the device is increased from 25°C to 120°C.

One way to mitigate this phenomenon is to apply a negative gate voltage as the off-state voltage level. The model is capable of predicting the behaviour of the inverter when a negative voltage is applied as an off-state voltage for the IGBTs using a bipolar

gate drive. The peak of the shoot-through current can be reduced significantly by using this mitigation method.

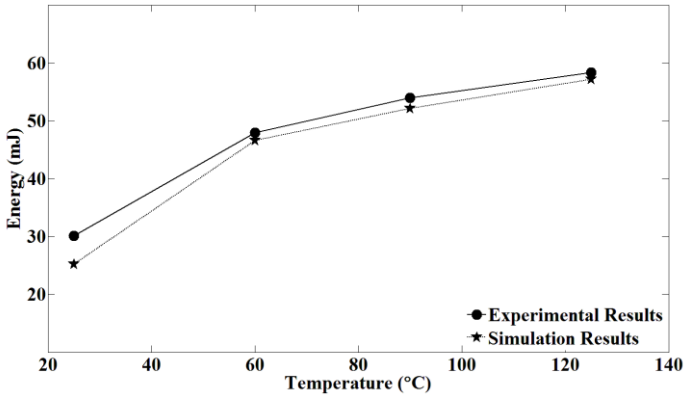


Fig. 5.20 Shoot-through switching power dissipation comparison between experiments and simulation.

Fig. 5.21 shows the simulation results using the negative gate voltage. In this study, the off-state of the gate driver is set to be -5 V and the on state remains as 18 V. As can be seen, the peak of the shoot-through approximately reduced by an order of magnitude in comparison to the time when 0 V were used as the off-state voltage (unipolar gate drive). This is due to the fact that the negative gate voltage increases the margin between the off-state and the threshold voltage of the IGBT.

Fig. 5.21 (a) shows the shoot-through current under the above condition. The duration of the short circuit is reduced using this mitigation method and the peak of the current is reduced to approximately 8A at room temperature in comparison to Fig. 5.15 which is about 80A at the same temperature.

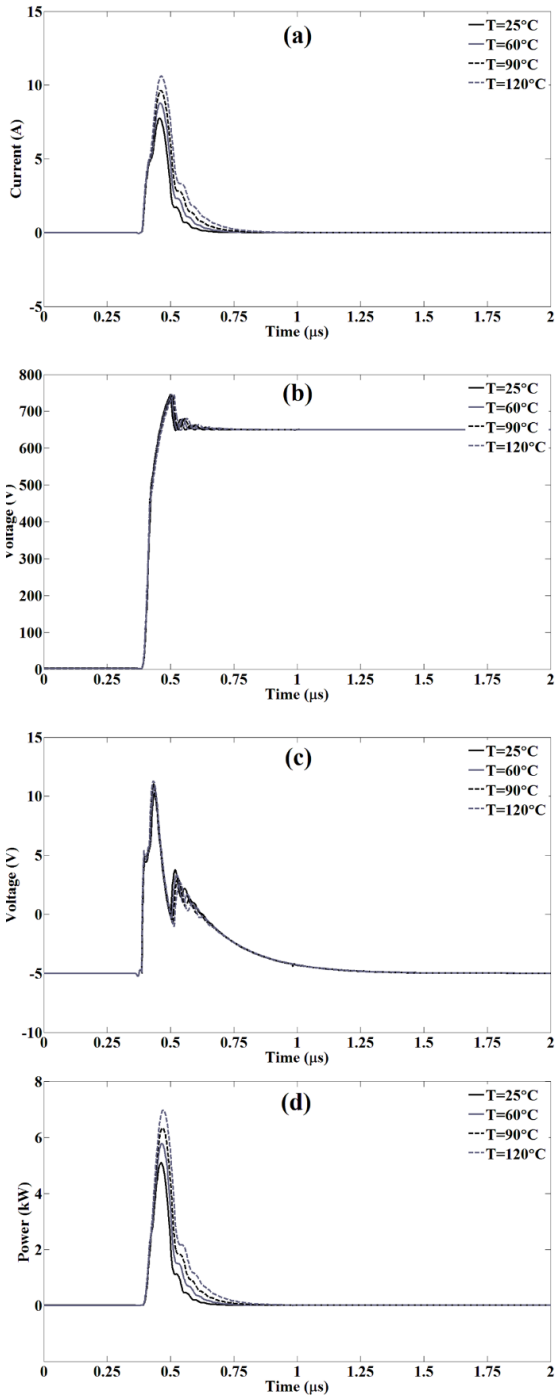


Fig. 5.21 Simulation result showing (a) shoot through current (b) collector-emitter voltage (c) gate-emitter voltage (d) power losses due to cross-talk for a single switching event for different temperatures.

The power dissipated in the device parasitically turned on using the bipolar gate drive reduced to approximately 5 kW at room temperature in comparison to Fig. 5.19 which peaks at almost 10 times larger value. Although the power losses in this case are significantly smaller, however it is still capable of increasing the junction temperature of the device.

The simulation results shown in Fig. 5.21 can be validated using the experimental results shown in Fig. 5.22. Fig. 5.22 compares the shoot-through current of the device at room temperature using the same gate resistors as in the simulation. As can be seen, the bipolar gate drive reduces the shoot-through current by the factor of 10 at the room temperature. Fig. 5.23 shows the calculated peak power dissipated due to cross-talk as a function of the negative gate bias. This plot is important in determining the magnitude of the negative bias required to completely eliminate cross-talk in the converter. It is important to minimize the magnitude of the negative bias on the IGBT gate in the off-state because negative bias is stressful to oxide integrity. Negative bias causes positive fixed oxide charge trapping which can cause threshold voltage drift and other long term reliability issues regarding gate dielectric integrity.

Although good IGBTs are now designed with negative gate voltage capability, the model presented in this paper is capable of optimizing the magnitude of negative bias given the switching rates and ambient temperatures. Another mitigation method is adding a bypass MOSFET to the gate to remove the current path that can pass through the gate resistor.

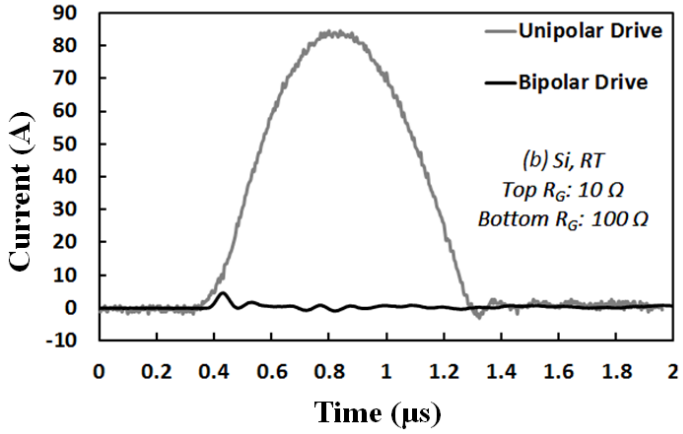


Fig. 5.22 Experimental result showing the comparison between the shoot-through current using unipolar gate drive and bipolar gate drive.

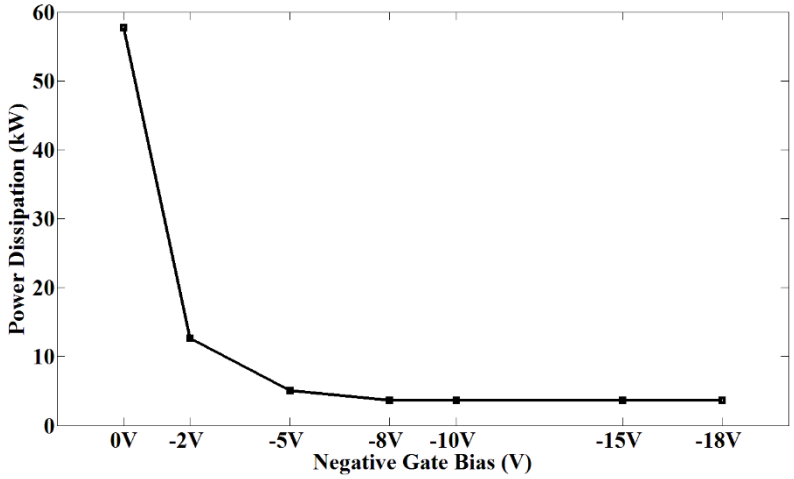


Fig. 5.23 Simulation result showing the peak power dissipation as a function of negative gate voltage at room temperature for 10Ω gate resistance at the top switch and 100Ω gate resistance at the bottom switch.

5.3 Parasitic Gate Turn-Off

This section investigates another parasitic induced gate switching phenomenon which predominantly happen in the SiC MOSFET switching devices. As the power MOSFETs are interesting area of research in automotive industry and they are a

candidate for replacing IGBTs, this reliability aspect of the devices are investigated in this section. This phenomenon is parasitic gate turn-off which happens when a MOSFET is switched with an anti-parallel PiN diode. This PiN diode can be an external SiC PiN diode, the MOSFET body diode or silicon-based PiN diode. In this section in order to amplify the impact and study all the aspects of this reliability, the MOSFET is switched with a discrete PiN diode. In Chapter 7, it is shown that this phenomenon can happen with the SiC MOSFET body diode and a discrete 3.3 kV SiC PiN diode fabricated at Warwick. PiN diodes are very important power electronics components used for rectification in power converters. PiN diodes are able to deliver low conduction losses because of conductivity modulation which results from its bipolar characteristics.

The on-state resistance of the voltage blocking drift region is reduced by creating a minority carrier plasma. However, the disadvantage is based on the fact that the minority carriers must be evacuated from the drift region before the diode can be turned-off. This increases the switching losses of the PiN diode, hence, not making it suitable for high frequency applications. This charge evacuation results in the reverse recovery characteristic which is comprised of a negative current. Because the peak of this reverse recovery current occurs at the same time the diode is blocking the supply voltage (V_{DC}), there is very high instantaneous power dissipation. Also, since the reverse recovery current of the PiN diode manifests itself in the MOSFET as turn-on current overshoot, reverse recovery also stresses the complementing transistor.

The other problems associated with PiN diodes are the potentially destructive consequences that can result with high current commutation rates (dI/dt) under hard

switching conditions. It is well known that increasing the turn-off rate of the PiN diode increases the peak reverse recovery current thereby making the diode turn-off snappy with potentially destructive consequences in the presence of parasitic inductances. One of these destructive manifestations is parasitic gate turn-off of the complementing transistor leading to thermal destruction via uncontrolled switching of the transistor and diodes. In the next section, this phenomenon is explained explicitly and in the coming sections the experimental set-up used to capture the parasitic gate turn-off and the measurement results used to characterise the oscillations between the high side diode and the low side SiC MOSFET transistors are shown and discussed. Later on, the physics-based model used to simulate this phenomenon is investigated.

5.3.1 Reverse Recovery Induced Parasitic Gate Turn-Off

In a classic clamped inductive switching circuit, a low side transistor and a high side PiN diodes are connected and a double pulse test was carried out. Fig. 5.24 shows the clamped inductive switching circuit with all the parasitic components. The switching behaviour of both devices can be investigated under this test. The current waveform of a PiN diode has two distinct slopes which are referred to as positive and negative *dI/dt*. The hard commutation of the current from the freewheeling top-side diode to the bottom-side SiC MOSFET transistor affects the negative and positive slopes. The negative slope is controlled by the switching rate of the transistor and the amount of voltage across the stray inductance of the bottom side transistor. During the reverse recovery of the PiN diode, a depletion region forms inside the diode and this

brings about a negative blocking voltage across the device. At the same time, the MOSFET voltage drops down as the gate voltage rises up and the current starts rising in the MOSFET. This voltage drop coupled with the stray inductance of the MOSFET, reduces the *dI/dt* of the transistor until it reaches the peak overshoot current. At this time, the diode reaches the peak of the reverse recovery current. As the high side PiN diode is turned off and goes into reverse recovery, the *dI/dt* of the current overshoot in the low side transistor can cause significant voltage rise across the source inductance *Ls*. This source voltage overshoot reduces the effective gate-source voltage driving the transistor and can result in unintentional/parasitic gate turn-off of the transistor if it becomes larger than the difference between the gate drive voltage and the threshold voltage.

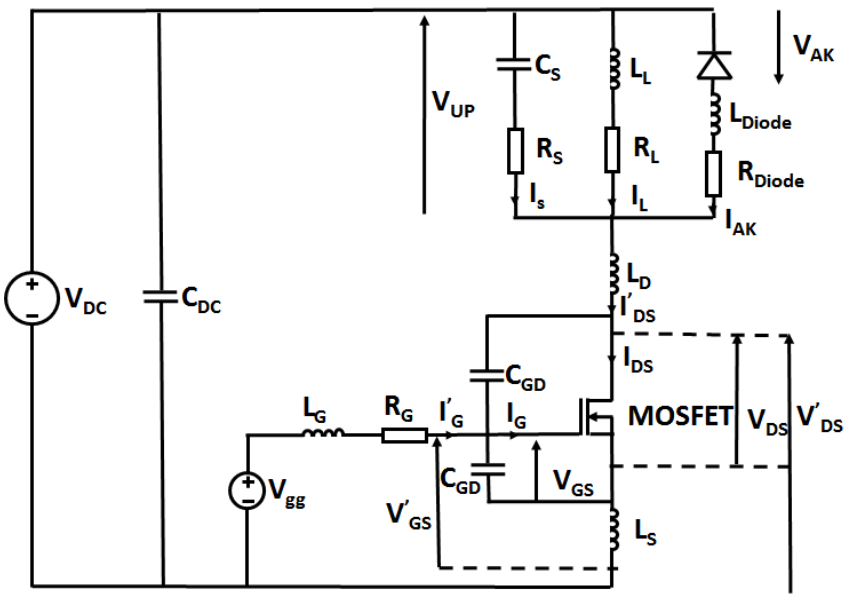


Fig. 5.24 Clamped inductive switching circuit compromising with a top side PiN diode and bottom side SiC MOSFET with all the parasitic components used to investigate the parasitic gate turn-off.

The negative slope of the current before the peak reverse recovery (I_{RR}) is the negative $\frac{dI^-}{dt}$ which is due to the recovery of the stored charge in the drift region of the PiN diode. The positive *dI/dt* which happens after the I_{RR} and is due to the recombination of the remaining minority carrier concentration in the drift region of the diode is referred to as$\frac{dI^+}{dt}$. This rate is determined by the Shockley-Read-Hall recombination rate of the carriers in the drift region. When the remaining charge is recombined and the diode current returns to zero, the device capacitance reduces.

In case of the hyper fast recovery diode, the carrier lifetime in the drift region of the diode is modified in order to reduce the reverse recovery and the diode is highly doped. This causes the depletion layer at both ends of the diode to meet in the drift region and hence the diode becomes snappy. The snappiness of the diode coupled with the stray inductance can bring the voltage of the diode back to zero and at this point the diode starts conducting and the MOSFET switches-off. This change of current coupled with the source inductance can bring down the gate-source voltage and switch-off the unintentionally.

Since the commutation rate of the reverse recovery current increases with temperature, the switching rate and the supply voltage, the probability of parasitic gate turn-off increases for high power converters driven at high temperatures and high switching rates.

As the transistor is parasitically turned-off and current commutates back to the diode, the process repeats itself as the diode re-enters reverse recovery. This process

can continue either until the oscillations are damped or until thermal runaway occurs depending on the ambient/junction temperature. Furthermore, the voltage overshoot in the parasitic MOSFET turn-Off can exceed the breakdown voltage depending on the drain inductance and *dI/dt* of the diode turn-on current. Fig. 5.25 shows the measured oscillations of a PiN diode at different temperatures showing subsequent parasitic diode turn-on (which is MOSFET turn-off).

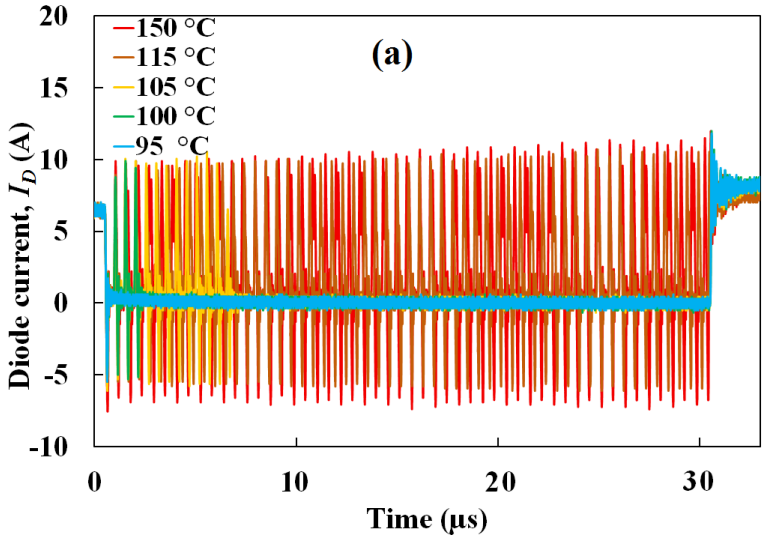


Fig. 5.25 Zoomed in view of the parasitic gate turn-off at different junction temperatures.

As can be seen in this figure, the duration of the oscillations due to the parasitic gate turn-off is increasing with the junction temperature and it damps down as the junction temperature is lower. Hence, it can be deduced that the junction temperature is one of the conditions which can trigger this phenomenon by providing suitable recombination rate of carriers for the diode. This coupled with the parasitic inductances can bring the gate voltage of the MOSFET to below the threshold voltage. Fig. 5.26

shows a zoomed-in view of the oscillations in the current due to the parasitic gate turn-off. Next, the experimental setup was used to characterize this occurrence is discussed.

Fig. 5.27 shows the clamped inductive switching test rig designed to capture the parasitic gate turn-off. The numbering labels in this figure are: (1) high voltage power supply and logic power supply unit, (2) test rig closure, (3) function generator to generate double pulses, (4) current probes amplifiers, (5) Techtronic oscilloscope, (6) temperature reader, (7) DC power supply for heaters, (8) DC link capacitor, (9) current probe, (10) diode, (11) MOSFET, (12) gate driver board, (13) current probe, (14) high voltage differential probe, and (15) inductive load.

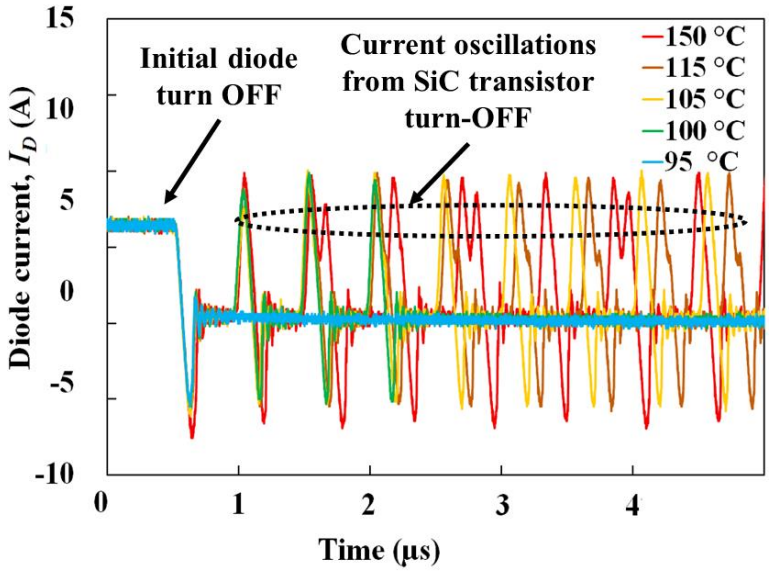


Fig. 5.26 Zoomed in view of the parasitic gate turn-off at different junction temperatures.

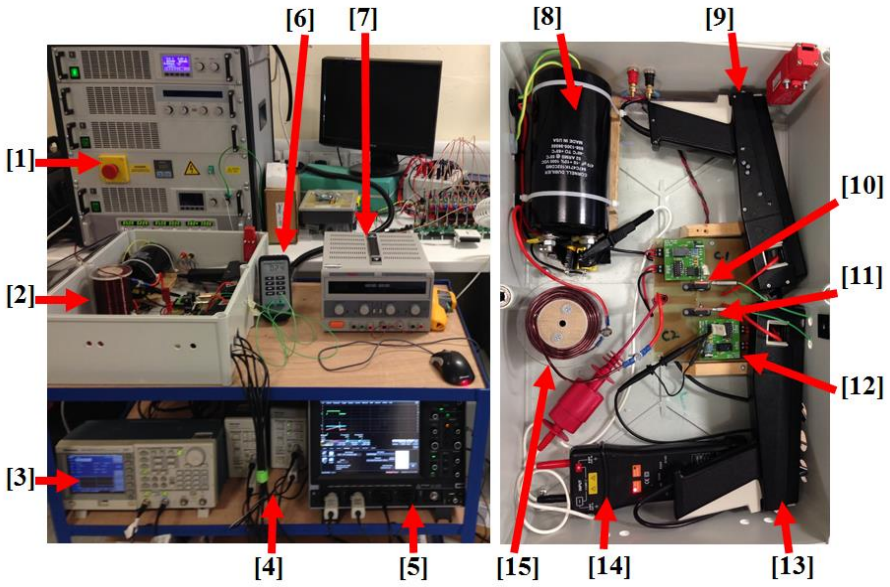


Fig. 5.27 Clamped inductive switching test rig setup.

This test rig was used to capture the switching characteristic of the PiN diode and the SiC MOSFET. During this test two pulses were applied to the gate of the bottom side SiC MOSFET. During the first pulse, the inductive load was charged and during the second pulse the turn-on and turn-off waveform of the device were captured on the oscilloscope. This phenomenon happens when the PiN body diode of the MOSFET is used as the top side freewheeling diode in the clamped inductive switching test. The results showing the parasitic gate turn-off is shown in Chapter 6, when the SiC MOSFET was packaged and the switching characteristic of the MOSFET alongside with the body PiN diode of the device was tested in the clamped inductive switching test. In order to investigate the root cause of this problem and amplify the effect through experiments, a fast recovery Si PiN diode is chosen which exhibits a larger *dI/dt* during the reverse recovery and has a slightly larger reverse recovery. The SiC MOSFET under

test was a 1200V/42A SiC MOSFET from Cree (P/N: CMF20120D) and the fast recovery diode used was an International Rectifier (Infineon) Hyperfast rectifier (P/N: 15ETH06). As mentioned earlier, if the current starts oscillating between the diode and the MOSFET and this oscillation and unintentional turning-off of the SiC MOSFET does not damp down, there is a chance of catastrophic breakdown of the SiC MOSFET due to the very large voltage overshoot and presence of large current during the hard commutation of the current between the two devices. Fig. 5.28 illustrates a device failed inside the test rig and the destroyed device due to the thermal runaway.

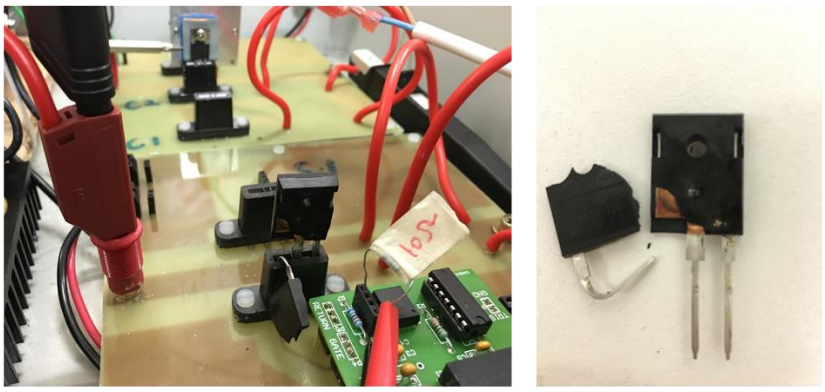


Fig. 5.28 Catastrophic breakdown of SiC MOSFET due to parasitic gate turn-off phenomenon induced by the high recombination rate of the top antiparallel diode.

During these experiments, a hotplate with a heating element was attached to the backside of the freewheeling diode and the temperature of this device was varied to investigate the impact of junction temperature of the diode on the parasitic gate turn-off. Moreover, the switching rate of the SiC MOSFET was varied by changing the gate resistance of the gate driver.

5.3.2 Experimental Results and Discussions

A double pulse test was used to assess the switching of the devices. Fig. 5.29 shows the experimental measurements with the diode junction temperature set at 25°C and 50°C. The measurements were performed with 10Ω gate resistance on the low side SiC MOSFET, 400V DC voltage supply and the length of the pulse was adjusted to provide 30A forward current through the diode. Fig. 5.29 (a) shows the SiC MOSFET gate-source voltage as it switches on, Fig. 5.29 (b) shows the reverse recovery current of the diode as it switches off and Fig. 5.29 (c) shows the turn-off drain-source voltage waveform of the low side SiC MOSFET. It can be observed that the characteristics measured at 50°C exhibits parasitic gate turn-off whereby V_{GS} falls back to zero thereby forcing current back to the diode and the V_{DS} across the SiC MOSFET experiences a large overshoot voltage as high as 800V.

As can be seen from Fig. 5.29 (b), the peak of the reverse recovery current waveform was slightly increased as the temperature was increased, hence, the recombination rate (the positive slope of the current waveform) was also increased. The parasitic gate turn-off happens due to the high positive dI/dt of the PiN diode coupled with the stray inductance of the circuit which causes a source voltage to rise beyond (V_{GG}-V_{th}) where V_{GG} is the gate driver voltage at on-state and V_{th} is the SiC MOSFET threshold voltage. As the channel is turned-off, the time derivative of the drain-source voltage of the transistor (dV_{DS}/dt) seen in Fig. 5.29 (c) coupled with the Miller capacitance of the SiC MOSFET induces a negative current at the gate of the SiC

MOSFET. This current multiplied in the gate resistance, creates a negative dV_{GS}/dt at the gate of the device. Consequently, the gate turns off parasitically and causes the current to start flowing into the PiN diode.

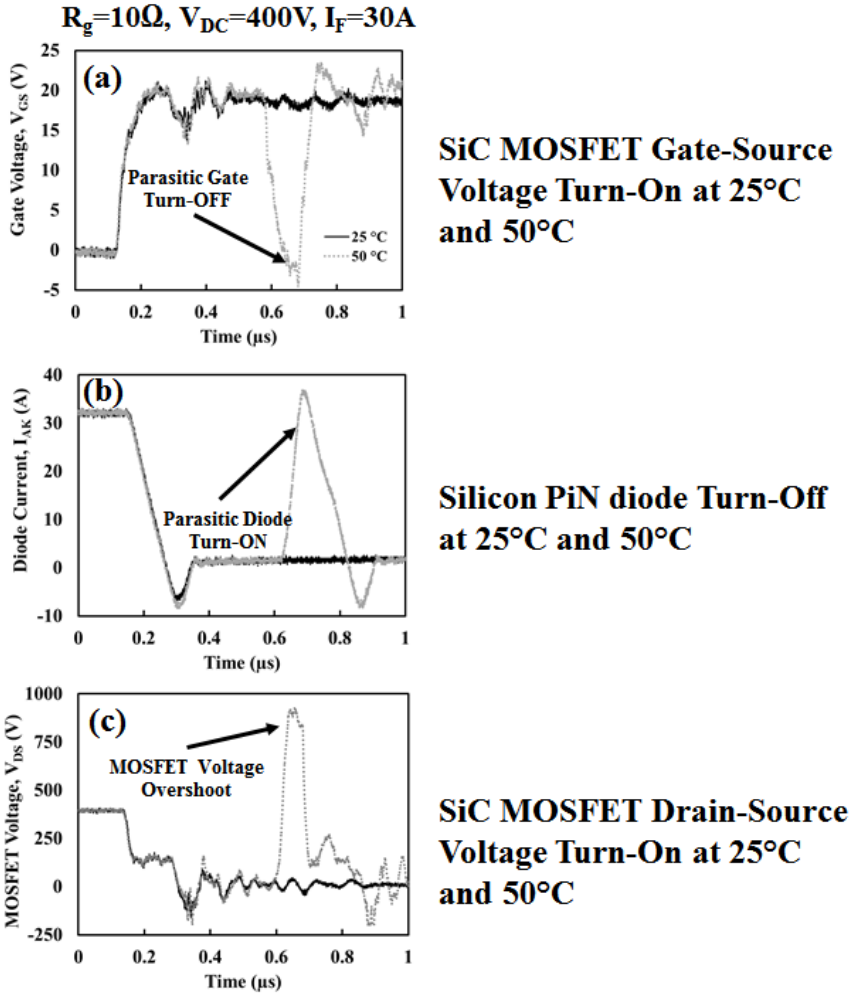


Fig. 5.29 (a) SiC MOSFET gate-source voltage during turn-on (b) Silicon PiN diode turn-off (c) SiC MOSFET drain-source voltage turn-on waveform at 25°C and 50°C.

As can be seen from Fig. 5.29, the instantaneous power dissipation in the SiC MOSFET is very large during the parasitic gate turn-off. Consequently, as shown previously, if the positive *dI/dt* is large enough to trigger the oscillations in the gate and the conditions do not allow damping in the oscillations, then catastrophic breakdown of the SiC MOSFET can occur due to thermal runaway.

By carrying out numerous experiment under different conditions, the main parameters which are capable of triggering the parasitic gate turn-off were discovered and the impact of changing these parameters were investigated through experimental measurements. All these parameters have direct impact on the positive recombination slope of the diode's current. These parameters are:

1. Junction temperature of the PiN diode
2. Forward current passing through the diode
3. DC link voltage supply
4. Switching rate of the bottom SiC MOSFET which can be adjusted by changing the gate resistance of the bottom side SiC MOSFET.

Fig. 5.30 (a) and (b) are experimental results showing the impact of the switching rate of SiC MOSFET on the reverse recovery of the freewheeling diode and the impact of the junction temperature of the PiN diode respectively. As can be seen: (a) The peak reverse recovery current increases with (i) temperature (ii) switching rate. (b) The positive current slope increases with (i) increasing temperature (ii) increasing switching speed.

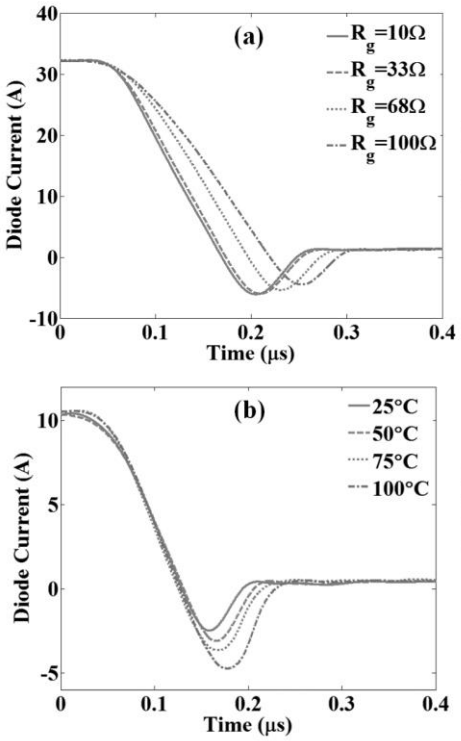


Fig. 5.30 Reverse recovery waveform of the PiN diode during turn off for (a) different MOSFET switching rates (b) different diode junction temperatures.

Fig. 5.31 shows the impact of supply voltage on the parasitic gate turn-off by changing the DC voltage from 100V to 300V. As can be seen from the parasitic gate turn-of of the low side SiC MOSFET occurs at 300V but not at 100V supply voltage. This is due to the fact that the peak reverse recovery current as well as the snappiness of the positive slope recombination current increases with the supply voltage.

This is due to the fact that increasing the supply voltage increases the depletion width during the diode turn-off, thereby, causing higher recombination currents. Also, the negative *dI/dt* during diode turn-off increases with the supply voltage because the internal electric field at the PN and N^-N^+ junctions are higher and form faster. The

voltage overshoot in Fig. 5.31 (c) due to parasitic diode turn-on (MOSFET turn-off) is a significant reliability concern.

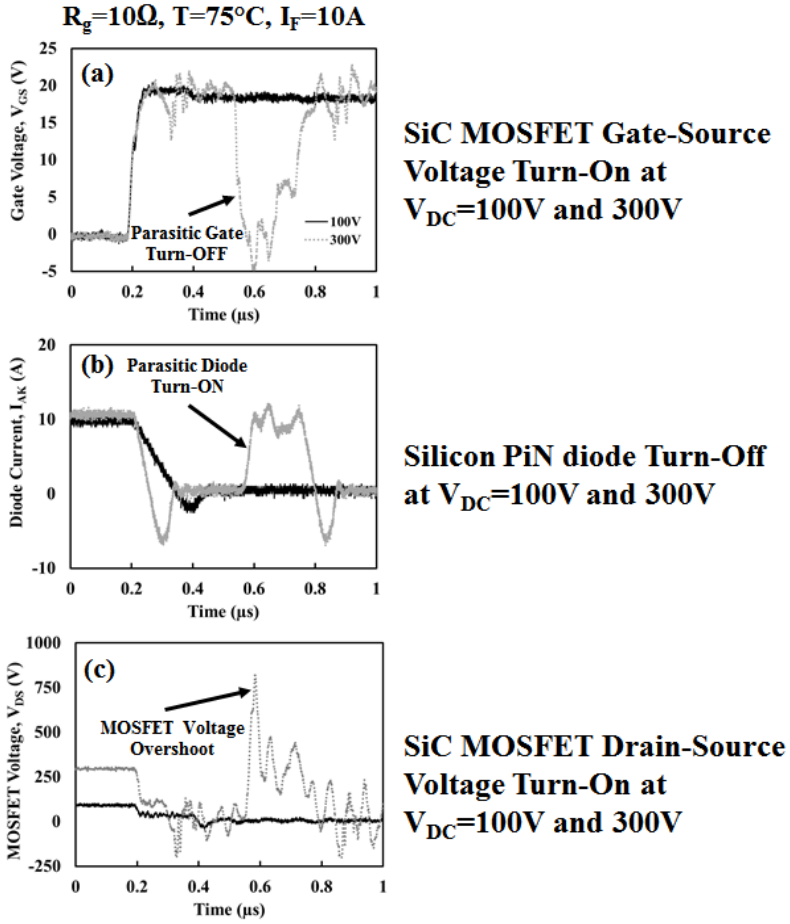


Fig. 5.31 (a) SiC MOSFET gate-source voltage during turn-on (b) Silicon PiN diode turn-off (c) SiC MOSFET drain-source voltage turn-on waveform at V_{DC}=100V and 300V.

Other measurements performed with different diode forward currents. Increasing the gate-source current increases the probability of this phenomenon.

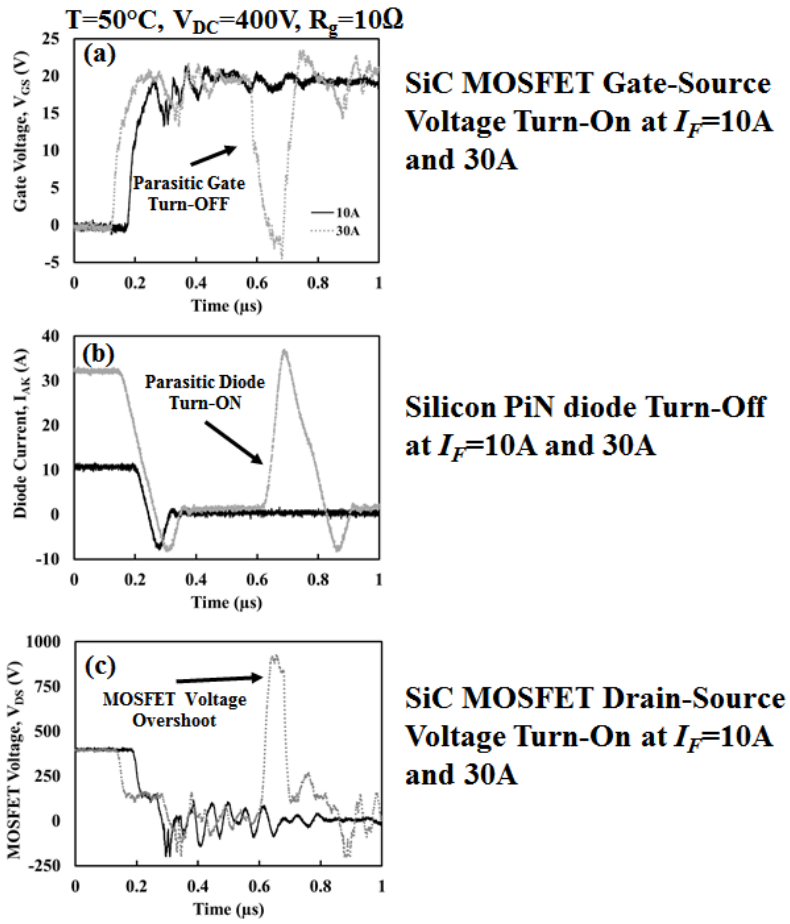


Fig. 5.32 (a) SiC MOSFET gate-source voltage during turn-on (b) Silicon PiN diode turn-off (c) SiC MOSFET drain-source voltage turn-on waveform at I_F=10A and 30A.

Similarly, Fig. 5.33 shows occurrence of this phenomenon caused by switching at higher rates by varying the gate resistance from 100Ω to 10Ω respectively. This is due to the fact that when the gate resistance becomes smaller, the SiC MOSFET switches on faster and consequently, the negative slope of the current waveform becomes steeper. The critical parameter that determines the occurrence of this destructive failure mode is the snappiness of the recombination current through the diode which can be quantified by the recombination *dI/dt*. This recombination current has been measured as a function of the forward current, gate resistance, junction temperature of

the diode and the supply DC voltage. The results are shown in Fig. 5.34 (a) to Fig. 5.34 (d).

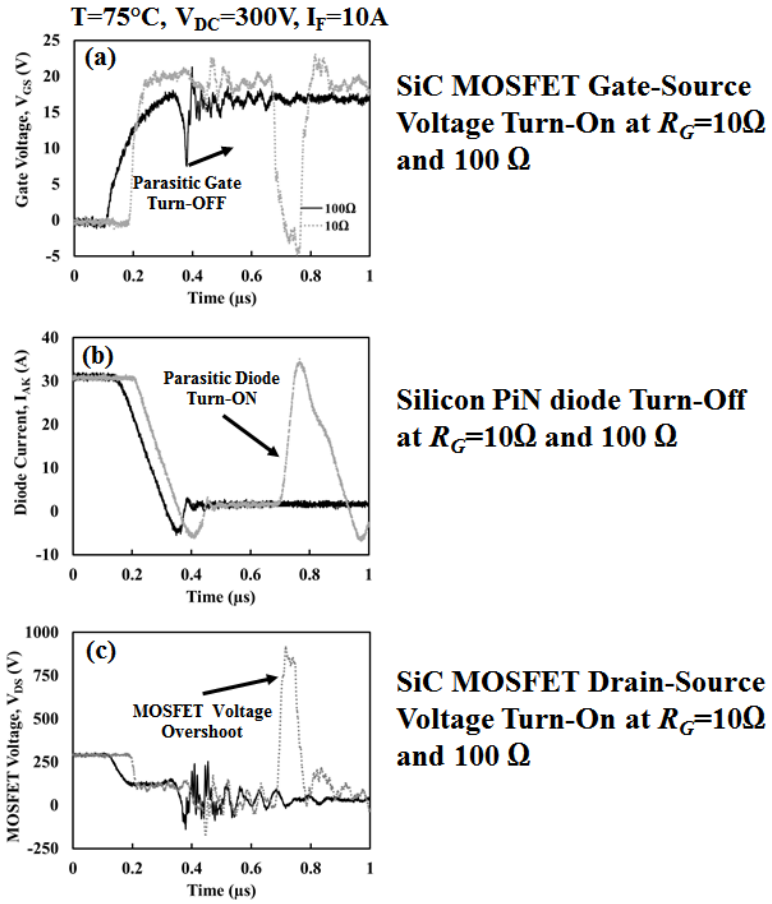


Fig. 5.33 (a) SiC MOSFET gate-source voltage during turn-on (b) Silicon PiN diode turn-off (c) SiC MOSFET drain-source voltage turn-on waveform at R_G=10Ω and 100Ω.

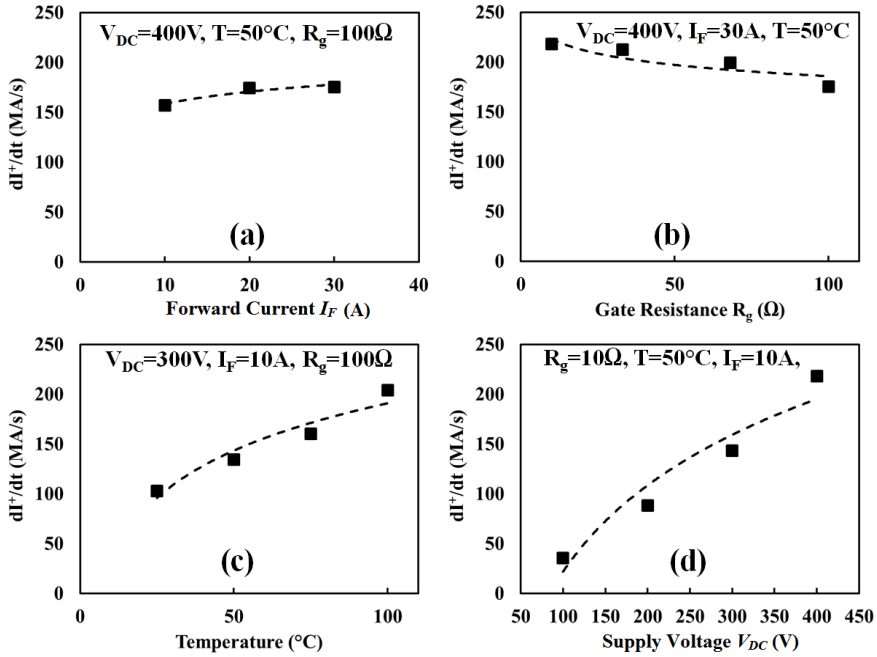


Fig. 5.34 The recombination *dI/dt* as a function of (a) Forward current, (b) Gate resistance, (c) Junction temperature and (d) The supply voltage.

A more comprehensive results showing the impact of these four parameters on the positive and negative slopes of the current during the reverse recovery is presented using color-codes in Fig. 5.35 and Fig. 5.36. In these two figures, the blank spaces indicate that the devices went under thermal runaway and catastrophic breakdown occurred.

Fig. 5.35 The impact of forward current, DC voltage, switching rate and temperature on the positive *dI/dt* during the reverse recovery.

Fig. 5.36 The impact of forward current, DC voltage, switching rate and temperature on the negative *dI/dt* during the reverse recovery.

5.3.3 Modelling Parasitic Gate Turn-off

Fig. 5.37 summarises the SiC MOSFET model equations in a block diagram.

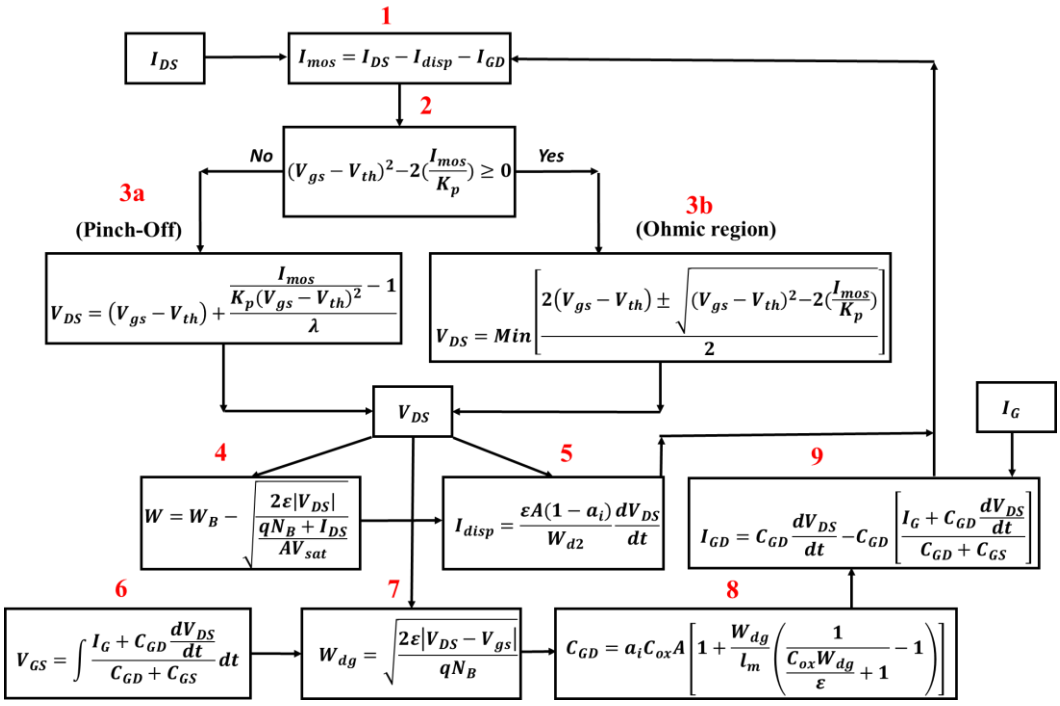


Fig. 5.37 SiC MOSFET model block diagram and physics-based equations.

Both SiC MOSFET and PiN diode models are used in a clamped inductive switching circuit shown in Fig. 5.24 and by solving Kirchhoff's voltage and current laws, circuit equations are obtained and shown in Appendix D.

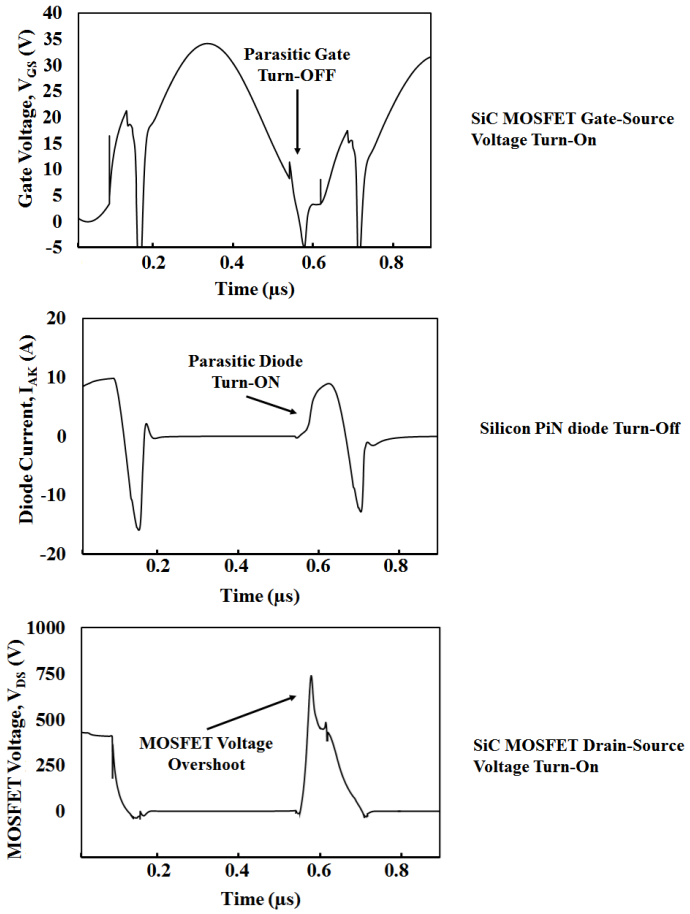


Fig. 5.38 Simulation results showing parasitic gate turn-off (a) Gate-source turn-on voltage waveform, (b) PiN diode turn-off current waveform, (c) MOSFET drain-source turn-on voltage.

Results of the MOSFET and diode models are shown in Fig. 5.38 where the experimental measurements have been used to calibrate the model and the parasitic gate turn-off has been emulated. As can be seen the device switches off and the diode starts conducting again. Moreover, due to presence of all the parasitic inductances and the accurate modelling of the voltage dependent Miller capacitance, the model is able to predict the overshoot voltage of the SiC MOSFET during this phenomenon.

5.4 Conclusions

A physics-based model has been used to accurately model the parasitic turn-on of an IGBT in voltage source inverters. This has been presented with experimental results. The model shows the nonlinear behaviour of the Miller capacitance to accurately model the two slopes of the voltage waveform during the cross-talk. This Miller capacitance is a series connection of two capacitors: fixed oxide capacitor and variable voltage dependent depletion capacitor. Moreover, the results obtained from the model has been compared with the SPICE mode. The model takes the effect of temperature on the device parameters into account; such as threshold voltage, carrier mobility, MOS transconductance and carrier lifetime in the drift region. The results show that increase in temperature can significantly increase the power dissipation. This is caused by the reduction of the threshold voltage of the device.

The shoot through current increases with the temperature due to the reduction of the threshold voltage. The collector-emitter voltage is shifted and becomes longer due to the increase in the carrier lifetime with temperature. Also, the *dV/dt* reduces with the temperature which is the case for the IGBT. The Miller capacitance in the proposed model consists of an oxide capacitor and a depletion capacitor which varies with voltage. This physics-based model can accurately predict current and voltage transients as opposed to compact models that use lumped parameters.

It was demonstrated that the power losses due to the parasitic turn-on of IGBTs in a voltage source inverter is capable of increasing the junction temperature of the device significantly. Hence, the model is very useful in predicting the behaviour of the device at different conditions such as temperature, gate resistance or physical device parameters such as gate oxide thickness, ratio of intercell area to active die area etc. Moreover, it was discussed that this effect can be reduced by applying negative gate voltage which can increase the margin between the off-state and the threshold voltage of the transistor. However, this method is less effective at higher temperatures where *dV/dt* across the device is high enough to trigger the gate-emitter of the device. The same method and technique can be used in case of a voltage source inverter based on SiC power MOSFETs. In the case of SiC MOSFETs, the threshold voltage of the device is significantly smaller than that of Si IGBTs. Moreover, the gate of these devices cannot withstand large negative voltage in comparison with the Si IGBTs. Consequently, it is even more important for power electronics engineers to be able to predict the shoot-through current as a function of switching rate and temperature.

Moreover, in this chapter, reverse recovery induced parasitic gate turn-off of SiC MOSFET coupled with a complementing top side PiN diode as a freewheeling diode has been investigated experimentally and through modelling. It has been shown that parasitic gate turn-off can have destructive consequences because of the resulting oscillation of current between the diode and the transistor. Four main parameters triggering this phenomenon were investigated through measurements:

1. DC voltage

2. Switching speed
3. Temperature
4. Forward current

It was shown that the critical parameter is the snappiness of the diode recombination current. It was shown that if the conditions are met, the oscillations start and if the conditions allow the parasitic gate turn-off and the resulting oscillations damp-down, then the device will survive this phenomenon. Otherwise, catastrophic breakdown of the SiC MOSFET may happen.

All these parameters and different combination of these conditions were tested experimentally and presented in this chapter. Moreover, an accurate SiC MOSFET model was developed and used to model this phenomenon. It was also discussed that the overshoot voltage of the SiC MOSFET during the parasitic turn-off and the voltage oscillations arising from this phenomenon, is a significant reliability concern for the high performance SiC MOSFETs.

Chapter

6 Current Sharing of Parallel IGBTs

6.1 Introduction

For high current applications, silicon IGBTs are normally connected in parallel to deliver the required current ratings [85-87]. The devices are normally designed to have identical electro-thermal parameters for equal current and power sharing. However, over the mission profile of the device, non-uniform degradation of the electro-thermal properties like wire bond lift-off, solder delamination or gate contact resistance as well as unequal heat extraction from the heatsink, can cause the parallel connected IGBTs to have different electro-thermal properties. In this Chapter, the model developed and described previously will be used to look at this problem. This Chapter is presented in [88].

Fig. 6.1 shows the power module of a (a) Nissan Leaf EV and (b) Infineon wind energy power electronic converter where several parallel dies can be seen. Thus, ensuring synchronised electrical switching and balanced electro-thermal parameters between these parallel devices becomes crucial for high power rated inverters with high current capability. Balanced power dissipation between the parallel connected devices is required for optimal temperature distribution [89, 90]. Some thermal

coupled impedance model and thermal analysis of multi paralleled IGBT dies are presented in [91] however, in this model the influence of different chip temperature on the current sharing between the devices was ignored. Current sharing between the devices depends on the device parameters as well as the circuit parameters such as the gate inductance and gate resistance. Hence, in order to have balanced current sharing between the devices, they all need to switch on and off at the same rate. This is usually achieved by power module designers, however, over the mission profile of the module, it is possible that non-uniform degradation of the device electro-thermal parameters can cause electro-thermal imbalance between the devices.

Common failure modes like solder/die attach voiding and delamination can cause a non-uniform thermal resistance across the die or DBC substrate, meaning that the parallel devices may be subject to different junction temperatures. Other parameter that may vary between the devices include the internal and external gate resistances due to increased gate wire bond contact resistance due to thermo-mechanical stress cycling. These variations in the gate resistance will introduce variations in the switching rate and switching energy. Hence, the two principal parameters under investigation in this chapter are electrical switching rates and the thermal resistance of the device. The electrical switching rate is set by varying the gate resistance of the parallel connected IGBTs which sets the gate charging and hence *dI/dt*. The junction temperature of the device is varied using a hotplate connected to the base of the device.

Using compact models to predict impact of electro-thermal variation on temperature imbalance between the parallel connected IGBTs is a useful tool for reliability analysis and FMEA in the automotive industry. The primary problem is the leakage inductances.

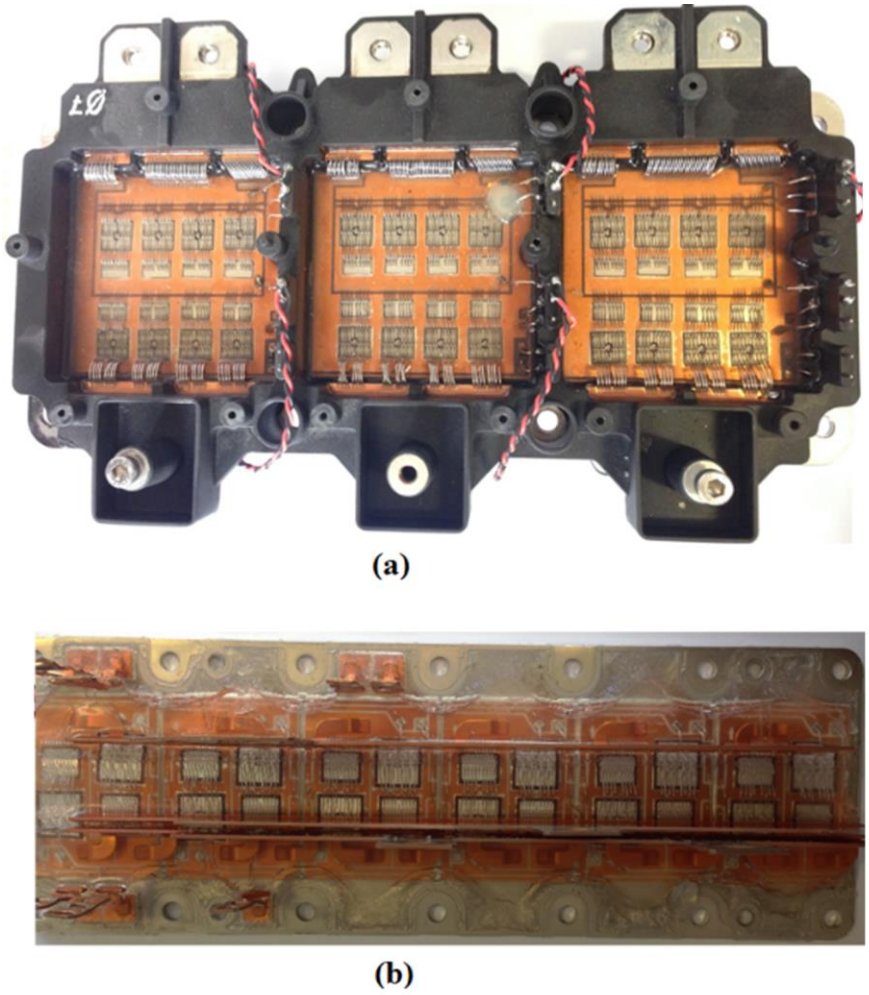


Fig. 6.1 (a) Nissan Leaf power inverter with 4 parallel IGBTs for each top and bottom switches in three phase voltage source converter, (b) Infineon power module (FF1000R17IE4) with 1.7kV/1 kA power rating showing 6 parallel IGBTs with a very long gate path and unbalanced gate resistance and inductance.

In order to understand how the current is shared between the devices it is very important to be able to model the behaviour of two parallel IGBTs working at different temperature or having different gate resistances/switching rates. The IGBT model along with a physics-based PiN diode model explained in Chapter 3 are used in a clamped inductive switching circuit with two parallel IGBTs. The circuit schematic of a clamped inductive switching circuit with two parallel IGBTs is

shown in Fig. 6.2. The Circuit equations are derived by applying Kirchhoff's current and voltage laws (KVL and KCL respectively) on the circuit shown in Fig. 6.2 and are presented in Appendix E.

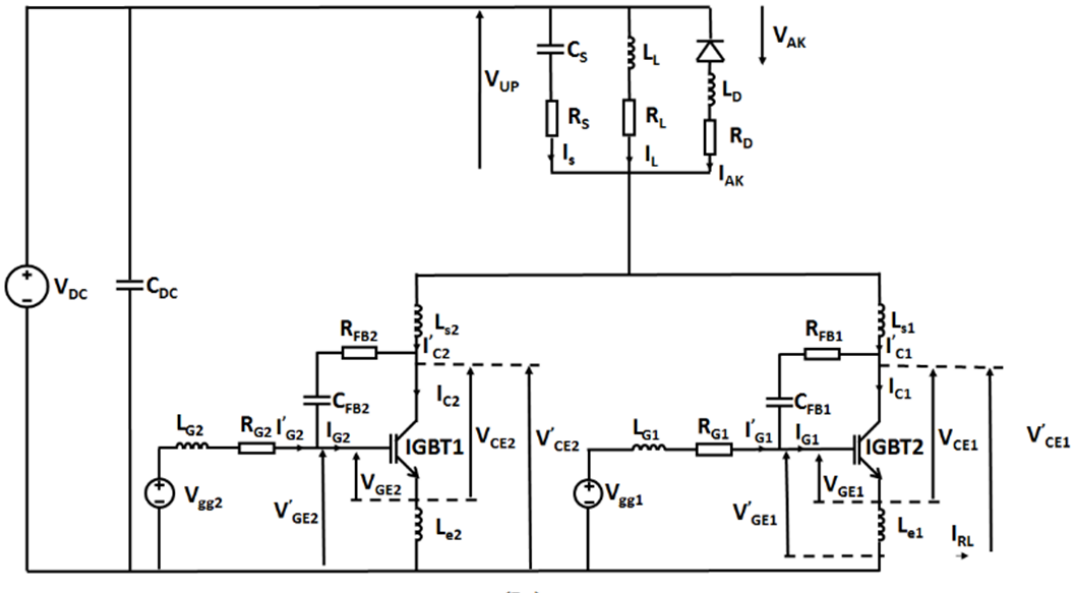


Fig. 6.2 Schematic of the clamped inductive switching circuit with all the parasitic inductances.

As explained in Chapter 2, the schematic shown in Fig. 6.2 is a half bridge configuration which is the basis of common inverters. In this circuit, two pulses are given to the gate of bottom parallel IGBTs. During the first pulse, inductive load is charged and during the second pulse, the switching behaviour of the IGBT and the diode are captured.

To achieve an accurate full electro-thermally coupled model of parallel connecting Si-IGBTs, it is necessary to decouple the electrical switching time constants which occur on the millisecond to second scale. To achieve this, an electro-thermal model that incorporates the physics of the IGBT is used for modelling the instantaneous power

over microseconds to generate the look-up table of losses. Afterwards, a thermal model fed from the look-up table is developed for longer timescale simulations capable of capturing electro-thermal imbalance between the parallel devices.

Fig. 6.3 shows how the model works. The electro-thermal model is comprised of Cauer-thermal network that calculates the transient junction and case temperatures of the devices due to conduction and switching losses. The thermal resistances and thermal capacitances of the Cauer-network are derived based on the dimensions of the TO-247 IGBT package and the thermal properties of the material for each layer. These losses are calculated from the voltage and current waveforms obtained from the IGBT and diode models. The losses have been determined for different switching rates which have been set by using different gate resistances on the low side IGBTs. Hence, electro-thermal imbalance between the parallel IGBTs is simulated simply by using different look-up tables for each IGBT in the thermal model. Once, the look-up table is complete, for different gate resistances and junction temperatures, the purely thermal model takes over and calculates the junction temperature of the parallel IGBTs using Cauer-network and look-up table. The purely thermal model is able to complete simulations lasting several minutes in a computationally effective manner because it does not solve the detailed physics-based ADE equations that have already been pre-solved by the electro-thermal model. Hence, the model is both accurate and computationally efficient. When, there is electro-thermal imbalance between the parallel IGBTs, the respective Cauer-networks take account of the different junction temperatures and updates the

temperature sensitive electrical parameters like the threshold voltage on-state resistance accordingly.

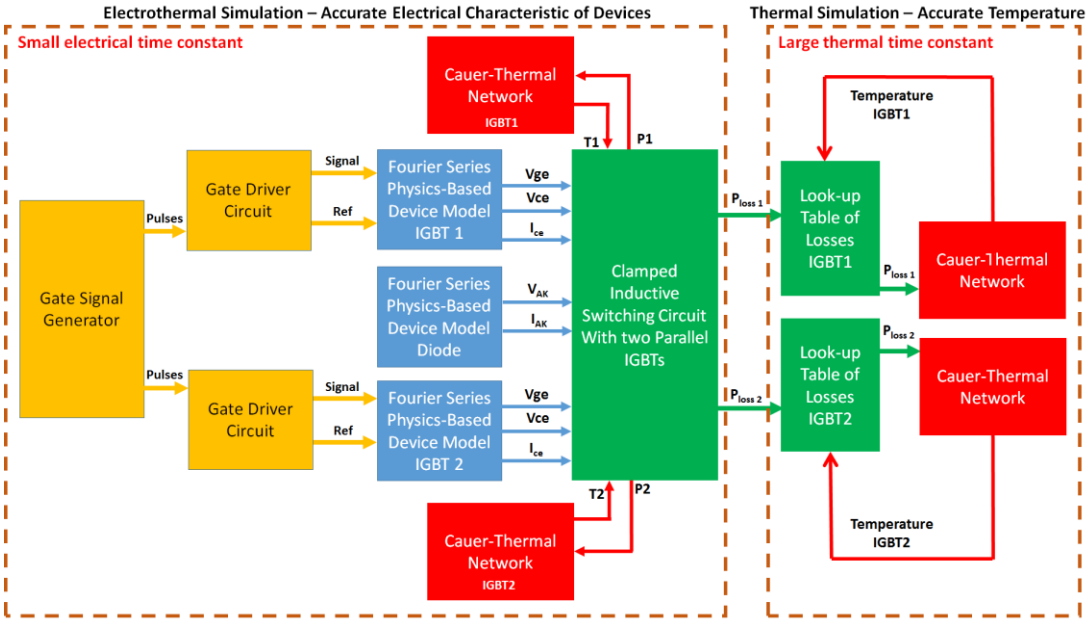


Fig. 6.3 Block diagram of the electro-thermal simulation.

For the electro-thermal simulation, the block diagram shown in Fig. 6.3 is used. The repetitive switching was carried out using fixed frequency pulses with a duty cycle of 10%. A typical power loss transient profile for one period of repetitive clamped inductive switching is shown in Fig. 6.4. In this graph the DC voltage was set to 50V similar to the experimental conditions and the current passing through the device was approximately 6A (12A in total).

The thermal simulation block shown on the right hand side of Fig. 6.3 is used to accurately model the temperature rise in the IGBT due to unbalanced current sharing using the look-up table of losses and two independent Cauer-thermal networks for each switching device when the simulation time is significantly larger than the minimum

simulation time-step of the electro-thermal model. This increases the performance of the simulation and reduces the computational load.

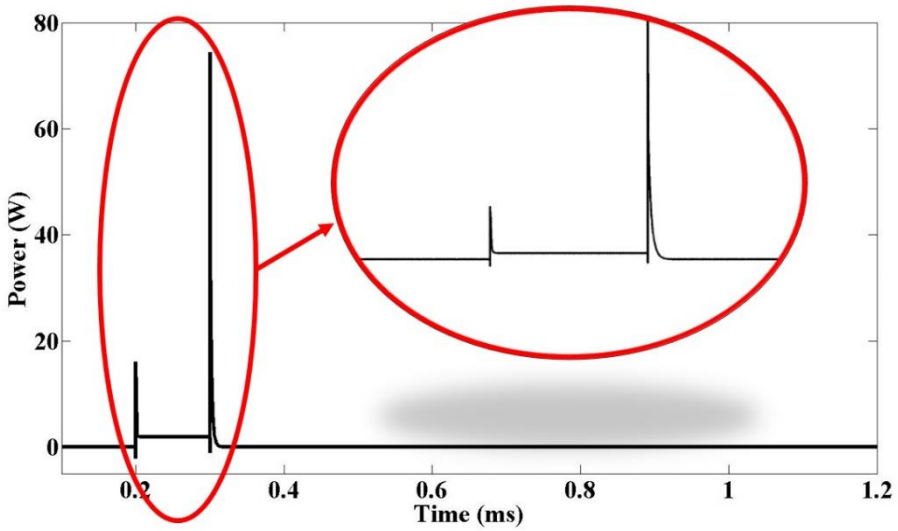


Fig. 6.4 A typical power loss during the repetitive clamped inductive switching for one period with duty cycle of 10%.

As can be seen in Fig. 6.4, the input power to the Cauer-thermal network is a pulse shape that has two overshoots and undershoots at both edges of the pulse. From the graph it can be observed that the turn-off loss for the IGBT is significantly larger than the turn-off loss. This is due to the excess amount of charge stored in the drift region of the IGBT which brings about the current tail of the IGBT. For simplicity, the integration of the power loss during a period, which is the energy loss in one period, was calculated and used in the look-up table of losses. In the thermal simulation, it is assumed that the overshoot and undershoot does not exist and the energy loss consists of the sum of turn-on losses, conduction losses and turn-off losses. This assumption is valid as the thermal time constants ($R_{th} \times C_{th}$) is significantly larger than the electrical time constant (the time that it takes for the device to turn on and off). At the end of

each simulation step, the junction temperature of each device was calculated and fed as an input to the look-up table of losses and a new value of losses was obtained based on the new temperature.

Next, the energy loss corresponding to the junction temperature at the certain gate resistance was divided by the time of the pulse (duty cycle multiplied in the period) and used as the input power to the Cauer-thermal networks. As the temperature rises, the amplitude of the pulse also increases and consequently the input power to the thermal network rises. The graph showing energy loss versus temperature for two scenarios for two IGBTs switching at different gate resistances (R_{G1}=100Ω and R_{G2}=15Ω for scenario 1 and R_{G1}=10Ω and R_{G2}=100Ω for scenario 2) is shown in Fig. 6.5. These differences are chosen to be big to amplify the impact of imbalanced current. However, in Chapter 7 it has been shown that even small differences arising from the DBC layout can lead to imbalanced junction temperatures. As can be seen, the energy loss for scenario 1 are very close and the device switching at R_{G2}=15Ω shows slightly higher losses. However, for the second scenario the energy losses are significantly different. Moreover, comparing scenario 1 and scenario 2, the device with R_{G1}=10Ω has less losses in scenario 2 than in the first scenario. This is further investigated in the Section 6.4.

IGBT devices used during the experiments are International Rectifier/Infineon IGBTs with datasheet reference IRG4PH20KPBF rated at 1.2kV/11A. This IGBT does not have an integrated antiparallel diode, hence all the heat generated in the device is due to the switching and conduction losses of the IGBT die. The dimensions of the device was taken from the device datasheet and the CAD design of the TO-247 package was drawn in Solidworks. The

other reason for choosing a discrete IGBT was to make sure that there is no thermal coupling between the parallel connected devices and the temperature of each device can be adjusted seperately. Fig. 6.6 shows the CAD design of the transistor and the cross section view of the device package. Equation (6.1) and (6.2) which are the same as equations (4.16) and (4.20) were used to derive the thermal resistance and the thermal capacitance of each layer of the Cauer-thermal network.

$$R_{th} = \frac{l}{K_{th} A} \tag{6.1}$$

$$C_{th} = V \rho C_p \tag{6.2}$$

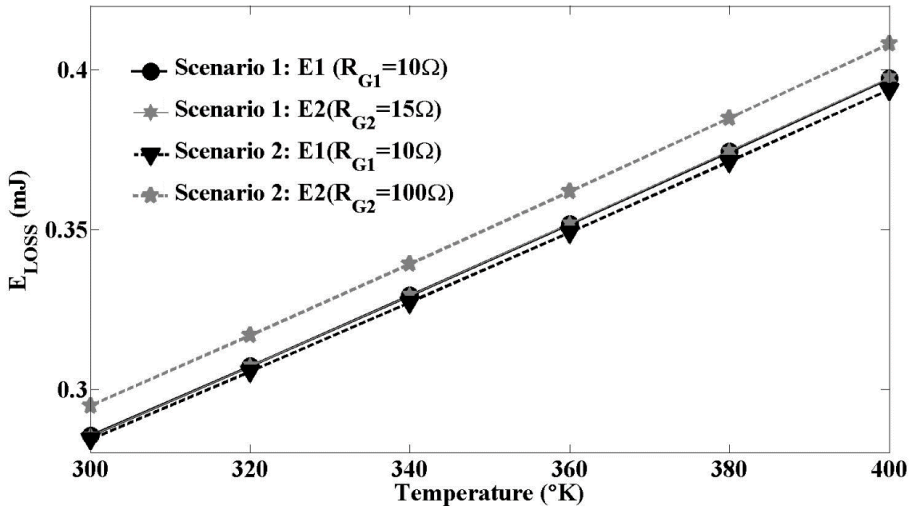


Fig. 6.5 Energy losses for two scenarios - scenario 1: R_{G1}=10Ω and R_{G2}=15Ω and scenario 2: R_{G1}=10Ω and R_{G2}=100Ω.

In these equations, R_{th} and C_{th} are the thermal resistance and capacitance respectively. K_{th} is the thermal conductivity of the material. A is the area of each layer and l represents the thickness of the layer. V represents the volume of each layer and

ρ is the density of the material and C_p is the specific heat of the material. Table 1 shows the parameters used to calculate the thermal conductance and capacitance of each layer of the device. The stack of material used in this type of package are summarised in Fig. 6.6. Table 6.2 shows the thermal parameters calculated for each layer of this graph. These calculated parameters are used in the Cauer-thermal network of the electro-thermal and independent thermal models. In the thermal model, a resistor is added in the last stage of the Cauer-thermal network which determines the heat exchange rate between the ambient temperature (voltage source with the value of 300°K) and the backside of the Cu lead frame.

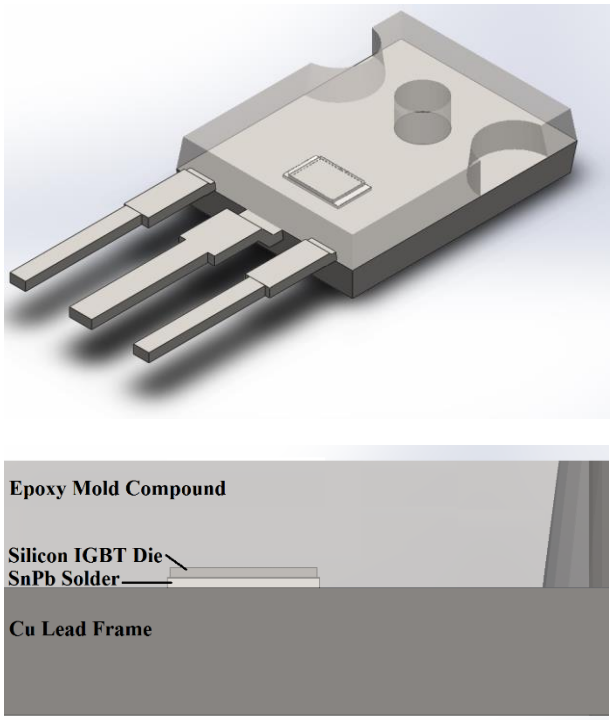


Fig. 6.6 CAD design for the discrete TO247 IGBT package and the cross-section view of the material stack.

6.2 Experimental Setup

The experimental setup used to capture the current and voltage waveforms of the parallel IGBTs is illustrated in Fig. 6.7. The devices under test were discrete IGBTs in TO-247 packages. They were driven using two separate gate drives. Consequently, they could be driven using different gate resistances. As explained earlier, non-uniform degradation of the electro-thermal properties like solder de-lamination or gate contact resistance, can cause the parallel connected IGBTs to have different temperatures or different gate resistances. Two heating elements were mounted on the back side of the two IGBTs and the devices were tested under the condition that they had different junction temperatures. Fig. 6.2 shows the schematic of the test circuit which is also used in the model. As can be seen all the parasitic elements and inductors of the circuit was included in the model.

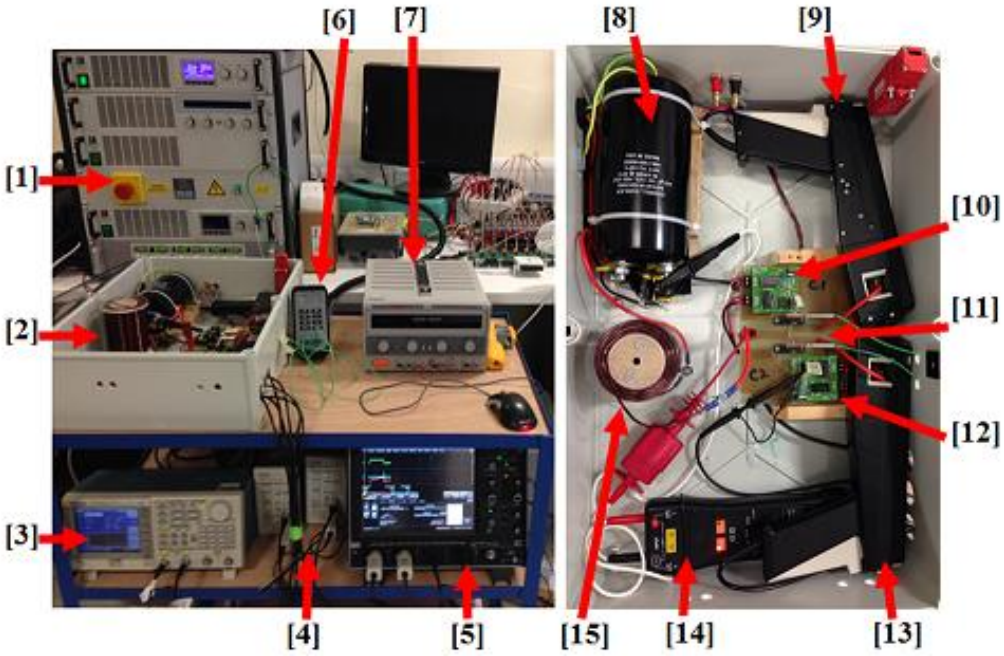


Fig. 6.7 Clamped inductive switching test rig with two parallel IGBTs and all the circuit components.

Table 6.1 Thermal parameters for materials used in power electronics packaging

Material	Thermal Conductivity	Thermal Capacity	Density
	W/mK	J/kgK	kg/m^3
Epoxy Mold Compound	0.72	794	2020
Silicon (at 25˚C)	148	712	2328.9
SnPb Solder	50	150	8500
Cu Lead Frame	360	380	8890

Table 6.2 Calculated 5 level Cauer-thermal network for TO247 Package

Silicon IGBT Die	R1	0.010135	C1	0.0249
SnPb Solder Layer	R2	0.0277	C2	0.0367
Cu Lead Frame	R3	0.021515	C3	2.7260
Epoxy Mold Compound	R4	10.7575	C4	1.2942
Cu Heatsink	R5	0.0222	C5	3.7564

The test rig is the same as used in Chapter 4, shown in Fig. 5.27; however, the only difference is that two IGBTs were put in parallel in the bottom side switching device and the current probes were used to capture the current passing through each device.

6.3 Results and Discussion

During the experiments, two IGBTs were connected in parallel at the bottom side of the half-bridge and double pulse test was carried out on both devices. Fig. 6.8 shows the experimental results

and the simulation results obtained from the physics-based model when one of the devices was working at higher junction temperature than the other; meaning the cooler device was at 25°C while the hotter device was at 110°C. As can be seen, the device with higher case temperature, takes less current than the cooler device. This is due to the positive temperature coefficient of the IGBT's on-state resistance and the current divider rule which means that more current flows through the less resistive IGBT.

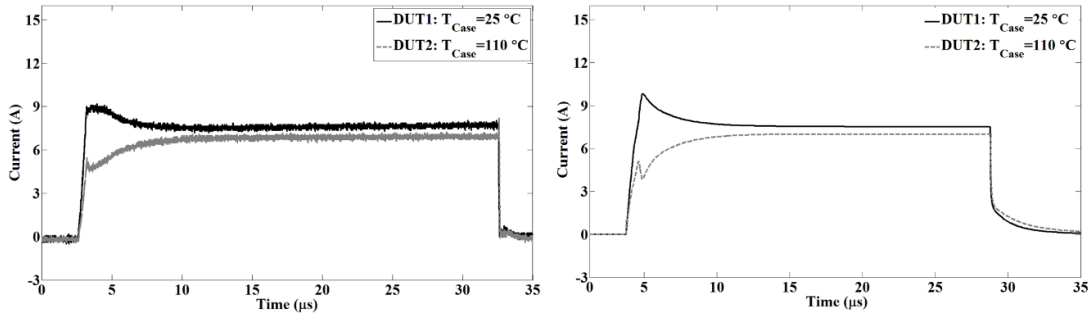


Fig. 6.8 Experimental results (Left) and Simulation results (Right) of turn-on and turn-off switching current waveforms of two parallel IGBTs working at different junction temperature.

In another case scenario, two devices were driven with different gate resistances; i.e. the slower switching device was switched with R_G=47Ω while the faster switching device was switched with R_G=10Ω. The experimental and simulation results showing turn-on and turn-off waveforms for two devices are shown in Fig. 6.9 and Fig. 6.10 below. Fig. 6.9 shows that the faster switching device takes on more load current since the slower switching device turns on later. Fig. 6.10 shows that during turn off, the slower switching device takes on more of load current. This can be used in condition monitoring of power IGBTs where one device is degraded at higher rate than the other IGBT and shows higher gate resistance due to gate wire bond delamination. As can be seen in Fig. 6.10, the device with higher gate resistance switches off slower than the device with lower gate resistance. This results in a peak current in this device as the faster device is switched-off and

consequently puts more load current on the slower device. As can be seen the model can accurately predict the device behaviour.

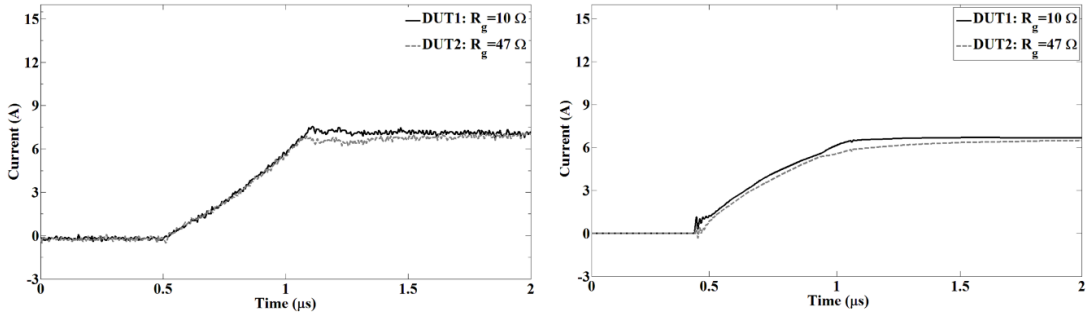


Fig. 6.9 Experimental results (Left) and Simulation results (Right) of turn-on switching current waveform of two parallel IGBTs working with two different gate resistances.

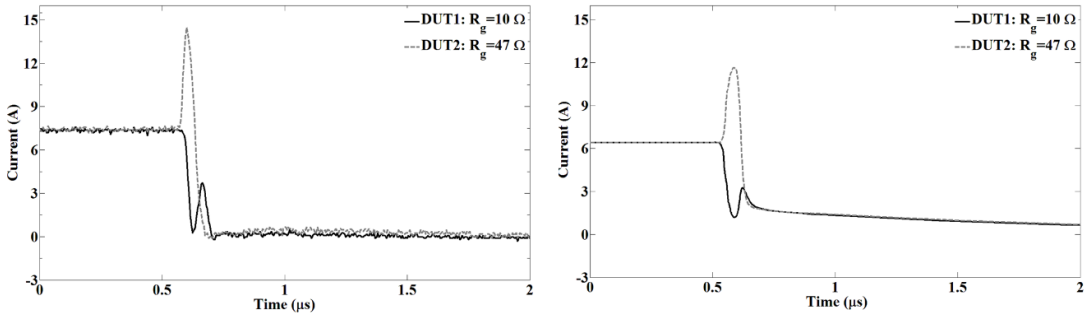


Fig. 6.10 Experimental result (Left) and Simulation results (Right) of turn-off switching current waveform of two parallel IGBTs working with two different gate resistances.

Fig. 6.11 and Fig. 6.12 show the turn-on and turn-off switching current waveforms of two parallel IGBTs when working under different case temperatures. The cooler device is working at room temperature (25°C) while the other device is heated to 55°C. The results indicate that when the junction temperature of devices increase, the device with lower junction temperature takes higher current and it switches at different switching speed (*dI/dt*). As can be seen, the model can accurately predict this behaviour. Moreover, Fig. 6.8 shows the hotter device is working at 110°C.

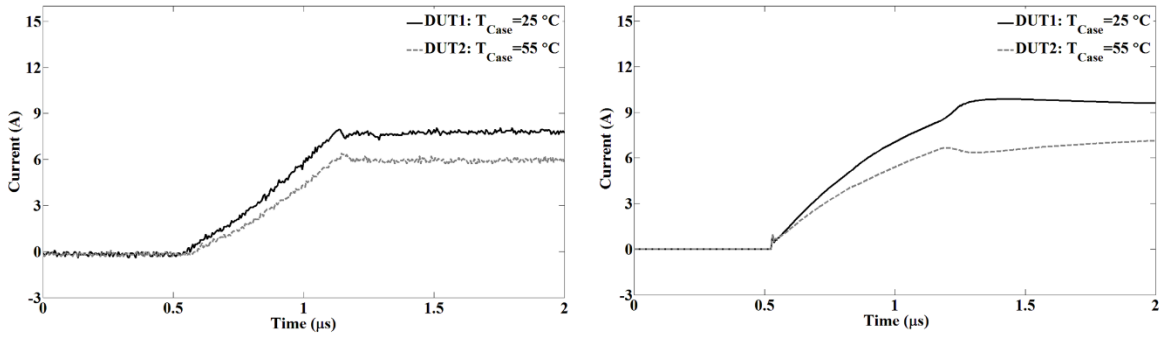


Fig. 6.11 Experimental result (Left) and Simulation result (Right) of turn-on switching current waveform of two parallel IGBTs working at different case temperature (25°C and 55°C).

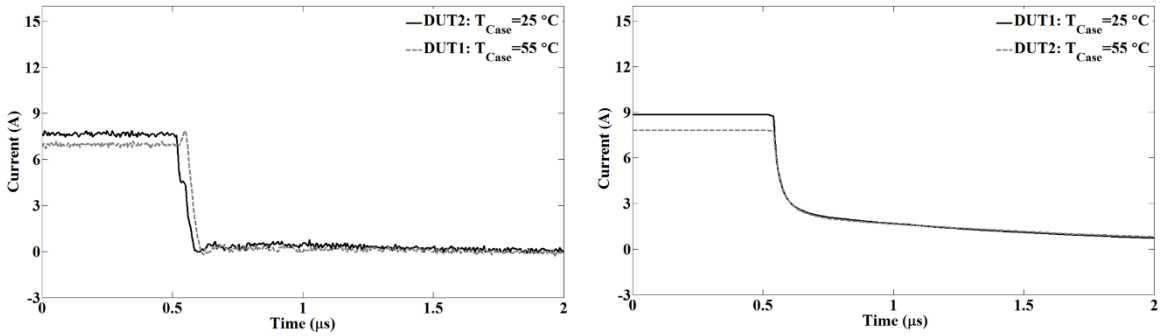


Fig. 6.12 Experimental results (Left) and Simulation results (Right) of turn-off switching current waveform of two parallel IGBTs working at different case temperatures (25°C and 55°C).

A closer look at the switching of the device working at 110°C is shown in Fig. 6.13 and Fig. 6.14. Comparing these results with the results at 55°C in Fig. 6.13 and Fig. 6.14, indicates that the current sharing between two devices becomes even more unbalanced. Consequently, the amount of current which passes through the warmer device reduces more significantly.

During the experiment, in order to evaluate the temperature rise in the unbalanced parallel IGBTs, the devices were switched under repetitive clamped inductive switching using different gate resistors. The temperature rise on the case of the devices were logged using thermocouples which were mounted at the backside of each IGBT. The frequency of pulses were set to 1 kHz and the duty

cycle of the pulses were set to 10%. Due to the unbalanced switching between the parallel devices, the device with the higher gate resistance showed a higher case temperature rise after 600 seconds of repetitive switching.

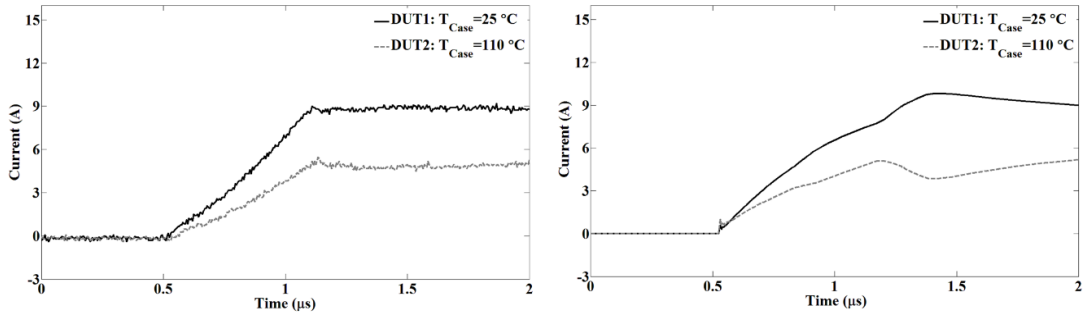


Fig. 6.13 Experimental results (Left) and Simulation results (Right) of turn-on switching current waveform of two parallel IGBTs working at different case temperatures (25°C and 110°C).

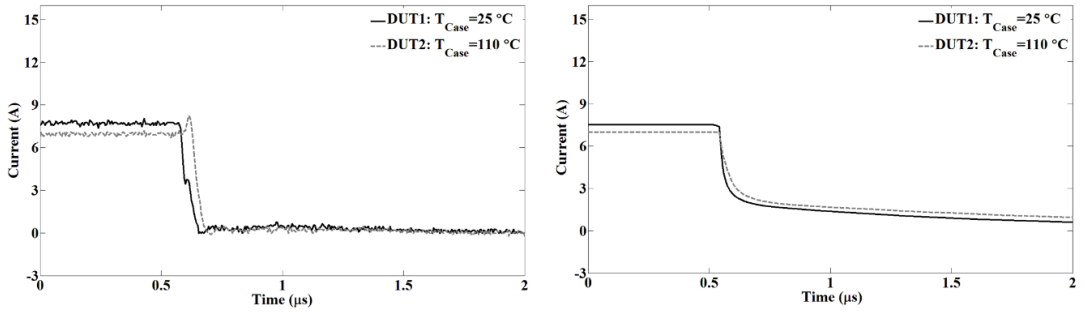


Fig. 6.14 Experimental results (Left) and Simulation results (Right) of turn-off switching current waveform of two parallel IGBTs working at different case temperatures (25°C and 110°C).

Fig. 6.15 shows the experimental result and the simulation result obtained from the Cauer-thermal network for two parallel IGBTs under repetitive clamped inductive switching using two different gate resistances. As can be seen, the thermal network can predict the temperature rise in the devices due to the unbalanced current sharing between the two IGBTs. The device with larger gate resistance switches slower than the device with a smaller gate resistance, hence, more current passes through this device and consequently the temperature of the device rises more rapidly than the device

with a smaller gate resistance. As the temperature of the device increases, the carrier lifetime and diffusivity of minority carriers increases and consequently the tail current of the device increases which brings about higher losses. Moreover, the threshold voltage of the device reduces as the temperature rises which brings about even slower turn-on rate. Turn-off losses are relatively larger than turn-on losses or conduction losses for IGBT and consequently the effect of turn-off losses is more dominant in temperature rise within the device when the current sharing is unbalanced.

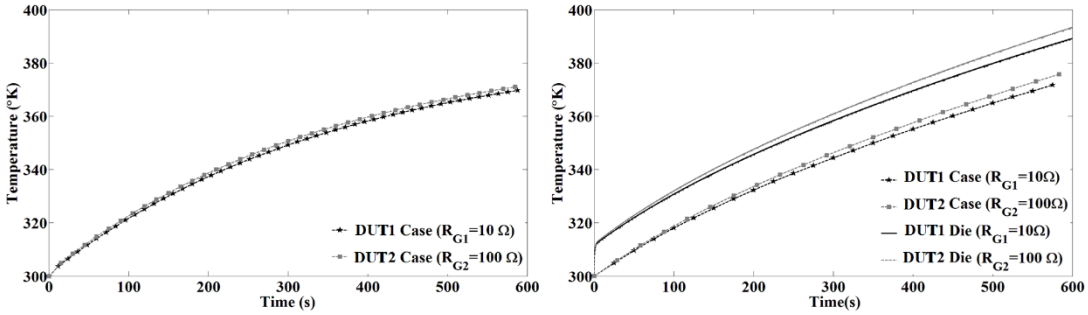


Fig. 6.15 Experimental results (Left) and simulation results (Right) of temperature rise within two parallel IGBTs with different gate resistances under repetitive clamped inductive switching.

Because the model does not take heat radiation into consideration, the final temperature obtained in the simulation is slightly higher than the experimental results. Moreover, the simulation results show that the temperature of dies are around 20°C higher than the case temperature and the temperature difference between two dies operating using different gate resistances is around 7°C. It is worthwhile to mention that this becomes significant in the power modules with higher current rating and working at higher voltages.

6.4 Conclusions

A physics-based temperature-dependent IGBT and diode models were used to model the current sharing between two parallel IGBT working under different electro-thermal conditions. In one scenario, the gate resistance of each device was varied and in another case scenario the junction temperature of devices were varied. The devices were tested in a clamped inductive switching test rig and the current passing through devices were measured. Using the model, the switching current waveform was predicted accurately. This model can be used by power electronic engineers to model non-uniform degradation of devices or reliability issues arising from solder delamination or gate wire bond degradation in individual devices in a module. The electro-thermal model is able to simulate the electrical switching characteristics of the IGBT very accurately on the microsecond scale while also being able to simulate the long thermal transient on the millisecond to second scale. This has been achieved by using 2 Cauer-thermal networks and a look-up table to decouple the electrical and thermal time constants. Hence, the effects of electro-thermal imbalance between parallel connected IGBTs can be captured accurately in a computationally inexpensive methodology.

Part II

Chapter

7 Design and Fabrication of an Automotive Power Inverter

7.1 Introduction

In previous chapters some of the reliability constraints of the most common power electronic devices were investigated and using modelling tools these failure modes were modelled. This chapter reviews fabrication of an automotive power converters and reviews some practical implications of power electronic packaging process.

Packaging of power electronic devices was briefly touched on in Section 2.4.2.1 where a brief introduction to packaging was presented. Fig. 2.13 and Fig. 2.14 showed a packaged SiC MOSFET and the cross section view of a conventional packaging technique in power electronic devices.

The performance and reliability of power inverters in any application requiring high power density depends on proper electrical, thermal and electromagnetic design

of the power stage. The electrical design needs to make sure that the complementing devices have the same voltage rating and current rating, the switching speed of the devices are within an acceptable range for the required switching frequency, devices are paralleled in a way that they can handle current equally and so on.

Based on the DC voltage level of the vehicle's battery and the required power and torque of the motor for different applications, inverters with different power, voltage, and current rating devices need to be carefully selected for that application. The power rating of a vehicle is based on the functionality of the electrical drive unit and can vary between 12kW up to a few hundreds of kW. Lower power electric drive units (EDU) may use a 48V system which is compliant with the health and safety standards for low voltage system and reduces the risk of electrocution. As the demand for the speed, torque and overall performance of the motor increases, higher voltage DC link and hence higher voltage power electronic devices are utilised to deliver the power to the wheels of the vehicle. At a constant DC voltage level, power can be increased by increasing the current. Hence, larger dies with higher current handling capability are needed. Alternately, more dies can be paralleled to achieve the higher current demand. Only devices with positive temperature coefficient of transconductance (K_P), on-state resistance and saturation voltage ($V_{CE\,(sat)}$) can easily be used in paralleling devices. Saturation voltage and transconductance determines the conduction losses of the device in the first quadrant operation. MOSFETs and NPT IGBTs are suitable for paralleling. Each power electronic device can handle a certain current density at a fixed

temperature. Generally, the current density of normal Si-based dies are approximately 200 Acm^{-2}.

A positive thermal coefficient infers that the operating voltage drop across the device increases with temperature. However, this is only seen at higher currents, above an isothermal point below which this behaviour reverses.

The thermal design of the power inverter determines how much heat must be transferred away from each device, how the temperature stress distribution affects the performance and reliability of each device and how much current can pass through the devices during conduction. It also imposes an upper limit on the switching frequency that can be used, before the device over heats. The electromagnetic design is essential in the layout of the design to reduce the parasitic inductances and resistances. Moreover, reduction of the inductance, reduces the amount of overshoot in the voltage and current and hence, can improve the EMI arising from the high current and voltage.

In this section, three power modules were designed and fabricated to investigate a number of critical features that impact on reliability. For example, the number of wire bonds and how this affects the switching performance of SiC MOSFETs (as discussed earlier), the parasitic induced gate turn-off in SiC MOSFETs, the impact of current loop on the electro-thermal performance of Si-IGBT and PiN diode pairs in a 2 level inverter and improve the thermal performance and increase the power density of a 3-phase 2 level automotive power inverter. The next section explains the packaging process used to fabricate the power modules followed by packaging of the three power modules.

7.2 Packaging Process

Packaging of power electronic devices and fabricating a power module starts from designing the power module components, carefully choosing materials and determining the dimensions for the modules and its components. These are based on the application requirements. The design process starts from designing the DBC substrate layout, choosing the DBC substrate materials and defining the thickness of each layer. For automotive applications, the layout of the DBC substrate is usually a simple 2-level 3-phase inverter comprising 6 switching devices with anti-parallel freewheeling diodes. This is shown in Fig. 2.2. This design is made by etching the top side copper of the DBC substrate into isolated islands in which each island is either gate, drain or source of the IGBTs and positive and negative DC side plus the phase output of each leg of the inverter. Thick copper is required for power modules (300 μm) because they must carry high currents. This means that the edges that are etched will not be perpendicular to the ceramic substrate and they will have a slope depending on the thickness. An alternative to etching the copper is laser machining of the copper to create the isolated islands. This gives a more precise layout and a sharper definition for thick copper. Fig. 7.1 shows the pitch and width of spacing between two conductor islands on a DBC substrate. These spacing are determined based on the techniques used to fabricate the DBC substrate and the thickness of the copper layer. Table 7.1 gives some indication of the spacing between two conductors on a DBC substrate. For a DBC substrate with two conductors with 1200V voltage difference, a minimum pitch of 1 mm with width of 0.5

mm is recommended which is viable using a copper thickness of 0.3mm. The minimum spacing is required for electrical isolation and preventing electrical arc to occur during the device operation.

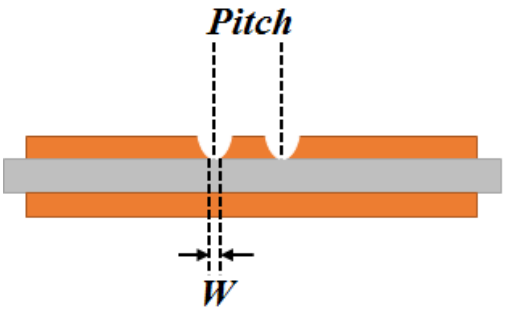


Fig. 7.1 Minimum pitch and minimum width of spacing between conductors on a DBC substrate.

Based on the DBC material property information provided in Table 2.2 and the voltage rating of the power inverter, the thickness of the ceramic layer is chosen. The ceramic used in the DBC substrate provides isolation between the active side of the inverter and the cooling system and between different parts of the circuit with different voltages. In automotive application, according to ISO 6469-3 standard document of electrically propelled road vehicles-safety specifications, part 3: protection of person against electric shock, section 8.3, the isolation material should be able to withstand 2 times of the maximum AC working voltage of the electric circuit plus 1000V. Hence, for a power inverter designed to work with 800V DC link voltage using 1.2kV devices, the ceramic substrate should be able to withstand 2600V AC (rms) voltage (peak voltage of 3702.66V). Hence, if AlN substrate with breakdown voltage 14 kV/mm is chosen for this hypothetical example, a minimum thickness of 0.235 mm is needed. These values are

valid for room temperature and altitude of below 2000m. For a vehicle which is required to operate at higher altitudes (for instance the Chinese requirement for vehicles operating in heights of Himalaya) the thickness of the 0.63 for AlN DBC substrate is recommended which ensures that the isolation does not break.

Table 7.1 Pitch and width (spacing) between conductors for different thickness of DBC substrate.

Cu Thickness	Width (W)	Pitch
0.127 mm	0.35 mm	N/A
0.200 mm	0.40 mm	N/A
0.250 mm	0.45 mm	N/A
0.300 mm	0.50 mm	0.5 mm
0.400 mm	0.60 mm	N/A
0.500 mm	0.70 mm	0.8 mm

Design of the layout of the DBC substrate may be carried out using any CAD software and during this process, it is important to keep the current path length as short as possible. Moreover, the lateral heat flow out of the devices needs to be considered and the shrinkage of the DBC footprint must not have negative consequences such as thermal runaway of the parallel devices due to the increased power density.

Next the power devices are selected, which depends on the DC voltage requirement of the application. Based on the parasitic inductance of the circuit layout and the load, a headroom is considered for the voltage rating of the devices. As a common practice in automotive industry, voltage rating of the power devices are chosen to be two times larger than the DC voltage level to take account for the switching transients and overshoot voltages which may occur during the operation of the inverter.

Moreover, this voltage rating needs to be large enough to be able to block the back-EMF of the electric motor in open circuit condition at maximum speed of the motor. The current rating of the device needs to be selected based on the electric motor current rating. The current rating of the anti-parallel diode also needs to be large enough for the regenerative braking rectification and the freewheeling of the current during the switching of the devices. These need to be considered at the peak operating temperature of the inverter (between 125-150°C).

Next, the die attach technique needs to be selected. There are two main methods for attaching the die to the substrate: i) soldering ii) sintering.

Soldering is the most popular way of attaching the device to the substrate. This involves applying a solder paste to the surface of the DBC substrate using a stencil and placing the die on the solder area and heating the substrate up to the melting point of the solder usually with a solder barrier. Once the solder is molten and the metallurgical contact between the back side metallization of the die and the substrate is formed, the device is cooled and the process is completed. The soldering process can be completed in a vacuum reflow oven. This reduces the void area under the device and this increases the reliability of the power module. In automotive applications soldering using vacuum reflow process is required. Several types of solder pastes exist with different melting point and wetting profiles which can be chosen based on the application. Most of the automotive power inverters are soldered using solders with the following particles: %95.5 Sn, %3.8 Ag and %0.7 Cu (which are lead free).

In contrast, sintering needs to be carried out at elevated temperature and pressure. The die attach is a silver film or silver paste containing silver particles and it shows a significant improvement in electrical conductivity, thermal conductivity and mechanical strength. Hence, the lifetime due to electro-thermal fatigue is increased. Silver sintering process usually starts with vapour deposition of a thin layer of silver on the substrate or using electro-less silver plating for the area that the die sits on top. Next, a thin layer of silver paste is applied to the deposited silver film using conventional silver printing. Following this, the device is placed on top of the substrate and it is preheated to 80°C. Then the temperature is elevated to 280°C and quasi-hydrostatic pressure sintering process takes place after this preheating process at 240°C during which a 40MPa pressure is applied for 5 minutes, and completed by sintering at 880°C at atmosphere pressure. [92, 93].

The stencil that is designed to apply solder paste is usually made from Aluminium of different thickness. The thickness of the stencil determines the thickness of the solder layer underneath the device. For normal applications where the thickness of the solder layer is not of importance, a stencil mask with thickness of 0.1524 mm is usually used. In order for the solder to stop flowing on the surface during the reflow process, the area of the pad which is exposed to the solder is reduced by factor of 10% in comparison to the pad size of the die itself. Moreover, if the pad size is very large, it can be divided into smaller rectangular net-like form to reduce the amount of solder flow during the reflow process. Fig. 7.2 illustrates an Al stencil used for solder screening with thickness of 6 thou (0.1524 mm). It is important to have a uniform solder across the die with the

same thickness. Hence, it is recommended to use a solder paste screen printing tool. Fig. 7.3 shows a solder screen printing machine at the University of Warwick.

Fig. 7.2 Al stencil for solder screening process with thickness of 6 thou.

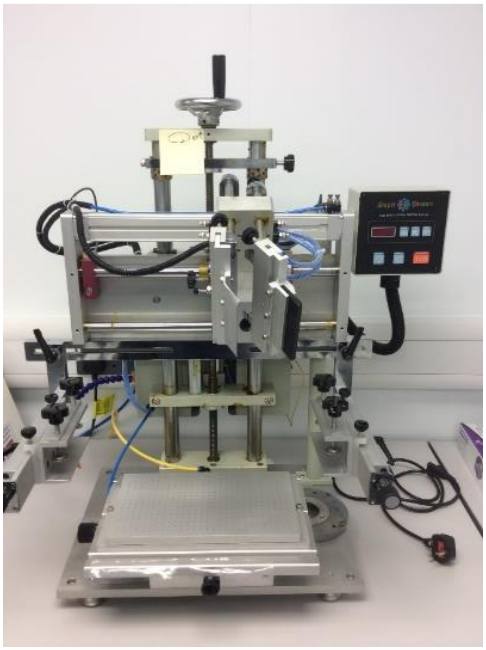


Fig. 7.3 Bench-top Mascoprint S200HFC semi-automatic solder screen printing machine with stencil holder.

Once the solder is applied, the devices need to be picked and placed on top of the solder layer. Fig. 7.4 shows a die pick and place equipment used to place device on top of the solder. Prior to placing the devices on the DBC substrate, if the devices are contaminated or oxidized, they need to be cleaned using isopropanol alcohol or by plasma etching process. Fig. 7.5 shows a PiN diode that has been exposed to air and been contaminated.

Fig. 7.4 Cammax Precima EDB65 Eutetic pick and place die bonder, including N2 cover gas.

Fig. 7.5 a PiN diode contaminated due to exposure to air.

Next, the sample is placed in a vacuum reflow chamber in which the soldering process occurs. Fig. 7.6 shows an ATV vacuum reflow oven. This oven is programmable and a soldering profile can be used to achieve the most optimum solder joint. During the soldering process in this vacuum, the pressure, temperature and gases entering the oven can be controlled through a program which opens or closes the gas valves and controls the temperature of the chamber and the sample. The chamber has two temperature sensors, one measuring the temperature of the carbon plate on which the sample is placed and the second temperature sensor sits on top of the sample and controls the temperature of the sample using a feedback loop.

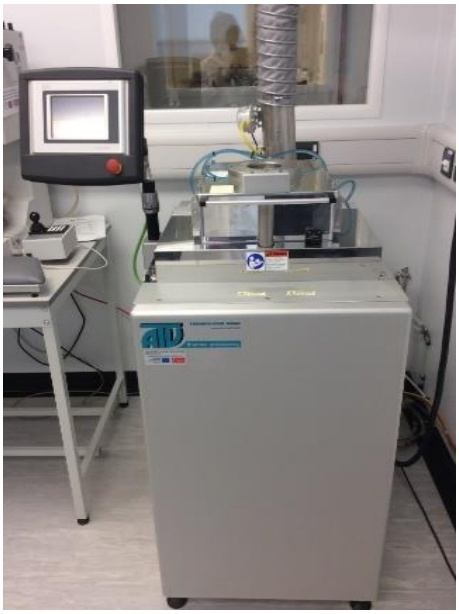


Fig. 7.6 ATV SRO-704 programmable solder reflow/thermal processing, rapid thermal annealing (RTA) oven with 950°C processing capability.

Fig. 7.7 shows an example of reflow oven profile, programmed on the ATV reflow oven. This profile is the most common used profile in automotive application which is used for solders with %95.5 Sn, %3.8 Ag and %0.7 Cu particles. An example of this solder is Indium 8.9HF Pb-Free solder paste. During the first phase of the process, Nitrogen is injected into the chamber for 60 seconds. In the next 60 seconds, the gases inside the chamber are vacuumed. This makes sure that the all the oxygen inside the chamber is removed. During this process, the pressure inside the chamber goes down to 2.3 mbar. In Stage 3, nitrogen is injected into the chamber and the oven is preheated to 50°C. At stage 4, the temperature is ramped up to 204°C while nitrogen is being injected into the chamber. The duration of this preheat is 2:30 minutes. At stage 5, the temperature is kept constant for 1:30 minutes to make sure that the temperature of the sample reaches to 204°C. During stage 6, the device is heated to 210°C which is below

the 217°C melting point of the solder. This is known as soaking stage which helps to minimize the voiding under the device.

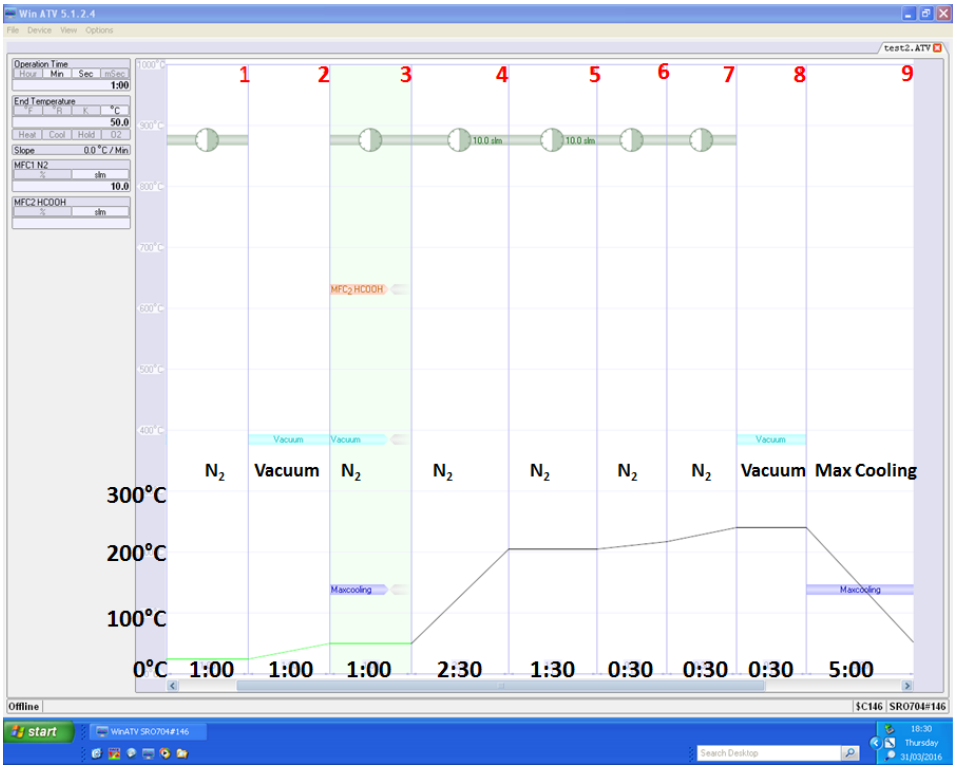


Fig. 7.7 Reflow soldering profile loaded on the programmable ATV reflow chamber.

Next, the temperature is ramped up to 217°C at which the solder melts and fumes due to existence of solvent in the solder emits and extracted. Now, the device might move slightly during reflow. In order to achieve an acceptable wetting and form a good quality metallurgical contact, the temperature of the solder is ramped to 15-30°C above the melting point and kept at this temperature for 30 seconds. During this stage, the vacuum starts operating and the gases are extracted from the chamber. This reduces the bubbles due to evaporation of the solvent to be taken from underneath the solder and places the solder on top of the solder paste if it moved in the previous stage. The

next stage is controlled cooling of the sample down to the room temperature using liquid Nitrogen. Fig. 7.8 shows a sample in the oven during the stage 6 of the reflow process.

Fig. 7.8 Sample in the ATV oven during stage 6 of the Indium 8.9HF Pb-Free solder reflow profile.

Once the device has cooled, it is removed from the chamber and the surface of the device is cleaned using IPA isopropyl alcohol (also known as isopropanol). This removes the residuals of flux in the solder from the surface and prepares the surface for the wire bonding process. Wire bonding process requires bonding pad cleanliness and removing the pad surface oxidation and wire oxidation. The surface may be plasma etched or the pad surface can be milled to remove the oxide and residues from the surface.

Wire bonds on top of the device are usually Al wire bonds as it requires less energy and pressure to have wire bond contact using ultrasonic welding process. Au, Al coated Cu and recently Cu heavy wire bond are alternates to the conventional Al wire bond as they can provide lower resistance, higher current handling capability and longer lifetime. Cu wire bonds are lower cost than Au, have superior electrical properties to Al and have higher mechanical property specifications. Hence, they are attracting more

interest for power electronics and microelectronics chip packaging. However, the metal plating of the surface for copper wire bond requires to be AlCu bond pad structure. Cu oxidises very quickly and hence, the process needs to be carried out in Ar and N_2 gas environment to prevent oxidation [94]. Fig. 7.9 shows a semi-automatic Orthodyne heavy wire bonder used for wire bonding power electronic devices. The thickness of the Al wires that can be used for this machine starts from 0.127 mm (5 thou) and moves up to 0.508 mm (20 thou). The reliability of wire bonding for power electronic modules for different wire thickness has been investigated in [95, 96] and shows that thin wires are able to withstand a higher number of electro-thermal cycles in comparison with thick wires.

Fig. 7.9 Orthodyne model 20 heavy wire bonder.

In order to achieve the same quality in the parallel wire bonds and increase the through put of the process, automatic wire bond machines can be used. The parameters

that are set in a wire bonding process are the ultrasonic time and power during the first bond and the second bond, force of the bonding tool, tail length of the wire and height of the wire loop. Fig. 7.10 shows an automatic wire bond tool which was used to carry out the wire bonding of the power inverter and parallel wire bonds on an IGBT carried out at Warwick.

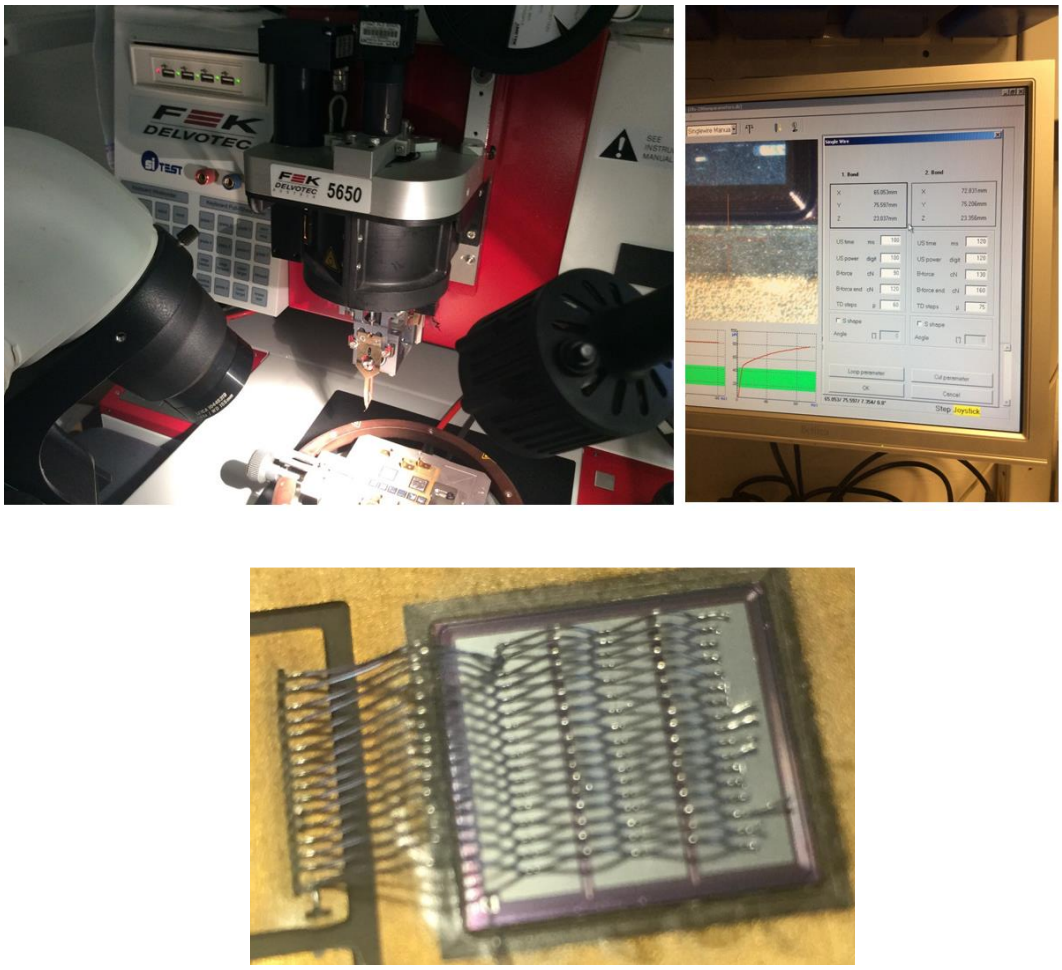


Fig. 7.10 FEK Delvotec 5650 heavy automatic wire bonder and a wire bonded IGBT made at Warwick.

7.3 Packaging SiC MOSFET

In this section, packaging of a SiC MOSFET using a conventional packaging technique is presented. The device packaged in Fig. 2.13 was packaged to compare the performance of the device when it is packaged using conventional techniques; i.e. Conventional soldering technique and Al wire bonding on the top side of the device.

The SiC MOSFETs packaged here were 1200V/50A Cree N-channel enhancement mode SiC MOSFET bare dies (now Wolfspeed and now again infineon) with part number of CPMF-1200-S080B. The dimensions of the die was 4.08×4.08 mm^2. The exposed metal pads were two pads with dimensions of 0.98×2.09 mm^2 each. The gate pad dimensions were 0.84×0.60 mm^2 and the thickness of the die was 365µm. The top side source metallization was Al with thickness of 4µm and the bottom side metallization was Ni/Ag with thickness of 0.8µm and 0.6µm respectively.

The DBC substrate used in here was AlN ceramic substrate with thickness of 0.63 mm sandwiched between two layers of Cu with thickness of 0.3 mm. The top and bottom surface finish is Ni with thickness of 5µm, Pd with thickness of 0.15µm and lastly Au with thickness of 0.03µm. The gold surface finish prevents the substrate from becoming contaminated and prevents oxide formation at the surface. This enhances the wetting process of the solder and also creates a good surface for wire bond attachment. However, this substrate is more expensive and hence, not recommended for commercial automotive application where the manufacturing cost is one of the most important

factors in material selection. AlN ceramic has the closest CTE with 4H-SiC and hence, it was chosen as the substrate. The CTE of 4H-SiC is approximately 4.0×10^{-6}/°C while CTE of AlN is 4.6×10^{-6}/°C. AlN is relatively expensive compared to alumina but it has 10-12 times better thermal conductivity and hence it enhances the thermal performance of the power module.

The drawback of the conventional packaging technique on SiC device is that it does not allow the device to operate to its maximum performance. The Al wire bonds limit the switching transient of the device due to the high parasitic inductances. This is due to the fact that the switching speed of SiC MOSFET are significantly higher than bipolar IGBT at the same voltage rating. Hence, at significantly higher *dV/dt* and *dI/dt* rates, parasitic inductances of the layout and the circuit can result in high overshoot in the voltage and current and can cause significant ringing in the switching transient of the device. The solder, limits the maximum operating temperature of the device to the melting point of the solder. In this case the solder used was Indium 8.9HF Pb-Free solder paste with melting point of 217°C.

Here, a SiC MOSFET is packaged using different number of wire bonds on the top side source of the device in order to investigate the impact of parasitic inductance of the wire bonds on the switching transient of the device. Fig. 7.11 shows the packaged SiC MOSFET using 2, 3 and 4 wire bonds on the source pads. The switching waveforms of the MOSFET during turn-on and turn-off was captured in a clamped inductive switching test and shown in Fig. 7.12 and Fig. 7.13 respectively.

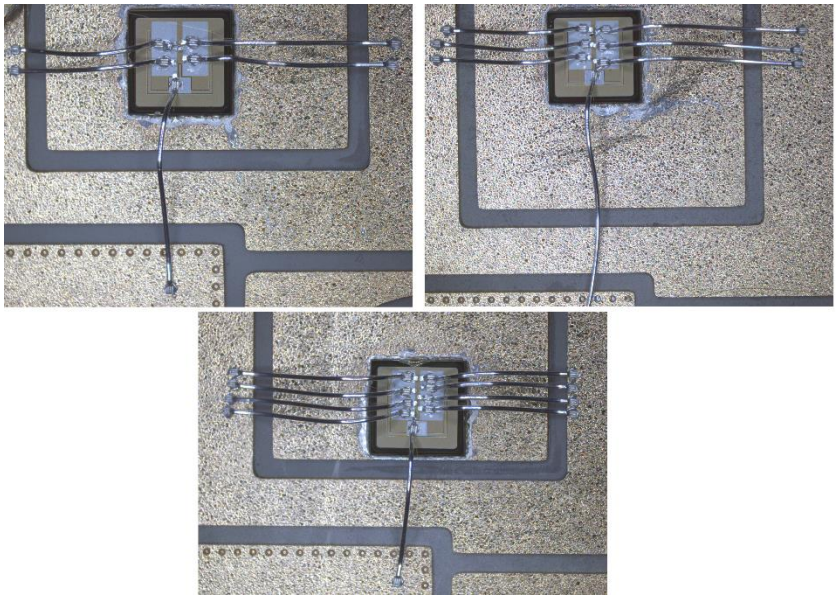


Fig. 7.11 SiC MOSFET packaged using different number of wire bonds.

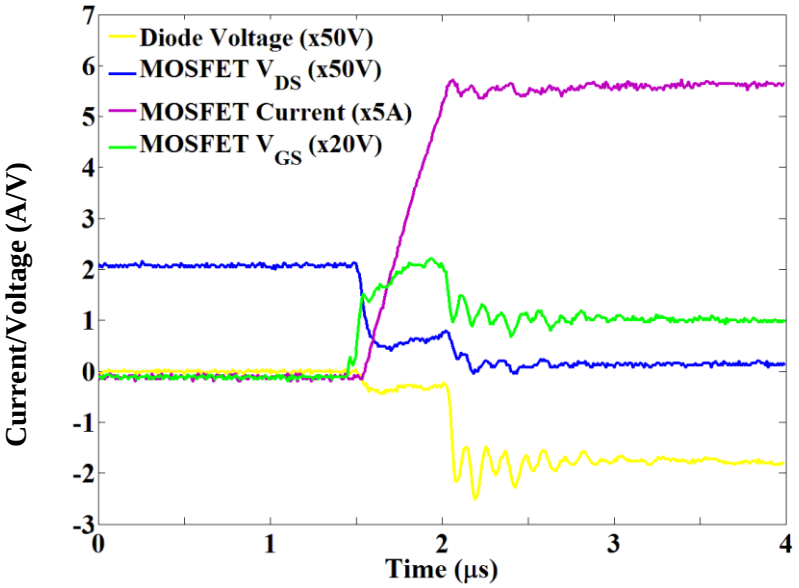


Fig. 7.12 Turn-on switching waveform of the SiC MOSFET with SiC Schottky diode at 100V and 30A Forward current at 125°C.

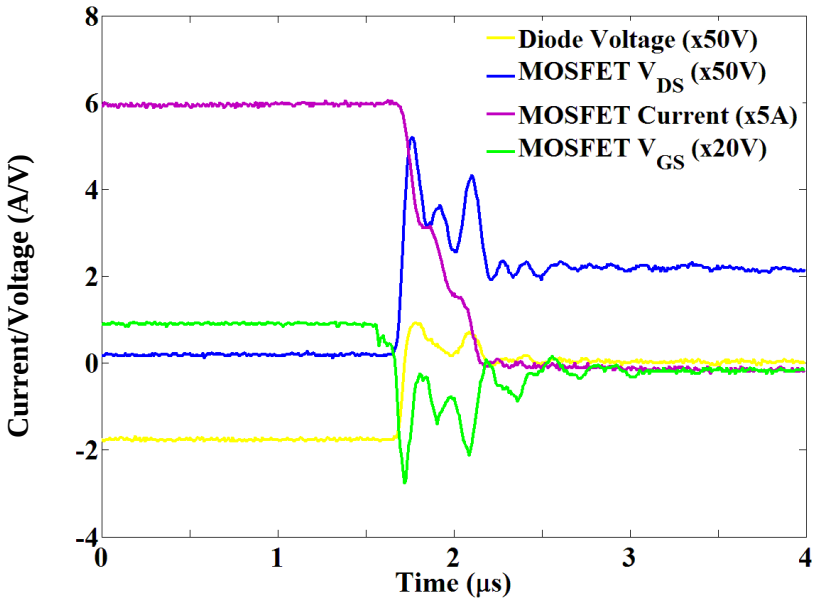


Fig. 7.13 Turn-off switching waveform of the SiC MOSFET with SiC Schottky diode at 100V and 30A Forward current at 125°C.

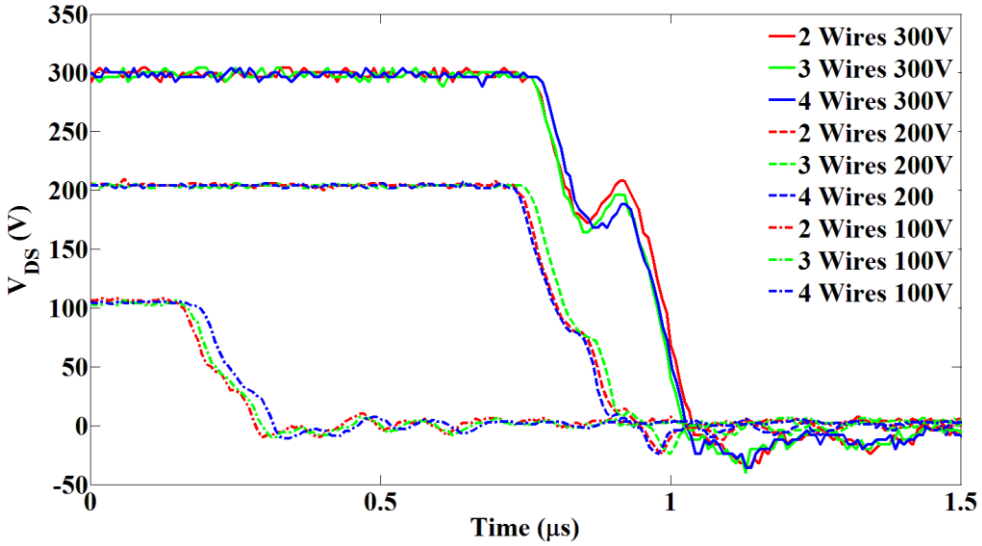


Fig. 7.14 Turn-on drain-source voltage waveform for SiC MOSFET packaged using 2, 3 and 4 wire bonds on the source pads.

This test was carried out for the device with 4 wire bonds at 100V and 30A forward current at 125°C which is the maximum current of the device at this temperature.

Fig. 7.15 shows the turn-off drain-source waveform using different number of wire bonds on the source pads. As explained earlier, the slope of the turn-off is determined by the rate of current commutation from the bottom MOSFET to the top side freewheeling diode and the overshoot in the voltage waveform of the device is determined by the parasitic inductance and the reverse recovery of the complementing freewheeling diode in the circuit. In this case, the impact of the freewheeling diode was dominant and the effect of number of wire bonds on the switching characteristic is not conclusive.

The impact of parasitic inductance due to the wire bonds on the source of the device at elevated temperatures on the current and voltage waveform of the SiC MOSFET during turn-on is shown in Fig. 7.16.

To further validate the parasitic gate turn-off phenomenon explained in Section 5.3, the MOSFET was switched with a SiC PiN diode fabricated at Warwick at different

temperatures and the switching waveforms and the reverse recovery induced parasitic gate turn-off phenomenon is shown in Fig. 7.17.

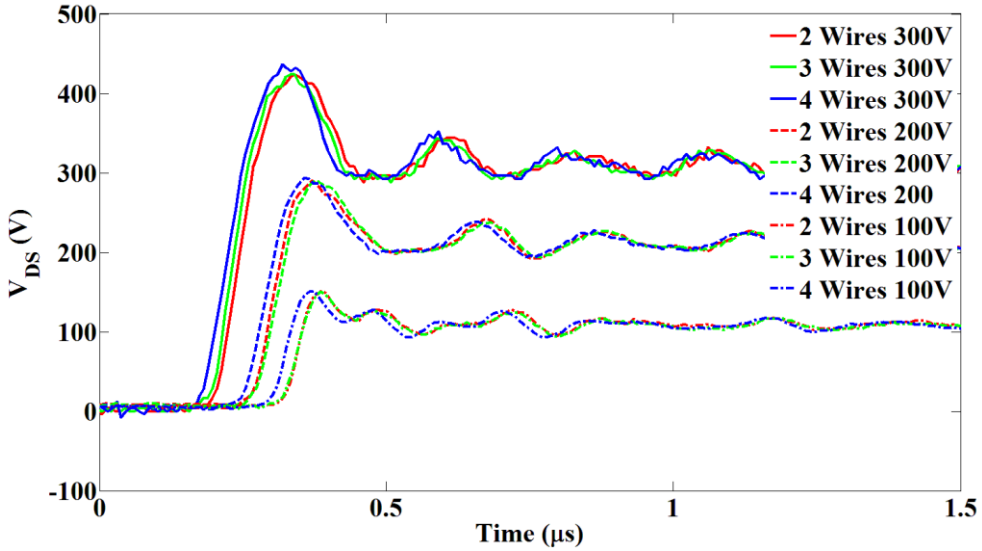


Fig. 7.15 Turn-off drain-source voltage waveform for SiC MOSFET packaged using 2, 3 and 4 wire bonds on the source pads.

As can be seen, even though the reverse recovery of SiC PiN diode is significantly smaller than that of Si-PiN diode, but at elevated temperature, this phenomenon occurs. This phenomenon is destructive and causes the MOSFET to go through thermal runaway due to high power dissipation due to switching losses. Basically, one of the consequences of snappy recovery failure mode during the parasitic induced gate turn-off is non-uniform current crowding in the MOSFET which results in generation of hot spots in the device [97]. This is shown in Fig. 7.18 for the device with 2 wire bond. The black dot on the device indicates the thermal runaway of the cells located under this spot.

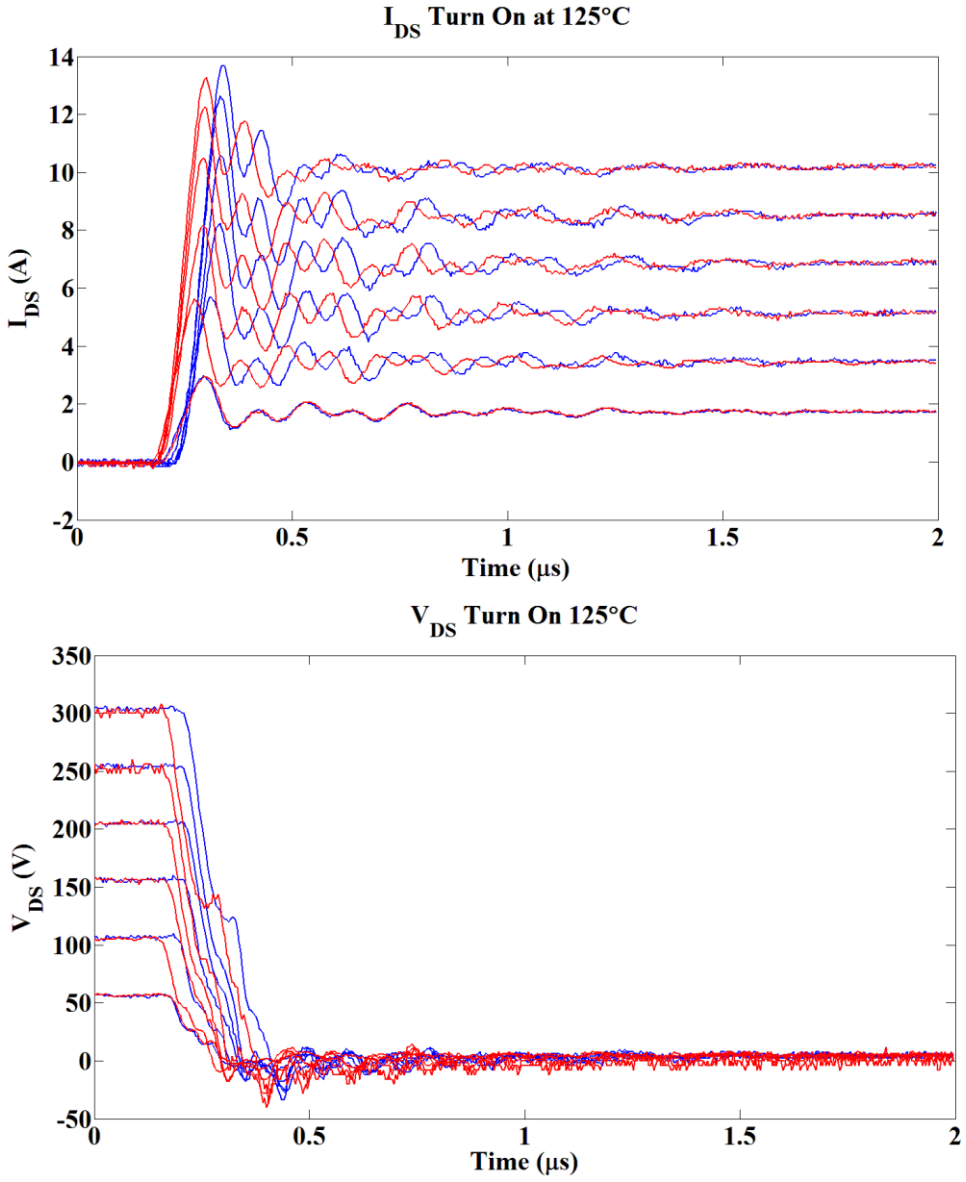


Fig. 7.16 Turn-on switching waveforms of SiC MOSFET with 2 (blue) and 4 (red) wire bonds at 125°C.

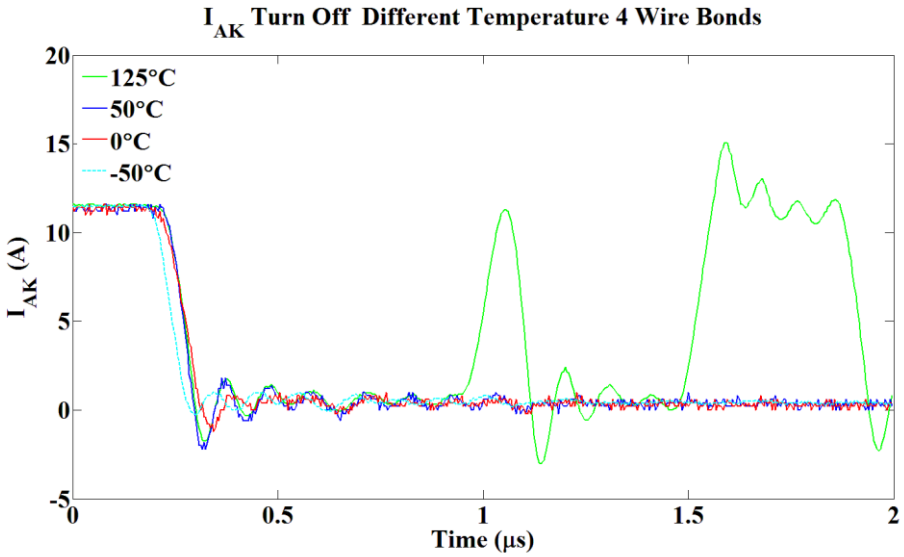


Fig. 7.17 Reverse recovery induced parasitic gate turn-off at elevated temperatures.

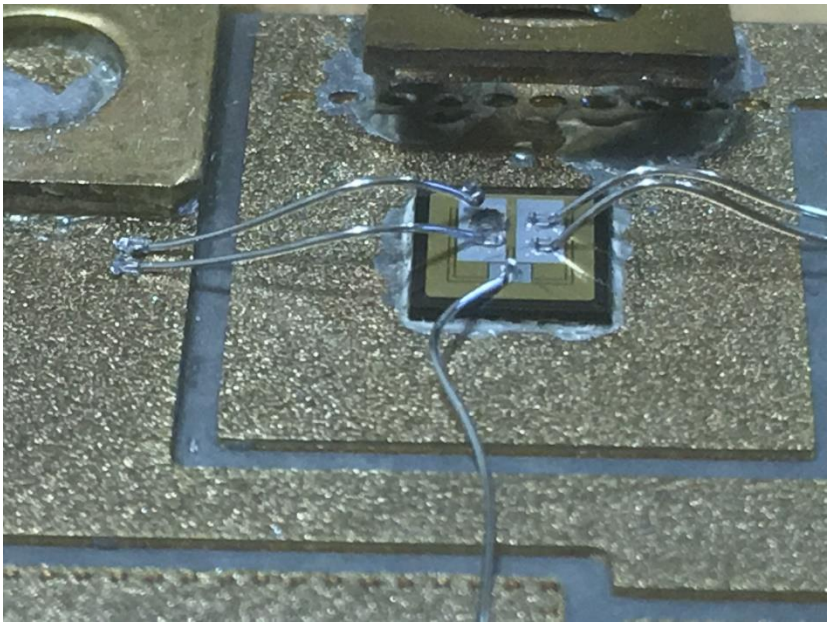


Fig. 7.18 SiC MOSFET device destruction due to thermal runaway.

7.4 Packaging a Power Inverter

A power inverter using Si-IGBTs and Si-PiN diodes was designed and fabricated. This section gives details about the design process and the fabrication of this power inverter. The aim was to develop a power stage for high DC voltage to drive a motor with power rating of 150kW. For this, 1200V/200A IGBT from International Rectifier (now Infineon) with part number of IRG8CH182K10 with complementing 1200V/50A PiN diodes with part number of IRD3CH101DB6 were used. In order to meet the power requirement, per switching device, two IGBTs and 6 antiparallel diodes were paralleled. An AlN DBC substrate was selected due to the high thermal conductivity and the top and bottom of the DBC substrate was NiPdAu electro-less plated. This enhanced the wetting process in the solder and also due to the fact that gold does not oxidize when exposed to air, the surface for wire bonding did not require further treatment and oxide removal process. Thickness of the ceramic was 0.63 mm and thickness of the top and bottom side copper layers were 0.3 mm. The area around the dies were defined to have high temperature solder stop. This prevents the solder from flowing and keeps the dies in place during the soldering process. As explained in Section 6.2, the PiN diode was contaminated. Hence, the device was cleaned and I-V curve of it was obtained to make sure that the device performance is not changed. Fig. 7.19 shows the forward characteristic of the diode. Fig. 7.20 shows the DBC substrate layout design using CAD software.

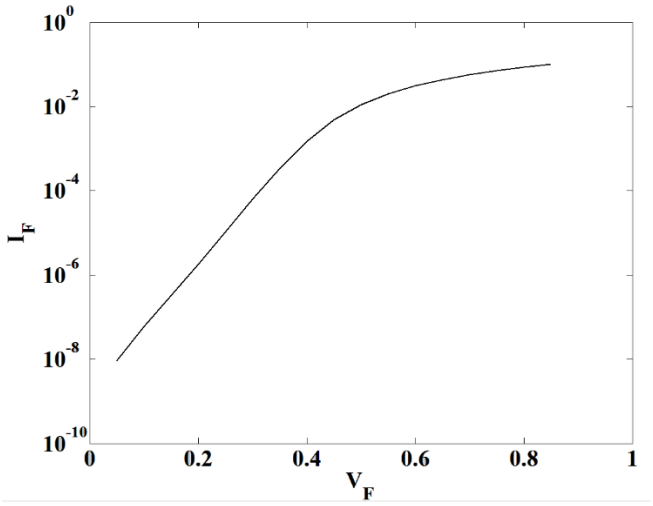


Fig. 7.19 I-V curve of the PiN diode.

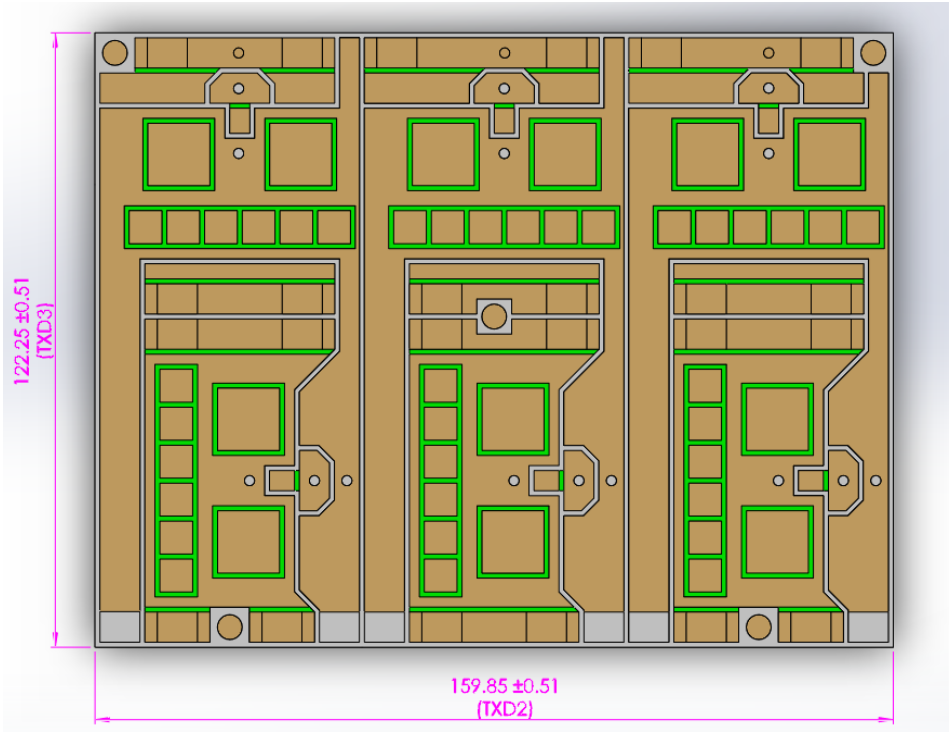


Fig. 7.20 DBC layout for three phase inverter.

After following the packaging process explained in Section 6.2, the power bridge is fabricated and ready for testing. This process is shown in Fig. 7.21.

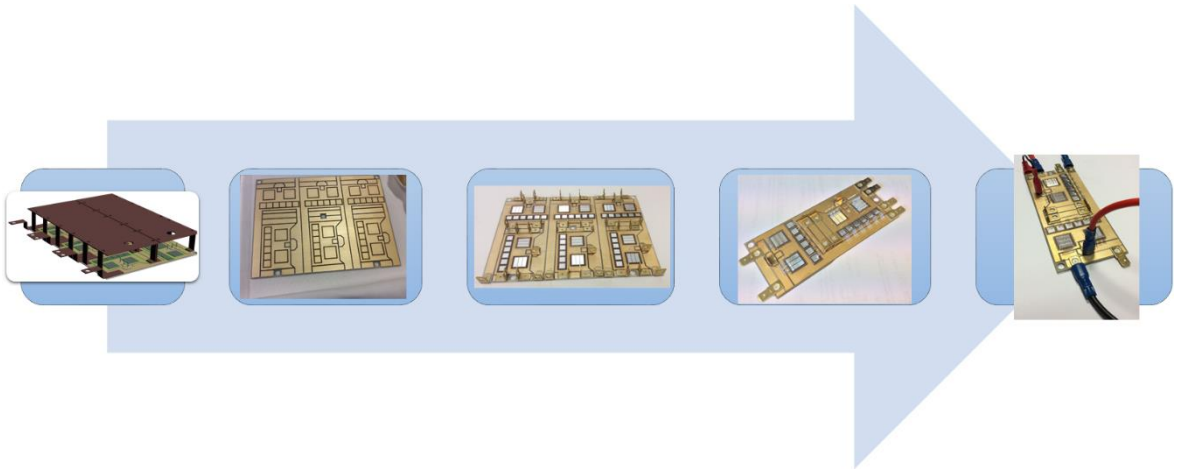


Fig. 7.21Process of fabricating the power bridge: (i) design, (ii) fabricating the layout of DBC, (iii) soldering devices (iv) wire bonding and (v) testing.

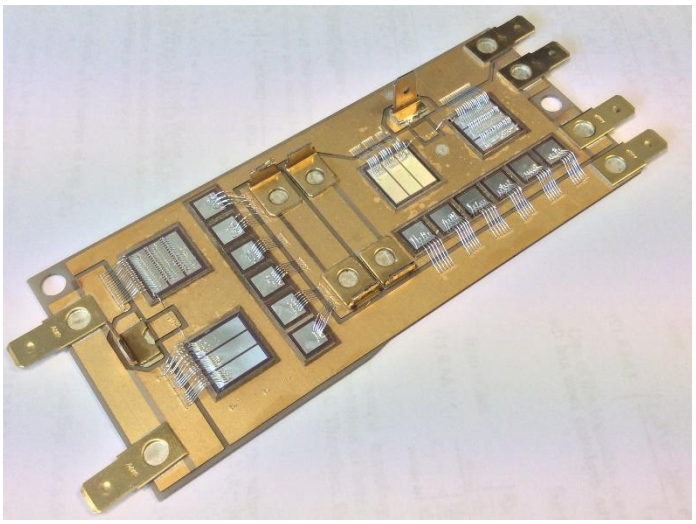


Fig. 7.22 One leg of the 3 phase power stage, showing parallel devices.

As can be seen in Fig. 7.22, the current path for the top and the bottom side switching devices are not designed to be equal and the bottom device has a longer current loop. This creates an unbalanced switching between the devices. This has feature was implemented in order to investigate the impact of unbalanced switching between two devices in the power inverter. In order to determine the parasitic

inductance of the layout, COMSOL Multiphysics was used to calculate the lumped value of parasitic resistance and inductances of each part of the layout. Moreover, inductance of a single wire bond was also calculated using this FEM tool. The impact of having multiple parallel wire bonds is the internal electric magnetic field coupling and an added mutual inductance can effectively reduce the amount of inductance. Fig. 7.23 shows the magnetic flux density and coil potential of a single coil modelled in COMSOL.

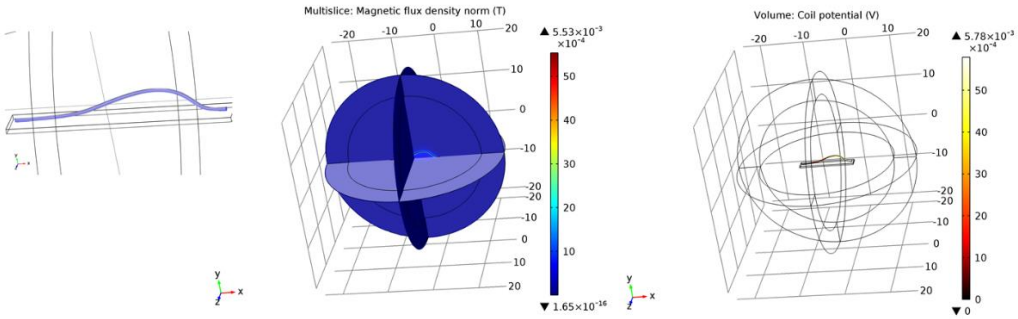


Fig. 7.23 Parasitic inductance modelling in COMSOL for a single wire bond.

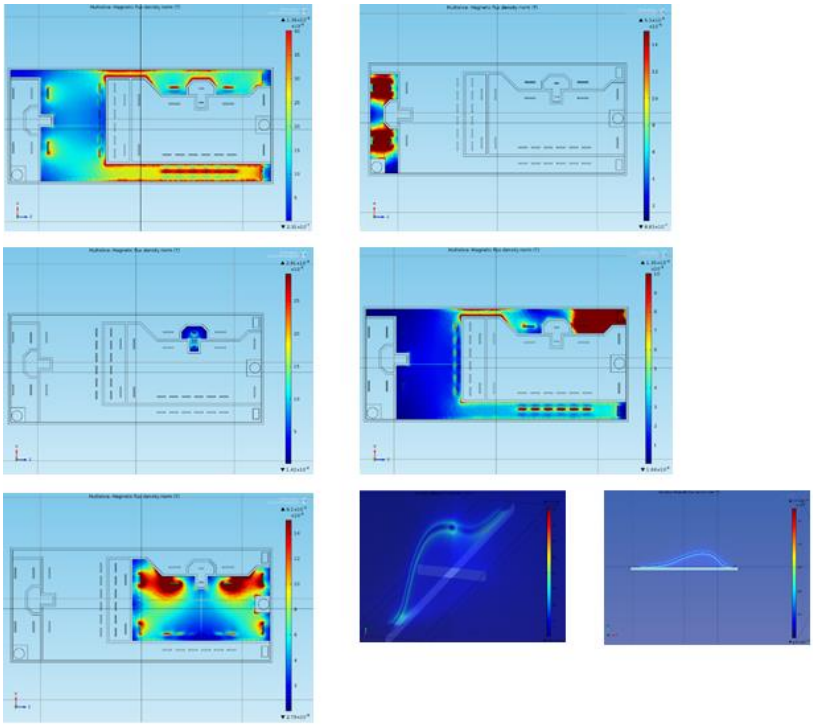


Fig. 7.24 Magnetic flux density of each island on the DBC during operation of top or bottom side IGBT/diode.

Table 7.2 Parasitic inductance and resistance of the DBC layout.

	INDUCTANCE	RESISTANCE
Bottom Switch Collector	10.4381 nH	0.358294 mΩ
Bottom Switch Emitter	0.906044 nH	0.0214592 mΩ
Gate	2.53047 nH	0.0817967 mΩ
Top Switch Collector	1.10261 nH	0.0267436 mΩ
Top Switch Emitter	3.11811 nH	0.087062 mΩ
Wire bond (per wire)	5.91523 nH	5.78 mΩ

Table 7.2 shows the calculated parasitic inductance and resistance. As can be seen, the results indicate that the bottom side collector has approximately 10 times higher parasitic inductance in comparison to the top side switch and this is due to the

very long current loop for this device. Equation (7.1) below was used to calculate the parasitic inductance of the circuit in which, $E_{p,m}$ is the total magnetic energy which is calculated by integrating the magnetic energy density and I is the current which induces the magnetic field. The magnetic field is calculated using Ampere's law and Maxwell's equations.

$$E_{p,m} = \frac{1}{2} LI^2 \tag{7.1}$$

In order to investigate the impact of current loop, the diode circuit was configured to have a long current loop path and a small current loop path and using a thermal camera, the temperature of the device was captured when repetitive clamped inductive switching test was carried out on the device. Fig. 7.25 shows the circuit configuration to obtain the short and long current paths during the repetitive clamped inductive switching test. The repetitive clamped inductive switching test was carried out at 4 kHz switching frequency and the temperature rise of the parallel diodes were captured. Fig. 7.26 shows the test rig configuration during this test.

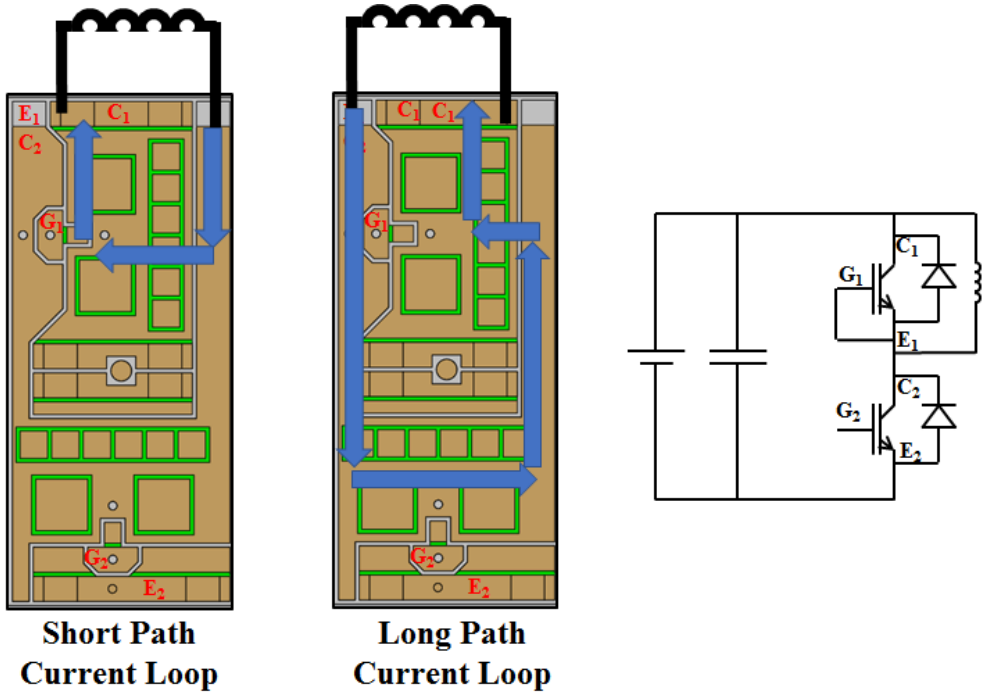
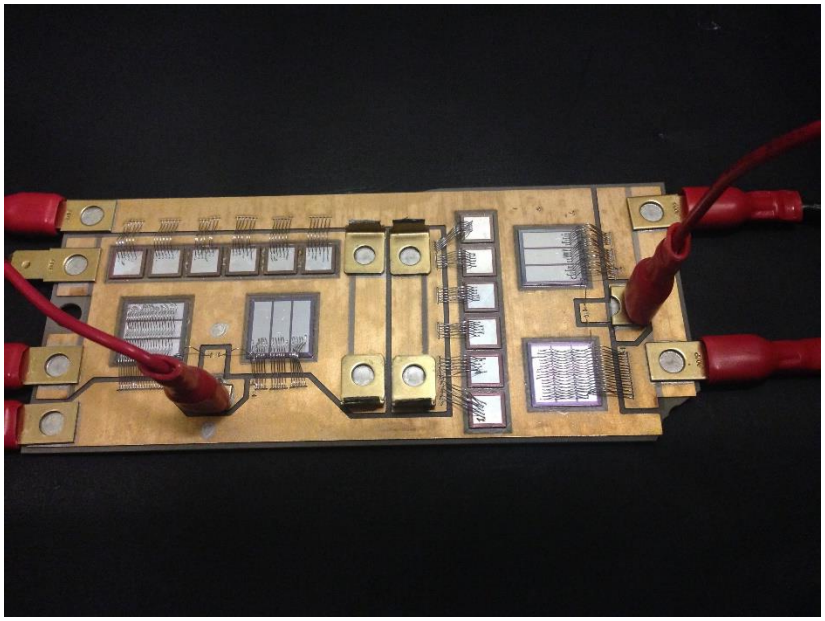


Fig. 7.25 Circuit configuration for long and short current paths for repetitive clamped inductive switching test.



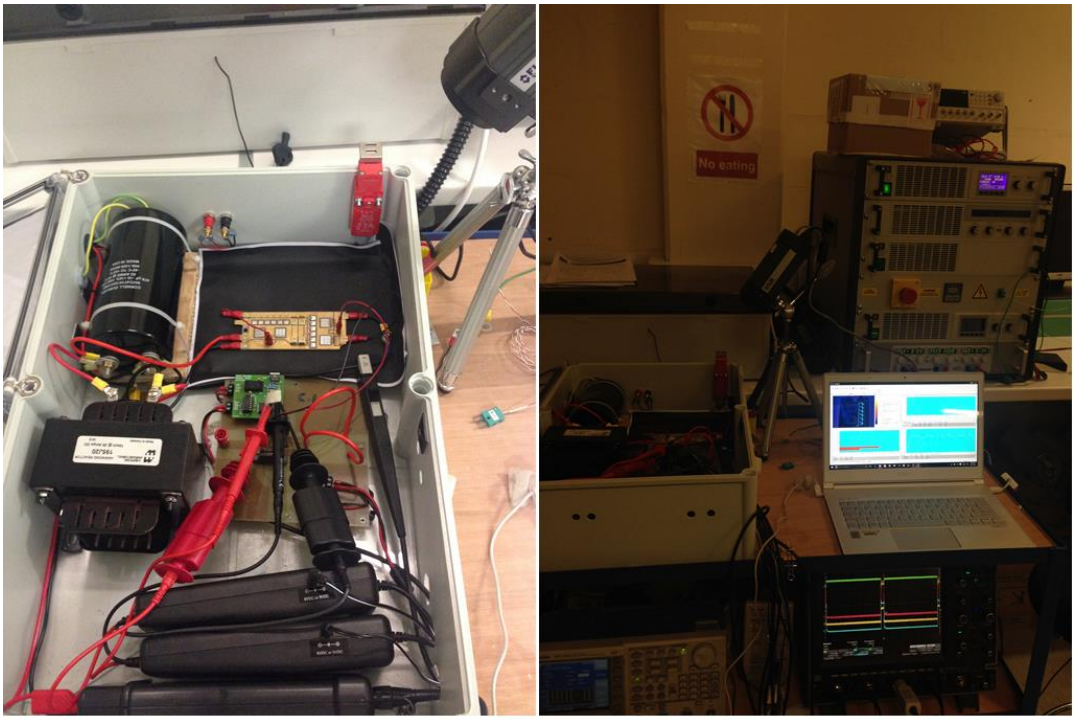


Fig. 7.26 Test rig setup for repetitive clamped inductive switching test.

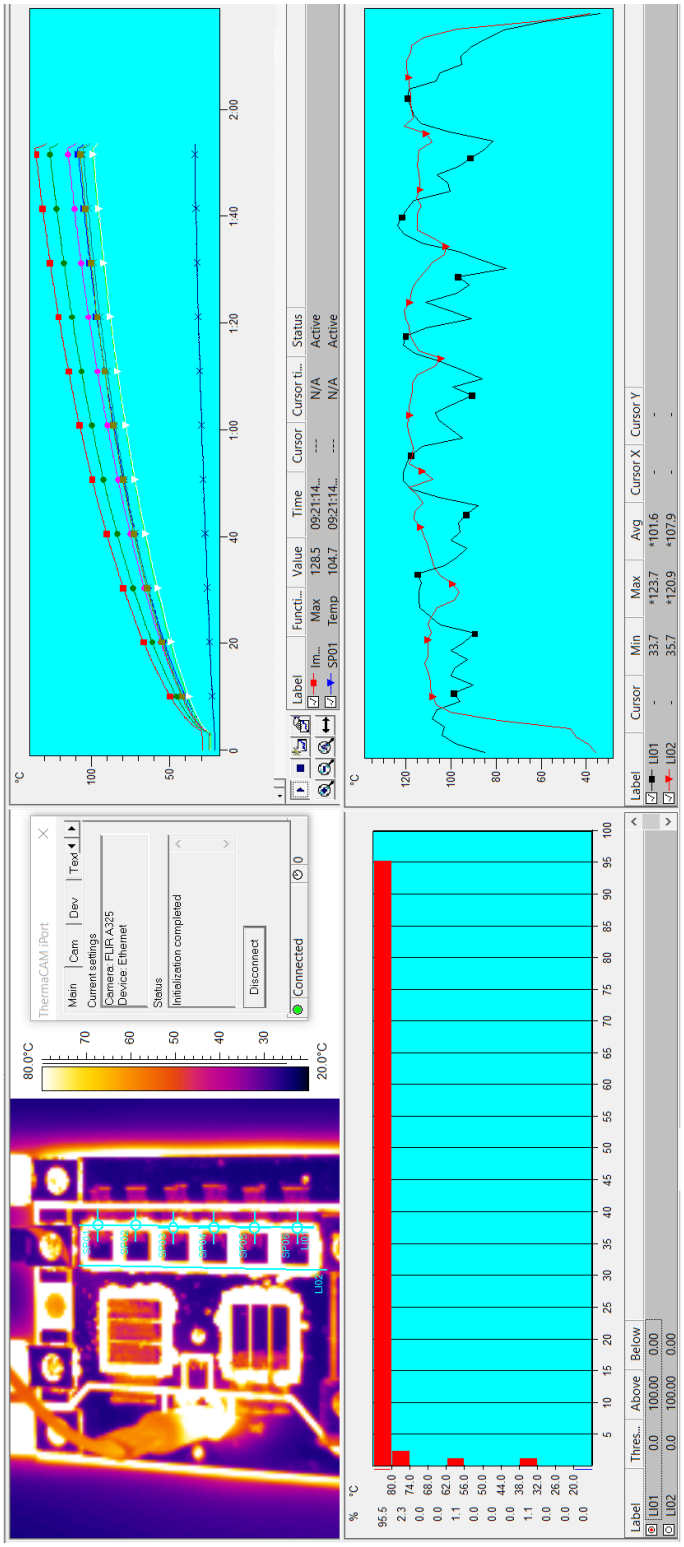


Fig. 7.27 Temperature imbalance for the long path current loop test.

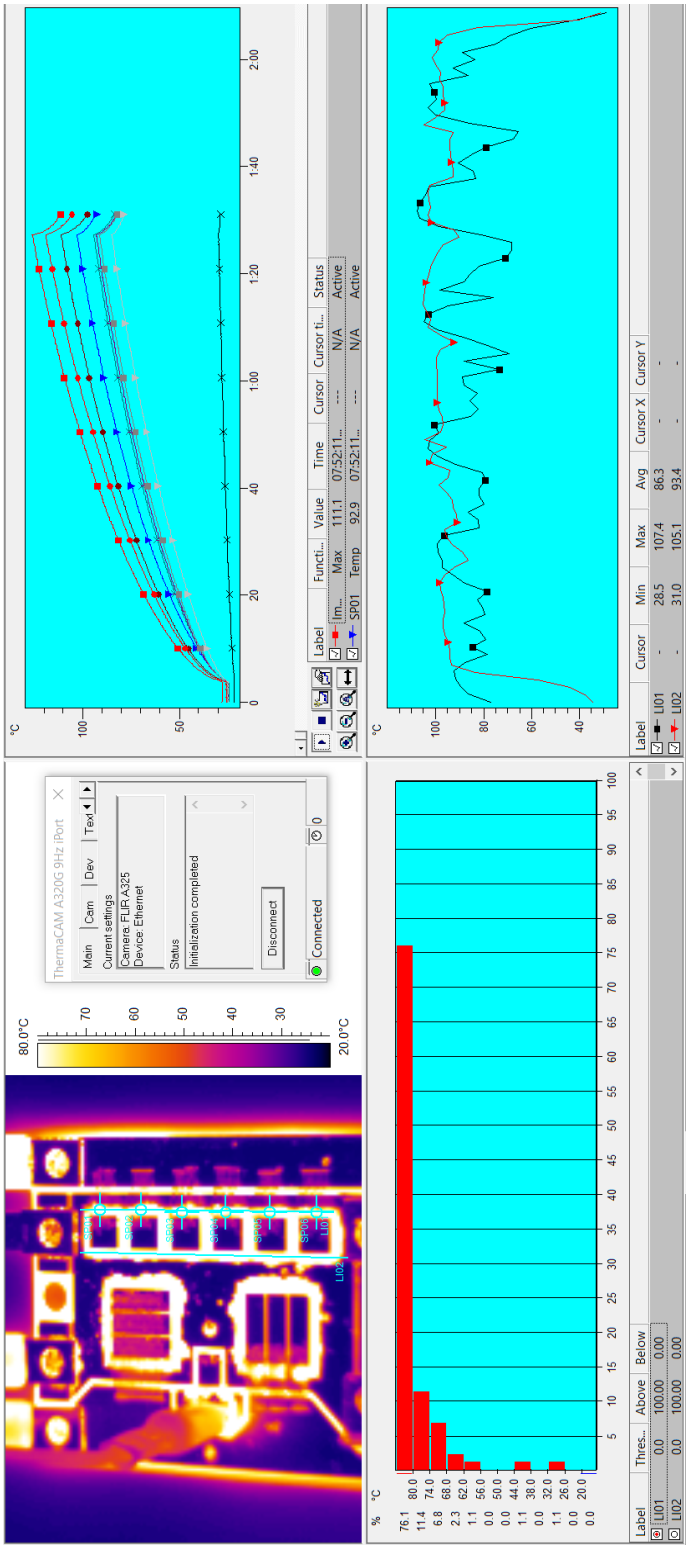


Fig. 7.28 Temperature imbalance during for the small current loop test.

Fig. 7.27 shows the temperature imbalance for the long current path loop test. The heat generated in the diodes are due to conduction of current in the diodes during the turn-off of the IGBTs and during the reverse recovery of the diodes during turn-on of the IGBTs. As can be seen, the temperature of the device located at the top side (having the longest parasitic inductance) is lower than the temperature of the device located at the bottom side (having a shorter parasitic inductance). This is due to the fact that the device with the longer current path, switches on slower than the device with a shorter current path taking less current during the turn-on of the diodes. During the turn-off of the diode, the reverse recovery happens at a faster rate as there is less current to be extracted from the device. Consequently, the temperature of this device becomes smaller. The temperature difference between these two devices are approximately 10°C at the end of the test with the hotter device at 110°C and the cooler device at 100°C. It is worthwhile to mention that the devices were not cooled during this operation and hence, the test was stopped when the temperature of the hottest spot on the sample were reaching 125°C. The DC link voltage was set to 80V and the peak current during the switching was 30A. Fig. 7.28 shows the temperature imbalance for the short current path loop test. The results indicate that the temperature rise was smaller in comparison to the test with the longer current path. During this test the temperature of the hottest device was 100°C while the temperature of the cooler device was approximately 90°C.

7.5 Prototyping a Double Side Cooling Power Inverter

Prototyping of the second automotive power inverter was carried out to improve the reliability and increase the thermal performance of the power electronic devices. Hence, a double sided cooling power inverter was designed and developed. As explained earlier in Section 1.4.2.1, one of the most common failure modes of power modules due to electro-thermal stress and fatigue is wire bond lift-off. Hence, in this design, this failure mode was eliminated by using double side solderable dies from International Rectifier (now Infineon). These devices have a trademark brand of CooliRIGBT and CooliRDiode with part numbers of AUIRGM765C1N0 and AUIRDM7V1CC10 respectively. Both diodes and IGBTs are rated at 680V with nominal current of 310A. The nominal power rating of the three phase inverter designed based on these dies is 210 kW. However, at higher temperature and with the DC voltage of 350V, this inverter is capable of driving a 90kW electric machine depending of the temperature of the coolant, the current can be increased.

The IGBT die size is 11.5×12.5 mm^2 and total active die area is 123 mm^2. The thickness of the die is 70µm and the maximum operation of the die is limited to 175°C. The die size of the diode is 11.5×8.269 mm^2 and the total active die area is 78.1 mm^2. The thickness of the die is 75µm. The metallisation of these dies are silver alloy for solder attach and hence, no wire bonding is possible. The dies are specifically designed

to be mounted and sandwiched between two layer of DBC substrates and hence can be cooled from both sides. Because the thickness of the diode and IGBT are not precisely equal, in order to achieve a good contact between the devices and the DBC substrates, it is important to have a uniform die attach between the diode and IGBTs to the DBC substrate with to make the height of the dies equal.

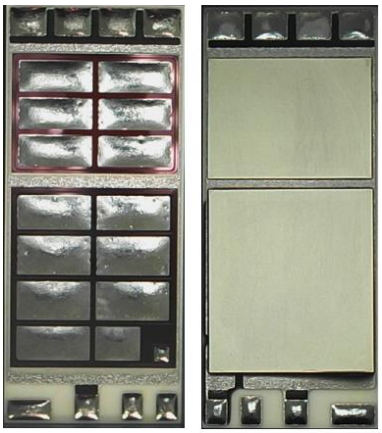


Fig. 7.29 Flip-die and die-up configurations.

The process starts from silver sintering one IGBT and diode on top of an Al_2O_3 DBC substrate with 200µm Cu on top and bottom side and ceramic thickness of 380µm. This increases the reliability and lifetime of the device. The IGBT/diode pair devices can be mounted on this substrate in two configurations: die-up and flip-die configuration. By putting these two configurations next to each other, a leg of an inverter is achieved. Fig. 7.29 shows this two configurations. A die up configuration comes with a pre-applied solder pads on the device surface. This is to make sure that the height of the IGBT/diode pairs are equal.

The layout of this DBC substrates for these two configurations are shown in Fig. 7.30. The second substrate (which is the main DBC substrate) was designed in a way that these two configurations are put next to each other to form a half-bridge. The layout of the second DBC substrate is shown in Fig. 7.31.

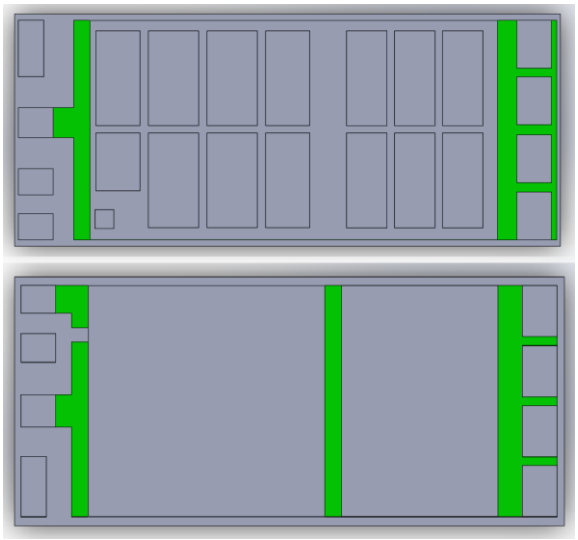


Fig. 7.30 Flip die and die-up DBC substrate layout design.

In the next stage, the die-up and flip-die configurations are soldered to the main DBC substrate shown in Fig. 7.31. As shown, the bottom side DBC substrate is the same size as an iPhone 4. The solder type and soldering profile in the ATV reflow chamber is the same specified in Section 6.2.1. The green colour shown in Fig. 7.31 is a high temperature solder stop which prevents solder from flowing during the reflow process.

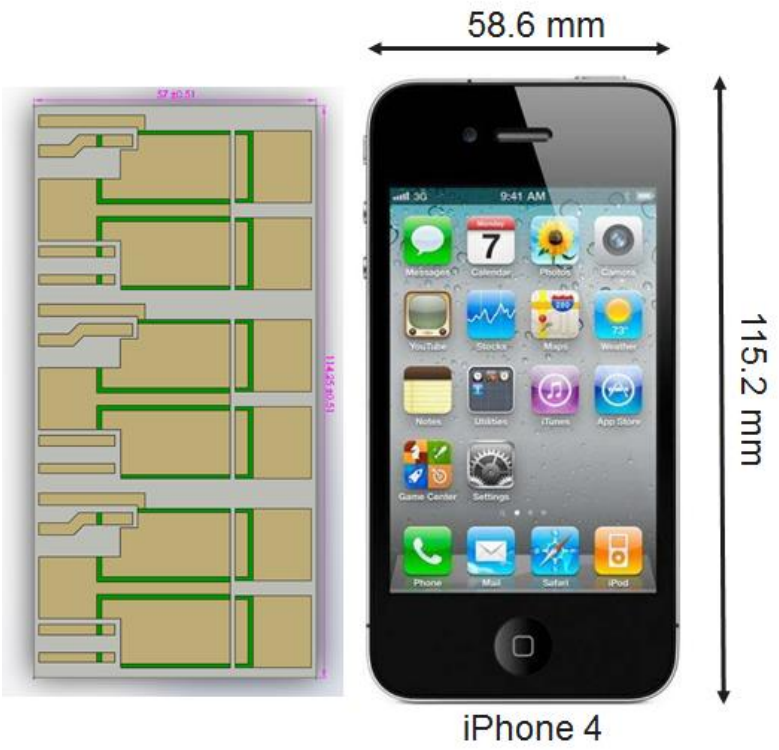


Fig. 7.31 Bottom side DBC layout design of a 3-phase double sided cooled inverter.

The stencil for applying solder paste was designed with different pad sizes (10%, 15%, and 20% smaller pad area than the area of the die. The thickness of the stencil was 6 thou. During the soldering profile, except for the solder pad with 20% smaller footprint, all the other devices soldered using larger solder pads were short circuited due to excessive amount of solder. This was due to the fact that the die is very thin and hence, if the amount of solder is large enough to cause it to flow, the top and bottom side of the die becomes disconnected. In order to overcome this problem and increase the throughput of the process, a mask was designed and applied to the area shown in Fig. 7.32. X-Ray scanning was used to understand the cause of failure. In a nutshell,

the failure was caused by the flipped die version in which the solder was connecting the collector and the emitter of the device. Fig. 7.33, Fig. 7.34 and Fig. 7.35 show the X-Ray scanning image of the solder layer for 3 different soldering profiles. As can be seen, the amount of solder flowing was decreased and in the case of 20% smaller pad size, only the flipped die in the middle was soldered correctly. In order to improve the process, a photo resist solder mask was applied to the surface and the pad area where it needs to be exposed to solder was etched. Moreover, a stencil with larger pad area for the edges of the device was designed to improve the collector-emitter contacts.

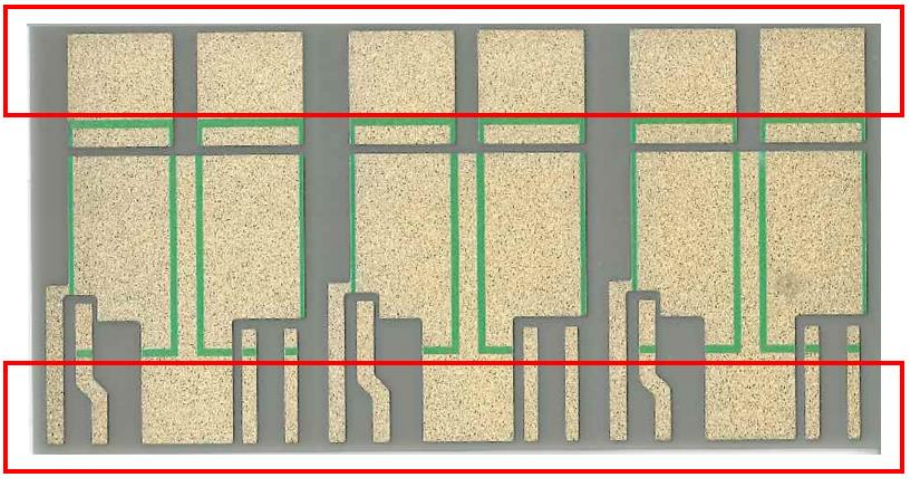


Fig. 7.32 DBC substrate and the area to apply solder mask.

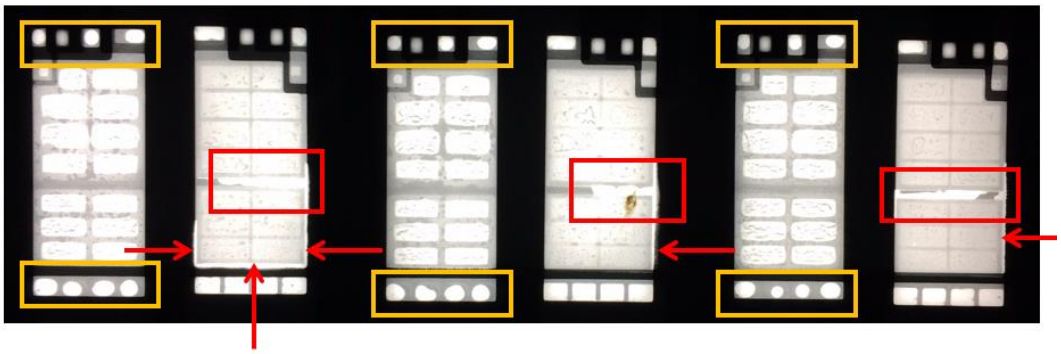


Fig. 7.33 X-Ray image of the solder layer with 10% smaller stencil size.

Fig. 7.34 X-Ray image of the solder layer with 15% smaller stencil size.

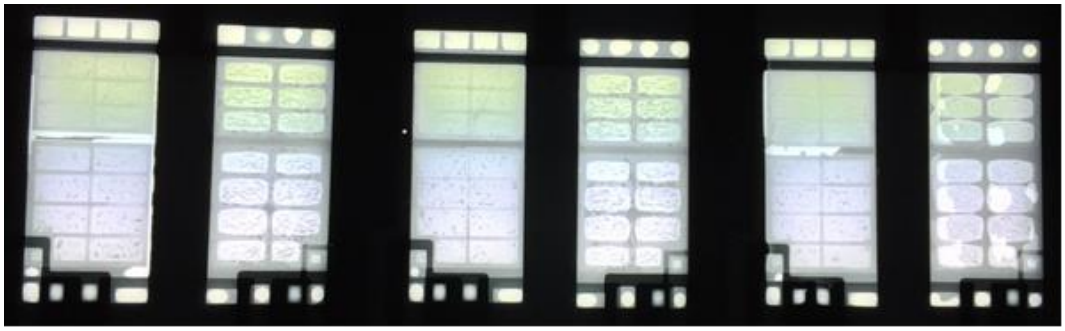


Fig. 7.35 X-Ray image of the solder layer with 20% smaller stencil size.

The next step, in order to reduce the risk of moisture entering the assembly and support the electric field under the IGBT and diode die, under-filling assembly process is carried out. The process involves pre baking at 100°C in order to dry out the moisture from the assembly, next the under-filling material is dispensed around the assembly

and it is cured. The under-filling material is Shin-Etsu SMC-375 TE-T12 from Japan and is in form of liquid which is dispensed using a needle and syringe.

Both top and bottom side DBC substrates are water cooled using circular pin fin baseplate. The bottom side baseplate material is made from Aluminium Silicon Carbide (AlSiC) which has a superior thermal performance to aluminium baseplates and it is lighter than copper baseplate. The material properties of AlSiC-9 is shown in Table 7.3.

Table 7.3 Material properties of AlSiC-9.

Aluminum Alloy A356.2	37% Vol.
Silicon Carbide (electronic grade)	63% Vol.
Density	3.01 g/cm^3
Thermal conductivity	200 W/m.K
Specific heat at 25°C	0.741 (J/g.K)
Coefficient of thermal expansion	7 /°K
Young's modulus	188 GPa
Shear modulus	76 GPa
Strength	488 MPa
Electrical Resistance	20.7 μΩ/cm

As can be seen, the CTE of AlSiC is very close to Alumina, AlN and Si in comparison to Al and Cu and hence it is significantly better than the conventional baseplate materials. This improves the lifetime to failure of the device under thermal cycling. Moreover, the thermal conductivity of this material is similar to AlN and hence, the heat exchange is very high for this design. Fig. 7.36 and Fig. 7.37 show the bottom and top side cooling system respectively. In order to create a free space for the connectors and also provide a clearance between the top side and the cooling system and moreover, create a thermal capacitance to damp the thermal transients, on top of each device a bump is designed which sits on the top side of the device. The bottom side

baseplate is soldered to the DBC substrate and the top side is attached using a thermal pad. The low thermal conductivity of the top side is the bottleneck in the heat exchange for the top side.

The height of the pin fins are set to be 3 mm. This is limited by the manufacturing process of AlSiC baseplate. The radius of the bottom of pin fins are 1 mm. This was limited by the minimum clearance specified by the manufacturing process. The area exposed to the coolant was optimised and maximised according to the process and is 14523.96 mm^2.

Fig. 7.38 shows the exploded view of the power inverter while Fig. 7.39 shows the final product after assembly is finished.

The clamped inductive switching test was carried out on the power inverter under low current and low voltage and the switching waveforms of the device was captured at various temperatures. Fig. 7.40 and Fig. 7.41 show the results obtained when the test was carried out with 15V DC voltage and 1.5A forward current at 25°C, 75°C and 125°C. The results indicate that the turn on voltage and current waveforms are not sensitive to the temperature and the rate of switching is not affected during the turn-on transients for both die-up and flip-die configurations. However, the turn-off transients are highly temperature dependent. As can be seen, the turn-off current and voltage gradients (*dI/dt* and *dV/dt*) become significantly smaller at elevated temperatures. Moreover, the results show that the die-up configuration is more temperature sensitive. Hence, the cooling system for the die-up configuration which is at the bottom DBC is

designed with AlSiC material in order to have a better heat exchange rate. This is due to the fact that the gate resistance and parasitic inductance is significantly smaller than the flip-die configuration, hence, the change in the switching speed of the complementing diode due to increasing temperature, can affect the turn-off speed of the IGBT in this configuration. Moreover, the results show that the Kelvin inductance of the IGBT is small and hence, the impact of temperature rise in the turn-on of the IGBT is negligible.

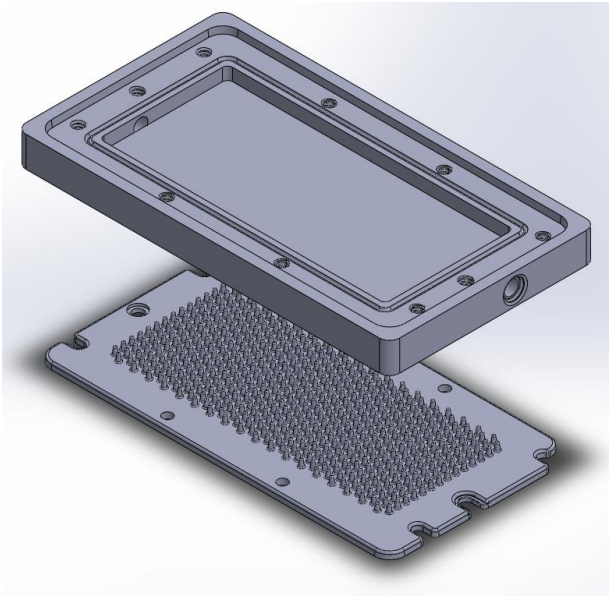


Fig. 7.36 Bottom side AlSiC baseplate with pin fin and Al cold-plate with water inlet and outlet.

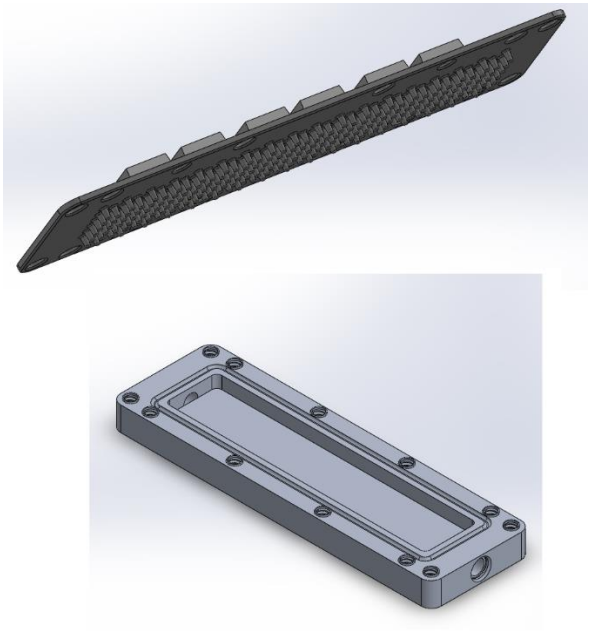


Fig. 7.37 Top side baseplate and coldplate.

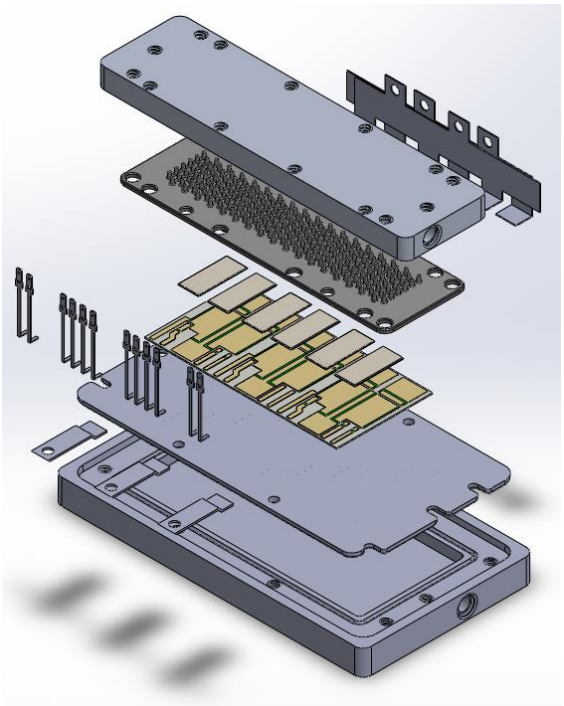


Fig. 7.38 Packaging process of the double side cooling power inverter prototype.

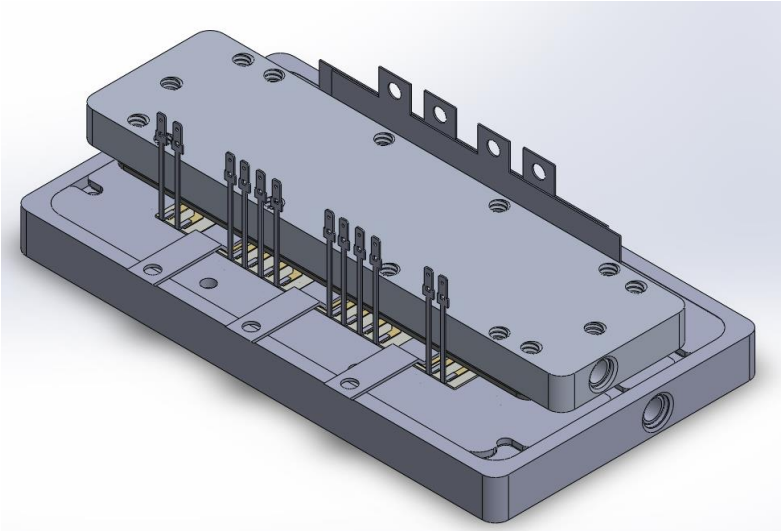


Fig. 7.39 Assembled power inverter prototype.

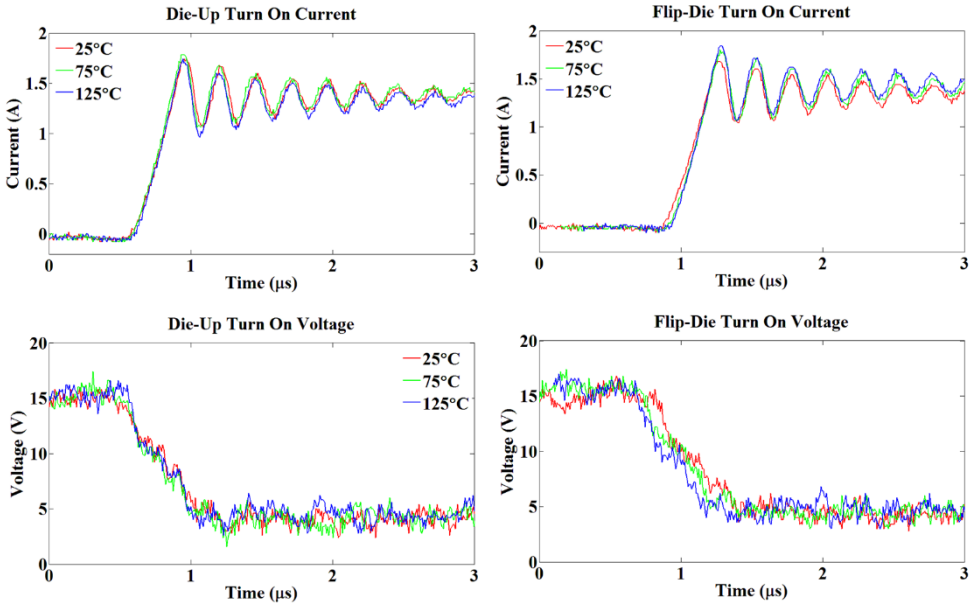


Fig. 7.40 Turn-on voltage and current waveforms of die-up and flip-die configuration at different temperatures.

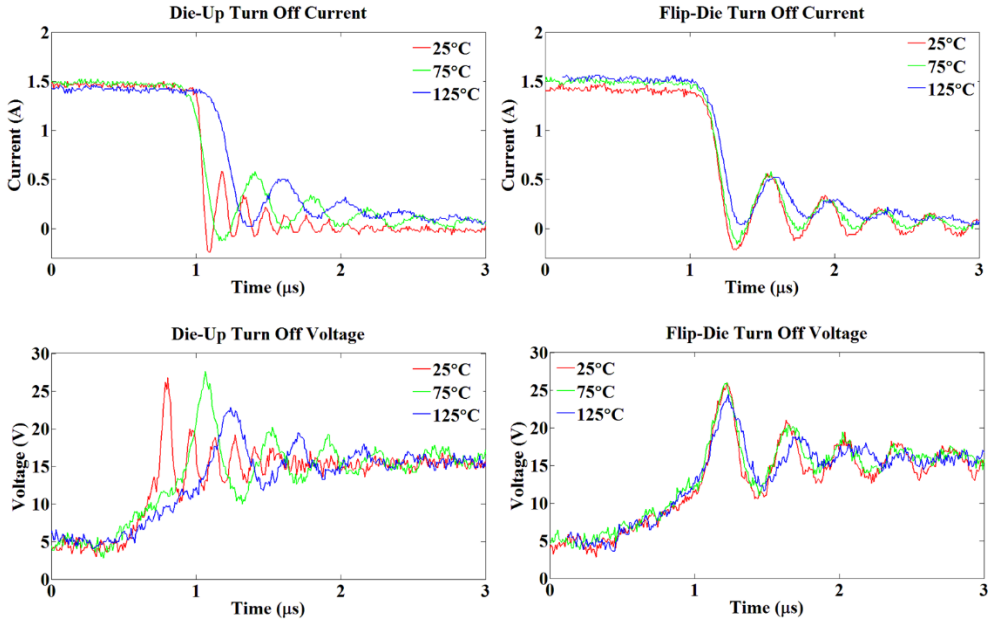


Fig. 7.41 Turn-off voltage and current waveforms of die-up and flip-die configuration at different temperatures.

Chapter

8 Conclusion and Suggestions for Future Work

8.1 Conclusions

Power electronic devices are used in automotive application to provide a bidirectional power conversion between the eMachine and the battery. Modelling power electronic devices in an inverter is an important phase of designing a high performance power inverter with high level of reliability that is required in automotive industry. The foundation of performance of power inverter relies on the switching and conduction behaviour of the devices and the heat management in the power inverter. Moreover, understanding the physics of failure in power electronic devices under variable load in automotive application is an essential in the design phase of power inverters for EDUs for an FMEA engineer.

The power semiconductor devices used in automotive are mostly IGBTs and PiN diodes and recently with advancement in the field of semiconductor and increased demand in high performance power electronic devices, SiC MOSFETs and Schottky diodes are developed and will be used in the near future in the automotive industry.

The switching transient of IGBTs, PiN diodes, BJTs, SiC MOSFETs has been studied and models with high fidelity was developed in Matlab/Simulink environment which is a well-established modelling environment in the automotive industry. The developed models were based on the physics of the semiconductor and they captured the behaviour of the devices and interaction between different components and power electronic devices in the circuit during the power conversion. The models were used to investigate some of the reliability aspects of power electronic devices such as the BJT latch-up of SiC MOSFET during the reverse recovery of the PiN body diode of the MOSFET, parasitic gate turn-on (shoot-through phenomenon) and parasitic gate turn-off of SiC MOSFET and failure of the device due to unbalanced current sharing of the parallel connected IGBTs. Rise in the junction temperature of the device during operation is one of the main parameters that brings about these failure modes. Hence, in order to model the abovementioned reliability aspects, rather than using the quasi-static temperature dependent parameters of the devices, the transient junction temperature was used to take the temperature dependant parameters into account.

The fast and compact electro-thermal model for power electronic devices were used to show the BJT latch-up in SiC MOSFET and CoolMOS during body diode reverse recovery of these devices. The PiN diode model for SiC MOSFET and CoolMOS were

developed by reconstructing the ADE in the drift region. In case of SiC MOSFET, holes were the minority carriers and in case of CoolMOS, electrons were the minority carriers in the P-pillar and holes were minority carriers in the N-pillars. In order to model the parasitic BJT within the MOSFETs, the Ebers-Moll BJT model was used. The latch-up of the BJT and the thermal runaway consequence of this latch-up was simulated by calculating the junction temperature of the device at each time step and feeding the temperature back to the Cauer-thermal network of the device. This way, a positive feedback loop of temperature was formed which could show the behaviour of the device during the thermal runaway.

The shoot-through (cross talk) phenomenon was simulated by creating a non-linear and voltage dependent Miller capacitor for the IGBTs. As explained earlier, this phenomenon is due to unintentional turn-on of the complementing IGBT due to high *dI/dt* and *dV/dt* during the switching. The two slopes of the voltage as well as the peak of the shoot-through current was simulated by using the same physics-based device models. Moreover, the impact of temperature in increasing the probability of cross talk due to reduction of threshold voltage and increase of MOS transconductance, increase of carrier mobility and carrier lifetime within the device was investigated. It was shown that this phenomenon gets worse at higher temperatures and may lead to thermal runaway of the devices. Moreover, mitigation methods were investigated and it was shown that by applying negative gate bias this effect can be reduced. However, at higher temperatures, still cross-talk may occur. Moreover, it was discussed that this phenomenon becomes worse for SiC MOSFET as the threshold voltage of the device is

significantly smaller than that of the IGBT. Also, due to the impurities and defects in the gate oxide, applying very high negative gate bias is not possible for some of the SiC MOSFETs.

The parasitic induced gate turn-off of SiC MOSFET switching with complementing PiN diodes were also investigated through experiments and were modelled using the compact electro-thermal models. It was shown through experiments that this parasitic gate turn-off can have destructive consequences. The key parameters that can trigger this phenomenon were investigated and pinpointed: temperature, switching rate, supply voltage and forward current. It was also shown that the overshoot voltage of the SiC MOSFET during the parasitic turn-off and the voltage oscillations arising from this phenomenon, is a significant reliability concern for the high performance SiC MOSFETs. In addition, it was discussed that this phenomenon is not only limited to the Si PiN diode but also it can happen when the body diode of the SiC MOSFET or even a discrete SiC PiN diode were used as a freewheeling diode.

It was discussed as the power density of inverter and required current for driving the electric motor increases, paralleling devices becomes a common practice in power inverters. It was shown that if the devices are not switching at the same rate and there are some imbalance between the parallel connected devices, the current is not shared equally between the devices. This leads to non-uniform stress between the devices and can become a reliability issue. Hence a model was developed to simulate the impact of current imbalance. This model can be used to investigate the non-uniform degradation

of devices or reliability issues arising from solder delamination or gate wire bond degradation in individual devices in a module.

In addition to the modelling and simulation, 3 different power modules were packaged using conventional packaging techniques. The first power module was SiC based and the impact of number of wire bonds on the switching performance of the MOSFET was investigated. The results showed that the by increasing the number of wire bonds, the overshoot in the voltage was slightly reduced. Moreover, the parasitic induced gate turn-off was investigated by packaging a power MOSFET and using it under clamped inductive switching. During this experiment, the body diode of the MOSFET was used as a freewheeling diode. The results showed that this phenomenon is not limited to the switching of the MOSFET with a Si PiN diode. Moreover, the results further confirmed that the gate turn-off happens at higher temperatures.

The second power module was developed to investigate the impact of current loop length on the switching performance of the devices and current sharing imbalance between the parallel connected IGBTs and PiN diodes. The results showed that by increasing the current loop, the devices with a longer current path, takes less current initially and during the turn-off, it shows a smaller reverse recovery. Hence the heat generated in this device is smaller than the heat generated in the device with a longer current loop. Moreover, the results showed that there thermal stress is different between these two devices and this can be a reliability issue. Furthermore, FEM was used to calculate the parasitic inductance due to the layout of the DBC substrate

designed for this inverter and the parasitic inductance of each wire bond was also calculated.

The third power module was made to enhance the cooling of a 3-phase automotive power inverter and increase the power density of the inverter. This is becoming more important in the automotive industry where weight and size is a constraint in the vehicle. The design was using a double sided cooling strategy. Moreover, the Cu baseplate was removed and the DBC substrates were directly attached to the pin fin cooling system. The material used was carefully selected to reduce the thermal stress due to mismatch between the coefficient of thermal expansion and it was tried to use materials with high thermal conductivity. Hence, AlSiC baseplate with a high thermal conduction and close CTE to Si was used. The CTE of AlSiC is even closer to SiC and hence, it can be used for SiC power modules with high temperature applications. The power devices used were designed to have two different configurations (die-up and flip-die). Hence, the current loop was reduced as the current could easily commutate between the top and bottom side power devices.

Findings in this thesis can be used for power inverter design engineers and they can assist them to investigate the impact of different physical parameters of the devices in order to achieve the highest performance, increase the reliability and predict the fault under different conditions. The models are compact and can be used in different circuit topologies to investigate the switching transient and current commutation between different components in the circuit. Moreover, the models are all developed in MATLAB/Simulink and can be integrated with other models developed in this

environment such as the high fidelity battery and motor models and the switching of the devices can be controlled using the control strategies and pulse generators built in Simulink environment. Moreover, as the models are compact and fast, they can be used with a built-in Cauer-thermal network which have higher simulation time constant and this can result in a fast electro-thermal simulation for the inverter.

8.2 Suggestions for Further Work

The reliability aspects investigated in this work are not the only problems existing in the power inverters used in an automotive application. However, the proposed models can be used to investigate other aspects such as electro-thermal modelling of power inverters, lifetime prediction, unclamped inductive switching condition and avalanche performance of single and parallel connected SiC MOSFETs and IGBTs and comparison of current sharing between parallel connected PiN diodes and Schottky diodes.

8.2.1 Electro-Thermal Modelling of Inverter

The model can be used to extract the heat generated in the devices and to create lookup table of losses. Using the loss lookup tables, the junction temperature of the devices can be calculated using fast modelling environment such as PLECS or PSIM. The models then can be used to optimise the cooling system designs for the inverter and even model at the vehicle level. Furthermore, as the need for integration of power

electronics into eMachines are increasing, the proposed models can be used in conjunction with electric machine models and thermal network of electric machines which take the AC losses and the core losses into consideration and hence, a compact electro-thermal model for electric machine and power electronics can be created.

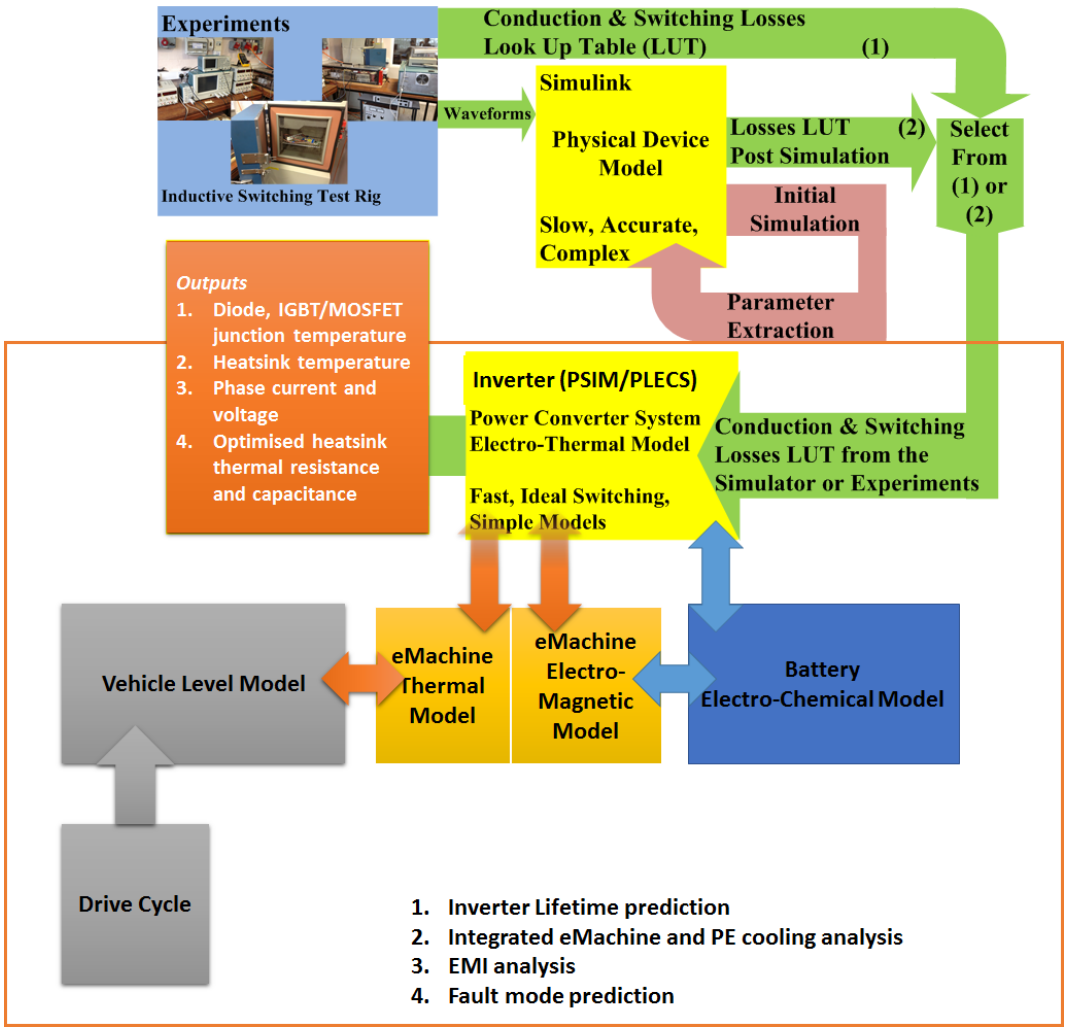


Fig. 8.1 Modelling block diagram

Fig. 8.1 shows the modelling block diagram proposed to optimise the thermal performance of the power inverter. The lifetime prediction of the inverter can be carried

out by mapping the losses and junction temperature rise of the device during drive cycle of the vehicle using Coffin-Manson accelerated temperature cycle model.

Furthermore, the MOSFET model developed can be used to model parallel connected SiC MOSFETs in high voltage applications such as racing cars for Formula-E or high performance supercars which are already using SiC based power inverters such as hybrid Mclaren. The same model can be used for low voltage 48V inverters used in HEVs with e-creep and e-launch capability which requires very high current at low voltage.

8.2.2 Testing the Double-Sided Cooled Inverter

The double sided cooling power inverter was made and the switching characteristic of the die-up and flip-die configurations were tested. In order to evaluate the cooling performance of this power module, it needs to be tested under full power. A back-to-back inverter circuit may be used along with hysteresis current control. Using this method, two identical inverters are required. One of them is used as an inverter and the second inverter is used as an active load. Only the power losses are fed to the circuit and hence, a smaller rate power supply is required to provide the current for the circuit. A three phase inductive load needs to be used between the two inverters. In order to obtain a realistic temperature rise within the power inverter, a drive cycle can be used and hence, the current of the inverter can be controlled to replicate the current that is required from the inverter during a drive cycle based on the torque request.

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Appendix

A. Introduction to different types of HEVs

Mild HEV are the least electrified type of vehicle in which a conventional combustion engine is utilised as the propulsion system, this is augmented by a larger starter motor which can be used as a generator and it is also equipped with a battery pack which can be charged by the motor. The starter motor is also known as integrated starter generator or belted alternator starter. This starter motor may be used as in idle stop mode of the vehicle which switches off the combustion engine when the vehicle is idle. In addition, during the high load on the engine, it assists the engine and enhances the overall performance of the vehicle (torque filling). While the engine is under low load, i.e. when the wheels are spinning freely, the starter charges the batteries. Most of the new premium vehicles are equipped with this technology which in return reduces the emissions of the vehicle. Fig. A.1 summarises the mild hybrid vehicle powertrain in a simple schematic.

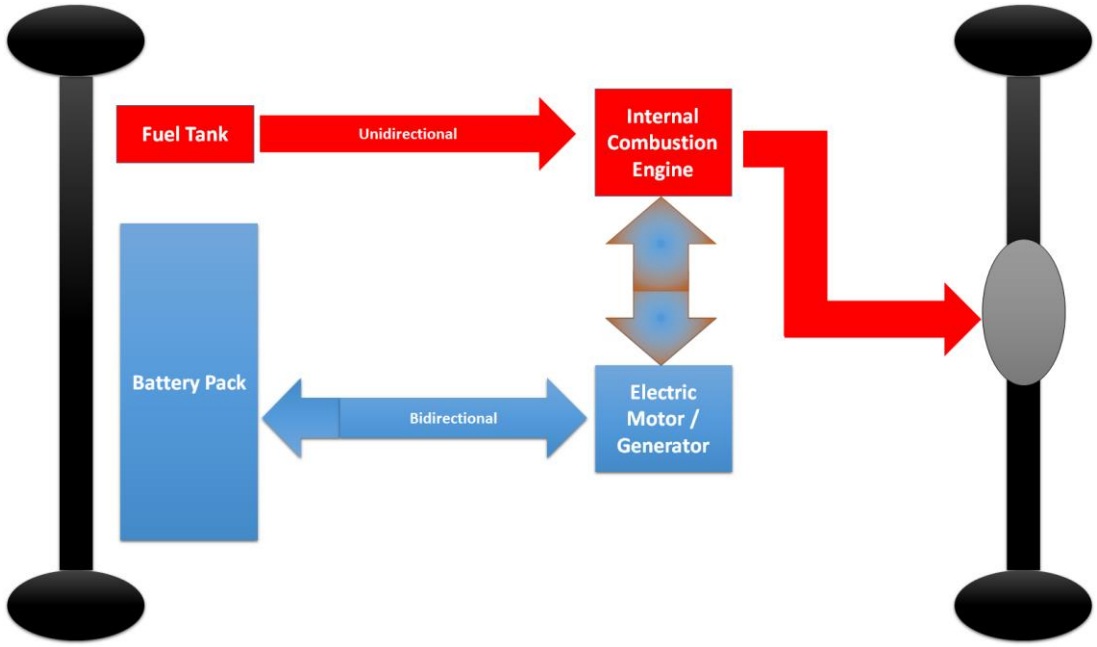

Fig. A.1 Block diagram of a mild hybrid vehicle architecture.

In case of series hybrid electric vehicles, there is a single path to the wheels (or differentials in the case of rear wheel drive vehicles). Consequently, the fuel is used in the combustion engine which in return rotates the shaft of the generator and keeps the batteries charged and the electric power coming from the battery is transferred to the electric motor and the motor rotation is transferred to the transmission. Some cars use direct coupling to the wheels rather than using the transmission. The electric motor in this configuration can also be used as a generator to charge the batteries during regenerative braking or under low motor load. A simple block diagram showing the architecture of a series hybrid electric vehicle is illustrated in Fig. A.2.

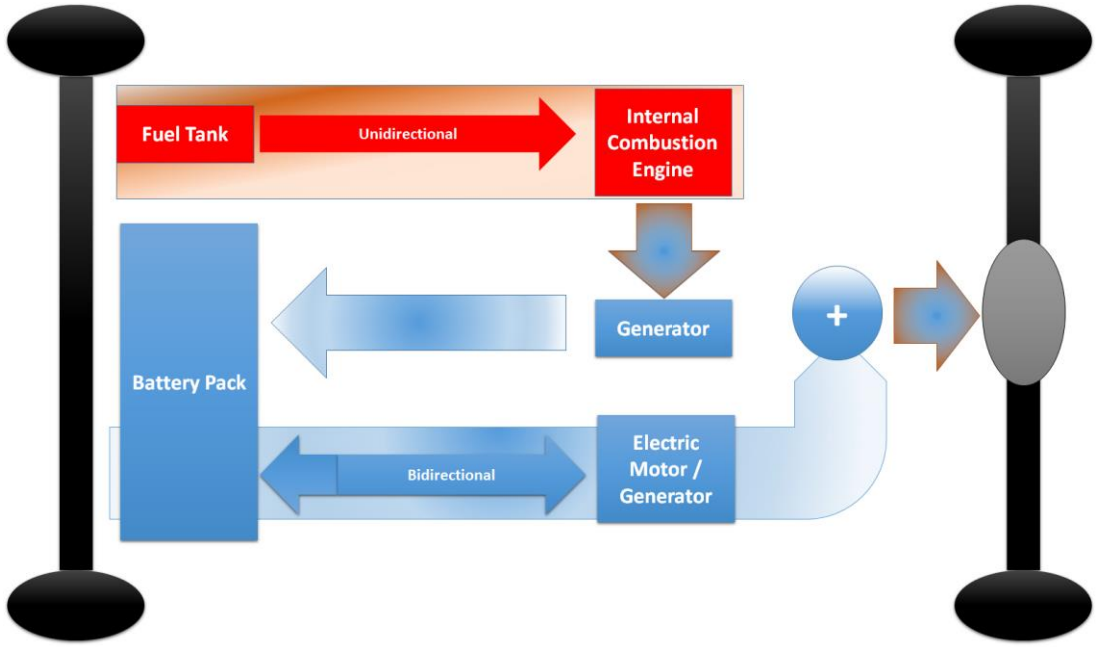

Fig. A.2 Block diagram of a series hybrid vehicle architecture.

In contrast to the series hybrid electric vehicle architecture, parallel HEVs have two parallel paths of power transmission to the wheels. The first path transmits the rotational movements of the combustion engine to the wheels and the second transmission path belongs to the electrical motor. This configuration enables the power to be transferred from either the electric or the combustion motors or from both at the same time. This configuration is more complex than the series hybrid electric vehicle. Fig. A.3 shows the block diagram of the parallel hybrid electric vehicle.

In the case of series-parallel hybrid electric vehicle the combustion engine and the electric motor are coupled using a gearing or power split which couples the power sources and enables charging of the batteries via the combustion engine.

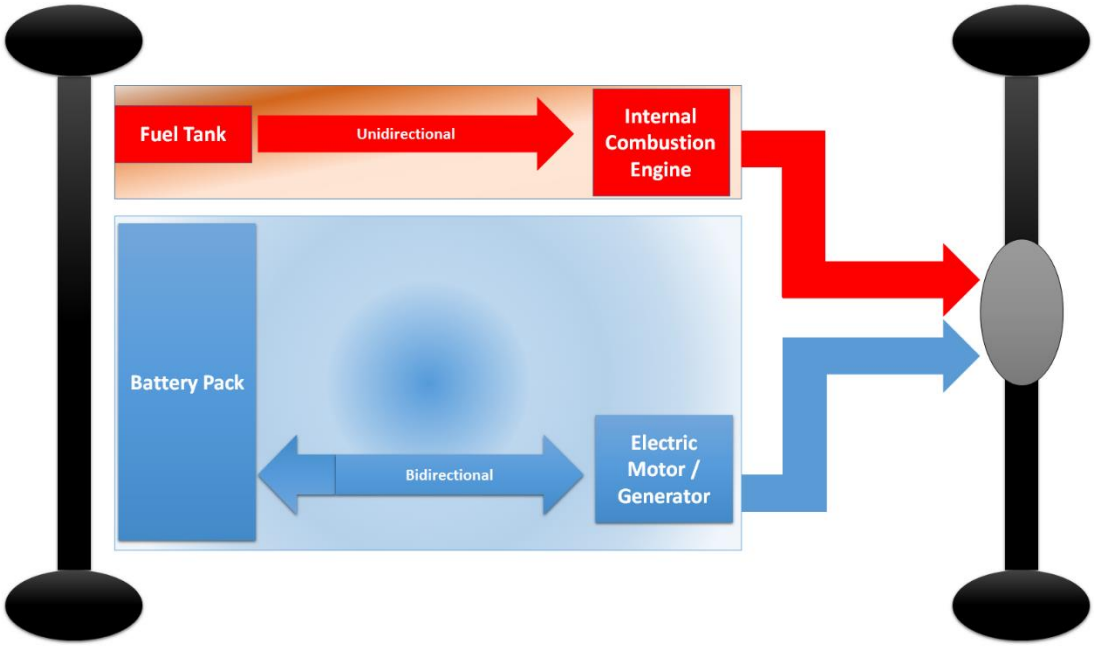

Fig. A.3 Block diagram of a parallel hybrid electric vehicle architecture.

This type of system is considered to be a complex hybrid classifications of hybrid electric vehicles and vehicles such as Toyota Prius and Ford Escape Hybrid are some examples of this system. Fig. A.4 shows a block diagram of a series-parallel hybrid electric vehicle architecture.

The PHEV architecture is similar to the HEV, but it has the capability of being plugged-in to the electricity grid to charge the larger sized battery packs. The capacity of the battery determines the all-electric range of the vehicle. Fig. A.5 shows a schematic of a hypothetical PHEV architecture.

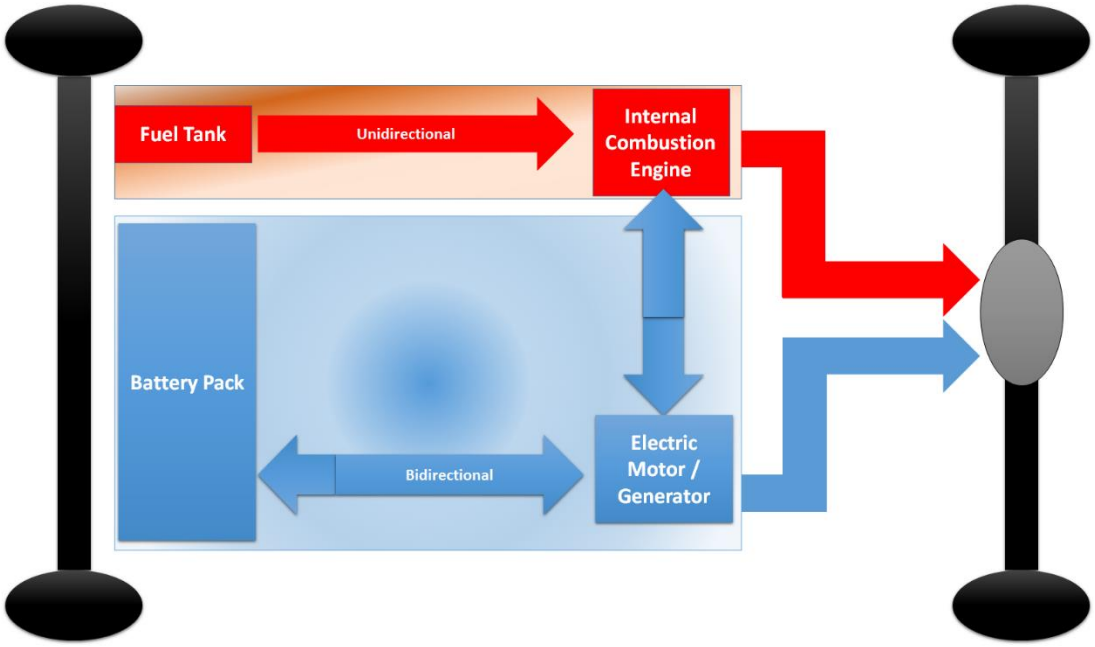

Fig. A.4 Block diagram of a series-parallel hybrid electric vehicle architecture.

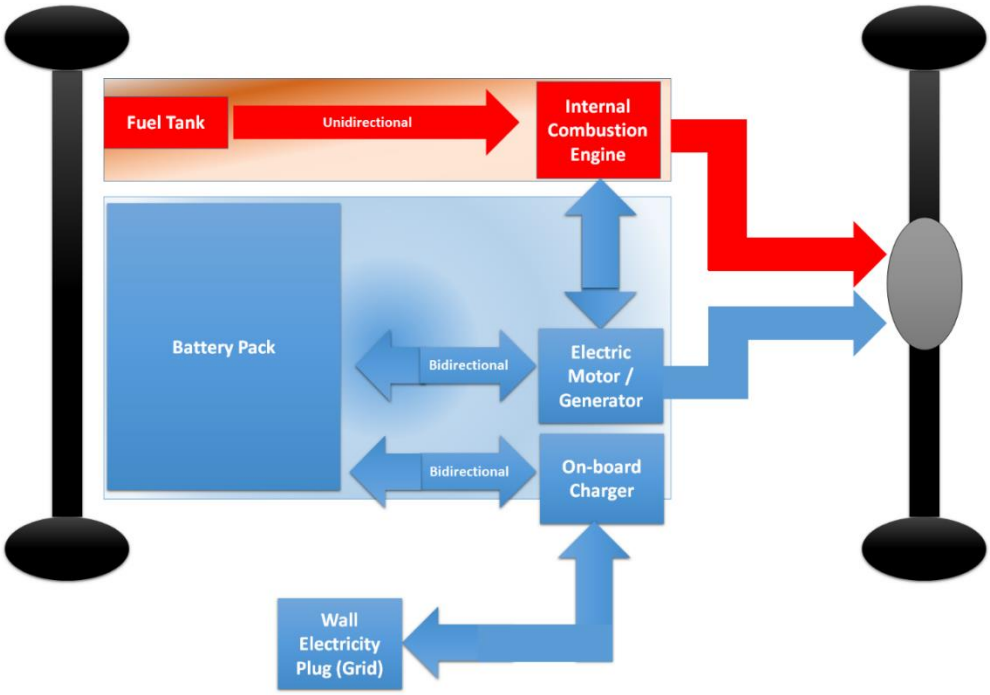

Fig. A.5 Block diagram of PHEV architecture.

B. SRM Inverter

The inverter drive for a switched reluctance motor has a different topology. Fig. B.1 illustrates a switched reluctance inverter. In this topology the three phase windings of the motor are connected between the two switches. In this circuit the windings are energised in sequence as the rotor salient pole approaches the stator tooth the energisation starts.

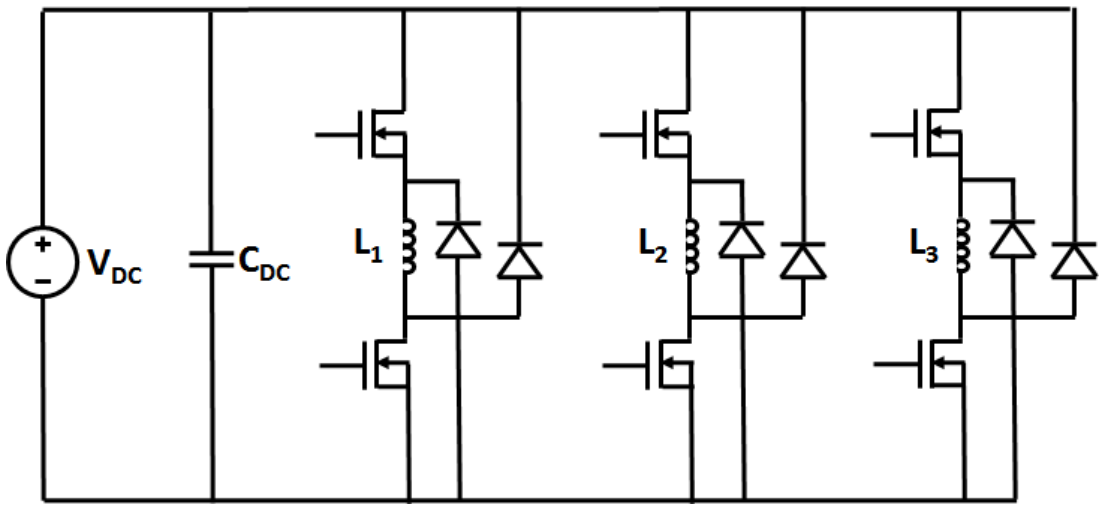

Fig. B.1 Switched reluctance motor drive topology.

The maximum torque is achieved as the centre of the rotor pole becomes aligned with the centre of the stator tooth. At this point the switches are turned-off and the next pole switches on and grabs the next pole and causes the motor to rotate. Due to sudden release of the stator pole by turning off the current during the alignment of the stator pole and the rotor tooth at the highest point that the torque is obtained, this kind of machine suffers from high torque ripples and high acoustic noise. This is due to the

very large axial force created by the sudden change of the magnetic flux during the switching which causes deformation of the stator's back iron. Several design methods and control strategies can be used to reduce the torque ripple and the acoustic noise in these kind of machines such as forming the current into an appropriate shape to increase early rise in the torque or increasing the stiffness of the back iron which are out of the scope of this project.

C. Power Device Modelling

Behavioural models are models which are made by the engineers to replicate an experimental result obtained in real application. These models are often optimised for simulation speed however, they might lack accuracy when it comes to predict the behaviour of the devices within the system. An example of a behavioural model is considering the power device as an ideal switch. This is the simplest explanation of the behaviour of the device when the switch is on or off, but, it does not provide any information about the switching or conduction losses of the device and it cannot be used to predict the reliability of the device under hard commutation condition. But, due to the very simplistic assumption of the model, the model can be used for multiple switching devices within the circuit and the simulation can be carried out for a long period of time and this can be very useful when a system with many components are needed to be modelled and the detailed behaviour of each device is not needed [9].

The level of complexity of a device model can be increased by adding on-state, off-state and some switching characteristics to the model in order to increase the complexity of a model. An example for this can be considering a slope rather than a step

in modelling the switching behaviour of the devices from on-state to off-state or vice versa. This kind of models often combine the behaviour of the device with some simple physical expressions within the device such as adding a resistor in series with the switch to consider the conduction losses of the device [9].

Some micro-electronic simulation tools which are used for simulation and prototyping of analogue and mixed signal circuits found their way into power electronics world such as PSPICE. These models are based on physics of the device and they use physics-based equations of the electrical components with some assumptions to reduce the simulation time of the model. These models often consider assumptions about making certain parameters of the device into a lumped value. An example of this is assuming the on-state resistance of different sections of a diode into a lumped resistive value or assuming the carrier dynamics within a device and lumping them into discrete charges. These models provide more insight into the device behaviour, however, they lack accuracy when compared to Finite Element Models (FEM) [9].

FEM divides the power electronic device into finite number of elements and it solves the nonlinear physical equations of semiconductors for each of the elements. The nonlinearity of the physics-based equations for semiconductors are due to the dependency of the carrier density of each element in the device to the potential within the device. By adding the solution to the carrier density profile and potential at each points of the mesh point, single solution to the equations are obtained and the most accurate simulation results can be obtained by fine meshing the device which can be computationally heavy and time consuming [9]. An example of commercially available

FEM tool for power electronic devices is Atlas or Silvaco which can simulate the device in 2D or 3D. This tool is widely being used by device manufacturers to design and optimise the device performance by accurately modelling the behaviour of the device. For instance, during the design process of an IGBT with a target blocking voltage, carrier life time in the drift region, threshold voltage, carrier combination rate, conduction losses and etc. a trade-off between different parameters of the device such as doping of the drift region, thickness of each region, length of channel, oxide thickness and so on exists which can be optimised for the specific application. Device manufacturers often use such tools to validate the performance of the device prior to fabrication.

FEM is a very useful tool which can predict the behaviour of the device very accurately; however, interaction of the device with the other devices in the circuit is not practical using FEM as the simulation would become very time consuming.

Modelling a circuit compromising of several different power electronic devices such as parallel diodes, IGBTs/MOSFETs requires a modelling tool which does not sacrifice the accuracy and at the same time can provide a high simulation speed. Moreover, the thermal simulation of power electronic devices has a significantly higher time constant than the electrical time constant of the carriers within the device making it very difficult to simulate the thermal rise within the power inverter with multiple dies under operation using FEM.

The switching and conduction performance of power electronic devices change with temperature. When the device is under operation, during each switching transient

from on-state to off-state and vice versa and during the conduction of current through the device, power is dissipated in form of heat and the heat flows vertically in the device. As the temperature of the device rises, the temperature dependent parameters of the device such as threshold voltage, carrier mobility, carrier lifetime (in case of bipolar devices), carrier recombination rate, MOS transconductance (for MOSFET and IGBT devices), on-state resistance, saturation velocity of electrons and leakage current changes. Hence, dynamic temperature modelling of power electronics devices which can take these changes into consideration is of high interest to model the reliability of devices under operation at high temperatures. This can be achieved by calculating the temperature rise of the device from the conduction and switching losses and taking the dimension of the device and material properties of each layer of material into consideration. Finite elements and Computational Fluid Dynamic (CFD) tools can accurately calculate the properties of heat transfer in the device and model the cooling system of the power inverter as a function of space and time. However, the simulation time can be time consuming and computationally heavy. There are some behavioural thermal models which can be used to model the heat flow into the device by simplifying the thermal model of the device into lumped electrical components. Cauer thermal network and Foster thermal networks are examples of such methods which can be used to model the heat flow in the device [10]. The idea is that the inverter can be divided into several sub-sections. Next, the thermal resistance and thermal capacitance of each material are considered as a lumped values and are replaced by electrical resistances and electrical capacitances. The equivalent of the heat flow is electrical current and

voltage of each node in the circuit (thermal network) represents the temperature of that sub-section. The accuracy of the thermal network can be increased by increasing the number of sub-system and dividing it into more parts and there is a trade-off between the simulation time and the accuracy of the thermal model [10, 52].

D. Semiconductor Crystal

The solid state semiconductor used in power electronics are usually Silicon and more recently Silicon Carbide. Semiconductors used to fabricate power devices are in a form of highly ordered crystal lattice which are three dimensional repeating patterns of atoms connected to each other [98].

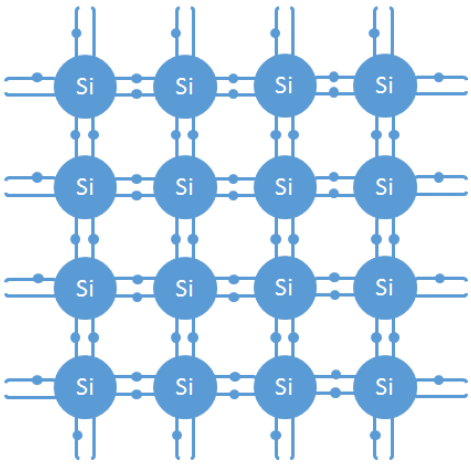

Fig. D.1 Intrinsic Silicon crystal structure.

Fig. D.1 shows an intrinsic Silicon crystal structure. Growing a crystalline Silicon is a similar procedure as growth of most crystals by cooling down a molten Silicon. Hence, a method for growing semiconductor is used which involves using a highly ordered crystal seed that is dipped from one end to the molten Silicon and the silicon crystal with a very high purity is grown in a cylindrical shape. This boule is then cut in

very thin layers which is called a “wafer” and it is used as a base material for Silicon-based device fabrication.

Energy Bands

Section 2.2.4, the energy band was briefly touched and Fig. 2.10 showed the energy band diagram. This section explains the physics behind the energy gap and introduces a very interesting characteristic of crystals which is used to calculate the fixed and mobile carriers in a semiconductor which will be used later on to calculate the current in power semiconductor devices.

The electrons which are in the outer shell of an atom are called valence electrons. As shown in section 3.2.1, silicon has 4 valence electrons which is one of the similarities that exists between silicon and carbon atoms. Carbon atom sits on top of silicon in Mendeleev’s periodic table. The silicon crystal has tetrahedral geometry which is similar to carbon in diamond crystal format. When two valence electron atomic orbitals in a Silicon crystal combine to form the covalent bonding, two possible molecular orbitals are formed. A bonding orbital is the molecular orbital that is lowered in energy in comparison to sum of the energies of individual electron orbitals. In contrary, relative to the sum of the energies of the individual electron orbitals, the other molecular orbital, which is also referred to as anti-bonding orbital, is raised in energy [99].

In solid materials where atoms are bonded together, some energy levels are lowered in energy and some are raised. These lowered and raised energies are considered with respect to the sum of all the energies within the valence electrons.

Within the lowered energy electrons, instead of these electrons having precisely the same amount of energy, the energy levels are in a form of an energy band; i.e. the difference between the energy of electrons within a band are not the same but they have small local differences within the lowered energy electrons. Similarly, the raised energy electrons also shape another band with higher energy with respect to the other lowered molecular orbitals. These energy bands are made from a finite number of electron energy levels which are spaced very closely. The valence electrons cannot have any energy outside of these two bands [100].

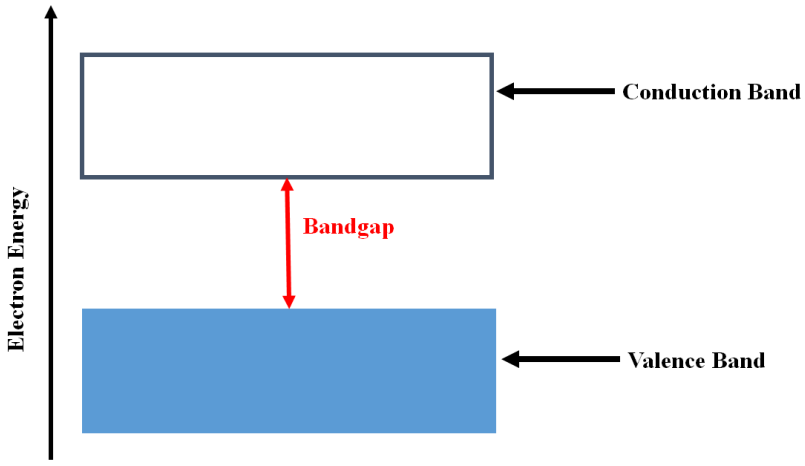

Fig. D.2 Energy band diagram of a semiconductor.

The space between the valence band and the conduction band is known as forbidden region or band gap. Electrons cannot have an energy in this band. Fig. D.2 shows the energy band of a hypothetical solid material at zero Kelvin when all the valence electrons are combine to form the bond between the atoms and all the electrons are completely filling the valence band and there is no electron in the conduction band. In this figure, the valence band is shown coloured meaning that all the electrons are in

this band and the conduction band is shown empty. This can theoretically happens for a pure silicon crystal at zero Kelvin degrees [101].

Doping of Semiconductors

As explained earlier, based on Octet-rule, Si atoms in a crystal lattice have 8 atoms in their valence layer and they get the extra electrons that they need by sharing the electrons with their neighbouring atoms. As mentioned in section 3.2.1, Si has 4 atoms in the valence layer. Hence, it requires 4 more electrons to each the stable state. Phosphorous (P) atom is in the column on the right hand side of Si in the periodic table. Hence, it has 5 electrons in the valence layer (pentavalent element). If a Si atom is replaced with a P atom, the other silicon atoms in the neighbouring of P tend to share 4 electrons with P. Hence, when the covalent bonding between these atoms are formed, P will have one extra electron which can freely move in the lattice.

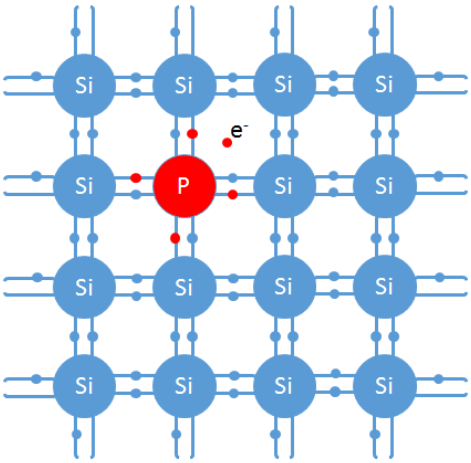

Fig. D.3 N-type doping of Si.

This is shown in Fig. D.3. As can be seen in this illustration, P atom is shown with red and the electrons in the valence layer of P is shown with the same colour. As

can be seen, this lattice has one extra electron in comparison to the pure Si crystal shown in Fig. D.1; This is known as N-type doping of the semiconductor and this is due to the fact that the semiconductor has one negative charge which can move freely and it is responsible for conduction of electricity in the semiconductor. This process is known as doping of the semiconductor. The P atom is known as donor atom and the number of atoms injected in the lattice to dope the semiconductor is shown by N_{D^+}.

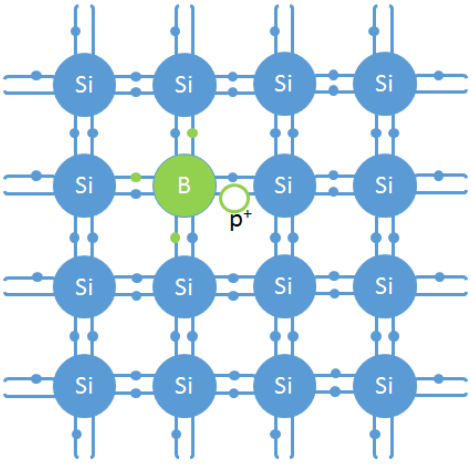

Fig. D.4 P-type doping of Si.

In contrast, in order to make a P-type doping silicon, an atom from the left hand column of the periodic table is replaced with a Si atom. Usually, Boron (B) which is the 5th element in the periodic table is used for P-type doping. This atom has 3 electrons in the last layer (trivalent element) and hence, it shares three electrons with the neighbour Si atoms and one hole remains in the lattice. Since, there is electron deficiency in the lattice, the hole existing in the hole can readily accept an electron and get to the stable state. However, the electron which is borrowed within the material will create another void/hole in the lattice and this seems like the hole is moving inside

the semiconductor and movement of hole is responsible for conduction in the semiconductor. Fig. D.4 shows a P-type doping of Si using B atom. As can be seen, the hole within the crystal is shown with a hollow circle and is signed with p^+. The B atom is known as an acceptor atom and the number of B atoms in the lattice is shown using N_A^-.

In order to increase the conductivity of the semiconductor and reduce the electrical resistivity, the semiconductor is usually heavily or lightly doped; e.g. the number of dopants (N-type or P-type) is in the order of $10^{19}\ cm^{-3}$ for heavily doped Si or $10^{13}\ cm^{-3}$ for lightly doped semiconductor. Doping of semiconductors is carried out by ion implantation process in which ions of a material are accelerated in an electric field and the semiconductor is bombarded with these beams. Other methods of doping are diffusion which is used for solid state or during the crystal growth. The ions lose their energy as they travel through the crystal, hence the diffusion length can be adjusted by adjusting the energy of the electric field. The implantation process damages the crystal structure. Hence, the implantation process is followed by a high temperature annealing process which enables the N-type or P-type dopant and the extra carriers. In case of 4H-SiC, the N-type and P-type dopants are usually Phosphorous (P) and Aluminium (Al) respectively.

Intrinsic Carrier Concentration

Electrons in valence energy layer, are at the most stable state and they have the lowest energy. If an electron receives enough energy to move from the valence band to the conduction band, then it can move freely between atoms within the solid material.

The amount of energy that the electron needs to receive in order to move from the valence band to the conduction band is equal to the band gap energy which is the difference between the energy level of the valence band and the conduction band. This energy can be received in form of a photon (basis of photovoltaic cells) or in form of heat or electrical potential. If the band gap is small, the energy needed would be very small [100]. This amount of energy for Si is equal to $1.11eV$ and in 4H-SiC is $3.23eV$.

At room temperature (300°K), silicon has 9.696×10^{9} cm^{-3} (approximately 1×10^{10} cm^{-3}) free electrons. This is referred to as intrinsic carrier concentration and is shown with n_i. Intrinsic carrier concentration is a function of temperature. Equation (D.1) and (D.2) show the temperature dependency of this parameter for Si and 4H-SiC [31].

Fig. D.5 shows the temperature dependency of intrinsic carrier concentration of Si and 4H-SiC. As can be seen, the intrinsic carrier concentration of 4H-SiC is significantly lower than that of Si and this is due to its large band gap and so less electrons can jump to the conduction band at elevated temperatures (also known as bulk generation current) [102]. This is a good indication that the bulk generation current is negligible for 4H-SiC devices in comparison to the conventional Si devices.

$$n_i(T,Si) = 3.87\times10^{16}T^{1.5}\exp\left(\frac{-7.02\times10^{3}}{T}\right) \qquad \text{(D.1)}$$

$$n_i(T,4H-SiC) = 1.70\times10^{16}T^{1.5}\exp\left(\frac{-2.08\times10^{4}}{T}\right) \qquad \text{(D.2)}$$

When an electron gains enough energy to move to the conduction band, an electron-holes pair is generated. This is known as charge carrier generation. A hole is a term used to show lack of existence of an electron at a position in the atomic lattice and is considered as a positive charge. The intrinsic carrier concentration of a material is determined by thermal generation of electron-hole pairs.

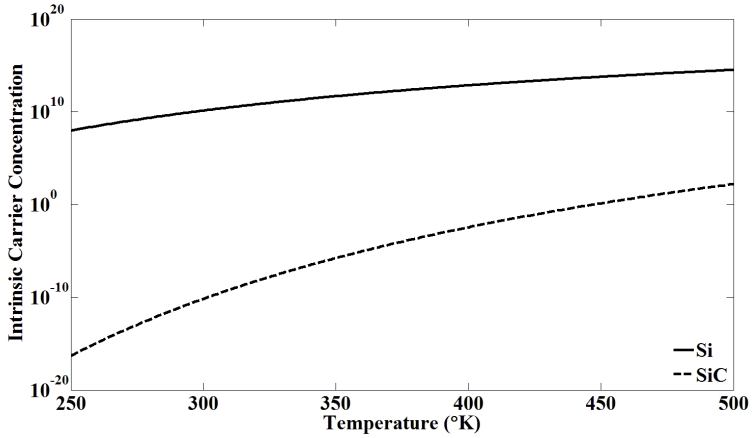

Fig. D.5 Temperature dependency of intrinsic carrier concentration for Si and 4H-SiC from equations 2.1 and 2.2.

In contrast to electron-hole pair generation, when an electron jumps back from the conduction band to the valence band by releasing its energy, it recombines with a hole existing in the lattice and this process is known as recombination of electron-hole pairs.

Carrier Recombination and Generation

There are three types of carrier recombination in which the excessive electron/hole pairs stabilise in the valence layer and they annihilate each other during this process. These are:

- Auger recombination
- Radiative recombination
- Shockley-Read Hall recombination

In Auger recombination, the energy of the electron and hole that recombine is transferred in the form of kinetic energy to another electron in the band edge of the conduction band. This electron moves to a higher energy in the conduction band it gradually releases the excessive energy in form of heat and moves down to the band edge of the conduction layer. This recombination often happens in the heavily doped semiconductor and during the high level injection. When the number of excessive minority carriers injected into the semiconductor becomes comparable to the background doping of the semiconductor, it is referred to as high level injection. Fig. D.6 illustrates the Auger recombination and the two steps of the process.

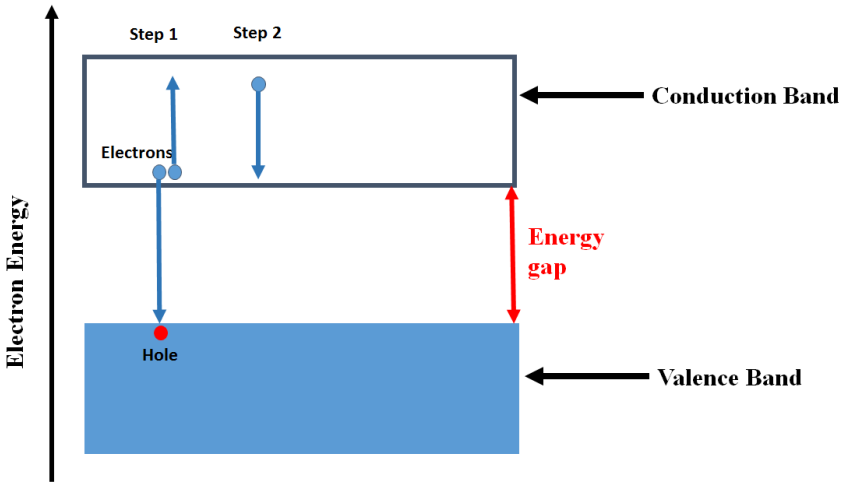

Fig. D.6 Auger recombination process. Step 1: electron recombines with a hole and releases its energy to the third electron in the conduction band causing it to move to higher energy, Step 2: the third electron moves back to the edge of the conduction band by releasing the extra energy that it received.

In radiative recombination, when an electron recombines with a hole and stabilises the valence band of the semiconductor atom, the energy that the carriers release is in form of photons. This type of recombination is also referred to as band-to-band recombination. Fig. D.7 shows band-to-band recombination process. This is the basic operation of Light Emitting Diodes (LED). This phenomenon is also known as electroluminescence. The band gap of the semiconductor and the amount of energy that the carrier releases, determines the wavelength of the photon and hence the colour of the light that is emitted from this recombination.

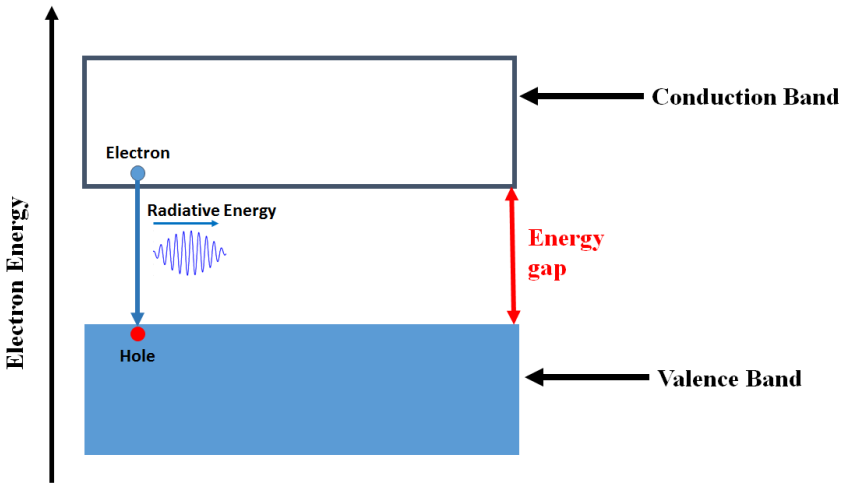

Fig. D.7 Band-to-band recombination process.

In case of Shockley-Read-Hall (SHR) recombination, the carriers are combined in a two-step process which requires presence of defects in the crystal. During SRH recombination, an electron or hole is trapped in an energy band in the forbidden band gap which is due to presence of defect in the material. These defects might be uncontrolled due to non-uniformity in the crystal lattice (for instance in case of SiC) or it can be a deliberate added material in form of doping in the semiconductor crystal. At

this point, if the electron in the trap does not move to the conduction band due to the energy that it receives thermally, and at the same time, another hole or electron receives enough thermal energy to move from the valence band to the trap band, then these two can recombine. Once the trap is filled, it cannot accept another carrier. In the second step, the electron in the trap can fall into an empty state in the valence band and complete the recombination process. Another interpretation of this process is that the electron and hole annihilate in the trap band as they meet each other in the trap. The trap band can either be close to the conduction band or the valence band and the SRH recombination rate, depends on where the trap band is located relevant to the conduction band or the valent band. If the trap band is close to the conduction band, SRH recombination rate is low. This is due to the fact that the electrons or holes trapped in this band can easily receive enough energy to jump up to the conduction band again. The most effective trap band to maximise the SRH recombination is in the mid-point of the band gap. Fig. D.8 shows the SRH recombination process.

Current Flow in Semiconductors

Current flow is movement of carriers in the semiconductor and the amount of current is the number of carriers that pass through a cross section of a device per second. The carrier transport mechanism can be divided in two categories: drift and diffusion.

Carrier Drift

Carrier drift is movement of carrier in the semiconductor when an electric field E (Vcm^{-1}) is applied to it. Based on the following assumptions, the drift current can be derived. The assumptions are:

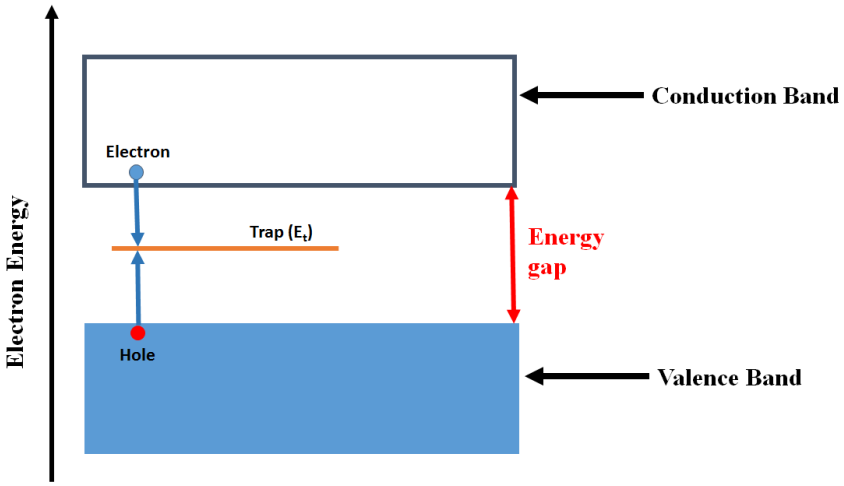

Fig. D.8 Shockley-Read-Hall recombination process.

- In the active area of the semiconductor, the temperature is uniform. This assumption is valid as the thermal conductivity of the semiconductor is relatively large. Thermal conductivity of Si is 1.3 $Wcm^{-1}°C^{-1}$ and thermal conductivity of 4H-SiC is 3.7 $Wcm^{-1}°C^{-1}$.
- The width of the device is a few hundreds of microns in case of Si and a between 30-300 μm in case of SiC.
- The average velocity of carriers in the semiconductor is the same for all the electrons and holes.

- The scattering effect and random movement of carriers due to thermal energy at zero electric field is considered here and the studies are carried out by assuming the average velocity of the carriers in the semiconductor $\vec{v}$.

The current passing through a semiconductor from electrode A to electrode B, when an electric field equal to E is applied to these two electrodes can be expressed as the total amount of charge in the semiconductor divided by the amount of time it takes for the carrier to travel between electrode A and B which depends on *v*, the velocity of the carrier in the semiconductor.

$$I = \frac{Q}{\frac{L}{V}} \tag{D.3}$$

Hence, the current density equation can be written as below. This equation is known as the drift current equation

$$\vec{J} = \frac{\vec{I}}{A} = \rho\vec{v} \tag{D.4}$$

In equation (D.4), ρ is the charge density and hence, this equation can be written based on positive charge (holes) and negative charge (electrons) as below in which n and p are electrons and holes charge density in the semiconductor:

$$\vec{J} = -qn\vec{v} \tag{D.5}$$

$$\vec{J} = qp\vec{v} \tag{D.6}$$

In equation (D.5) and (D.6), due to the negative and positive electronic charge of the electrons and holes, and due to the fact that it is assumed that holes move in the direction of the electric field and electrons move in the opposite direction, the equations have a negative and positive signs respectively.

Based on the 4th assumption mentioned above, the force applied to the electron due to thermal scattering of carriers and the electrostatic force can be written as:

$$\vec{F} = m\vec{a} = q\vec{E} - m\frac{\vec{v}}{\tau_c} \tag{D.7}$$

In equation (D.7), the scattering force is the momentum of the carrier divided by the time between each carrier scattering (τ_c). From equation (D.7) we have an equation for average carrier velocity in a semiconductor based on the electric field applied to it:

$$q\vec{E} = m\frac{d\vec{v}}{dt} + m\frac{\vec{v}}{\tau_c} \tag{D.8}$$

In the steady state mode when the carriers reach a constant average speed, an expression for the mobility (μ) of the carriers is achieved:

$$\mu = \frac{q\tau_c}{m} \tag{D.9}$$

The carrier mobility determines the conductivity and resistivity of a semiconductor device. It is worthwhile mentioning that the carrier mobility for electrons and holes are doping dependant. The velocity of electrons and holes increases with the increase of electric field; however, it saturates when the carrier energy goes beyond the optical phonon energy. In Si, there are no accessible higher energy band that the electron can go to and the velocity of the electrons saturates at the saturation velocity of v_{sat}. This velocity may be calculated at different temperatures using equation (D.10).

$$v_{sat} = \frac{2.4 \times 10^7}{1 + 0.8 \exp\left(\frac{T}{600}\right)} \tag{D.10}$$

Using expression (D.9) and applying it to the drift current equation (D.4), the drift current equation for electrons and holes are obtained:

$$\begin{cases} \vec{J}_n = qn\mu_n \vec{E} \\ \vec{J}_p = qp\mu_p \vec{E} \end{cases} \tag{D.11}$$

Considering that the conductivity of the material is based on drift movement of electrons as well as holes and combining both equations in (D.11), we have:

$$J = q\left(n\mu_n + p\mu_p\right)E \tag{D.12}$$

From equation (D.12) conductivity of a material due to drift of electrons and holes can be achieved:

$$\sigma = \frac{J}{E} = \frac{1}{q\left(\mu_n n + \mu_p p\right)} \tag{D.13}$$

The conductivity of the material due to movement of electrons and holes is highly temperature dependent. The temperature dependency of electron and hole carrier mobility in Si is:

$$\mu_{n,p} = \mu_{n0,p0}\left(\frac{300}{T}\right)^{2.5} \tag{D.14}$$

In which, $\mu_{n0,p0}$ is the mobility of electrons or holes at room temperature (300°K). As can be seen from equation (D.14), the mobility reduces at higher temperatures and this indicates that the conductivity of the material reduces and resistivity increases at higher temperatures. This is due to the fact that the vibration and lattice scattering of atoms at higher temperature dominates and builds a resistance against the movement of the carriers in the solid state material. Electron/hole mobility of 4H-SiC and the equation that expresses the impact of temperature on the carrier mobility in this material is explained in Chapter 4, section 4.3, equation (D.13). By increasing the density of dopant, mobility of electrons and holes decreases due to increase of scattering occurrences. It is worthwhile to mention that conduction through the bulk material (i.e. drift region of power devices) is less affected by the scattering in comparison to the surface and hence, the mobility of the bulk is higher than the surface mobility.

Carrier Diffusion

Carrier diffusion due to gradient in the carrier concentration within the semiconductor crystal lattice can result in diffusion current in the carrier. The diffusion current for electrons and holes can be expressed using equation (D.15) and (D.16) as below:

$$J_n = qD_n \frac{dn}{dx} \tag{D.15}$$

$$J_p = qD_p \frac{dp}{dx} \tag{D.16}$$

In these two equation, D_n and D_p are diffusivity of electrons and holes and they are expressed using Einstein relation:

$$D_n = \mu_n \frac{kT}{q} = \mu_n V_T \tag{D.17}$$

$$D_p = \mu_p \frac{kT}{q} = \mu_p V_T \tag{D.18}$$

In the Einstein relation, k is Boltzmann's constant which is 1.38×10^{-23} J.K^{-1}, T is temperature in Kelvin, q is electron elementary charge, 1.60217662×10^{-19} Coulombs. V_T is thermal voltage and is equal to Boltzmann's constant multiplied in temperature divided by the electron elementary charge and is equal to approximately 26mV at 300°K.

Total Current

The total current in a semiconductor is obtained by adding the drift and diffusion currents together. The total current due to electrons is shown in equation (D.19) and the total current due to holes is shown in equation in 1-D (D.20). The current is the sum of electrons and holes densities multiplied in the semiconductor active area perpendicular to the current flow direction (D.21).

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx} \tag{D.19}$$

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx} \tag{D.20}$$

$$I_{tot} = A\left(J_n + J_p\right) \tag{D.21}$$

Equations (D.19) and (D.20) are also known as current transport equations. The first term of these equations are current due to drift of carriers and the second term of these equations show the current due to diffusion of carriers.

Basic Equations Governing Semiconductor Devices

In this section, the basic equations that describes the physics behind the behaviour of power semiconductor devices is explained. The first equation, is continuity equation. Continuity equation, shows the rate of change of charge over time (change of carrier density profile) is due to the difference between the incoming and outgoing current flux density, plus the net of generation and recombination of carriers in that region of the semiconductor. The equation is shown in (D.22).

$$\frac{\partial n(x,t)}{\partial t}Adx = \left(\frac{J_n(x)}{-q} - \frac{J_n(x+dx)}{-q}\right)A + (G_n(x,t) - R_n(x,t))Adx \qquad \text{(D.22)}$$

In this equation, $n(x,t)$ denotes the number of carriers in the region between position x and $x+dx$ in the semiconductor (carrier density) at time t. J_n shows the current flux entering or exiting the cross section A of the device. G_n shows the generation rate at in time and space domain in which carrier generation is due to impact ionisation or avalanche and R_n shows the recombination rate in which carriers annihilate each other as explained earlier. Taylor series expansion can be applied to the incoming and outgoing fluxes as below:

$$J_n(x+dx) = J_n(x) + \frac{dJ_n(x)}{dx}dx \qquad \text{(D.23)}$$

Using equation (D.23) in (D.22), continuity equation can be rewritten as (D.24) for electron carrier concentration and (D.25) for holes carrier concentration:

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{q}\frac{\partial J_n(x,t)}{\partial x} + (G_n(x,t) - R_n(x,t)) \qquad \text{(D.24)}$$

$$\frac{\partial p(x,t)}{\partial t} = -\frac{1}{q}\frac{\partial J_p(x,t)}{\partial x} + (G_p(x,t) - R_p(x,t)) \qquad \text{(D.25)}$$

By replacing in equation (D.19) and (D.20) in equations (3.24) and (D.25) respectively, two partial differential equations are obtained as below:

$$\frac{\partial n(x,t)}{\partial t} = \mu_n n \frac{\partial E(x,t)}{\partial x} + \mu_n E \frac{\partial n(x,t)}{\partial x} + D_n \frac{\partial^2 n(x,t)}{\partial x^2} + G_n(x,t) - R_n(x,t) \quad \text{(D.26)}$$

$$\frac{\partial p(x,t)}{\partial t} = -\mu_p n \frac{\partial E(x,t)}{\partial x} - \mu_p E \frac{\partial p(x,t)}{\partial x} + D_p \frac{\partial^2 p(x,t)}{\partial x^2} + G_p(x,t) - R_p(x,t) \quad \text{(D.27)}$$

The second equation is the charge density equation in a semiconductor. Based on this equation, the charge density is equal to the number of free electrons and holes plus the number of positive and negative ions due to doping of the semiconductor multiplied in the electron elementary charge. This equation is shown in (D.28).

$$\rho = q\left(p - n + N_D^+ - N_A^-\right) \quad \text{(D.28)}$$

Based on the differential form of one equation of the Maxwell's equations which is derived from the Gauss' law for electricity, the electric field E can be related to the charge density equation as below:

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon} = \frac{q}{\varepsilon}(p - n + N_D^+ - N_A^-) \quad \text{(D.29)}$$

In which ε is the permittivity of the semiconductor which is equal to relative permittivity of the semiconductor material multiplied in the vacuum permittivity. The permittivity of zero space and is equal to $8.854187817\times10^{-12}$ F.m^{-1} and the relative permittivity of Si is 11.7 and 4H-SiC relative permittivity is equal to 9.7 [103].

Moreover, the electric field is related to the electric potential (Φ) using the equation shown in (D.30):

$$\frac{d\Phi}{dx} = -E \tag{D.30}$$

Using equation (D.29), (D.30), Poisson's equation can be derived:

$$-\frac{d^2\Phi}{dx^2} = \frac{dE}{dx} = \frac{q}{\varepsilon}(p - n + N_D^+ - N_A^-) \tag{D.31}$$

Combining the current continuity equation (D.24) and (D.25) with the Poisson's equation (D.31), the Maxwell's equation for the total current can be derived. This equation, basically sums the total current as the drift and diffusion currents plus the displacement current which is the last term of the equation below. The displacement current shows the rate of change of displacement electric field in time in a semiconductor.

$$J_{tot} = J_n + J_p + \varepsilon_s \frac{\partial E}{\partial t} \tag{D.32}$$

Minority Carrier Saturation Current

The emitter recombination current and the electron and hole recombination coefficients are equivalent to the minority carrier saturation current and they are expressed as below:

$$J_{n(PN-)} = J_{sne}\left(\frac{p_{(PN-)}}{n_i}\right)^2 \tag{D.33}$$

$$J_{sne} = qh_p n_i^2 \tag{D.34}$$

In these equations, J_{sne} is the minority saturation current density.

Depletion Region Voltage Feedback Loop

Similar to op-amp operation, a feedback loop with a high gain is used to detect the zero crossing of the carrier concentration during formation of the depletion region and to calculate the voltages at the edges of the boundary conditions.

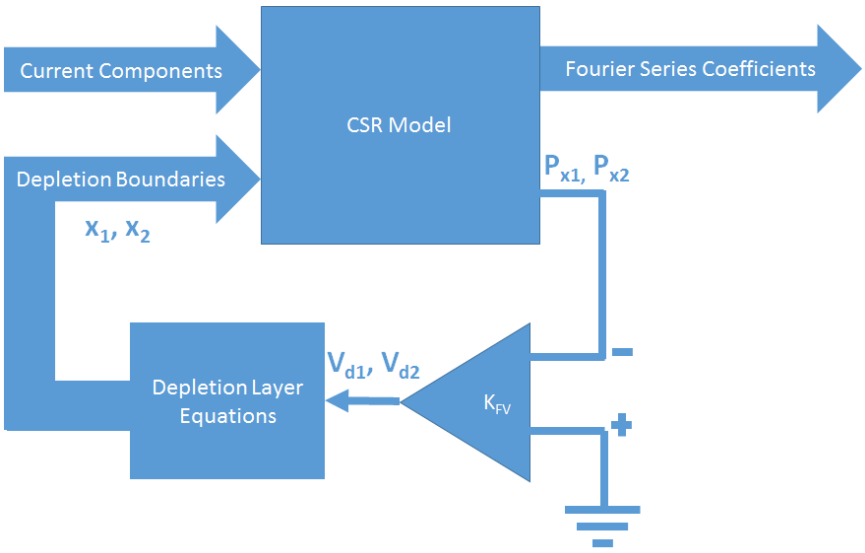

Fig. D.9 Feedback block diagram to calculate the depletion region voltage.

MOSFET Parasitic Capacitances

The vertical MOSFET cell shown in Fig. 3.11 is one of the cells that makes a larger MOSFET. In another word, a commercial MOSFET is made from many of these cells in parallel which enables the device to handle higher current. The 3D view of a MOSFET half-cell is shown in Fig. D.10.

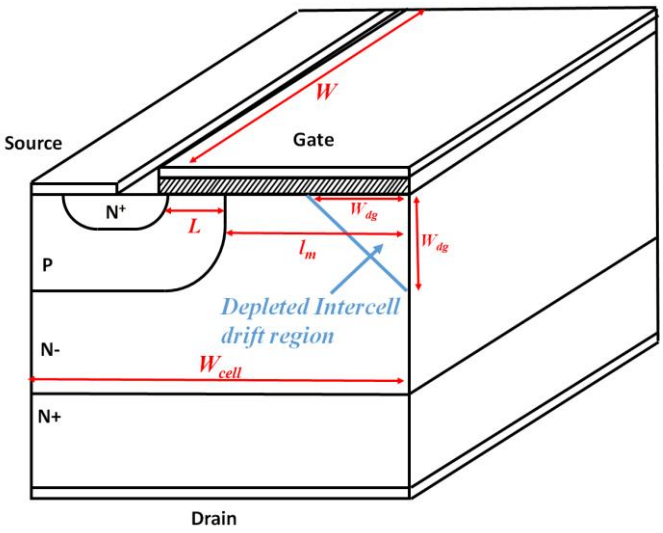

Fig. D.10 3D view of a MOSFET cell with stripe gate configuration.

As shown in Fig. D.10 the width of the depletion region is equal to the side length of the right triangle and is referred to as W_{dg}. In order to accurately model the operation and switching transient of a MOSFET, the voltage dependent depletion capacitors need to be modelled accurately. In this type of cell configuration, the undepleted accumulation layer capacitance (C_{UAC}) is calculated using equation below:

$$C_{UAC} = C_{ox} W \left[\left(W_{cell} - W_{dg}{}' \right) - \left(W_{cell} - l_m \right) \right] \tag{D.35}$$

In which:

$$W_{dg}{}' = \min\{W_{dg}, l_m\} \tag{D.36}$$

In this equation, l_m is known as intercell half-width the distance from the depletion width, formed at the centre of the Intercell region, to the edge of the P^+ region at the bottom of the gate. The depleted Intercell drift region capacitance (C_{DIC}) is calculated as below:

$$C_{DIC} = \int_{W_{cell}-W_{dg}'}^{W_{cell}} \frac{C_{ox}\dfrac{\varepsilon}{y-(W_{cell}-W_{dg})}}{C_{ox}+\dfrac{\varepsilon}{y-(W_{cell}-W_{dg})}} W dy \tag{D.37}$$

Hence, the voltage dependent gate-drain capacitance can be calculated using equation below:

$$C_{GD} = \frac{A}{W_{cell}}\left(C_{UAC} + C_{DIC}\right) \tag{D.38}$$

By substituting equations (3.62) and (3.64) in equation (3.65) the depletion capacitance is calculated as below:

$$C_{GD} = a_i C_{ox} A\left[1+\frac{W_{dg}}{l_m}\left(\frac{1}{\dfrac{C_{ox}W_{dg}}{\varepsilon}+1}-1\right)\right] \tag{D.39}$$

In this equation, a_i is the Intercell ratio and I_{DS} is the drain-source current. The voltage dependent depletion width is equal to:

$$W_{dg} = \sqrt{\frac{2\varepsilon V_{dg}}{qN_B}} \tag{D.40}$$

E. Parasitic Gate Turn-On Circuit Equations

The following equations are obtained by applying Kirchoff's voltage and current laws to the circuit shown in Fig. 5.2.

$$I_{G1} = I'_{G1} + \left(V_{CE1} - V_{GE1}\right)\left(\frac{sC_{FB1}R_{FB1}}{1+sC_{FB1}R_{FB1}}\right)\left(\frac{1}{1+s\tau_{\lim}}\right) \tag{E.1}$$

$$I_{G2} = I'_{G2} + \left(V_{CE2} - V_{GE2}\right)\left(\frac{sC_{FB2}R_{FB2}}{1+sC_{FB2}R_{FB2}}\right)\left(\frac{1}{1+s\tau_{\lim}}\right) \tag{E.2}$$

$$I'_{G1} = \frac{1}{L_{G1}}\int\left(V_{gg1} - I'_{G1}R_{G1} - V'_{GE1}\right)dt \tag{E.3}$$

$$I'_{G2} = \frac{1}{L_{G2}}\int\left(V_{gg2} - I'_{G2}R_{G2} - V'_{GE2}\right)dt \tag{E.4}$$

$$I_{C1} = I'_{C1} - \left(V_{CE1} - V_{GE1}\right)\left(\frac{sC_{FB1}R_{FB1}}{1+sC_{FB1}R_{FB1}}\right)\left(\frac{1}{1+s\tau_{\lim}}\right) \tag{E.5}$$

$$I_{C2} = I'_{C2} - \left(V_{CE2} - V_{GE2}\right)\left(\frac{sC_{FB2}R_{FB2}}{1+sC_{FB2}R_{FB2}}\right)\left(\frac{1}{1+\tau_{\lim}}\right) \tag{E.6}$$

$$V_{Ls2} = V_{RL} - V'_{CE2} \tag{E.7}$$

$$I'_{C2} = \frac{1}{L_{s2}}\int V_{Ls2}dt = \frac{1}{L_{s2}}\int\left(V_{RL} - V'_{CE2}\right)dt \tag{E.8}$$

$$V_{Ls1} = V_{DC} - V'_{CE1} - V_{RL} \tag{E.9}$$

$$I'_{C1} = \frac{1}{L_{s1}} \int V_{Ls1} dt = \frac{1}{L_{s1}} \int \left(V_{DC} - V'_{CE1} - V_{RL} \right) dt \tag{E.10}$$

$$I_{RL} = I_{C1} + I_{G1} - I'_{C2} \tag{E.11}$$

$$V_{RL} = I_{RL} R_L \tag{E.12}$$

$$V'_{CE2} = V_{CE2} + L_{e2} \left(I_{C2} + I_{G2} \right) \left(\frac{1}{1 + s\tau_{\lim}} \right) \tag{E.13}$$

$$V'_{CE1} = V_{CE1} + L_{e1} \left(I_{C1} + I_{G1} \right) \left(\frac{1}{1 + s\tau_{\lim}} \right) \tag{E.14}$$

$$V'_{GE2} = V_{GE2} + L_{e2} \left(I_{C2} + I_{G2} \right) \left(\frac{1}{1 + s\tau_{\lim}} \right) \tag{E.15}$$

$$V'_{GE1} = V_{GE1} + L_{e1} \left(I_{C1} + I_{G1} \right) \left(\frac{1}{1 + s\tau_{\lim}} \right) \tag{E.16}$$

$V'_{CE1}, V'_{CE1}, V'_{GE1}$ and V'_{GE2} in equations (E.13-E.16) are observed collector-emitter and gate-emitter voltages at the top and bottom switches respectively. The differential limiting time constant τ_{lim} is set to be 10^{-12} s. This time constant is used to avoid algebraic loop and the direct feed through loops by using a Laplace transfer function with a more poles than zeros. The transfer function containing this limiting time constant, is basically a differentiator with a frequency limiter.

F. Parasitic Gate Turn-Off Circuit Equations

The following equations are obtained by applying Kirchoff's voltage and current laws to the circuit shown in Fig. 5.24.

$$V_{UP} = I_S R_S + 1/C_S \int I_S dt \tag{F.1}$$

$$I_S = I_{AK} + I'_{DS} - I_L \tag{F.2}$$

$$I_{AK} = 1/L_D \int (-V_{UP} - V_{AK} - V'_{DS}) dt \tag{F.3}$$

$$I'_{DS} = 1/L_D \int (V_{DC} - V_{UP} - V'_{DS}) dt \tag{F.4}$$

$$I_{DS} = I'_{DS} - (V_{DS} - V_{GS}) \left(\frac{sC_{FB}R_{FB}}{1+sC_{FB}R_{FB}} \right) \left(\frac{1}{1+s\tau_{\lim}} \right) \tag{F.5}$$

$$I'_G = 1/L_G \int (V_{gg} - I'_G R_G - V'_{DS}) dt \tag{F.6}$$

$$I_G = I'_G + (V_{DS} - V_{GS}) \left(\frac{sC_{FB}R_{FB}}{1+sC_{FB}R_{FB}} \right) \left(\frac{1}{1+s\tau_{\lim}} \right) \tag{F.7}$$

$$V'_{GS} = V_{GS} + L_S (I_{DS} + I_G) \left(\frac{s}{1+s\tau_{\lim}} \right) \tag{F.8}$$

G. Parallel Connected IGBTs Circuit Equations

$$V_{UP} = I_S R_S + 1/C_S \int I_S dt \tag{G.1}$$

$$I_{AK} = 1/L_D \int (-V_{UP} - V_{AK} - V'_{CE}) dt \tag{G.2}$$

$$I_S = I_{AK} + I'_{C1} + I'_{C2} - I_L \tag{G.3}$$

$$I'_{C1} = 1/L_{S1} \int (V_{DC} - V_{UP} - V'_{CE1}) dt \tag{G.4}$$

$$I'_{C2} = {}^{1}\!\!\diagup\!\!_{L_{S2}} \int \left(V_{DC} - V_{UP} - V'_{CE2}\right)dt \tag{G.5}$$

$$I'_{G1} = {}^{1}\!\!\diagup\!\!_{L_{G1}} \int \left(V_{gg1} - I'_{G1}R_{G1} - V'_{GE1}\right)dt \tag{G.6}$$

$$I'_{G2} = {}^{1}\!\!\diagup\!\!_{L_{G2}} \int \left(V_{gg2} - I'_{G2}R_{G2} - V'_{GE2}\right)dt \tag{G.7}$$

$$I_{G1} = I'_{G1} + \left(V_{CE1} - V_{GE1}\right)\left(\frac{sC_{FB1}R_{FB1}}{1+sC_{FB1}R_{FB1}}\right)\left(\frac{1}{1+s\tau_{\lim}}\right) \tag{G.8}$$

$$I_{G2} = I'_{G2} + \left(V_{CE2} - V_{GE2}\right)\left(\frac{sC_{FB2}R_{FB2}}{1+sC_{FB2}R_{FB2}}\right)\left(\frac{1}{1+s\tau_{\lim}}\right) \tag{G.9}$$

$$V'_{GE1} = V_{GE1} + L_{E1}\left(I_{C1} + I_{G1}\right)\left(\frac{s}{1+s\tau_{\lim}}\right) \tag{G.10}$$

$$V'_{GE2} = V_{GE2} + L_{E2}\left(I_{C2} + I_{G2}\right)\left(\frac{s}{1+s\tau_{\lim}}\right) \tag{G.11}$$

$$R_{ds(ON)1} = {}^{V_{CE1}}\!\!\diagup\!\!_{I_{C1}} \tag{G.12}$$

$$R_{ds(ON)2} = {}^{V_{CE2}}\!\!\diagup\!\!_{I_{C2}} \tag{G.13}$$

Publications

The chapters presented in this thesis are published online and the published journal and conference papers are listed on pages *xv* and *xvi.* For the ease of access to the reader the first pages of these papers are gathered in this section and they can be access online on IEEE Digital Library.

Investigating the Reliability of SiC MOSFET Body Diodes using Fourier Series Modelling

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***Abstract*— Using the Fourier series solution to the ambipolar diffusion equation, the robustness of the body diodes of SiC MOSFETs during reverse recovery has been studied. Parasitic bipolar latch-up during the reverse recovery of the body diode is a possible if there is sufficient base current and voltage drop across the body resistance to forward bias the parasitic BJT. SiC MOSFETs have very low carrier lifetime and thin epitaxial drift layers, which means that the dV/dt during the recovery of the body diode can be quite high. This dV/dt coupled with the parasitic drain-to-body capacitance can cause a body current. The paper introduces a new way of assessing the reliability of SiC MOSFETs during the reverse recovery of the body diode. The impact of switching rates, parasitic inductances and carrier lifetime on the activation of the parasitic BJT has been studied.**

***Index Terms*—Ambipolar Diffusion Equation, Fourier series, MOSFET, PiN Diodes, Body Diode, Inverter.**

I. INTRODUCTION

Power MOSFET circuits often use PiN body diodes as the anti-parallel diodes. This includes applications such as DC-DC buck converters, bridge topology switching circuits, high performance PV converter cell and can also be employed in synchronous rectified BLDC motor drive inverter circuits [1-4]. The voltage blocking drift region sandwiched between the drain and source shapes the PiN body diode in a vertical MOSFET. A significant portion of electrical stress and power losses in these applications are caused by the diode snappiness, high *dV/dt* across the body diode and high reverse recovery charge of the body diode [5]. The large reverse recovery is the result of high excessive amount of carriers stored in the charge storage region (drift layer) of the diode. The lifetime control techniques (gold or platinum doping as well as irradiation) are not applicable to reduce the carrier lifetime in some devices such as CoolMOS. The robustness of the MOSFET body diode is the main concern especially under hard commutation of the device. This is the case in applications like synchronous rectification, or motor drives or primary side switching of SMPS power supplies circuits [6]. High demands for higher frequency and more efficient converters introduced wide bandgap materials such as SiC material and consequently high blocking voltage SiC MOSFETs were developed. Carrier lifetime in of SiC material, with the same base doping as silicon material, is much shorter. SiC device can withstand higher reverse voltages and consequently 10 times smaller thickness is needed to have the same level of voltage blocking capability as silicon-based devices [7]. Thus, SiC MOSFETs show smaller reverse recovery with a higher breakdown voltage. The effect of using SiC MOSFET in synchronous rectification is studied in [2] which shows a negligible SiC MOSFET body diode reverse recovery and in addition to that, it showed feasibility of increasing the switching frequency. All in all, SiC devices are a suitable candidate for power application named above due to their superior performance. However, there are concerns regarding the reliability of SiC MOSFET body diode.

Vertical MOSFET structure consists of a parasitic NPN BJT coupled with a PiN body diode. The parasitic BJT can switch-on if the emitter-base voltage is forward biased, the base-collector voltage is reverse biased and there is sufficient body current in the base of the BJT. When the body current rises the voltage drop in the base of the BJT due to existence of body resistance increases. Body resistance is highly dependent to the doping and temperature of the P-body. If the voltage drop becomes greater than the base-emitter voltage, then the parasitic BJT latches-up. This can happen at high temperatures. By grounding the source to the body using a high dose body implant and a common metal contact, the parasitic BJT is prevented from latching. Moreover, the high voltage variation (*dV/dt*) of the body diode during reverse recovery coupled with the parasitic drain-to-body capacitance within the MOSFET can produce enough amount of body current ($C \cdot dV/dt$) swich the parasitic BJT on. This phenomenon happens especially in SiC MOSFETs where *dV/dt* is high, minority carrier lifetime in the drift region is very short and the body diode is snappy. In this paper, the reliability of the SiC MOSFET body diode under reverse recovery is investigated experimentally and by modelling. The body diode of the MOSFET has been

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Modeling of Temperature Dependent Parasitic Gate Turn-On in Silicon IGBTs

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***Abstract*—Parasitic turn-on can cause unintentional triggering of the IGBTs since the discharge current of the Miller capacitance coupled with high *dV/dt* can activate a device that should be off. The short circuit current resulting from parasitic turn-on coupled with the high voltage causes significant power dissipation which can be a reliability issue. This issue is exacerbated by higher ambient temperatures since the negative temperature coefficient of the IGBT's threshold voltage as well as the positive temperature coefficient of the minority carrier lifetime will increase the peak and duration of the short circuit current. Accurate modeling of the shoot-through power and its temperature dependency is important for circuit designers when designing mitigation techniques like multiple resistive paths and bipolar gate drivers. The physics-based model proposed in this paper can produce accurate results with good matching over temperature. The model improves on compact circuit models based on lumped parameters.**

***Index Terms*-- IGBT Parasitic Turn-On Modeling, Temperature Dependent, Shoot-through Current, Voltage Source Converter.**

NOMENCLATURE

C_{FB1}	Top IGBT feedback capacitance (F)
C_{FB2}	Bottom IGBT feedback capacitance (F)
I_{C1}	Top collector current (A)
I_{C2}	Bottom IGBT collector current (A)
I'_{C1}	Top IGBT observed current (A)
I'_{C2}	Bottom IGBT observed current (A)
I_{G1}	Top IGBT gate current (A)
I_{G2}	Bottom IGBT gate current (A)
I'_{G1}	Top IGBT internal gate current (A)
I'_{G2}	Bottom IGBT internal gate current (A)
I_{RL}	Load current (A)
K_p	MOSFET device transconductance (AV^{-2})
K_{p0}	MOSFET device transconductance at room temperature (AV^{-2})
L_{e1}	Top IGBT Kelvin emitter inductance (H)
L_{e2}	Bottom IGBT Kelvin emitter inductance (H)
L_{G1}	Top IGBT gate stray inductance (H)
L_{G2}	Bottom IGBT gate stray inductance (H)
L_{s1}	Top IGBT stray inductance (H)
L_{s2}	Bottom IGBT stray inductance (H)
R_{FB1}	Top IGBT feedback resistance (Ω)
R_{FB2}	Bottom IGBT feedback resistance (Ω)
R_{G1}	Top IGBT gate resistance (Ω)
R_{G2}	Bottom IGBT gate resistance (Ω)
R_L	Load resistance (Ω)
T	Temperature (K)
T_0	Room temperature (K)
V_{CE1}	Top IGBT collector-emitter voltage (V)
V'_{CE1}	Top IGBT observed collector voltage (V)
V_{CE2}	Bottom IGBT collector-emitter voltage (V)
V'_{CE2}	Bottom IGBT observed collector voltage (V)
V_{DC}	DC link or supply voltage (V)
V_{GE1}	Top IGBT gate-emitter voltage (V)
V_{GE2}	Bottom IGBT gate-emitter voltage (V)
V'_{GE1}	Top IGBT observed gate voltage (V)
V'_{GE2}	Bottom IGBT observed gate voltage (V)
V_{gg1}	Top IGBT gate drive voltage (V)
V_{gg2}	Bottom IGBT gate drive voltage (V)
V_{Ls1}	Top IGBT stray inductance voltage (V)
V_{Ls2}	Bottom IGBT stray inductance voltage (V)
V_{RL}	Load voltage (V)
V_{th}	Threshold voltage (V)
V_{th0}	Threshold voltage at room temperature (V)
μ_n	Electron mobility ($cm^2V^{-1}s^{-1}$)
μ_{n0}	Low-field (maximum) electron mobility ($cm^2V^{-1}s^{-1}$)
μ_p	Hole mobility ($cm^2V^{-1}s^{-1}$)
μ_{p0}	Low-field (maximum) hole mobility ($cm^2V^{-1}s^{-1}$)
τ_{HL}	High-level carrier lifetime (s)
τ_{HL0}	High-level carrier lifetime at room temperature (s)
τ_{lim}	Differentiator limiting time constant (s)

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I. INTRODUCTION

The unintentional turn-on of a power switching device in voltage source converters, which is influenced by the high switching frequency of the complementing device in the same phase leg is known as cross-talk or parasitic turn-on. The demand for higher switching frequency causes higher *dV/dt* and *dI/dt* which consequently coupled with the Miller capacitance of the device, induces a voltage greater than the threshold voltage of the device across the gate-emitter. Hence, a short circuit occurs across the leg of the inverter since both devices are simultaneously conducting [1].

In the half-bridge topology, which is the main block in the full-bridge and three-phase inverters, the power devices should not be switched simultaneously. However, due to parasitic turn-on, a high surge of current capable of destroying the devices can pass through the devices. The severity of this problem increases with the switching

Compact Electrothermal Reliability Modeling and Experimental Characterization of Bipolar Latchup in SiC and CoolMOS Power MOSFETs

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***Abstract*—In this paper, a compact dynamic and fully coupled electrothermal model for parasitic BJT latchup is presented and validated by measurements. The model can be used to enhance the reliability of the latest generation of commercially available power devices. BJT latchup can be triggered by body-diode reverse-recovery hard commutation with high *dV/dt* or from avalanche conduction during unclamped inductive switching. In the case of body-diode reverse recovery, the base current that initiates BJT latchup is calculated from the solution of the ambipolar diffusion equation describing the minority carrier distribution in the antiparallel p-i-n body diode. For hard commutation with high *dV/dt*, the displacement current of the drain-body charging capacitance is critical for BJT latchup, whereas for avalanche conduction, the base current is calculated from impact ionization. The parasitic BJT is implemented in Simulink using the Ebers–Moll model and the temperature is calculated using a thermal network matched to the transient thermal impedance characteristic of the devices. This model has been applied to CoolMOS and SiC MOSFETs. Measurements show that the model correctly predicts BJT latchup during reverse recovery as a function of forward-current density and temperature. The model presented, when calibrated correctly by device manufacturers and applications engineers, is capable of benchmarking the robustness of power MOSFETs.**

***Index Terms*—Body diode, compact electrothermal modeling, inverter, MOSFET, p-i-n diodes, parasitic BJT latchup, SiC MOSFET reliability.**

I. Introduction

BODY diodes can sometimes be used as the antiparallel diodes in power MOSFET circuits. Because of the voltage blocking drift layer between the p-body and the drain, the body diode is effectively a p-i-n diode. Power MOSFET body diodes can be used in applications, such as dc–dc buck converters, bridge topology switching circuits, and high-performance PV converter cell, and can also be employed in synchronous rectified brushless DC motor drive inverter circuits [1]–[6]. In such applications, diode snappiness and high reverse recovery charge of the body diode can impose a significant amount of electrical stress and power loss on the MOSFETs [7]. The large reverse recovery charge is the result of an excessive amount of carriers stored in the charge storage region (drift layer) of the diode. Conventional lifetime control techniques (gold or platinum doping as well as irradiation) are not applicable in reducing the carrier lifetime as is the case with discrete diodes; hence, the body diode of the MOSFET can suffer from significant reverse charge. One of the main concerns regarding the usage of the body diode of power MOSFETs is the robustness of the device under hard commutation, e.g., in synchronous rectification, or in other circuits such as motor drives or primary-side switching of switch-mode power supplies [8], [9].

The high demand for high-frequency and efficient power converters has triggered research into SiC devices including power MOSFETs [10]. SiC MOSFETs are more suitable for high-voltage and high-speed applications due to their higher breakdown voltage, lower on-state resistance, and faster switching. SiC has a significantly smaller minority carrier lifetime, and as a result of the higher critical field, the thickness of the voltage blocking drift layer is approximately ten times less than silicon devices. Consequently, they show smaller reverse recovery with a higher breakdown voltage. The effect of using SiC MOSFET in synchronous rectification was studied in [2], which shows that the reverse recovery of SiC body diode was negligible as well as an improvement in the switching speed of the MOSFET. MOSFETs have parasitic n-p-n BJTs that can latchup under the right conditions, i.e., when the emitter–base voltage is forward biased, the base–collector voltage is reverse biased, and there is sufficient body current in the base [11], [12]. For the BJTs to latch, there must be a body current sufficient to cause a voltage drop greater than the emitter–base junction voltage of the parasitic BJT. To prevent this from happening, the source is usually grounded to the body by a high dose body implant and a common metal contact. However, at high temperatures, a nonzero body resistance and a nonzero body current can cause BJT latchup. The high *dV/dt* of the body diode during reverse recovery coupled with the parasitic drain-to-body capacitance within the MOSFET can cause a body current (*CdV/dt*) sufficient to latch the parasitic BJT. This is particularly pertinent to SiC MOSFETs where *dV/dt* is high, the minority carrier lifetime is low, and the body diode is snappy.

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Compact Electrothermal Models for Unbalanced Parallel Conducting Si-IGBTs

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***Abstract*—For high current applications, silicon IGBTs are normally connected in parallel to deliver the required current ratings. The devices are normally designed to have identical electrothermal parameters for equal current and power sharing. However, over the mission profile of the device, non-uniform degradation of the electro-thermal properties like solder de-lamination or gate contact resistance as well as unequal heat extraction from the heat sink, can cause the parallel connected IGBTs to have different electrothermal properties. In this paper, a compact and accurate electro-thermal model for parallel connected IGBTs has been developed and validated by experimental measurements.**

Keywords—Parallel IGBT, Current Sharing, Electrothermal, Model

I. INTRODUCTION

IGBT based power modules are normally comprised of several dies connected in parallel to deliver a defined current rating [1-3]. Fig. 1. shows the power module of a (a) Nissan Leaf EV and (b) Infineon wind energy power electronic converter where several parallel dies can be seen. Furthermore, the Tesla Model S power inverter uses 14 parallel IGBTs in TO-247 packages which are mounted on a PCB board [4]. This is unlike other hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV) or electric vehicles which use the packaged power module as shown in Fig. 1. Consequently, ensuring synchronized electrical switching and balanced electrothermal parameters between these parallel devices becomes more crucial for high power rated inverters with high current capability. Balanced power dissipation between the parallel connected devices is required for optimal temperature distribution [5, 6]. Current sharing between the devices depends on the device parameters as well as the circuit parameters such as the gate inductance and gate resistance. Hence, in order to have balanced current sharing between the devices, they all need to switch ON and OFF at the same rate i.e. switching needs to be synchronized. While this is usually achieved by power module designers, however, over the mission profile of the module, it is possible that non-uniform degradation of the device electrothermal parameters can cause electro-thermal imbalance between the devices.

Common failure modes like solder/die attach voiding and delamination can cause a non-uniform thermal resistance across the die or DBC substrate, meaning that the parallel devices may be subject to different junction temperatures. Other parameters that may vary between the devices include the internal and external gate resistances due to increased gate wire-bond contact resistance due to thermo-mechanical stress cycling. These variations in the gate resistance will introduce variations in the switching rate and switching energy. Hence, the two principal parameters under investigation in this paper are electrical switching rates and the thermal resistance of the devices. The electrical switching rate is set by varying the gate resistance of the parallel connected IGBTs while the junction temperature of the devices is varied using a hotplates connected to the base of the device.

It is important that accurate compact models are developed with the capability of probing the effect of these electrothermal variations between parallel connected devices. These compact models should be computationally efficient and be physics-based. Finite element methods are computationally expensive and time consuming. Furthermore, the electrical switching time constants are on the order of microseconds while thermal response time constants range from milliseconds to seconds. Hence, finite element methods will be a cumbersome approach. SPICE based IGBT models on the other hand do not capture some physics-based thermal effects that will impact the parallel operation of the IGBTs. Hence, in this paper, a physics based compact modelling approach is used to capture the internal physics of the IGBT and couple it with circuit equations. The Ambipolar-Diffusion-Equation (ADE) that describes the carrier distribution profile in the IGBT is solved using the Fourier series approach developed elsewhere [6-15]. Look-up tables are used to de-couple the electrical time constants from the thermal time constants, thereby ensuring a fully coupled electrothermal model of parallel connected IGBTs. Using compact models to predict impact of electrothermal variation on temperature imbalance between the parallel connected IGBTs is a useful tool for reliability analysis.

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Physics-Based Modelling and Experimental Characterisation of Parasitic Turn-On in IGBTs

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Keywords

«IGBT Parasitic Turn-On Modelling», «Temperature Dependent», «Shoot-through Current», «Voltage Source Converter», and «Miller Capacitor».

Abstract

As power electronic engineers increase the switching speed of voltage source converters for the purpose of higher power density, the *dI/dt* and *dV/dt* across the power semiconductors increases as well. A well-known adverse consequence of high *dV/dt* is parasitic turn-on of the power device in the same phase leg as the device being triggered. This causes a short circuit with high shoot-through current, high instantaneous power dissipation and possibly device degradation and destruction. It is critical for converter designers to be able to accurately predict this phenomenon through diagnostic and predictive modelling. In this paper, a physics-based device and circuit model is presented together with experimental results on parasitic turn-on of IGBTs in voltage source converters. Because the model is physics based, it produces more accurate results compared with compact circuit models like SPICE and other circuit models that use lumped parameters. The discharge of the Miller capacitance is simulated as a voltage dependent depletion capacitance and an oxide capacitance as opposed to a lumped capacitor. The model presented accurately simulates IGBT tail currents, PiN diode reverse recovery and the non-linear miller capacitance all of which cannot be solved by lumped parameter compact models. This is due to the fact that the IGBT current in the model is calculated using the Fourier series based re-construction of the ambipolar diffusion equation and the miller capacitances are calculated using fundamental device physics equations. This paper presents a physics-based device and circuit model for parasitic turn-on in silicon IGBTs by numerically modelling the minority carrier distribution profile in the drift region. The model is able to accurately replicate the transient waveforms by avoiding the use of lumped parameters normally used in compact models.

Nomenclature

C_{FB1}	Top IGBT feedback capacitance (F)	T_0	Room temperature (K)
C_{FB2}	Bottom IGBT feedback capacitance (F)	V_{CE1}	Top IGBT collector-emitter voltage (V)
I_{C1}	Top collector current (A)	V'_{CE1}	Top IGBT observed collector voltage (V)
I_{C2}	Bottom IGBT collector current (A)	V_{CE2}	Bottom IGBT collector-emitter voltage (V)