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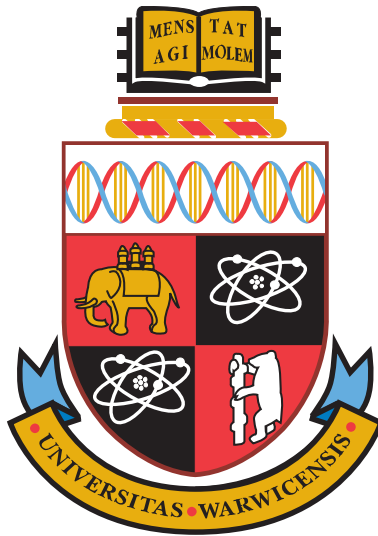
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Fabrication and Characterisation of 3C-SiC on Si Semiconductor Devices



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Dissertation submitted for the degree of

Doctor of Philosophy

October 2016

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Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has not been submitted for a degree at any other University. The author wishes to declare that apart from commonly understood and accepted ideas, or where reference is made to the work of others, all of the work described in this thesis was carried out in the School of Engineering, University of Warwick from October 2012 until August 2016.

F. Li

October 2016

Acknowledgements

Four years of work and joy during the study in the Warwick PEATER group, I would like to express my sincere gratitude and appreciation to my colleagues and friends, without whom I would never have been able to come this far.

Prof. Philip Mawby is my supervisor and had provided me the invaluable opportunity to make research on semiconductor electronics, in a working environment that is one of the best in the world. Throughout these years whenever I feel confused or lost, he always tried his best to advise me using his wisdom and professional experience. Beyond work, he is also a great friend and I do very appreciate those comfortable and relaxing conversations between us. Thank you, Phil.

Next person I want to thank particularly is Dr. Yogesh Sharma, a friend as well as a teacher to me. In the start of my study, I feel so fortunate that Yogesh was there helping me. His great passion and enthusiasm has been a great push behind me to initiate the experiments and analysis. As an expert of silicon carbide MOS technology, he walked me through the first step to the MOSFET fabrication, not to mention those endless discussions I still miss a lot now. Even after leaving for another position, Yogesh still called on me from time to time, helping and advising me on my research.

Special thanks to Dr. Mark Crouch for keeping the clean room facilities running, I do realise how difficult it is now. Thanks also go to Dr. Mike Jennings, Dr. David Martin, Dr. Dean Hamilton, Dr. Vishal Shah and particularly, Dr. Amador Perez-Tomas for their invaluable suggestions on the experiments design and paper writings. Some of the publications would never come out without their help. One more person, Dr. Hua Rong. It was great helpful to have someone else working together in the clean room at late nights and have a drink afterwards.

Last but most importantly, my dear parents have been supporting me forever and I can't thank them enough, although I am sure they are proud of me regardless.

Publications

1. **F. Li**, Y. Sharma, D. Walker, S. Hindmarsh, M. Jennings, D. Martin, C. Fisher, P. Gammon, A. Prez-Toms and P. Mawby, “3C-SiC Transistor with Ohmic Contacts Defined at Room Temperature”, *Electron Device Letters*, Vol. 37, pp. 1189-1192, 2016.
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Abstract

Attributed to the superior electrical and thermal properties, wide band gap semiconductors have been considered as the next generation electronic materials, among which 4H-SiC is the most mature technology. Even though, currently wide band gap devices are still not widely adopted, mainly due to the much higher cost compared with conventional Si devices. Large area 3C-SiC wafer grown directly on Si substrate is considered as one of the approach to make wide band gap materials more cost attractive. As such, this thesis is focused on the developments of fabricating semiconductor devices on 3C-SiC/Si materials.

A degenerate wide band gap semiconductor is a rare system. In general, dopant energy levels lie deeper in the band-gap and carriers freeze-out even at room temperature. Nevertheless, we observed that heavily doped n-type degenerate 3C-SiC films are achieved by nitrogen implantation level of $6 \times 10^{20} \text{ cm}^{-3}$ at 20 K. Free donors are found to saturate in 3C-SiC at $7 \times 10^{19} \text{ cm}^{-3}$ and fully thermally ionized at 150 K. Ohmic contacts (Ti/Ni bilayer) were manufactured on these implanted 3C-SiC surface and the electrical characterisation revealed the unique accumulation-type metal-semiconductor interface. As-deposited Ti/Ni Ohmic contact was obtained with low contact resistivity around $2 \times 10^{-5} \Omega \cdot \text{cm}^2$ and even lower contact resistivity approaching $1 \times 10^{-6} \Omega \cdot \text{cm}^2$ was achieved by performing a post metallisation annealing at 1000°C for 1 min after the contact deposition.

Both lateral MOS capacitors and lateral MOSFETs were fabricated on 3C-SiC(001)/Si wafers to study the 3C-SiC/SiO₂ interface. Oxidation temperature above 1200°C turned out to have negligible influence on the final MOSFET peak channel mobility. O₂ dry oxidised MOSFETs readily have a relatively high mobility around $70 \text{ cm}^2/\text{V.s}$ while a N₂O post oxidation annealing further increases it to $90 \text{ cm}^2/\text{V.s}$. LDMOSFETs were fabricated on 3C-SiC(001)/Si wafers. Despite of the low current density of $1.37 \text{ A}/\text{cm}^2$, it is still more than 10 times higher than the 4H-SiC reference device. Finite element simulation demonstrated that the 3C-SiC/Si lateral device current density can be greatly increased (above 3 times) using novel RESURF structures.

Nomenclature

AFM	Atomic force microscopy
BJT	Bipolar junction transistors
C-TLM	Circular transmission line method
C-V	Capacitance-Voltage
CMP	Chemical-mechanical polishing
CTE	Coefficient of thermal expansion
CVD	Chemical vapour deposition
FE	Field emission
FET	Field-effect transistors
FWHM	Full width half maximum
GaN	Gallium nitride
IGBT	Insulated gate bipolar transistors
M-S	Metal/semiconductor
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
PIA	Post-implantation annealing
PMA	Post metallisation annealing
POA	Post-oxidation annealing
RCA	Radio Corporation of America
RESURF	Reduced surface field
RIE	Reactive ion etching
RTA	Rapid thermal anneal
SF	Stacking faults
Si	Silicon
SiC	Silicon carbide
SIMS	Secondary ion mass spectrometry
slm	Standard litre per minute
TE	Thermionic emission
TEM	Transmission electron microscopy

TFE	Thermionic-field emission
TLM	Transmission line method
WBG	Wide band gap
XPS	X-ray photoelectron spectroscopy
XRD	X-ray powder diffraction
α_n	Electron impact ionization coefficient
α_p	Hole impact ionization coefficient
χ	Semiconductor affinity (eV)
ΔV_{fb}	Flat band voltage shift (V)
$\Delta \Phi_B$	Schottky barrier lowering (eV)
μ_{ch}	Channel mobility ($\text{cm}^2/\text{V.s}$)
μ_{epi}	Epilayer electron mobility ($\text{cm}^2/\text{V.s}$)
μ_{FE}	Field-effect mobility ($\text{cm}^2/\text{V.s}$)
μ_{n0}	Bulk electron mobility ($\text{cm}^2/\text{V.s}$)
μ_{p0}	Bulk hole mobility ($\text{cm}^2/\text{V.s}$)
Φ_B	Schottky barrier height (eV)
Φ_M	Work function (eV)
ρ_c	Contact resistivity ($\Omega.\text{cm}^2$)
ρ_{imp}	Implanted layer resistivity (Ω/square)
ρ_{sh}	Sheet resistivity (Ω/square)
σ	Surface potential fluctuation
τ_{it}	Trap time constant (s)
ϵ_0	Vacuum permittivity (F/cm)
ϵ_{ox}	Oxide dielectric constant
ϵ_s	Semiconductor Dielectric constant
φ_s	Surface potential (eV)
ς	Energy difference between semiconductor conduction band minimum and Fermi level (eV)
A^*	Effective Richardson constant
C_m	Measured capacitance (F)
C_{ox}	Oxide capacitance (F)
C_p	Parallel capacitance (F)
C_s	Semiconductor capacitance (F)
D_{fix}	Fixed charge density (cm^{-2})
D_{it}	Interface trap density ($\text{cm}^{-2}\text{eV}^{-1}$)
E_{00}	M-S interface characteristic energy (eV)
E_c	Conduction band edge (eV)
E_d	Donor activation energy (eV)
E_f	Fermi level (eV)

E_g	Band gap (eV)
E_i	Intrinsic level (eV)
E_v	Valence band edge (eV)
G_m	Measured conductance (S)
g_m	Gate trans-conductance (S)
G_p	Parallel conductance (S)
h	Planck constant (J.s)
I_{ds}	Drain-source current (A)
k	Boltzmann constant (J/K)
L_{ch}	Channel length (m)
L_{fp}	Field plate length (m)
L_t	Transfer length (m)
$m_{d,e}$	Effective mass of density of states
m_{tun}	Electron conductivity effective mass
N_a	Acceptor concentration (cm ⁻³)
N_C	Effective density of states in conduction band (cm ⁻³)
N_d	Donor concentration (cm ⁻³)
n_i	Intrinsic carrier density (cm ⁻³)
q	Magnitude of unit electronic charge (C)
R_{ch}	Channel resistance (Ω)
R_c	Contact resistance (Ω)
R_{sh}	Sheet resistance (Ω)
t_{imp}	Implanted layer thickness (m)
T_{ox}	Field oxide thickness (m)
t_{ox}	Gate oxide thickness (m)
V_{br}	Breakdown voltage (V)
V_{ds}	Drain-source voltage (V)
$V_{fb,ther}$	Theoretical flat band voltage (V)
V_{fb}	Flat band voltage (V)
V_g	Gate voltage (V)
V_{satn}	Electron saturation velocity (cm/s)
V_{satp}	Hole saturation velocity (cm/s)
V_{th}	Threshold voltage (V)
Z_{ch}	Channel width (m)

Chapter

1

Introduction

In spite of two world wars, the last century still witnessed the biggest science and technology leap ever in human history. The fashion in which people live today is nothing like it was a century ago: automobiles instead of horse-powered wagons, telephones and emails instead of hand-written letters, and so on. Modern life style is supported by the invisible yet enormous engineering systems. Electricity powers countless domestic and industrial systems nowadays and represents the highest level of human attainment. Electrification is considered, by many, as the most important engineering achievement in 20th century [1]. However, electricity barely exists in nature and the huge amount of electricity keeping modern civilisation active every day is converted from other primary energy sources on earth.

1.1 Energy Crisis and Global Warming

From year 1900 to 2000 the world annual energy consumption increased by a factor of 10 [2], and this increasing demand was mainly met by fossil fuels (coal, oil or natural gas), which can be simply burned to extract the energy chemically contained. The high energy density and considerable large stocks made fossil fuels the most affordable, thus most popular energy source. Right now the global energy system is still massively dependent on fossil fuels, even though they are well known as non-renewable. The creation of fossil fuels took millions of years, clearly not matching up with the continuously increasing global energy demand, pushed by both population growth and modernisation of developing countries. It is therefore reasonable to believe that one day, the fossil fuel reserves on earth will run out and serious consequences will follow if we fail to find an alternative energy source before that. The “Energy Crisis” so it is called, a word frequently heard in the beginning of 21st century. Despite some up and downs in the history, the global oil price has seen a continuous increase, although there are debates that the reasons behind may be more politics related.

The energy crisis raises public concerns on continue using fossil fuels, whereas environmental issues may lead to the real end of it. Since the mid-20th century, it was observed that there had been an increase in global mean temperature, known as “Global Warming”, which is directly related to the rise of greenhouse gas concentration in atmosphere. From year 1750 to 2015, concentration of CO_2 in atmosphere increased 40% [3]. It is generally

accepted that human activities, particularly fossil fuel combustion whose main product is CO_2 , had caused this global warming [4]. To prevent catastrophic climate change, there had been warnings from environmental scientists that by 2050, the global greenhouse gas emission needs to drop 40% compared with the current level [5], and efforts are urgently needed towards a low carbon society. The EU is targeting an 80% reduction of CO_2 emission by 2050 compared with 1990 levels by stepping down gradually: 40% by 2030 and 60% by 2040 [6]. Such targets are impossible as long as fossil fuels remain as primary energy sources. Alternative energy sources such as wind, solar, tidal, hydro and nuclear were extensively studied in the past several decades. Today many places of the world have put them into use, contributing to the global energy usage, even though still a small portion yet getting bigger every day.

1.2 Power Electronics in a More Electric Society

Once in the electrical form, energy can be converted to do mechanical work with high efficiency generally above 90%. More importantly, this conversion process is emission free: electricity is as clean as what it is generated from. The low carbon society proposed by most organisations and governments requires an upgrade of the current electricity grid. A “Smart Grid” as many call, in which carbon-free or very low-carbon power plants are connected to almost all society sectors such as transportation, industry, and agricultural. In short words, everything can be electrical should be electrical, namely a more electric

society. Power electronics has been one of the most important parts in the existing energy chain, fulfilling its responsibility whenever an electrical energy conversion is required. In power electronics systems, semiconductor devices are switched to process electrical energy, thus also called power devices to be different from their roles in microelectronics, where electrical information is processed instead. A more electric society will bring a huge change in the power electronics industry, which is entering a new territory that used to be ruled by heat engines as seen in Figure 1.1. Of course, opportunities are usually accompanied by challenges. Potential applications now are expanding beyond 10 kV and 1 kA for some very heavy duty jobs that are out of the reach of most power devices currently on the market.

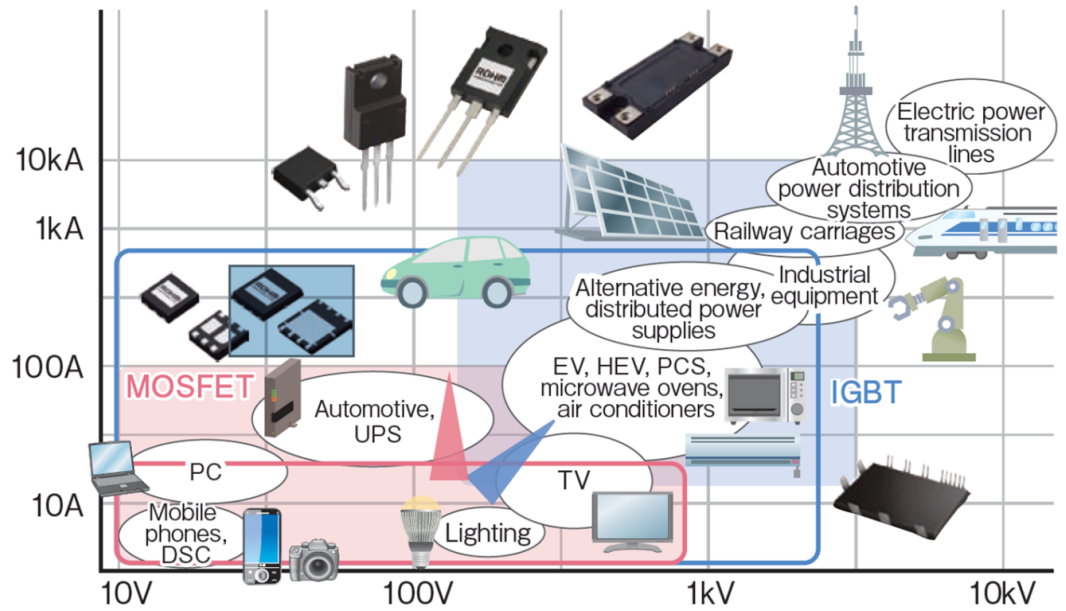


Figure 1.1: Expanding range of power devices applications [7].

1.3 Silicon Carbide instead of Silicon

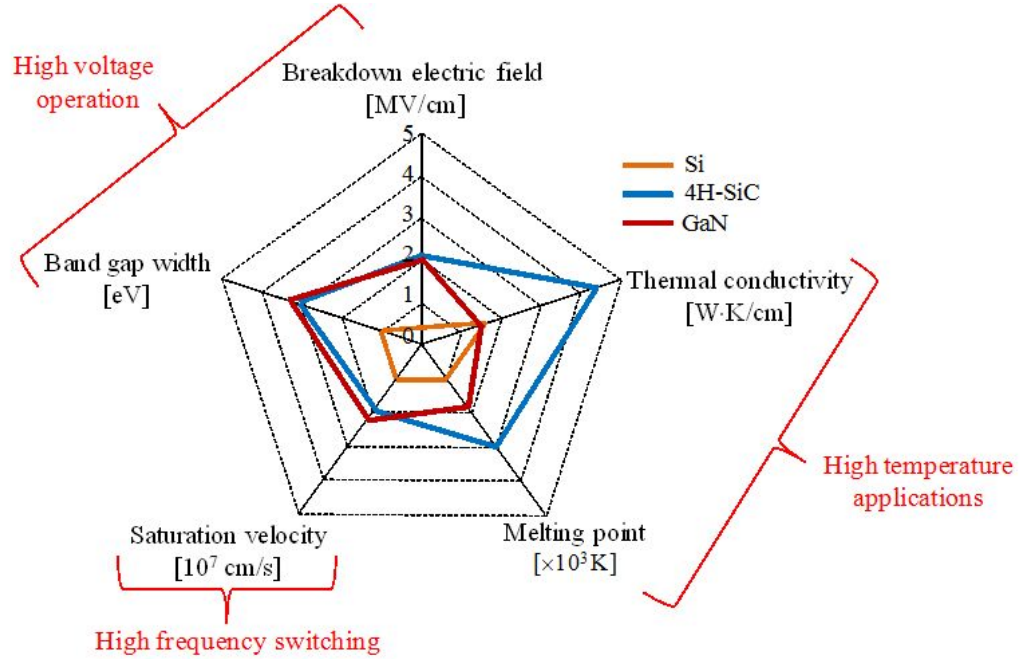


Figure 1.2: A comparison of Si, SiC, and GaN relevant material properties [8].

Silicon (Si) has dominated the electronics industry ever since it was born. In power electronics area, nearly all commercial power devices are made of Si nowadays. However, due to the target of a more electric society as mentioned earlier, there has been a continuously increasing demand of power devices working in more harsh conditions such as higher power, higher temperature, higher frequency or even higher radiation, some of which are well beyond the physical limits of Si. For the first time, the position of Si is challenged by some other materials, most of which have a larger bandgap than Si, thus called Wide Band Gap (WBG) semiconductors, including Silicon Carbide (SiC), Gallium

Nitride (GaN) and diamond. SiC is the most promising candidate at the moment. With more than twenty years of developments, SiC technology is most mature among WBG semiconductors with commercial devices readily on market [9, 10]. A comparison of the mostly considered material properties for designing power devices is shown in Figure 1.2, which clearly demonstrates the electrical advantage of SiC over Si and its thermal advantage over GaN. And most importantly, SiC is the only WBG semiconductor with SiO_2 as the natural oxide. SiO_2 is used extensively in power devices as an insulator, a dielectric and diffusion barrier [11].

Power electronics system will benefit a lot from adopting SiC devices. For example, power inverters composed of Si Insulated Gate Bipolar Transistors (IGBT) and fast recovery PiN diodes are most commonly used for electric vehicles currently on markets [12]. Generally these devices work at 600-1200 V with current density around 100 A/cm², and have maximum operational junction temperatures of 150°C to 200°C depending on the package technology [13]. The high voltage demand favours the use of IGBT instead of metal-oxidesemiconductor-field-effect transistor (MOSFET) as power switches, mainly because of the fact that MOSFETs on-state resistance (namely conduction losses) increases quickly with the blocking voltage. IGBTs do not have this limitation thanks to the bipolar conductivity modulation effect [14]. Usually, unipolar devices such as Si MOSFETs and Schottky diodes are only used for applications with voltage demand lower than 200 V [15]. On the other hand, however, high reverse recovery currents of IGBT and PiN diodes limit the inverter switching frequency to below 25 kHz [16], much lower than

the hundreds of kHz achievable by MOSFETs. SiC MOSFETs and Schottky diodes can greatly upgrade the inverter efficiency. For a 55 kW rated inverter, just by replacing the Si freewheeling diodes with SiC Schottky diodes, the whole drive system can see a 10-30% reduction in energy losses [17], which means less cooling requirements namely smaller size, higher power density ($W/Litre$). Power density is one of the most important parameters in power electronics design for mobile environments such as vehicles, trains and aviation.

Cost, on the other hand, is currently what hinders the wide application of SiC power devices. Size of semiconductor wafers used for devices fabrication is the key indicator of cost. Manufacturing cost changes little between different wafer sizes, while larger diameter wafer yields more devices, consequently lower cost per device, as can be described by Equation 1.1 below:

$$Cost/device = \frac{\text{Wafer cost} + \text{Manufacturing cost}}{\text{Number of devices per wafer}} \quad (1.1)$$

Nowadays, in industry SiC usually refers to 4H-SiC, which has been most studied so far mainly due to the availability of high quality commercial wafer substrates. With years of development, 150 mm diameter 4H-SiC wafers have recently been demonstrated by the industry [18], who potentially can reduce 4H-SiC devices cost by half. Even though, its cost disadvantage is still obvious in comparison with Si devices fabricated on 200 mm or even larger wafers, not to mention that 4H-SiC wafers themselves are also much more expensive, because of the much higher thermal budget [19] and a new fabrication line to

deliver it. Surely 4H-SiC devices can be made smaller for the same power level, namely higher power density, attributed to its superior electrical properties, this compensation does not change the fact that 4H-SiC still cannot compete with Si in terms of cost. The cost concerns, however, potentially can be solved by growing 3C-SiC, another SiC polytype, directly on large area Si wafers, by which cost per device can be greatly reduced. Growth of 3C-SiC on Si had been in research for years and 150 mm 3C-SiC wafer with device fabrication feasibility was demonstrated in 2003 [20]. Recently, 300 mm single crystal 3C-SiC wafer was also reported in labs [21]. These are all exciting news for 3C-SiC power devices developments and provided great inspirations for the research carried out here in University of Warwick, which will be demonstrated in this thesis.

1.4 Thesis Outline

In the next chapter, an introduction to 3C-SiC technology is made, including the material properties, growth and defects. Physical characterisation results of the 3C-SiC/Si wafers used in this work are discussed. Chapter 3 introduces the implantation and activation of nitrogen heavily implanted 3C-SiC films. The effects of activation annealing conditions are systematically studied to check various parameters effects on the electrical properties of resultant films. Chapter 4 continues the work by fabricating low resistivity Ohmic contacts on the implanted 3C-SiC films. The electrical and physical properties of the fabricated 3C-SiC Ohmic interface are analysed using various tools, with a focus on the carrier

conduction mechanism. In Chapter 5, a thorough study on the 3C-SiC/SiO₂ interface is conducted by fabricating MOS capacitors on n-type 3C-SiC epilayers. Investigations were made to explore the effects of different oxidation conditions including temperature and precursor gas selections. The results are then fed into the fabrication of lateral MOSFETs on 3C-SiC/Si wafers as is demonstrated in Chapter 6. Both long channel lateral MOSFETs and LDMOSFETs are manufactured for channel mobility and forward conducting evaluations, respectively. Finally, Chapter 7 discusses the potential use of 3C-SiC/Si technology in power ICs.

Chapter

2

3C-SiC Properties, Growth and Characterisation

This chapter provides an overview of the physical and electrical properties of 3C-SiC. The difficulties in growing 3C-SiC on Si are then discussed and the latest growth techniques are introduced. In the end, a short summary is provided for the physical characterisation of 3C-SiC/Si wafers used in this study.

2.1 SiC Polytypes

As a compound semiconductor, SiC is different from Si that it consists of two elements, and they always bond to each other rather than self-bonding. Each carbon atom is bonded to four silicon atoms, and in turn each silicon atom bonded to four carbon ones, both in a tetrahedral fashion. The same Si-C bond, however, leads to two possible lattice cells. One is hexagonal as shown in Figure 2.1a, most SiC polytypes have this structure and are called α -SiC, apart from 3C-SiC, who has a cubic lattice (Figure 2.1b) and is called

β -SiC.

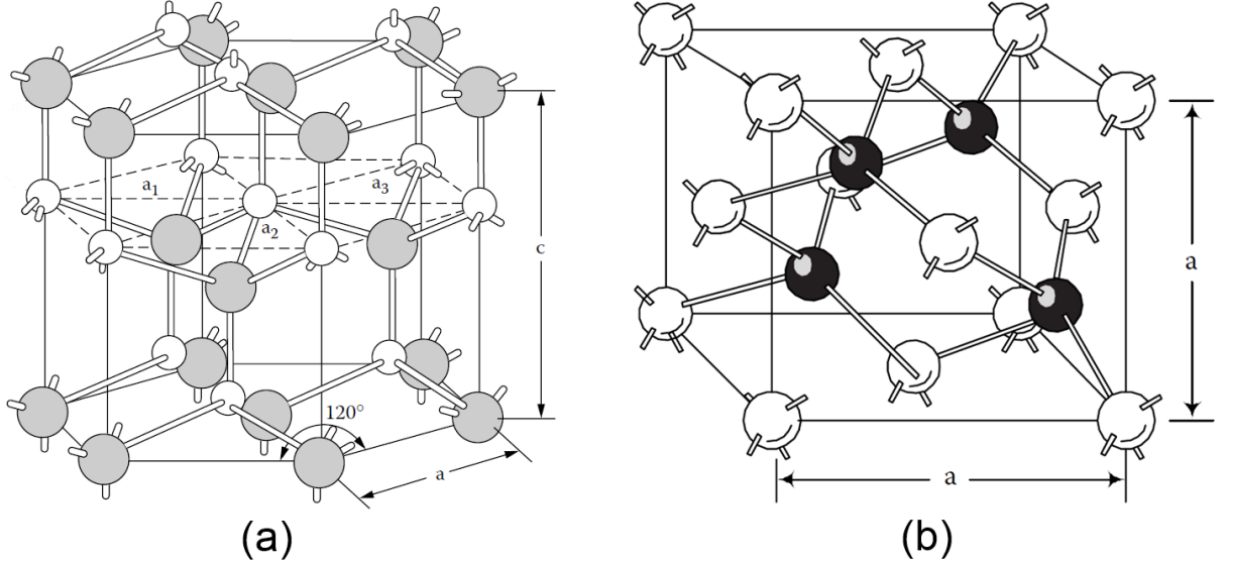


Figure 2.1: Hexagonal (a) and cubic (b) SiC lattice, dark spheres represent Si and light ones are C [22].

Considering each Si-C bond as one unit, the 2D top view of Figure 2.1a and 2.1b can then be illustrated in Figure 2.2, where each circle represents a Si-C unit. If position A is the first layer layout, subsequently the layer above it can fall into two possible positions, B and C as indicated. If it is position B, then the third layer again has two options, position C or back to position A, and this continues with the stacking of more layers. These variations lead to more than 250 SiC polytypes [23], among which three (3C-SiC, 4H-SiC and 6H-SiC) are identified as most suitable substrate candidates for power devices fabrication. The number “3” in 3C-SiC represents the three bilayer periodicity from the stacking elements of ABC shown in Figure 2.3 and the letter “C” refers to cubic. Similarly, the number “4” and “6” in 4H- and 6H- represent periodicity of 4 and 6 layers respectively,

and “H” refers to hexagonal.

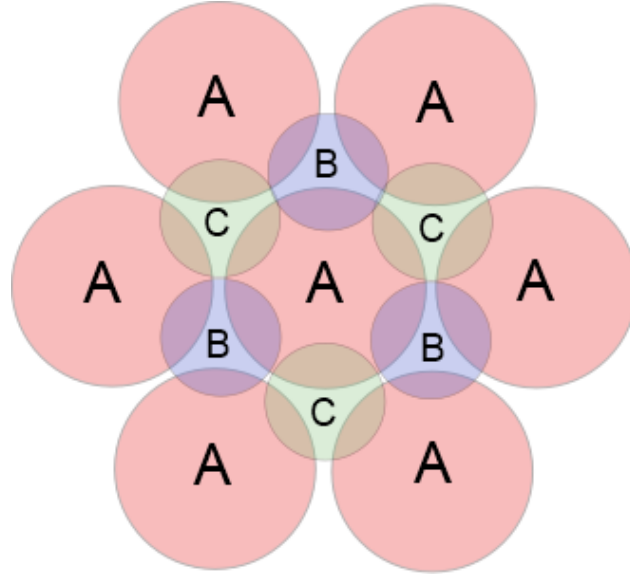


Figure 2.2: The hexagonal packing of Si-C bilayer with three potential positions.

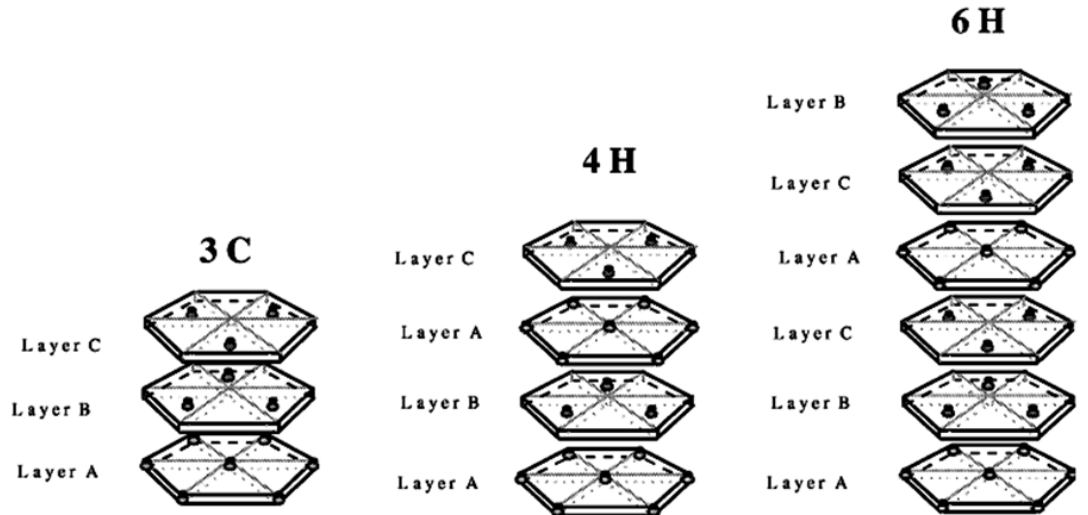


Figure 2.3: Stacking sequence of Si-C bilayer for 3C-SiC, 4H-SiC and 6H-SiC [24].

Table 2.1: A summary of main electrical properties of Si, GaN and SiC at 300 K [25].

Properties	Units	Si	3C-SiC	6H-SiC	4H-SiC	GaN
Bandgap	(eV)	1.12	2.4	3.0	3.2	3.4
Critical field	(MV/cm)	0.25	2	2.5	2.2	3
Thermal Conduct.	(W/cm.K)	1.5	3-4	3-4	3-4	1.3
Elec.Sat.Velocity	(cm/s)	10^7	2.5×10^7	2×10^7	2×10^7	2.5×10^7
Electron mobility	(cm^2/Vs)	1350	1000	500	950	1000
Hole mobility	(cm^2/Vs)	480	40	80	120	30
Int.Carrier Conc.	(cm^{-3})	$\sim 10^{10}$	~ 10	$\sim 10^{-5}$	$\sim 10^{-7}$	$\sim 10^{-10}$
Dielectric constant	None	11.9	9.7	9.7	9.7	9.5

2.2 Electrical Properties

For power devices fabrication considerations, the material electrical properties such as bandgap (blocking voltage), thermal conductivity (operation temperature), bulk carrier mobility (resistance) and carrier saturation drift velocity (switching speed) are crucial factors. A summary of the main electrical properties of 3C-SiC is shown in Table 2.1, in comparison with Si and some other WBG semiconductors.

The much lower intrinsic carrier density of SiC enables devices to operate at a junction temperature above 600°C [26] without significant leakage currents concerns. More than two times the thermal conductivity of Si and GaN makes sure that heat can be quickly extracted from SiC substrates. Critical electric field of SiC is 10 times higher than Si, with some variations depending on the polytypes. Although 3C-SiC has a narrower band gap (2.4 eV) than 6H-SiC (3.0 eV) and 4H-SiC (3.2 eV), it has the highest bulk electron mobility thus lower electrical resistance. Also, the unique cubic lattice provides the most isotropic electrical property, which is convenient from a fabrication point of view. Despite

the lower electron mobility than Si, the much thinner drift region of SiC devices for a same blocking voltage makes them much less resistive than the Si counterparts.

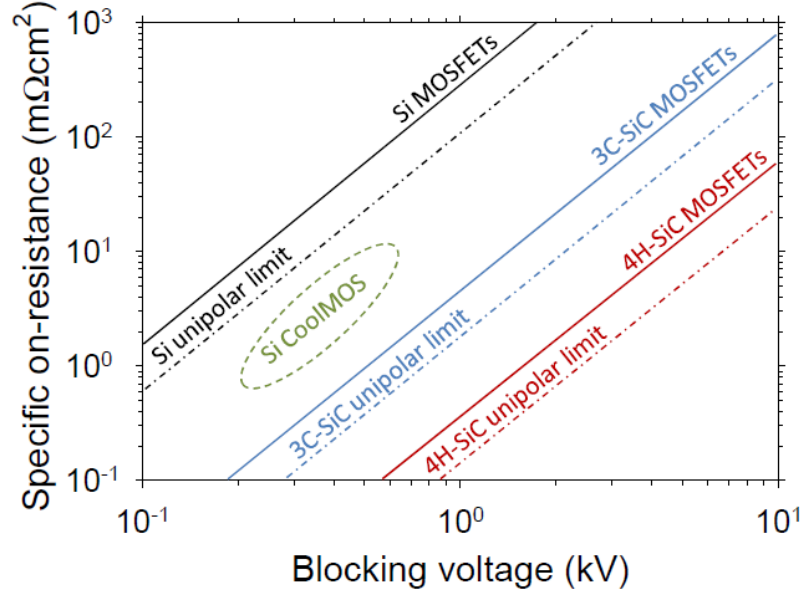


Figure 2.4: A general guide for the theoretical specific on-resistance of bulk Si, 3C- and 4H-SiC against the blocking voltage based on the one-dimensional unipolar structure [27].

It is true that 3C-SiC is not as competitive as 4H-SiC in high voltage applications targeting 10 kV and above. The device theoretical specific on-resistance is plotted in Figure 2.4 against the blocking voltage for Si, 3C-SiC and 4H-SiC based on bulk properties. Conventional one-dimensional unipolar structures without contact corner effects are assumed for the calculations in Figure 2.4, the depletion region width for specific-on resistance estimation is the minimum required for the desired blocking voltage. It seems to suggest that 4H-SiC outperforms 3C-SiC in all voltage ratings. This, however, may not be the case for real devices, whose total resistance does not only come from the bulk

region. In high voltage MOS devices design, the channel region does not contribute a significant fraction of the total resistance compared to the thick bulk drift region. For low and medium voltage devices, however, channel resistance becomes an important contributor to the total on-resistance. Figure 2.5 (blue dashed lines) shows how the specific on-resistance of 4H-SiC commercial devices rated below 1200 V suffer from high channel resistance, with the actual device on-resistance considerably higher than the unipolar limit. 3C-SiC MOS devices, however, result in much lower channel resistance, and consequently have some advantages in medium voltage (600-1200 V) applications. This is a compelling advantage to fabricating 3C-SiC power devices in addition to the cost factor mentioned before.

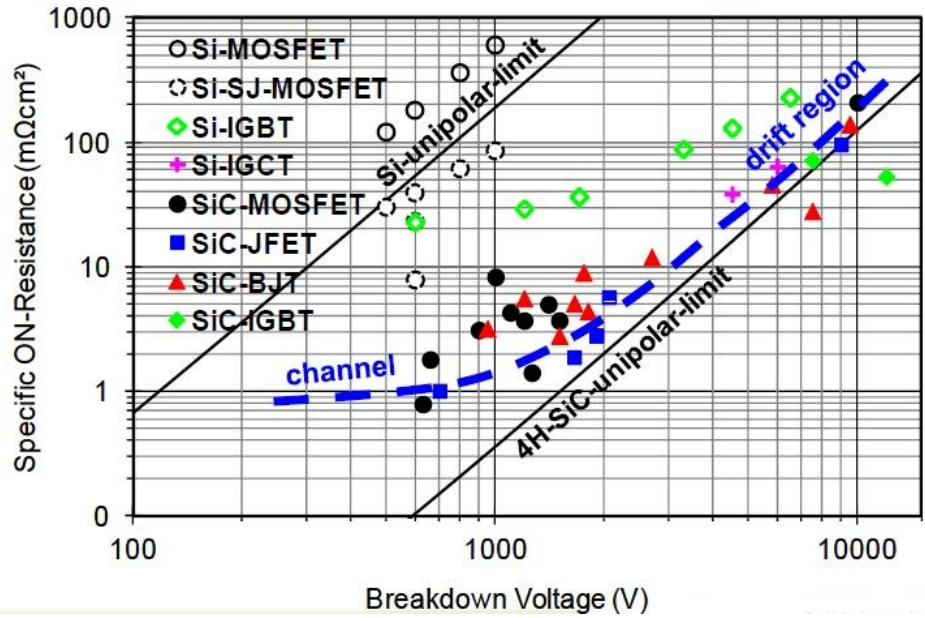


Figure 2.5: Specific on-resistance of commercial 4H-SiC devices compared to the theoretical limit [28].

2.3 Challenges for 3C-SiC Grown on Si

Regardless of the best MOS interface quality among all common polytypes, 3C-SiC power devices are not available on market mainly due to the lack of commercial 3C-SiC wafers. Behind the attractive facade of growing 3C-SiC on Si there are a few tricky issues. 3C-SiC can be readily heteroepitaxial grown on Si wafers back to 1984 [29], but these films suffered from a high density of planar defects, limiting their use for power devices. Most defects are induced by the mismatch between two semiconductors: $\approx 20\%$ in lattice constant and $\approx 8\%$ in coefficient of thermal expansion (CTE) [30]. A strain energy accumulates at the 3C-SiC/Si interface due to the mismatch, while forming planar defects tends to partially release this stress. These planar defects are generally in low energy levels thus quite stable once formed. Previous studies on 3C-SiC epitaxy layers have identified two types of defects as most important, namely stacking faults and anti-phase domains [31, 32].

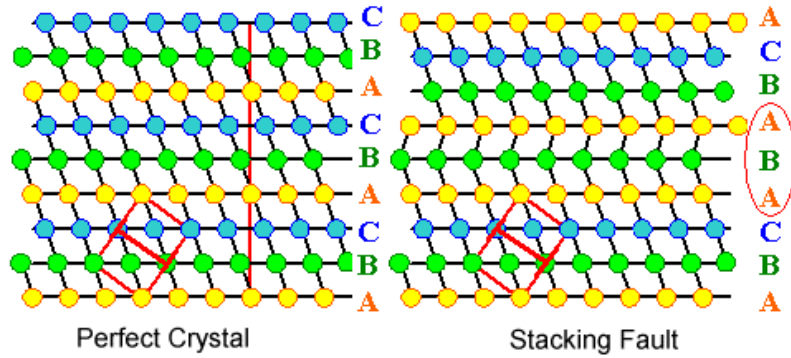


Figure 2.6: A schematic diagram of a stacking fault.

Stacking faults occur where the original stacking sequence of the Si-C bilayer is inter-

rupted, such as ABC becoming ABA as seen in Figure 2.6. They act as current paths and lead to the rise of leakage in device off-state. Theoretical calculations suggested that the forming energy of stacking faults is negative in 3C-SiC [33], which explains why it is so difficult to avoid them during the crystal growth stage.

Anti-phase domains are “killers” of power devices, less common than stacking faults yet much more harmful. They are generated due to the alignment of a polar 3C-SiC film and a non-polar Si film. In the initial growth stage, multi-nucleation of 3C-SiC occurs since Si- and C- faces are simultaneously aligned in the [111] direction [34]. With the growing process being carried on, nuclei with different polar face meet each other, forming an anti-phase boundary as shown in Figure 2.7.

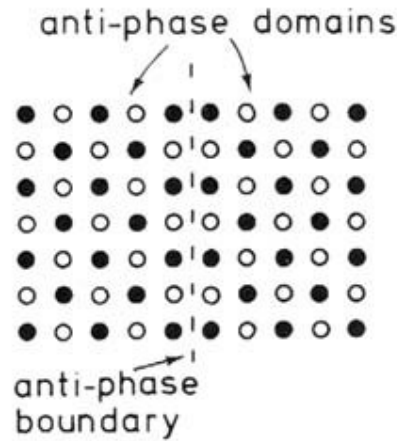


Figure 2.7: Schematic graph of anti-phase domains [35].

Another issue related to growing high quality 3C-SiC film on Si substrate is the “bowing”. The lattice and CTE mismatch between Si and 3C-SiC causes the wafer to bow

as seen in Figure 2.8, and since the 3C-SiC epilayer is usually much thinner than the Si substrate, it is more significantly affected. This obviously does not favour devices fabrication and limits the 3C-SiC film thickness because the strain increases with the epilayer thickness.

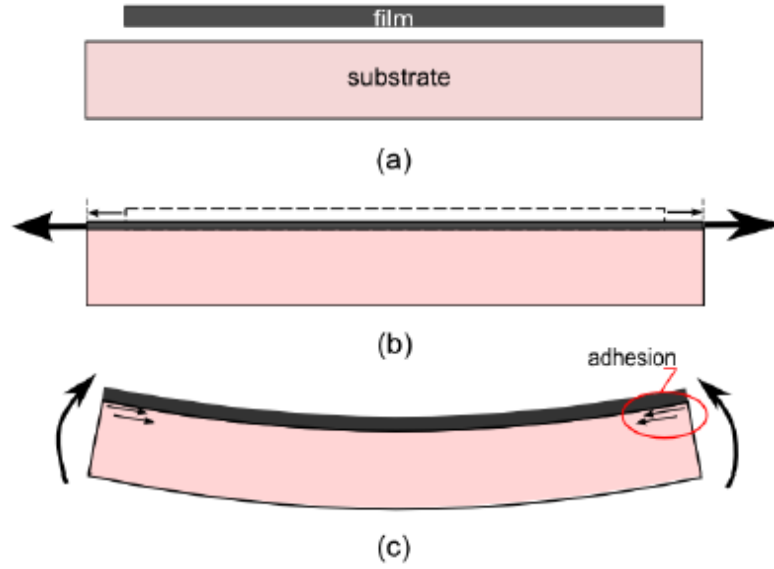


Figure 2.8: Film bow caused by the 3C-SiC/Si interface strain and thick substrate [36].

The adoption of buffer layers is a potential solution to the interface strain. Introducing a SiO_2 layer between 3C-SiC and Si, for example, is quite effective. During the growth process at a relative high temperature above 1000°C , the softened SiO_2 layer shares some of the interface stress going to the 3C-SiC film. Highly oriented polycrystalline 3C-SiC(111) films grown on poly Si/ SiO_2 /Si substrate were reported [37]. The extra poly Si layer was deposited to achieve a better lattice match with 3C-SiC. In addition, it was found that the thin poly-silicon layer (50 nm) effectively reduced the number of voids at

heteroepitaxy interface [38]. Schottky diodes were made on polycrystalline 3C-SiC film grown on similar substrates (SiO_2/Si) and achieved a breakdown voltage of 140 V, but the leakage current was quite high as 1 mA/cm^2 due to a high stacking faults density [39]. While being more economical and friendly to MEMS applications attributed to easily obtained sacrificial SiO_2 layers, polycrystalline 3C-SiC grown on oxidized Si or other SOI substrates are not very effective in reducing anti-phase domains and stacking faults, thus not great for power devices fabrications.

2.4 Chemical Vapour Deposition

Planar defects are inherently far fewer in single crystal 3C-SiC films, consequently growth of single crystal 3C-SiC are of more interests. Variety of methods such as fast sublimation [40,41] and solution growth [42,43] were reported. Some of them obtained high quality single crystal films with stacking faults density as low as $10\text{-}100 \text{ cm}^{-1}$ [42]. Nevertheless, none of them is able to produce large area 3C-SiC wafers suitable for industry scale fabrications. As a result, although not the most convenient since usually higher temperature and lower pressure than other methods are required, direct Chemical Vapour Deposition (CVD) is still mostly preferred.

Figure 2.9 shows the layout of a typical induction heated horizontal CVD reactor. Precursor gases (such as SiH_4 and C_3H_8) are transported by the carrier gas (usually highly purified H_2), into the heated reactor containing a high temperature tolerant susceptor,

on which the Si substrate wafer is loaded. Gas flow can be controlled independently by respective controllers. Reactions between precursor gases and Si substrate go through several stages subsequently as shown in Figure 2.10, after which a 3C-SiC layer is left behind on the Si substrate while most H is released in the H_2 form.

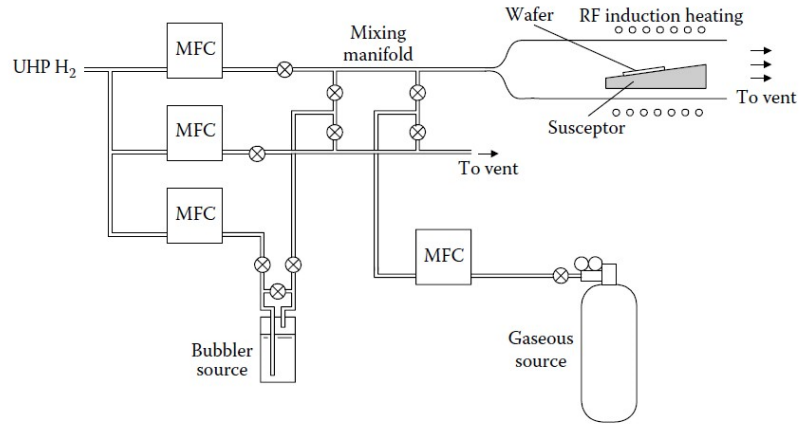


Figure 2.9: Illustration of the layout of a typical CVD system [22].

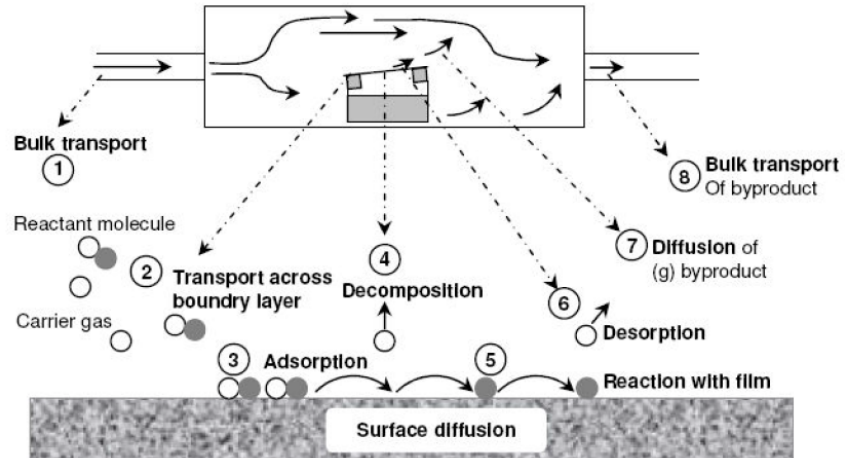


Figure 2.10: CVD reaction stages break-down [44].

The specific temperature and pressure of the CVD process varies between groups for various purposes, but typically it consists of 2 stages as shown in Figure 2.11. In the first stage, the reactor temperature is ramped gradually to a value lower than the actual growth temperature, and remains there for a period to carbonize the Si substrate surface. After that, the temperature is raised again until reaching around 1400°C, when the real growth process kicks off.

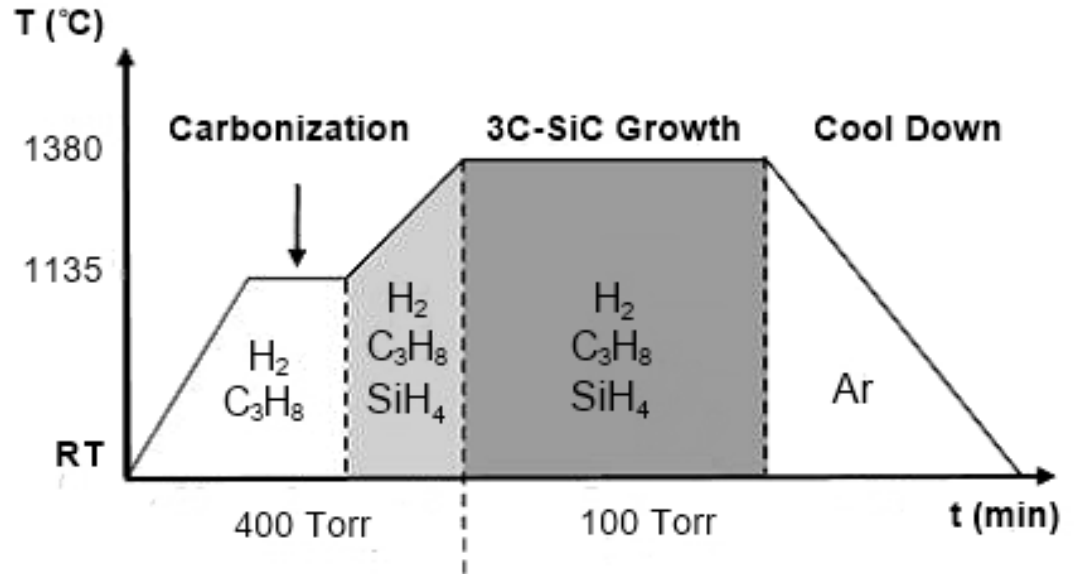


Figure 2.11: Temperature and pressure changes during a common 3C-SiC CVD process [45].

2.5 Novel Techniques Reducing Planar Defects

The research into propagation principles of anti-phase domains and stacking faults in 3C-SiC epitaxy films leads to the abandon of flat substrates. A misoriented Si(001) substrate

with 4° offset towards $[110]$ direction was found to successfully eliminate anti-phase domains in epitaxy films with increasing thickness [31]. On such tilted substrates, growing speed of domains on Si-faces are much faster than the ones on C-faces, consequently the resulting film mainly consists of domains grown on Si-faces. However, misoriented substrate was not able to reduce stacking faults, which does not only grow in a single plane. A patterned substrate is shown by recent studies [31] to effectively reduce the stacking fault density. More specifically, an undulant Si substrate which has counter slopes oriented in the $[110]$ and $[-1-10]$ directions as shown in Figure 2.12 below.

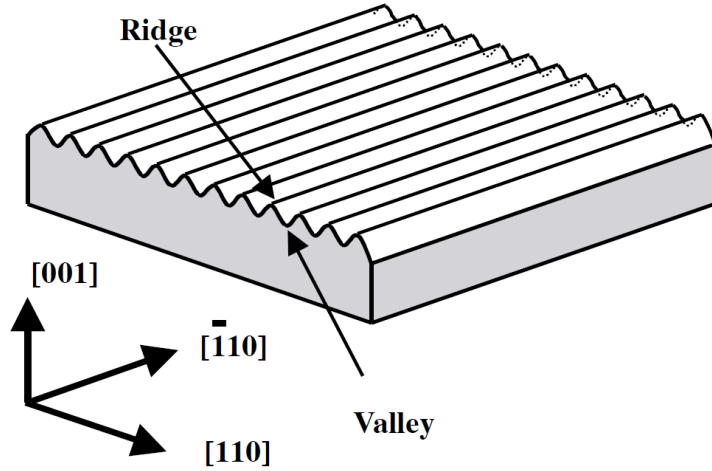


Figure 2.12: Schematic structure of undulant Si substrate [31].

The reduction was achieved by annihilation of stacking faults originated from counter ridges of the undulant substrate. Propagation principles of both Si-terminated stacking faults (SF_{Si}) and C-terminated ones (SF_C) are shown in Figure 2.13 [46]. With the increase of epitaxy film thickness, SF_C shrinks, annihilating with each other, and gradually

vanishes in the $[001]$ direction. SF_{Si} , on the other hand, expands with increasing film thickness, resulting in much lower annihilation rate. Ideally 3C-SiC should have isotropic electrical properties since it has a cubic lattice structure, while in real cases the bulk electron mobility of 3C-SiC film grown on Si had been found to be orientation dependent [31]. This is most likely caused by the density difference between SF_{Si} and SF_C , which as seen in Figure 2.13, grow perpendicularly to each other in the top view.

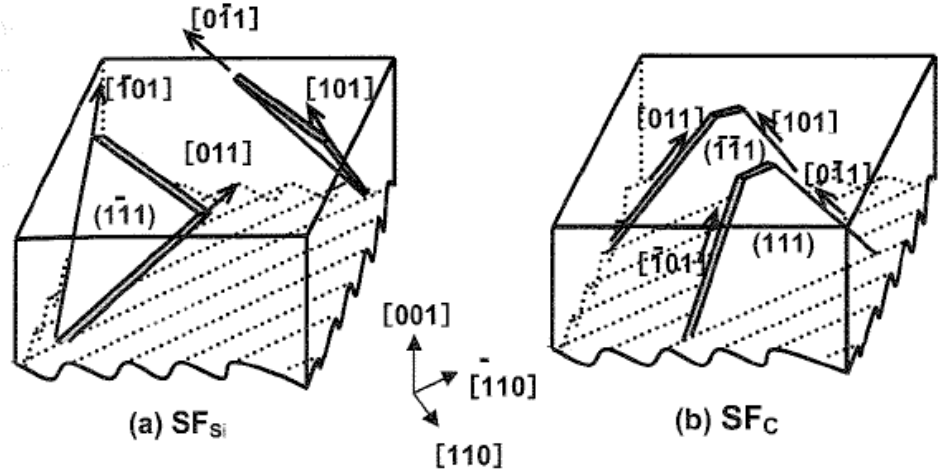


Figure 2.13: Propagation of both (a) Si terminated and (b) C terminated stacking fault in 3C-SiC [46].

Use of undulant Si substrate successfully reduced the stacking fault density to $5 \times 10^3 \sim 4 \times 10^4 \text{ cm}^{-1}$ range [47], still much higher than 700 cm^{-1} , which is considered as the threshold value for fabricating 600 V devices with leakage current below 10^{-4} A/cm^2 [46]. The epitaxy 3C-SiC film quality can be further improved by conducting homoepitaxial growth on 3C-SiC substrates, namely a hetero-homo two stage process. A switch back epitaxy [32] method was proposed to remove the 3C-SiC film from the Si substrate and invert it upside

down, in which way SF_{Si} were transformed into SF_C so can be effectively reduced by a follow-up homo-epitaxial growth on the back face. Selective epitaxial growth on patterned 3C-SiC substrate was also studied in [48], where sidewall patterns parallel to the (110) face were introduced to cause some discontinuity on the 3C-SiC(001) surface, successfully reducing the stacking fault density to less than 400 cm^{-1} . A Monte Carlo simulation-based comparison of above growing techniques for the stacking faults reduction is shown in Figure 2.14, which indicates the superior performance of the two stage growing process and the patterned 3C-SiC substrate yields the best quality epilayer. 3C-SiC on patterned Si or SOI substrate via lateral overgrowth methods were also reported in literature [49–54], while the quality are generally not as good as the homoepitaxy 3C-SiC films.

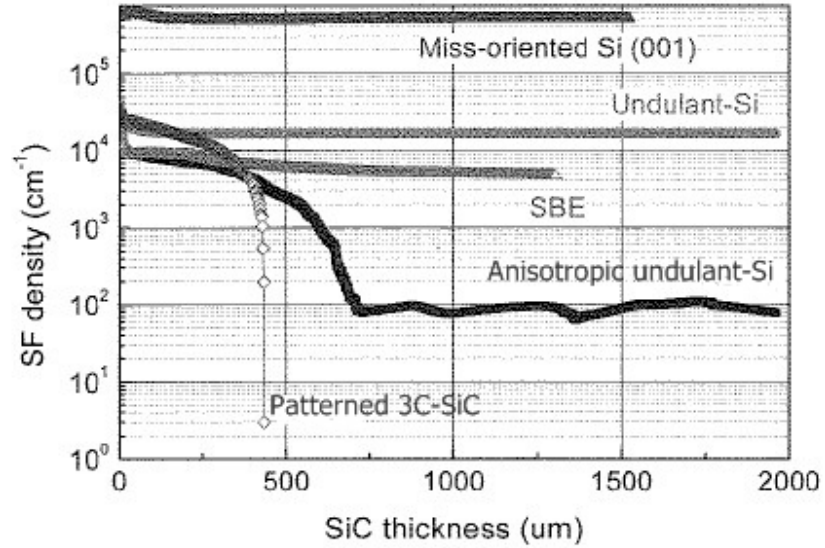


Figure 2.14: Comparison of recently developed 3C-SiC CVD epitaxy techniques in terms of stacking faults reduction [48].

2.6 Physical Characterisation of 3C-SiC/Si Materials in This Study

Despite the fact that homoepitaxy 3C-SiC film is of the finest quality for power devices fabrication, there are currently no free-standing 3C-SiC wafers on market. In this work, study materials are commercial 4 inch 3C-SiC(001)/Si wafers provided by NOVASiC. Details about the growth process are kept as classified by the supplier, but generally it follows the conventional two-stage process as described in Figure 2.11, a $\sim 1000^{\circ}\text{C}$ carbonization step followed by a 1380°C epilayer growth process. SiH_4 and C_3H_8 were used as dual-precursor gases and diluted by highly purified H_2 . As-grown 3C-SiC surfaces went through a Chemical-Mechanical Polishing (CMP) process (again NOVASiC classified) to achieve a smooth initial surface for device fabrications. Before proceeding to any further processing, a physical characterisation of NOVASiC materials was conducted using various tools including X-Ray powder Diffraction (XRD), Atomic Force Microscopy (AFM) and Transmission Electron Microscopy (TEM), and the results are summarised in following sections.

2.6.1 X-ray powder diffraction

First of all, XRD is used to evaluate the crystal structure quality of NOVASiC wafers. High-resolution XRD was performed using a Panalytical X'Pert Pro MRD equipped with a 4-bounce hybrid monochromator giving pure Cu K α 1 radiation and a solid-state

Pixel detector. $2\theta - \Omega$ “powder” scans were measured between 35 and 100 2θ degrees and the spectrum is illustrated in Figure 2.15. The only observable 3C-SiC phases are (200) and (400), and the peaks have very small Full Width Half Maximum (FWHM) angles, indicating the 3C-SiC film is single crystal with negligible polytype inclusions.

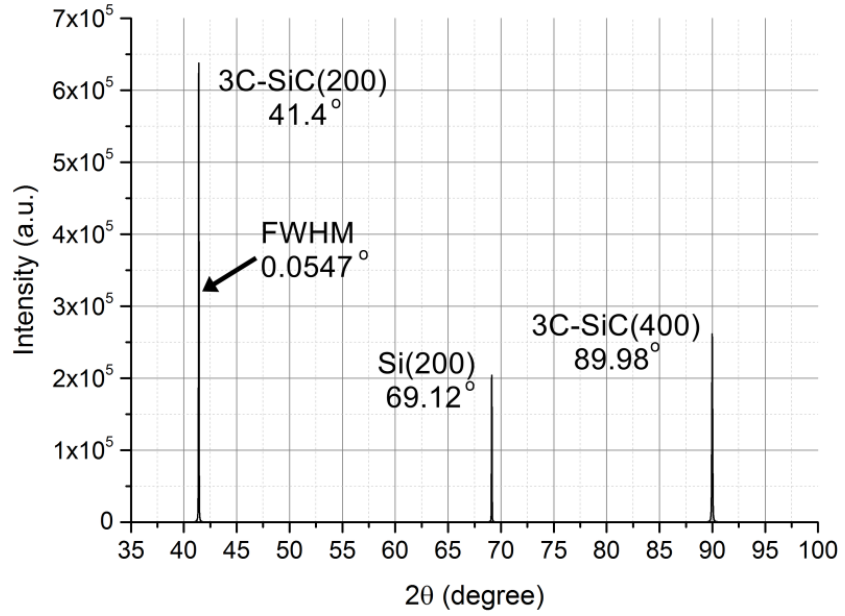


Figure 2.15: XRD spectrum of the NOVASiC 3C-SiC(001)/Si wafer (as-grown after CMP polishing).

2.6.2 Atomic force microscopy

The as-grown 3C-SiC surface condition is unknown since the wafers were received after the polishing process. AFM is used to evaluate the as-polished 3C-SiC surface. A Veeco multimode AFM with Nanonis controller was used in the contact mode with a diamond tip. A representative AFM figure as well as the 3D demonstration is shown in Figure

2.16 for reference. The as-polished 3C-SiC film surface has a quite low root mean square roughness value of 0.53 nm, an average value from five $10\ \mu\text{m} \times 10\ \mu\text{m}$ area measurements on different locations of a $1\ \text{cm} \times 1\ \text{cm}$ chip. Regardless of the potential damages left in the surface caused by CMP, this low surface roughness value is encouraging for the fabrication of most device features.

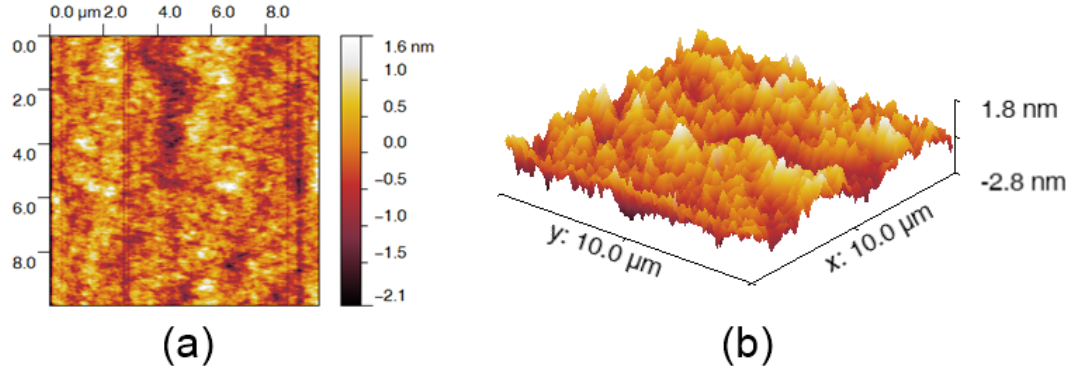


Figure 2.16: (a) A representative AFM figure of a $10\ \mu\text{m} \times 10\ \mu\text{m}$ area of the as-polished 3C-SiC surface and (b) a 3D view of the same area.

2.6.3 Transmission electron microscopy

To have a better idea of the 3C-SiC film quality, a TEM study was conducted using JEM 2100 to check the cross section of the grown epilayer. The samples were prepared with FIB-SEM utilising a standard lift-out technique, followed by low energy polishing. A montage of the scanned areas from the 3C-SiC/Si interface up to the 3C-SiC surface is shown in Figure 2.17 with enlarged views for certain regions. As can be seen, the 3C-SiC/Si interface is the mostly deteriorated region with a huge number of defects as a

natural result of interface strains concentrating here. The bright voids spotted in the Si substrate at the interface are probably a result of the Si consuming to form SiC seeds in the initial stage of growing process. Further away from the interface, the defects density gradually reduces, although never really vanishes even in the surface region. The stripes which are in parallel with the Si substrate surface are stacking faults propagating in the fashion as shown in Figure 2.13, and the inclined lines are stacking faults growing in the other direction with the opposite termination. There are no anti-phase domains being identified in the scanned region, which makes it promising for fabricating working devices on these materials, even though they probably will be troubled by leakage currents due to the considerable amount of stacking faults.

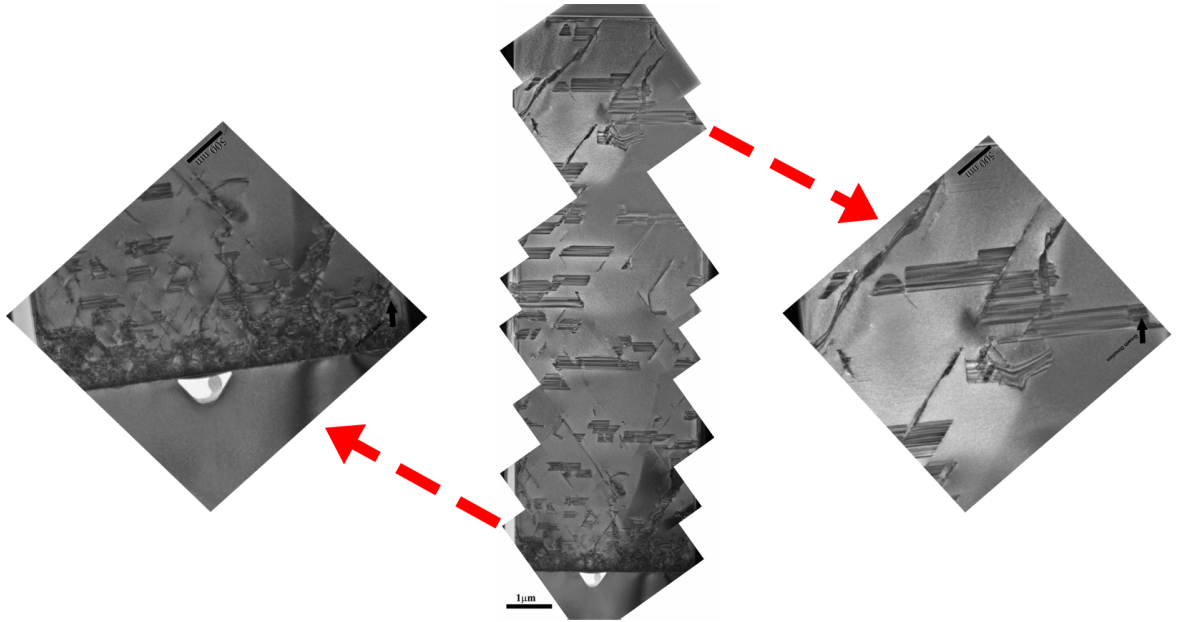


Figure 2.17: TEM montage of the NOVASiC 3C-SiC epilayer cross section with a considerable number of stacking faults.

2.7 Summary

This chapter was aimed at providing the background information related to the 3C-SiC technology with an emphasis on the topics about growth and defects. The physical characterisation of NOVASiC 3C-SiC/Si materials laid the foundation for the studies on further processing of these materials in the following chapters.

Firstly reported by Bernhard Gudden in 1930 [55], the unique electrical properties of semiconductors are attributed to the impurities within their crystal lattices. It is known that there are no chemically pure semiconductors, the frequently seen term “Intrinsic Semiconductors” actually refers to those of negligible impurities with electrical properties similar to insulators, which is dominated only by intrinsic carriers. In comparison, “Extrinsic Semiconductors” contain considerable amount of impurities, either intentionally or non-intentionally doped. If the impurity concentration becomes too high, the semiconductor becomes metallic. In other words, the electrical property of a semiconductor can be modulated by controlling its impurity concentration to meet various design requirements. As such, the study of doped semiconductor is crucial for device performance optimisation.

In this chapter, the electrical properties of implanted n-type 3C-SiC are characterised and discussed. Beginning with an introduction to the semiconductor doping and charac-

terisation tools, commonly used concepts are explained. It is then followed by a review of previous techniques developed for SiC. Finally, a study on nitrogen heavily implanted 3C-SiC films targeting device source/drain regions is demonstrated.

3.1 Intentional Doping of the Semiconductor

Impurities are usually introduced to the semiconductor bulk in early stages of a device fabrication process. The most commonly used dopants are group V elements (N, P, and As) for n-type and group III elements (B, Al, and Ga) for p-type doping purposes. The bulk doping can be relatively easily achieved by adding dopant elements into the substrate or the epilayer growth process, and the doping level can be modulated by controlling the precursor gases concentrations [56]. The epilayer surface is where most device features are. Take a typical vertical MOSFET structure as an example (Figure 3.1), multiple n-type and p-type doping regions are required for ohmic contact, MOS channel and body diode. The selective doping area can be accurately defined by doping masks made of dielectrics or metals using standard photolithography processes. Nowadays the selective doping of semiconductor is achieved mostly in two ways, namely thermal diffusion and ion implantation.

It is well-known that molecules tend to move from higher to lower concentration regions, and this process can be enhanced by increasing the ambient temperature, pressure or concentration gradient in-between. This idea is adopted in semiconductor industry to

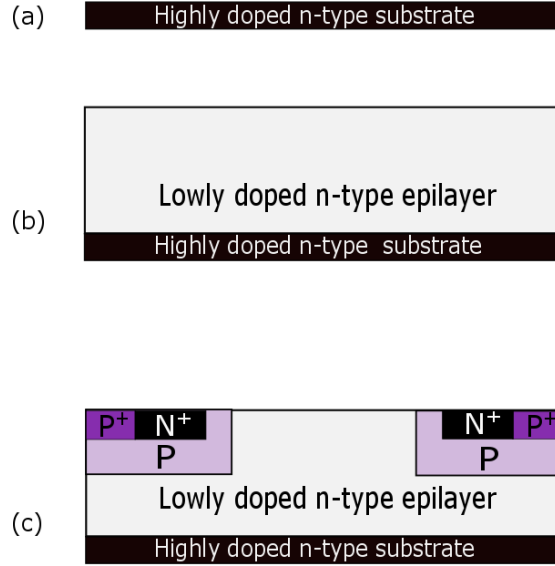


Figure 3.1: (a) Bulk substrate, (b) epilayer and (c) selective doping of a typical vertical MOSFET.

introduce impurities using dopant sources of various phases: gas, liquid or solid. Thermal diffusion based doping process often occurs in a quartz tube in an inert gas atmosphere to minimise contaminations. The dopants firstly arrived at the semiconductor surface form a relative high impurity concentration region, consequently a concentration gradient exists between the surface and bulk, after which the diffusion is initiated by the thermal energy provided. With the time going on, dopants diffuse deeper into the semiconductor bulk and when the desired doping profile is obtained, the process can be stopped conveniently by simply cutting the heat supply.

Attributed to the development of experimental physics, the ion implantation of dopants into semiconductors is also available now. Until 1970s ion implanters were still not widely

available to device engineers [57], while now they are commonly used in both lab and industry processing. In an ion implantation system, dopants are ionized atoms generated from an ion source as seen in Figure 3.2. Being ionized, the dopant atoms can be accelerated by the electromagnetic field to gain a energy so high that, when hitting the target surface, dopants are able to break the semiconductor chemical bonds and penetrate into the crystal lattices. The implantation depth can be controlled by changing the electromagnetic field strength and the resultant impurity concentration (cm^{-3}) is determined by the amount of dopants supplied by the source, which is called “Dose” and usually expressed in number per specific area (cm^{-2}).

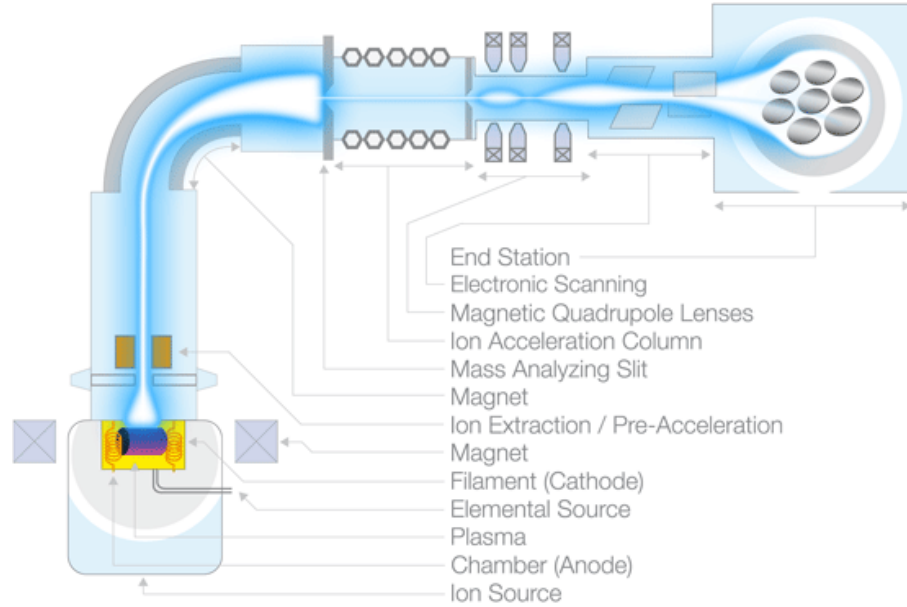


Figure 3.2: The schematic diagram of an ion implantation system [58].

For Si devices fabrication, both thermal diffusion and ion implantation can be used depending on specific requirements. For WBG semiconductors such as SiC, however,

diffusion coefficients of common dopants are negligible below 1800°C [59], which means thermal diffusion is not feasible thus leaving ion implantation the only option. Although a complex and expensive system, ion implantation is more controllable than thermal diffusion so that the process reproducibility is better assured. Also, the movement of dopants in a thermal diffusion process may involve unexpected spreading in other directions, leading to poor doping profiles. This is not an issue for ion implantation since dopants movement in the semiconductor is minimal, which means the elimination of dopants out-diffusion. There are, of course, also limitations for ion implantations. First of all, it is essentially a dopant bombarding process, which means damages are inevitably induced to the target, particularly in the surface region. Secondly, as-implanted dopants are almost always interstitial (not chemically bonded), namely not active carriers. An extra post-implantation annealing (PIA) process is typically required to recover the lattice damage and put the implanted dopants into substitutional positions so they can contribute to current conduction, which is called dopants activation.

3.2 Doping Level Characterisations

During the device development stage, it is desired that the semiconductor doping level can be measured for a better understanding of the device performance. The commonly used evaluation tools include Capacitance-Voltage (C-V) method, Hall-effect measurements and Secondary Ion Mass Spectrometry (SIMS).

For non-intentionally or lowly doped bulk regions, C-V method is an easy yet effective tool. It is known that the width of a depletion region at an electrical junction increases with the rising voltage in reverse bias. By calculating the free carrier density in each depletion region width increment, a doping profile can then be obtained [60]. The junctions studied can be semiconductor-semiconductor junction (PN), metal-semiconductor interface (e.g. Schottky) or dielectric-semiconductor interface (e.g. MOS). A more detailed introduction to the C-V technique is included in Chapter 5.

Sometimes the implanted region is very close to the surface or highly implanted, either way the depletion region is very shallow, making C-V characterisations not suitable. Hall-effect measurements can be applied in these conditions. The advantage of Hall-effect measurements is that rather than only free carrier density, it extracts more information such as resistivity, carrier mobility values from the studied material.

SIMS is widely used for general solid element concentration analysis. By sputtering and removing ionized atoms from the target, SIMS analysis can detect almost all elements concentrations above $1 \times 10^{14} \text{ cm}^{-3}$ [60]. Although it does not provide as sensitive results as C-V or Hall-effect measurements, SIMS can be useful for the ion implantation study as an independent analysis too. While both C-V and Hall-effect measurements only give electrically active dopant concentrations, SIMS outputs the total implanted dopant concentrations, regardless of being active or not.

3.3 Post-Implantation Activation of SiC

As mentioned before, a thermal annealing process is usually applied to put the dopants into substitutional positions after the ion implantation. This can be called thermal activation, to be separated from the electrical activation, which means dopants gain enough energy and get into the conduction band, becoming conducting carriers. To avoid further confusions, in the following text, “activation” will be solely used for thermal activation, while “ionization” refers to electrical activation. The activation of 4H-SiC dopants has been intensively studied and previous efforts are mainly put into two areas, namely protecting the semiconductor surface morphology and increasing the active dopant concentration.

The temperature required for SiC post-implantation activation (PIA) is very high, above 1400°C [61, 62] is common for n-type material, while even higher (>1600°C) for p-type [63–65]. The high temperature leads to a roughened semiconductor surface after annealing, enhanced in implanted regions, which can deteriorate the performance of interface features such as Schottky contacts and FET channels [66–68]. A protection capping layer is often used to preserve the SiC surface, such cap materials studied for 4H-SiC include AlN [69, 70], BN/AlN [71] and graphite [64, 67]. AlN and BN/AlN processes are found to be quite complex and expensive, thus not widely accepted. The graphite cap has been shown to be effective up to 1800°C [63] but may reduce the MOSFET channel mobility due to the excessive silicon vacancies induced by the reaction between diffused

Si atoms and the graphite [63, 72]. A SiO_2 layer, which should not react with Si or C at the common annealing temperatures, can be easily deposited by the CVD method and removed via HF etching. Studies show that a similar surface roughness level as a graphite cap [73] is achieved using this method. In the few publications on 3C-SiC, n-type implanted 3C-SiC was studied for different annealing conditions (1150°C to 1400°C) with [74] and without [75, 76] a graphite cap, and it turned out that there was little advantage of using a graphite cap in terms of protecting the 3C-SiC surface, this is probably because the annealing temperature is not high enough to make the difference, as it is limited by the melting point of the Si substrate.

For a given implanted doping level, the active dopant concentration generally increases with the PIA process temperature. And for a fixed annealing temperature, the active dopant concentration increases with the implanted doping level [77], although the percentage of activated dopants (activation rate) seems to decrease [61]. Complete activation of n-type implanted 4H-SiC have been demonstrated by annealing at 1700°C and using phosphorous as dopant [78], while p-type material still remains a challenge. For 3C-SiC, the information is again very limited, although it seems that nitrogen has some advantages over phosphorous in that it generates fewer defects and the resultant film has a lower resistivity [74]. A summary of the recent study on the post-implantation annealing of 4H- and 3C-SiC is provided in Table 3.1.

Table 3.1: A summary of the recent study on the post-implantation annealing of 4H- and 3C-SiC.

Starting substrate	Implantation procedure	Post-implantation anneal	Activation ratio	Reference
$4.5 \times 10^{15} \text{cm}^{-3}$ p-type 4H-SiC(0001)	700°C N implantation $1 \times 10^{18} \text{cm}^{-3}$ $1 \times 10^{20} \text{cm}^{-3}$	30 mins anneal in Ar at 1550°C with carbon cap	87% 21%	[61]
$1 \times 10^{16} \text{cm}^{-3}$ n-type 4H-SiC(0001)	400°C P implantation $3 \times 10^{20} \text{cm}^{-3}$	in Ar at 1650°C	100%	[62]
$1 \times 10^{16} \text{cm}^{-3}$ n-type 4H-SiC(0001)	400°C Al implantation $1 \times 10^{20} \text{cm}^{-3}$	in Ar at 1700°C with carbon cap	20%	[64]
$1 \times 10^{16} \text{cm}^{-3}$ p-type 3C-SiC(001)	Room temperature N implantation $1 \times 10^{20} \text{cm}^{-3}$	10 mins anneal in Ar at 1500°C	68%	[79]
$1 \times 10^{16} \text{cm}^{-3}$ n-type 3C-SiC(001)	RT N implantation $5 \times 10^{20} \text{cm}^{-3}$ $5 \times 10^{19} \text{cm}^{-3}$	1 hour anneal in Ar at 1350°C	17% 60%	[76]

3.4 Electrical Activation of Nitrogen Heavily

Implanted 3C-SiC(001)/Si

In this study, the PIA temperature is limited by the melting point of Si substrate, 1412°C, well below that of SiO₂ (1610°C) [68] so a SiO₂ capping layer can be a good choice. A study using deposited SiO₂ as the PIA capping layer for heavily implanted n-type 3C-SiC/Si is demonstrated below. Results are reported for sheet resistivity, dopant activation energy, activation rate and free carrier mobility as a function of following parameters: implant doses, PIA conditions and SiO₂ capping effects.

Table 3.2: Implantation doses and energies used for 3 batches of samples.

Energy(keV)	20	40	70	100	150
Low dose(cm^{-2})	2×10^{13}	4×10^{13}	4.4×10^{13}	6×10^{13}	1.1×10^{14}
Medium dose(cm^{-2})	1×10^{14}	2×10^{14}	2.2×10^{14}	3×10^{14}	5.4×10^{14}
High dose(cm^{-2})	1×10^{15}	2×10^{15}	2.2×10^{15}	3×10^{15}	5.4×10^{15}

3.4.1 Experimental details

The samples studied in this work were $10 \mu\text{m}$ thick unintentionally doped ($< 1 \times 10^{17} \text{ cm}^{-3}$) 3C-SiC films epitaxial grown on a 4 inch Si(001) substrate by NOVASiC. The wafer was cut into thirty $8 \text{ mm} \times 8 \text{ mm}$ pieces and equally divided into 3 batches. An on-axis nitrogen implantation process was conducted on the blank surface of all samples at room temperature. A series of energies with increasing total doses (shown in Table 3.2) were applied to form box profiles at three doping levels, which will be called high dose, medium dose and low dose in the following. The detailed doping profiles are shown later. Nitrogen was selected as the dopant rather than phosphorous since it does less damage to the 3C-SiC film [74, 75], although it also saturates more quickly [67].

Prior to the annealing, $1 \mu\text{m}$ thick SiO_2 was deposited on the surface of half samples from each batch via Low Pressure Chemical Vapour Deposition (LPCVD). To study the SiO_2 capping effect, one capped and one uncapped sample from each batch (six all together) went through the PIA process with continuous Ar flow at 5 slm. Five annealing conditions shown in Table 3.3 (for each condition two samples from each batch) with different temperature and time durations were applied to study the effects on resultant 3C-SiC film properties. The maximum annealing temperature applied was 1375°C . After

Table 3.3: Post-implantation activation annealing conditions.

PIA Temperature(°C)	1175	1275	1275	1375	1375
Duration(hour)	2	1	2	1	2

all the annealings, the SiO₂ cap layer was removed by HF etching. All samples were solvent cleaned (acetone, propanol, acetone and methanol, all 5 mins) followed by a standard Radio Corporation of America (RCA) cleaning procedure (15 mins RCA 1 + 15 mins RCA 2). Van der Pauw structures were then patterned using photolithography and ICP etching. The Van der Pauw structures are 1 μm deep 1 mm² square mesas with 100 μm \times 100 μm contact pads at each corner. A previously reported process [80] was used for the ohmic contacts formation in this work: Ti(30 nm)/Ni(80 nm) bilayer metal contacts were deposited at a low pressure (2×10^{-7} Torr) in an E-beam evaporator. Ti is deposited as an interlayer to improve the adhesion between Ni and the 3C-SiC surface. Ohmic contacts were annealed for 1 min at 1000°C in a Rapid Thermal Anneal (RTA) furnace in an Ar ambient. All contacts were isolated by 1 μm LPCVD SiO₂ to reduce surface recombination effects. Room temperature I-V measurements were made to study the implanted film sheet resistivity. For carrier concentrations and mobility values extraction, temperature dependent Hall-effect measurements were performed with a magnetic field strength of 800 mT and an input current of 10 μA .

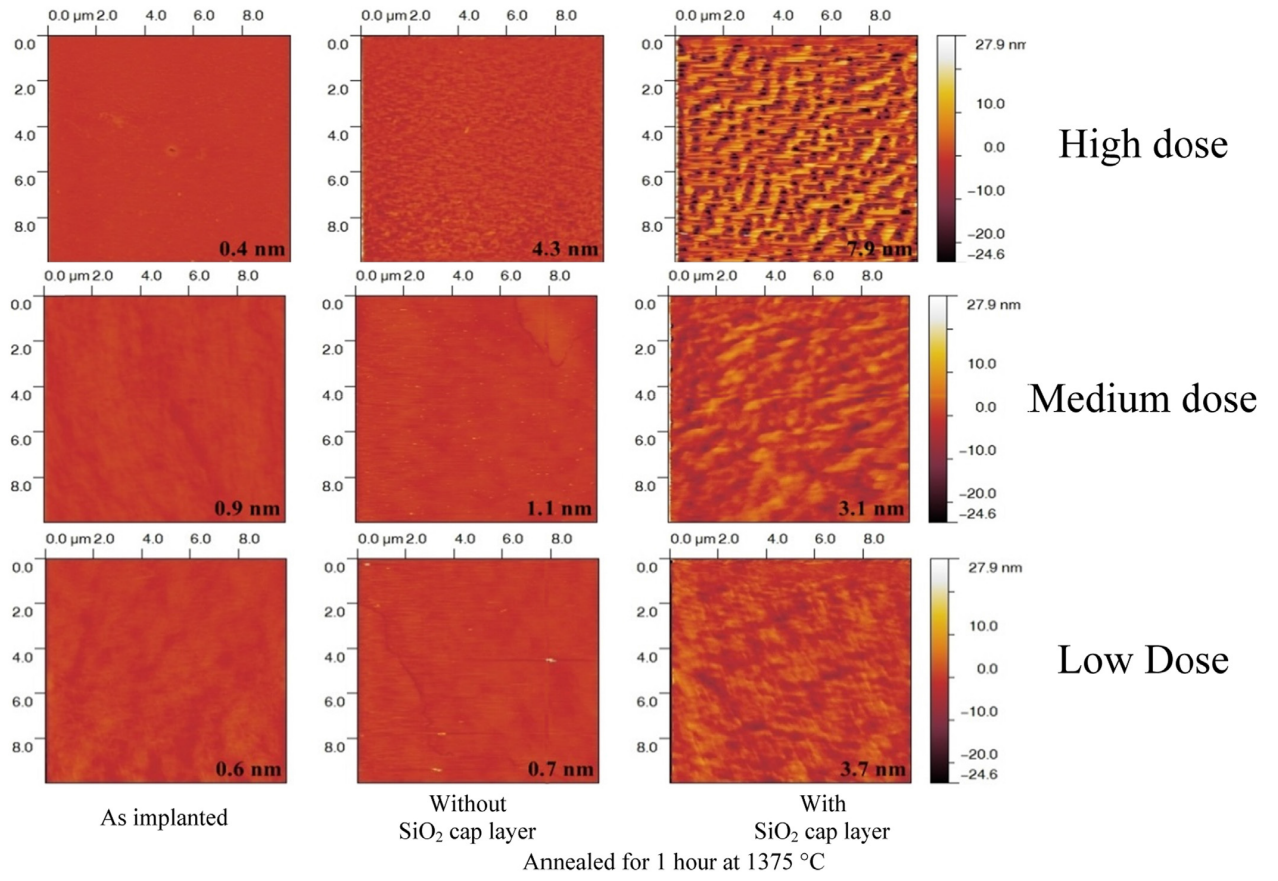


Figure 3.3: AFM images illustrating 3C-SiC surface evolutions for samples with 3 doses, inset values are RMS surface roughness values.

3.4.2 Implanted 3C-SiC surface morphology

Figure 3.3 shows the implanted 3C-SiC surface evolutions of samples from each dose batch after a 1 hour PIA process at 1375°C. It can be seen that regardless of the dose levels, all groups experienced a surface degradation, although the high dose sample surfaces were degraded more severely, indicating higher lattice damage [61, 75]. The SiO₂ capped samples were left with a higher roughness compared to the uncapped ones in all batches. A considerable amount of pits were observed on the SiO₂ capped high dose sample, resulting in a higher surface roughness value of 7.9 nm compared with as-implanted (0.4 nm) and without a cap (4.3 nm). The SiO₂ cap aimed at protecting the 3C-SiC surface seems to lead to a worse surface morphology after PIA, conflicting with the previous results on 4H-SiC [71]. This is most likely due to the interaction between SiO₂ and SiC, which was not supposed to occur at 1400°C but may be triggered by the high impurity concentration [81].

3.4.3 Doping profiles by SIMS measurements

After the PIA process, SIMS analysis was conducted on samples from each dose batch for the toughest annealing condition (1375°C, 2h) and the results are shown in Figure 3.4. The profiles before PIA are not known but are expected to be similar to the annealed ones due to the unlikely observable diffusion of nitrogen in 3C-SiC below 1800°C [74, 79]. High and medium dose samples both achieved an implantation depth of 300 nm with peak values around $6 \times 10^{20} \text{ cm}^{-3}$ and $4 \times 10^{19} \text{ cm}^{-3}$, respectively. For the low dose sample, a

depth of 500 nm was observed and the peak value was determined as around 1.5×10^{19} cm^{-3} .

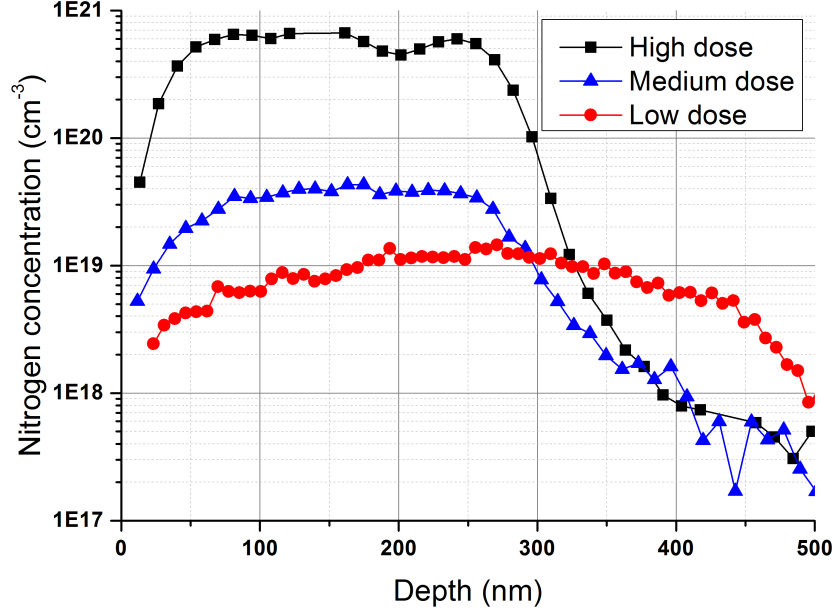


Figure 3.4: SIMS profiles for 3 dose samples after post-implantation annealing at 1375°C for 2 h.

3.4.4 Room temperature I-V measurements

I-V measurements were performed on the fabricated Van der Pauw structures at room temperature. Linear IV curves were obtained for all samples (see Figure 3.5), indicating a typical ohmic behaviour for the Ti/Ni bilayer contacts. Sheet resistivity ρ_{sh} can be calculated following Equation 3.1 [60], where t_{imp} is the implanted film thickness and R is the resistance value obtained from IV measurements using the configurations shown in

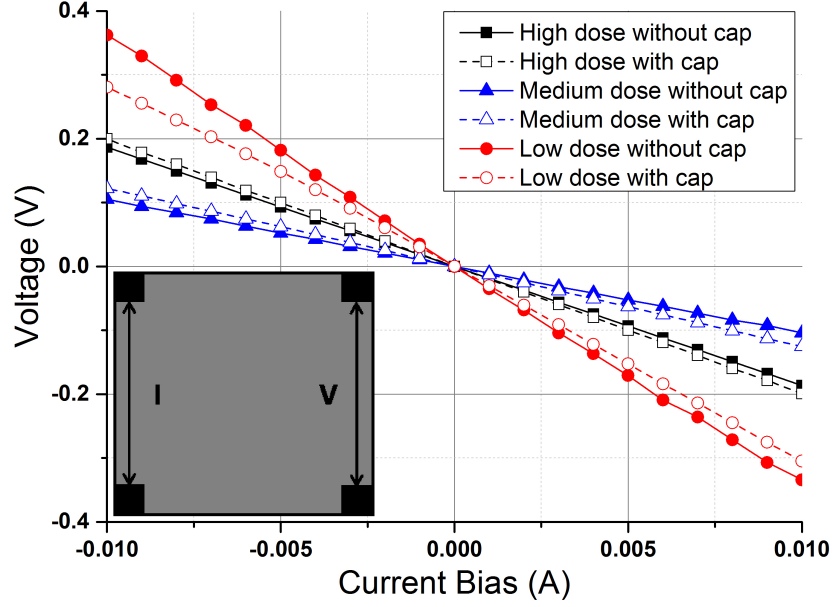


Figure 3.5: Room temperature I-V curves of Van der Pauw structures fabricated on samples annealed at 1375°C for 1 hour.

the Figure 3.5 inset.

$$\rho_{sh} = \frac{\pi t_{imp} R}{\ln 2} \quad (3.1)$$

Due to the existence of a conduction n-type epilayer (see Figure 3.6), the resistance R in Equation 3.1 can be considered as the result of paralleling the implanted and epilayer films, since the contact resistance can be reasonably neglected. Then the implanted layer sheet resistivity ρ_{imp} can be calculated following Equations 3.2 to 3.4, where T is the as-grown epilayer thickness, q is the electron charge. From the epilayer doping N_d of $1 \times 10^{17} \text{ cm}^{-3}$, the epilayer electron mobility μ_{epi} can be estimated as $763 \text{ cm}^2/\text{V.s}$ [82].

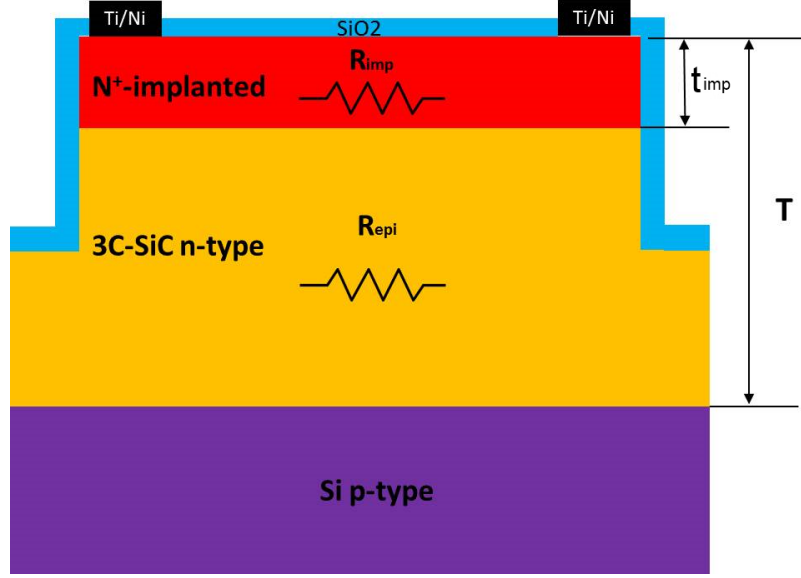


Figure 3.6: Implanted 3C-SiC layer sheet resistivity calculation model.

Calculation indicates the epilayer conduction accounts for 15-20% of the overall measured current in the low dose case and below 10% in the high dose case. The real value should only be even lower considering the current crowding at the semiconductor surface in a lateral conduction situation.

$$\frac{1}{R} \approx \frac{1}{R_{imp}} + \frac{1}{R_{epi}} \quad (3.2)$$

$$R_{epi} = \left(\frac{\ln 2}{\pi} \right) \left(\frac{1}{T - t_{imp}} \right) \rho_{epi} = \left(\frac{\ln 2}{\pi} \right) \left(\frac{1}{T - t_{imp}} \right) \frac{1}{q\mu_{epi}N_d} \quad (3.3)$$

$$\rho_{imp} = \frac{\pi}{\ln 2} t R_{imp} = \frac{\pi}{\ln 2} t \left(\frac{R R_{epi}}{R_{epi} - R} \right) \quad (3.4)$$

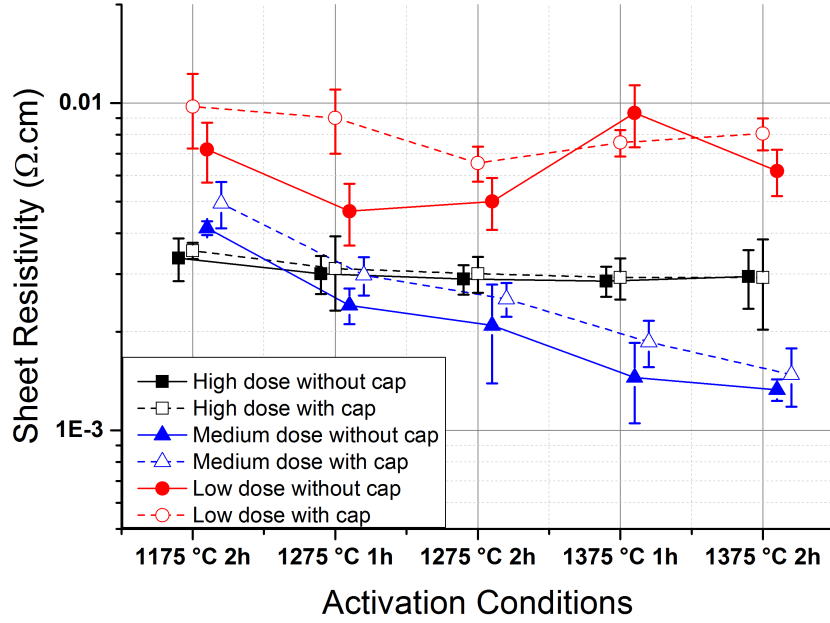


Figure 3.7: Effect of PIA temperatures and time durations on implanted layer sheet resistivity.

The resultant ρ_{imp} values (averaged from 4 devices on each sample) are plotted as a function of annealing conditions in Figure 3.7. It can be seen that for the medium doped samples (blue lines), sheet resistivity values for capped and uncapped samples both gradually decrease with annealing temperatures and time durations. The lowest sheet resistivity value is $\approx 1.4 \Omega.cm$ obtained for the 2h 1375°C annealing condition. There is more than 50% reduction comparing to the 2h 1175°C process. This trend suggests an increasing free nitrogen concentration accomplished by raising annealing temperature as well as time durations. The SiO_2 capped samples for the medium doped cases all yielded a slightly higher sheet resistivity value. Relating this to the mild surface roughening

observed on the SiO₂ capped sample compared with the uncapped one (2 nm difference in Figure 3.3), it suggests that for a doping level of $\approx 4 \times 10^{19} \text{ cm}^{-3}$, surface roughness is an important indicator of the implanted film electrical performance. For the high dose sample (black lines), the dependence of sheet resistivity on annealing conditions is so weak that can barely be identified. This is most likely caused by the saturation of donors in 3C-SiC [83], which means a higher concentration of free donors is physically impossible with higher annealing temperatures or longer time periods. There is almost no difference between capped and uncapped samples in high dose case, even with a bigger surface roughness difference (3.6 nm difference) and much more obvious surface morphology change (pits formation for SiO₂ capped sample). It indicates that for doping levels above $6 \times 10^{20} \text{ cm}^{-3}$, surface roughness has little effect and the implanted film is dominated by the impurity scattering. The low dose samples, however, demonstrate quite random sheet resistivity behaviour. A possible explanation is that in this case, all nitrogen dopants had been activated and the fluctuations in the sheet resistivity curve (red lines) actually come from the disturbance of contact resistance, which is known to be heavily dependent on the semiconductor doping level. In the next chapter it is demonstrated that the low dose sample contact resistance is one order of magnitude higher than the other two. Follow-up Hall-effect measurements also support this explanation.

3.4.5 Temperature dependent Hall-effect measurements

Temperature dependent Hall-effect measurements were performed on the high dose ($\approx 6 \times 10^{20} \text{ cm}^{-3}$) and low dose ($\approx 1.5 \times 10^{19} \text{ cm}^{-3}$) sample annealed at 1375°C for 1 hour. The studied temperature range was between 20 K and 300 K. Figure 3.8 is the temperature dependent carrier mobility curve. Due to a high impurity scattering effect, the high dose curve (black lines) shows almost no temperature dependence. In the low dose case, peak mobility value around $225 \text{ cm}^2/\text{V.s}$ is achieved at 100 K for the uncapped sample and $\approx 80 \text{ cm}^2/\text{V.s}$ at room temperature. Compared with the literature results summarized in Table 3.3 (end of the section), the values obtained in this work are in agreement with the general rule that higher impurity concentration results in reduced carrier mobility. Above 100 K, the free carrier mobility is dominated by phonon scattering and falls with increasing temperature roughly as $T^{-0.8}$, which is slower compared with the results obtained from more lightly doped epitaxial 3C-SiC layers, $\sim T^{-1.8}$ in [84] and $\sim T^{-1.2-1.4}$ in [29]. On the other hand, below 100 K, free carrier mobility drops quickly with decreasing temperature. This is probably induced by the hopping phenomenon. It was previously found in heavily doped n-type and p-type 4H-SiC films when temperature was so low that free carriers were frozen on the dopants [85, 86]. Near room temperature, the carrier conduction in a semiconductor is dominated by ionized carriers and the temperature dependence can be described by the ionization energy. In very low temperature, however, carriers are frozen to dopant atoms and the conduction band becomes almost empty, causing a

dramatic reduction of the carrier mobility. In this case, the difference in the dopant energy levels leads to the quantum mechanical tunnelling of electrons between dopant atoms, which is quite random and usually accompanies abnormal mobility and free concentration measurements, which can be seen in the low temperature region in Figure 3.9 and Figure 3.10.

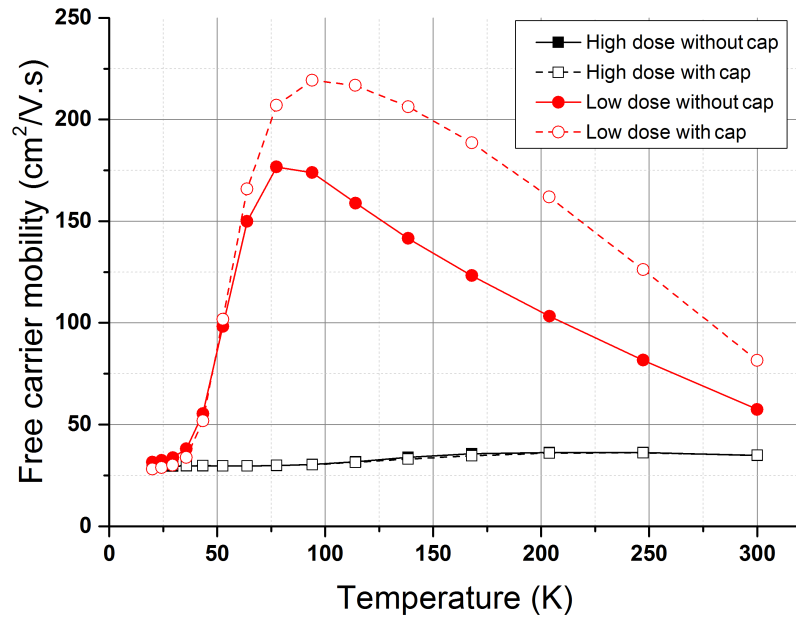


Figure 3.8: Temperature dependence of free carrier mobility for $6 \times 10^{20} \text{ cm}^{-3}$ and $1.5 \times 10^{19} \text{ cm}^{-3}$ implanted 3C-SiC film annealed at 1375°C for 1 hour corrected for the epilayer conduction).

From the almost perfectly overlapped curves for high dose sample, again it is confirmed that the SiO_2 cap has a negligible effect on high dose film electrical performance. While for the low dose sample, a considerable higher mobility is consistently observed in the whole temperature range for the SiO_2 capped sample as seen in Figure 3.8. This can be explained by a lower free carrier concentration, namely lower impurity scattering, found in

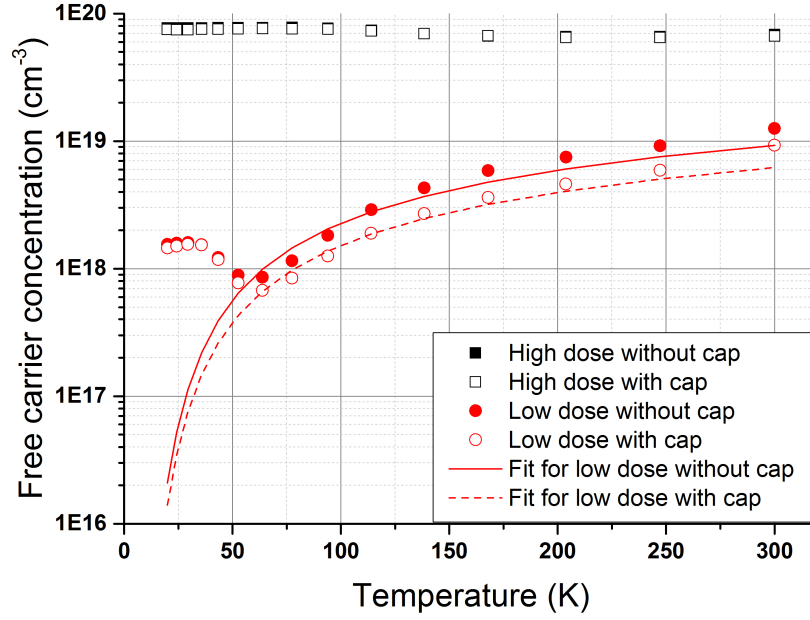


Figure 3.9: Temperature dependence free carrier concentrations for $6 \times 10^{20} \text{ cm}^{-3}$ and $1.5 \times 10^{19} \text{ cm}^{-3}$ implanted 3C-SiC annealed at 1375°C for 1 hour.

the capped sample as seen in Figure 3.9. For N+ implantation on n-type 3C-SiC epilayer in this case, the following assumptions can be made: $N_d - N_a \approx N_d$ and $1 + \alpha N_a \ll 4\alpha N_d$ with α defined by Equation 3.5 [87]. Then the temperature dependent semiconductor free carrier concentration $n(T)$ can be approximated using Equation 3.6 [87] as below:

$$\alpha = \frac{2}{N_C} e^{\frac{E_d}{kT}} \quad (3.5)$$

$$n(T) = \frac{2(N_d - N_a)}{1 + \alpha N_a + \sqrt{(1 + \alpha N_a)^2 + 4\alpha(N_d - N_a)}} \approx \sqrt{\frac{N_C N_d}{2}} e^{-\frac{E_d}{2kT}} \quad (3.6)$$

Where N_d is the free donor concentration, E_d is the donor activation energy, k is

the Boltzmann constant, T is the measuring temperature and N_C is the 3C-SiC effective density of states in conduction band, which is further defined by Equation 3.7 [87]:

$$N_C = 2 \left(2\pi m_{d,e} kT / h^2 \right)^{1.5} \quad (3.7)$$

Where $m_{d,e}$ is the 3C-SiC effective mass of density of states ($0.72m_0$ [88]) and h is the Planck constant. Using N_d and E_d as fitting parameters, best theoretical fits (red solid and dashed lines in Figures 3.9 and 3.10) were achieved with $N_d \approx 1 \times 10^{19} \text{ cm}^{-3}$ and $\approx 1.5 \times 10^{19} \text{ cm}^{-3}$ for capped and uncapped low dose samples respectively, and the donor activation energy E_d is around 15 meV.

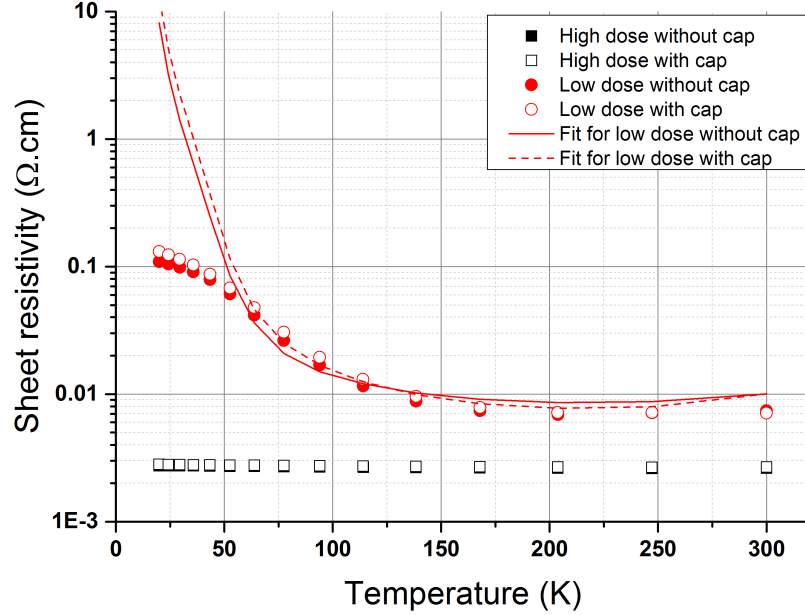


Figure 3.10: Temperature dependence of sheet resistivity values for $6 \times 10^{20} \text{ cm}^{-3}$ and $1.5 \times 10^{19} \text{ cm}^{-3}$ implanted 3C-SiC annealed at 1375°C for 1 hour.

Comparing with the SIMS profile in Figure 3.4, an N_d value of $1.5 \times 10^{19} \text{ cm}^{-3}$ indicates almost 100% activation for low dose uncapped case, while the SiO_2 capped sample yields a lower activation rate (67%). Previous results on the residual donor activation energy of 3C-SiC covered quite a range from 18 to 54 meV using various characterizing tools as shown in Table 3.3. 15 meV is lower than most of the literature values, but this is the first time that such a value ever reported for 3C-SiC epilayer with an implantation level $> 1 \times 10^{19} \text{ cm}^{-3}$. In [89] an expression was derived to show that the residual donor energy E_d in 3C-SiC decreased with the donor (nitrogen) concentration, and when N_d was around $1 \times 10^{19} \text{ cm}^{-3}$, E_d approached 0, which is similar to our case. For the high dose case, a theoretical fit is impossible indicating the degeneracy of the implanted layer. And the almost flat out free carrier concentration values ($\approx 7 \times 10^{19} \text{ cm}^{-3}$, 12% activation rate) in the whole temperature range for the high dose sample confirms the donor saturation in 3C-SiC. Figure 3.10 shows that even for the low dose sample, sheet resistivity starts to become thermal insensitive above 150 K, which means all nitrogen donors have been thermally ionized. For both the free carrier density and sheet resistivity curves, the experimental data departs from the theoretical fit below 75 K, which as mentioned before, is induced by hopping phenomenon [84]. A summary of the obtained results in this work are listed in Table 3.4 together with some literature results for comparisons.

Table 3.4: Comparison between results obtained in this work and previous literatures on n-type 3C-SiC(100), RT is room temperature.

Free carrier concentration (cm⁻³)	PIA process	E_d (meV)	RT mobility (cm²/V.s)	Reference
Not Given	None	53 (luminescence)	Not given	[90]
$1 - 3 \times 10^{15}$	None	20 (Hall)	763	[82]
$\approx 2 \times 10^{16}$	None	38 (ECR)	300	[91]
$3 - 7 \times 10^{16}$	None	18 (Hall)	400-550	[84]
$1 - 2 \times 10^{17}$	None	47 (Hall)	305	[88]
$0.5 - 1 \times 10^{18}$	None	40-50 (Hall)	120-200	[29]
$\approx 1 \times 10^{19}$ (RT, 1.5×10^{19} implanted)	1375°C 1h with SiO ₂ cap	15 (Hall)	95	This work
$\approx 1.5 \times 10^{19}$ (RT, 1.5×10^{19} implanted)	1375°C 1h without cap	15 (Hall)	70	This work
$\approx 7 \times 10^{19}$ (RT, 6×10^{20} implanted)	1375°C 1h w/o SiO ₂ cap	Degenerated	35	This work

3.5 Summary

The dependence of the nitrogen implanted 3C-SiC layer electrical performance on the implantation doses, surface preparations and annealing conditions are investigated in this chapter. The surface morphology turns out to be an important indicator for low and medium doses layer properties, while not for the very highly doped $\approx 6 \times 10^{20} \text{ cm}^{-3}$ implanted layer. Nitrogen activation rate is found to be increasing with post-implantation annealing temperature and time durations in medium dose case. For the $\approx 1.5 \times 10^{19} \text{ cm}^{-3}$ and $\approx 6 \times 10^{20} \text{ cm}^{-3}$ samples, activation rates are not much PIA process dependent. This is due to 100% activation for low dose sample and only 12% activation rate but with donor saturation for high dose case, both confirmed by Hall-effect measurements. By fitting the low dose sample experimental data points with a theoretical curve, an activation energy

value of 15 meV was extracted for nitrogen in 3C-SiC. The high dose film is found to be completely degenerated. Also, it was found that nitrogen donors in 3C-SiC are readily fully thermally ionized at 150 K.

Chapter

4

Ohmic Contact on n-Type

3C-SiC(001)/Si

In solid-state physics, a “contact” refers to the junction formed when a different material is brought into close contact with a semiconductor substrate. Regardless of the device structure, there are always contact features, usually acting as terminals in a semiconductor device design. Being the bridge between the device and the external circuit, a good contact is crucial for device operation, particularly for power electronics that are targeting harsh environments. Most metals are known to be highly electrically and thermally conductive attributed to their delocalized electrons, not to mention the convenient alloying process which helps to form reliable interactions for packaging. Consequently, metals are the most widely used material for contacts in the semiconductor industry. Dating back to Braun’s discovery in 1874 [92], the study of metal/semiconductor (M-S) interface is almost as old as the semiconductor device itself. Over a hundred years, a great deal of effort has been put into exploring the M-S interface and there are classic physics models those are

well developed. Yet still, this area remains active with new discoveries reported and novel theories developed continuously. As long as solid-state devices are still made from semiconductors and metals, the study of their interface is far away from fading into history. The emergence and adoption of WBG semiconductors raises discussions on new experimental results and the well-established theories are being challenged again.

Following the previous work on electrical activation, this chapter will be talking about fabricating Ohmic contacts on the activated 3C-SiC films. Firstly the classic and then more recent theories about M-S interfaces are reviewed, followed by a discussion on WBG semiconductors. After that the contact resistance evaluation tools are briefly introduced. Finally, Ohmic contacts are fabricated on nitrogen heavily implanted 3C-SiC(001) surface and the results are discussed.

4.1 Metal/Semiconductor Interface: Classic Theories and More

As the name suggests, the term “Ohmic Contact” is used to describe an electrical junction at which the current passing through it follows the Ohm’s Law: a linear current-voltage relationship. However, a non-linear relationship, also known as rectifying, is a more likely result after the direct deposition of metal on an intrinsic semiconductor surface. A contact with rectifying behaviour is called Schottky contact, named after the German physicist who developed the well known Schottky-Mott rule in the 1930s [93].

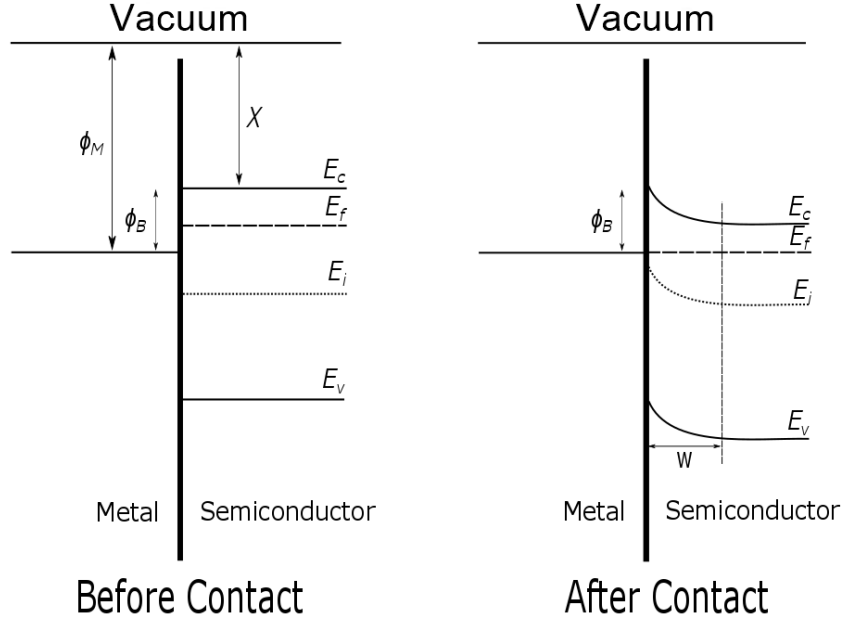


Figure 4.1: Metal-semiconductor (n-type) interface band bending before and after contact formation following Schottky-Mott rule.

This rule is based upon the conventional energy band theory. Here n-type material is taken as an example but the principle applies to p-type materials as well. Since the Fermi level in a metal is pinned (constant work function), after contact formation, to reach thermal equilibrium, the Fermi level in the metal and semiconductor will align to each other, and as a result energy bands of the semiconductor bend upwards at the M-S interface as seen in Figure 4.1. This forms a depletion region of width W and an electron exchange barrier height Φ_B (eV). Φ_B does not change before or after contact formation, and is defined only by metal work function Φ_M and semiconductor electron affinity χ as

in Equation 4.1 below:

$$\Phi_B = \Phi_M - \chi \quad (4.1)$$

It can be seen from Equation 4.1 that when $\Phi_M \leq \chi$, Φ_B becomes zero or negative. Physically this means the energy barrier for electron exchange between metal and semiconductor is eliminated, namely as-deposited (accumulation type) Ohmic contact is obtained. Unfortunately, however, Φ_M of most metals used in electronic industry are quite big compared with most semiconductor electron affinity values as shown in Figure 4.2, which also explains why Schottky behaviour is typically observed for most as-deposited metal contacts.

The Schottky-Mott rule provides a general picture of the M-S interface, experimental results, however, indicate this is not necessary the whole thing in reality. Experimental results of Φ_B values for M-S systems are usually found to be independent of Φ_M , namely Schottky barrier height is constant regardless of contact metals. This had been mainly considered to be a result of Fermi level pinning, that is, the semiconductor Fermi levels E_f are pinned to a fixed energy position in the band gap instead of aligning to Φ_M . In 1974, Bardeen was the first one to point out that Fermi level pinning may be due to non-ideal semiconductor surface states caused by defects or dangling bonds [96], a picture which is mostly accepted today.

To make it even more difficult, the barrier lowering caused by image charges also has to

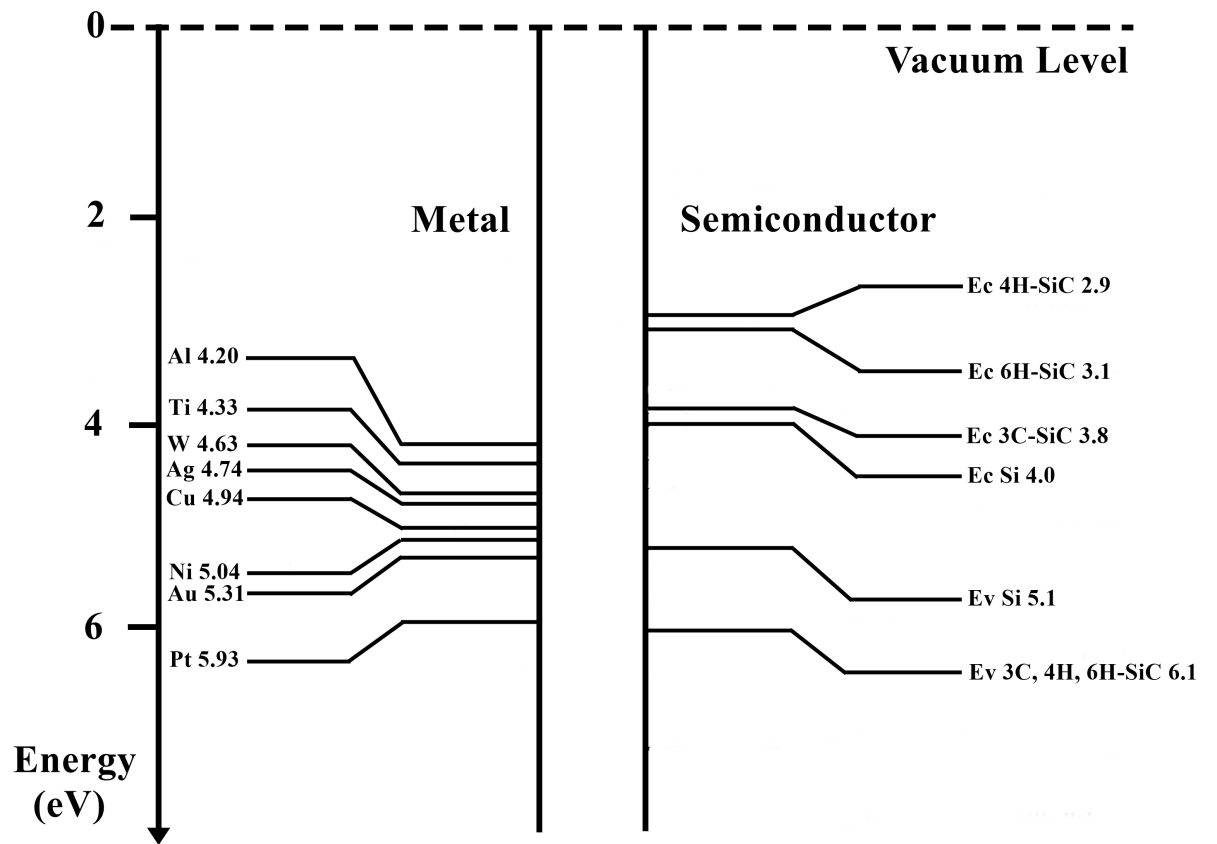


Figure 4.2: Band diagrams of Si, 3C-, 4H-, 6H-SiC in comparison to work functions of commonly used metals in electronic industry [94, 95].

be taken into consideration. When an electron in the semiconductor approaches the M-S interface, an equal yet opposite charge is created in the metal and the related potentials will reduce the effective barrier height. As a result, actual Φ_B values depends weakly on the semiconductor doping and the respective barrier lowering $\Delta\Phi_B$ caused by image charges can be calculated by Equation 4.2 below [97]:

$$\Delta\Phi_B = \frac{q^6 N_d}{8\pi^2 \varepsilon_0^3 \varepsilon_s^3} (\Phi_B - \varsigma - kT)^{\frac{1}{4}} \quad (4.2)$$

Where N_d is the n-type semiconductor free donor concentration, ε_0 is the vacuum permittivity, ε_s is the relative semiconductor dielectric constant, and ς is the energy difference between semiconductor conduction band minimum and Fermi level, which can be shown to be:

$$\varsigma = \frac{E_g}{2} - kT \ln \left(\frac{N_d}{n_i} \right) \quad (4.3)$$

Where E_g is the semiconductor band gap and n_i is the intrinsic carrier density.

$\Delta\Phi_B$ is often much lower than Φ_B so that it will not be able to eliminate the barrier, and the contact will remain rectifying. However, locally increasing N_d value by thermal diffusion or ion implantation is actually the most common way to fabricate Ohmic contacts. This is because increasing N_d value brings another effect, namely the shrinking of depletion width W in Figure 4.1. As seen in Figure 4.3 (still taking n-type as an

example), when the semiconductor is lowly doped, the depletion region is quite wide so that the electron exchange at the M-S interface is only possible when electrons overcome the barrier by gaining enough energy, usually thermally activated thus called thermionic emission (TE). If N_d is very high, the depletion region becomes very narrow, and electrons can tunnel through the barrier freely with the help of an external electric field, which is called field emission (FE) mechanism. When N_d is a middle value, the depletion region is narrowed but not enough to enable electron tunnelling. In this case, electrons still need extra thermal energy to “climb up” the barrier, but not as much as TE. The energy required just needs to be adequate for the electrons to “climb” to a position shallow enough for tunnelling begins to take effect. Since both TE and FE mechanisms are involved, this is therefore called as thermionic-field emission (TFE).

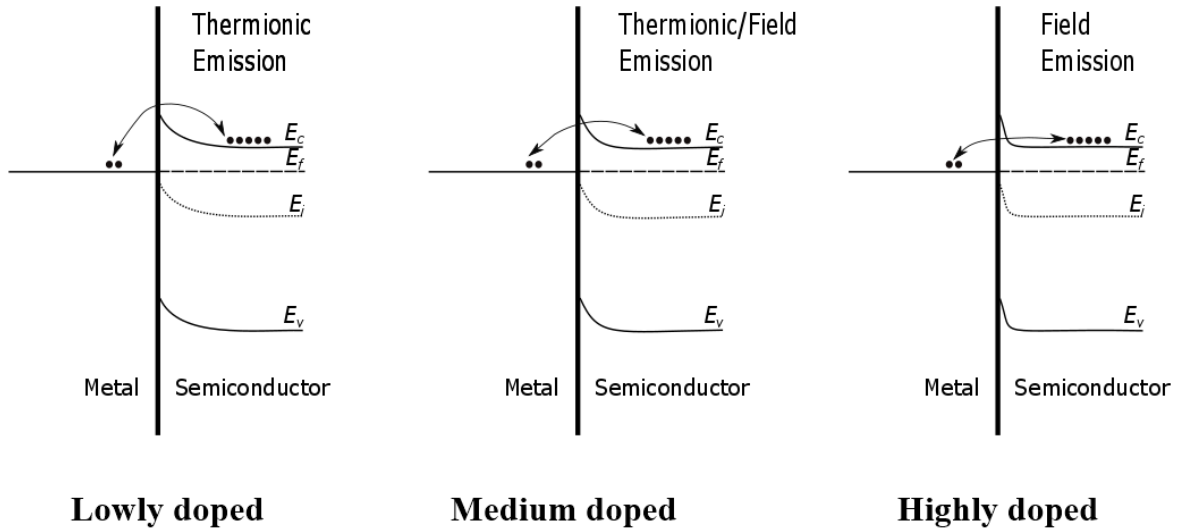


Figure 4.3: Metal-semiconductor (n-type) interface carrier conduction mechanisms for different doping levels.

FE is the most desired conduction mechanism for depletion-type Ohmic contacts, since it is not a thermally activated process, namely the electrical performance is temperature insensitive, which is attractive in a more reliable devices operation point of view. In real cases, both TFE and FE conduction are quite common. Since the contact resistance of TFE dominated cases decreases slowly with increasing temperature while FE is quite thermally stable, the conduction mechanism at fabricated Ohmic contact interfaces can be easily identified by plotting the contact resistance values against elevated measuring temperature. However, from the device design point of view, it is also vital to be able to predict the conduction mechanism before going for real fabrications. To quantitatively describe it, the M-S interface characteristic energy E_{00} , firstly proposed by Padovani in 1966 [98], is mostly used as an indicator and is expressed by Equation 4.4 as below:

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N_d}{\varepsilon_0 \varepsilon_s m_{tun}}} \quad (4.4)$$

Where m_{tun} is the electron conductivity effective mass.

The three conduction mechanisms can then be identified by comparing E_{00} to the thermal energy kT as below:

- a: if $E_{00} \ll kT$ ($E_{00}/kT \leq 0.5$), TE is the dominant conduction mechanism;
- b: if $E_{00} \gg kT$ ($E_{00}/kT \geq 5$), FE dominates;
- c: anything in between ($0.5 \leq E_{00}/kT \leq 5$) is TFE.

The specific boundaries between three mechanisms may vary a bit between research

Table 4.1: Dielectric constants and electron conductivity effective mass of Si, 3C-, 4H- and 6H-SiC [99].

Semiconductor	Dielectric constant ϵ_s	Elec. Cond. Eff. Mass m_{tun}
Si	11.7	0.25
3C-SiC	9.72	0.32
4H-SiC	9.66	0.36
6H-SiC	9.66	0.57

groups, the 0.5-5 boundary used here is proposed by Schroder [60]. From the literature values of ϵ_s and m_{tun} shown in Table 4.1, the characteristic energy E_{00} are plotted against doping levels for Si, 3C-SiC, 4H-SiC and 6H-SiC in Figure 4.4. As can be seen, to enable FE tunnelling, a doping level above $1 \times 10^{20} \text{ cm}^{-3}$ is required for all semiconductors studied here.

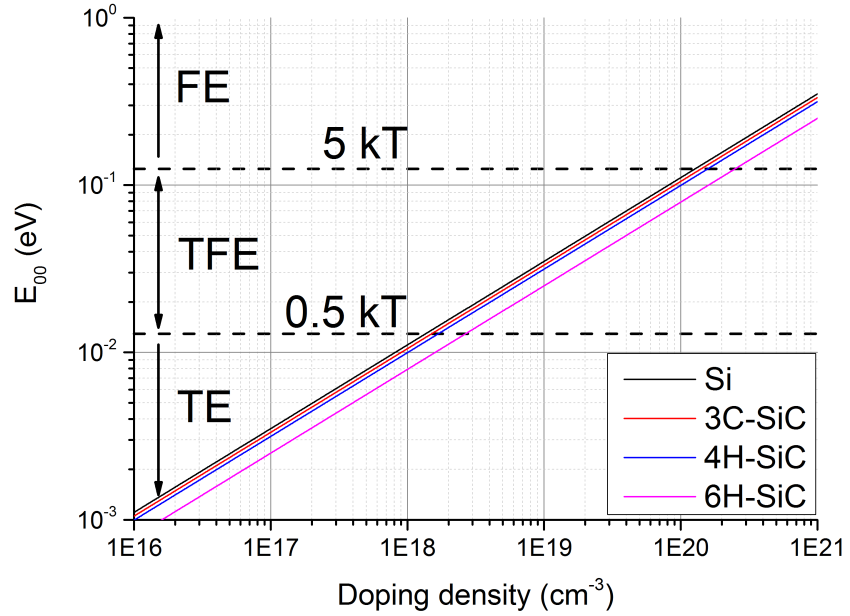


Figure 4.4: E_{00} as a function of doping density for n-type Si, 3C-, 4H- and 6H-SiC (curves generated using data in Table 4.1).

Even further, the theoretical contact resistance R_c can then be calculated for all three mechanisms using Equations 4.5 to 4.7 following Yu's model [100]:

$$TE : R_c = \frac{k}{qAA^*T} e^{\frac{\Phi_B}{kT}} \quad (4.5)$$

$$TFE : R_c = \frac{k^2}{qAA^*} \sqrt{\frac{\coth \frac{E_{00}}{kT}}{E_{00}\pi(\Phi_B + \varsigma)}} \cosh\left(\frac{E_{00}}{kT}\right) e^{\left(\frac{\Phi_B + \varsigma}{E_{00} \coth \frac{E_{00}}{kT}} - \frac{\varsigma}{kT}\right)} \quad (4.6)$$

$$FE : R_c = \frac{k^2}{qAA^*} \left[\frac{\pi kT}{\sin(\pi c_1 kT)} e^{\frac{-\Phi_B}{E_{00}}} - \frac{1}{c_1} e^{\left(-\frac{\Phi_B}{E_{00}} - c_1 \varsigma\right)} \right]^{-1}, c_1 = \frac{1}{2E_{00}} \ln\left(\frac{4\Phi_B}{\varsigma}\right) \quad (4.7)$$

Where A is the contact area, and A^* is the effective Richardson constant.

All the theoretical models discussed above consider N_d as a constant, which cannot be true for WBG materials. This is because with a wider band gap, dopants naturally sit in deeper energy levels and may not be thermally ionized at room temperature, which is known as “freeze-out” [101]. The partial ionization of carriers leads to quite different Ohmic contact performance from conventional theories. FE, for example, in which the contact resistance used to be temperature independent now will drop with elevating temperature. This is because with more dopants ionized, the semiconductor doping level closer to the contact interface increases, thus the depletion width is reduced [87], becoming

more in favour of the FE conduction. On the other hand, partial ionization also means it is more difficult to achieve lower contact resistance at room temperature. To compensate this, after metal deposition on even very highly doped SiC films, an extra annealing step is usually required to form silicides at the interface, which further lowers Φ_B , leading to a lower contact resistance.

4.2 Contact Resistance Evaluation Tools

The theoretical contact resistance calculation shown in last section can be used as a benchmark for experimental results. Actual fabricated Ohmic contacts are evaluated by specifically designed test structures. The most commonly used ones are transmission line method (TLM) and its modified variants, such as circular transmission line method (C-TLM). The main advantage of C-TLM over TLM is that it is radial conducting so the isolation mesa structure required by TLM is not necessary. However, the radial structure also requires more space on the semiconductor surface.

The TLM structure has a top and cross section view as shown in Figure 4.5. The highly doped semiconductor region (red) is defined by a rectangular mesa, usually achieved via Reactive Ion Etching (RIE). Multiple rectangular metal pads (green) are deposited on the mesa, with increasing spacing ($d_6 > d_5 > d_4 > d_3 > d_2 > d_1$) between each other. IV measurements are performed between adjacent contact pads. Four-terminal rather than two-terminal measurements are typically applied to eliminate the series resistance of

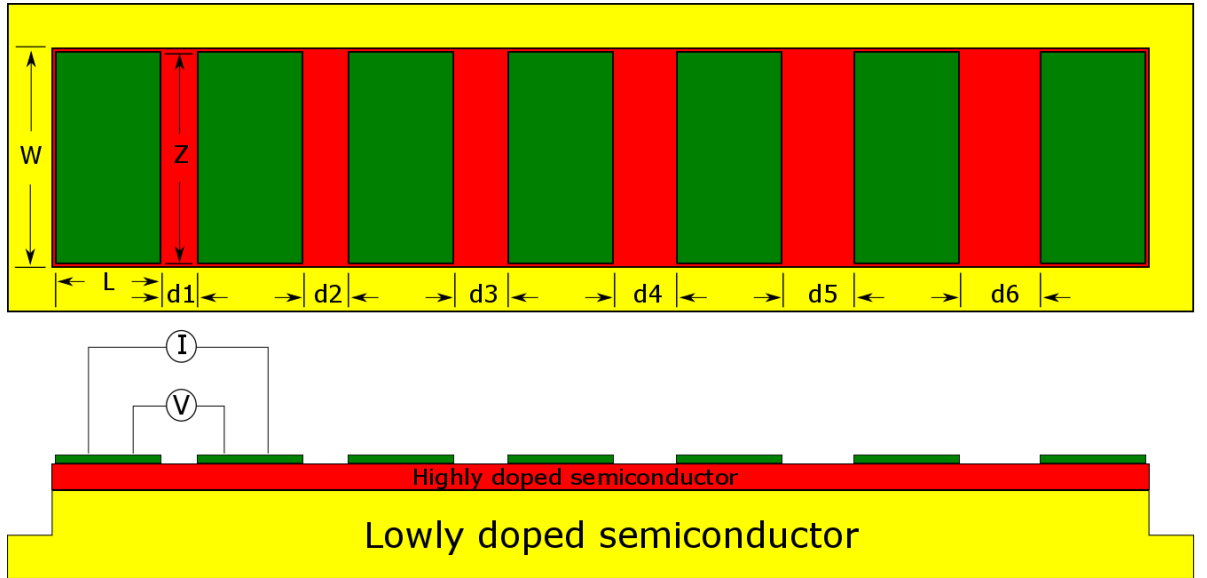


Figure 4.5: Top and cross section views of a conventional TLM testing structure.

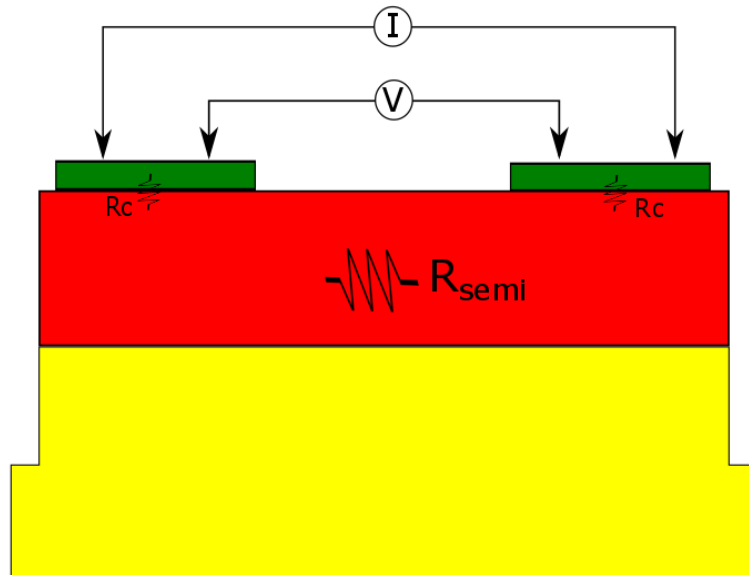


Figure 4.6: Two contact test structure using the four-terminal characterisation method.

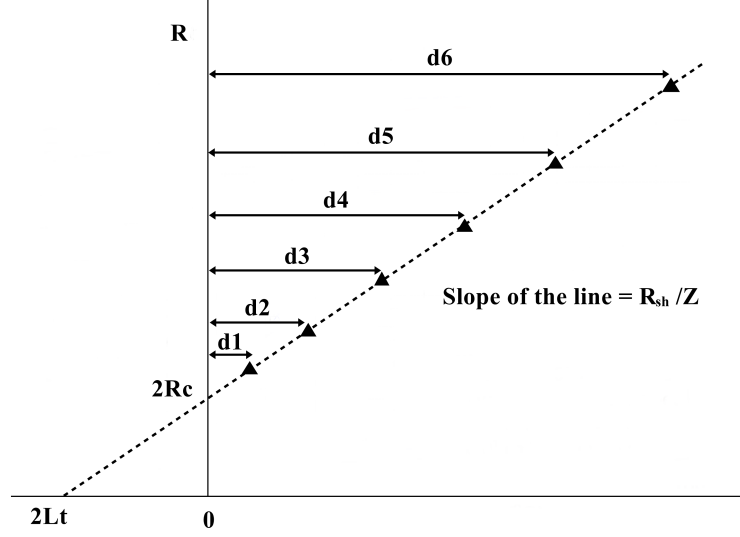


Figure 4.7: A typical plot of total resistance R as a function of contact spacing d .

probes and cables. For each measurement, if a linear IV curve is obtained, then the total resistance R between two adjacent contact pads can be calculated. Ignoring the contact metal resistance, for each measurement (as seen in Figure 4.6), the total resistance R can be considered as a combination of 3 resistors in series, two contact resistance R_c at the contact interfaces and the semiconductor resistance R_{semi} in between, which can be further expressed by the semiconductor sheet resistances R_{sh} , the contact spacing d and the pad width Z as Equation 4.8. This describes a linear relationship between R and d as seen in Figure 4.7, which should stand true considering the fact that Z is a dimension constant, and for a homogeneous semiconductor layer, R_{sh} and R_c can be treated as constants as well. This model assumes a 2D current flow between two contacts, thus any current spreading in the third dimension has to be minimized by keeping $W - Z \ll W$

(see Figure 4.5).

$$R = 2R_c + R_{semi} = 2R_c + \frac{R_{sh}d}{Z} \quad (4.8)$$

By fitting the experimental data (triangular) to a straight line in Figure 4.7, R_c can be obtained as the intersection between the fitting line and y-axis, and R_{sh} as the product of line slope and Z . Since the current going through a contact is proportional to the contact area, the current density (A/cm²) is more used as the indicator for the evaluation of semiconductor electrical conductance performance. Consequently, the extracted contact resistance R_c needs to be multiplied by the conducting area A , and the product is the contact resistivity ρ_c . However, the determination of current conducting area A can be tricky. Unlike the vertical structure commonly used in actual power devices, TLM structure has a lateral current conduction path and inevitably there is current crowding at the contact edges, which means the contact pad length L cannot be treated as the effective conducting length. Instead, a transfer length L_t , defined as the distance over which most of the current transfer between metal and semiconductor, is used for contact area calculation as seen in Equation 4.9. The L_t value can also be extracted from Figure 4.7 as the intersection between the fitting line and x-axis. Now with both R_c and L_t known, ρ_c can be calculated. In most cases, $L \gg L_t$, so that $\tanh(L/L_t) \approx 1$, and

Equation 4.9 can be simplified to Equation 4.10.

$$\rho_c = \frac{VA}{I} = R_c A = R_c Z L_t \tanh\left(\frac{L}{L_t}\right) \quad (4.9)$$

$$\rho_c = R_c Z L_t \tanh\left(\frac{L}{L_t}\right) \approx R_c Z L_t \quad (4.10)$$

4.3 A Review of 3C-SiC Ohmic Contacts

With the limited few studies of 3C-SiC Ohmic contacts, the contact resistivity values reported fluctuate in a big range from 10^{-1} [102] to $10^{-5} \Omega.\text{cm}^2$ [103]. As for any semiconductor contact study, two topics have been discussed a great deal, surface preparation and contact metal. For WBG semiconductors there is another one, namely Post Metallisation Annealing (PMA).

Depending on the growth method, 3C-SiC epilayer surface roughness can be quite different from below 1 nm [75] to as high as tens of nm [104]. To obtain a smooth initial semiconductor surface for Ohmic contact fabrication, polishing is quite often performed before any further processing. It is shown in [102] that the RMS surface roughness value dropped from 20 nm to 7.5 nm, and respectively, the contact resistivity value ρ_c was reduced by one order of magnitude, from $8.6 \times 10^{-1} \Omega.\text{cm}^2$ to $2.8 \times 10^{-2} \Omega.\text{cm}^2$. As mentioned

previously, actual device fabrication process involves a high temperature ($> 1400^{\circ}\text{C}$) post implantation annealing (PIA) process, which can potentially degrade the surface again even if polishing was performed. In [75], a thorough discussion was made on the PIA effects on the 3C-SiC surface morphology and how it is related to the resultant ρ_c values. It was pointed out that although a severe surface degradation can be a major limiting factor, the ρ_c value will not be affected much so long as the surface roughness value stays below 10 nm.

Quite a few metals, including Al [103, 105–107], Ti [103, 105–107], Ni [65, 102–104, 106–109], Ni/Ti [75, 83, 103], Au/Ti [103], Pt [109], W [65], and TiW [110] have been studied for 3C-SiC Ohmic contact fabrications, mainly for n-type materials. Amongst them, Ni seems to be the most favoured one, not only because it can achieve a low ρ_c value, but also the value has been shown to decrease with elevated PMA temperature up to $\sim 1000^{\circ}\text{C}$ [104, 107, 111]. Even though Ti and Al can achieve the same level or even lower ρ_c values, it was previously reported ρ_c increases with rising PMA temperature for these metals, which is an indicator of the Schottky barrier height (Φ_B) increase, not to mention that both of them suffer from easy surface oxidation [106]. A summary of studies on Ohmic contact for n-type 3C-SiC is included in Table 4.2 for reference.

Table 4.2: A summary of recent Ohmic contact study on n-type 3C-SiC, the contact resistivity values given are for room temperature.

Contact metal	PMA conditions	Semiconductor doping level (cm⁻³)	ρ_c ($\Omega \cdot \text{cm}^2$)	Reference
Al	As-deposited	5×10^{18} N implanted	1×10^{-4}	[105]
Al	As-deposited	3×10^{19} N implanted	6×10^{-5}	[105]
Al	As-deposited	1×10^{20} N implanted	5×10^{-5}	[105]
Al	As-deposited	3×10^{20} N implanted	1.3×10^{-5}	[105]
Al	As-deposited/ 500°C	6×10^{19} N implanted	5×10^{-7} / 6×10^{-5}	[107]
Al	300°C	6×10^{18} N implanted	5×10^{-7}	[103]
Al	As-deposited/ 500°C	$\sim 1 \times 10^{17}$ epilayer	2×10^{-4} / 1×10^{-4}	[65]
Ti	As-deposited	5×10^{18} N implanted	7×10^{-5}	[105]
Ti	As-deposited	3×10^{19} N implanted	4×10^{-5}	[105]
Ti	As-deposited	1×10^{20} N implanted	2×10^{-5}	[105]
Ti	As-deposited	3×10^{20} N implanted	1.5×10^{-5}	[105]
Ti	As-deposited/ 500°C	6×10^{19} N implanted	5×10^{-6} / 6×10^{-5}	[107]
Ni	1000°C	Not konwn, epilayer	3.7×10^{-4}	[102]
Ni	As-deposited/ 500°C	6×10^{19} N implanted	2×10^{-5} / 5×10^{-6}	[107]
Ni	950°C	3×10^{19} epilayer	1.2×10^{-5}	[103]
Ni	As-deposited/ 500°C	1×10^{17} epilayer	5×10^{-4} / 5×10^{-5}	[65]
Ni	1000°C	1×10^{20} P implanted	1.4×10^{-5}	[108]
Ni	As-deposited	Not known, polycrystal epilayer	1.6×10^{-6}	[109]
Ni	950°C	5×10^{17} epilayer	1.5×10^{-5}	[104]
Ni/Ti	1000°C	5×10^{20} N implanted	8×10^{-6}	[75]
Ni/Ti	1000°C	5×10^{20} P implanted	2×10^{-5}	[75]
Ni/Ti	1050°C	$> 1 \times 10^{20}$ N implanted	2×10^{-5}	[103]
Ni/Ti	1000°C	5×10^{19} N implanted	3.2×10^{-6}	[83]
Au/Ti	600°C	3×10^{20} N implanted	1.2×10^{-5}	[103]
Pt	As-deposited	Not known, polycrystal epilayer	1.2×10^{-5}	[109]
W	As-deposited/ 500°C	1×10^{17} epilayer	2×10^{-3} / 2×10^{-3}	[65]
TiW	1000°C	Not known, epilayer	4.6×10^{-4}	[110]

4.4 Ti/Ni Ohmic Contacts on n-Type 3C-SiC(001)

From the literature review, it is seen that although some work has been done on 3C-SiC Ohmic contacts, and low contact resistivity values below $1 \times 10^{-5} \Omega \cdot \text{cm}^2$ have been reported, the carrier transportation mechanism at the metal/3C-SiC interface was rarely discussed. In this section, Ohmic contacts were fabricated on nitrogen heavily implanted 3C-SiC(001) film. Both physical and electrical properties are characterised and discussed, with an emphasis on the carrier transportation mechanisms.

4.4.1 Experimental details

The electrically activated 3C-SiC(001)/Si samples from last chapter were used as the substrate for Ohmic contacts fabrication. All samples were annealed without any surface protection cap layer at 1375°C for 1 hour in Ar atmosphere. It has been shown that for three doping levels ($1.5 \times 10^{19} \text{ cm}^{-3}$, $4 \times 10^{19} \text{ cm}^{-3}$ and $6 \times 10^{20} \text{ cm}^{-3}$), the 1h 1375°C process was able to achieve free donor concentration above $1 \times 10^{19} \text{ cm}^{-3}$, which should be adequate for Ohmic contact formation. After the Post Implantation Annealing (PIA) process, all samples went through a standard solvent and RCA cleaning procedure before conventional TLM structures were fabricated. A Ti(30 nm)/Ni(100 nm) bilayer metal stack was deposited subsequently in low pressure (2×10^{-7} Torr) to form direct contact with the 3C-SiC surface. 4 TLM test structures were fabricated on each sample and all TLM contact pads are isolated from each other by $1 \mu\text{m}$ thick LPCVD SiO_2 to minimize

the surface recombination and the dimensions of the final test structure are shown in Figure 4.8. The surface passivation SiO_2 was deposited at $\approx 600^\circ\text{C}$ in a low pressure CVD furnace. After the contact metallisation, some of the samples were annealed in Ar atmosphere for 1 minute at various temperatures.

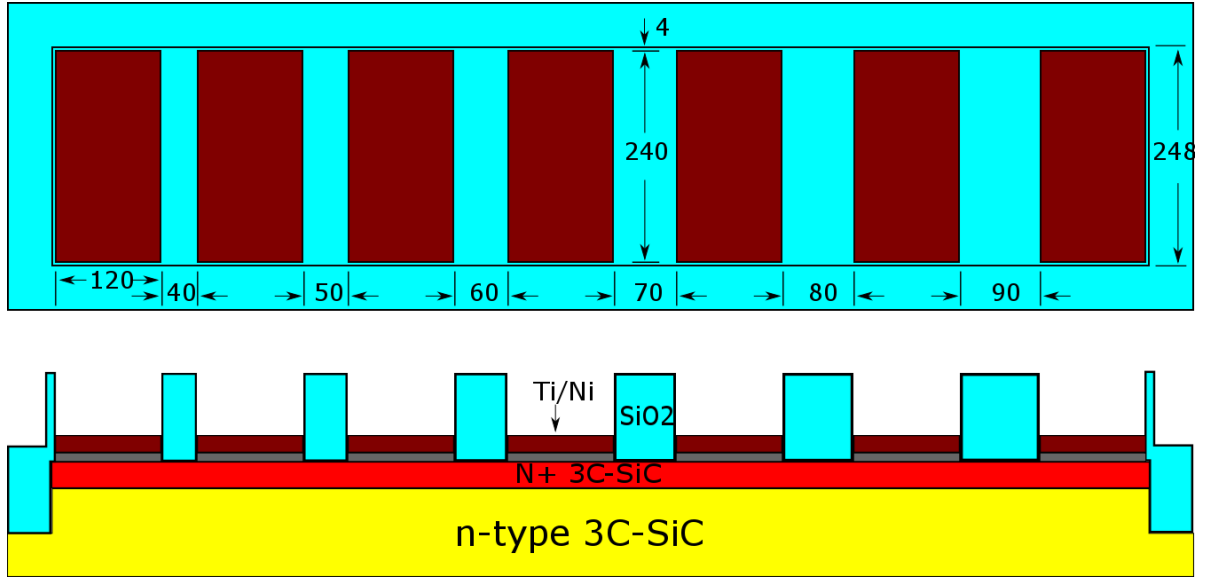


Figure 4.8: A schematic view of the fabricated TLM test structures with dimensions specified in μm .

4.4.2 Electrical characterisation

The as-deposited contacts exhibit Ohmic behaviour on the two more highly doped (4×10^{19} and $6 \times 10^{20} \text{ cm}^{-3}$) samples but rectifying on the least doped one ($1.5 \times 10^{19} \text{ cm}^{-3}$) as seen in Figure 4.9. After 1 minute RTA at 1000°C in Ar atmosphere, the lowest doped sample also became Ohmic. IV characterisations were conducted for all 5 samples ($4 \times 10^{19} \text{ cm}^{-3}$, $6 \times 10^{20} \text{ cm}^{-3}$ as-deposited and $1.5 \times 10^{19} \text{ cm}^{-3}$, $4 \times 10^{19} \text{ cm}^{-3}$, $6 \times 10^{20} \text{ cm}^{-3}$ annealed

at 1000°C) from 25°C up to 225°C. The calculated ρ_c values are plotted against the measuring temperature in Figure 4.10. It can be seen that after the contact annealing, ρ_c of the $4 \times 10^{19} \text{ cm}^{-3}$ doped sample drops significantly from $7 \times 10^{-4} \Omega \cdot \text{cm}^2$ to $4 \times 10^{-5} \Omega \cdot \text{cm}^2$, and for the more highly doped one ($6 \times 10^{20} \text{ cm}^{-3}$), from $4 \times 10^{-5} \Omega \cdot \text{cm}^2$ to $9 \times 10^{-6} \Omega \cdot \text{cm}^2$. The lowest doped sample still shows a fairly high ρ_c value of $2 \times 10^{-4} \Omega \cdot \text{cm}^2$ after RTA. The resistivity values mentioned here are for room temperature and averaged from 4 TLM structures on each sample.

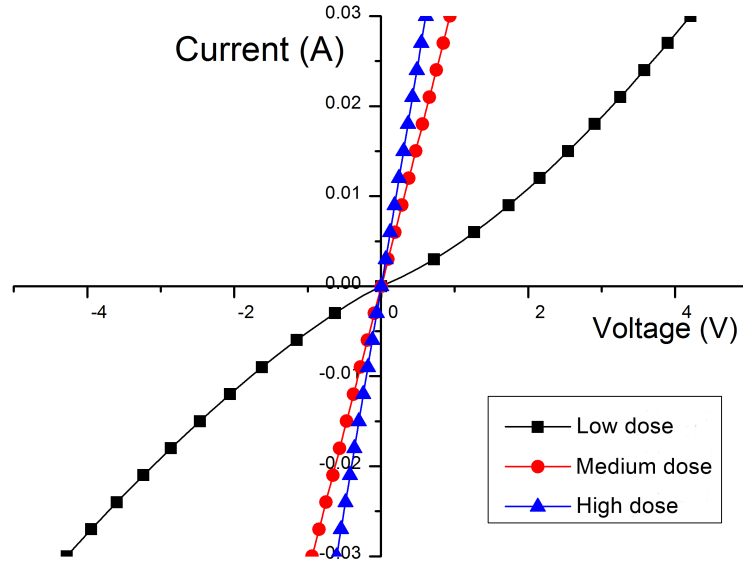


Figure 4.9: Room temperature IV characteristics of as-deposited Ni/Ti contacts on n-type 3C-SiC with 3 different doping levels: $1.5 \times 10^{19} \text{ cm}^{-3}$, $4 \times 10^{19} \text{ cm}^{-3}$ and $6 \times 10^{20} \text{ cm}^{-3}$.

Metallic contacts were known to be formed when metal was deposited onto a semiconductor surface with high density dislocations, which can then shunt the space-charge layer and make field emission the dominant mechanism [112,113] regardless of the semi-

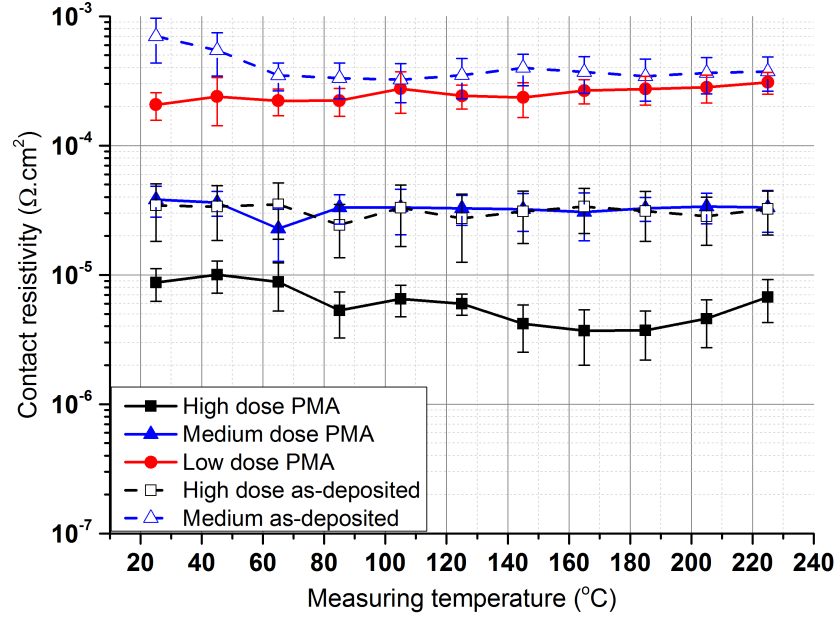


Figure 4.10: Temperature dependence of as-deposited and 1000°C annealed Ohmic contact resistivity.

conductor doping levels. Considering the 3C-SiC layer used in this study was grown on Si thus contains a large amount of defects, they may have helped towards a lower contact resistance. However, the “metal shunts” requires the dissolution and recrystallization of semiconductor in metal, namely additional heat treatment [114]. We believe the as-deposited Ohmic contacts were obtained more likely by the formation of an impurity band caused by the excessive doping. In last chapter it has been shown that the activation energy E_d of nitrogen for $1.5 \times 10^{19} \text{ cm}^{-3}$ implanted samples is approaching zero (15 meV). It is reasonable to assume that E_d becomes zero for $4 \times 10^{19} \text{ cm}^{-3}$ and $6 \times 10^{20} \text{ cm}^{-3}$ samples, making them behave as degenerate semiconductors [62]. The slowly increasing sheet resistance with temperature in Figure 4.11 below also favours this idea.

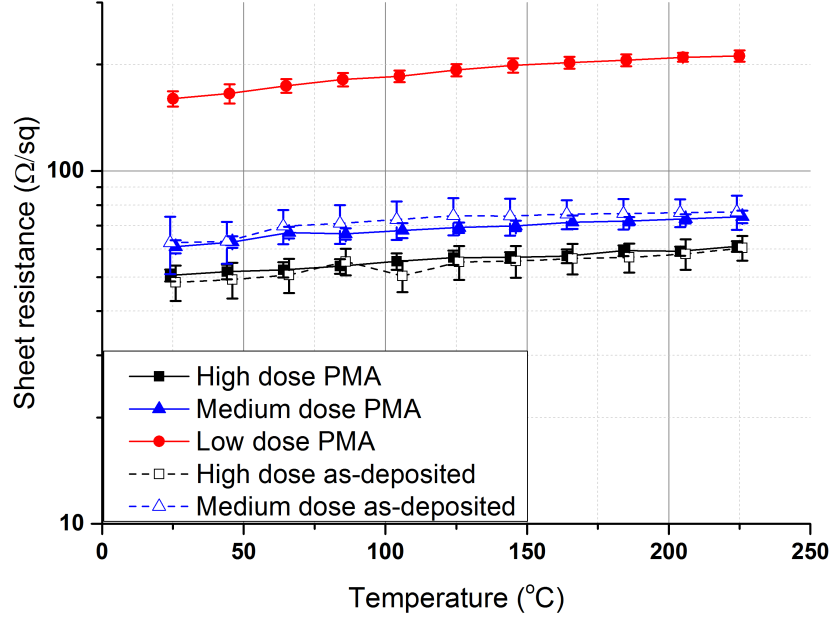


Figure 4.11: Temperature dependence of as-deposited and 1000°C annealed sheet resistance (averaged from 4 TLM structures on each sample).

Figure 4.10 shows that all Ohmic contacts have very low temperature dependence from 25°C up to 225°C. As-deposited contacts on the $6 \times 10^{20} \text{ cm}^{-3}$ and $4 \times 10^{19} \text{ cm}^{-3}$ implanted samples readily behave as temperature independent, which means the PMA (similarly “metal shunts”) did not play a big role in this. Also, the $1.5 \times 10^{19} \text{ cm}^{-3}$ doped sample has as-deposited rectifying behaviour, therefore not degenerated by the implantation process, whereas after PMA the ρ_c is also thermally stable, namely ruling out the degeneracy being the main cause. With the 3C-SiC electron effective mass of conductivity $0.32m_0$ [99], dielectric constant 9.72 [115] known, the characteristic energy E_{00}/kT for the non-degenerated $1.5 \times 10^{19} \text{ cm}^{-3}$ doped 3C-SiC/metal interface is calculated [100] to be ≈ 1.3 , which means the contact interface should be dominated by TFE, and ρ_c should decrease

considerably with increasing temperature. This is, however, conflicting with the Figure 4.10 curves, which, if anything, appear more field-emission dominated. According to the conventional Schottky barrier theory [6], the Schottky barrier height reduction $\Delta\Phi_B$ due to image charges can be calculated by Equation 4.2 using the Ti work function of 4.33 eV, the 3C-SiC affinity of 3.8 eV [95], and a 3C-SiC doping level N_d of $6 \times 10^{20} \text{ cm}^{-3}$ (100% activation and ionization assumed), Φ_B and $\Delta\Phi_B$ can be calculated as 0.53 eV and 0.4 eV respectively, which shows that even for the highest doping level used in this study, image force alone is not enough to eliminate the barrier, not to mention that it is known from last chapter that N_d is overestimated with the actual maximum value being around $7 \times 10^{19} \text{ cm}^{-3}$.

It was recently reported [116] that the metal-semiconductor interface band bending can be caused by dopant-induced dipole field between the interface and the dopant site, and is more severe in defective regions or when dopants lie closer to the semiconductor surface, which may explain what is observed in this study. We then believe the thermally stable ρ_c is due to the Schottky barrier elimination caused by the interface band bending.

4.4.3 Surface morphology and microstructure at the metal/3C-SiC interface

To further confirm the above assumption, a detailed structural view of the implanted 3C-SiC film can be helpful. TEM was used to observe the as-deposited metal/3C-SiC in-

terface. The samples were prepared with FIB-SEM utilising a standard lift-out technique, followed by low energy polishing.

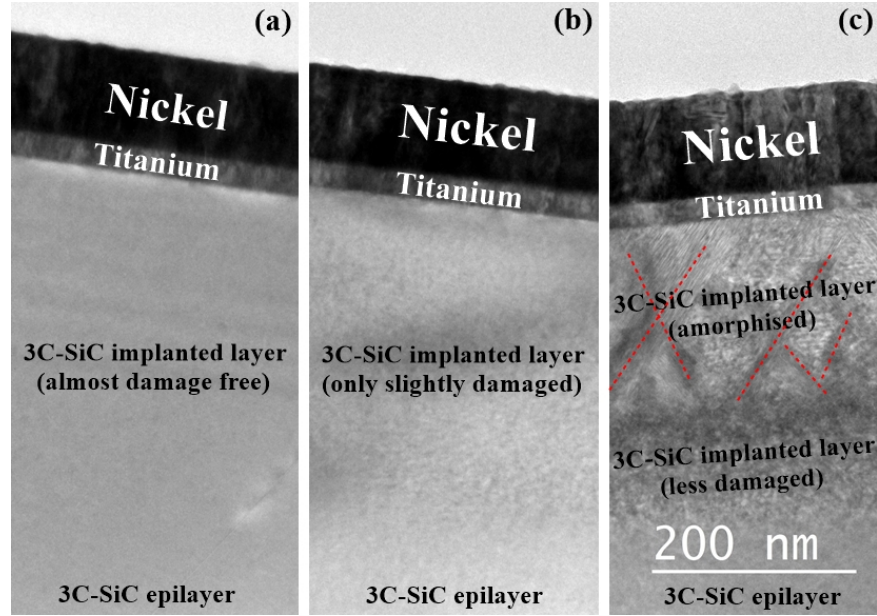


Figure 4.12: TEM images for the as-deposited Ni/Ti/3C-SiC interface: (a) $1.5 \times 10^{19} \text{ cm}^{-3}$, (b) $4 \times 10^{19} \text{ cm}^{-3}$ and (c) $6 \times 10^{20} \text{ cm}^{-3}$.

As can be seen in Figure 4.12c, for the highest doped sample, even after the 1h 1375°C PIA, there is still a great amount of line defects (highlighted with red dotted lines) remaining in the top layer. Since these defects do not extend into the as-grown epilayer, they can be ruled out as stacking faults and are most likely lattice damages induced by the ion implantation. In [83], a similar amorphous layer was observed in nitrogen implanted 3C-SiC, and with a 1h 1350°C annealing process, the amorphous layer depth and defect density was found to decrease in more lowly doped samples, also observed here as seen in Figure 4.12a and 4.12b. According to the dopant position-dependent band bending theory,

the Schottky barrier elimination at the metal/3C-SiC interface then can be attributed to the dipole field created by the excessive lattice defects located near the interface. For the lowest doped sample, the defect density in the top surface layer was probably not high enough to flatten the barrier, and an additional heat treatment was necessary to bring the interface to a more suitable position, although some other mechanisms may also have occurred during the RTA.

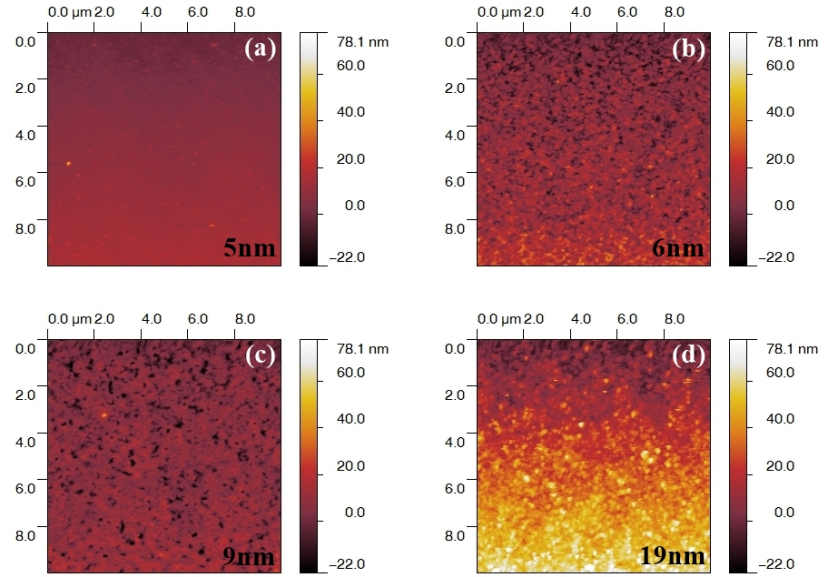


Figure 4.13: AFM images for the metal/3C-SiC ($6 \times 10^{20} \text{ cm}^{-3}$) contact surface: (a) as-deposited, (b) 900°C annealed, (c) 1000°C annealed and (d) 1100°C annealed.

Although the post metallisation heat treatment is found not to change the carrier transport mechanism, it successfully reduces ρ_c values, thus is still vital in achieving low resistivity Ohmic contacts. As such, it is also studied here for the highest doped sample who gives lowest ρ_c values. AFM results shown in Figure 4.13 indicate a surface

degradation with the increasing annealing temperature, most likely caused by stronger silicide reactions.

ρ_c values of the as-deposited contact and those annealed (800°C, 900°C, 1000°C and 1100°C) on the $6 \times 10^{20} \text{ cm}^{-3}$ doped sample are compared in Figure 4.14. It shows a continuous reduction of contact resistivity from $3 \times 10^{-5} \Omega \cdot \text{cm}^2$ to $9 \times 10^{-6} \Omega \cdot \text{cm}^2$ with increasing annealing temperature up to 1000°C, after which the value increases to $2.5 \times 10^{-5} \Omega \cdot \text{cm}^2$ at 1100°C.

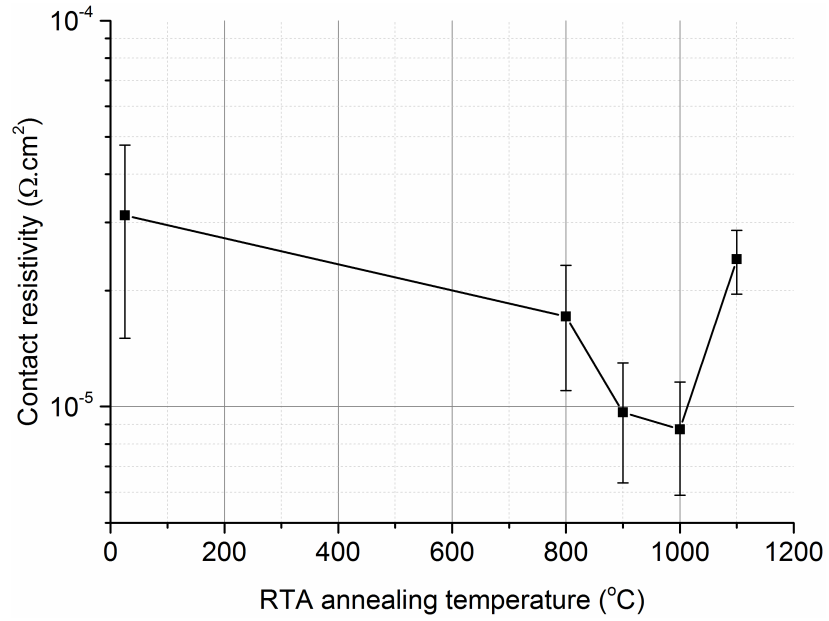


Figure 4.14: Contact resistivity dependence on the PMA temperature for the $6 \times 10^{20} \text{ cm}^{-3}$ doped sample.

In Figure 4.12 the as-deposited contact interface demonstrates three distinctive layers: Ni, Ti and 3C-SiC. After 900°C annealing (see Figure 4.15a), however, the Ni layer diffused through the Ti interlayer and reacted with the 3C-SiC beneath. According to the EDX

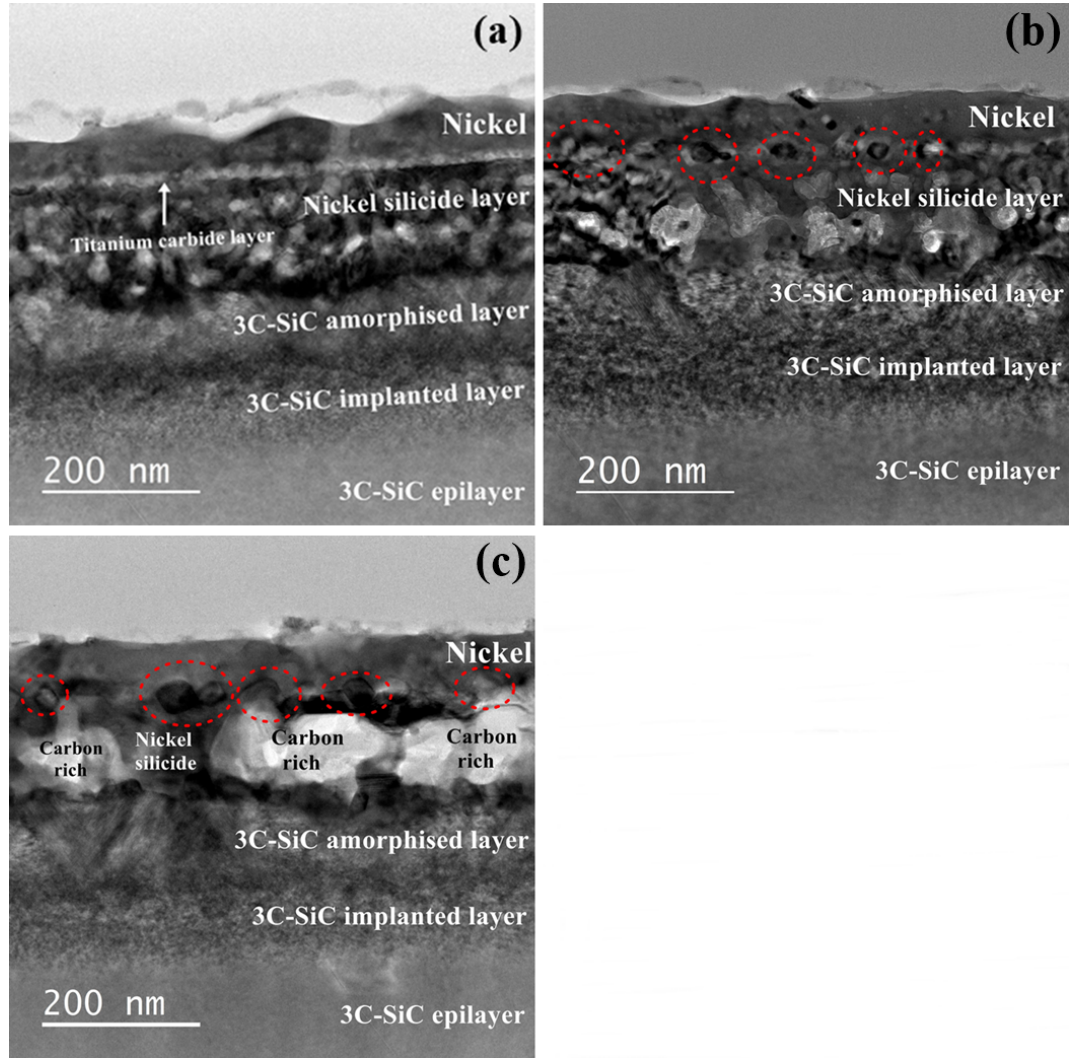


Figure 4.15: Metal/3C-SiC ($6 \times 10^{20} \text{ cm}^{-3}$) interface structure evolution with the heat treatment (a) 900°C, (b) 1000°C and (c) 1100°C annealed for 1 min.

analysis, the region formed by dark lumps is nickel- and silicon-rich, namely most likely a nickel silicide layer. Along with the dark lumps there are some small bright dots, which were found to be carbon-rich. These carbon clusters were commonly found before inside 4H- and 6H-SiC silicide [117,118] and were considered to increase the interfacial net carriers, helping to reduce the contact resistivity. With the annealing temperature further increased to 1000°C (Figure 4.15b), the Ti interlayer became less noticeable and a series of void (highlighted by red dotted circles) emerged along it. These vacancies are caused by silicon diffusion into the nickel (Kirkendall Effect) and will not have an impact on the contact resistivity, although they are harmful in terms of contacts reliability [119]. The small carbon clusters spotted previously are shown to expand in Figure 4.15b, which can be explained by the further reaction of Si with Ni. This further increases the interfacial carrier concentration, leading to a resistivity drop from 900°C to 1000°C. At 1100°C, even more severe carbon clustering is observed (Figure 4.15c) with large carbon crystallites formed. It is hypothesised that the extra active donors generated could be high enough that Coulomb scattering effects start to dominate and increase the contact resistance.

4.4.4 Silicide phase at the metal/3C-SiC interface

The TEM and EDX results in last section reveal the existence of a ≈ 150 nm silicide layer below the interface, indicating a strong reaction between metal and 3C-SiC during the PMA. In this section, XRD is applied to further explore the details of the silicide.

High-resolution XRD was performed using a Panalytical X'Pert ProMRD equipped with a 4-bounce hybrid monochromator giving pure Cu K α radiation and a solid-state Pixel detector, the wavelength was 1.540598 Å. The 3C-SiC(200) peak was aligned to maximise the intensity and minimize the full-width at half-maxima (FWHM). $2\theta - \Omega$ “powder” scans were measured between 35 and 55 2θ degrees and the resultant spectrums for as-deposited contact and those annealed from 500°C to 1100°C are shown in Figure 4.16.

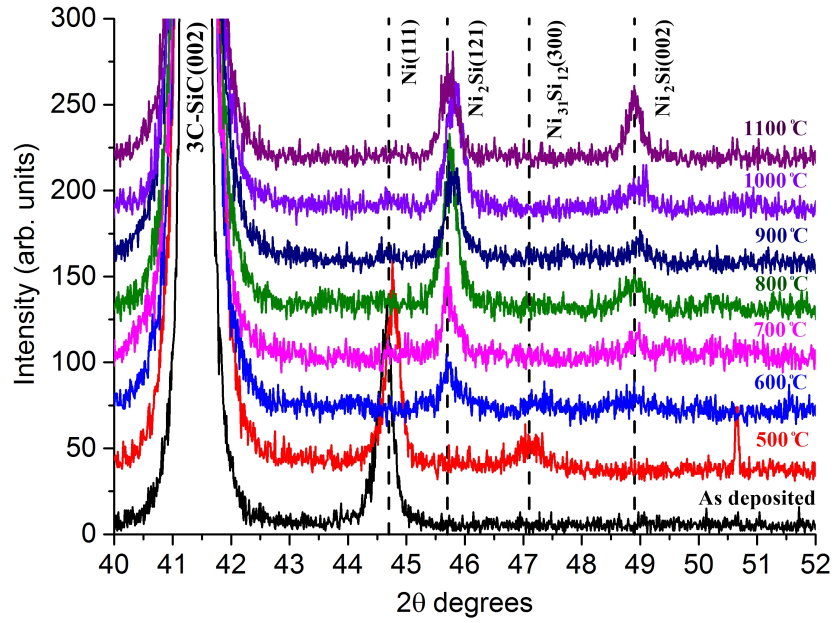


Figure 4.16: XRD measurements of metal/3C-SiC ($6 \times 10^{20} \text{ cm}^{-3}$) interface after various temperatures PMA.

As can be seen, between 500°C and 600°C, a coexistence of $\text{Ni}_2\text{Si}(121)$ and $\text{Ni}_{31}\text{Si}_{12}(300)$ are observed. While the $\text{Ni}_{31}\text{Si}_{12}(300)$ peak gradually vanishes at higher temperature, $\text{Ni}_2\text{Si}(002)$ appears and continues to enhance all the way to 1100°C. With $\text{Ni}_2\text{Si}(121)$

readily formed at 600°C and no other phases noticeable above that temperature, the $\text{Ni}_2\text{Si}(002)$ phase enhancement can be one of the reasons behind the contact resistivity drop from 800°C to 1000°C. The Ti interlayer should have reacted with 3C-SiC forming TiC or Ti_3SiC_2 [120], but no products are observable probably because the 30nm Ti layer is too thin.

4.5 Summary

In this chapter, the formation of Ni/Ti Ohmic contacts on nitrogen heavily implanted 3C-SiC layer are investigated using both electrical and physical characterisation. Temperature dependent I-V measurements reveal the unique inherent thermally stable feature of 3C-SiC Ohmic contacts, which is explained by the elimination of Schottky barrier at the metal/3C-SiC interface. The accumulation type Ohmic contact is possible with 3C-SiC due to its relatively high electron affinity of 3.8 eV and will be difficult to reproduce on 4H-SiC who has a much lower value of 2.9 eV. Relating TEM results to the literature, dopant and defect-induced dipole field was considered to have caused severe band bending at the metal/3C-SiC interface, and should be the main cause of the temperature independent ρ_c values. As-deposited Ohmic contacts are particular attractive from a fabrication point of view, since it not only reduces the thermal budget but also eliminates the potential harms which the contact annealing process can induce to other sensitive device features, such as Schottky and MOS interface. The lowest as-deposited ρ_c value is already quite

low, around $2 \times 10^{-5} \Omega \cdot \text{cm}^2$ obtained for the highest doped sample. However, there had been suggestions that the SiC contact resistivity has to be less than $1 \times 10^{-5} \Omega \cdot \text{cm}^2$, otherwise the advantage of the reduction in specific on-resistance over Si power devices will be nullified [17]. As a consequence, an extra contact annealing had to be applied to further reduce ρ_c , and the lowest value is $\sim 1 \times 10^{-6} \Omega \cdot \text{cm}^2$ obtained for the $6 \times 10^{20} \text{ cm}^{-3}$ doped sample annealed at 1000°C for 1minute. The effect of thermal treatment after contact metallisation was also examined. XRD results indicated an enhancement of the $\text{Ni}_2\text{Si}(002)$ phase for annealing temperatures above 600°C , which may have helped to reduce Φ_B . However, it is considered that the reduction of contact resistivity up to 1000°C should be mainly caused by the increment of interface carbon clusters with increasing annealing temperatures, as revealed by TEM analysis.

In 1914, Thomson may have been the first to postulate the existence of field-effect [121], which describes the phenomenon that, with an external electric field being applied on a semiconductor surface, the concentration or even polarity of free carriers in that region can be altered. In such a way that the current conduction can be modulated and devices working on this principle are called field-effect transistors (FET). The very early FETs were proposed by Lilienfeld [122] and Heil [123] in 1930s, which included a MOS feature in the device structure. “MOS” is short for metal-oxide-semiconductor, one of the most widely seen features in integrated circuits today. Back then, these devices were suffering from unstable electrical performance due to the poor semiconductor/insulator interface (more frequently called MOS interface), thus did not draw much attention from the industry. The insulator in a MOS system was introduced to protect the semiconductor surface from potential damage caused by the electric field, while on the other hand, the

amount of charge built up at the MOS interface due to the poor processing environment led to the shielding of the field-effect, and cause the device to malfunction [96]. Around the same period, Bipolar Junction Transistors (BJT) were invented, and proved to be much more reliable since they do not have a MOS interface. As a result, BJT technology dominated the transistor market for quite a long time, until 1970s, when the computer industry started to develop. Computer microprocessors and memories favour the idea of fabricating multiple transistors on a single chip rather than discrete transistors, since more devices and therefore more operations per unit area can be achieved in this way [124]. The features of MOSFET technology such as low fabrication cost, large yield, and particularly, improving performance with smaller dimensions seemed very attractive. Also, the MOS interface quality had been greatly improved by Kahng and Atalla, by using Si as the substrate and thermally growing oxide on top of it [125]. In spite of that, MOSFETs have been mainly used for low power applications, due to the rapidly increasing of devices resistance with voltage and operating temperature. The adoption of WBG semiconductors enables MOSFETs to be used in power electronics applications with much higher power levels. While the Si/SiO₂ interface has been intensively studied and the technology is very mature, the SiC/SiO₂ interface is still an active topic, revealing many challenges.

We will now describe the operation principles of MOS devices and discuss trap models developed for the MOS interface. Previous efforts for improving the SiC/SiO₂ MOS interface are also discussed. Finally, commonly used MOS characterising tools are introduced, and applied to the 3C-SiC/SiO₂ interface.

5.1 MOS Technologies: Theories and Applications

5.1.1 Ideal MOS interface

To demonstrate how the field-effect works in a MOS structure, the energy band diagram is a useful tool, which is shown in Figure 5.1 for an ideal MOS interface with main energy levels specified. An n-type semiconductor is discussed here, but the principle applies to p-type materials as well.

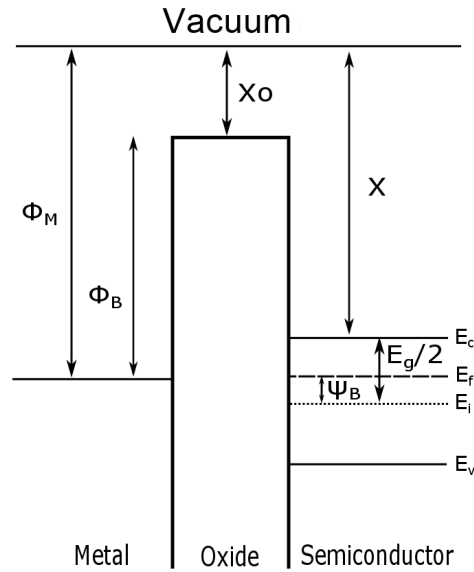


Figure 5.1: Energy band diagram for an ideal MOS interface (n-type semiconductor) in flat band.

The ideal MOS interface is based on one important assumption: the metal Fermi level aligns with that of the semiconductor E_f , and this is described by Equation 5.1 below:

$$\Phi_M = \chi + \frac{E_g}{2} - \Psi_B = \chi + \frac{E_g}{2} - \frac{kT}{q} \ln \left(\frac{N_d}{n_i} \right) \quad (5.1)$$

Where χ is the semiconductor affinity, E_g is the band gap, N_d is the free donor concentration and n_i is the intrinsic carrier density. It should be noted that in Equation 5.1, the intrinsic level is approximated to be at half band gap, which is reasonable for SiC, whose electron and hole effective masses are similar. While for some other materials, such as GaAs whose electron effective mass is 10 times smaller than the hole, this approximation does not stand true and the intrinsic Fermi level sits much closer to the conduction band. Figure 5.1 illustrates the interface situation when metal and semiconductor reach equilibrium, namely no free carrier exchanges in-between. Without band bending, this is called the flat band condition, and the external voltage bias required to achieve this condition is called flat band voltage V_{fb} . For an ideal MOS interface, $V_{fb} = 0$ (Figure 5.1), while in real situations there is usually a difference between Φ_M and E_f , and an extra gate bias ($V_{fb} \neq 0$) is necessary to achieve the flat band.

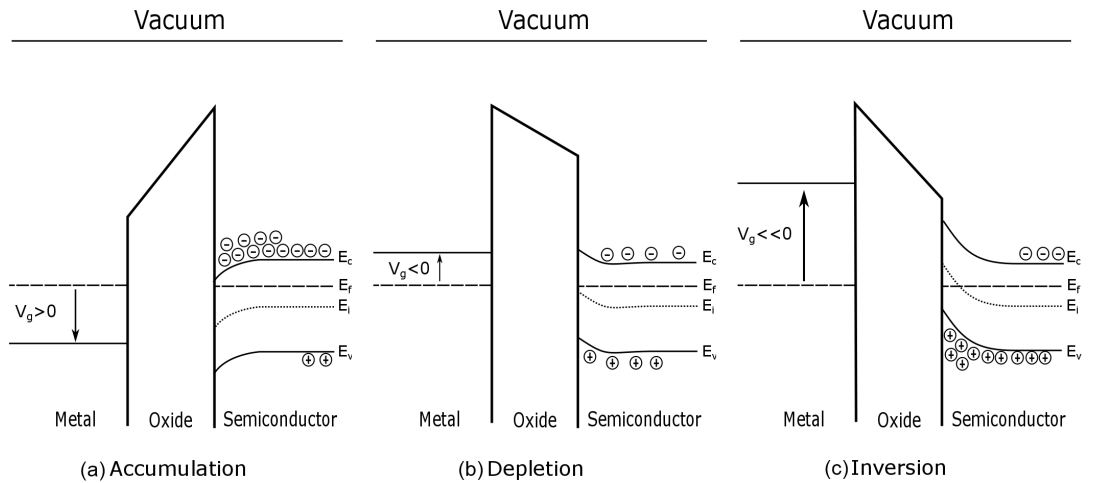


Figure 5.2: Energy band diagrams for an ideal MOS interface (n-type semiconductor) in (a) accumulation, (b) depletion and (c) inversion.

For n-type semiconductors, electrons are the majority carriers in the semiconductor bulk and are represented by circles with negative signs in Figure 5.2. In the case of a positive gate bias being applied to the gate electrode, electrons are attracted to the MOS interface, and an excess of electrons will accumulate at the oxide/semiconductor interface, the Fermi level E_f now moves closer to the conduction band edge E_c , causing the semiconductor band bending downwards as seen in Figure 5.2a. In this case, the semiconductor does not deplete due to the high electron concentration in the surface region, consequently the gate bias is supported solely by the oxide. However, if the gate bias is negative, then the metal becomes negatively charged and consequently electrons will be repelled away from the MOS interface and holes (circles with positive signs in Figure 5.2) are attracted to the surface instead. With fewer electrons at the surface, Fermi level departs away from the conduction band and the semiconductor bands bend upwards as seen in Figure 5.2b. With much fewer majority carriers (electrons) available in the surface region, the semiconductor depletes significantly under the bias and therefore partially supports the gate voltage. With a larger gate bias going more negative, there will be a point when the number of holes becomes more than the equilibrium density of electrons, namely the n-type semiconductor surface will be inverted to become p-type. In inversion, the semiconductor energy bands bend even more upwards, and E_f goes below the intrinsic level E_i as seen in Figure 5.2c. The gate voltage required for the semiconductor surface entering strong inversion is called threshold voltage V_{th} .

5.1.2 Working principles of MOSFETs

To explain how the field-effect is used to modulate current conduction in a MOSFET, the n-channel lateral MOSFET in Figure 5.3 is used as an example.

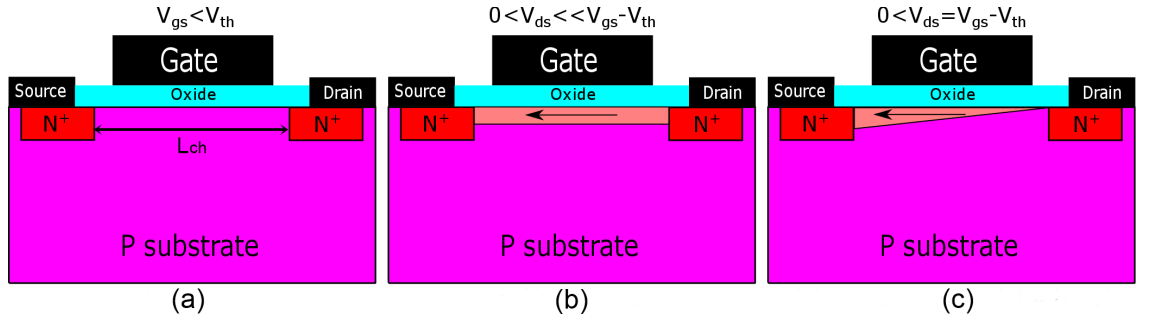


Figure 5.3: Lateral n-channel MOSFET operating in (a) off state, (b) on state-linear region and (c) on state-saturation region.

With the p-type region lying in between two n-type regions (source and drain), the device will not be able to conduct current even if an external bias is applied between drain and source ($V_{ds} > 0$), as one of the PN junctions will be reverse biased and therefore in a blocking state. Since the source is usually grounded, V_g and V_{gs} are interchangeable. As long as V_{gs} stays below V_{th} , lateral MOSFET stays in the off-state as shown in Figure 5.3a with only thermally generated leakage current at the reverse biased drain/substrate junction. When V_{gs} goes above V_{th} , namely at the onset of strong inversion, current conduction becomes possible due to the substrate surface region being inverted (n-type), thus creating a channel between source and drain as seen in Figure 5.3b. In the case of low conduction current I_{ds} , there is only a small voltage drop V_{ds} along the channel, which makes the channel almost uniformly charged, namely constant thickness. In this

condition, drain current increases with both V_{ds} and V_{gs} , and almost linearly with V_{ds} for a fixed V_{gs} , as shown by the linear region in Figure 5.4. However, if V_{ds} is increased further, then it is no longer negligible compared with the gate bias V_{gs} . Which means the effective gate bias is weakened along the channel, mostly in the drain end, leading to a tapered wedge shape. When V_{ds} becomes so high ($V_{ds} = V_{gs} - V_{th}$) that the effective V_{gs} becomes zero in the drain end, the conduction channel is pinched off, and becomes a triangular shape as shown in Figure 5.3c. In this condition, I_{ds} saturates at a value which is solely dependent on V_{gs} as seen in the Figure 5.4 saturation region.

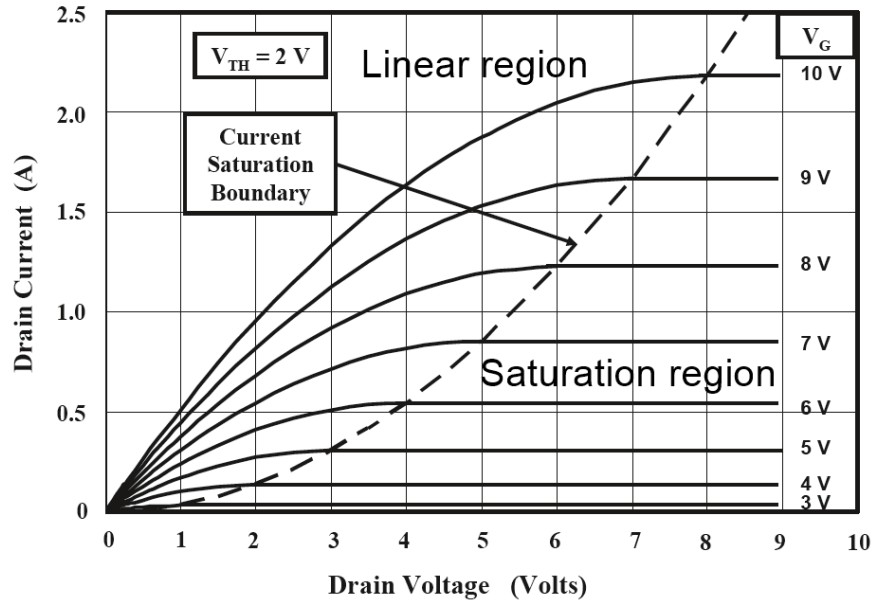


Figure 5.4: Typical MOSFET forward conducting curves with linear and saturation regions defined [126].

The importance of channel resistance R_{ch} for a MOSFET, particular in low and medium voltage applications, has been emphasized in Chapter 1. The analytical model

Equation 5.2 is given below for calculating R_{ch} [126]:

$$R_{ch} = \frac{L_{ch}}{Z_{ch}\mu_{ch}C_{ox}(V_{gs} - V_{th})} \quad (5.2)$$

Where L_{ch} is the channel length shown in Figure 5.3a, Z_{ch} is the channel width in the third dimension, C_{ox} is the oxide capacitance per unit area, and μ_{ch} is the channel carrier mobility. Usually the dimensions L_{ch} , Z_{ch} are defined by length of the device and C_{ox} , V_{th} , V_{gs} are dictated by physical and operational considerations, which leaves μ_{ch} the key factor determining the final channel resistance.

5.1.3 Degradation of channel mobility

Figure 5.5 provides a general view of how channel mobility is affected by various scattering mechanisms. Apart from phonon and Coulombic scattering mechanisms who are also present in the bulk region, there is an extra surface roughness scattering in the channel region. When the effective gate field is low, there are fewer carriers in the channel, thus the channel mobility is mainly dominated by the Coulomb scattering caused by interface traps and ionized dopants. In this condition, less scattering centres and higher carrier concentration (higher gate bias) can improve the channel mobility. As the gate field increases to a medium value when there are many carriers in the channel that the scattering centres effect is screened, phonon scattering becomes the dominant mechanism. In this case, the channel mobility decreases with elevated temperature and higher carrier

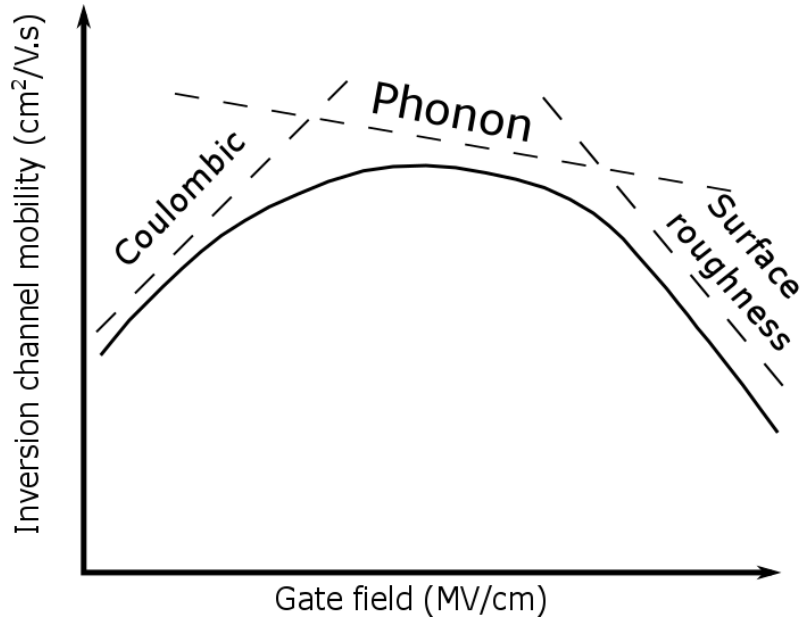


Figure 5.5: General view of the MOSFET channel mobility as a function of the gate electric field under the influence of Coulombic, phonon and surface roughness scattering.

concentrations. Finally, if the gate effective fields gets too high and attracts too many carriers in the channel, this will cause a significant reduction of the channel width. Since the channel carriers get really close to the MOS interface, the surface roughness scattering becomes important and now the channel mobility drops rapidly with gate field.

Phonon scattering is attributed to lattice vibrations and little can be done about it. The other two mechanisms, however, are much more process dependent and can be optimised by experimental work. Even though surface roughness scattering only becomes dominant in high electric field as seen in Figure 5.5, the carrier mobility can still be considerably reduced near a rough surface even in a low gate bias. Coulombic scattering discussed here mainly refers to the extra charges near the MOS interface caused by oxide

charges and interface states. The common impurity scattering still occur regardless of the interface charges in the way that a more heavily doped channel region will lead to a lower channel mobility. In short, a significant degradation of channel region carrier mobility can be avoided by maintaining a smooth oxide/semiconductor interface and minimising the extra interface charges.

5.1.4 Charge effects at the MOS interface

In Section 5.1.1, MOS interface was considered as ideal, while in real life oxides often have defects acting as carrier leakage paths and cause early breakdown. By trapping and discharging carriers during the MOS device operation, these defects are the main reason behind the severe Coulombic scattering at the MOS interface. Extra charges found in most MOS systems are categorised into four groups, namely mobile charges, fixed charges, oxide trapped charges and interface charges. A schematic diagram indicating the general location and polarity of various charges are shown in Figure 5.6.

Mobile charges arise from metal ionic impurities (such as Na^+) introduced during the device fabrication process and can move freely in the oxide with a gate bias. Since they are positively charged, they will attract semiconductor electrons to the surface and induce extra band bending, leading to a shift of V_{fb} from the ideal value. However, this shift is non-reproducible since the movement of mobile charges are quite random. Mobile charges are highly uncontrollable thus must be minimised through a clean and careful fabrication

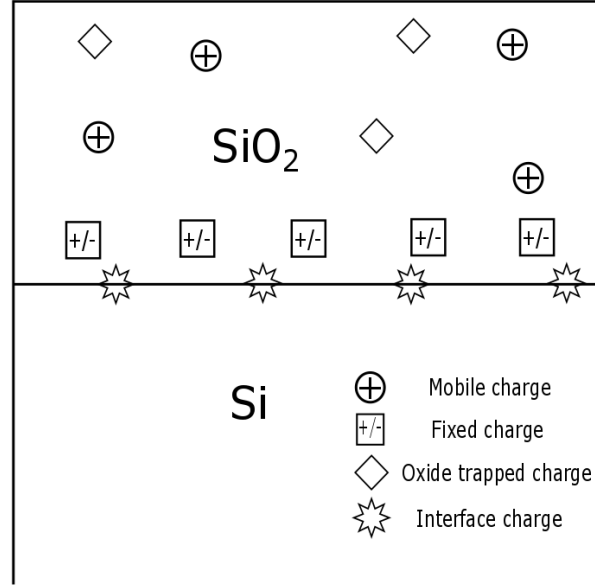


Figure 5.6: Common oxide charges at MOS interface with locations and charge polarity indicated.

process.

In contrast to mobile charges, fixed charges refer to those who do not move with gate biases. The origin of fixed charges is believed to be the excessive ions left near the interface after the oxidation process termination [127]. They are usually located in the oxide and close to the MOS interface as shown in Figure 5.6. Fixed charges can be either positive or negative, and the total amount depends heavily on the oxidation condition. Since fixed charges stay close to the interface, they also affect the semiconductor band bending. As a result, a shift of V_{fb} from the theoretical value is again observed, only this time it is fixed.

Interface charges, which as the name suggests, sit at the MOS interface. The energy

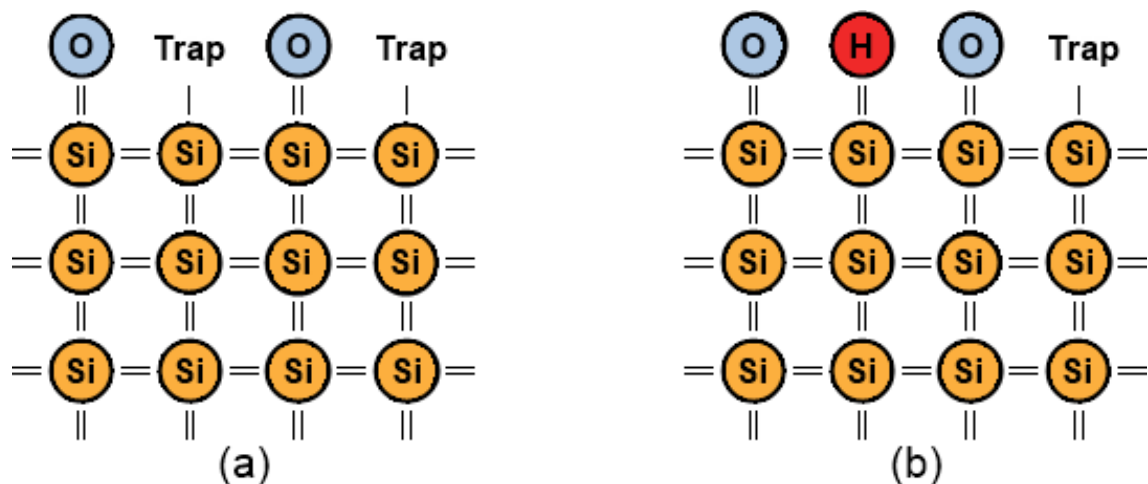


Figure 5.7: Si dangling bonds (a) without passivation and with (b) hydrogen passivation at the SiO₂/Si interface [128].

levels of these traps are in the semiconductor band gap, consequently they can act as carrier traps charging/discharging with the bulk semiconductor carriers during device operation. And since these traps are right at the MOS interface, they can considerably scatter the channel carriers much more than other charges. The origins of interface traps vary among different MOS systems. For Si/SiO₂, most of the interface traps come from unterminated Si dangling bonds as shown in Figure 5.7a. H₂ annealing after the gate oxidation is typically applied to passivate the unterminated Si dangling bonds (Figure 5.7b).

Unlike the previous three, oxide trapped charges are induced by the device operation rather than the fabrication process. Both thermally grown and deposited oxide layers contain intrinsic defects such as oxygen vacancies [129]. Although these defects are electrically neutral, during device operations, carriers may be injected into them and make

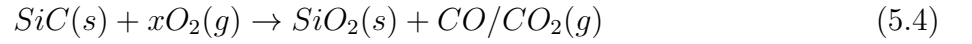
them either negatively or positively charged. For states very close to the MOS interface which are able to be charged and discharged during device operation, these oxide trapped charges effectively behave as interface traps, while those further away are similar to fixed charges.

5.1.5 SiC/SiO₂ interface traps

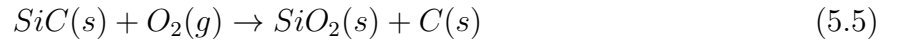
With all the superior electrical performance of SiC introduced in Chapter 1 and the ability to be thermally oxidised, it is no surprise that there are a lot of interests in making SiC MOS devices. The most commercialised form of silicon carbide, namely 4H-SiC is naturally mostly studied. The hexagonal lattice of 4H-SiC means there will be several faces available for oxidation. Most of the work has been devoted into the (0001) Si-face, the only one readily available in commercial wafers. The following discussions are therefore mainly focused on the (0001) Si-face. There have been studies suggesting that MOS interface traps for all SiC polytypes are similar [130], thus the study on the 4H-SiC/SiO₂ interface also provides a great insight into the 3C-SiC/SiO₂ interface.

Unfortunately, the 4H-SiC/SiO₂ interface turns out to be quite poor and the electrical performance is not even close to the Si case. The interface trap density (D_{it}) at an as-grown 4H-SiC/SiO₂ interface is typically close to $1 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$, which is hundreds of times higher than the Si/SiO₂ interface [131]. The channel mobility generally decreases with increasing D_{it} , thus the latter is commonly used as an indicator for the MOS interface

quality. With decades of study, the mechanisms causing the poor 4H-SiC/SiO₂ interface are still not fully understood. In [129], a discussion was made on the potential origins of interface traps and two sources were identified, first of which is the carbon accumulated at the MOS interface during the SiC oxidation process. The reactions occurring during Si and SiC oxidation processes can be generally expressed by reactions 5.3 and 5.4 as below:



Depending on the oxygen pressure, there may be some intermediate reactions [132] but it can be seen that SiC oxidation is accompanied by the release of gaseous carbon, either CO or CO₂. However, the increase of oxide thickness makes it more difficult for carbon to escape after the oxidation process goes on for a while and the reaction 5.5 may occur instead:



The theory of carbon failing to escape through thicker oxide naturally leads to the idea that there should be less carbon at the MOS interface with thinner oxide. Indeed, a recent study [133] demonstrated an almost ideal SiC/SiO₂ interface with a very thin oxide layer

(≈ 14 nm), the D_{it} value was below $1 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$. However, a certain oxide thickness (≈ 50 nm for SiC MOS devices) is necessary for a reasonable V_{th} to prevent devices from being accidentally switched on, which means very thin gate oxide is not practical. Thin thermally grown oxide with deposited oxide on top of it may be an option but still not easy, since deposited oxide is known to contain many more defects than thermally grown ones [134]. This leads to the second source of SiC/SiO₂ interface traps, namely oxide defects. Oxide defects induced traps are essentially the oxide trapped charges mentioned before. In SiC/SiO₂ study they are also known as “near-interface traps” since they do not actually sit at the interface but instead are located in the SiO₂ very close to the interface. For Si, energy levels of oxide trapped states are in the conduction band thus not electrically active. For SiC, however, whose band gaps are 2-3 times wider, many of the oxide trapped charges are located in the band gap, and are electrically active, as has been confirmed by photon stimulated electron tunnelling [135]. The near-interface traps have time constants much smaller than the carbon-cluster related traps, thus are also called fast traps while the latter known as slow traps.

A schematic representation of the carbon cluster model is illustrated in Figure 5.8 with energy levels of the traps specified. Due to the much lower mobility of holes compared with electrons, SiC MOS devices are almost exclusively based on n-channel design, naturally the traps scattering the channel carriers most are the ones located close to the conduction band edge. Figure 5.8 shows the 4H-SiC conduction band edge is mostly affected by near-interface traps and π -bonded carbon clusters, with the former being more dominant.

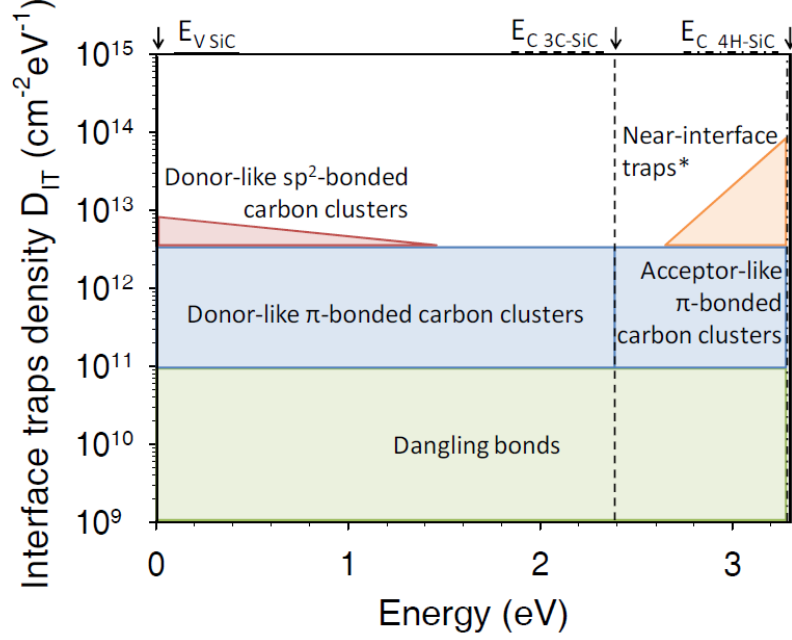


Figure 5.8: Schematic representation of the “carbon cluster model” [136].

Both of these traps are acceptor-like namely negatively charged when occupied, which can explain the quite positive V_{fb} values often observed for 4H-SiC MOS devices. On the other hand, 3C-SiC is free from near-interface traps attributed to a smaller band gap, but is still troubled by π -bonded carbon clusters. These carbon clusters near the 3C-SiC conduction band edge are donor-like, thus positively charged if occupied, which means the resultant V_{fb} may be more negative. Dangling bonds still contribute to some of the interface states here, but are only secondarily concerns. Consequently for SiC, H_2 annealing is not as effective as it is for Si. Other techniques have to be explored for SiC/SiO₂ interface optimisation.

5.1.6 SiC/SiO₂ interface treatments

The efforts put into improving the SiC/SiO₂ interface can be divided into three groups, namely Post-Oxidation Annealing (POA), channel counter-doping, and high temperature oxidation.

Up to now, nitridation may be the most widely used method to improve the 4H-SiC/SiO₂ interfaces. It is usually achieved by annealing thermally grown gate oxides in nitrogenous trace gases environment (NO or N₂O), called post-oxidation annealing. During the annealing process, it is believed that the N-O bond breaks at high temperature and supplies free oxygen which oxidises 4H-SiC [137], consequently nitridation by POA is accompanied by a further growth of the oxide, although not significantly. Sometimes gate oxide can also be directly grown in such an atmosphere to obtain similar benefits. Previous X-ray Photoelectron Spectroscopy (XPS) results demonstrated that after NO/N₂O POA, there were fixed nitrogen atoms near the interface with an area density around $1 \times 10^{14} \text{ cm}^{-2}$ [138], even after removing all the oxide by a hard HF etching. This suggests that nitrogen atoms were strongly bonded to 4H-SiC substrate. There has been evidence showing the nitridation process reduced both carbon related traps and near-interface traps [139], even though there is still no complete theory established to explain it. The near-interface traps are probably reduced by the formation of an oxynitride layer between 4H-SiC and gate oxide, which redefines the oxide/semiconductor boundary [140] so that oxide trapped charges are no longer near the interface. In terms of the carbon clusters,

they are probably decomposed by inserted nitrogen atoms, which shift the energy levels of remaining clusters deeper into bandgap, namely further away from the conduction band edge so are less effective in terms of scattering channel carriers [141]. Apart from NO/N₂O, it was reported that annealing the gate oxide in a phosphorous trace atmosphere (POCl₃ [142] or P₂O₅ [143]) also led to a channel mobility improvement, although it introduced severe threshold voltage instability as a result of SiO₂ being converted into phosphor silicate glasses. Reducing the number of interface traps by introducing extra atoms into the interface is called passivation, and regardless of the source (N or P), it is always required that enough foreign atoms diffuse through the gate oxide and reach the MOS interface. Certainly higher annealing temperature and time duration will help with that, as long as the SiO₂ crystal structure is still well preserved. However, due to the very low diffusion coefficient of nitrogen in SiC as mentioned in Chapter 3, nitrogen atoms incorporated through POA saturates only within a monolayer deeper into the interface [144], and consequently the mobility value does not increase further and the peak value typically stays around 40 cm²/V.s [145]. Phosphorous has a higher saturation density than nitrogen in 4H-SiC, but still, the peak mobility value stays around 80 cm²/V.s [146] regardless of further increased annealing time durations.

The limitation of thermal diffusion naturally leads to the idea of incorporating more passivating atoms into the interface by ion implantation, which is also known as channel counter-doping. 4H-SiC MOSFETs were fabricated on nitrogen implanted substrates and higher peak channel mobility (≈ 60 cm²/V.s) than un-implanted or even NO/N₂O

annealed samples was observed [147–149], before the mobility curve becomes significantly distorted by a dose level of $2.2 \times 10^{14} \text{ cm}^{-2}$. The success of counter-doping technique brings in another possible explanation [149] other than the defects passivation for the improved 4H-SiC/SiO₂ interface. With the channel surface being partially compensated by the nitrogen implantation, a depletion region is formed between the thin counter-doped n-type surface and the underlying p-type channel region. The n-type counter-doped surface may be positive charged even without any gate bias due to the p-n junction depletion. In inversion mode, higher carrier mobility can be achieved since these positive charges will cancel part of the negative electric field build in the channel region, reducing the surface roughness scattering. Apart from nitrogen, other elements were also studied for the counter-doping. In [150], a variety of ions including B, N, F, Al, P and Cl were individually implanted into a 4H-SiC substrate, which was then oxidised to make MOS capacitors. It turned out only group V elements (N and P) led to a reduced D_{it} while the others increased it. A negative shift of V_{fb} is always observed for N or P counter-doped MOSFETs, a natural result of the channel being partially compensated. For devices fabricated with N or P based POAs, similar negative shifts were also observed, which suggests that counter-doping may have occurred in POAs through minor thermal diffusion, making it difficult to distinguish the effects from passivation and counter-doping. More recently [151], counter-doping 4H-SiC MOSFET channel using Sb was studied and a peak field-effect mobility as high as $80 \text{ cm}^2/\text{V.s}$ was obtained. The fact that the mobility value dropped to almost zero at 70 K (Sb freezes out) confirmed the improvement is not

achieved by defect passivation, since otherwise the mobility should only be influenced by SiC electrons and the Sb freeze-out will have minimal effect. Further processing the Sb counter-doped sample with NO POA led to an increased channel mobility in all temperatures including 70 K, which suggests that the counter-doping and defects passivation may be two independent mechanisms yet both increase the channel mobility.

Both previous methods introduce extra foreign element atoms to the SiC/SiO₂ system. It will be ideal to have an as-oxidised MOS interface free from excessive interface traps. High temperature oxidation is considered as a possible solution. It was firstly reported in [152] that D_{it} decreases with increasing oxidation temperature, which was related to a reduction of SiC_xO_y near the interface at higher oxidation temperature. More recently [153], a channel mobility of 40 cm²/V.s was reported for 4H-SiC MOSFET with gate oxide thermally grown at 1500°C without any further treatment, and the XPS measurement suggests a reduction of carbon near the interface. The mechanism behind high temperature oxidation is still unclear and needs to be explored further.

The 3C-SiC/SiO₂ interface is much less studied than 4H-SiC. Past literature reveals the benefits of including hydrogenation processes either during gate oxidation or via POA, which decreases D_{it} as well as effectively reduces positive fixed charges [154, 155]. Thus wet oxidation/POA is frequently used in 3C-SiC MOSFET fabrication [156, 157]. In terms of nitridation, extra deep interface traps revealed by the double peak conductance spectra were found from MOS capacitors fabricated using direct N₂O oxidation and oxygen oxidation on nitrogen implanted films [154, 158]. The inefficiency of the nitridation process

for 3C-SiC is strange since according to the carbon cluster model shown in Figure 5.8, the 3C-SiC/SiO₂ interface is dominated by π -bonded carbon clusters, which should be reduced by the nitridation process just as 4H-SiC. Recent results on fabricating 4H-SiC and 3C-SiC MOSFETs are summarised in Table 5.1.

Table 5.1: Recent results on 4H and 3C-SiC MOSFET fabrications.

Substrate material	Channel doping	Gate oxidation	POA treatment	Peak channel mobility	Ref.
4H-SiC Si-face	$5 \times 10^{15} \text{ cm}^{-3}$ p-type epilayer	O ₂ dry oxidation at 1150°C for 7 hours	NO anneal at 1175°C for 4 hours	$\approx 48 \text{ cm}^2/\text{V.s}$	[145]
4H-SiC Si-face	$8 \times 10^{15} \text{ cm}^{-3}$ p-type epilayer	O ₂ dry oxidation at 1200°C for 2.5 hours	POCl ₃ anneal at 1000°C for 10 mins	$\approx 90 \text{ cm}^2/\text{V.s}$	[150]
4H-SiC Si-face	$6 \times 10^{15} \text{ cm}^{-3}$ p-type epilayer	O ₂ dry oxidation at 1150°C for 11 hours	Sb implanted channel	$65\text{-}80 \text{ cm}^2/\text{V.s}$	[151]
3C-SiC on Si (CVD)	$2 \times 10^{17} \text{ cm}^{-3}$ p-type epilayer	O ₂ wet oxidation at 1150°C for 2.5 hours followed by Ar annealing at 1150°C for 30 mins	O ₂ wet re-oxidation at 950°C for 2 hours	$\approx 165 \text{ cm}^2/\text{V.s}$	[156]
Free standing 3C-SiC	$1 \times 10^{16} \text{ cm}^{-3}$ p-type epilayer	O ₂ dry oxidation at 1100°C, followed by Ar annealing at 1150°C for 30 mins	O ₂ wet re-oxidation at 800°C for 30 mins	$\approx 229 \text{ cm}^2/\text{V.s}$	[159]
Free standing 3C-SiC	$7 \times 10^{16} \text{ cm}^{-3}$ p-type epilayer	O ₂ dry oxidation at 1100°C for 90 mins	O ₂ wet re-oxidation at 950°C for 3 hours	$5\text{-}10 \text{ cm}^2/\text{V.s}$	[160]
Free standing 3C-SiC	$1 \times 10^{18} \text{ cm}^{-3}$ Al implanted	O ₂ dry oxidation at 1100°C for 90 mins	O ₂ wet re-oxidation at 950°C for 3 hours	$\approx 40 \text{ cm}^2/\text{V.s}$	[161]
Free standing 3C-SiC	Not known Al implanted	O ₂ wet oxidation at 1150°C	None	$\approx 150 \text{ cm}^2/\text{V.s}$ for [110] and $\approx 300 \text{ cm}^2/\text{V.s}$ for [-110]	[162]

5.2 MOS Interface Characterisation Tools

Interface trap density D_{it} is the mostly used indicator for evaluating a MOS interface electrical performance. Consequently it is crucial to be able to accurately measure it and this section introduces the most commonly used characterising tools.

5.2.1 Capacitance-voltage method

D_{it} is usually obtained by performing Capacitance-Voltage (C-V) measurements on MOS capacitors. A conventional vertical n-type MOS capacitor is shown in Figure 5.9, which can be represented by two capacitors (C_{ox} and C_s) connected in series.

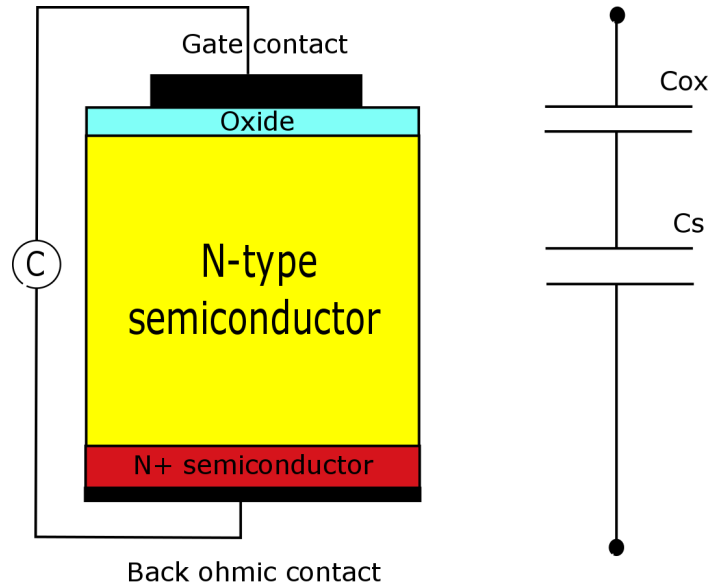


Figure 5.9: A conventional n-type MOS capacitor structure and the simplified circuit graph.

In a C-V measurement, V_{gs} is swept from negative to positive or opposite to cover

accumulation, depletion and inversion modes. The sweeping stops at each voltage step for a while to allow for the capacitor charging up, during which short period the displacement current is measured, and by integrating the current over time the stored charge Q is obtained. Since $C = Q/V$, the device capacitance is also obtained and can be plotted as a function of V_{gs} . In accumulation, the excessive electrons at the MOS interface shorts the semiconductor, thus measured capacitance only comes from the gate oxide. With the capacitor going into depletion mode, the mobile electrons move below the depletion layer. Now the measured capacitance is a series combination of oxide capacitance C_{ox} and semiconductor depletion region capacitance C_s . Inversion mode is similar to accumulation, except that now it is the mobile holes shorting the semiconductor, and the measured capacitance again equals C_{ox} . The MOS interface reaches equilibrium at every sweeping step during the gate sweep, thus it is called quasi-static measurements.

C-V characterisation can also be performed by adding a small AC (mostly sinusoidal) signal into V_{gs} and measure the impedance directly. If the applied AC signal has a very high frequency, the gate electric field oscillations may be too fast for channel carriers to follow, because the minority carrier generation is usually a slower process. As a result, the measured inversion capacitance is fixed regardless of V_{gs} . In both accumulation and depletion modes, devices are dominated by the majority carrier diffusion, thus the measured capacitance is almost the same regardless of the AC signal frequency. If the frequency is sufficiently low, minority carrier generation is able to follow the AC signal, then the resultant CV curve is similar to quasistatic.

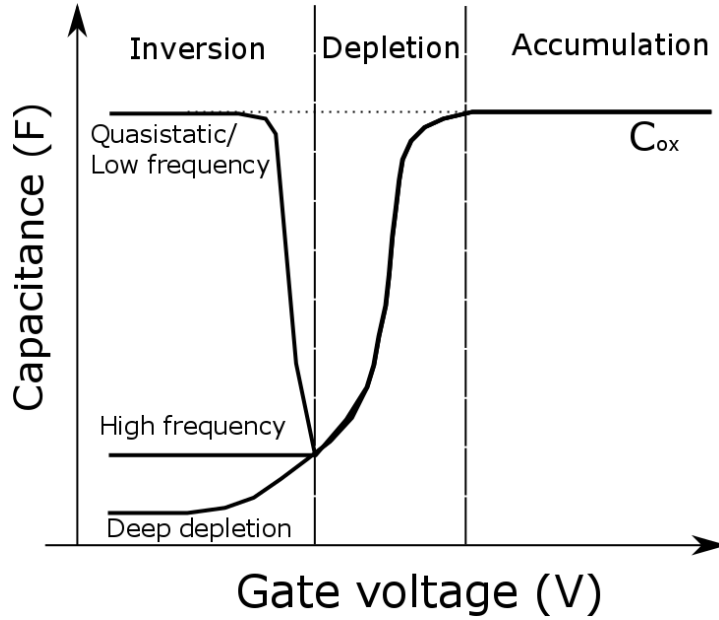


Figure 5.10: A conventional n-type MOS capacitor structure and the simplified circuit diagram.

Until now, discussions are based on conventional semiconductors such as Si. It is previously introduced in Chapter 1 that WBG semiconductors have very low intrinsic carrier density, which is proportional to the carrier generation-recombination rate. As a result, for SiC MOS capacitors, the inversion channel cannot be formed for room temperature measurements, because the minority carrier generation is so slow that it cannot even catch up with the DC V_{gs} sweeping rate. Without inversion, the measured capacitance will continue to decrease due to the further depletion of the semiconductor as seen in Figure 5.10, thus called deep-depletion.

Apart from D_{it} estimation, C-V measurement also provides useful information of the MOS system being studied. First of all, since the measured capacitance in accumulation

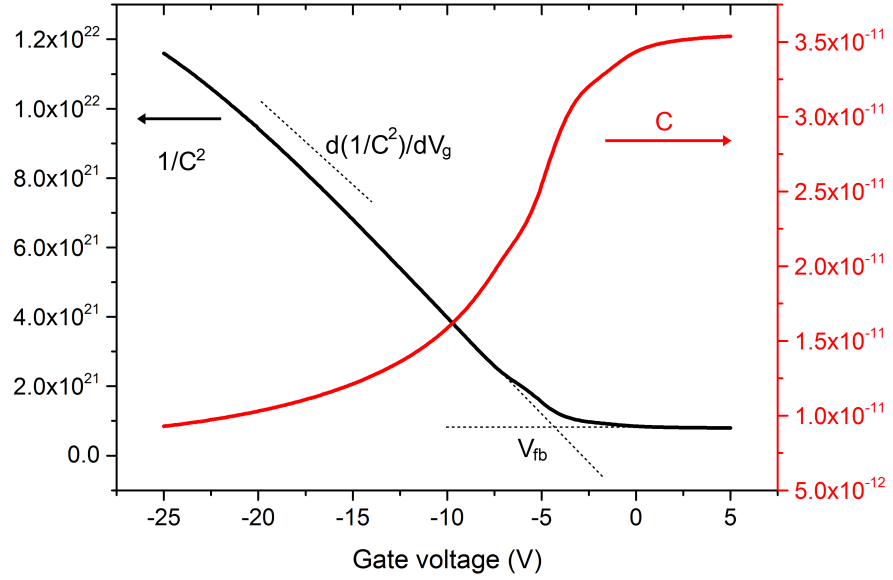


Figure 5.11: $1/C^2$ -V of an n-type semiconductor MOS capacitor.

mode is basically C_{ox} , the oxide thickness t_{ox} can be calculated following Equation 5.6 [60]:

$$t_{ox} = \frac{\varepsilon_{ox}\varepsilon_0 A}{C_{ox}} \quad (5.6)$$

Where ε_{ox} is the oxide dielectric constant, ε_0 is the vacuum permittivity, A is the gate area. By converting the C-V curve into $1/C^2$ -V, V_{fb} can be identified as the lower knee as seen in Figure 5.11. Moreover, the n-type semiconductor free donor N_d can then be extracted from the slope of $1/C^2$ -V curve using Equation 5.7 as below [60]:

$$N_d = \frac{2}{q\varepsilon_s\varepsilon_0 A^2} \frac{d(1/C^2)}{dV_g} \quad (5.7)$$

And the depletion region width W obtained [60]:

$$W = \frac{\varepsilon_0 \varepsilon_s A}{C} \quad (5.8)$$

In such a way C-V measurements can be used for semiconductor doping level estimation as introduced previously in Chapter 3.

With the extracted C_{ox} , N_d values and providing other basic parameters known, the theoretical C-V curves for the studied MOS system free from any traps can be generated. More detailed information can be found in [60], here only the most relevant one namely the deep-depletion model which applies to both high and low frequency for SiC, is demonstrated and used in following work [60]:

$$C_{s.dd} = \frac{C_{ox}}{\sqrt{1 + 2(V_g - V_{fb})/V_0}} \quad (5.9)$$

and V_0 is further defined as below:

$$V_0 = \frac{q \varepsilon_s \varepsilon_0 N_d}{C_{ox}^2} \quad (5.10)$$

The total SiC MOS capacitor is simply the series of oxide and depletion region capac-

itance as below:

$$C_{dd} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{s.dd}}} = \frac{C_{ox}C_{s.dd}}{C_{ox} + C_{s.dd}} \quad (5.11)$$

The theoretical C-V curve, however, is usually quite different from the experimental results. The extra charges introduced in section 5.1.4 distort the theoretical curve in different ways as shown in Figure 5.12 below and are introduced in the following.

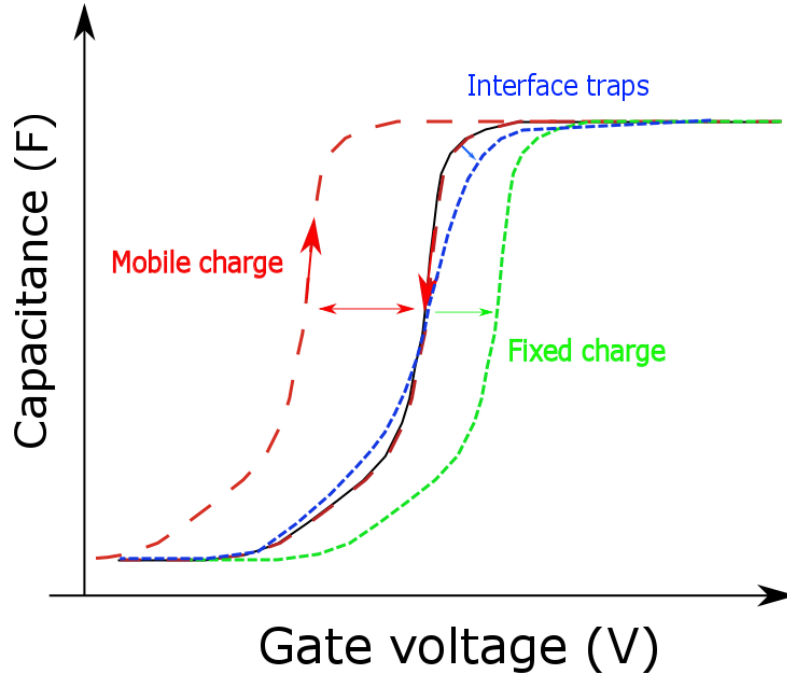


Figure 5.12: Schematic representation of how various oxide traps distort an ideal n-type SiC MOS capacitor C-V curve.

The hysteresis between C-V curves (red dashed lines) obtained from bi-directional measurements (“double sweep”) is caused by mobile charges and is not repeatable. Consequently, a quantitative analysis for the mobile charge cannot be achieved by C-V meth-

ods.

The V_{fb} shift caused by fixed charges (green dashed line), however, should stay as the same with repeating measurements. The fixed charge density D_{fix} is usually expressed in specific area (cm^{-2}) and can be calculated from ΔV_{fb} as below:

$$D_{fix} = \frac{\Delta V_{fb} C_{ox}}{q} \quad (5.12)$$

For a non-ideal n-type MOS interface, the theoretical flat band voltage $V_{fb,ther}$ can be calculated as below with all the parameters defined before:

$$V_{fb,ther} = \Phi_M - \chi - \frac{E_g}{2} + \frac{kT}{q} \ln \frac{N_d}{n_i} \quad (5.13)$$

As mentioned in Section 5.1.4, some oxide trapped charges act as fixed charges if being occupied, yet they can not be distinguished from the real fixed charges by C-V methods.

5.2.2 Terman method

For interface trapped charges, if the experimental C-V curve was obtained at sufficiently high frequency, interface states are not able to follow thus do not contribute any capacitance. However, interface trapped charges do follow the much slower DC V_{gs} sweeping. And due to their communications with the semiconductor, extra gate bias is necessary to reach the same capacitance level. As a consequence, the experimental C-V curve is

stretched out along the x-axis (blue dashed lines) as seen in Figure 5.12 and D_{it} can be estimated as below:

$$D_{it} = \frac{C_{ox}}{q^2} \frac{d\Delta V_{gs}}{d\varphi_s} \quad (5.14)$$

Where φ_s is the semiconductor surface potential and ΔV_{gs} is the difference between experimental and theoretical V_{gs} to achieve a same capacitance level. D_{it} as a function of φ_s is obtained. And by converting φ_s into the corresponding energy position within the band gap as below following Equation 5.15, a plot of D_{it} distribution within the bandgap can then be obtained.

$$E_c - E_t = \frac{E_g}{2} + \varphi_s - \frac{kt}{q} \ln \frac{N_d}{n_i} \quad (5.15)$$

Where $E_c - E_t$ represents the relative energy position of the interface traps with respect to the conduction band edge.

Since it is $d\Delta V_{gs}/d\varphi_s$ which determines D_{it} , the V_{gs} shift caused by fixed charges is not an issue thus D_{it} can still be extracted for MOS interface troubled by fixed charges. This method was developed by Terman and it requires only one high frequency C-V curve thus quite convenient. Generally, Terman method is considered to be useful for measuring D_{it} values above $1 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ [163]. However, the accuracy has long been questioned due to the fact that even above 1 MHz, C-V curves still have capacitance contributions

from interface traps, which is non-negligible compared with ΔV_g , particular for thin oxide devices [164]. Also, the theoretical high frequency C-V curve generation depends heavily on the accuracy of input parameters. As such, nowadays Terman method is no longer commonly used for SiC/SiO₂ interface characterisation.

5.2.3 High-low method

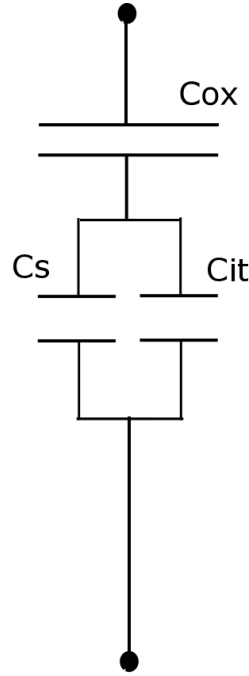


Figure 5.13: Modified measuring circuit diagram for the high-low C-V method.

Combined high-low C-V measurement has been the most popular technique in decades. At high frequency, again the interface traps are assumed not contributing to the measured capacitance. For low frequency measurement, however, the interface traps do respond to the AC probe frequency, consequently the effective measurement circuit is modified to

what is shown in Figure 5.13. Based on this model, the low frequency capacitance can be expressed by Equation 5.16. The contribution from interface traps capacitance C_{it} leads to a high-low C-V curve difference, behaving as an extra hump within the low frequency curve compared to the high frequency as shown later.

$$C_{lf} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}}} \quad (5.16)$$

Since $D_{it} = C_{it}/q^2$, rearrangement of Equation 5.16 leads to the expression of D_{it} as a function of measured capacitances:

$$D_{it} = \frac{1}{q^2} \left(\frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - C_s \right) \quad (5.17)$$

Since Equation 5.11 applies to both high and low frequency then there is :

$$C_s = \frac{C_{ox}C_{hf}}{C_{ox} - C_{hf}} \quad (5.18)$$

Where C_{hf} is the measured high frequency capacitance, and by substituting C_s in Equation 5.17, there is:

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \quad (5.19)$$

For high-low C-V method, φ_s can be calculated from C_{lf} as below and then again can

be converted to trap energy positions:

$$\varphi_s = \int_{V_{fb}}^{V_{gs}} \left(1 - \frac{C_{lf}}{C_{ox}}\right) dV_{gs} \quad (5.20)$$

High-low method eliminates the errors induced by theoretical C-V curve generation, but it only gives D_{it} values for a limited range within the band gap, starting from about 0.2 eV away from the conduction band edge. This is, however, not a big issue since as said in Section 5.1.5, these traps cause most severe scattering. The range 0.2-0.6 eV from the conduction band edge is mostly used in literatures for D_{it} estimation and will be adopted in following work.

Both methods introduced before are based on the assumption that interface traps do not contribute to the measured high frequency capacitance. However, there are reports suggesting that for 4H-SiC, some of the very fast traps can respond to the AC signal even above 1 MHz [165]. Also, the surface potential fluctuation σ can be quite large for non-uniform MOS interface, which is the case of SiC/SiO₂. This leads to a large dispersion of the trap time constant [166]. This dispersion broadens the transient range between high frequency and low frequency behaviours and causes an underestimation of D_{it} .

5.2.4 Conductance method

The conductance of a MOS capacitor is an indicator of the carriers capture-emission, namely can also be used to estimate D_{it} . By embedding the carriers capture-emission

(represented by resistance R_{it}), the measuring circuit is as shown in Figure 5.14a, which can be further simplified into Figure 5.14b using a parallel capacitance C_p and parallel conductance G_p .

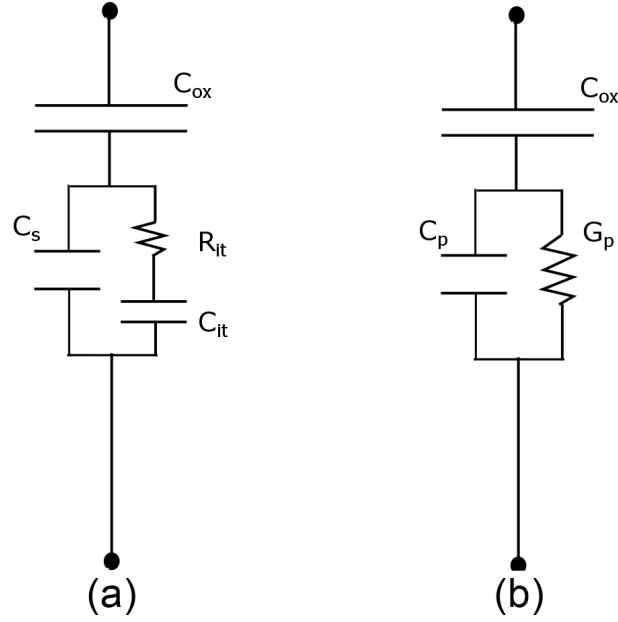


Figure 5.14: Equivalent circuits for conductance method (a) measuring and (b) simplified circuit.

Quite often the ratio G_p/ω is used as an indicator and can be calculated from the experimentally measured conductance G_m as below:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (5.21)$$

Where ω is the AC signal measuring frequency (rad/s), G_m is the measured conductance and C_m is the measured capacitance. There is also a theoretical G_p/ω model as

described by Equation 5.22 [167]:

$$\frac{G_p}{\omega} = \frac{q}{2} \frac{D_{it}}{\omega \tau_{it}} \frac{1}{\sqrt{2\pi\sigma^2}} \int_{-\infty}^{\infty} \ln [1 + (\omega \tau_{it})^2 e^{2\varphi_s}] e^{-\frac{\varphi_s^2}{2\sigma^2}} d\varphi_s \quad (5.22)$$

Where τ_{it} is the trap time constant and σ is the surface potential fluctuation.

By adjusting D_{it} , τ_{it} , and σ values in Equation 5.22, the theoretical curve of G_p/ω as function of ω can be fitted with the experimental curve obtained from Equation 5.21. Although a more complete analysis covering D_{it} , τ_{it} , and σ can be achieved, conductance method is not as much used as high-low CV due to the amount of work involved in making CV measurements in a wide range of frequencies and performing the curve fitting.

5.3 D_{it} study of 3C-SiC/SiO₂ interface

The oxidation temperature effect on the 3C-SiC/SiO₂ interface was investigated by fabricating MOS capacitors and evaluating the D_{it} values. For the first time, oxidation temperature above 1200°C was used to fabricate 3C-SiC MOS devices. Nitridation process was also applied to clarify the conflicts between previous reported results and the carbon cluster model mentioned in section 5.1.6.

5.3.1 Experimental details

The material used for the MOS capacitors fabrication was again 10 μm thick n-type 3C-SiC(001)/Si wafers provided by NOVASiC. The 3C-SiC epilayer was unintentionally doped with nitrogen background doping below $1 \times 10^{17} \text{ cm}^{-3}$. Since the interface of interest is between SiO_2 and the n-type 3C-SiC epilayer, the 3C-SiC/Si heterojunction can be rather disturbing in a conventional vertical structure. To exclude the heterojunction from the test circuit, a lateral structure shown in Figure 5.15b was adopted. An inner dot is surrounded by a much bigger ring with a gap in between. With both ends on top, the test circuit can be considered as two capacitors C_1 and C_2 connected in series and since $C_2 \gg C_1$, the measured capacitance $C_m \approx C_1$ as below:

$$\frac{1}{C_m} = \frac{1}{C_1} + \frac{1}{C_2} \approx \frac{1}{C_1} \quad (5.23)$$

Lateral MOS capacitors were fabricated on 14 mm \times 14 mm chips cut by laser. Apart from the solvent and RCA cleanings, all samples went through an extra 15 mins Piranha clean. The gate oxide was grown in a custom designed SiC oxidation furnace (shown in Figure 5.16) based in the Science City Clean Room, University of Warwick. The furnace tube is made from 6H-SiC so it can sustain very high temperature up to 1600°C. The furnace was idling at 600°C with continuous 1 slm N_2 if not operating. As soon as the oxidation process was initiated, N_2 was cut off and switched to 5 slm Ar during the 8°C/min ramping up process to flush the furnace. After reaching the oxidation temperature, 4 slm

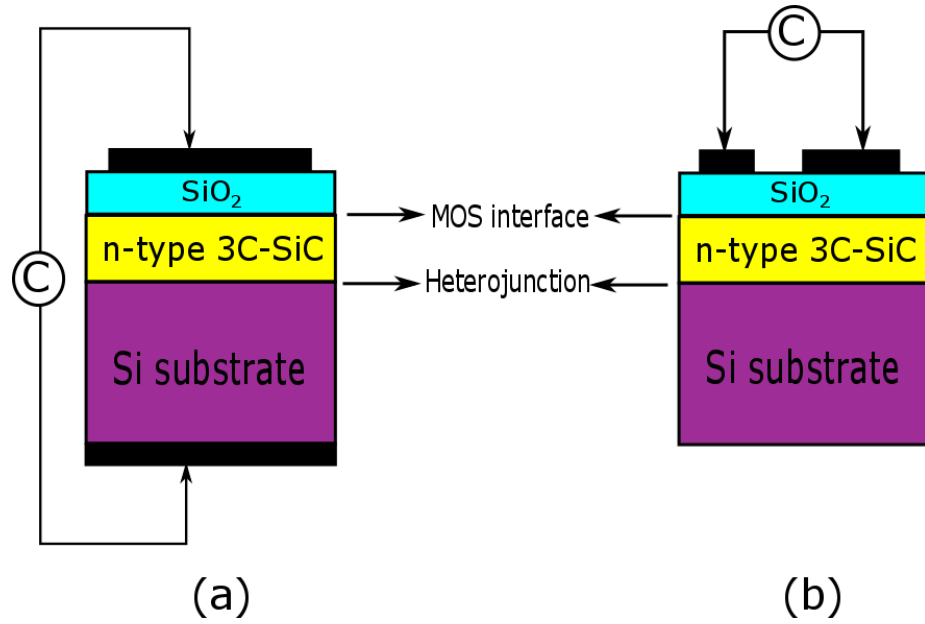


Figure 5.15: Schematic diagrams of (a) the conventional vertical MOS capacitor structure and (b) the lateral MOS capacitor structure adopted in this work.



Figure 5.16: Custom designed high temperature SiC oxidation in the Science City Clean Room, University of Warwick.

Table 5.2: Gate oxidation processes for the four 3C-SiC/Si lateral MOS capacitors fabricated.

Sample	Gate oxidation	POA
MOS 1	1200°C O ₂ dry oxidation (60 mins, O ₂ 4 slm)	NA
MOS 2	1300°C O ₂ dry oxidation (20 mins, O ₂ 4 slm)	NA
MOS 3	1400°C O ₂ dry oxidation (5 mins, O ₂ 4 slm)	NA
MOS 4	1300°C O ₂ dry oxidation (20 mins, O ₂ 4 slm)	1300°C N ₂ O annealing (2 hr, N ₂ O 1slm)

O₂ was fed into the furnace and the Ar flow was reduced to 1 slm. The total gas flow rate remained unchanged throughout the oxidation process. A 30 mins Ar (5 slm) annealing was applied to terminate the oxidation stage at the same temperature. This is commonly used in SiC technology and believed to improve the oxide reliability [168]. After Ar annealing, the furnace temperature was lowered back to 600°C at a rate of -8°C/min. 3 samples were oxidised at 1200°C, 1300°C and 1400°C respectively. A fourth sample was oxidised at 1300°C and went through an extra N₂O POA process. More detailed descriptions for oxidation conditions are summarised in Table 5.2. A general diagram describing the overall oxidation process is shown in Figure 5.17.

After the gate oxidation and POA, photolithography was used to make gate patterns on the oxide surface. 500 nm Al was deposited as the gate contact at 3×10^{-7} Torr in an E-beam evaporator. Using conventional lift-off technique, the gate electrode is obtained as inner dot of 300 μm diameter surrounded by much larger metal rings with dimensions specified in Figure 5.18. Since the outer ring has an area 105 times of the inner dot, the

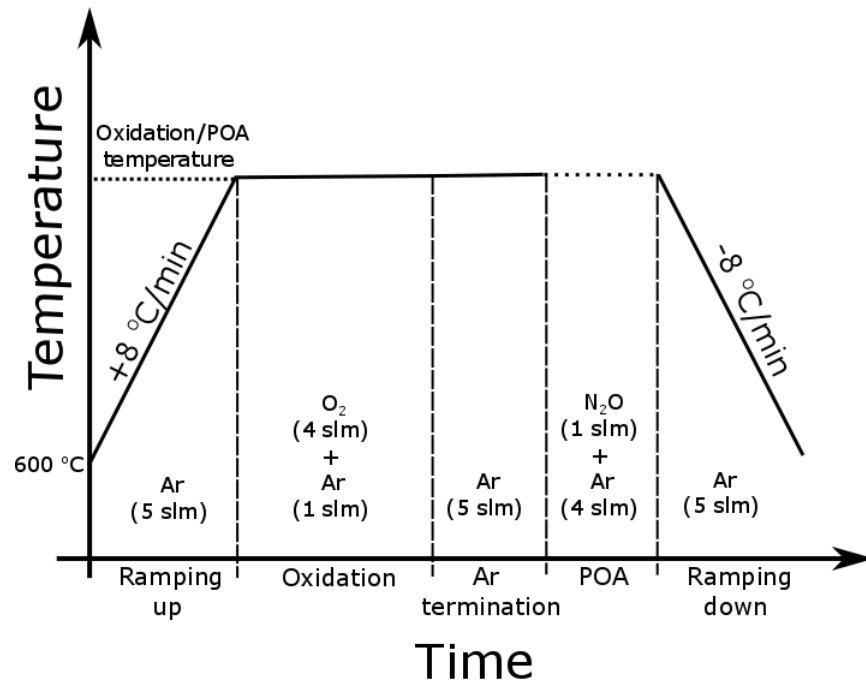


Figure 5.17: A general description of the lateral MOS capacitors gate oxidation process.

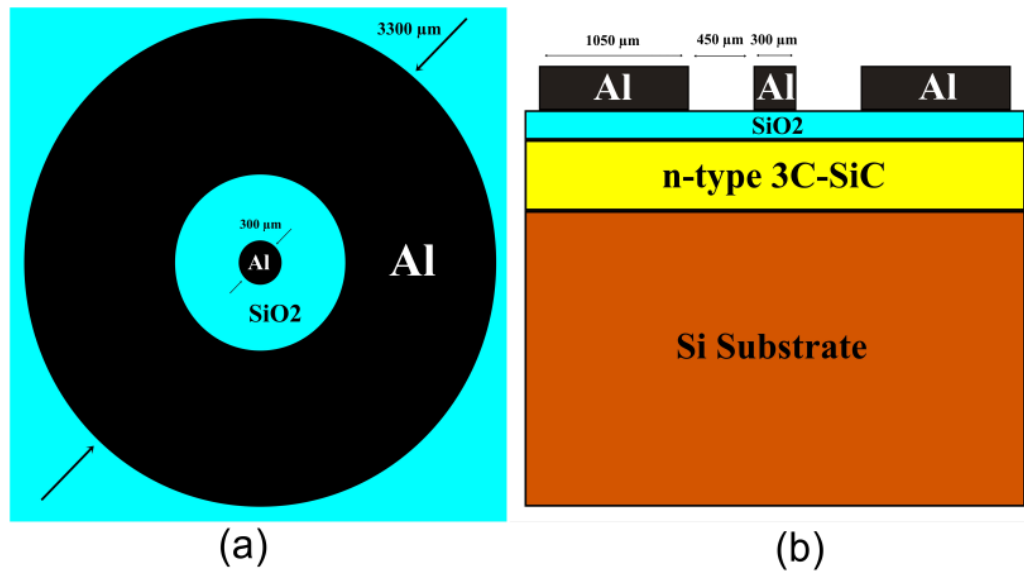


Figure 5.18: Schematic (a) top and (b) side view of the fabricated lateral MOS capacitors with dimensions specified.

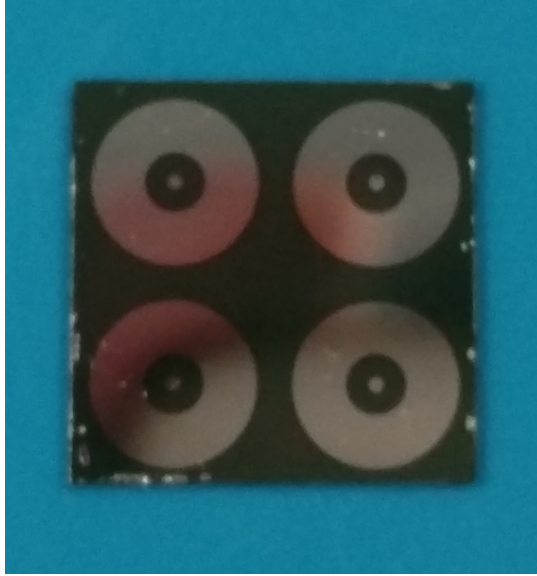


Figure 5.19: A photo demonstration of the actual fabricated 3C-SiC on Si lateral MOS capacitors.

$C_2 \gg C_1$ condition is met and the measured capacitance value is essentially the inner dot capacitance. A photo of the actual fabricated lateral MOS capacitors is shown in Figure 5.19 for reference.

With the fabrication process finished, the rest of this section will be focused on characterising the 3C-SiC/SiO₂ interface electrical and physical features using various techniques including C-V, conductance method, AFM, XRD as well as SIMS.

5.3.2 High frequency C-V characterisation

First of all, high frequency C-V measurements were performed on all 4 samples to extract the oxide thickness and the 3C-SiC epilayer doping values. The AC signal applied was 25 mV with a frequency of 1 MHz. The gate bias was swept from accumulation to deep

depletion, then back to accumulation. The typical C-V responses are shown in Figure 5.20 for 4 samples. As can be seen, all curves demonstrate only a small hysteresis, indicating a low number of mobile charges.

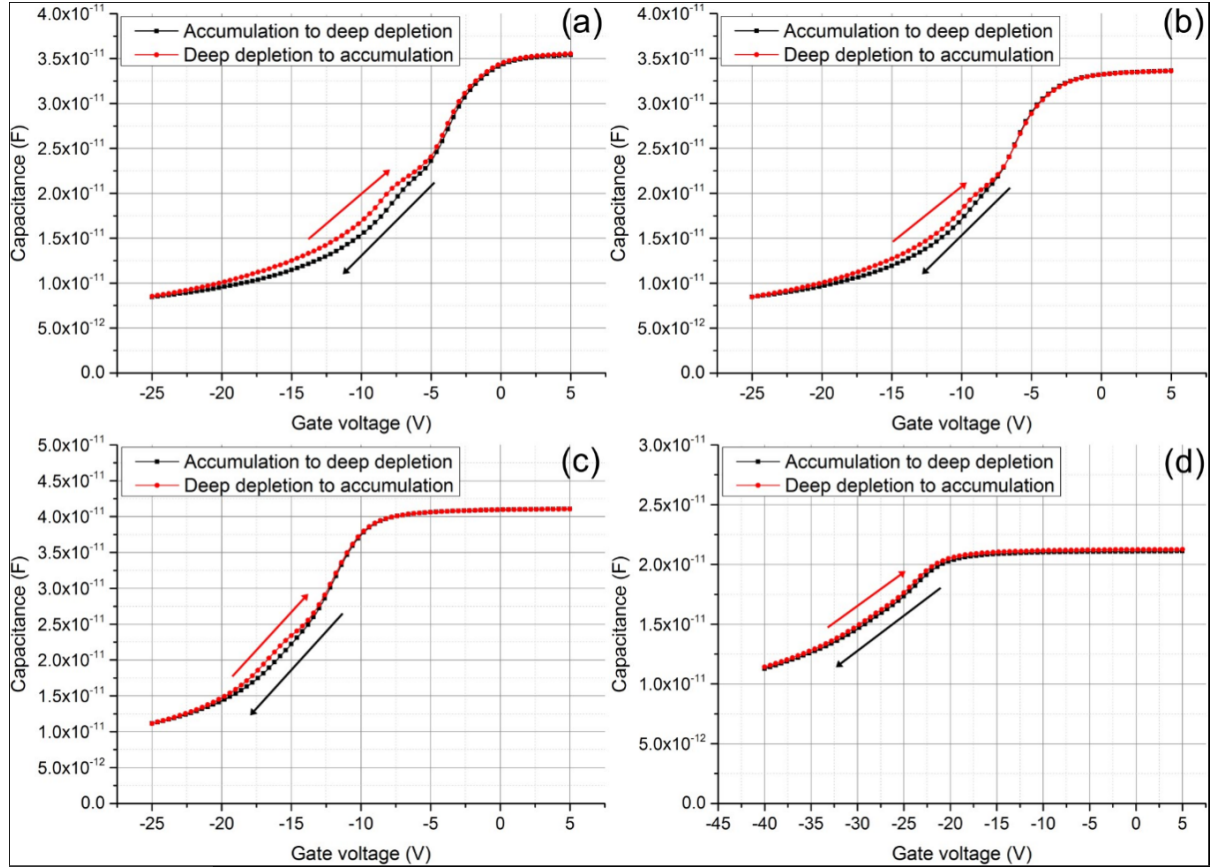


Figure 5.20: Typical 1 MHz CV responses for (a) MOS 1, (b) MOS 2, (c) MOS 3 and (d) MOS 4, the arrows indicate the sweeping directions.

The n-type 3C-SiC epilayer doping levels are calculated for all devices (9 devices on each different sample) using Equation 5.7, and the average N_d values are obtained for all four samples as shown in Table 5.3. The N_2O annealing step for MOS 4 may be responsible for the extra donors. Oxide thickness values are calculated using Equation

Table 5.3: Information extracted from high frequency CV curves for MOS 1-4.

Sample	Calculated doping (cm^{-3})	Oxide thickness (nm)	Flat band voltage (V)	Fixed charge density (cm^{-2})
MOS 1	$(5.35 \pm 0.39) \times 10^{16}$	68.92 ± 1.98	≈ -4	1.1×10^{12}
MOS 2	$(5.63 \pm 0.24) \times 10^{16}$	73.28 ± 3.17	≈ -6	1.6×10^{12}
MOS 3	$(5.52 \pm 0.46) \times 10^{16}$	60.15 ± 1.34	≈ -13	4.5×10^{12}
MOS 4	$(9.44 \pm 0.53) \times 10^{16}$	109.33 ± 3.08	≈ -22	$4. \times 10^{12}$

5.6 and are summarised in Table 5.3. With the oxide thicknesses and 3C-SiC epilayer doping known, the ideal CV curves for all 4 sample are generated and plotted against the experimental ones in Figure 5.21. Since all samples have different oxide thickness, it is more convenient to use the normalised capacitance C/C_{ox} for direct comparisons. which shows that the one for MOS 4 (red dashed line) is more stretched in the x-axis due to the higher doping level.

A negative shift of the experimental C-V curves from the ideal ones is clear for all samples, indicating the existence of positive fixed charges. As explained before, only donor-like states are present at the 3C-SiC/SiO₂ interface, and since they are positively charged when empty, these donor-like states may be responsible for the negative V_{fb} , which are extracted from $1/C^2$ -V curves and shown in Table 5.3. Comparing MOS 1, 2 and 3, it can be seen that V_{fb} is shifted to more negative values when the oxidation temperature increases. The N₂O annealed MOS 4 has the biggest shift of all. Following Equation 5.12, fixed charge densities for all samples were calculated using and are shown in Table 5.3. It can be seen that MOS 4 does not have the highest fixed charge density, thus the significant V_{fb} shift of MOS 4 most likely comes from the counter-doping effect. SIMS analysis was

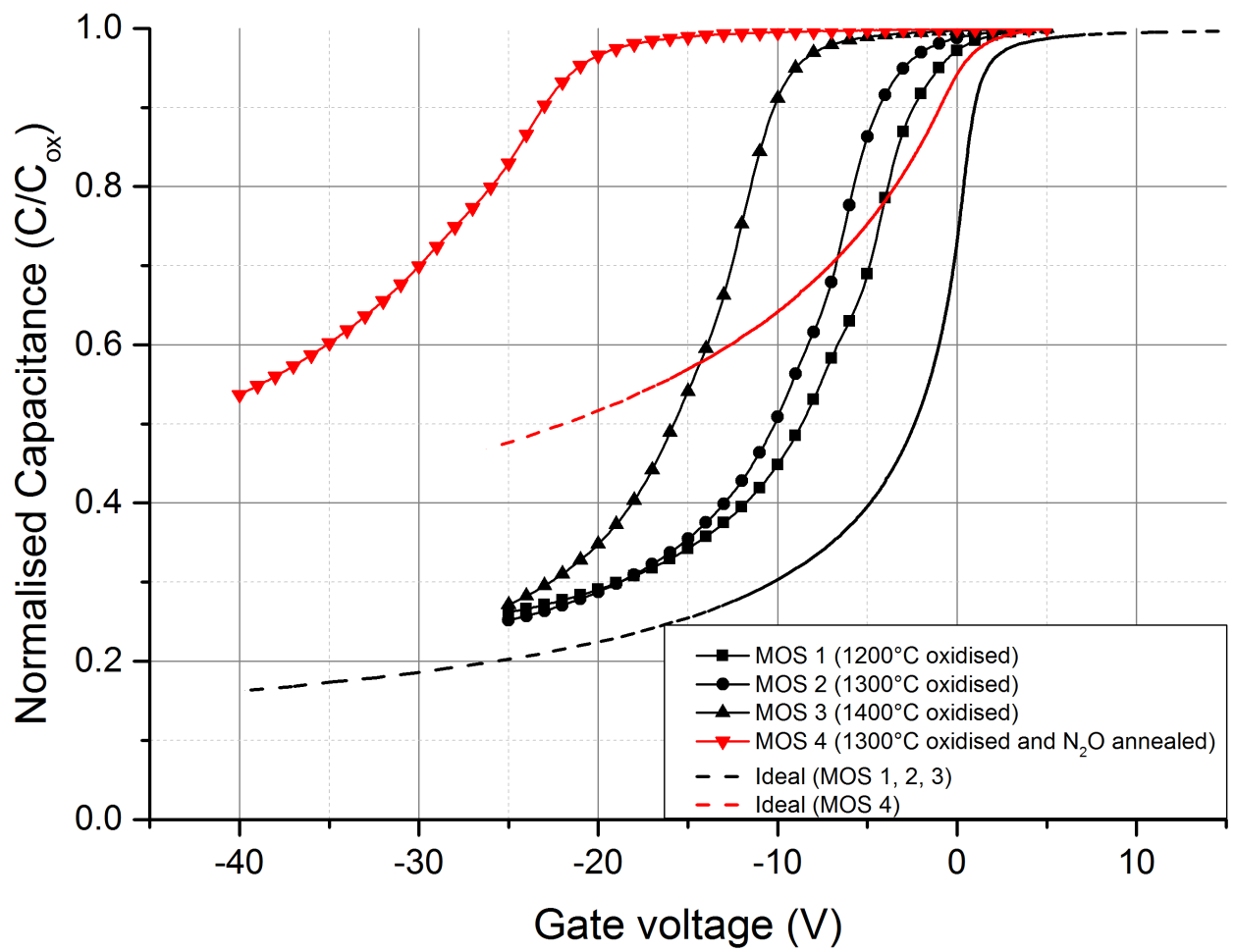


Figure 5.21: Ideal and experimental (1 MHz) normalised C-V curves for MOS 1- 4.

performed on all samples, and the N concentrations are plotted against the sputtering time in Figure 5.22. There is clearly a sharp peak of N concentration (black line) in MOS 4 results compared with the other samples, which means that similar to 4H-SiC, nitrogen atoms only accumulate at a very shallow depth at or around the 3C-SiC/SiO₂ interface.

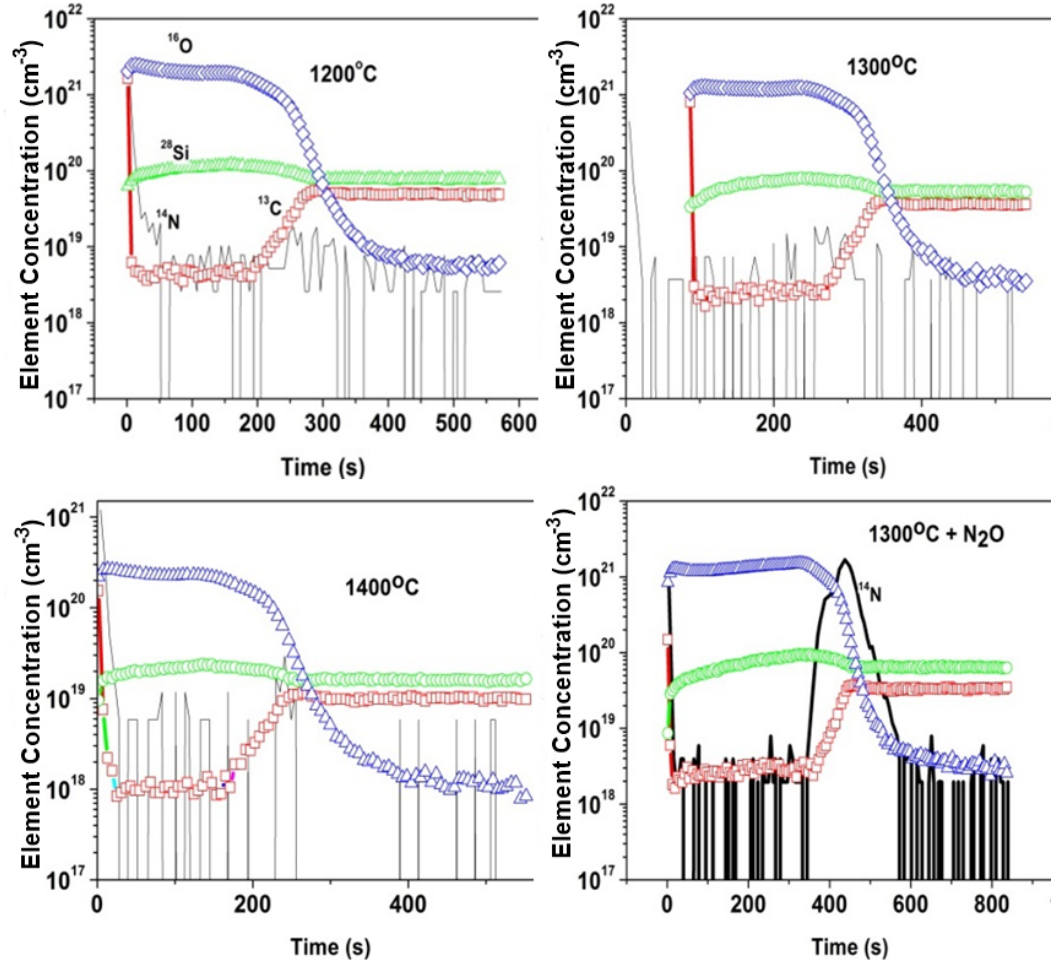


Figure 5.22: Si, C, O and N concentration profiles for (a) MOS 1, (b) MOS 2, (c) MOS 3 and (d) MOS 4 as a function of sputtering time, starting from the oxide surface.

The Terman method was applied using these 1 MHz C-V curves and D_{it} values are plotted against energy positions 0.2-0.6 eV away from the conduction band edge for all

samples in Figure 5.23. Regardless of the oxidation temperature, as-oxidised samples (MOS 1, 2 and 3) all have a D_{it} value around $3 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ at 0.2 eV position, which is already several times lower compared with the $\sim 1 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ value typically observed for dry oxidised 4H-SiC. Deeper into the bandgap, D_{it} values seem to increase with the oxidation temperature. MOS 4 achieved a three times lower value around $1 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ at 0.2 eV. A quick study using Terman method suggests a positive effect of including nitridation steps.

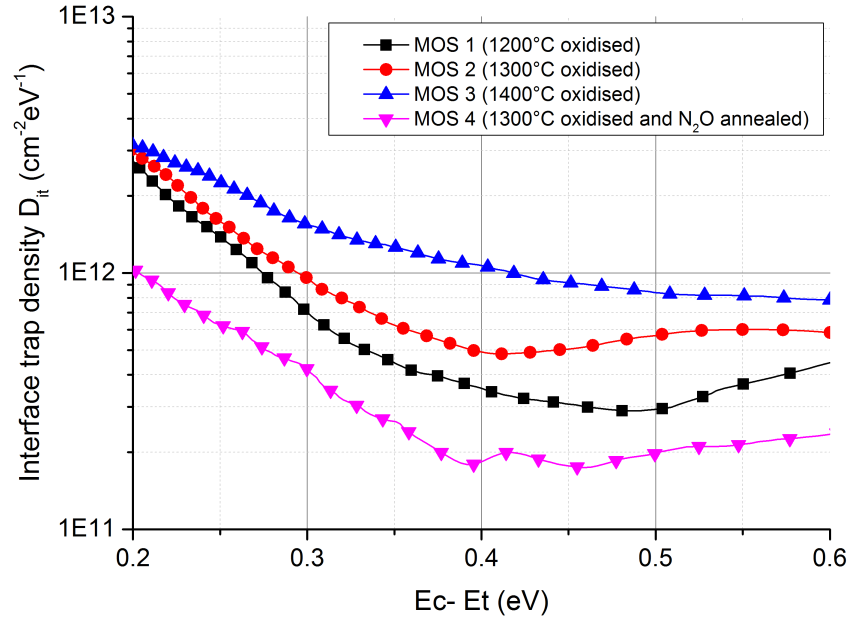


Figure 5.23: D_{it} as a function of energy positions for MOS 1-4 using Terman method.

5.3.3 Combined high-low C-V characterisation

Next the more commonly used high-low method was applied. Ideally, quasi-static rather than low frequency measurement should be applied. It is, however, usually not practical

due to the rapidly increasing noise levels in the C-V data obtained with lower probing frequency. For the 300 μm diameter MOS capacitor in this study, the minimum frequency before significant noise appears turned out to be 200 Hz. All devices were swept from accumulation to deep depletion with an AC signal magnitude of 25 mV and a frequency of 200 Hz. The resultant CV curves are plotted against 1 MHz curves in Figure 5.24. Dispersions between two curves in the depletion region are observed for all samples, confirming the existence of slow traps similar to those observed at the 4H-SiC/SiO₂ interface. Looking into Figure 5.25, MOS 4 still has the lowest D_{it} value among all, and the dry oxidised curves are almost the same in the whole 0.2 to 0.6 eV range.

5.3.4 Conductance method characterisation

Finally, the conductance method was also performed as an independent study. G-V curves were obtained for a frequency range of 1 kHz to 100 kHz and the AC signal magnitude was still 25 mV. Firstly the normalised G-V plots of all 4 samples are shown in Figure 5.26 for the frequency of 1 kHz. The area under the conductance peak is a measure for D_{it} . Devices (MOS 1-3) without the N₂O POA clearly have larger areas under G-V curves compared with MOS 4.

The measured G_p/ω vs ω curves (symbols) are plotted in Figure 5.27. By fitting the theoretical curves (lines) to the experimental ones, the D_{it} , trap time constant (τ_{it}) and the surface potential fluctuations (σ) are obtained as shown in Figures 5.28 and 5.29.

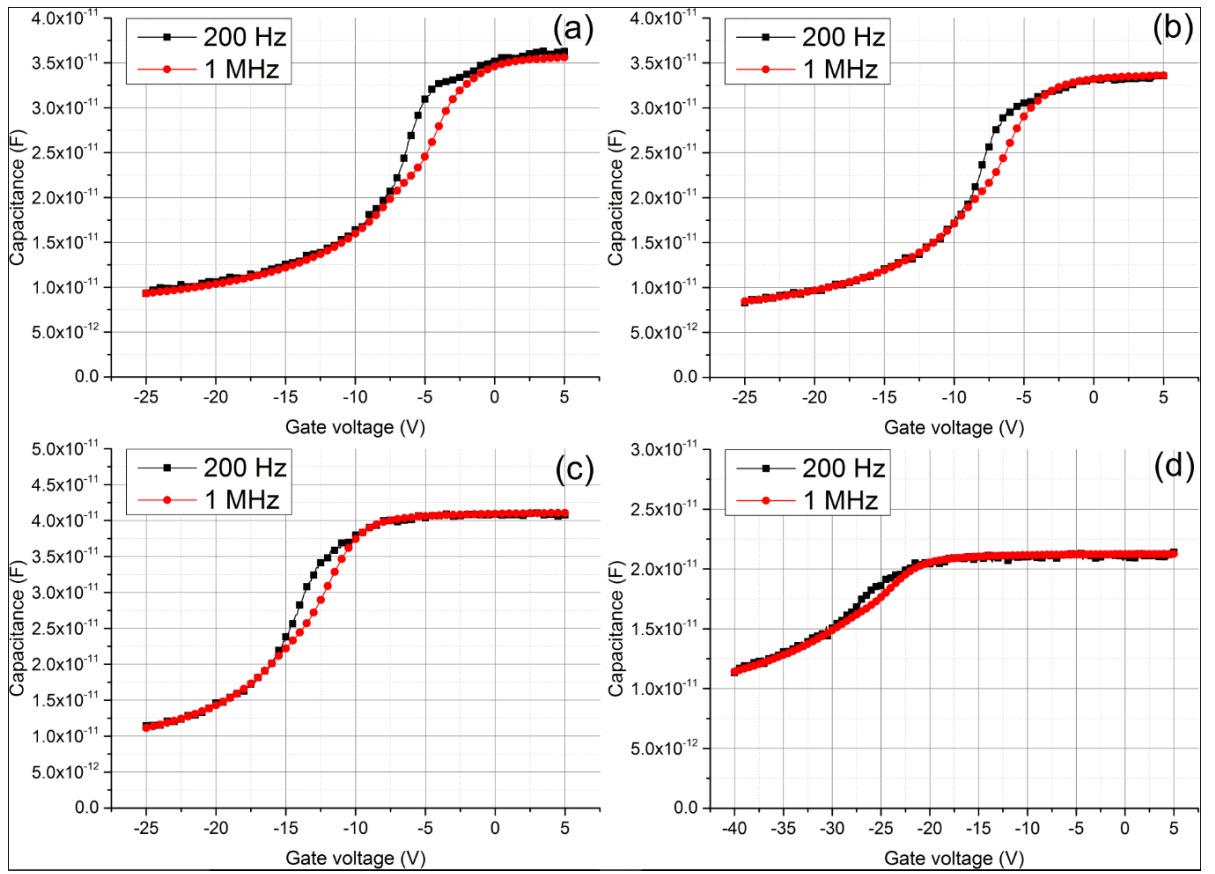


Figure 5.24: Typical 200 Hz-1 MHz C-V curves for (a) MOS 1, (b) MOS 2, (c) MOS 3 and (d) MOS 4.

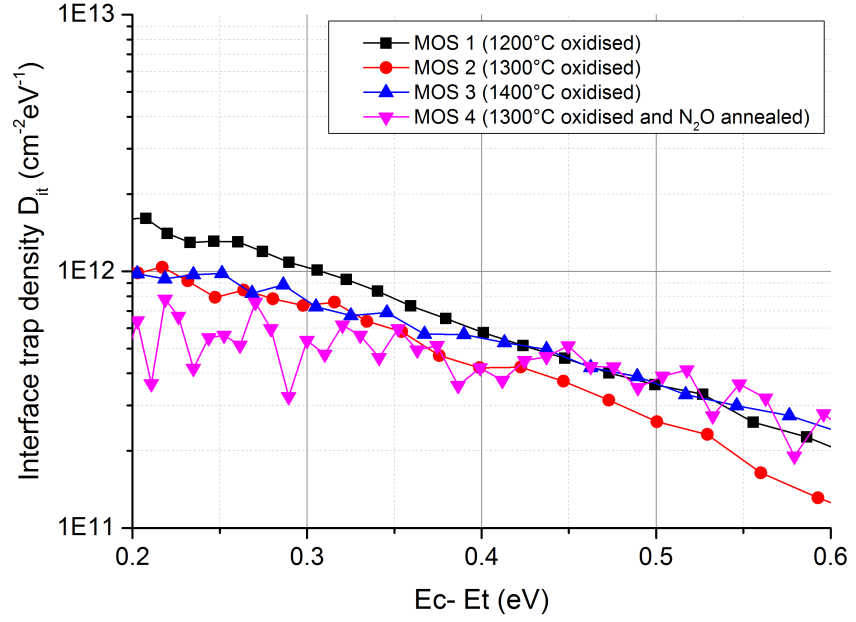


Figure 5.25: D_{it} as a function of energy positions for MOS 1-4 using high-low method.

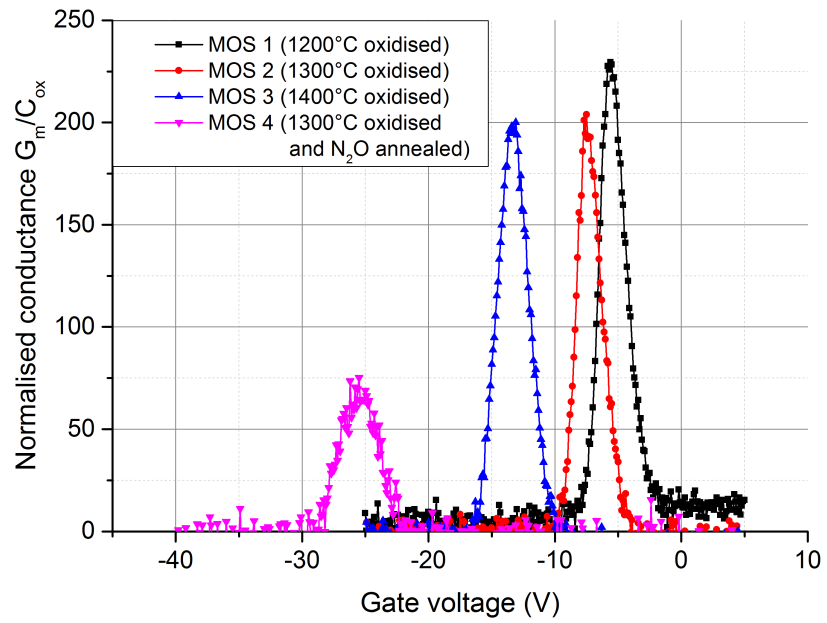


Figure 5.26: Normalised typical G-V curves of MOS 1-4 obtained for 1 kHz C-V measurement.

Since all SiC polytypes share the same valence band edge and 3C-SiC has a smaller band gap than 4H-SiC, the traps close to the 3C-SiC conduction band edge will lie deep in the 4H-SiC band gap. And also the traps sitting in the mid gap are slower than those close to the conduction band edge (also shown in Figure 5.29a), this explains why the obtained 3C-SiC trap time constants are almost one order of magnitude higher than those reported for 4H-SiC. For the dry oxidised samples (Figure 5.27a, b, c), a fit using a single τ_{it} seems to be impossible to cover both low and frequency regions, as can be noticed by the considerable departure of experimental curve from the theoretical one around 100 kHz. It means that apart from the slow traps previous identified by high-low method, there may also be fast traps existing at the 3C-SiC/SiO₂ interface. Unfortunately, even increasing the measuring frequency to 2 MHz (the facility capability) did not unveil the other peak position, thus the D_{it} curves in Figure 5.28 only represent the slow traps. For MOS 4, the experimental curve has no Gaussian dispersion or a very wide Gaussian dispersion, indicating a huge σ . As a result, it is not possible to fit using a theoretical curve. The conductance method leads to a similar conclusion as the high-low method, that is, a higher oxidation temperature did not reduce the D_{it} value.

Apart from the D_{it} values, it is not difficult to find out that the peaks in Figure 5.27 shifted to the lower frequency with the increasing oxidation temperature, as confirmed by the fitting trap time constants shown in Figure 5.29a. σ values used in curve fittings for MOS 1-3 are shown in Figure 5.29b, which indicates a worsened surface potential uniformity with the increasing oxidation temperature.

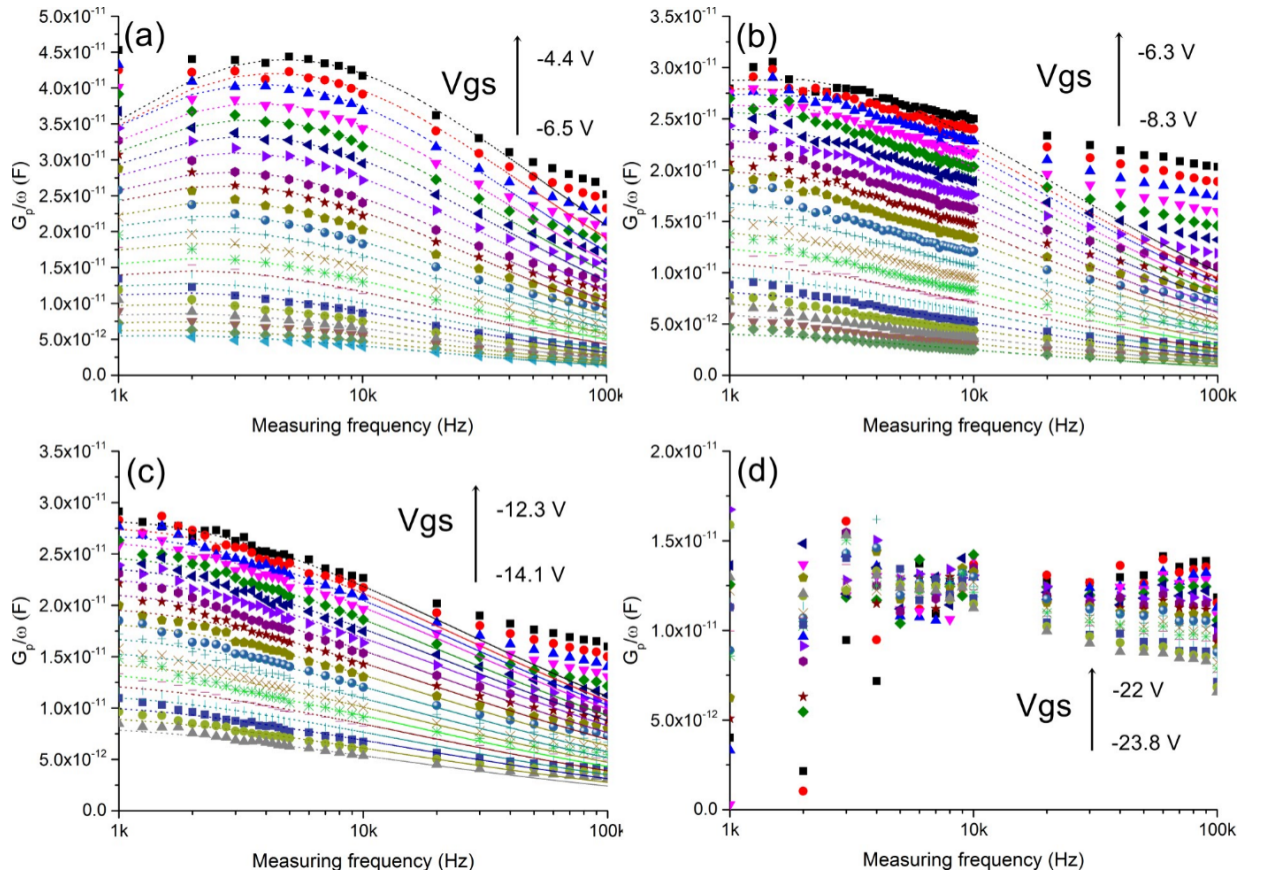


Figure 5.27: Theoretical and experimental G_p/ω vs ω curves for (a) MOS 1, (b) MOS 2, (c) MOS 3 and (d) MOS 4.

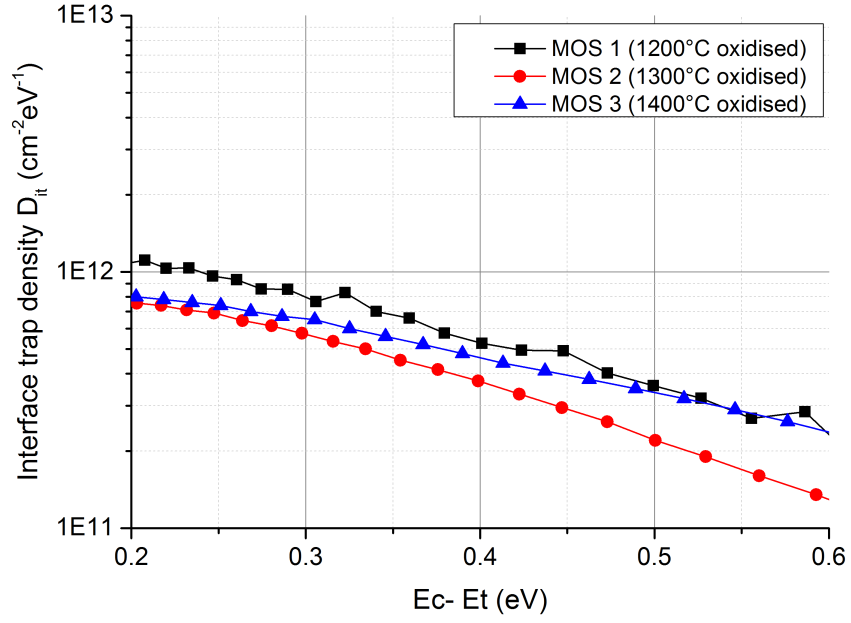


Figure 5.28: D_{it} as a function of energy positions for MOS 1-3 using conductance method (MOS 4 curve missing because it is impossible to fit the experimental curve).

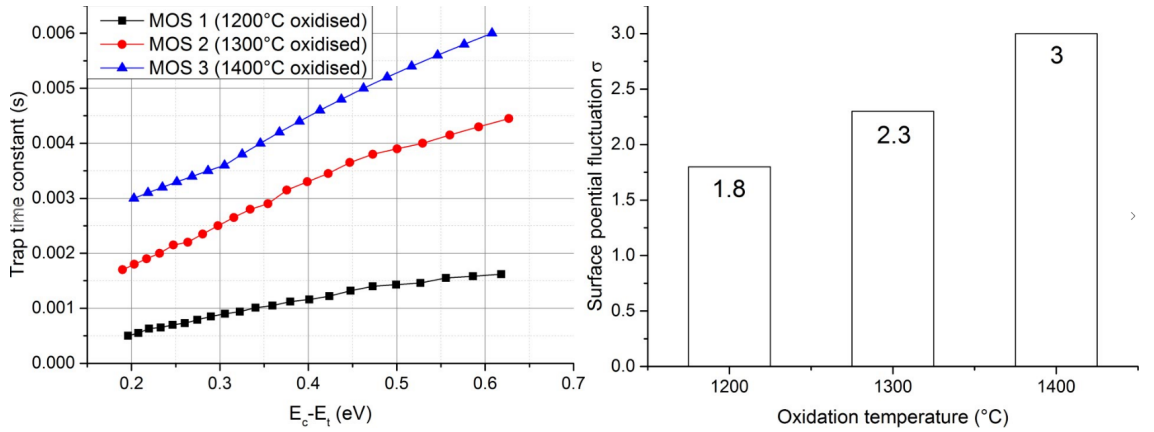


Figure 5.29: Extracted (a) trap time constants and (b) surface potential fluctuations of MOS 1, 2, 3 using conductance method.

5.3.5 Comparing Terman, high-low and conductance methods

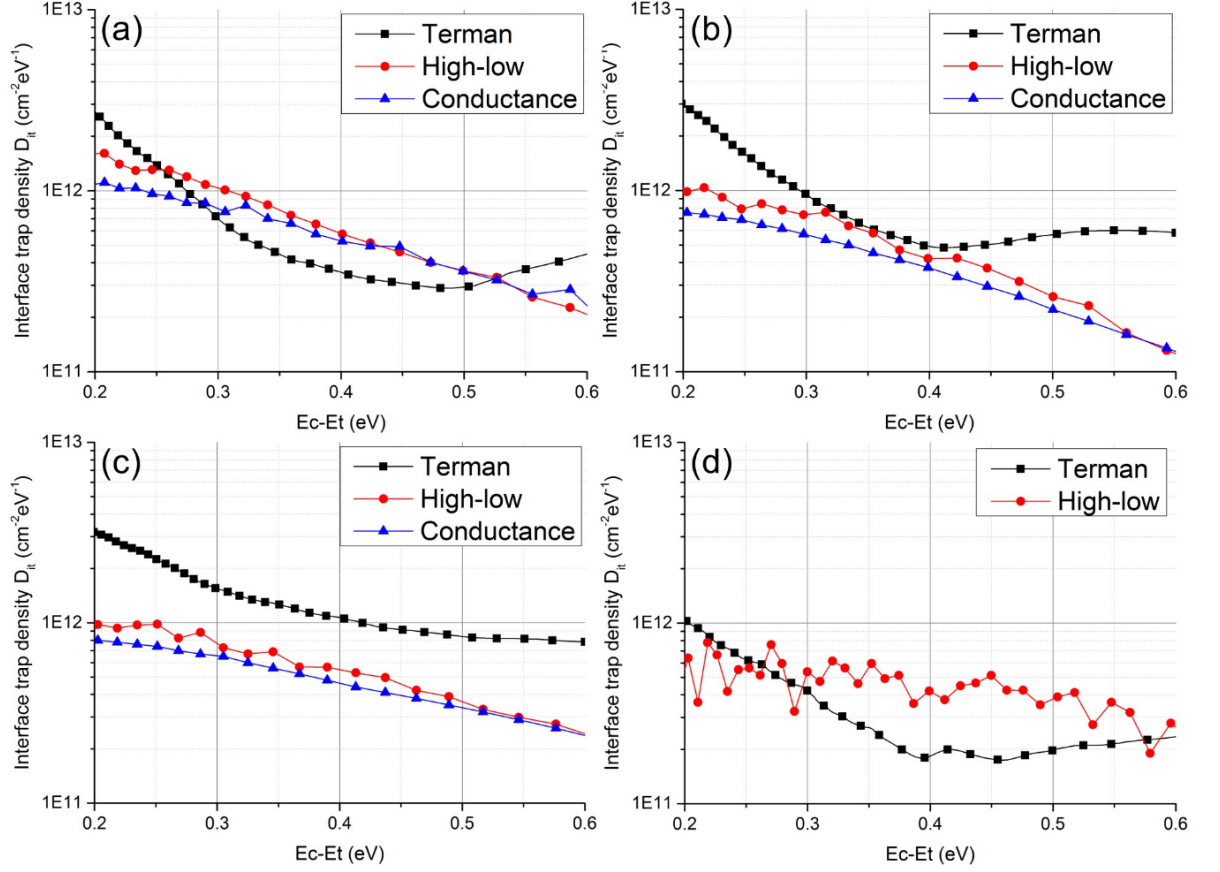


Figure 5.30: Comparisons between the D_{it} curves obtained using Terman, high-low and conductance methods for (a) MOS 1, (b) MOS 2, (c) MOS 3 and (d) MOS 4.

D_{it} obtained using different techniques are repeated in Figure 5.30. It can be seen that the high-low and conductance methods consistently give similar results regardless of the oxidation temperature, while the Terman results are only matching the other two for the lowest oxidation temperature (Figure 5.30a). Both Terman and high-low methods do not take the surface potential fluctuations into consideration, however, the similarity between high-low and conductance method results suggest this may not be as a serious

issue for 3C-SiC/SiO₂ interface. σ values of the fabricated MOS capacitors are around 2 to 3 as seen in Figure 5.29b, while for 4H-SiC, the typically obtained value is around 4 [166]. This also explains why high-low method proved to be more accurate for Si and less for 4H-SiC, since Si also has a σ value generally around 2. For MOS 2 and 3, the fact that Terman method gives considerable higher D_{it} than both high-low and conductance methods can be explained by its larger sensitivity to σ . Indeed, the dispersion between the Terman results with the other two methods can be found to decrease for a lower oxidation temperature, namely smaller σ . For MOS 4, Terman and high-low methods give D_{it} values at the same level probably due to the fact that now σ is too big that the high-low method is no longer reliable, either. The real D_{it} value should be lower than both of them, although cannot be known using the conductance method due to the huge noise in the G_p/ω vs ω curves.

5.3.6 High temperature effects on the 3C-SiC physical features

As said before it is the first time 3C-SiC is oxidised above 1200°C, as such it is useful to check if this high temperature had degraded the physical properties of the 3C-SiC epilayer. Such analyses were performed after all the electrical characterisations.

Figure 5.31 shows the AFM images obtained on all 4 samples after wet etching away Al gate in H₂SO₄ contained etchant and the oxide in HF. The RMS roughness values all lie in the range of 0.5~0.6 nm, indicating the high temperatures above 1200°C does

not have significant detrimental effects on the 3C-SiC surface. Also, XRD spectrums for as-grown 3C-SiC epilayers and after high temperature oxidations are shown in Figure 5.32. It can be seen that the main 3C-SiC(200) peak has not shifted after the oxidation process, although the peak width is slightly widened, which suggests that the 3C-SiC crystal quality is not much compromised, either.

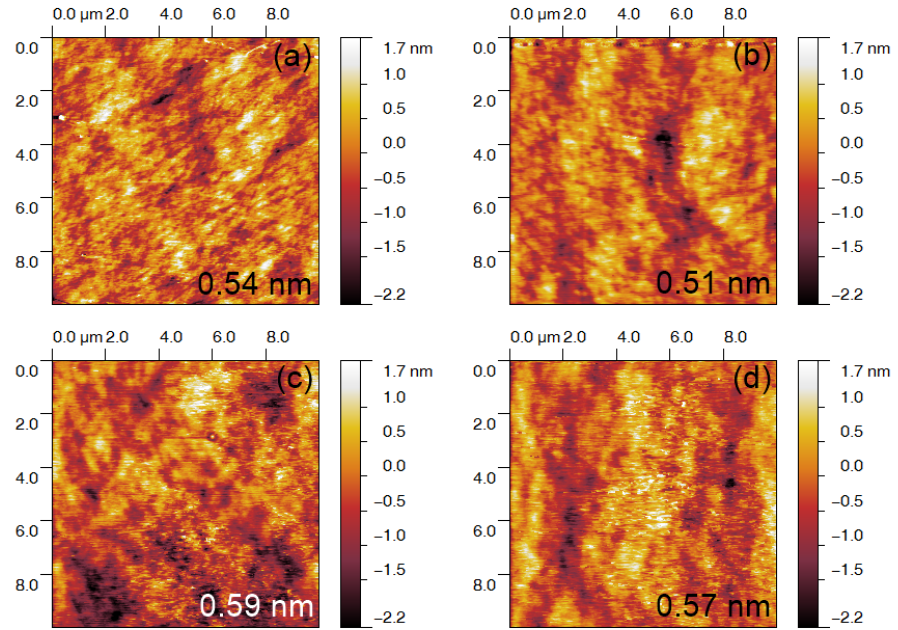


Figure 5.31: AFM images of the 3C-SiC surface for (a) MOS 1, (b) MOS 2, (c) MOS 3 and (d) MOS 4 after removing the gate oxide by HF etching, inset values are RMS surface roughness.

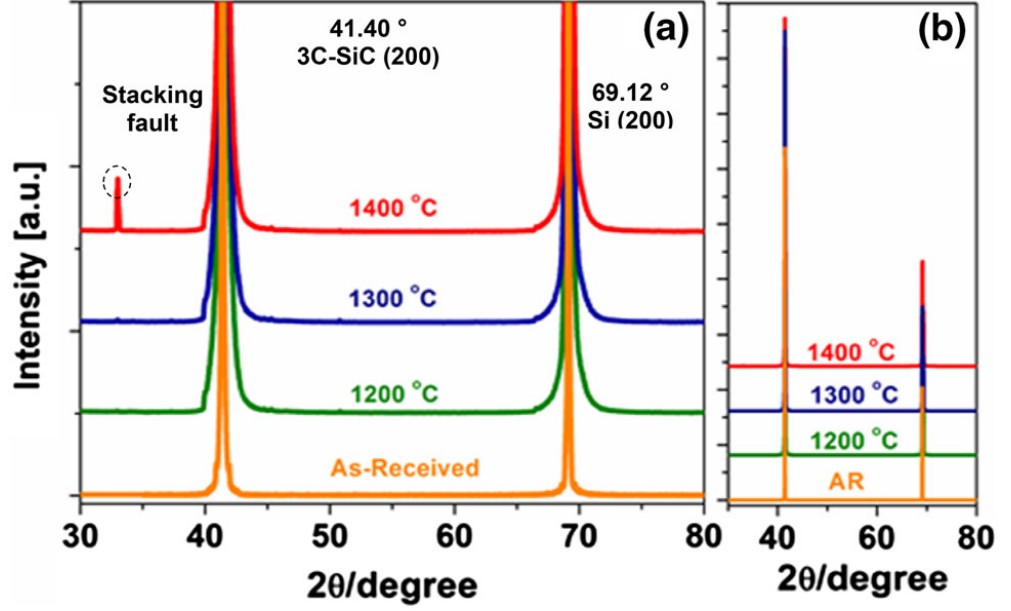


Figure 5.32: XRD spectrum of the 3C-SiC epilayer before and after the gate oxidation.

5.4 Summary

In this chapter, a study of the 3C-SiC/SiO₂ MOS interface has been performed by fabricating lateral MOS capacitors on n-type doped 3C-SiC(001)/Si wafers. The electrical performance of the fabricated MOS capacitors were characterised by various techniques including Terman, high-low and conductance method. While the low surface potential fluctuation value (σ) similar to Si indicates that the 3C-SiC/SiO₂ interface is electrically better than its 4H-SiC counterpart, no extra advantage was gained by growing the 3C-SiC/SiO₂ interface at higher oxidation temperatures. MOS capacitors fabricated with 1200°C, 1300°C and 1400°C oxidation process all have a D_{it} value around 1×10^{12} cm⁻²eV⁻¹. Nitridation (N₂O POA) of the interface proved to be effective in reducing the

trap density values, although a negative shift of V_{fb} was accompanied due the counter-doping effect. The conductance method indicates that there may be additional super fast traps, which unfortunately requires C-V measuring frequency above 2 MHz, which is the facility capacity in the lab thus could not be characterised.

The very first MOSFET device previously shown in Figure 5.3 had a long channel region, leading to excessive on-state resistance which is not appropriate for power electronics, thus only applied in low power levels such as microprocessors, micro-controllers and logic circuits. On the other hand, the voltage-control and fast-switching features of MOSFETs are very attractive for power switch applications, consequently much efforts had been put into making power MOSFETs.

The first high-voltage structure was developed in 1970s and called V-MOSFET [169], named after the V-shape groove channel as seen in Figure 6.1a. This design never became popular due to the difficulty in fabricating a smooth V-shape trench on Si substrates, which was at that time formed by potassium hydroxide based etching whereas etching rate varies in different crystal orientations [126]. Also, the pointy trench bottom causes severe electric field crowding and easily leads to device early breakdown. Not long after,

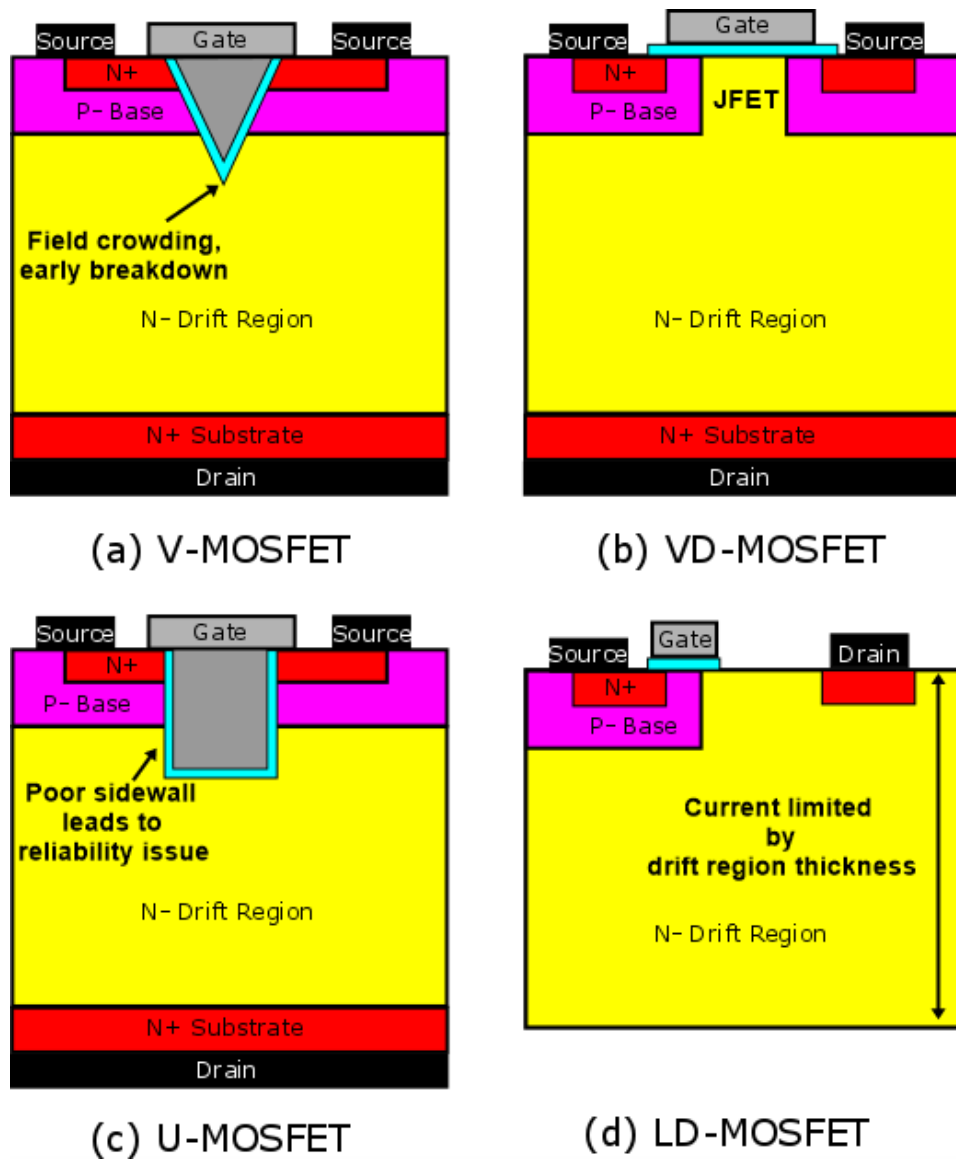


Figure 6.1: Schematic structure views of various MOSFET designs.

a planar structure shown in Figure 6.1b was invented. Instead of a V-shape groove, the channel was defined by controlling the thermal diffusion of dopants in the P-base and N⁺ source regions, thus called Vertical-Diffused (VD) MOSFET. With main features relatively easy to fabricate and quite reliable, VD-MOSFET is the most successful design up to date. To achieve higher forward current density, the cell pitch of VD-MOSFET is usually made as small as possible. However, the narrow JFET region between two P-bases restricts the current flowing between channels and the drift region, inducing extra on-resistance [170]. In the late 1980s, U-MOSFET design (Figure 6.1c) was proposed as a potential solution to getting rid of the JFET region. U-MOSFET is similar to the V-groove design in the sense that both of them use a trench to eliminate the JFET region, reducing the device on-resistance. By the time U-MOSFET was proposed, Si etching technology had been greatly improved that rounded trench corners are possible with reactive ion etching and other techniques [171]. However, the trench MOS interface and oxide reliability issues are not fully solved yet, consequently U-MOSFETs still cannot compete with their planar counterparts for now.

All three power MOSFET designs introduced above have a vertical structure to maximise current handling ability of discrete devices. For vertical devices, the current rating can be increased by simply enlarging the device active area, such as bigger contacts for diodes or more parallellised cells for MOSFETs. In some applications where power devices and control & logic circuits are integrated (e.g. smart power devices, power ICs), the processing and packaging may require all electrodes to be on the same side of the

device, which makes a lateral design necessary and this is where Lateral-Diffused (LD) MOSFET fits in. As a modification from the long channel design, LDMOSFET usually has a much shorter channel length to minimise the on-resistance. Meanwhile, a long drift region is included for high voltage purpose as seen in Figure 6.1d. Unlike vertical designs whose breakdown voltage is constrained by the drift region (epilayer) thickness, LDMOSFET can utilise the semiconductor surface to greatly increase the device blocking voltage. Inevitably, the current conducting ability of LDMOSFET has to be greatly compromised. As a result, LDMOSFETs are mostly used for RF power amplifiers, microwave and medium power switching applications. In Section 2.6.3, the poor quality of the 3C-SiC/Si heterojunction was illustrated by TEM analysis. To minimise the heterojunction influences on device performance, lateral MOSFETs rather than vertical ones were fabricated on 3C-SiC(001)/Si wafers.

The remainder of this chapter will be talking about fabricating 3C-SiC MOSFET devices. Firstly the MOSFET characterisation tool is briefly introduced, after which the manufacturing and analysis of long channel lateral 3C-SiC MOSFETs with various oxidation conditions are demonstrated. Electrical characterisation was performed at both room and elevated temperatures to study the dominant scattering mechanisms of 3C-SiC MOS interfaces processed in different ways. The conclusions were then put into fabricating short channel 3C-SiC LDMOSFETs. The forward conducting advantage of 3C-SiC LDMOSFET is demonstrated in comparison with a 4H-SiC reference device.

6.1 Channel Mobility Characterisation Tool

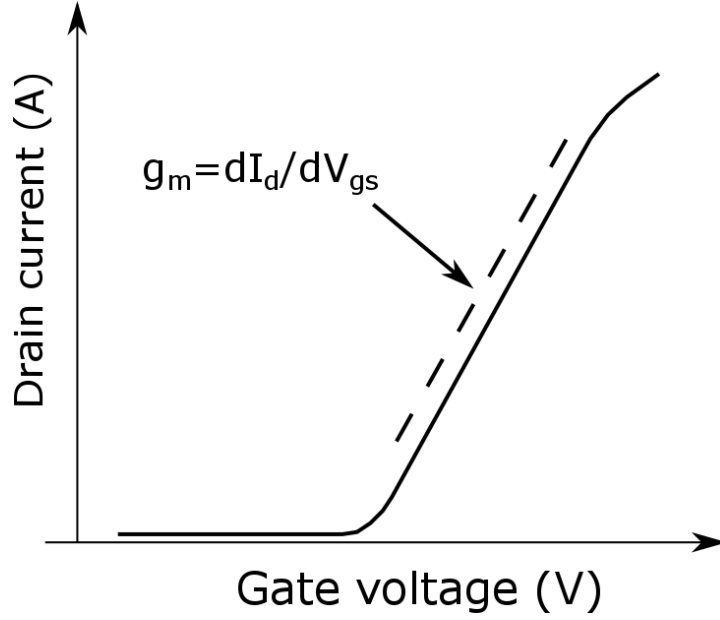


Figure 6.2: Typical transfer curve of a MOSFET.

From the typical MOSFET turn-on I-V response shown in Figure 6.2, the gate transconductance g_m can be extracted from the slope of the linear part of the curve. If the measured device resistance only comes from the channel, R_{ch} in Equation 5.2 can then be replaced by V_{ds}/I_{ds} as Equation 6.1 below:

$$I_{ds} = V_{ds} \frac{Z_{ch} \mu_{ch} C_{ox} (V_{gs} - V_{th})}{L_{ch}} \quad (6.1)$$

Assuming channel mobility μ_{ch} is independent of V_{gs} , there is:

$$\frac{dI_{ds}}{dV_{gs}} = g_m = V_{ds} \frac{Z_{ch}\mu_{ch}C_{ox}}{L_{ch}} \quad (6.2)$$

Solve Equation 6.2 for the mobility:

$$\mu_{ch} = \frac{L_{ch}g_m}{Z_{ch}C_{ox}V_{ds}} \quad (6.3)$$

This is called field-effect mobility μ_{FE} , which is usually lower than the real mobility value since it neglects the electric field dependence of the channel mobility, which has been explained in section 5.1.3. Nevertheless, it is still the most frequently used indicator for MOSFET channel mobility evaluations.

6.2 μ_{FE} Study of Long Channel Lateral

3C-SiC(001)/Si MOSFETs

Last chapter investigated the 3C-SiC/SiO₂ interface by fabricating MOS capacitors and analysing the interface trap densities, which gives a guideline of the MOS feature electrical properties. Using the technique introduced in the previous section, the channel mobility of a 3C-SiC MOSFET can be directly measured. In this section, a thorough study on long channel MOSFETs fabricated with various gate oxidation steps is conducted. Apart from

the O₂ dry oxidation and N₂O nitridation previously studied on lateral MOS capacitors, the effect of high temperature hydrogenation process using wet oxidation/POA is also evaluated.

6.2.1 Experimental work

For the long channel lateral MOSFET fabrications, 4 μm thick n-type non-intentionally doped CVD grown 3C-SiC epilayer on Si(001) substrate provided by NOVASiC was used. Al and N were implanted to form the P-body and N+ source/drain regions. Instead of an as-grown P-type epilayer, it was decided to implant the n-type epilayer surface into P-body because this is a better representation of the actual power MOSFETs fabrication process. Both implantations use multiple energies and doses to form box profiles. For the N+ source and drain regions, the room temperature “high dose” condition specified in Chapter 3 (Table 3.1) was applied to achieve a peak N concentration around $6 \times 10^{20} \text{ cm}^{-3}$. The P-body implantation energies and doses are shown in Table 6.1. SRIM simulation indicates the resultant P-body box profile has a peak Al concentration around $1 \times 10^{18} \text{ cm}^{-3}$ as illustrated in Figure 6.3. Energies as high as 500 keV were used to achieve an implant depth of around 600 nm so that it will include the N+ regions which was around 300 nm deep. It is known that acceptors are more difficult to activate than donors because of their deeper energy levels, and the 3C-SiC/Si wafer processing temperature is limited by the Si melting point 1412°C, consequently a relative high Al dose was applied and

Table 6.1: Al implantation doses and energies for the P-body region.

	35 keV	80 keV	150 keV	250 keV	350 keV	500 keV
Dose (cm^{-2})	3×10^{12}	6.5×10^{12}	9.5×10^{12}	1.1×10^{13}	1.1×10^{13}	2.2×10^{13}

the implantation was conducted at 600°C, both aiming to increase the resultant active acceptor concentration in the channel region.

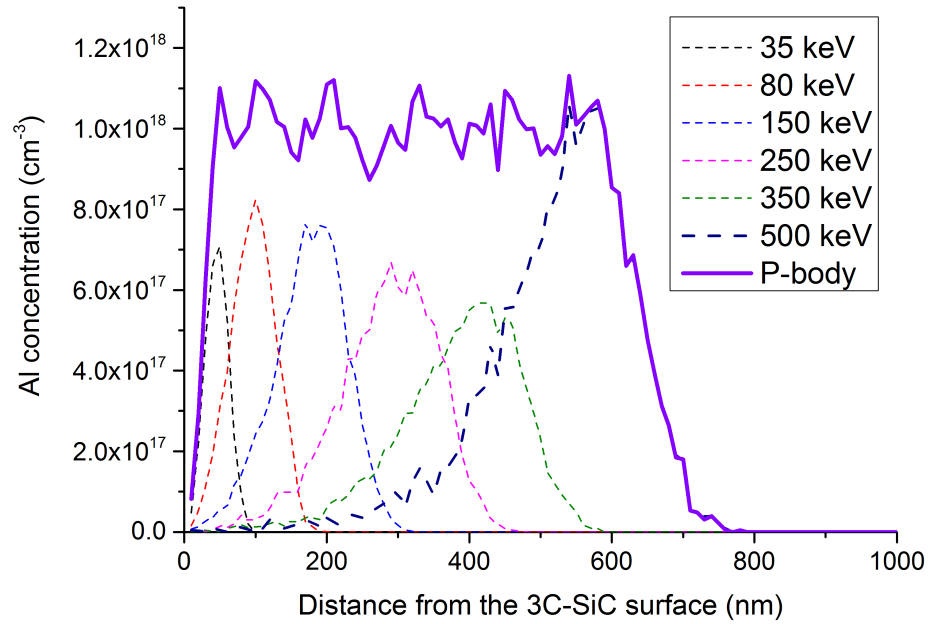


Figure 6.3: SRIM simulated doping profile for the Al implanted P-body layer.

After ion implantations, wafers were cut into 5 mm \times 5 mm chips. All samples went through a 1 hour post implantation annealing process at 1375°C in Ar atmosphere (5 slm) to activate both Al and N dopants. No surface protection caps were applied. Prior to the gate oxidation, all samples were cleaned following the same procedures (solvent, Piranha then RCA) as MOS capacitors. To remove the ion implantation induced damage in the surface region, a sacrificial oxidation at 1300°C for 2 hours (1 slm dry O₂)

followed by a deep HF dip (10 min) was performed. After that, various gate oxidation processes including O₂ dry oxidation, O₂ wet oxidation/POA, and N₂O oxidation/POA were conducted to form 3C-SiC/SiO₂ interfaces. Due to a considerably higher oxidation rate of the implanted layer than the epilayer, a lower concentration precursor gas (1 slm precursor gas + 4 slm Ar) than MOS capacitors was fed to the furnace during the oxidation stage as seen in Figure 6.4. For O₂ wet oxidation, the oxygen gas went through a bubbler heated at 95°C before entering the oxidation furnace. Ti30nm/Ni100nm bilayer Ohmic contacts annealed in Ar ambient at 1000°C for 1 minute were fabricated in the N+ regions. Finally, Al gate was patterned using a standard lift-off technique. The finished device has a channel length of 150 μm and a width of 300 μm as seen in Figure 6.5. An optical photo of the fabricated MOSFET devices is shown in Figure 6.6 for reference.

6.2.2 3C-SiC oxidation rate

Due to the limited information on 3C-SiC, an oxidation rate test was conducted to set up a benchmark for further study. Al implanted 3C-SiC samples were oxidised for 1 to 4 hours at 1300°C in three different atmospheres, 20% dry oxygen, 20% wet oxygen, and 20% N₂O, all with Ar as the carrier gas making up a total gas flow of 5 slm. The resultant oxide thicknesses were obtained by an ellipsometer and are plotted in Figure 6.7. Clearly O₂ wet oxidation is much faster than the other two, and N₂O dry oxidation is the slowest, but quite close to O₂ dry oxidation.

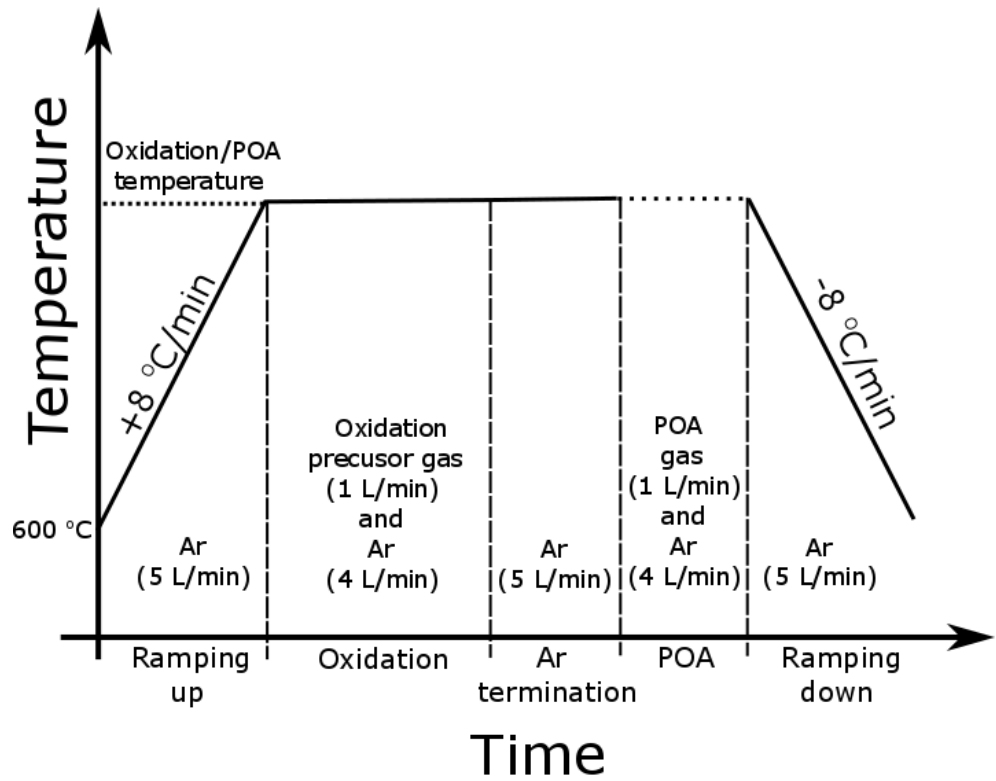


Figure 6.4: A general description of the lateral MOSFET gate oxidation process.

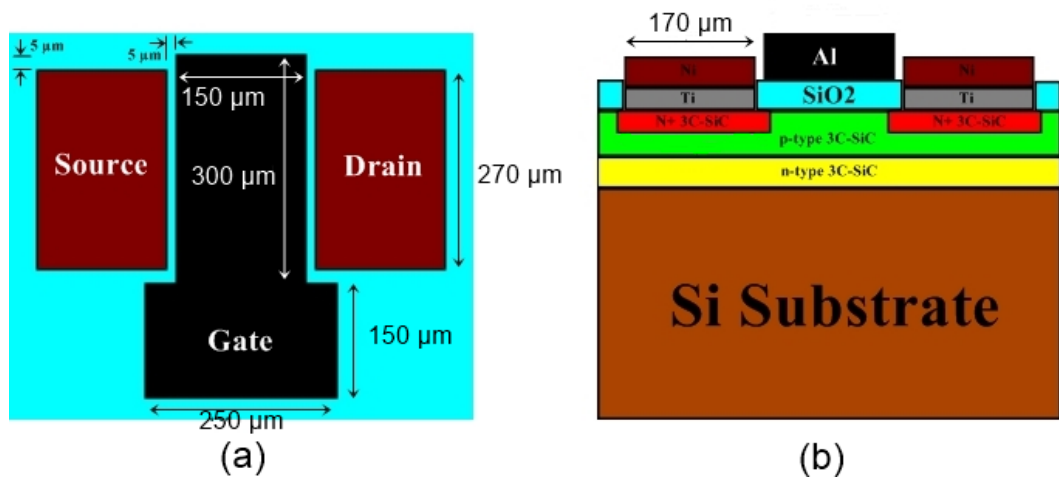


Figure 6.5: Schematic diagrams of (a) top and (b) side view of the fabricated lateral MOSFETs.

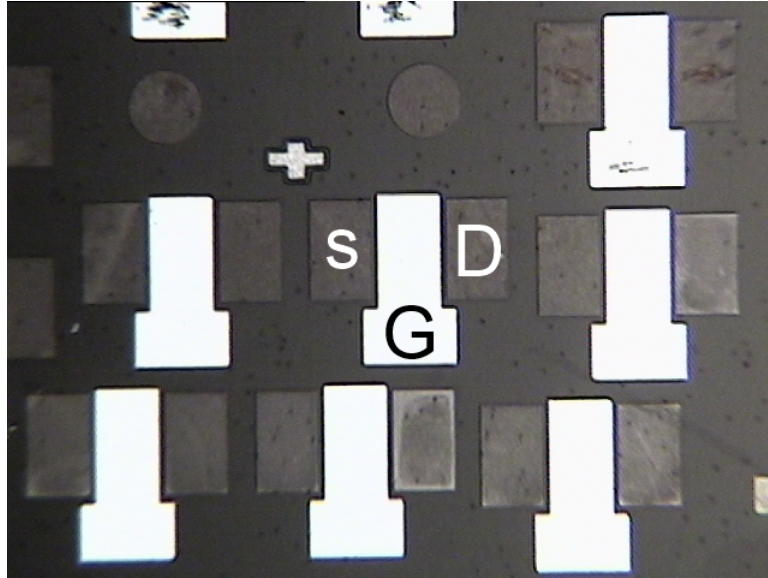


Figure 6.6: An optical figure of the fabricated 3C-SiC lateral MOSFETs, with source (S), drain (D) and gate (G) specified.

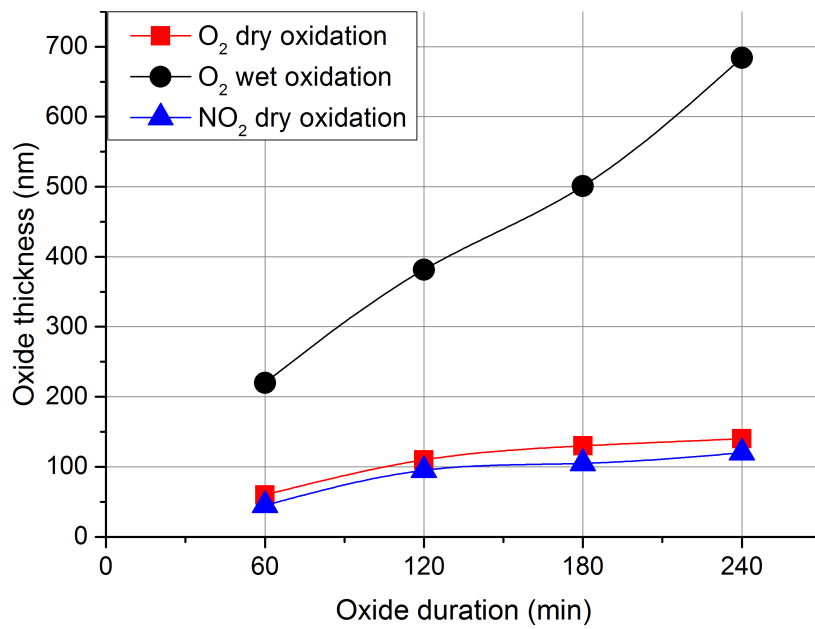


Figure 6.7: 1300°C 3C-SiC oxidation rate test (5 slm total gas flow, 20% precursor gas and 80% Ar).

Table 6.2: Oxidation conditions for the devices with different oxidation temperatures (1200°C, 1300°C and 1400°C) and atmospheres (dry O₂, dry N₂O, and wet O₂).

Sample	Oxidation process	Oxide thickness
1	5 slm diluted O ₂ (O ₂ :Ar=1:4) at 1200°C for 240 mins	≈ 42 nm
2	5 slm diluted O ₂ (O ₂ :Ar=1:4) at 1300°C for 90 mins	≈ 93 nm
3	5 slm diluted O ₂ (O ₂ :Ar=1:4) at 1400°C for 20 mins	≈ 61 nm
4	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1200°C for 240 mins	≈ 37 nm
5	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 90 mins	≈ 85 nm
6	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1400°C for 20 mins	≈ 55 nm
7	5 slm diluted wet O ₂ (O ₂ :Ar=1:4) at 1200°C for 60 mins	≈ 57 nm
8	5 slm diluted wet O ₂ (O ₂ :Ar=1:4) at 1300°C for 15 mins	≈ 70 nm
9	5 slm diluted wet O ₂ (O ₂ :Ar=1:4) at 1400°C for 5 mins	≈ 75 nm

6.2.3 Oxidation temperature effects on μ_{FE}

In last chapter we investigated the oxidation temperature effects by fabricating lateral MOS capacitors and it was concluded that it has little effects on the reduction of slow traps. Here we repeat the experiments (1200°C, 1300°C and 1400°C) on lateral MOSFETs and directly evaluate the μ_{FE} values. Additionally, N₂O direct oxidation and O₂ wet oxidation were also studied. Detailed oxidation conditions are specified in Table 6.2.

All devices have typical turn-on behaviours as shown in Figure 6.8 for a drain bias of 0.1 V. Since the gate oxide thickness for these devices vary quite a lot as shown in Table 6.2, gate field (MV/cm) instead of gate voltage V_{gs} (V) is used as x-axis for direct compar-

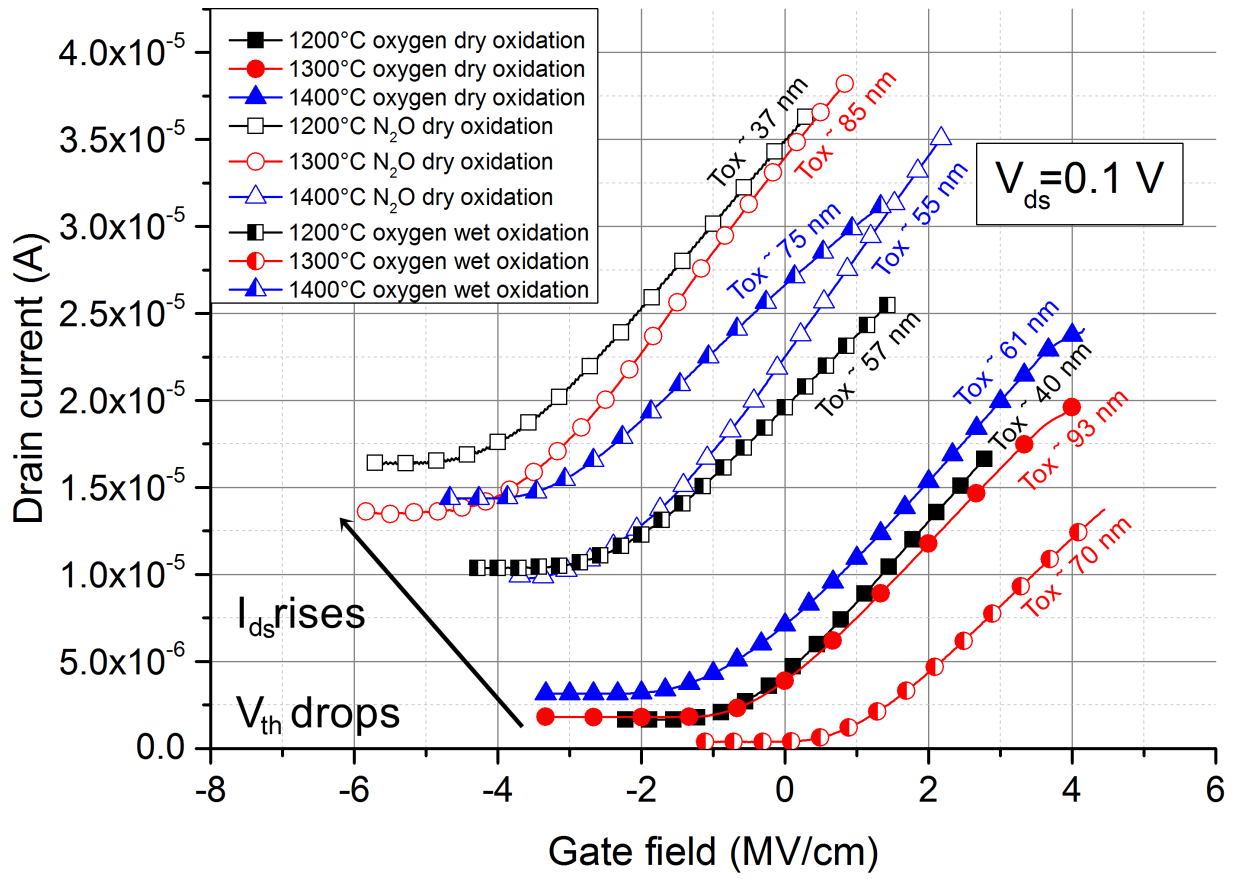


Figure 6.8: Turn-on behaviours of MOSFETs fabricated with different gate oxidation temperatures, $V_{ds}=0.1 \text{ V}$ for all measurements.

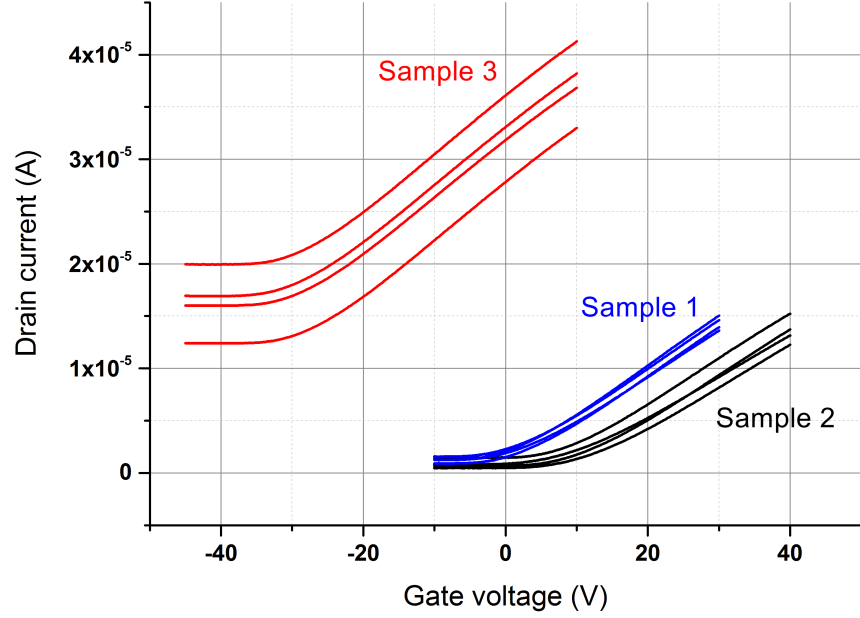


Figure 6.9: Turn-on behaviours of MOSFETs fabricated with the same wet oxidation process at 1300°C for 15 mins, $V_{ds}=0.1$ V for all measurements.

isons between samples. Regardless of the oxidation conditions, almost all MOSFETs are normally-on devices with a negative V_{th} , which agrees to last chapter that considerable positive charges exist at the 3C-SiC MOS interface. The commonly observed [159,161,162] negative V_{th} of 3C-SiC MOS devices can be explained by the carbon-cluster interface traps model [172], which describes that due to the smaller band gap, only donor-like interface states (carbon clusters/dangling bonds) are present at the 3C-SiC/SiO₂ interface. Consequently, 3C-SiC MOS interface is normally positively charged and demonstrates a negative V_{th} [154]. In addition, Figure 6.8 demonstrates that there is a clear relationship between more negative V_{th} and higher channel leakage current. The abnormal high leakage current should be caused by stacking faults [161] acting as leakage current paths in device off-

state. Defects may have propagated into the gate oxide from the epilayer, creating more fixed charges in the oxide grown on more defective regions. It should be noted here that, a typical or reproducible I-V characteristic for these devices even with the same processing steps is difficult to obtain. As shown in Figure 6.9, V_{th} values obtained for samples with identical processing steps or even devices on the sample can be quite inconsistent, thus only best results namely those with least leakage currents are shown in Figure 6.8. This indicates that the sample defective condition, rather than the fabrication processing, has a dominant effect on the resultant device leakage currents and threshold voltages.

A representative forward conduction curve of the fabricated lateral MOSFETs is shown in Figure 6.10 for a device with gate oxide grown at 1300°C in dry O₂. It can be seen that the leakage current contributes significantly to the overall forward current and is hardly affected by the gate bias. The leakage current for $V_g < 0$ does not decrease if gate voltages goes to even lower values. By subtracting the leakage contribution from the overall forward current, a more typical MOSFET forward I-V curve can be obtained as seen in Figure 6.11.

The positive charges and high leakage current observed are issues for power devices fabrications, since extra charges are known to degrade the MOS interface reliability and leakage current is least desired in device off-state. For now, the study here can be continued since Equation 6.3 shows that μ_{FE} is determined by trans-conductance (slope of the transfer curve linear part) rather than the absolute current levels. μ_{FE} are plotted against gate bias in Figure 6.12 for all samples and again the gate field rather than gate voltage

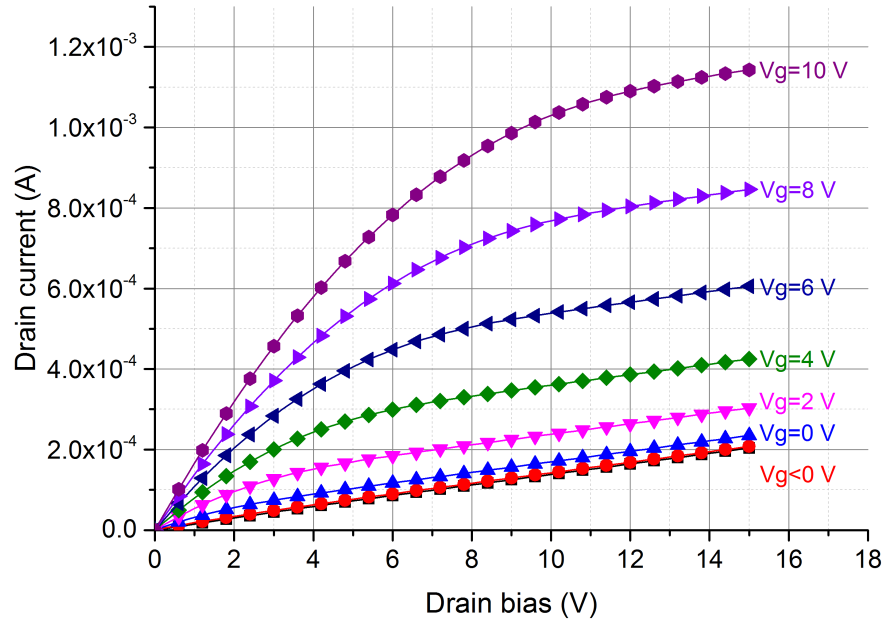


Figure 6.10: Representative forward output characteristics of lateral MOSFETs (1300°C O₂ dry oxidation).

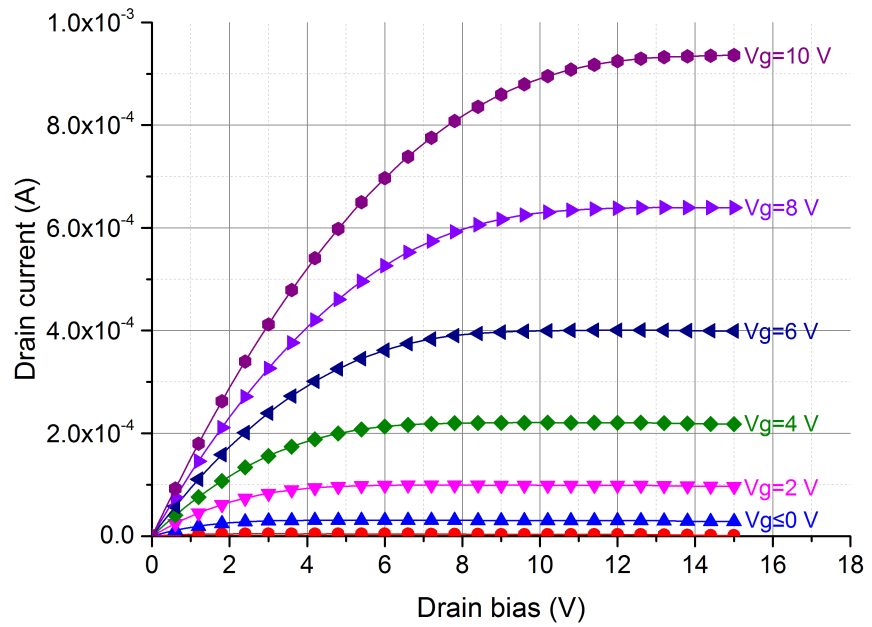


Figure 6.11: Forward characteristics of lateral MOSFETs (1300°C O₂ dry oxidation) with the leakage current part removed.

is used as x-axis for the same reason mentioned before. Figure 6.12a demonstrates that μ_{FE} of dry O_2 oxidised samples remains around $70 \text{ cm}^2/\text{V.s}$ regardless of the oxidation temperature, which is also consistent with previous MOS capacitors results. In Figure 6.12b it can be seen that N_2O direct oxidation at 1200°C does not lead to noticeable μ_{FE} improvements, while values approaching $90 \text{ cm}^2/\text{V.s}$ are obtained for 1300°C and 1400°C conditions. This indicates that the nitrogen passivation process for 3C-SiC interface is not activated below 1200°C . On the other hand, wet oxidation turns out to result in the lowest mobility values around $60 \text{ cm}^2/\text{V.s}$ for all oxidation temperatures. Wet oxidation is known to cause extra negative oxide charges [173, 174] thus introduced in this study targeting at achieving a more positive threshold voltage by compensating some of the inherent positive charges at the 3C-SiC MOS interface. The mobility reduction can then be explained by more severe Coulomb scattering caused by these negative charges near the MOS interface. Unfortunately, even with the scarification of channel mobility, wet oxidation did not bring a positive threshold voltage. The film defect density still has the overwhelming dominant effect.

6.2.4 Nitridation time duration study

In last section, it was observed that at 1200°C the N_2O oxidation process is not activated, while above 1300°C more significant improvements on μ_{FE} are observed. Following that, the 3C-SiC MOSFET channel mobility improvements with increasing nitridation time

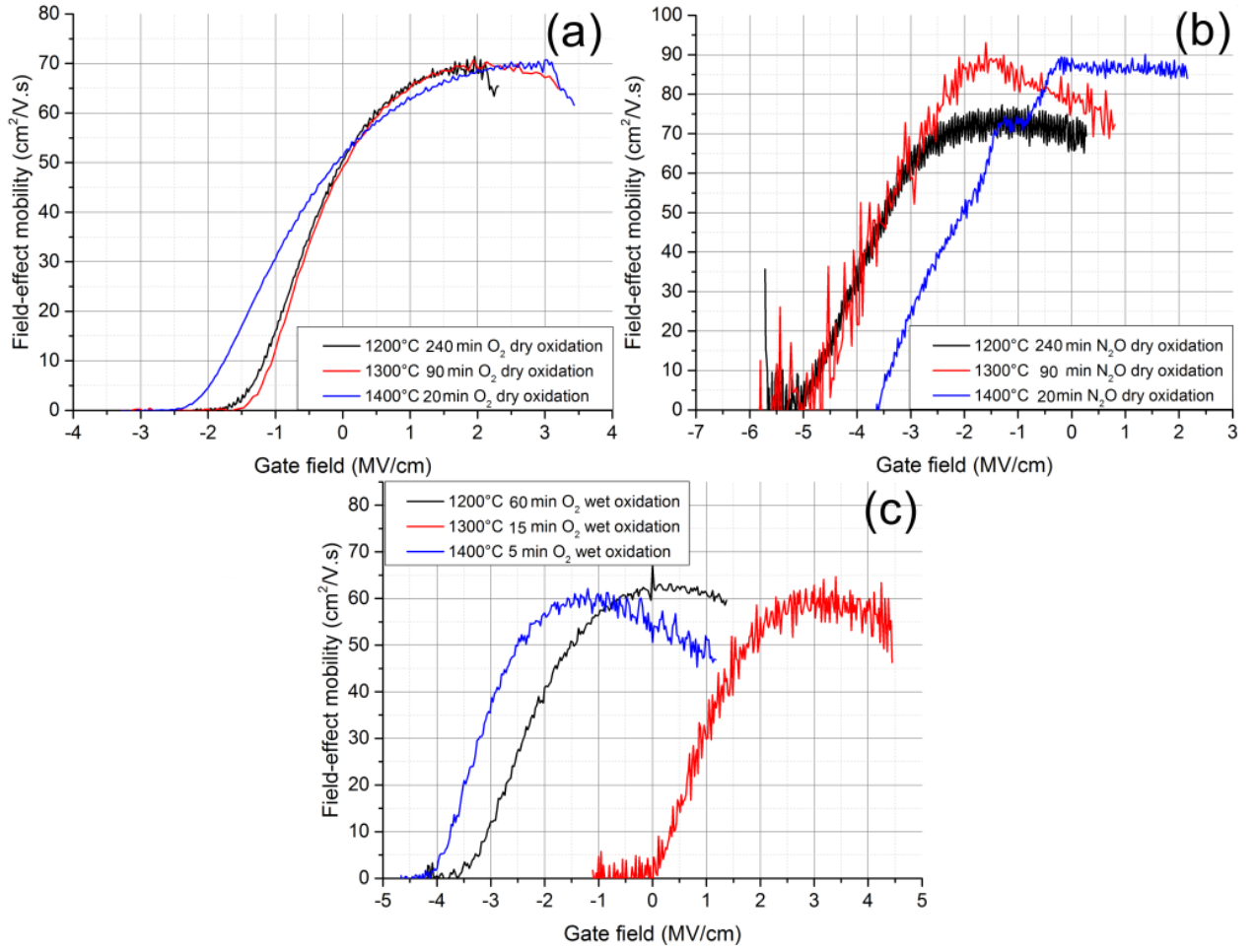


Figure 6.12: Field-effect mobility vs gate voltage curves of MOSFETs fabricated with different gate oxidation temperatures for (a) O₂ dry oxidation, (b) N₂O dry oxidation and (c) O₂ wet oxidation.

Table 6.3: Specific oxidation conditions for the 1300°C nitridation time durations study.

Sample	Oxidation process	Oxide thickness
1	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 60 mins	≈ 50 nm
2	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 120 mins	≈ 95 nm
3	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 180 mins	≈ 105 nm
4	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 240 mins	≈ 120 nm

durations at 1300°C is studied here. 4 samples were oxidised in N₂O atmosphere for 1 to 4 hours and the resultant oxide thickness are listed in Table 6.3 with the oxidation conditions specified as well. For the first 1 hour there is barely any improvement (Figure 6.13), the peak value is $\sim 70 \text{ cm}^2/\text{V.s}$, same as those O₂ dry oxidised ones in Figure 6.12(a). Another 1 hour N₂O oxidation led to a considerable rise of the peak value from ~ 70 to $\sim 90 \text{ cm}^2/\text{V.s}$. Even longer nitridation time durations of 3 hours and 4 hours, however, did not lead to further improvements. At 1300°C, The N₂O passivation effects on 3C-SiC/SiO₂ interface seem to start after 1 hour oxidation and saturate after 2 hours with a flow rate of 1 slm. In Section 5.1.6, it was mentioned that all passivation techniques are essentially thermal diffusion. The study here can be considered as the same, thus the saturation of passivation effects can be explained as a result of nitrogen failing to diffuse deeper into the 3C-SiC substrate.

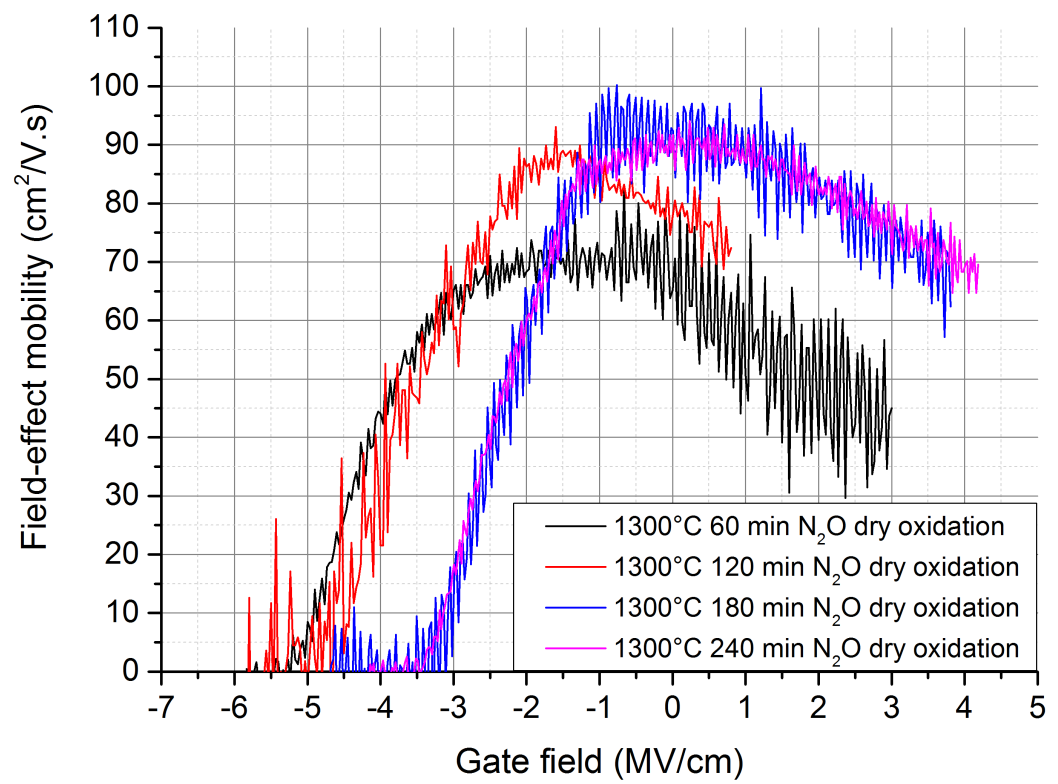


Figure 6.13: Field-effect mobility (μ_{FE}) of MOSFETs fabricated with different N_2O oxidation time durations (1, 2, 3 and 4 hours).

Table 6.4: Specific oxidation conditions for the direct oxidation and post-oxidation annealing comparison.

Sample	Oxidation process	Post-oxidation process	Oxide thickness
1	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 120 mins	None	≈ 98 nm
2	5 slm diluted dry O ₂ (O ₂ :Ar=1:4) at 1300°C for 30 mins	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 90 mins	≈ 56 nm
3	5 slm diluted wet O ₂ (O ₂ :Ar=1:4) at 1300°C for 20 mins	None	≈ 78 nm
4	5 slm diluted dry O ₂ (O ₂ :Ar=1:4) at 1300°C for 30 mins	5 slm diluted wet O ₂ (O ₂ :Ar=1:4) at 1300°C for 10 mins	≈ 61 nm
5	5 slm diluted wet O ₂ (O ₂ :Ar=1:4) at 1300°C for 10 mins	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 90 mins	≈ 68 nm
6	5 slm diluted N ₂ O (N ₂ O:Ar=1:4) at 1300°C for 90 mins	5 slm diluted wet O ₂ (O ₂ :Ar=1:4) at 1300°C for 10 mins	≈ 63 nm

6.2.5 Comparing direct oxidation and post-oxidation annealing

Until now, both nitridation and hydrogenation were performed by direct oxidation in N₂O or wet oxygen atmosphere. In this section, direct oxidation results are compared with samples fabricated by combined oxidation and POA process. The specific oxidation conditions are summarised in Table 6.4 and μ_{FE} curves plotted in Figure 6.14.

Figure 6.14a shows that there is only a small difference between the peak μ_{FE} values obtained from samples being directly oxidised or POA annealed in N₂O, all between 90 and 100 cm²/V.s. However, the sample that was dry oxidised in O₂ followed by N₂O POA has the least noisy curve (red in Figure 6.14a), similar to what was observed in Figure

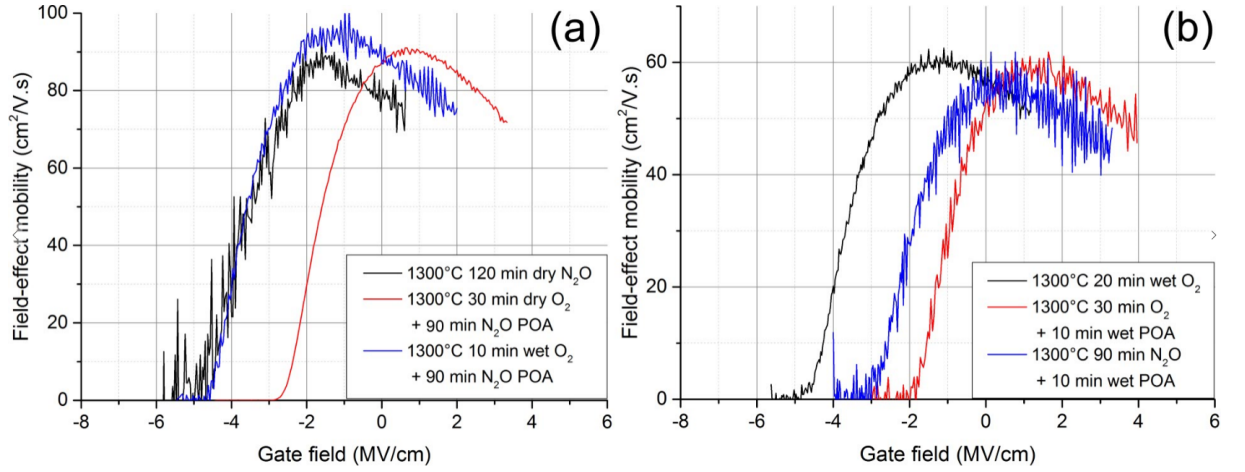


Figure 6.14: Field-effect mobility of MOSFETs fabricated with direct oxidation and combined oxidation-POA process for (a) N_2O process and (b) wet O_2 process.

6.12. This indicates that the more uniform MOS interface obtained by O_2 dry oxidation is preserved after the N_2O POA. In terms of the wet oxidised devices, both peak values and noise levels of μ_{FE} curves do not change much between samples. It can be said that, if nitridation or hydrogenation processes were used to fabricate the 3C-SiC MOS interface, the final conduction characteristic is determined by the last treatment.

6.2.6 The 3C-SiC/SiO₂ interface scattering mechanism

To look into the scattering mechanism at the fabricated 3C-SiC/SiO₂ interfaces, μ_{FE} vs V_{gs} curves were obtained at elevated measuring temperatures from 300 K to 500 K and plotted in Figure 6.15. It can be seen that all samples demonstrate a negative temperature coefficient for mobility values, which indicates that phonon scattering rather than Coulomb scattering is the dominant carrier transport mechanism at the fabricated

3C-SiC MOS interfaces [175]. It can also be noticed that the peak mobility value of the wet oxidised sample (Figure 6.15d) drops considerably slower than the other two. It suggests that although still dominated by phonon scattering, the wet oxidised 3C-SiC/SiO₂ interface has the highest Coulomb scattering among all. This also confirms that the low mobility value is a result of the extra negative charges introduced during the wet oxidation process.

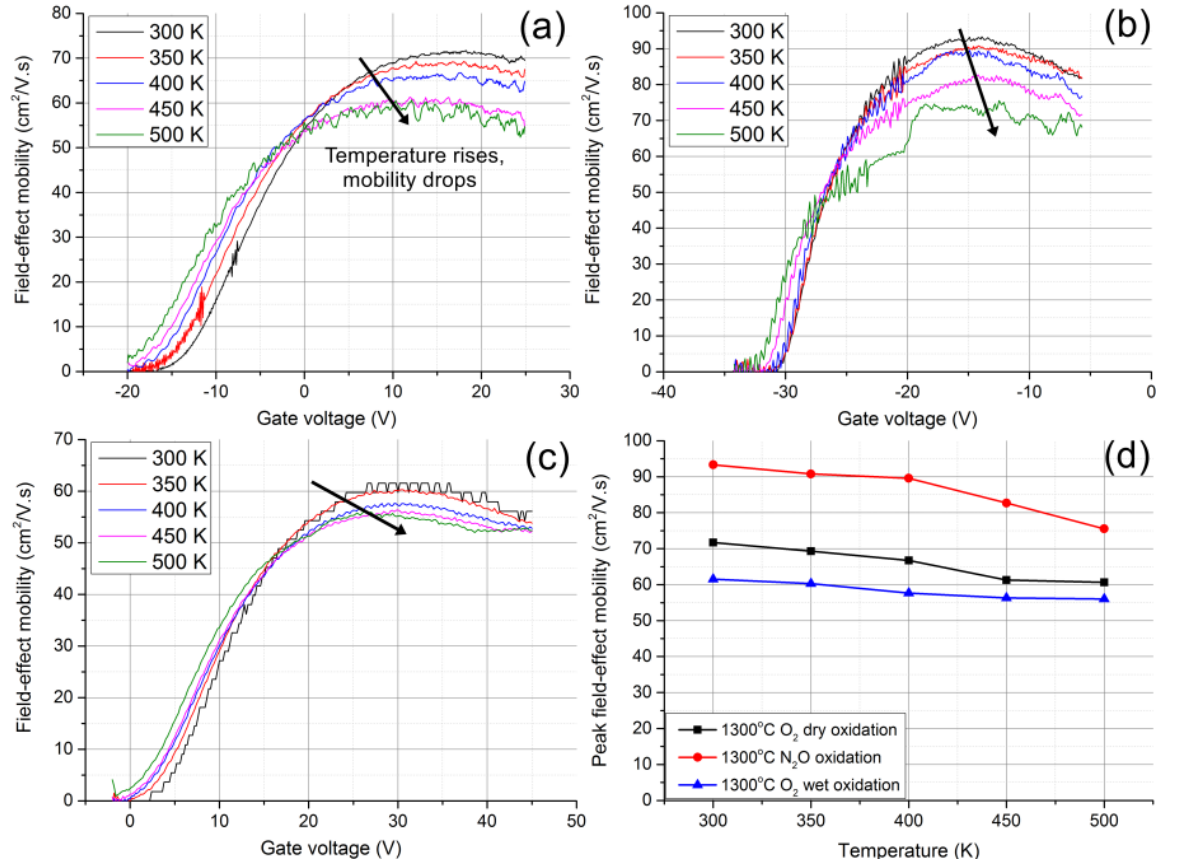


Figure 6.15: Field-effect mobility vs gate bias curves of MOSFETs fabricated by (a) 60 mins 1300°C O₂ dry oxidation, (b) 120 mins 1300°C N₂O dry oxidation, (c) 15 mins 1300°C O₂ wet oxidation at elevated measuring temperatures from 300 K to 500 K and (d) how the peak mobility of various devices changes with the measuring temperature.

6.2.7 Dielectric breakdown of gate oxides

In the end, the critical strength of fabricated oxides were characterised by applying a positive bias between gate and source ($V_{gs} > 0$). The drain was shorted to source during the measurements ($V_{ds} = 0$). The resultant I-V curves are demonstrated in Figure 6.16 for four conditions: O₂ dry oxidation, O₂ wet oxidation, N₂O dry oxidation and O₂ dry oxidation with N₂O POA, all 1300°C.

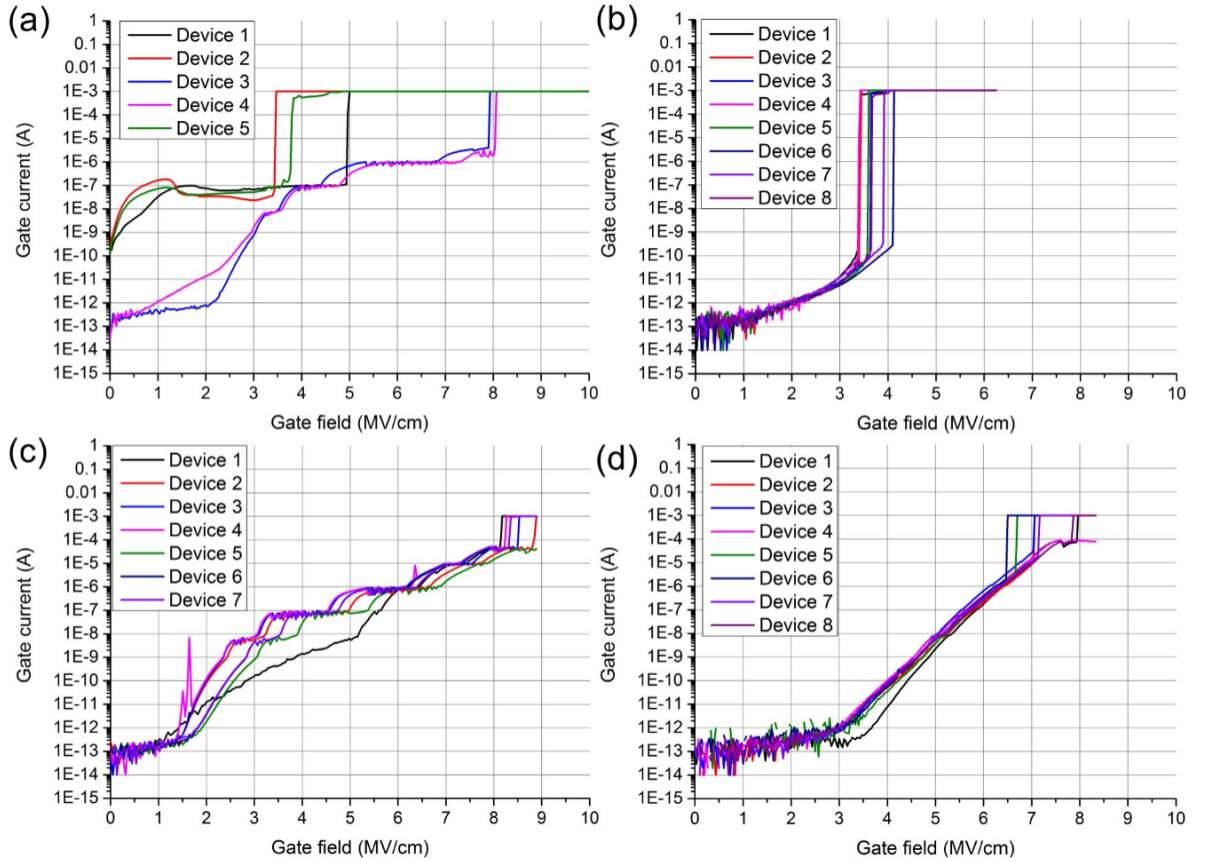


Figure 6.16: Dielectric breakdown curve of gate oxides fabricated by (a) 60 mins 1300°C O₂ dry oxidation, (b) 15 mins 1300°C O₂ wet oxidation, (c) 120 mins 1300°C N₂O dry oxidation and (d) 30 mins 1300°C O₂ dry oxidation + 90 mins 1300°C N₂O POA.

While some of the dry O_2 oxidised gate oxides demonstrate quite high critical strength close to 8 MV/cm, there are also some of them breaking down below 5 MV/cm as shown in Figure 6.16a. The number of working devices on a single chip is also lowest for the O_2 dry oxidised samples. Both of these suggest a wide spread of oxide quality, which may be caused by the randomly distributed defects in the gate oxides originated from the 3C-SiC epilayer. On the other hand, the wet O_2 oxidised devices demonstrate quite consistent critical strengths (Figure 6.16b), although all in a lower region between 3.5 to 4 MV/cm. The hydrogen ions in wet atmosphere may have helped to repair the oxide defects, whereas the extra negative charges were introduced at the same time, leading to overall degraded oxide reliability. N_2O direct oxidised samples have gate oxide critical field around 8.5 MV/cm (Figure 6.16c), higher than both previous samples. But the Fowler-Nordheim tunnelling regions of these curves are quite wide and noisy, which again, should be attributed to the less uniform surface potential at the nitride MOS interface. Using the combined dry O_2 gate oxidation with N_2O POA process, the noise level was greatly reduced and the leakage region was extended to around 3 MV/cm as seen in Figure 6.16d, at the same time the critical strength was able to be kept as around 8 MV/cm.

In short, it seems that dry O_2 gate oxidation with N_2O POA process produce a MOS interface with best conducting performance (lowest D_{it} , highest μ_{FE}) as well as the most reliable gate oxides, although the counter doping effect causes the negative shift of V_{th} . As such, it is used for the fabrication of LDMOSFET in the next section.

6.3 Fabricating 3C-SiC(001)/Si LDMOSFETs

The 3C-SiC/SiO₂ interface had been studied by fabricating both lateral MOS capacitors and long channel lateral MOSFETs. In this section, short channel LDMOSFETs are fabricated on 3C-SiC(001)/Si wafers using techniques developed in previous sections.

6.3.1 Experimental work

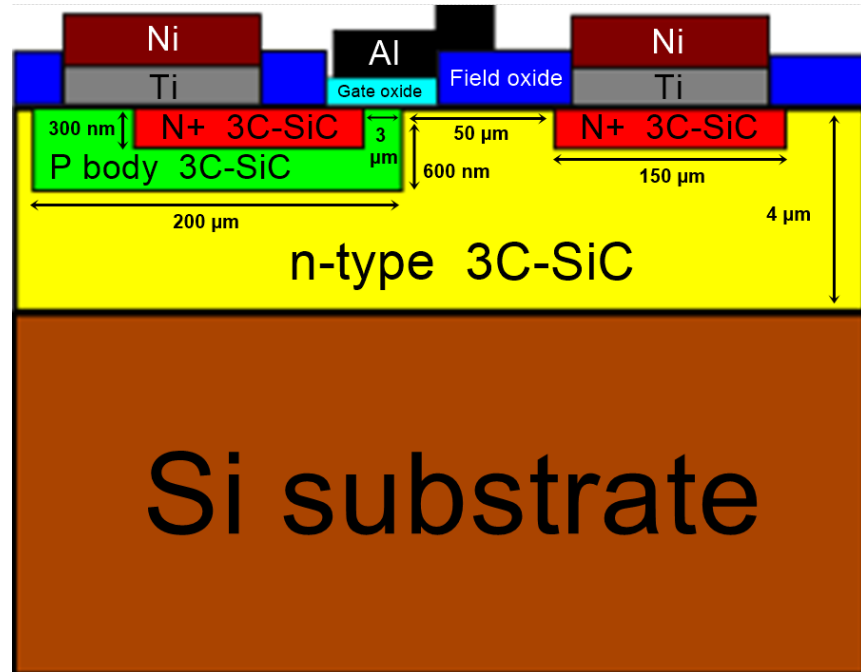


Figure 6.17: A schematic graph of the LDMOSFET structure.

LDMOSFETs were fabricated on the same 4 μm thick non-intentionally doped n-type 3C-SiC(001)/Si wafers as the long channel lateral MOSFETs. A schematic diagram of the LDMOSFET structure is shown in Figure 6.17 with key dimensions specified. Long

channel lateral MOSFETs in last section have shown that there is high leakage current conducting in the channel even in off-state. It is clear that these devices will not be able to meet the requirements of power switches applications, thus here the LDMOSFET design was not optimised for voltage blocking or switching. There is no P+ region side by side with the N+ source to prevent the latch-up, or a more highly doped P shielding layer beneath the P-body region for channel reach-through concerns. Only the forward conducting performance of the fabricated LDMOSFETs will be evaluated to demonstrate the potential advantage of 3C-SiC in making lower on-resistance power MOSFETs.

The same implantation/post implantation activation procedures as long channel lateral MOSFETs were applied to form P-body and N+ source/drain regions. Before gate oxidation, a 500 nm thick LPCVD SiO₂ layer was deposited on all samples to passivate the surface states. The gate oxide active area was then opened using photolithography and RIE etching just above the channel region. The channel length is determined as 3 μm to suit the clean processing limit, and the spacing between P-body and drain region is 50 μm . Source and drain Ohmic contacts were again formed by depositing Ti30nm/Ni100nm bilayer metal stack and performing a 1 minute RTA annealing at 1000°C. 500 nm Al was used as the gate contact. And after the patterning of all contacts, a 1 μm thick Al layer was deposited on top, extending them to a 500 $\mu\text{m} \times 500 \mu\text{m}$ pad for more convenient probe measurements. The mask design layout for a single chip (1.2 cm \times 1.2 cm) is shown in Figure 6.18 and an optical photo for the top view of one actual device is also provided in Figure 6.19 for reference. Both 1 mm and 4 mm long devices were fabricated to check

the material scaling ability.

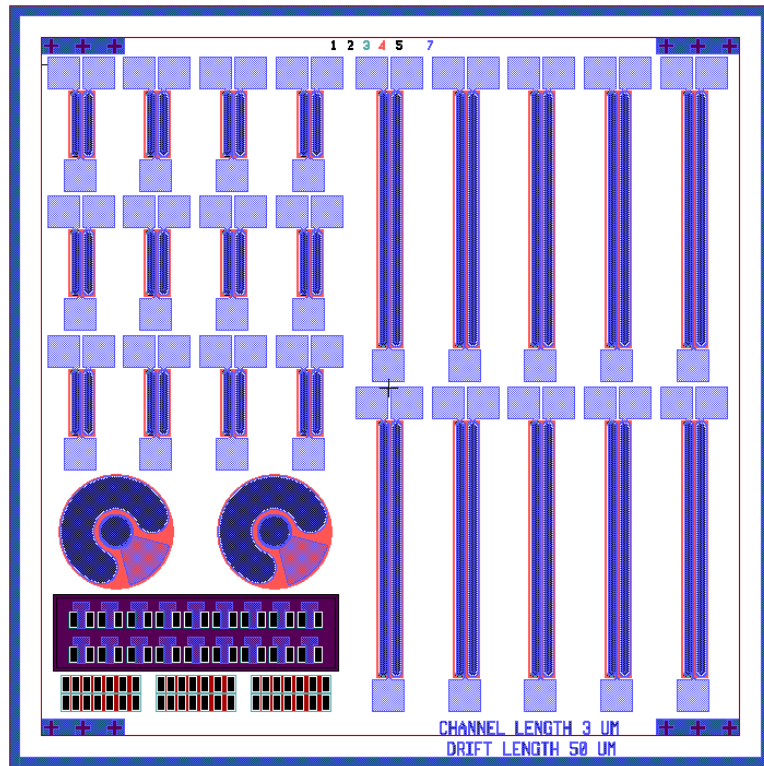


Figure 6.18: Mask design for a single chip (1.2 cm x 1.2 cm).

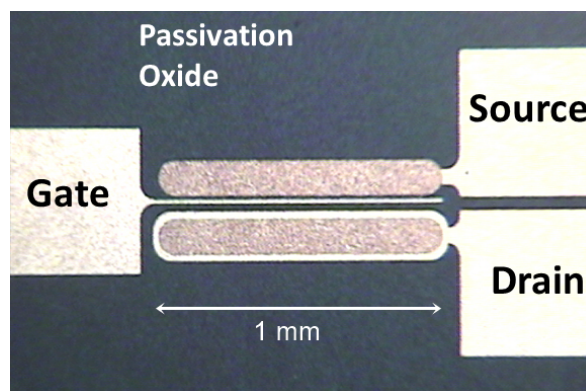


Figure 6.19: An optical photo of the 1 mm long LDMOSFET with gate, source and drain specified.

The gate oxide was thermally grown using the following recipe: 30 min O_2 (1 slm O_2 + 4 slm Ar) dry oxidation + 90 min N_2O (1 slm N_2O + 4 slm Ar) POA, all at 1300°C . For comparison, 4H-SiC devices with nitrated gate oxide and 3C-SiC(001)/Si devices with only dry O_2 oxidation were also fabricated as references. The 4H-SiC gate oxide was grown following a previously optimized N_2O passivation process: 1400°C dry oxidation 1 hour (1 slm O_2 + 4 slm Ar) + 1300°C N_2O 3 hours POA (1 slm N_2O + 4 slm Ar) [175]. For the 3C-SiC reference device, a 90 min O_2 dry oxidation at 1300°C with standard 30 mins Ar termination at the same temperature was applied.

6.3.2 LDMOSFET forward conducting performance

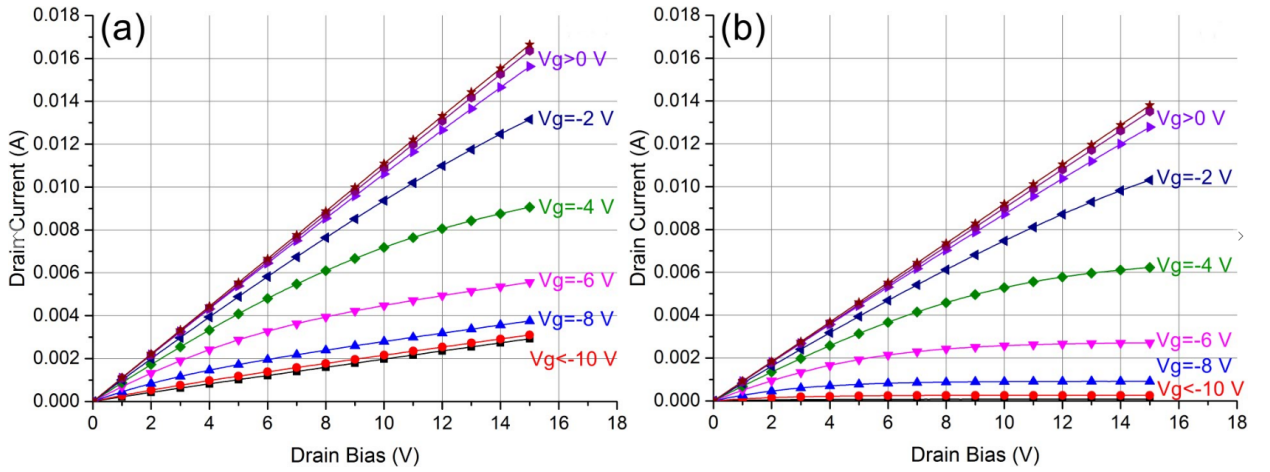


Figure 6.20: (a) Measured and (b) corrected forward IV characteristics of the reference 3C-SiC(001)/Si LDMOSFETs, with 90 min O_2 dry oxidation and 30 mins Ar termination at 1300°C .

The representative forward IV response of the reference 3C-SiC(001)/Si sample (with-

out gate nitridation) is shown in Figure 6.20a. The high leakage current in device off-state ($V_{gs} < -10$ V) still exists and varies from device to device, sample to sample. In order to properly compare between samples, the leakage current contribution is subtracted from the measured I_{ds} values and the resultant IV curve is as seen in Figure 6.20b with linear and saturation regions more distinguishable.

The same correction procedure is applied to other samples and the resultant I-V characteristics with gate effects are shown in Figure 6.21. It can be seen that the N₂O annealed device (Figure 6.21c) has 10% higher forward conduction current comparing with the reference 3C-SiC(001)/Si sample (Figure 6.21b). The drift region length used here is 50 μ m (Figure 6.17), which is a quite big value in a vertical equivalent structure. With such a long drift region, the device on-resistance should be dominated by the drift region so that 10% overall improvement by reducing channel resistance is actually quite remarkable. From the active area dimensions (0.406 mm x 1.05 mm for 1 mm long device and 0.406 mm x 4.05 mm for 4 mm long device), the current density of these devices can be estimated. The nitrided 3C-SiC(001)/Si LDMOSFETs have a forward current density around 1.37 A/cm² ($V_{ds}=5$ V, $V_{gs}=-5$ V), which is still far away from a power device value that is usually around 100 A/cm². Novel structure designs such as Reduced Surface Field (RESURF) technology may help to increase the device conducting performance, but only to certain extends. It seems that 3C-SiC power devices are only practical on free standing wafers with vertical structures.

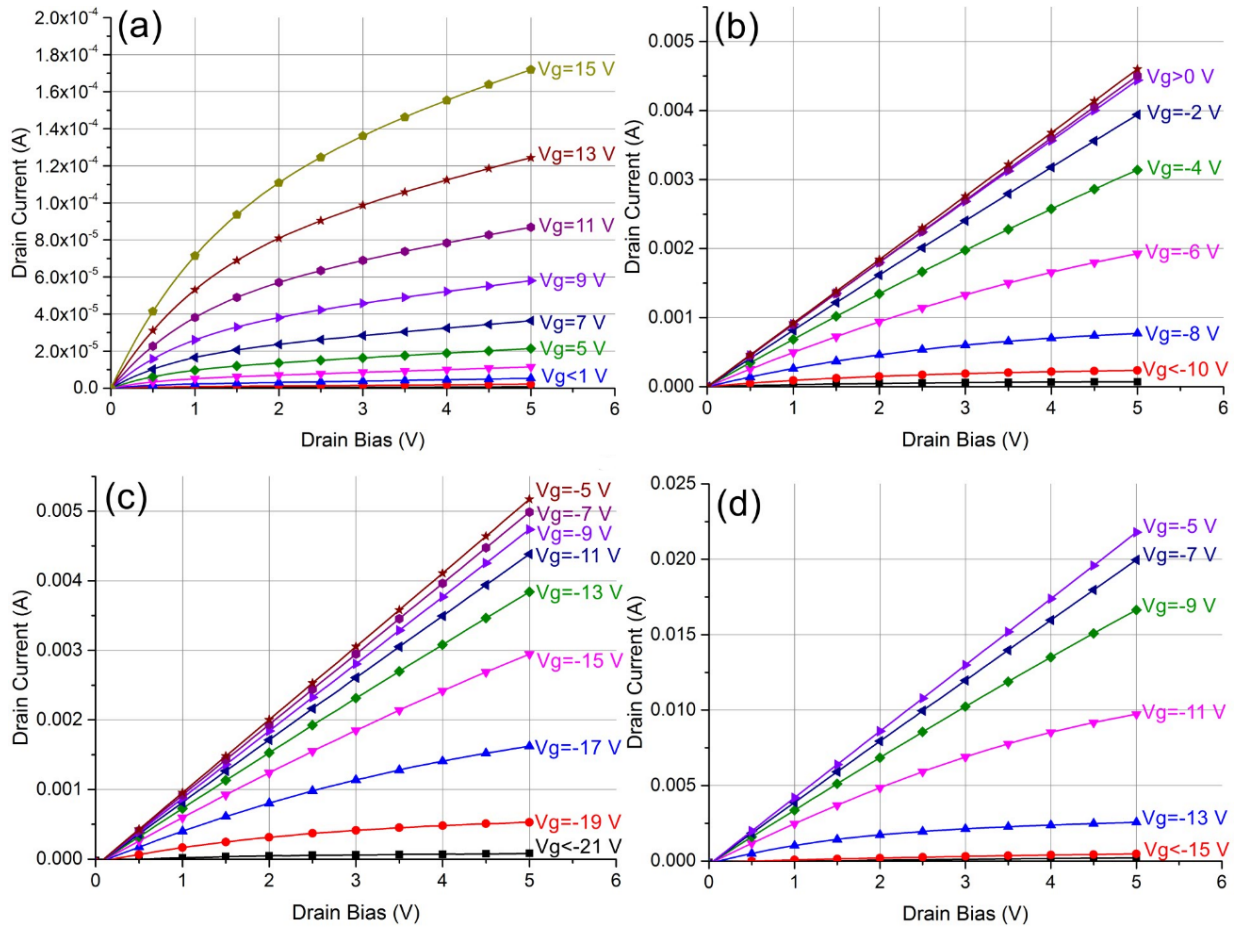


Figure 6.21: Corrected forward IV characteristics of (a) 1 mm wide reference 4H-SiC, (b) 1 mm wide reference 3C-SiC(001)/Si, (c) 1 mm wide nitrated 3C-SiC(001)/Si and (d) 4 mm wide nitrated 3C-SiC(001)/Si

6.4 Summary

In this chapter, the fabrication and characterisation of lateral MOSFETs on 3C-SiC(001)/Si wafers have been demonstrated. After a further study on the 3C-SiC/SiO₂ interface by fabricating long channel lateral MOSFETs and investigating various parameters, the gate oxidation recipe is optimised as a combined 30 mins O₂ dry oxidation followed by a 90 mins N₂O POA, both at 1300°C, which yields the best conducting performance ($\mu_{FE} \approx 90$ cm²/V.s) as well as highest SiO₂ critical strength (≈ 8 MV/cm). However, the device is normally on due to the inherent positive charges at the 3C-SiC/SiO₂ interface and the N counter doping in the channel region. This process is then applied to fabricate LD-MOSFET, which has more than 10 times lower on-resistance compared with an identical 4H-SiC devices processed in parallel. The devices demonstrate quite good scaling ability that conducting current increases almost linearly with the active area. However, the 3C-SiC(001)/Si LDMOSFET overall current density is only around 1.37 A/cm², still too low for power switching applications. Also, high leakage current is observed for all devices in off-state, indicating an inadequate material quality for blocking mode operation. Nevertheless, the efforts put into this work can always be applied in the future, when the device grade 3C-SiC material eventually becomes available.

In last chapter it has been shown that the current density of 3C-SiC/Si LDMOSFET is very limited, even though high channel mobility values approaching $90 \text{ cm}^2/\text{V.s}$ were achieved. Vertical devices fabricated on free standing 3C-SiC wafers seem to be inevitable for high current applications. On the other hand, there are high-voltage yet low-current applications such as smart power devices or power ICs [176]. The idea of smart power devices is to fabricate one chip containing both power devices and respective control circuits to reduce costs, which apparently favours a lateral structure. 3C-SiC on Si can be a good choice for these devices, which will benefit from the superior electrical performance of WBG semiconductors with a reasonable cost.

This chapter demonstrates a novel 3C-SiC/Si lateral Schottky diode design targeting high blocking voltage beyond 1200 V. The physical models used in the modelling process will be firstly introduced, after which the benchmark is validated using literature results.

Then the design and modelling of a 3C-SiC on Si novel power device are conducted using the validated benchmark physical model. Although modelling was based on a Schottky diode structure, the knowledge shall be able to be well transferred to other unipolar devices such as a MOSFET.

7.1 Benchmark Model and Basic Design

All modelling investigations below were carried out using the finite element device simulator Silvaco. The operation temperature is fixed as 300 K and the relevant material parameters are listed in Table 7.1.

7.1.1 Physical models

One of the first requirements of designing power devices is to estimate the avalanche breakdown voltage of the bulk semiconductor for a given impurity concentration and thickness. Unlike Si or 4H-SiC, whose models have been studied in depth and correspondingly improved, the models for 3C-SiC are quite lowly developed. As such, research

Table 7.1: Relevant material parameters used in the modelling process [177].

Semiconductor	3C-SiC	Si
Dielectric Constant	9.72	11.8
Band Gap (eV)	2.2	1.08
Electron Affinity (eV)	3.8	4.17
Intrinsic Carrier Concentration (cm³)	1.1	1.45×10^{10}
Bulk Electron Mobility (cm²V⁻¹s⁻¹)	1000	1000
Bulk Hole Mobility (cm²/V.s)	50	500

Table 7.2: Parameters for 3C-SiC impact ionisation and mobility models [179, 180].

	A (cm⁻¹)	B (MV/cm)	μ_0 (cm²/V.s)	β	
Electron	1.28×10^6	5.54	1000	4.38×10^7	1.48
Hole	1.07×10^7	11.2	50	1×10^7	1

into the physical models for 3C-SiC device modelling is still required. The key parameters to calculate the critical electric field of a semiconductor are electron and hole impact ionization coefficients (α_n and α_p). Ignoring the temperature dependence, $\alpha_{n,p}$ can be given by Shockley's model [178] as below:

$$\alpha_{n,p} = A_{n,p} e^{-\frac{B_{n,p}}{E}} \quad (7.1)$$

where E is the local electric field and $A_{n,p}$, $B_{n,p}$ are material constants. In case of 3C-SiC, experimental data of $A_{n,p}$ and $B_{n,p}$ are not available. The values used in this work (see Table 7.2) were adopted from [179], where Monte Carlo simulations were used to study the carrier transport mechanisms in bulk 3C-SiC. In the following, breakdown voltage is defined as where the leakage current goes up by 100%.

Due to the fact that bulk electron mobility of a semiconductor does not change significantly in the low doping range, a concentration-independent mobility model was applied. In the low field condition (forward bias), bulk electron and hole mobility values (μ_{n0} and μ_{p0}) were assumed to be constant. However, in the case of high electric field, where the carrier velocity will saturate, the field-dependent Caughey-Thomas model [181] as below

was applied:

$$\mu_{n,p} = \frac{\mu_{n0,p0}}{\left[1 + \left(\frac{\mu_{n0,p0}E}{V_{satn,p}}\right)^{\beta_{n,p}}\right]^{\frac{1}{\beta_{n,p}}}} \quad (7.2)$$

where $\mu_{n0,p0}$ are electron and hole mobility values in low field condition, $V_{satn,p}$ are electron and hole saturation velocities, $\beta_{satn,p}$ are material constants and E is the local electric field. Due to the lack of experimental $\beta_{satn,p}$ data, fitting results of MC studies [180] were used to model the electron mobility. For holes, the default values provided in the Silvaco ATLAS software package were applied. Since here we are studying an unipolar device, this will have a negligible influence on the simulation result.

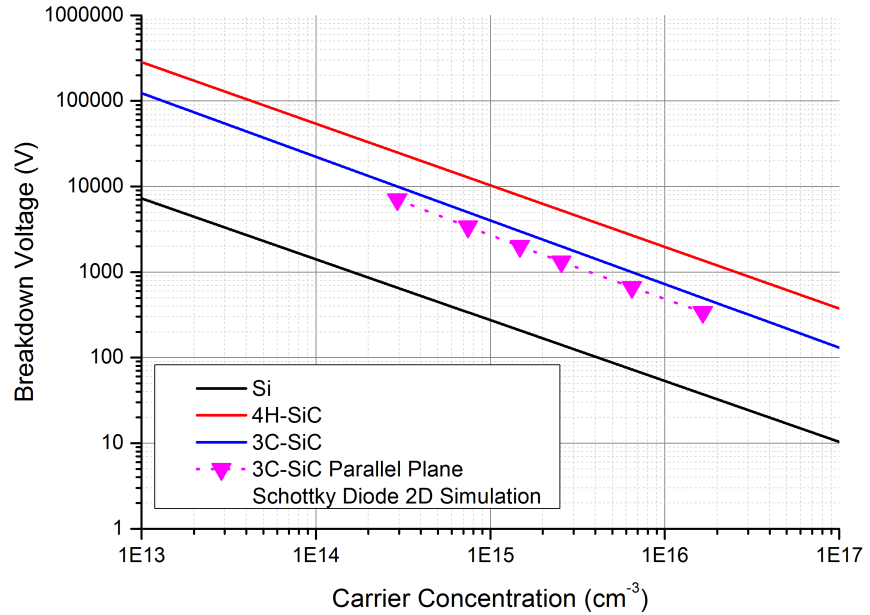


Figure 7.1: Semiconductor breakdown voltage as a function of the impurity concentration (Literatures [182] and simulation results here).

The simulated breakdown voltages for various free carrier concentrations are plotted in Figure 7.1 as triangular marks. Simulations were based on a parallel-plane vertical Schottky diode structure. The resulting relationship between blocking voltage (V_{br}) and impurity concentration (N_d) can be fitted by an analytical expression as below:

$$V_{br} = 5.16 \times 10^{14} N_d^{-0.752} \quad (7.3)$$

Literature results for 3C-SiC, Si as well 4H-SiC [182] have also been included in Figure 7.1 (solid lines) for comparison purpose. According to Equation 7.3, for 600 V blocking voltage, the 3C-SiC impurity concentration should be around $7.4 \times 10^{15} \text{ cm}^{-3}$, which is however $1.3 \times 10^{16} \text{ cm}^{-3}$ according to [182]. In previous work, a 600 V vertical 3C-SiC MOSFET was fabricated on free standing 3C-SiC wafers with low planar defects density using a $5 \times 10^{15} \text{ cm}^{-3}$ doped epilayer [183], and more recently $7 \times 10^{15} \text{ cm}^{-3}$ [162], which is in better agreement with results in this work.

7.1.2 Device structure design

The 2D structure view of the proposed 3C-SiC on Si lateral structure is shown in Figure 7.2. The lightly doped n-type 3C-SiC epilayer on a $500 \text{ } \mu\text{m}$ (assuming a common commercial 4-inch Si wafer) p-type Si substrate was used as the voltage blocking drift region. 3C-SiC epilayer surface was selectively highly doped ($1 \times 10^{19} \text{ cm}^{-3}$) for ohmic contact formation. The deposited field oxide (SiO_2) layer on the epilayer surface was not only

aimed at minimising the surface recombination effects, but also will act as an insulation layer for the field plate feature. Windows were opened in the field oxide layer for Ohmic (cathode) and Schottky (anode) contacts metallisation. Nickel was used to form both contacts, and a Schottky barrier height of 0.95 eV was assumed for the Schottky contact. Both anode and cathode metallisation extended over the field oxide layer, acting as field plates to reduce electric field crowding at contact corners in reverse bias, protecting the device from early breakdown [184]. In lateral structures particularly, the field plate provides extra benefits that higher blocking voltage than the usual “parallel plane” limit can be achieved, which is similar to the super-junction designs for vertical devices. The Si substrate for the 3C-SiC on Si diode was p-type doped to enable the RESURF effect. As a comparison, a free standing 3C-SiC lateral diode with identical feature dimensions was also modelled as shown in Figure 7.3. Field plate for the free standing diode was only applied at the anode, since without the RESURF feature, there will be no electric field crowding around the cathode corner as will be shown later.

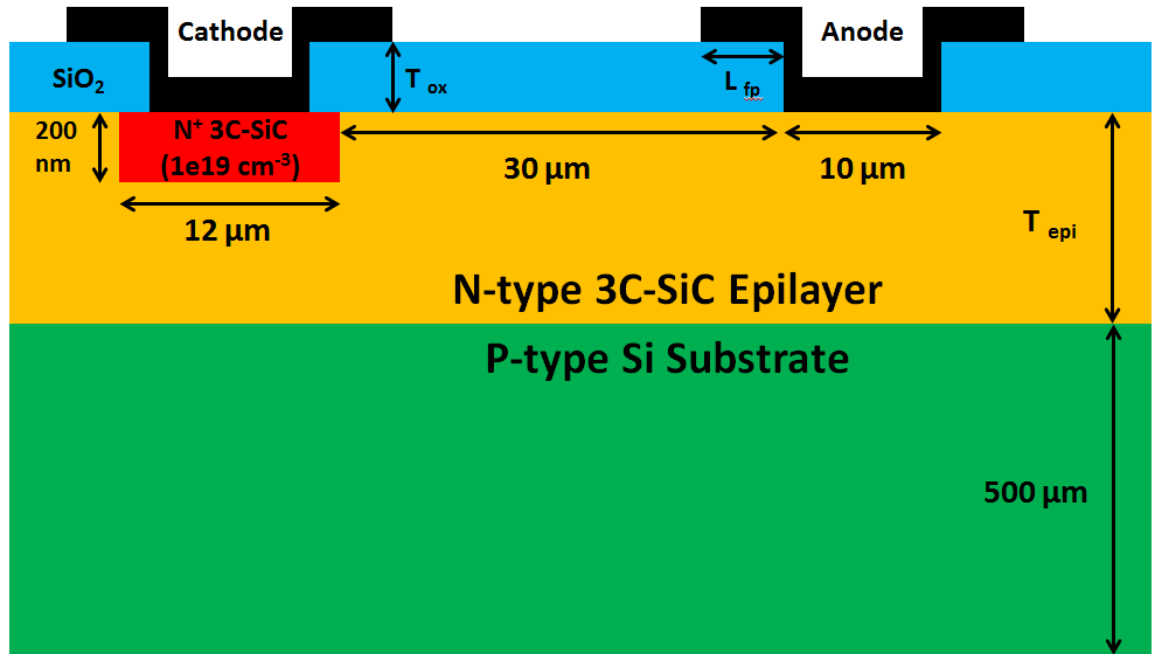


Figure 7.2: 2D schematic structure of the designed 3C-SiC/Si lateral RESURF diode (dimensions not to scale).

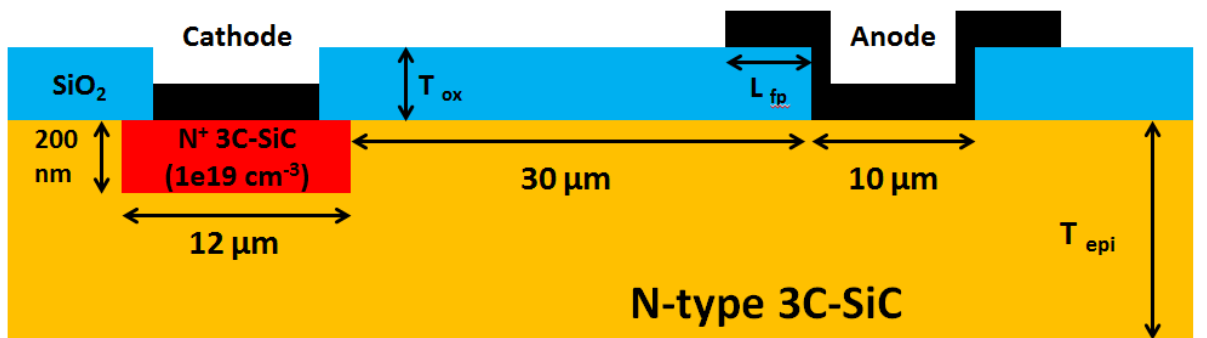


Figure 7.3: 2D schematic structure of the comparing purpose free standing 3C-SiC lateral diode (dimensions not to scale).

7.2 Simulation Results and Discussions

7.2.1 Free standing 3C-SiC lateral diode

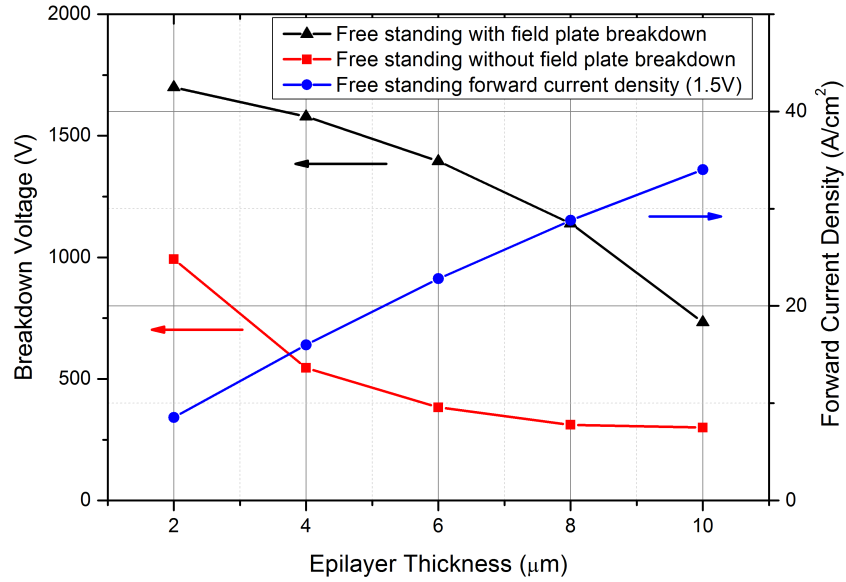


Figure 7.4: Reverse breakdown voltage and forward current density (under 1.5 V bias) of free standing 3C-SiC lateral diodes with and without field plate.

Free standing 3C-SiC lateral diodes without field plate terminations were modelled as a reference. First of all, the effect of 3C-SiC epilayer thickness was studied. Epilayers of fixed n-type doping ($3 \times 10^{15} \text{ cm}^{-3}$) with thickness ranging from 2 to 10 μm were looked into. It turned out that in contrary to a vertical design where thicker epilayers are required for higher voltages; lateral diodes with a thicker epilayer yielded lower blocking voltage as seen in Figure 7.4 (red line). Figure 7.5 demonstrates that in both 2 μm and 10 μm epilayer conditions the device reaches the 3C-SiC critical field ($\approx 2 \text{ MV}/\text{cm}$), but the depletion region in the 2 μm case is more uniform and closer to the ideal parallel-plane

condition, thus less prone to early breakdown. With the epilayer thickness decreasing to $2\text{ }\mu\text{m}$, the blocking voltage 992 V is approaching the 1185 V limit ($N = 3 \times 10^{15}\text{ cm}^{-3}$ in Equation 7.3). The device forward current density (Figure 7.4 blue line) increases rapidly with increasing epilayer thickness because of a larger conduction area. Now the higher forward current demand conflicts with higher reverse blocking ability, which can be solved by adding the field plate feature into the design.

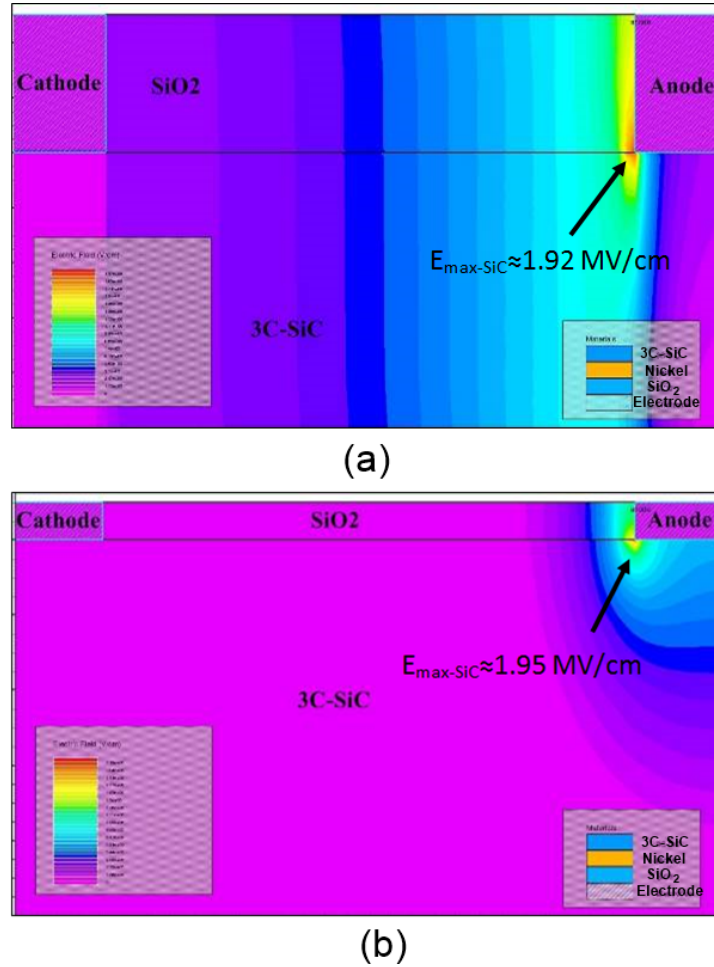


Figure 7.5: Electric field contour plot of 3C-SiC lateral diodes without field plates fabricated on free standing (a) $2\text{ }\mu\text{m}$ and (b) $10\text{ }\mu\text{m}$ epilayers at breakdown point.

Field plate terminations proved to be effective in protecting contact corners from electric field crowding [185, 186] as shown in Figure 7.6. In this lateral design, it also modifies the epilayer depletion in reverse biased condition. The electric field at the 3C-SiC surface with and without field plates are plotted in Figure 7.7. As can be seen, the field plate edge expands the depletion region further away from the anode contact edge, greatly increasing the area under the curve, which represents the blocking voltage. With this improvement, the device blocking ability is no longer limited by the parallel-plan model (Equation 7.3) while its forward performance is also not compromised.

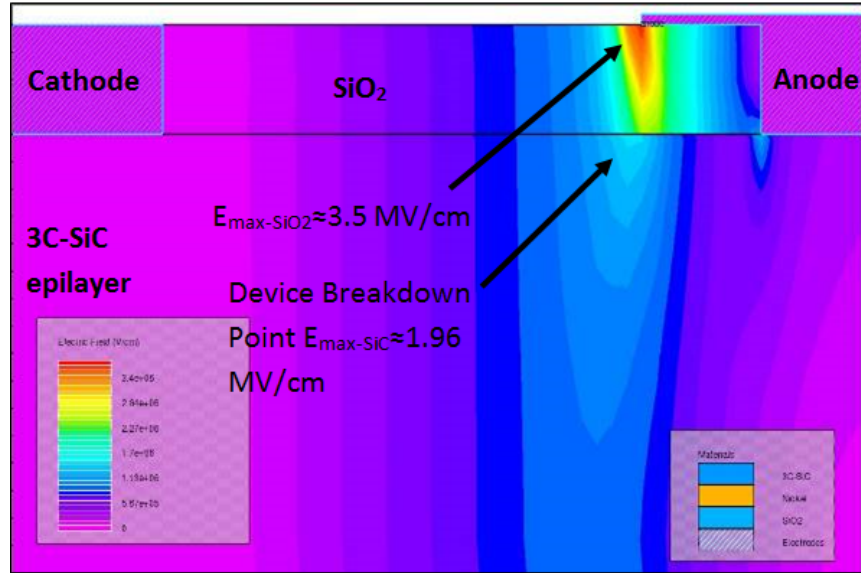


Figure 7.6: Electric field contour of free standing 3C-SiC lateral diode at breakdown point with anode field plate ($N_d = 3 \times 10^{15} \text{ cm}^{-3}$, $T_{ep} = 4 \text{ } \mu\text{m}$, $T_{ox} = 1 \text{ } \mu\text{m}$ and $L_{fp} = 6 \text{ } \mu\text{m}$).

To optimize the field plate design, influences of the SiO_2 thickness and field plate length were studied. Figure 7.8 shows that the highest blocking voltage is obtained with

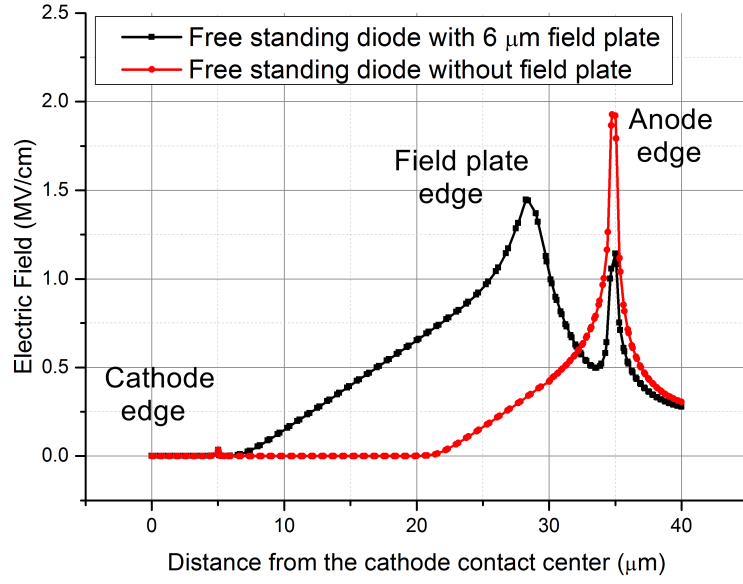


Figure 7.7: Surface field plot of free standing 3C-SiC lateral diode at breakdown point with and without an anode field plate ($N_d = 3 \times 10^{15} \text{ cm}^{-3}$, $T_{ep} = 4 \text{ μm}$, $T_{ox} = 1 \text{ μm}$ and $L_{fp} = 6 \text{ μm}$).

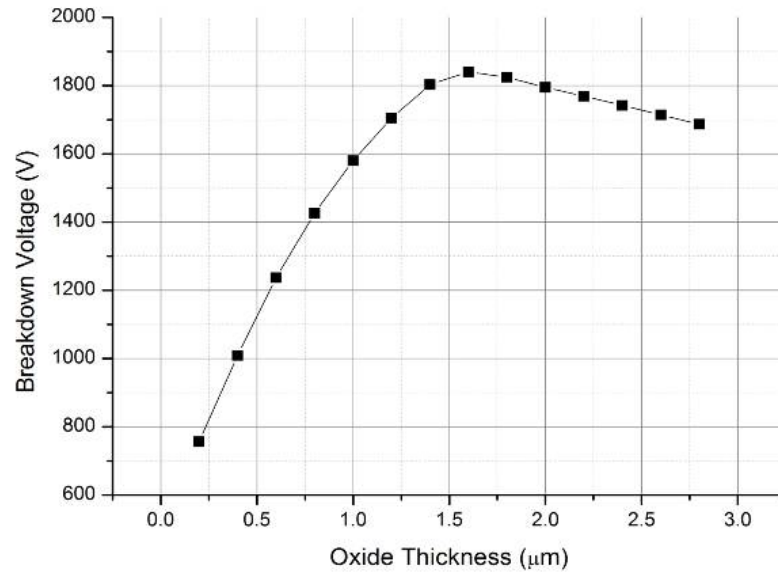


Figure 7.8: Oxide thickness effects on the breakdown voltage of free standing lateral device with field plate.

a 1.6 μm thick SiO_2 layer. Considering the difficulty in fabricating field plates on such thick layer, a lower value (1 μm) was chosen, which is still thick enough to prevent itself from breaking down before 3C-SiC (Figure 7.6). The breakdown voltage increases with field plate length and saturates at 4 μm as seen in Figure 7.9. The free standing lateral diode with parameters specified in Figure 7.6 and 7.7 demonstrates a breakdown voltage of 1580 V and the forward current density is 16 A/cm² at a anode bias of 1.5V.

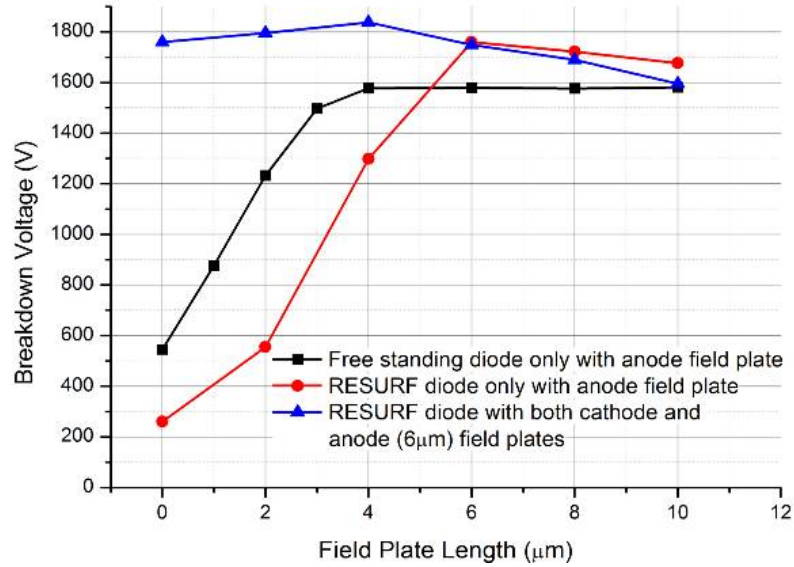


Figure 7.9: Field plate length effects on device breakdown voltage of lateral free standing and RESURF diodes.

7.2.2 3C-SiC on Si lateral RESURF diode

To directly compare with the reference free standing diode, the RESURF diode was formed by simply adding an extra 500 μm p-type Si substrate (see Figure 7.2). The substrate was shorted with the anode to prevent its potential from floating. The influence of the

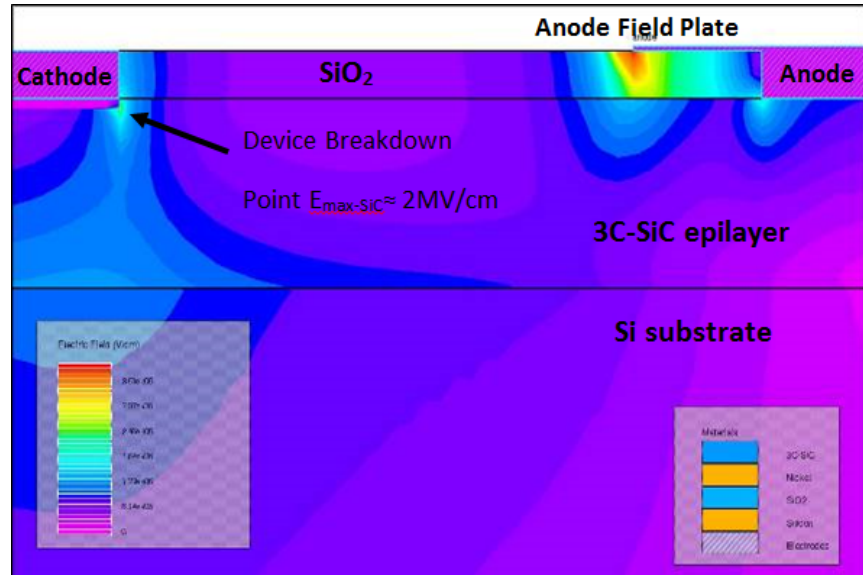


Figure 7.10: RESURF diode electric field contour at breakdown point with field plate for anode only.

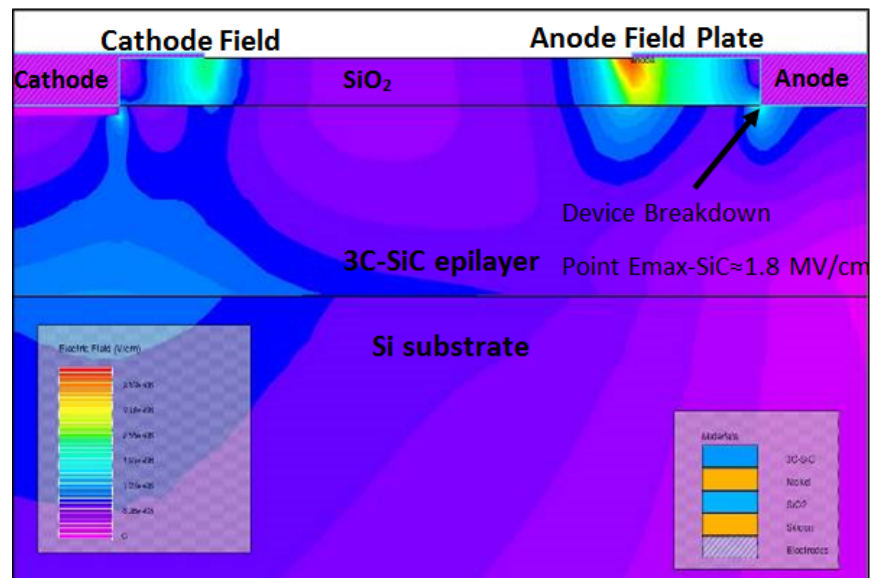


Figure 7.11: RESURF diode electric field contour at breakdown point with field plate for both anode and cathode.

anode field plate length is again illustrated in Figure 7.9. With the same epilayer ($4\ \mu\text{m}$) and oxide thickness ($1\ \mu\text{m}$), now device breakdown voltage saturates after field plate length reaches $6\ \mu\text{m}$ instead of $4\ \mu\text{m}$. This change comes from the extra depletion region formed under the cathode as seen in Figure 7.10, which is induced by the reverse biased PN junction between the cathode and the substrate. Consequently field plate was added to protect the cathode corner from field crowding as shown in Figure 7.11. Although the electric field at the corner is effectively reduced (see Figure 7.12), the device breakdown voltage is not greatly influenced by the cathode field plate length, and it reaches the peak value when cathode field plate is $4\ \mu\text{m}$ long, as shown by the blue line in Figure 7.9. Due to the vertical depletion under the cathode, the diode reverse blocking ability is limited by the $4\ \mu\text{m}$ epilayer thickness. With the same impurity concentration ($3 \times 10^{15}\ \text{cm}^{-3}$) for the drift region as the free standing diode and p-type Si substrate $1 \times 10^{15}\ \text{cm}^{-3}$ doped, the RESURF diode achieves maximum only 800 V, even with the help of both anode and field plates. However, for a RESURF device design, the optimum doping level for the drift region is not necessarily the lowest one.

7.2.3 Optimisation of the n-type 3C-SiC epilayer doping for the 3C-SiC/Si RESURF diode

To find out the optimum charge for the epilayer, the p-type Si substrate doping is fixed as $1 \times 10^{15}\ \text{cm}^{-3}$, and breakdown simulations were carried out for the devices with various

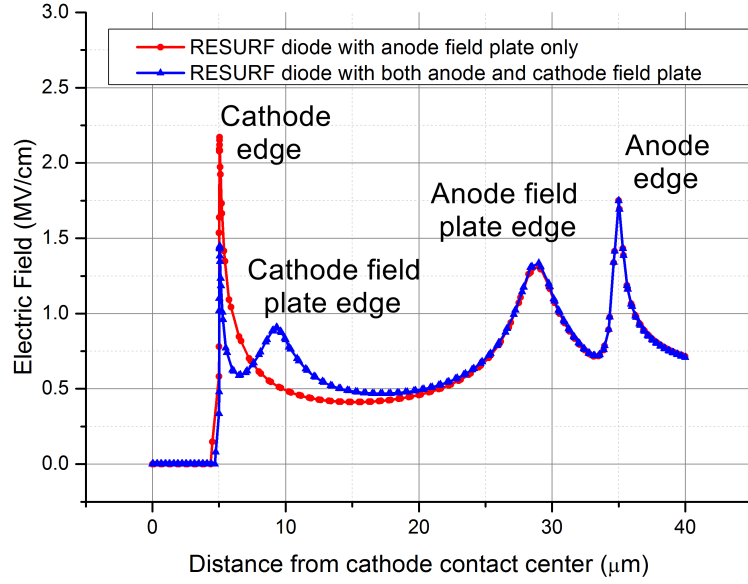


Figure 7.12: Surface electric field plot of the RESURF diodes at breakdown point with anode field plate only and with both anode & cathode field plates.

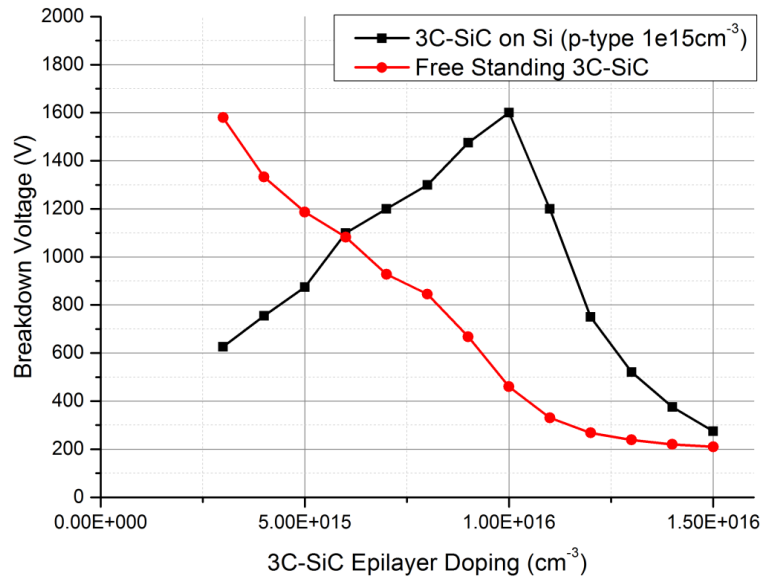


Figure 7.13: 3C-SiC epilayer doping influences on breakdown voltages of free standing & RESURF diodes (both $4\ \mu$ epilayer).

3C-SiC epilayer doping levels. In all cases, epilayer thickness was $4\ \mu\text{m}$ and field plates were applied to both anode ($4\ \mu\text{m}$) and cathode ($6\ \mu\text{m}$). As seen in Figure 7.13, the breakdown voltage increases gradually with the epilayer doping at first but once reaching the peak point, drops rapidly. This suggests that a lower doping than the optimum value should be used in actual fabrication because of the difficulty in controlling epilayer doping during the growth process. The optimum doping for the RESURF diode in this condition is found to be around $1 \times 10^{16}\ \text{cm}^{-3}$, where the device breakdown voltage reaches 1600 V. The 1200 V target can be achieved within the window between $7 \times 10^{15}\ \text{cm}^{-3}$ and $1.1 \times 10^{16}\ \text{cm}^{-3}$.

For comparison purposes, the reverse blocking performance for a $4\ \mu\text{m}$ thick epilayer free standing diode with the same doping range was also investigated and the results are plotted against the RESURF device in Figure 7.13. It is found that in the 1200-1700 V range, the RESURF diode allows for a relative more highly doped ($0.7 - 1.1 \times 10^{16}\ \text{cm}^{-3}$) epilayer compared with free standing diode ($< 5 \times 10^{15}\ \text{cm}^{-3}$). Higher doping level in the epilayer means less resistive devices. The leakage current density of the RESURF diodes remains below $1\ \text{mA}/\text{cm}^2$ as seen in Figure 7.14, much higher than the free standing device ($< 10\ \text{nA}/\text{cm}^2$ in all cases) due to the strained 3C-SiC/Si hetero-junction (see Figure 7.10) in reverse bias. Also, it can be seen that the higher epilayer doping leads to a more abrupt breakdown curve, which confirms the high leakage current is due to the depletion in the 3C-SiC epilayer.

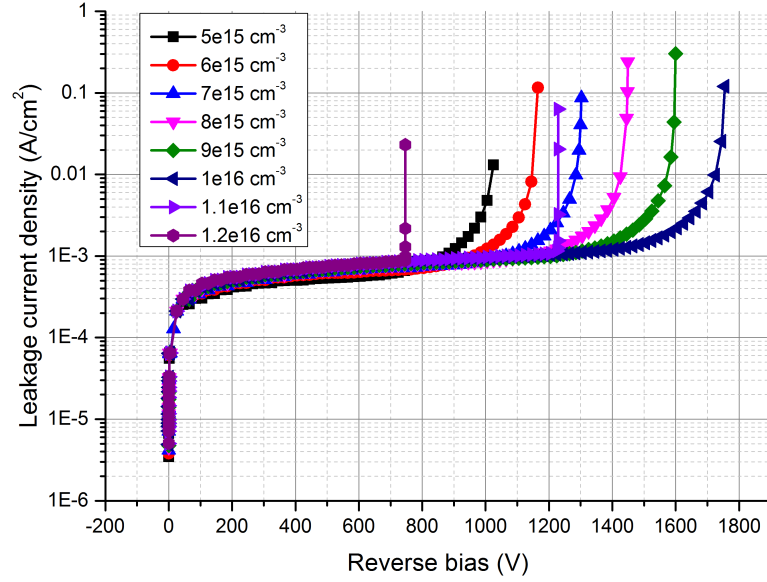


Figure 7.14: 3C-SiC epilayer doping influences on reverse current density-voltage (J-V) performance of RESURF diodes.

7.2.4 Optimisation of the p-type Si substrate doping for the 3C-SiC/Si RESURF diode

The Si substrate doping influences the device performance in a way that it hardly changes the peak breakdown voltage magnitude but shifts the optimum epilayer doping. Still 4 μm 3C-SiC epilayer, the $1 \times 10^{15} \text{ cm}^{-3}$ doped substrate (red line) shifts the peak voltage position to a higher drift region doping compared with the $5 \times 10^{14} \text{ cm}^{-3}$ (black line) as seen in Figure 7.15, which means lower resistance device. Further increasing the substrate doping to $5 \times 10^{15} \text{ cm}^{-3}$ (blue line) results in a dramatic drop of the device breakdown voltage, although the peak position again shifts to the higher drift doping region. This is due to the fact that when the substrate doping is high, in reverse bias the depletion at

the substrate/epilayer PN junction goes more into the epilayer, and if the epilayer is not thick enough to prevent the punch through, the early breakdown happens.

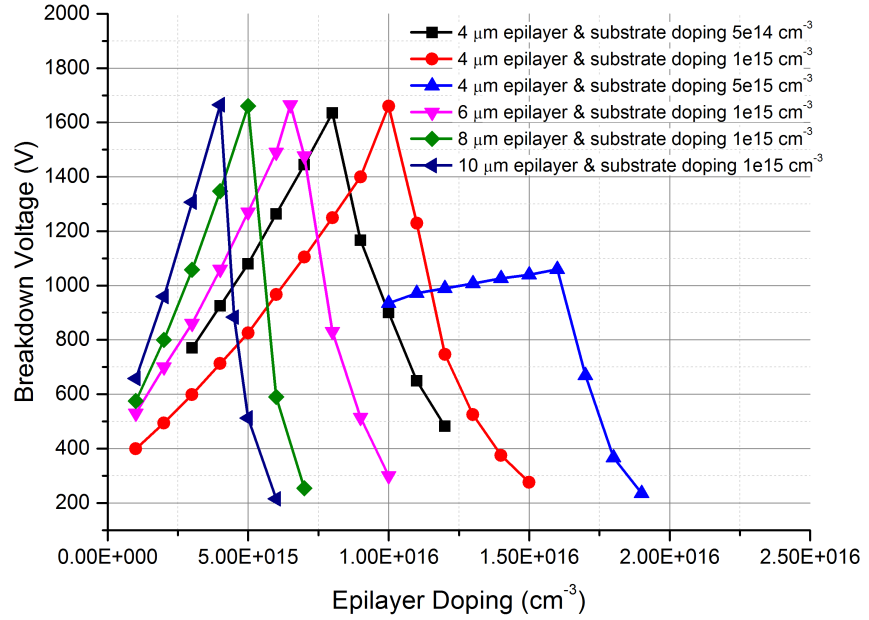


Figure 7.15: RESURF diodes breakdown voltage for various substrate doping and epilayer thickness values.

Figure 7.16 proves that increasing the epilayer thickness to 15 μm brings the peak value back to near 1600 V, but also shifts the peak to a lower epilayer doping position, namely higher device resistance, even considering the increased conduction area due to thicker epilayer. On the other hand, when the epilayer is thick enough to prevent the punch through from taking place, making it even thicker will not simply result in higher blocking voltage. As seen in Figure 7.15, with $1 \times 10^{15} \text{ cm}^{-3}$ doped Si substrate, increasing the epilayer thickness from 4 μm (red) to 10 μm (dark blue) has a minimal impact on the peak breakdown voltage, but it greatly reduces the optimum drift region doping value.

Thus, a thicker epilayer in this RESURF diode design is not beneficial for achieving better performance. When the epilayer thickness and doping levels are determined, a small variation ($\pm 20\%$) in the substrate doping does not have a great influence on the final device blocking performance as seen in Figure 7.17.

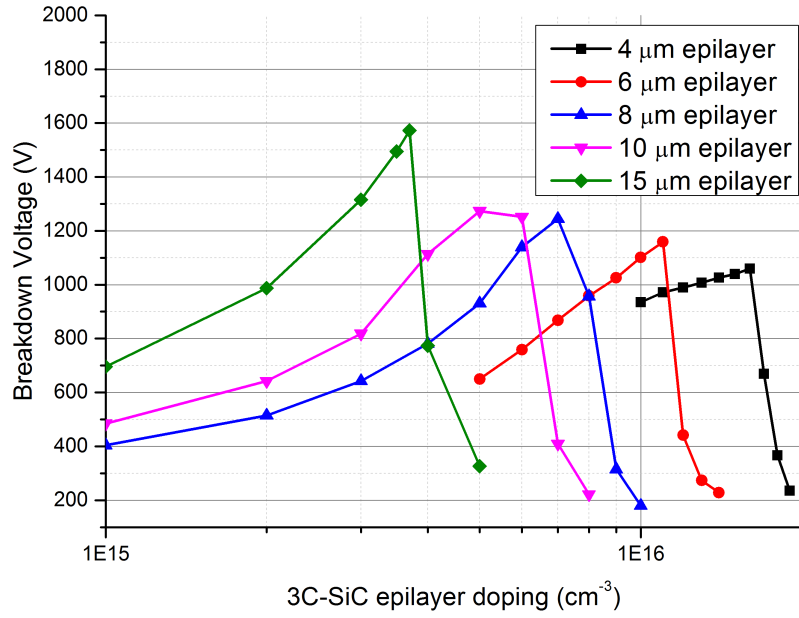


Figure 7.16: RESURF diode breakdown voltage for various epilayer thickness with p-type Si substrate doping of $5 \times 10^{15} \text{ cm}^{-3}$.

A comparison of the 1600 V free standing diode and RESURF diode is summarised in Table 7.3, which demonstrates that the RESURF diode can achieve the same level blocking voltage as free standing diode with almost 3 times lower resistance.

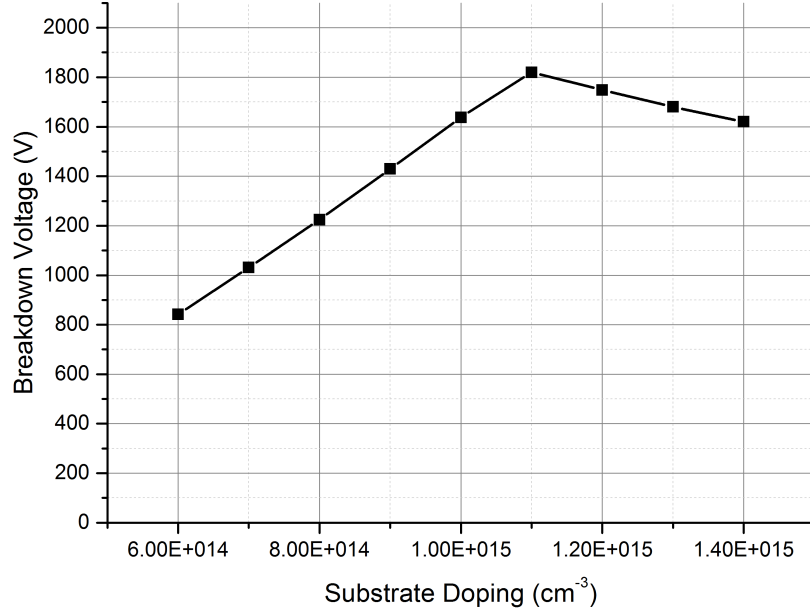


Figure 7.17: The influence of small variations in the substrate doping on the RESURF diode breakdown voltage.

Table 7.3: Parameters comparison between free standing and RESURF diode.

Design Parameters	Free standing diode	RESURF diode
Passivation oxide thickness (μm)	1	1
Anode field plate length (μm)	6	6
Cathode field plate length (μm)	NA	4
3C-SiC epilayer thickness (μm)	4	4
3C-SiC epilayer doping (cm^{-3})	3×10^{15} (n-type)	1×10^{16} (n-type)
Si substrate thickness (μm)	NA	500
Si substrate doping (cm^{-3})	NA	1×10^{15} (p-type)
Breakdown voltage (V)	1580	1600
Leakage current density (A/cm^2)	4×10^{-9}	4×10^{-4}
Forward current density at Anode bias of 1.5 V (A/cm^2)	18	52

7.2.5 Study of surface charge, interface charge and bulk trap effects on the RESURF diode performance

Up to now, the simulation results had been based on ideal materials and fabrication processes which do not include any intrinsic (bulk traps, heter-junction defects) or extrinsic (surface charge) defects. This section looks into how these traps and charges may degrade the device performance. A range of positive fixed charge density was added to the 3C-SiC/SiO₂ interface. Figure 7.18 shows that the surface charge has a bigger influence on the cathode than the anode. The extra charge accelerates the depletion at the PN junction, leading to early device breakdown. Significant blocking capability degradation happens when the surface charge density reaches $1 \times 10^{11} \text{ cm}^{-2}$ as seen in Figure 7.19.

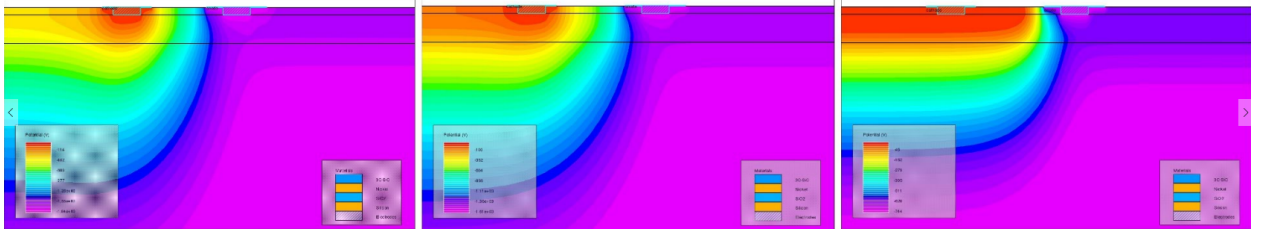


Figure 7.18: Potential contour graph of the RESURF diode with surface charge density of 0, 1×10^{11} and $5 \times 10^{11} \text{ cm}^{-2}$ (from left to right).

When applying fixed charges to the 3C-SiC/Si interface, very similar potential contour graphs (see Figure 7.20) are observed. The threshold after which device blocking ability rapidly degrades is also around $1 \times 10^{11} \text{ cm}^{-2}$ as seen in Figure 7.21.

In terms of the bulk defects, firstly the total bulk trap density effects were studied by assuming a constant bulk trap density throughout the band gap. It turned out that

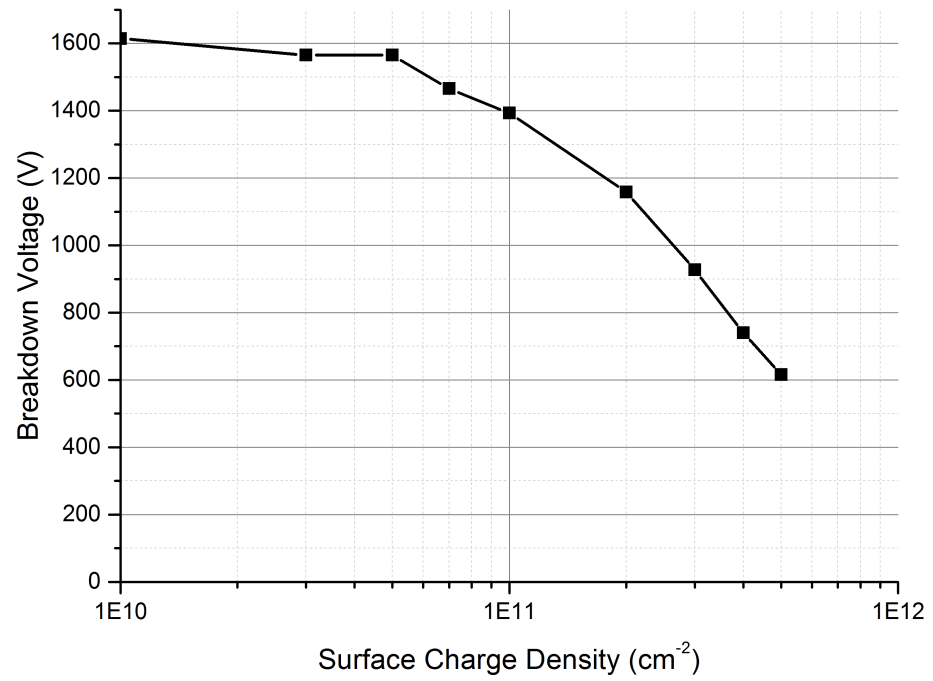


Figure 7.19: Surface charge effects on device blocking ability.

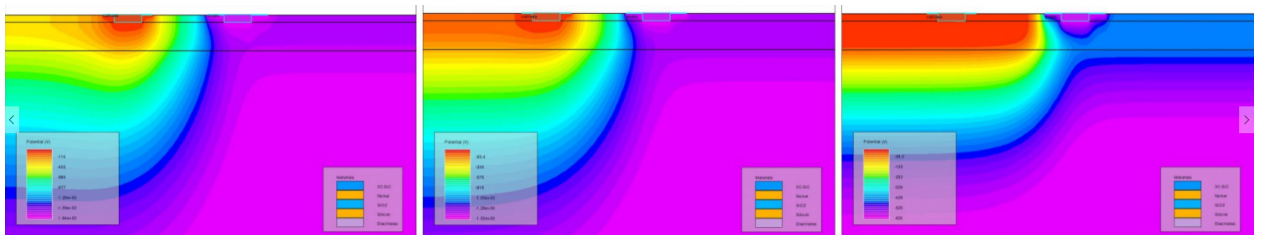


Figure 7.20: Potential contour plot of the RESURF diode with interface charge density of 0, 1×10^{11} and $5 \times 10^{11} \text{ cm}^{-2}$ (from left to right).

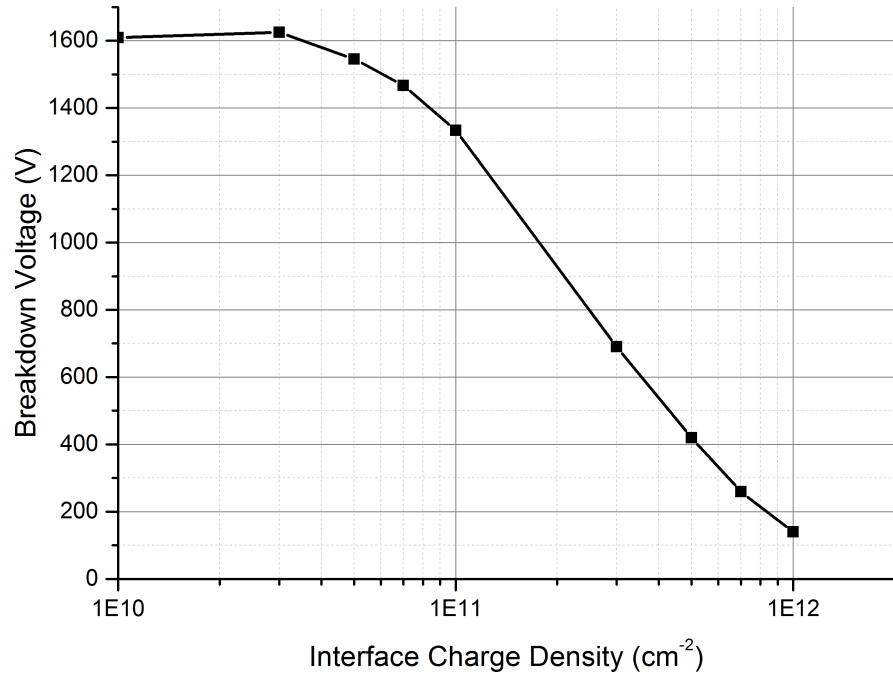


Figure 7.21: 3C-SiC/Si interface charge density effects on device blocking ability.

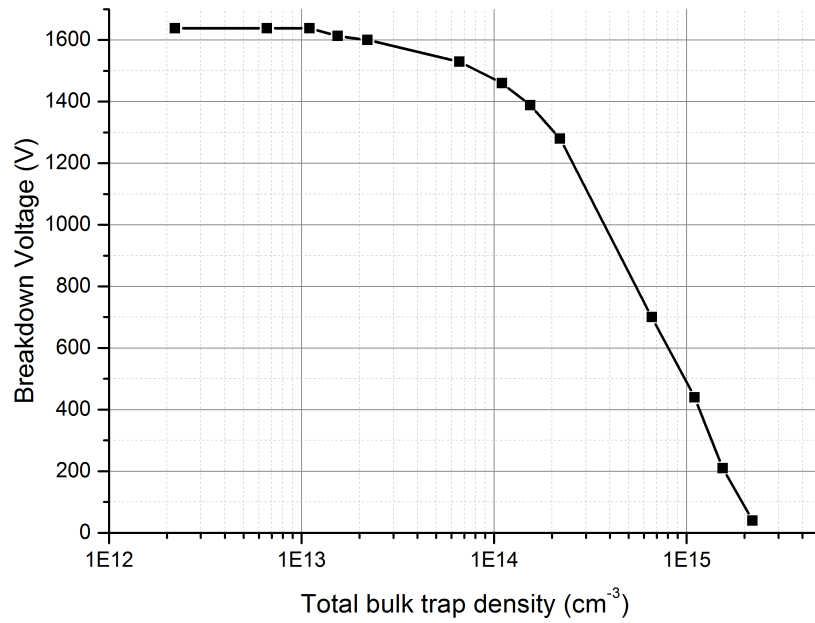


Figure 7.22: The effects of bulk trap total density on device breakdown voltage.

the device blocking ability degrades significantly after the total bulk trap density exceeds $1 \times 10^{14} \text{ cm}^{-3}$ as shown in Figure 7.22. The way that the bulk traps are distributed in the band gap turned out to have little influence.

Figure 7.23 demonstrates 4 Gaussian distributions of bulk traps in the band gap with the same total density of $1.1 \times 10^{14} \text{ cm}^{-3}$. The peak position was fixed to 0.4 eV away from the conduction band edge. As can be seen from the inset graph, the device breakdown voltages are close in all 4 conditions. The trap density peak position was then shifted along the band gap with the total trap density still fixed. Figure 7.24 shows that the peak position has little influence on the device blocking ability, either.

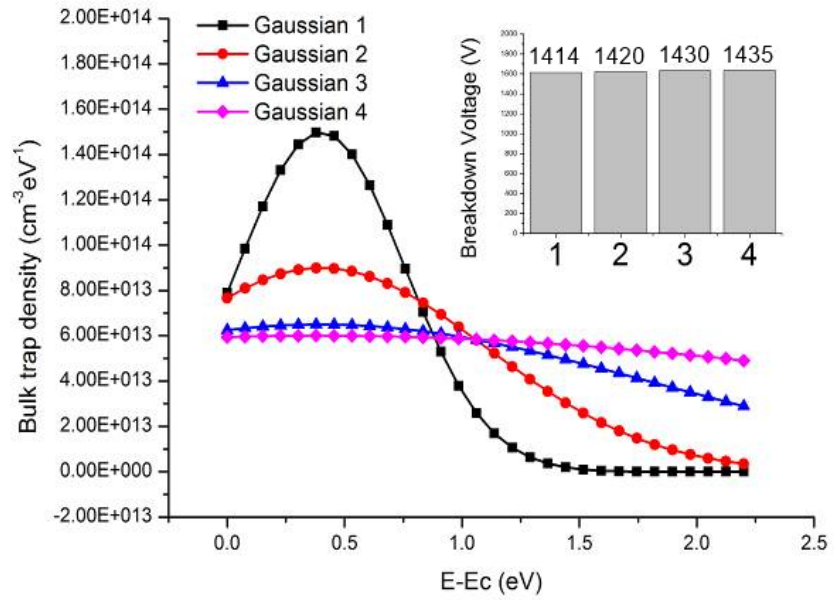


Figure 7.23: Effects of the bulk trap density distribution on the RESURF device blocking ability.

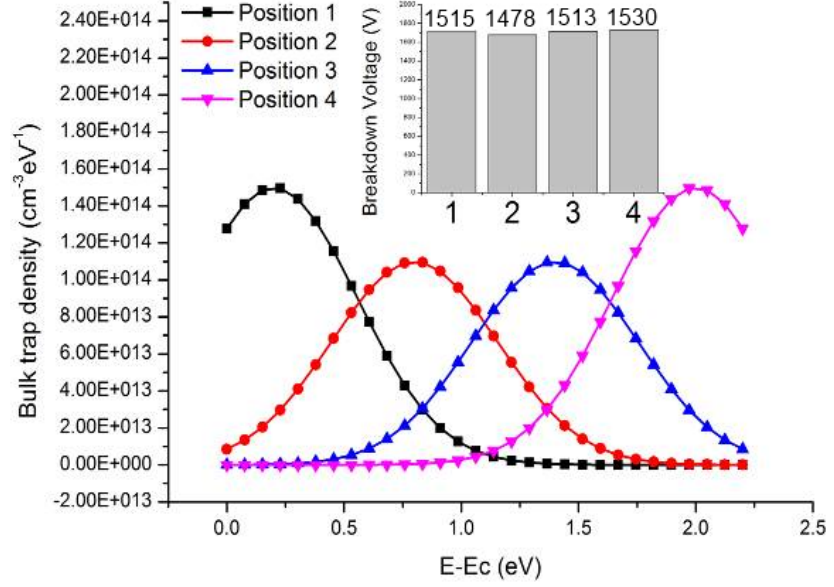


Figure 7.24: Effects of the bulk trap peak position on the RESURF device blocking ability.

7.3 Summary

In this chapter we introduced a novel RESURF device design based on on 3C-SiC/Si wafers. Physical models were built upon literature results and validated with recent fabrication reports on high quality 3C-SiC materials. It has been shown that by applying the RESURF and field plate features, the proposed structure achieves blocking voltage beyond 1200 V without a thick 3C-SiC epilayer. Comparing with a conventional lateral device structure, almost 3 times lower on-resistance can be obtained for the same feature dimensions. This innovative design can be utilised for lateral devices design targeting medium voltage range with relative low current handling ability, such as power ICs and smart power devices.

Coming to this last part of the thesis, the overall conclusions are made for the study conducted in previous chapters. The most significant highlights from the research are summarized below, after which several directions for potential future work are outlined, targeting at further pushing forward the 3C-SiC device technology.

8.1 Conclusions

The general idea of this research was to explore the potential and capability of fabricating power MOSFETs on 3C-SiC/Si wafers. The biggest motivation behind this is the possibility of growing 3C-SiC layers directly on large area commercial Si wafers, which can substantially reduce the cost of WBG devices. The 2.4 eV band gap of 3C-SiC makes it more suitable and competitive in medium voltage (600 V to 1700 V) applications among all polytypes. Due to the lack of commercial 3C-SiC wafers until recently, the study on 3C-

SiC devices fabrication is quite limited. As such, a lot of efforts in this research are put into some fundamental processing, including implantation, activation, Ohmic contacts, and MOS interface fabrication on 3C-SiC/Si wafers.

In all devices fabrications, selective doping of semiconductor surface is a necessary step. And for SiC MOSFET manufacturing, high concentration nitrogen is the most common dopant for source and drain regions. In Chapter 3, a thorough study was conducted to investigate the effects of implantation doses, surface preparations, and post implantation annealing conditions on the resultant nitrogen implanted 3C-SiC film electrical properties. The general trends observed are similar to 4H-SiC such as: activation rate increases with annealing temperature and duration, decreases with initial dose levels. Due to a relative smaller band gap compared with other WBG materials, the activation energy of donors in 3C-SiC is quite low that 15 meV was observed for a $1.5 \times 10^{19} \text{ cm}^{-3}$ doped sample. At a $6 \times 10^{20} \text{ cm}^{-3}$ level, the activation energy becomes zero and the implanted 3C-SiC film was degenerated, making it easier for Ohmic contact fabrication. A more interesting discovery is that, unlike other WBG semiconductor which are almost always partially ionized at room temperature, nitrogen carriers in 3C-SiC are readily fully ionized at 150 K. This means Ohmic contact obtained on 3C-SiC is free from the effects of more carriers being thermally ionized at elevated temperatures.

The on-resistance of a power device determines its conduction losses in operation, namely has a great impact on the device efficiency and needs to be minimised. In Chapter 4, a comprehensive investigation was undertaken to characterise the fabricated Ohmic

contacts, physical and electrical. A Ti/Ni bilayer stack was used to form Ohmic contacts on previous nitrogen implanted & activated 3C-SiC films. From the I-V characterises obtained at elevated temperatures, it is found that the fabricated Ti/Ni Ohmic contacts are thermal stable yet the surface doping levels suggests the interface carrier transportation should not be dominated by field emission. Looking back into literatures, this unique feature is explained by the Schottky barrier height elimination at the metal/3C-SiC interface, which is further attributed to the relative low affinity level of 3C-SiC among WBG semiconductors. It is worth mentioning that as-deposited Ti/Ni Ohmic contact was obtained with low contact resistivity around $2 \times 10^{-5} \Omega.\text{cm}^2$. This reduces the thermal budget of 3C-SiC device fabrications and opens new doors to the application of SiC transistors with other low temperature technologies, including high k dielectrics atomic layer deposited (e.g. Al_2O_3 or HfO_2) with relative low temperature of growth, ferroelectric polymers a classical example being polyvinylidene fluoride, organic semiconductors such as polythiophenes that can become conducting owing to their conjugated π -orbitals, fullerenes or carbon nanotubes, organic trihalide perovskites, and classic heterojunction or wafer bonded devices. On the other hand, even lower ρ_c approaching $1 \times 10^{-6} \Omega.\text{cm}^2$ was achieved by performing a post metallisation annealing at 1000°C for 1 min after the contact deposition.

The most critical feature for a MOSFET is the MOS interface, particularly for low and medium voltage devices whose total on-resistance is dominated by the channel region. To establish an optimising oxidation recipe for 3C-SiC in Warwick clean room, both lateral

MOS capacitors and lateral MOSFETs were fabricated on 3C-SiC(001)/Si wafers and the results were analysed in Chapter 5 and 6. Various tools were used to characterise the MOS capacitors and it is found that both high-low and conductance methods give similar D_{it} values, while for 4H-SiC the latter usually yields a higher value. This is due to a more uniform surface potential at the 3C-SiC MOS interface, which however can be deteriorated by the N_2O passivation process which also reduced the overall interface trap density. It is also observed that there are very fast traps at the 3C-SiC/ SiO_2 interface, which, however, cannot be quantified by conventional C-V methods even going up to 2 MHz. After a quick study using MOS capacitors, long channel lateral MOSFETs were fabricated using various combinations of oxidation conditions to directly evaluate the channel field-effect mobility. O_2 dry oxidised MOSFETs readily have a relative high mobility around $70 \text{ cm}^2/\text{V.s}$ while a N_2O POA further increases it to $90 \text{ cm}^2/\text{V.s}$. However, almost all devices are normally-on due to the inherent positive charges at the 3C-SiC MOS interface and the counter doping effect of N_2O passivation shifts V_{th} even more into negative. High temperature hydrogenation process was studied by performing gate oxidation in wet atmosphere. This, however, did not lead to normally-off devices even with a compromised mobility value of $60 \text{ cm}^2/\text{V.s}$ due to extra negative charges created at the interface. Since a clear relationship was observed between a higher leakage current and more negative threshold voltage, it can be concluded that V_{th} of these devices is mostly determined by the defect density level of the 3C-SiC eplayer region on which oxide was grown upon, rather than any other processing techniques. The gate oxidation recipe is optimised as a combined 30 mins O_2

dry oxidation followed by a 90 mins N₂O POA, both at 1300°C, which yields the best conducting performance ($\mu_{FE} \approx 90 \text{ cm}^2/\text{V.s}$) as well as highest SiO₂ critical strength ($\approx 8 \text{ MV/cm}$).

Finally, all the techniques developed in previous chapters for individual features are put into fabricating LDMOSFETs on 3C-SiC(001)/Si wafers. The 3C-SiC/Si devices processed with the optimised recipe demonstrates one magnitude higher forward conducting current density than a reference 4H-SiC as well as good scaling ability that 4 mm long devices have almost 4 times higher current than the 1 mm device. Unfortunately, due to the limiting current handling ability of lateral structures, the 3C-SiC/Si LDMOSFET devices only have a current density around 1.37 A/cm^2 ($V_{ds}=5 \text{ V}$, $V_{gs}=-5 \text{ V}$), which is clearly not acceptable for power devices design, not to mention the high leakage current in the channel region even in off-state. It seems that 3C-SiC power devices will only be plausible on free standing 3C-SiC wafers where vertical structures can be fabricated, and the leakage current may also no longer an issue since homoepitaxy 3C-SiC layers are with much better quality. However, it should be emphasised that the fabrication techniques and physics founding developed in work are still valuable and can be directly used even if switching to a vertical structure.

As an independent study, Chapter 7 covers the design and modelling of a novel lateral RESURF structure for 3C-SiC/Si devices targeting at high voltage but low current applications. Device being able to block 1600 V and with a forward current density of 52 A/cm^2 at 1.5 V bias is demonstrated. This novel design demonstrates 3 times lower

on-resistance than a conventional lateral structure and is suitable for power ICs and smart power devices design, which are alternative applications for 3C-SiC apart from being used as power switches.

8.2 Future Work

The biggest obstacle encountered in this work has been the uncertainties about the quality of 3C-SiC(001) epilayer grown on Si substrates. While most of the processing steps are not much affected, some surely can be further optimised if epilayer grown on free standing 3C-SiC substrates can be used.

First of all, the trials made in this work to fabricate normally-off 3C-SiC/Si MOSFETs had been unsuccessful, not due to processing limitations, but because the epilayer defect density overwrites other parameters effects. If much higher quality material is to be available, a more systematically study can be made on the effects of introducing hydrogenation process such as wet oxidation or forming gas annealing. Making normally-off devices will make 3C-SiC technology much more friendly in practical applications.

Another thing worth to be looking into is to reduce the channel region doping level for MOSFET fabrications. Here the post implantation annealing temperature is limited by the melting point of Si substrate 1412°C, thus a high doping level of $1 \times 10^{18} \text{ cm}^{-3}$ was applied for the p-body region implantation to compensate the low activation rate of a relative low annealing temperature (1375°C). Free standing 3C-SiC wafer is free from

this concern and typical p-type dopant activation temperature (1600°C to 1700°C) for SiC then can be applied, which means a lower initial doping level such as $1 \times 10^{17} \text{ cm}^{-3}$ is possible. This will reduce the Coulomb scattering at the MOS interface, helping to achieve higher channel mobility.

Also, all electrical characterisations performed in this work are static since the devices have no blocking ability with the observed leakage current level. This is quite a shame since as shown in the Table 2.1, 3C-SiC has the highest saturation drift velocity among all polytypes. The switching losses of a power devices decreases with switching frequency, thus a comparison between Si, 4H-SiC and 3C-SiC would be useful in evaluating the 3C-SiC devices overall performance.

In the end, for the lateral RESURF structure demonstrated in Chapter 7, all modelling activities had been limited to 2D simulations due to the capacity of the simulator. It has been demonstrated on Si that by using a 3D RESURF structure of segmented n-p drift regions [187], the device specific on-resistance can be further reduced that approaching vertical designs. It will be very interesting to see the result of implementing this 3D RESURF feature on 3C-SiC/Si structures.

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