Wave function-dependent mobility and suppression of interface roughness scattering in a strained SiGe *p*-channel field-effect structure

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The 4 K Hall mobility has been measured in a top-gated, inverted, modulation-doped $Si/Si_{0.8}Ge_{0.2}$ structure having a Si:B doping layer beneath the alloy. From comparisons with theoretical calculations, we argue that, unlike an ordinary enhancement-mode SiGe *p*-channel metal–oxide–semiconductor structure, this configuration leads to a decrease of interface roughness scattering with increasing sheet carrier density. We also speculate on the nature of the interface charge observed in these structures at low temperature. © *2000 American Institute of Physics.* [S0003-6951(00)01518-7]

Sakaki[1] first pointed out that deformation of the wave function by gating could be used to realize a velocity modulation transistor and Kurobe[2] calculated the effects of such a wave form deformation on the transport times in a back gated GaAs/AlGaAs heterostructure. Wave function manipulation also has relevance for the worldwide efforts to fabricate SiGe *p*-channel metal–oxide–semiconductor (*p*MOS) devices of enhanced carrier mobilities as compared to Si *p*MOS. A particularly attractive structure for SiGe *p*MOS, first investigated by Verdonckt-Vandebroek *et al.*,[3] is one having a $n+$ poly-Si gate with a boron layer beneath the alloy. This combination minimizes parallel conduction in the silicon cap, whilst maintaining a low threshold gate voltage. A further virtue of having the *p*-type doping below the alloy, as noted by Niu *et al.*,[4] is the reduction of the (vertical) effective field in the inversion layer with increasing sheet carrier density. In principle, this would correspond to an increase in the width of the wave function, rather than a decrease found in a conventional SiGe *p*MOS device. This would tend to reduce the deleterious effects of interface roughness scattering. Throughout this letter, the interface of concern is the back interface, i.e., the one furthest away from the gate (see Fig. 1).

To investigate this idea further we have fabricated the top-gated inverted modulation doped structure shown schematically in Fig. 1. The structure, intended for low temperature measurements only, was grown by solid-source molecular beam epitaxy[5] on a low-doped (*n*-type) Si(100) substrate. The growth sequence consisted of a 200-nm-thick Si buffer layer, followed by a 30 nm Si:B doped layer (2×10^{18} cm^{-3}), a 20 nm Si spacer, a 20 nm coherently strained $Si_{0.8}Ge_{0.2}$ layer, and finally a 180 nm Si capping layer. The top gate consisted of a sputtered Ti/Al Schottky barrier, and ohmic contacts for Hall measurements were made to the two-dimensional hole gas (2DHG) by sputtering Al and annealing in a nitrogen ambient at 450 °C for 30 min. The absence of an oxide layer limits the maximum (negative) gate bias, V_g, to about -1.2 V (insisting that the gate leakage current never exceeds 20 pA, as compared to the Hall measuring current of 20 nA). However, this still enabled us to increase the 2DHG sheet carrier density, n_s, from $\sim1.5\times10^{11}$ to $\sim5.2\times10^{11}$ cm^{-2}, while the corresponding Hall mobility (at 4 K) increased from ~700 to ~4650 $cm^2\,V^{-1}\,s^{-1}$. Single subband occupancy and transport solely at the lower heterointerface were confirmed by comparison of the carrier densities obtained from Hall and Shubnikov de-Haas measurements. As Fig. 2 shows, the measured variation of n_s with V_g and the corresponding Poisson–Schrödinger prediction (see e.g., Ref. 6) are in good agreement.

To calculate the mobility as a function of n_s we have used the self-consistent multiple-scattering theory proposed by Gold and Götze.[7,8] The central equation used to evaluate the transport time, τ, is

$$\frac{1}{\tau}=\frac{1}{4\pi n_s m^*}\int_0^\infty q^3 U_q^2 \phi''(q,i0^+)\,dq, \tag{1}$$

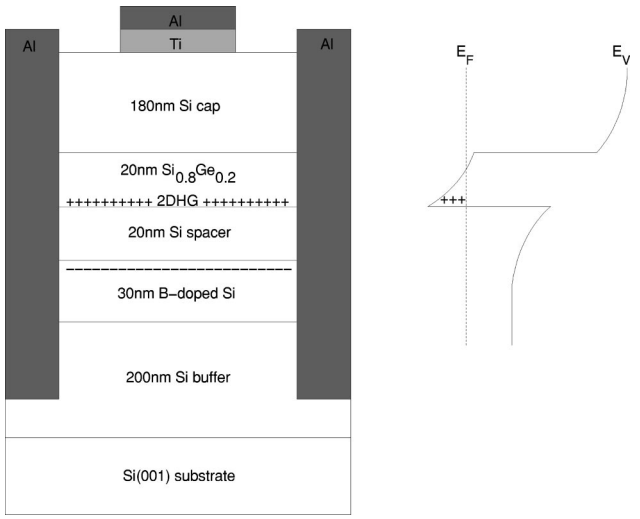

FIG. 1. Schematic of the top-gated inverted modulation-doped structure and the associated valence band diagram. The B-doping slab concentration is 2×10^{18} cm^{-3}.

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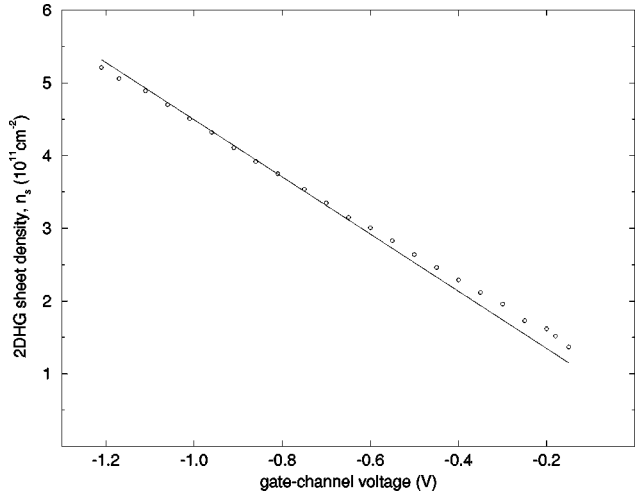

FIG. 2. Measured (circles) and calculated (solid line) variation of carrier sheet density with gate voltage. A valence band offset of 180 meV for $Si_{0.8}Ge_{0.2}$ is assumed.

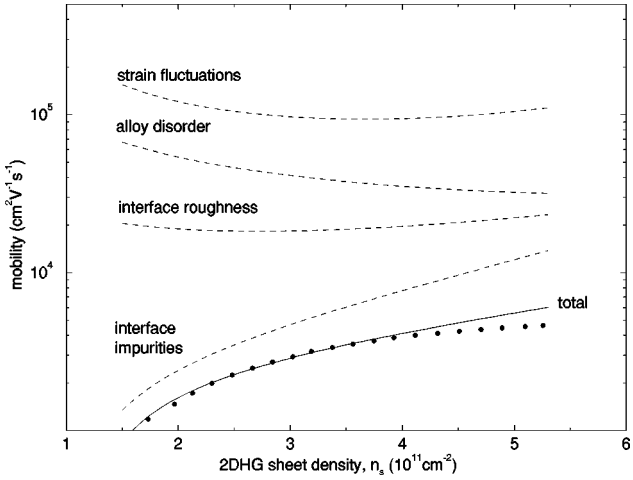

FIG. 3. Measured 4 K Hall mobility (circles) vs hole sheet density compared with theory (solid lines). The roughness parameters are as follows: $\Delta\sim0.95$ nm, $L\sim1.9$ nm, $n\sim1$. The comparison yields an interface charge density of $\sim0.9\times10^{11}$ cm^{-2}. The relatively poor fit at high carrier densities is attributed to the breakdown of the triangular well approximation, as the width of the state approaches the alloy thickness.

where $\phi''(q,i0^+)$ is the zero-frequency density propagator (with screening included) and U_q^2 is a scattering function or sum of such functions for each type of mechanism included. In the present work we have taken account of: (i) interface roughness scattering associated with random variations in the confining potential,[9] (ii) scattering due to strain fluctuations in the channel caused indirectly by the roughness,[10] (iii) scattering from interface impurity charges,[11] and (iv) alloy disorder scattering.[12] The standard model of interface roughness scattering gives

$$U_q^2 \approx \frac{e^4}{\epsilon_L^2}\left(N_c+\frac{n_s}{2}\right)^2\Delta_q^2, \tag{2}$$

where Δ_q^2 characterizes the roughness distribution. In the present structure, N_c is the capside charge density consisting of surface charges and charges induced by the gate bias. Both N_c and n_s are functions of V_g and are determined by the Poisson–Schrödinger modeling exercise referred to earlier. Rather than make the standard assumption of Gaussian correlated roughness[9] we will, following Ref. 10, assume a power-law distribution of roughness for which

$$\Delta_q^2=\frac{\pi\Delta^2L^2}{\left(1+\dfrac{q^2L^2}{4n}\right)^{n+1}}. \tag{3}$$

Here, Δ is a measure of the roughness amplitude deviations, L is the roughness correlation length, and the exponent n describes the falloff of the distribution at high wave numbers. For scattering from strain fluctuations due to roughness at the interface we have (adapting the theory in Ref. 10 to a triangular confining potential)

$$U_q^2 \approx \frac{f^2\Xi_u^2}{4}\frac{(1+\nu)^2}{(1-\nu)^2}\frac{q^2}{[1+(q/b)]^6}\Delta_q^2, \tag{4}$$

where Ξ_u ($\sim$4.5 eV) is the deformation potential, $f(\sim7.9\times10^{-3})$ is the lattice mismatch factor, and ν ($\sim$0.28) is Poisson's ratio. The parameter b is the one that appears in the Fang–Howard variational wave function[9]

$$b=\left[\frac{12m_ze^2}{\hbar^2\epsilon_L}\left(N_c+\frac{11}{32}n_s\right)\right]^{1/3}, \tag{5}$$

where m_z ($\sim0.28\ m_0$) is the effective mass in the growth direction. Our treatment of the other two scattering mechanisms is as described in Refs. 11 and 12; the alloy disorder potential is assumed to be $U_{\mathrm{AL}}\sim0.6$ eV.

Experimental results for the 4 K Hall mobility are compared with the theoretical predictions in Fig. 3. We have taken the Hall factor to be unity (a good approximation). The theory suggests, in common with previous findings,[6,13,14] that interface charge plays an important role in limiting the mobility at low temperatures. Alloy disorder, interface roughness, and strain fluctuations are relatively less important at 4 K (at least for the carrier concentration range in question), but at 300 K they become much more significant. One can do little about alloy disorder scattering, but the predicted trend whereby the mobility due to interface roughness and strain variations increases with n_s is highly desirable for SiGe pMOS applications at 300 K.[11,13,15] This trend is a direct consequence of the fact that scattering processes associated with roughness at the interface are especially sensitive to the width of the state (wave function).[11,16] As shown in Fig. 4, increasing n_s in the present configuration corresponds to an increasing state width (chosen to be $\sim6/b$ for illustrative purposes). In Fig. 5 we compare the calculated interface roughness and strain fluctuation limited mobilities at 4 K for the present device configuration with an ordinary enhancement mode SiGe pMOS structure,[13] i.e., one not possessing the Si:B doping slab beneath the alloy, but otherwise having the same roughness parameters. Figure 5 does not represent a full calculation for realistic device structures intended for room temperature operation (with oxide layers etc.), but the results do suggest that the trend towards the reduced importance of the rough interface at the higher carrier concentrations is at least plausible.

The values of Δ ($\sim$0.95 nm), L ($\sim$1.9 nm), and n ($\sim$1) chosen to fit to the mobility suggest that the interface is quite rough, although they have not been independently verified by

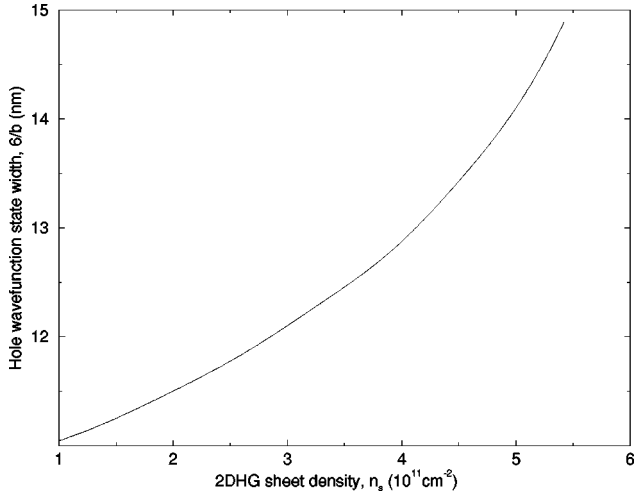

FIG. 4. Variation of the state (wave function) width (taken as $\sim 6/b$, where b is the Fang–Howard parameter) as a function of sheet carrier density.

structural measurements. The results are relatively insensitive to choice of n between about 1 and 3, so this is not seen as a crucial parameter. Regarding the values of Δ and L, there are a number of similar findings in the literature. The high-resolution electron microscopy measurements of Hull *et al.*[17] indicate that the Si on SiGe and SiGe on Si interfaces are rough on this sort of scale. Powell *et al.*[18] also find that the SiGe on Si and Si on SiGe surfaces have comparable roughness on a scale of order 1 nm. Finally, the results of Penner *et al.*[19] suggest a value of the product $\Delta L \sim 0.6$ nm^2 (cf. $\Delta L \sim 1.8$ nm^2 in the present work). One would hope, of course, that these values represent almost a worst case scenario, and that in time higher quality interfaces will be fabricated.

Although interface charge is less relevant at 300 K, it is interesting that the value deduced for the interface charge density ($n_i \sim 0.9 \times 10^{11}$ cm^{-2}) corresponds closely to what has been observed previously for the upper interface.[6,13] This symmetry suggests that the interface charge might be an intrinsic effect not associated with unintentional doping of the alloy. One possibility is that it may be piezoelectric in origin. Several authors have found experimental evidence for piezoelectric effects in the Si/SiGe system.[20–23] Xie *et al.*[20,21] deduced a piezoelectric constant of 1.35×10^{-2} cm^{-2} for $Si_{0.8}Ge_{0.2}$. Braithwaite *et al.*[24] deduced a value of 0.9×10^{-2} cm^{-2} from the ab initio calculations of de Gironcoli and Molinari.[25] From these results one can postulate an interface charge density of order 10^{11} cm^{-2}. The agreement with experiment could be fortuitous but suggests that possible piezoelectric phenomena in this strained layer system are worthy of further investigation.

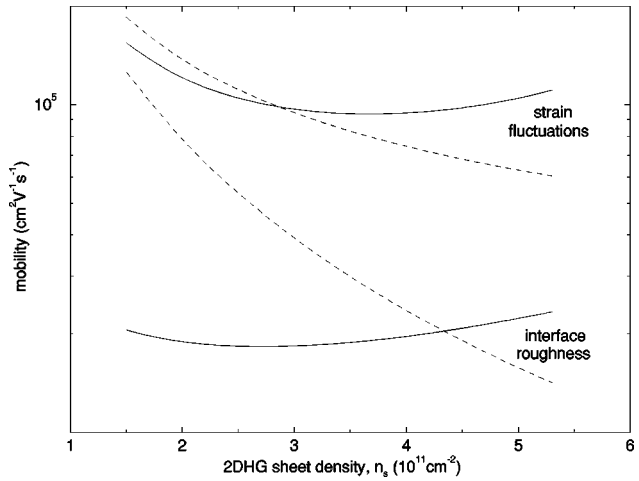

FIG. 5. Theoretical calculations of interface roughness scattering and scattering from strain fluctuations at 4 K: Solid lines-inverted structure (present work), dashed lines-conventional enhancement-mode SiGe pMOS structure which does not have a Si:B doping slab below the alloy. The roughness parameters are $\Delta \sim 0.95$ nm, $L \sim 1.9$ nm, and $n \sim 1$ in both cases.

In conclusion, it appears that interface roughness scattering in the Si/SiGe system can be alleviated to some extent by reducing the vertical electric field in the conducting channel—equivalent to increasing the width of the hole wave function. We further speculate that the principal scattering process at the interface at 4 K might be piezoelectric in origin. Although these studies were conducted at 4 K we consider that they have important consequences for 300 K device operation.

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