Design, simulation and analysis of RESURF Si/SiC power LDMOSFETs

By

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A thesis submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy

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March 2018

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Acknowledgements

I would like to first thank Peter Gammon, who has been supervising me and offering academic support throughout my PhD. You are a true professional, enthusiastic about research with an ambition to achieve the best, and more importantly always having an optimistic 'aura' around. No matter how negative I am to one question, you never show a sense of gloomy view but look on the bright side. Without this, I would have published fewer papers than I did, gotten stuck at one point and struggled to move forwards. Not to mention how many Chinglish you spot in my writing, all these let me know how to be competent, confident and self-motivated.

To my second supervisor Phil Mawby, I thank you for your enlightenment and encouragement for my first journal paper. Also the Chinese dinner you and your wife host each year is truly impressive, and I really appreciate your hospitality.

I would like to express my acknowledgements to my family, who have been supporting me during my PhD study. Without doubt, this contributes significantly to my work and continues to be one of important factors to push me forwards.

A special thank goes to Mark Crouch and Corinne Maltby, who are the technicians working at Science City cleanroom. Your experience, expertise and patience in teaching helped me gain some helpful skills about semiconductor processes. It is a priceless memory to be guided by someone with industrial backgrounds, and indeed will be quite useful in my upcoming career. I also appreciate the instructions on the MBE machine from one of our legends: Vishal Shah, though I never had a chance to operate it during my PhD.

Last but not least, I would like to thank the other members of our PEATER group at the University of Warwick, those who are still there and those who have left for other companies: Fan Li, Rong Hua, Tianxiang Dai, Dean Hamilton, Mohammad Al-Amin, Robert Espley-Jones, Craig Fisher, Stephen Russell, Li Ran, Olayiwola Alatise, Mike

Jennings, Roozbeh Bonyadi & Yeganeh Bonyadi, Blossom Mohammadi, Saeed Jahdi, Ji Hu and Petros Alexakis.

Declaration

This thesis is submitted in partial fulfilment for the degree of Doctor of Philosophy under the regulations set out by the Graduate School at the University of Warwick. I certify that this thesis does not incorporate any material without acknowledgement previously submitted to any institution for a higher degree or previously published. The work is this thesis is my own except where stated, under the supervision of Dr Peter M. Gammon and Prof. Philip Mawby.

Chunwa Chan

March 2018

List of publications

Patent

1. P. M. Gammon and C. W. Chan, (WO2016132089) Power Semiconductor Device, 2015. Filed, USA and UK, International Application No.: PCT/GB2015/050467. Link: https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2016132089

Journal articles

1. C. W. Chan, F. Li, A. Sanchez, P. A. Mawby and P. M. Gammon, "Comparative Study of RESURF Si/SiC LDMOSFETs for High-Temperature Applications Using TCAD Modelling," in IEEE Transactions on Electron Devices, vol. 64, no. 9, pp. 3713-3718, Sept. 2017.
2. C. W. Chan, P. A. Mawby and P. M. Gammon, "Analysis of Linear-Doped Si/SiC Power LDMOSFETs Based on Device Simulation," in IEEE Transactions on Electron Devices, vol. 63, no. 6, pp. 2442-2448, June 2016.

Conference papers

1. C. W. Chan, F. Li, P. A. Mawby and P. M. Gammon, "Numerical study of energy capability of Si/SiC LDMOSFETs," 2016 European Conference on Silicon Carbide & Related Materials (ECSCRM), Halkidiki, Greece, Vol. 897, pp. 751-754, 2017.
2. C.W. Chan, Y. Bonyadi, P. A. Mawby, P. M. Gammon, "Si/SiC Substrates for the Implementation of Linear-Doped Power LDMOS Studied with Device Simulation", Materials Science Forum, Vol. 858, pp. 844-847, 2016.
3. C.W. Chan, P. M. Gammon, V. Al Shah, H. Chen, M.R. Jennings, C.A. Fisher, A. Pérez-Tomás, Maksym Myronov, P.A. Mawby, "Simulations of a Lateral PiN Diode on Si/SiC Substrate for High Temperature Applications", Materials Science Forum, Vols. 821-823, pp. 624-627, 2015

Abstract

It is necessary for power laterally diffused MOSFETs (LDMOSFETs) to operate efficiently and reliably in high temperature (<300 °C), hostile environments such as those found in downhole, space, automotive and aerospace applications. Currently, silicon-on-insulator (SOI) technology is a dominant method to achieve this goal due to low leakage current and complete electrical isolation. However, the buried oxide (BOX) layer causes self-heating, which can impact device performance, cause thermal runaway and shorten device lifetime. To address this issue, one solution is to combine a silicon thin film with a semi-insulating (SI) SiC substrate, forming the Si/SiC architecture. LDMOSFETs built on this substrate are expected to deliver much better thermal performance, with electrical isolation comparable to the SOI case. However, the Si/SiC LDMOSFETs do not have a strong substrate assisted depletion effect, which can result in poorer electrical performance than those of the Reduced Surface Field (RESURF) bulk-Si and SOI LDMOSFETs. This thesis investigates the PN and SOI RESURF layouts and uses them to optimise 190 V and 600 V Si/SiC LDMOSFETs. DC and transient modelling will be conducted on the optimised Si/SiC and their SOI and bulk-Si equivalents. Based upon this, several comparative studies are conducted on their simulation results to see the effects of the Si/SiC architecture on the LDMOS designs.

The comparative studies are made on the 600 V Si/SiC LDMOSFETs and their bulk Si and SOI equivalents. It is shown that the Si/SiC devices have the potential to operate with an off-state leakage current as low as the SOI device. However, the low-side resistance of the SOI LDMOSFET is smaller in value and less sensitive to temperature, outperforming both Si/SiC devices. Conversely, under high-side configurations, the Si/SiC transistors have resistances lower than that of the SOI at high substrate bias, and invariable with substrate potential up to −200 V, which behaves similar to the bulk-Si LDMOS at 300 K. A clamped-inductive switching circuit is simulated for the Philips SOI and the Si/SiC equivalent. It is shown that even though the SOI has a smaller chip area and suffered from strong substrate effects during the transient state, the two devices had similar currents and power dissipations at the gate, drain and source. The turn-on losses are higher than that of the turn-off losses due to the presence of parasitic capacitors. However, these similarities do not lead to similar thermal responses in both devices and the SOI is heated up at a much faster rate. By contrast, the SiC substrate in the Si/SiC behaves like an embedded heat sink regulating device temperature close to that of the ambient environment (423 K). In the high current condition, the peak temperature in the Si/SiC is 425 K, lower than 463 K in the SOI, thereby increasing reliability.

The comparative studies are carried out on the 190 V LDMOSFETs in SOI, Si/SiC, Partial SOI (PSOI) and PSOSIC technology, based upon a capacitive and an inductive switching circuit. It is revealed that in spite of having a chip area 75% larger than the SOI structure, the Si/SiC solution undergoes negligible heating in any of the switching conditions simulated, exhibiting a very high energy capability. By contrast, the 22% area increase in the PSOSiC does not considerably change the way the energy is handled. This indicates that the Si/SiC is much more effective than PSOI and PSOSIC in dealing with the transient heating.

List of symbols and abbreviations

E_a	Thermal Activation Energy
C_P	Specific Heat at constant pressure
E_g	Band Gap
N_A	Acceptor Doping
N_C	Effective Density Of States For Electron
N_V	Effective Density Of States For Hole
N_b	Base Doping
Q_{eff}	Effective Dose
T_L	Lattice Temperature
V_{dep}	Depletion Volume
t_{ox}	Oxide Thickness
t_{si}^*	Effective Si Layer Thickness
ε_{ox}	Oxide Dielectric Constant
$\kappa_{\|\|}$	Thermal Conductivity In Parallel To The C Axis
$\kappa_{\perp}$	Thermal Conductivity In Normal To The C Axis
BV_{DSS}	Breakdown Voltage
E_C	Conduction Band
E_{Cri}	Critical Electric Field
E_F	Fermi Level
$\mathfrak{E}_M$	Maximum Electric Field
$E_{surface}$	Surface Electric Field
E_V	Valance Band
$\boldsymbol{E_x}$	Horizontal Electric Field
$\boldsymbol{E_y}$	Vertical Electric Field

H	Heat Generation
$hc.a$	Coefficient For Calculating Heat Capacitance
$hc.b$	Coefficient For Calculating Heat Capacitance
$hc.c$	Coefficient For Calculating Heat Capacitance
$hc.d$	Coefficient For Calculating Heat Capacitance
j	Current Density
k	Boltzmann Constant
L	Device Length
N_d	Doping Of The Drift Region
n_i	Intrinsic Carrier Density
Q_d/q	Drift Region Dose
R_{DS}	On Resistance
R_{sp}	Specific On Resistance
T	Temperature
T_a	Ambient Temperature
T_j	Junction Temperature
tsi	Si Layer Thickness
U	Recombination Rate
W	Lateral Depletion Distance Or Device Width
ε_{si}	Si Dielectric Constant
C	Heat Capacitance Per Unit Volume
V	Voltage
q	Elementary Charge
μ	Carrier Mobility
ρ	Density Of The Material
τ	Carrier Lifetime

2DEG	2-D Electron Gas
2DHG	2-D Hole Gas
CDM	Charge Device Model
BOX	Buried Oxide
DI	Dielectric Isolation
DRIE	Deep Reactive Ion Etch
DUT	Device Under Test
ESD	Electrostatic Discharge
eSOA	Electrical Safe Operation Area
FEM	Finite Element Method
FET	Field Effect Transistor / Field Emission Triode
FOX	Field Oxide
GTO	Gate Turn-Off
HBM	Human Body Model
HCI	Hot Carrier Injection
HEMT	High Electron Mobility Transistor
HHMT	High Hole Mobility Transistor
HTGB	High Temperature Gate Bias
HTRB	High Temperature Reverse Bias
HV	High Voltage
IGBT	Insulated Gate Bipolar Transistor
IOS	Insulator On Silicon
JFET	Junction Field Effect Transistor
JI	Junction Isolation
LDMOSFET	Laterally Diffused MOSFET
LOCOS	Local Oxidation Of Silicon
M/SOS	Metal/ Silicon-SiO_2-Silicon

MIS	Metal-Insulator-Semiconductor
MM	Machine Model
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MTTF	Mean Time To Failure
PCSS	Photoconductive Semiconductor Switch
PSiP	Power Supply In Package
PSoC	Power Supply On Chip
PSOI	Partial SOI
PSOSIC	Partial Si/SiO_2/SiC
RESURF	Reduced Surface Field
RPP	Rectangular Power Pulse
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscopy
SI	Semi-Insulating
Si/SiC	Silicon On Silicon Carbide
SiOSiC	Silicon/Oxide/Silicon Carbide
SOA	Safe Operation Area
SOD	Si-On-Diamond
SODI	Silicon On Double Insulator
SOI	Silicon On Insulator
SON	Silicon On Nothing
SOS	Silicon-SiO_2-Silicon / Silicon On Sapphire
SOTI	Silicon On Thick Insulator
TCAD	Technology Computer-Aided Design
TRIAC	Bilateral Triode Thyristor
tSOA	Thermal Safe Operation Area
UID	Unintentional Doped

XRD	X-Ray Diffraction

Chapter 1 Introduction

Semiconductor devices are key elements in the development of compact, reliable and highly efficient power systems. Other than being used as passive components (e.g. resistors and capacitors), these fundamental devices can be deployed as switches that perform logic control or handle power flows, in the form of either diodes or transistors. Over past decades, the performance of power management modules has been improved significantly, due to the increase in system integration enabled by the advancement of semiconductor and packaging technologies. Examples of such integration are power supply in package (PSiP) and Power supply on chip (PSoC) [1], which feature smaller space, fewer components and reduced parasitic effect.

High voltage (HV) lateral transistors, for instance LDMOSFETs and LIGBTs, can be found in many integrated power systems, such as AC/DC power conversion, HV gate drivers and HV half-bridge stages [2]. Different from their vertical counterparts, their electrical contacts are on a single side of a semiconductor wafer, with the backside potential the same as that of an IC chip. Therefore, they can either be part of an IC chip where the CMOS components are made, or be a discrete unit sharing the same lead frame with the chip in a package [3]. Bulk-Si wafer is widely used for HV power devices, due to the cost-effectiveness of this substrate. The Silicon-on-insulator (SOI) solution is selected if high temperatures and a high degree of isolation is required. Self-heating may cause some problems in this structure, depending on the device area and pulse duration [4]. Considerable effort has been put into substrate engineering to achieve a better trade-off between electrical isolation and heat conduction, leading to structures like partial SOI (PSOI) [5], Silicon-on-sapphire (SOS) [6] and compound buried layers [7] [8].

Si-on-Diamond (SOD) and Silicon-on-semi-insulating SiC (Si/SiC) are the two latest substrates capable to offer outstanding cooling and electrical confinement comparable to the SOI case. However, they are unlikely to challenge the traditional substrates in domestic applications, due to the relatively high price of diamond and SiC. Space and military operations, by contrast, are less cost-sensitive and focus more on device

survivability in the long term. Exposure to cosmic radiation, high temperature (200 ^{0}C+) and high humidity can cause device malfunctions, which needs to be counteracted by a degree of protection. This could mean a larger area, more circuit elements and higher cost for an integrated system. In this respect, the implementation of SOD and Si/SiC in harsh environments seems more promising, as diamond and SiC are chemically inactive and highly thermal conductive, forming very reliable heat sinks. They are also free from a buried oxide (BOX) layer, which is one source of radiation-induced problems in the SOI layout.

Despite having higher heat transfer than SiC in theory, diamond used in practice is often synthesised and has electrical and thermal properties poorer than one in nature. High cost is one factor preventing diamond from being used in mass production currently, unless technological breakthroughs for this material emerge. Alternatively, semi-insulating (SI) SiC wafers are commercially available and has been employed in next generation electronics, such as AlGaN/GaN-on-(SI) SiC transistors at 500 ^{0}C [9], 3510 V lateral SiC-on-(SI) SIC JFETs [10] and 50 kV (SI) SiC photoconductive switches [11].

It is worth noting that GaN and SiC-based devices can outperform their Si counterparts and revolutionise the integrated power systems. However, currently, SiC MOSFETs have a poor channel mobility, which prevents these devices being used in low voltage applications. In order to minimise the parasitic effects, GaN CMOS is being developed and was first reported in 2016 [12] as a stepping-stone for fully integrated GaN power systems. This can be a strong candidate in the harsh environment market, but requires a time period during which the associated technologies are developed, leading to the reduction of bulk/interfacial defects, cost and manufacturing difficulties. It takes time for the industry to manufacture these devices as well, for example, converting the conventional fabrication line to that suitable for such materials. As a result, the complete replacement of Si with wide band gap materials for electronics is a long-term process and more likely, both will co-exist and complement each other in some applications.

When considering all these, it becomes apparent that the Si/ (SI) SiC architecture can be a viable option in the near future, for customers who are looking for integrated power modules operating in extreme conditions. The thermal conduction of this substrate is dominated by the (SI) SiC whereas the top Si film performs electrical actions. These features are illustrated in Fig. 1.1 for the Si/SiC structure, along with its SOI counterpart.

This nature determines that the Si/SiC devices are still bound by the Si limits, such as the critical breakdown field and maximum junction temperature (300 ˚C). However, this also indicates that these devices can be produced with the traditional Si technologies and manufacturing foundry, with the SiC being the only new aspect. Wafer bonding, which binds materials with atomic bonds, can treat this new aspect as a purely SOI case and minimise the problems encountered in the hetero-epitaxy growth [13]. In addition, it has been proven experimentally [14, 15] that the Si fabrication processes can engineer the Si layer of the Si/SiC structure, resulting in electrical characteristics similar to those extracted from the equivalent bulk-Si and SOI devices.

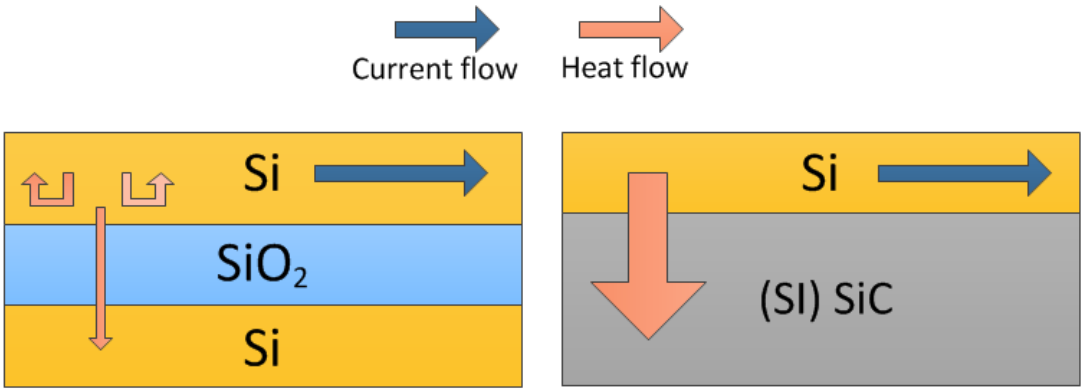

Figure 1.1. The basic features of the SOI (left) and the Si/SiC substrate (right)

1.1. Background

This thesis summarises the initial development of Si/SiC power LDMOSFETs which comprises the theoretical study of the RESURF technologies, TCAD models verification and discussion, design of RESURF Si/SiC LDMOSFETs and numerical analysis of the Si/SiC LDMOSFETs by TCAD simulation. The effect of such architecture on the electrical and thermal characteristics was reported and evaluated, by using bulk-Si and SOI devices as references for comparison.

An investigation into the Si/SiC substrate [13, 16] was carried out at the University of Warwick in 2007-2009, prior to this project. These studies were not limited to lateral devices and was a more general study. Apart from being used as a device layer, one idea

was that the top Si film could be fully oxidised to form a SiO_2 layer on top of SiC. Alternatively, it was proposed as a low-resistance ohmic contact to p-type SiC [13]. Both have the potential to significantly improve the SiC-based devices, yet with some difficulties being introduced, such as the precise control of the thermal oxidation and the reduction of carrier scattering at the Si/SiC hetero-junction [13]. No subsequent work has been carried out to address these issues and therefore, this architecture has not been implemented for SiC products so far. Nevertheless, it is the success in establishing Si/SiC substrates with wafer bonding, as demonstrated in those studies [13, 16] that laid a foundation for the this project, where the Si/SiC hetero-structure is designed to behave like SOI with better thermal conductivity, thereby minimising self-heating effect.

This Si/SiC concept was not without problems. One concern was the presence of disordered layers at the bonded Si/SiC interface, which can negatively affect the device performance. Secondly is whether the SiC can be treated as a dielectric material, by which the active region is confined and leakage current reduced. These were not answered until Shinohara et al. demonstrated experimentally the first functional Si/SiC MOSFETs, with the electrical characteristics comparable to a bulk-Si equivalent [14]. Soon after this, Lotfi et al. showed that even the poly-SiC was capable of offering decent electrical isolation, and that the resulting Si/SiC LDMOSFET performed in a way similar to their fabricated SOI devices [15]. Supported by this evidence, the Si/SiC structure appeared suitable for use in Si-based lateral power electronics.

The targeted high breakdown voltage (200-600 V) is one aspect that differentiates the current work from prior Si/SiC designs [14, 15]. This feature is obtained via a relatively long drift region, placed laterally between the low and high voltage terminal. This region determines the blocking voltage of a device, and contributes the most to the on-resistance for the aforementioned voltage range. Reduced surface field (RESURF) technology is widely used to design the drift region for achieving a better trade-off between the on-resistance and breakdown voltage. Even though this principle was not employed in the previous Si/SiC studies, Lotfi et al. pointed out that a p+ region could be created underneath the n well to enhance the depletion of the drift region in their Si/SiC LDMOSFETs [17], a layout reflecting the RESURF concept. In this thesis, the incorporation of RESURF into the Si/SiC LDMOS design are detailed and investigated, with the temperature effect being considered.

1.2. Thesis outlines

The following chapter first introduces the applications of power electronics and the challenges of harsh environment operation. Next, the high temperature effects on the semiconductor devices are presented before moving on to the approaches to manage the junction temperature and the stress tests to qualify the device's reliability at high temperature. Following this, the high temperature potential of different semiconductors are discussed based on their physical properties and technologies. Finally, two solutions to high temperature operation are discussed, namely semi-insulator and vacuum electronics. This chapter is aimed to offer a general view of how competitive Si-based RESURF LDMOSFETs are to be used for high temperature power ICs (<300 ^{0}C), compared with power switches made from wide/ultra-wide bandgap materials. This device type will be incorporated into the Si/SiC architecture in the following chapters.

Chapter 3 presents some background knowledge required to understand the results chapters. The first to be introduced is the LDMOSFET I-V behaviour, followed by an introduction of different substrates for the LDMOSFET. After this, the LDMOS structure will be described prior to the investigation on the SOI and PN RESURF technologies. The last section talks about the on-state resistance and saturation current of the LDMOS, in terms of low and high-side configuration as well as their temperature dependencies.

In Chapter 4, a 600 V and a 190 V SOI LDMOSFET were constructed in the simulator to verify the TCAD models against the references over the temperature range of 27-300 °C. In Appendix C, the transferability of these models to the Si/SiC architecture are discussed with the literature. These two procedures are aimed to ensure the credibility of the simulation results.

Chapter 5 starts with a preliminary TCAD study of non-RESURF PiN diodes on different substrates, in an attempt to build up the basic knowledge of the Si/SiC architecture. Based upon this study and the RESURF technologies introduced in Chapter 3, three Si/SiC RESURF LDMOSFETs are conceived and described with their SOI, bulk Si and PSOI counterparts. The first embodiment is a 600 V Si/SiC LDMOSFET with a SOI RESURF layout. The second Si/SiC LDMOS structure is also rated at 600 V, but designed with a PN RESURF layout. The third is established with the same technology as the first, albeit the blocking voltage is reduced to 190 V. Following this, the simulation

setups are detailed, with emphasis on the four switching circuits for the aforementioned LDMOSFETs. They are a clamped-inductive circuit, a rectangular power pulse circuit, a capacitive and an inductive circuit with a Zener diode. The first two are for the 600 V devices and the other two for the 190 V transistors.

Chapter 6 provides a TCAD study on the static and dynamic characteristics of the 600 V Si/SiC LDMOSFETs. The DC analysis first compares the Si/SiC device in the SOI RESURF technology with its SOI equivalents. Secondly, the Si/SiC LDMOSFET in the PN RESURF technology is compared with its bulk-Si counterpart. The last part compares all the aforementioned 600 V transistors, in terms of the leakage current, low and high-side resistance. The study on the transient characteristics are split into two parts and based upon the switching circuits described in Chapter 5. The first section compares the dynamic behaviour of the Philips SOI and its Si/SiC equivalent in the inductive switching circuit mentioned in Chapter 5. Next, comparison is made among the Philips SOI, bulk Si and the two Si/SiC LDMOSFETs, of the heating effects in the RPP circuit introduced in Chapter 5.

Chapter 7 presents a TCAD study on the energy capability of 190 V LDMOSFETs in Si/SiC, SOI, PSOI and PSOSiC technology, using the capacitive and inductive switching circuit mentioned in Chapter 5. The first section of this chapter analyses the on/off I-V behaviour of the four transistors under isothermal condition at 300 K (27 ^{0}C). Secondly, a comparison is made between the four transistors on their switching performances during the capacitive turn-on and inductive turn-off events.

The last chapter provides the summary of the results and the conclusions. Suggestions are made for further research of the Si/SiC architecture.

Chapter 2 High temperature power electronics

2.1. Introduction of power electronics

Semiconductor devices have already penetrated every single aspect of human life, from food production, trading and transportation, to education, entertainment and medical treatment. All these activities depend on power generation and distribution systems, which employ a large number of electronics as well. Power electronics is a term to describe semiconductor devices that control or convert electrical power, instead of sensing or processing signals and data.

With the advance of semiconductor technologies, many forms of Si power electronics have been invented for a specific function, to achieve a better compromise between cost, efficiency, complexity and robustness. As can be seen in Fig. 2.1, the capacity (VA) and operation frequency (Hz) is one trade-off that determines the selection of different Si power electronics. The thyristor family, namely Gate turn-off (GTO), bilateral triode thyristor (TRIAC) and normal thyristors, are capable of handling very high power, but perform poorly in medium-to-high frequency operations. Insulated gate bipolar transistors (IGBTs) exhibit a better switching behaviour than thyristors, at the expense of a lower power handling ability. Metal–oxide–semiconductor field-effect transistor (MOSFETs) modules are better options than IGBTs for applications where high frequencies are involved, though the capacity level is reduced even further. High voltage and power integrated circuits (HVICs & PICs) are compact solutions specific for very high frequency operations, albeit its power capability is the least among the power electronics illustrated in Fig. 2.1.

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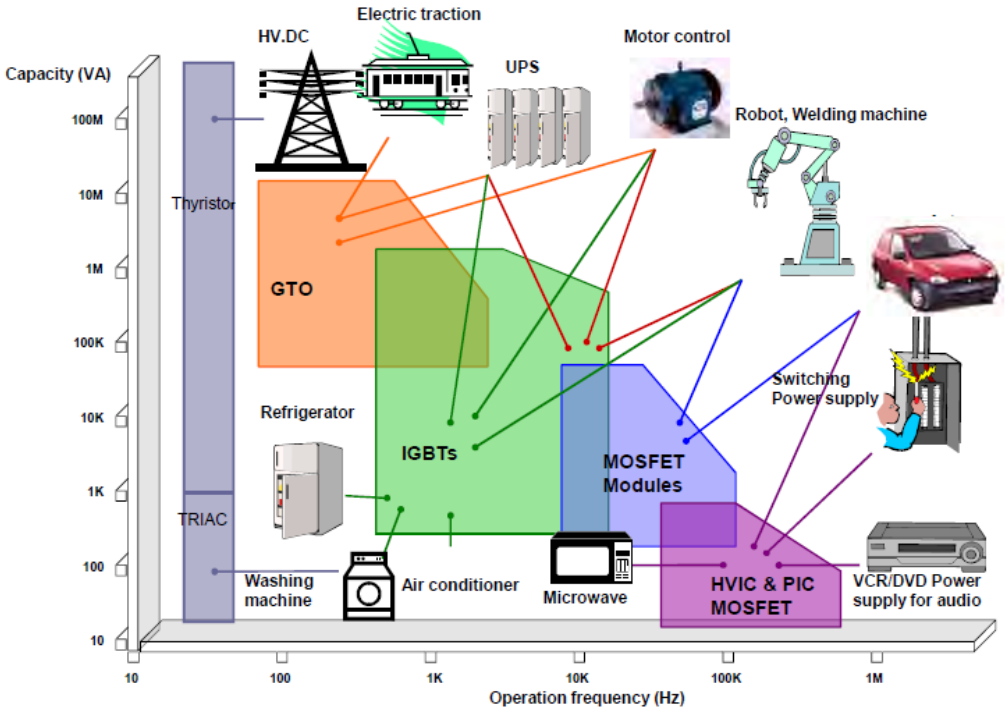

Figure 2.1. Current applications of Si power electronics, taken from [18]

It is expected that the trade-off between capacity and operating frequency can be improved with the continued development of Si power devices. Nevertheless, as silicon approaches its fundamental limit, the gains become more marginal, and significant attention has been paid to wide band gap materials due to their superior properties such as high critical field and saturation velocity. Over the last decade, the research on these materials has led to many commercial products, for instance GaN high electron mobility transistors (HEMTs) and SiC MOSFETs, though some challenges still exist that limit their impact on the Si dominated market. However, as the technology matures, wide-band gap materials are predicted to be the key players in the new frontier, where new higher limits are placed on the frequency-capacity trade-off (see Fig.2.2).

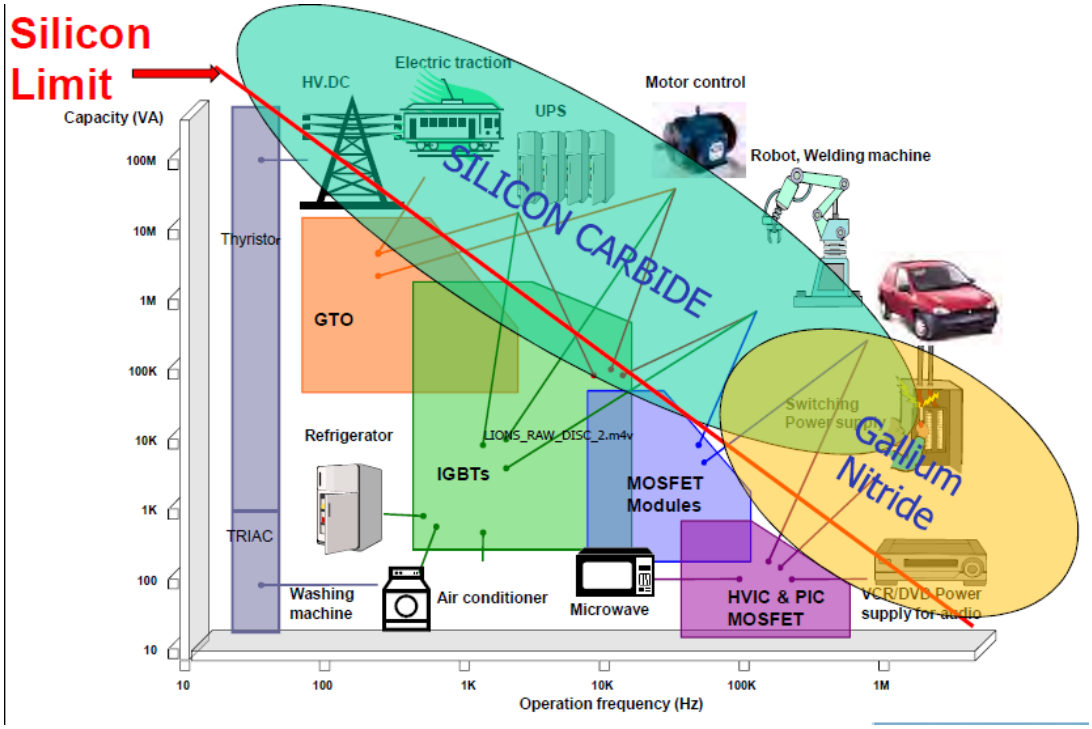

Figure 2.2. Current applications of Si power electronics, with the new frontiers enabled by SiC and GaN, taken from [18]

Although several different power devices exist, at a fundamental level the electrical actions they perform are similar and can be understood via two basic diagrams shown in Fig. 2.3. A common feature to them is a voltage varying resistor and a current control unit which is either a low-voltage diode or switch. In the on-state, the power diode conducts current from anode (A) to cathode (C), as does the power MOSFET from drain (D) to source (S) with the switch closed. The off-state is actuated by reverse-biasing the anode and cathode in the diode, or opening the switch in the transistor. The series resistance becomes significantly higher in the off-state and sustains most of the applied voltage. However, this resistance will be lowered rapidly at the devices rated breakdown voltage. It has to be mentioned that the diagram for the power MOSFET can also be used for other transistors like IGBTs and bipolar junction transistors (BJTs), although the names for the terminals can be different.

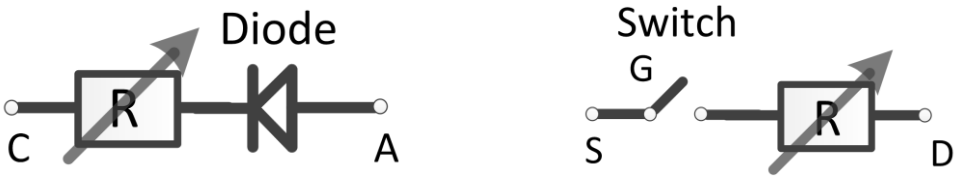

Figure 2.3. Two simple diagrams for a power diode (left) and a power MOSFET (right)

2.2. Harsh environment operations

One challenge in power electronics is the exposure to harsh environment which includes but not limited to shock, high vibration, high radiation and high/low temperature. These extreme conditions can occur simultaneously or/and successively, depending on different applications. In automotive and aerospace, there is an increasing demand in the replacement of traditional mechanical, hydraulic and pneumatic units with electronics for higher reliability and lower life-cycle cost [19, 20]. In this case, semiconductor components will be placed close to the engine and experience vibration and high temperature (125~150 ^{0}C) [20]. Electronics solutions in well-logging will suffer even more severe conditions, for example shock, extreme vibration and very high temperature (225 ^{0}C), which surpass some military specifications [21]. Nuclear plant and waste storage is one area in need of radiation-hard power electronics, for achieving more reliable fuel usage and recycling [22].

Driven by a need to reduce mass and volume, electronics components will be at the core of next generation equipment for space applications [23, 24]. To be used in space, power devices have to meet more stringent requirements than those for customary cases. Electric Power units designed for satellites are required to first survive the launching (high vibration & temperature), then the thermal cycling with the presence of cosmic radiation. Long term reliability is one concern for electric power systems targeted at outer-planetary missions, given that the spacecraft is showered with high-energy particles on the long journey and repair or replacement of broken parts most often impossible. Another problem of space exploration is cryogenic temperature (e.g. 80 K) which will cause carrier freeze-out in most of semiconductor devices [25].

2.2.1. High temperature environment

Among all the extreme ambient conditions, high temperature is of paramount importance in power electronics as it appears in most harsh-environment applications and can induce various side effects, such as chemical reactions, dopant diffusion, performance degradation, electromigration and mechanical stress [22]. Some of these phenomena can cause irreversible damage to semiconductor devices, resulting in system breakdown and a short lifetime. Additionally, the solutions to these failure mechanisms can increase complexity and cost, perhaps with some parameters being compromised. One typical example is the mean time to failure (MTTF) due to electromigration, described by Black's equation (see below) [22]:

$$MTTF = Aj^{-n}e^{E_a/kT} \tag{2.1}$$

Where A is a metal process specific coefficient, j is current density, n is a factor (typically 2 or 3 [22]) T is temperature and E_a is a thermal activation energy. It can be found in Equation 2.1 that MTTF is less sensitive to current density (j), than E_a and T which form the exponent with the Boltzmann constant (k). Even so, it is much easier to reduce the current density for a longer lifetime as this can be done by just adjusting the bias conditions, whereas the variation of E_a involves the change of recipe for contact metals [20, 22] and the reduction of temperature depends on the design of cooling equipment which is more challenging in a hot environment.

2.2.2. Self-heating effects

It should be noted that the temperature in equation 2.1 is not always equal to ambient temperature. The device will generate power losses in operation, which will mean the local junction temperature (T_j) is greater than the ambient temperature (T_a) by an amount dependent on the thermal properties of the system. This will contribute to a decrease of the MTTF according to Equation 2.1, while a variation of T_j within a device can also exist, causing mechanical stress in metal contacts. As temperature increases, the electrical and thermal behaviour of a device will degrade, producing more heat, which exacerbates the situation and can lead to thermal runaway. To alleviate self-heating effects, electronics must be equipped with thermal management units, which add mass, volume and complexity to a system.

One way to regulate temperatures of a power module is to improve heat transfer by using techniques such as air flow cooling, liquid cooling, microchannel cooling, and electrical-thermal cooling [26]. Common to those methods is the presence of a heat exchanger, which can be a heat sink, liquid-cooled cold plate or P/N type pellets [26]. A heat sink is made from metals with good thermal conductivity (e.g. Al & Cu), and can achieve enhanced heat conduction with fins and flip-chip layout [26]. The implementation of liquid-cooled cold plates and circulation of fluid flows in a package can lead to thermal convection, thereby reducing heating effects. By biasing P/N type pellets, the heat can be pumped from the device and directed to an external heat sink, yet with poor thermal efficiency [27].

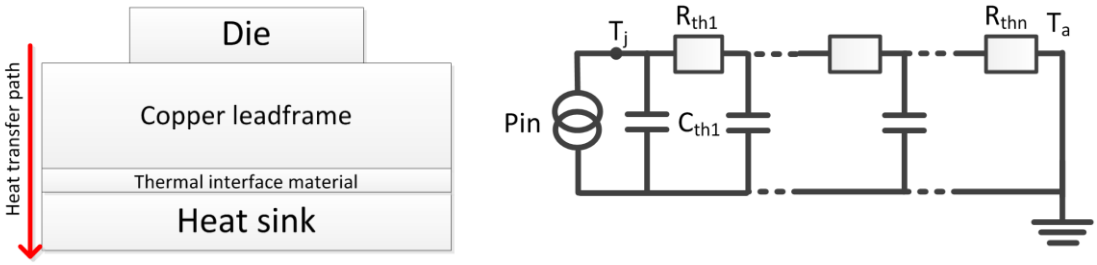

Figure 2.4. A simplified side view of a power module (left) and a 1-D thermal circuit consisting of multiple RC sections to represent the thermal properties of different materials (right). Thermal radiation and advection are not considered

Fig. 2.4 depicts a simple layout for a power component where a heat sink is used for heat extraction from a die. Between the die and heat sink are a copper lead frame and thermal interface materials for adhesion. Also illustrated is a Cauer thermal network formed by a series of RC sections, each of which represents the unique thermal properties of different substances along the vertical heat transfer path. In this circuit, a source is employed to simplify the power dissipation of a device, and thermal radiation and convection are not taken into account. If the source outputs a DC power signal, all the thermal capacitors are open-circuited and the junction temperature can be obtained by Equation 2.2:

$$T_j = T_a + P_{in} \times (R_{th1} + \cdots + R_{thn}) \tag{2.2}$$

This is an approximation of the junction temperature of a device, which is not true to any real application. On the one hand, a device will operate in a switching mode so that the junction temperature is reduced during the off-state. The thermal capacitors will delay the increase of temperature, by absorbing part of the thermal energy. Also, the device can

also be cooled down by lateral heat transfer and thermal radiation, neither of which are considered in the 1-D Cauer network. On the other hand, the switching mode will lead to dynamic losses, which can be significant if a device is driving inductive loads or working at high frequencies. Complicating matters further, thermal impedance is not constant and increases with increasing temperature. When all these issues are factored in, Equation 2.2 appears to be unreliable and a much more detailed model of junction temperature must be derived from finite element methods (FEM).

Another approach to avoid overheating is the application of sensors in a device. This enables the power electronics to be 'self-aware' of the danger that can happen, and respond to it by entering the off-mode. For instance, once the voltage, current or temperature exceed the maximum allowable value, the sensing units will take over the gate control of a transistor and shut it down forcibly [28]. During this idle state, power dissipation significantly drops and temperature is reduced to a safety level, after which device functionality is restored. For achieving an uninterrupted operation, it is necessary to add some redundancies into the system, such as a backup unit that delivers the same function as the device under thermal cut-off. Such protection will make the power module more reliable, but features a complex logic that gives rise to cost and longer development time.

2.2.3. High junction temperature operation

In a datasheet for a power device, a manufacturer usually provides the electrical behaviour of the component at junction temperatures up to 150 or 175 ^{0}C [29] [30], which corresponds to operations in some automotive and aircraft applications. In such hot environment, the switching and conduction losses of the device are higher than those at room temperature as a result of activation of parasitic structures and degradations such as the increase in specific resistance. Furthermore, a greater thermal stress will be exerted on the device package, shortening the lifetime. Therefore, a larger chip area will be arranged for the component to counteract the temperature effects, at the expense of a higher cost. These are the issues encountered by power electronics in high junction temperature operations.

2.2.4. High temperature reliability tests

Before being launched onto the market, semiconductor products will undergo a series of tests to define their lifetime, safe operation area, degradation and fail mechanisms. The tests often stress the products with high humidity, high temperature and high voltage, which makes them degenerate at a fast rate and eventually leads to device breakdown [31]. These tests can not only show the reliability and robustness of devices working in harsh environments but also indicate the period over which the electronics will operate under normal conditions prior to malfunctioning. There are many stressing tests for different applications [32] [31], among which high temperature reverse bias (HTRB) test, high temperature gate bias (HTGB) test and electrostatic discharge (ESD) test are essential to power transistors designed to work at high temperature.

In the HTRB tests, a power IGBT/MOSFET will be configured in a static mode at 150 ^{0}C with its collector/drain biased at the maximum-rated blocking voltage [31]. The same applies to the HTGB tests, except for the gate contact biased to its oxide breakdown limit instead of the collector/drain [31]. Under both conditions, a large number of carriers with high kinetic energy will be created and able to damage the gate/field oxide layers of the device. Trapped charges will therefore be produced at the oxide interface and lead to variations of parameters such as threshold voltage and on-state current [33]. These parameter shifts will be very large after a long working time and the device will be deemed to be unusable. This phenomenon is termed hot carrier injection (HCI) and the ‘hot’ is referred to carrier temperature instead of device temperature [34]. Nevertheless, it is found that in those tests, the parameter shifts of devices in the main rise with increasing junction temperature [33]. ESD tests are designed to mimic the hazard events electronics usually encounter during operation, fabrication and assembly process. Three models are used in these stress tests, namely the human body model (HBM), charge device model (CDM) and machine model (MM). A poor ESD immunity of devices means that an appreciable temperature rise will occur in response to the ESD stress, damaging metal contacts or even causing localised silicon melting [35]. Therefore, power electronics with less self-heating effects is more likely to pass those tests and exhibit stable operation and long-term reliability in high-temperature environments.

2.3. Semiconductor materials and technologies

From section 2.2.2, it can be inferred that the design of any thermal management unit is a huge part in the development of power systems, especially at elevated temperature. Every thermal control unit is tailored for power electronics based upon their losses, thermal behaviour and operating environment. Semiconductor materials have a strong influence on these parameters. They also determine the breakdown voltage and on-resistance, which are two important factors to assess the power transistors. Unless being processed, pure semiconductors do not exhibit any useful electrical functions, such as rectifying and ohmic characteristics. Such materials are not controllable by applied voltages and described as being intrinsic. By contrast, processed semiconductors can transform into a conductor or insulator depending on the voltage bias, thereby realising the on/off-state behaviour. Doping is a very common way to precisely alter the electrical properties of semiconductor and the resulting materials are referred to as being extrinsic.

Material	Si	GaAs	AlGaAs (alloy)	2H-GaN	4H-SiC	Ga_2O_3	Diamond	2H-AlN
Eg (ev)	1.12	1.42	1.9	3.39	3.26	4.5-4.9	5.45	6.2
Direct/ Indirect	I	D	D	D	I	D	I	D
n_i (cm^{-3})	1.5×10^{10}	1.8×10^{6}	—	1.9×10^{-10}	8.2×10^{-9}	2.6×10^{-19} - 1.2×10^{-22}	1.6×10^{-27}	$\sim10^{-34}$
ε_r	11.8	13.1	—	9.9	10	10	5.5	8.5
μ_n ($cm^2/V\cdot s$)	1350	8500	3000	900-2000	900	300	2800	300
E_c (MV/cm)	0.25	0.4	0.5	3.5	3	8	10	12
V_{sat} (10^7 cm/s)	1.0	1.2	1.0	2.5	2.0	—	2.7	1.7
κ (W/cm-K)	1.5	0.55	0.1	1.3 [38]	4.5	0.13-0.21	22	2.85

Table 2.1 Physical properties of semiconductor materials at 300 K [22] [36] [37]

Table 2.1 lists several material parameters associated with power devices, for Si, GaAs and AlGaAs, wide band-gap 2H-GaN and 4H-SiC as well as ultra-wide band-gap Ga_2O_3, Diamond and 2H-AlN [36]. Every semiconductor has its unique band structure, which is responsible for their distinct characteristics. The differences in the band structure can be simply described by the band gap and whether the band is direct or indirect. As shown in Fig. 2.5 for an intrinsic semiconductor, the band gap is defined as the difference between the minimal energy state of the conduction band (E_C) and the maximal energy state of the valance band (E_V). If these two states occur at the same momentum, the band structure is direct, otherwise it is indirect (see Table 2.1). The band gap indicates the minimum energy required by an electron to move from the valance band, which is almost filled by electrons, to the conduction band, which is nearly empty. In the valance band, voids are created after the electron displacement and are termed holes. The generated electron-hole pairs will increase the conductivity of an intrinsic semiconductor, with the few electrons freely traveling in the conduction band, and the holes representing the massive movement of electrons in the valence band. Within the bandgap of an intrinsic semiconductor, there are no other electron states that contributes to the current conduction. The higher the lattice temperature is, the more electron-hole pairs that will be produced, as greater thermal energy is available for the electron transition. However, a wider bandgap leads to a lower intrinsic carrier density (n_i) (see Table 2.1), thereby reducing the off-state current and enabling high temperature applications.

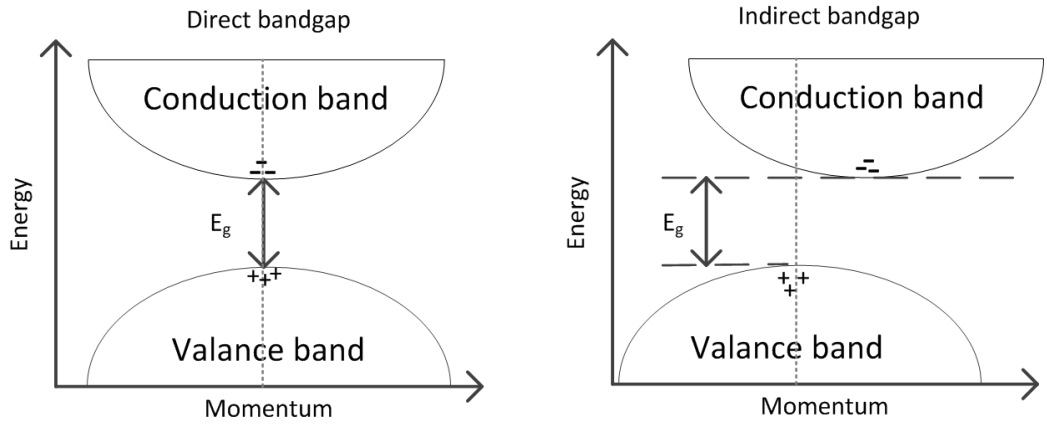

Figure 2.5. Direct and indirect band structures for intrinsic semiconductors, with plus sign (+) and minus sign (-) indicating holes and electrons

It can also be found in Table 2.1 that a wider bandgap gives rise to a higher critical electric field (E_{Cri}). The critical electric field is the limit beyond which the semiconductor loses its intrinsic property and becomes a low resistance short, the result of avalanche breakdown [39]. Avalanche occurs when highly energised carriers collide with the lattice freeing more electrons which are then also energised, producing electron-hole pairs. However, the electrons cannot be set free from the lattice if the energy they possess is less than that of the bandgap. This is similar to the previous case where the electron-hole pairs are thermally produced, albeit the cause here is the electric potential energy.

Within a bandgap, the position of the Fermi level (E_F) with respect to the band edges (E_C or E_v) determines the electrical conductivity of a material. In an intrinsic semiconductor, the Fermi level is close to neither E_C nor E_v, resulting in the least amount of carriers for current conduction (see Fig. 2.6). By introducing dopants in the intrinsic semiconductor, the Fermi level will be shifted towards E_C or E_v according to the dopant type and density. Assuming that all the dopants are ionised, the Fermi level near E_V induces a great number of holes with very few electrons. This extrinsic semiconductor is referred to as P-type material with holes as majority carriers. The opposite case is N-type materials whose majority carriers are electrons.

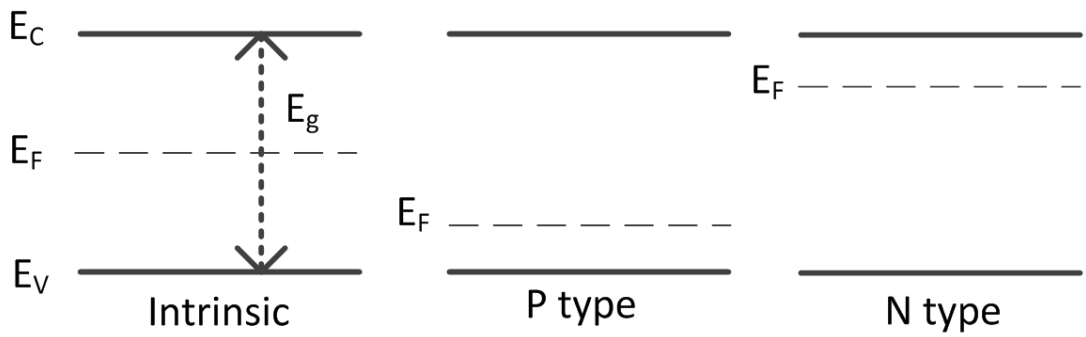

Figure 2.6. The simplified bandgap structure of an intrinsic, P-type and N-type semiconductor

To control the electrical conductivity of extrinsic semiconductors with the applied voltage, the N and P-type materials can be connected together, forming a PN junction (see Fig. 2.7 left). The depletion region in the junction can enlarge or shrink in response to the applied voltage, which gives rise to rectifying behaviour [39]. The Fermi level in this region is positioned in a way similar to the case of intrinsic semiconductor, leading to a very high resistivity. At the junction (x = 0), the electric field reaches a maximum

($\mathcal{E}_M$) which is proportional to the square roots of applied voltage and doping concentration [39]. This means that if the PN junction is reverse-biased and doping level is high, the $\mathcal{E}_M$ can reach the avalanche breakdown limit of a material with a relatively low applied voltage. This relationship is of paramount importance in the design of power electronics. Another way to alter an extrinsic material is by using a metal-insulator-semiconductor (MIS) structure (see Fig. 2.7 right). By applying a positive voltage at the gate, the surface area of the semiconductor will be depleted and exhibit intrinsic property. However, if the bias is large enough, the Fermi level will approach E_C and an inversion layer formed, which is responsible for the current conduction in n-channel enhancement mode MOSFETs [39].

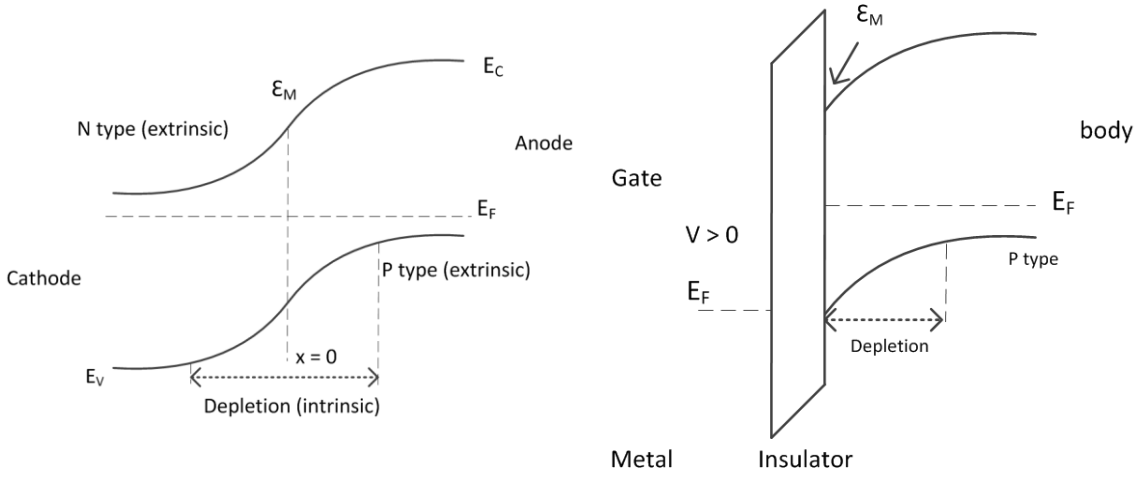

Figure 2.7. The band diagrams of a PN junction (left) and Metal-insulator-semiconductor (MIS) structure (right)

In High Electron Mobility Transistors (HEMTs), the electrical conductivity depends more on the surface band bending than the doping level. This is explained in Fig. 2.8 where a band diagram of AlGaN/GaN heterojunction is illustrated. The bandgap of GaN is smaller than that of AlGaN. Due to the discontinuity in the polarisation field at the junction [37], positive interfacial charges are generated and pull the band downwards at both sides. In this case, the Fermi level is above E_C near the junction in the GaN, which traps a large number of electrons to balance the surface charges. The trapped carriers are confined in the vertical direction but can travel horizontally according to the drain-source bias. This is termed 2-D electron gas (2DEG). Even though the Fermi level is outsides the energy gap near the junction, akin to the case of degenerate semiconductor (very extrinsic) [39], the doping concentration is the same as that of the bulk GaN region,

thereby minimising the effect of impurity scattering on mobility [37]. GaAs is another III-V group material for HEMTs, albeit no polarisation effect is involved. This mechanism can also be implemented in the Al_2O_3/Diamond heterojunctions with the C-H surface treatment, though the conduction relies on holes and the resulting devices are termed High Hole Mobility Transistors (HHMTs) [40].

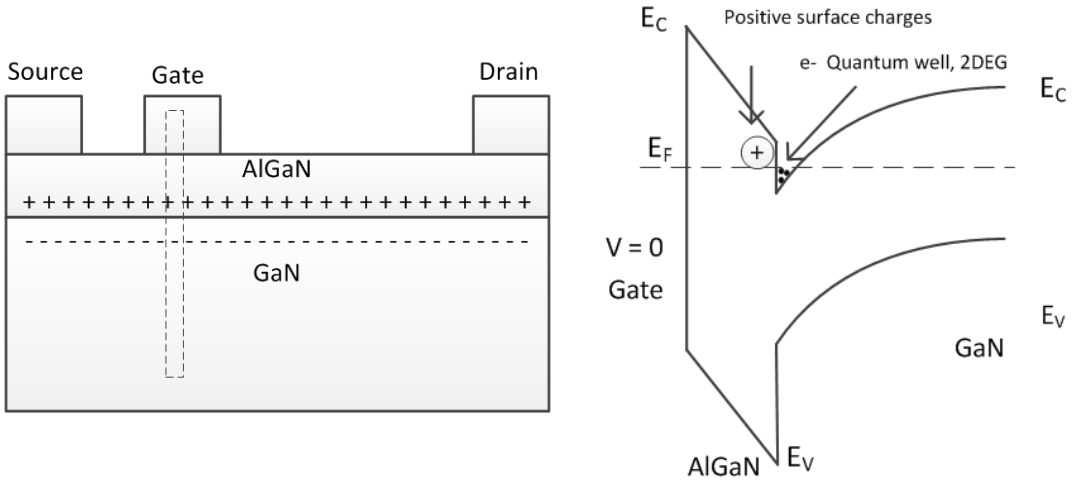

Figure 2.8. The simplified AlGaN/GaN HEMT structure and the band diagram at the gate region

2.3.1. Semiconductors of choice for high-temperature power applications

At sufficiently high temperature, the intrinsic carrier density (n_i) will dominate the electrical properties of semiconductors, instead of the manufacturing processes performed on them. When this occurs, the device is non-functional as there is little difference between the on and off-state current. Therefore, the intrinsic carrier density can be used to predict the maximum operating temperature for a semiconductor. Fig. 2.9 shows the relationship between the n_i and temperature for different materials [41]. Ge and InN are not relevant here. Although 4H-SiC, Ga_2O_3 and Diamond are not shown in the plot, the behaviour of their intrinsic carrier density can be referred to the curves for 6H-SiC and AlN. For $n_i = 1 \times 10^{15}\ cm^{-3}$, a value approaching the doping level in a power device, the critical temperatures of Si is about 300 °C whereas this can be more than 1000 °C for 6H-SiC, GaN and AlN. Despite this, the theoretical limits have not been evidenced in the

power systems made from wide/ultra-wide-bandgap materials, due to the lack of packaging and cabling able to work reliably beyond 300 °C [22]. Therefore, 300 °C is the upper limit of the 'high temperature' described in this work. In the range of 27-300 °C, other factors can be as important as temperature for the leakage current in wide/ultra-wide-bandgap materials. For example, Lee et al. found that at room temperature, the leakage of their HV SiC LDMOSFETs was measured to be a value three order of magnitude higher than that obtained from the simulation [42]. This is because the modelling only considered the effect of intrinsic carrier density on the leakage but in reality, material defects can dominate the off-state characteristics [42].

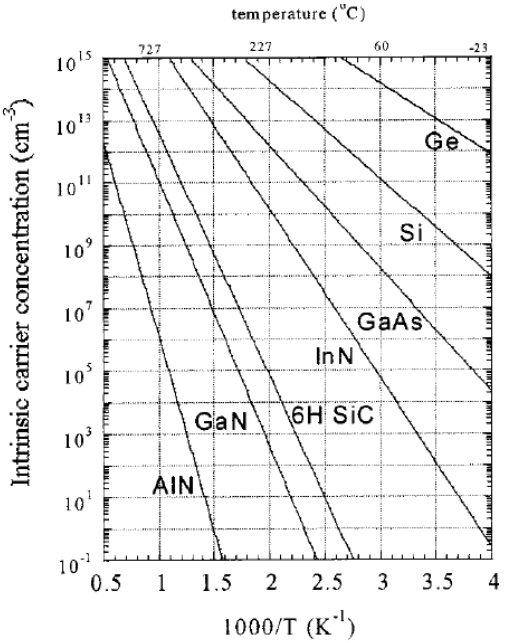

Figure 2.9. Intrinsic carrier density vs Temperature for different materials, namely Ge, Si, GaAs, InN, 6H-SiC, GaN and AlN [41]

2.3.1.1 Silicon

Si is the most widely-used and commercialised material in the semiconductor industries due to its low cost, very high integration level and processing maturity [22]. In spite of having a mediocre thermal conductivity, the smallest bandgap and critical field in Table 2.1, Si is still a strong candidate for power electronics if the targeted voltage and temperature are less than 1200 V and 300 °C. Furthermore, the native oxide layer (SiO_2) thermally grown on Si has a low quantity of defects, which allows a high quality MOS and SOI layout to be formed. The MOS structure is crucial to the long-term reliable operation at high temperature while the SOI can provide full isolation for lateral devices,

thereby significantly reducing the leakage current. For assessing unipolar power transistors, the specific on-resistance is plotted against the breakdown voltage. These figure of merits for Si, SiC and GaN are presented in Fig. 2.10, regarding vertical power MOSFETs [43] [44]. It can be clearly seen that in theory, Si is inferior to SiC and GaN owing to the lower breakdown field. Nevertheless, RESURF technologies (super-junction) can rotate the Si limit curve clockwise (Fig. 2.10 right) and therefore improve the trade-off between the breakdown voltage and on-resistance. This improvement can also be observed in RESURF LDMOSFETs at 25 °C and 125 °C (Fig. 2.11) [45], though the figure of merits are poorer than that of its vertical counterparts due to a less efficient use of the chip area. By using SOI and RESURF technologies together, Philips company developed a 600-700 V LDMOSFET for power ICs, featuring a leakage current of only 1.5 nA/μm at 300 ^{0} C, and a specific on-resistance smaller (7.6 Ωmm^2 at 300 K) and less sensitive to temperature compared with the bulk-Si reference [46]. However, heat dissipation can be an issue due to the presence of buried SiO_2 layer [1].

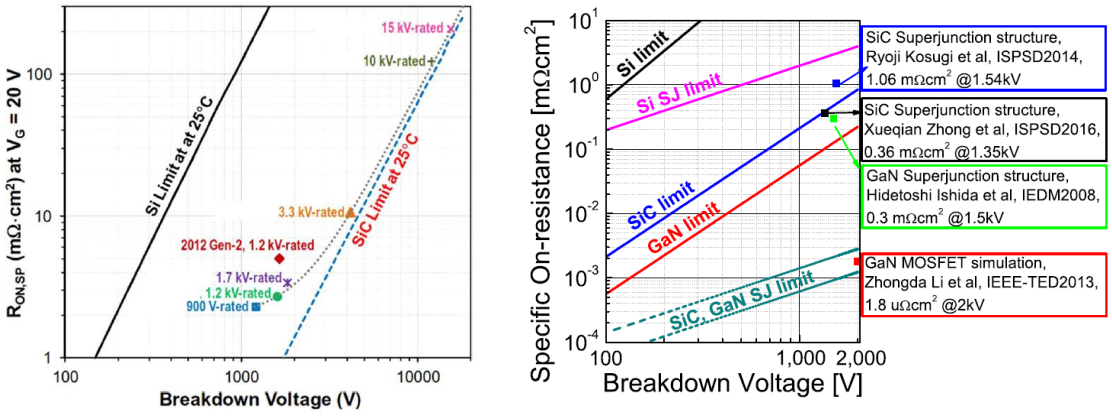

Figure 2.10. The specific on-resistance vs breakdown voltage in [43] (left) and [44] (right), for vertical power MOSFETs made from Si, SiC and GaN

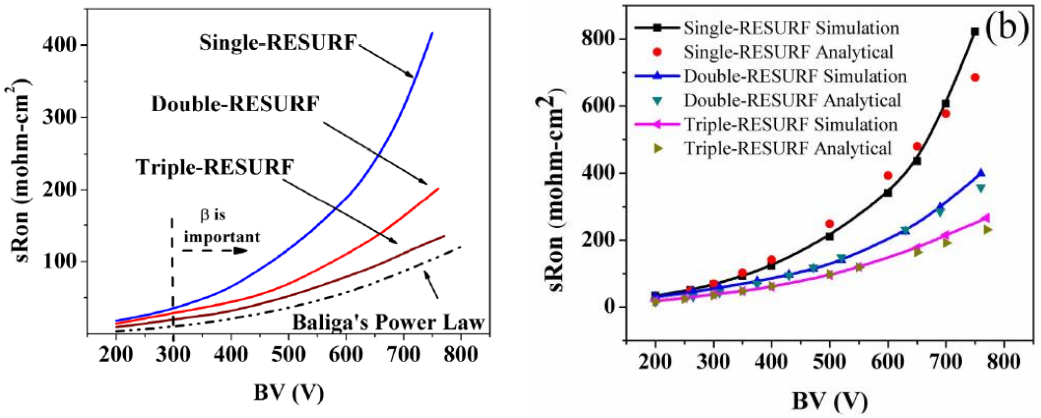

Figure 2.11. The specific on-resistance and breakdown voltage for LDMOSFETs at 25 ^{0}C (left) and 125 ^{0}C (right), designed with different RESURF technologies [45]

2.3.1.2 GaAs

GaAs has a well-developed fabrication processes and specialises in RF, optoelectronic and lighting operation [36]. Due to the availability of semi-insulating (SI) GaAs substrates, this material can also be used for high frequency (200 MHz) power ICs, albeit the rated voltage is limited to 50 V [36]. As such, GaAs and Si do not compete for the same market in general. GaAs devices usually take the form of HEMTs to exploit its ultra-high electron mobility (over 6000 $cm^2V^{-1}S^{-1}$ [36]). However, its superior properties cannot be realised in the p-type devices as the hole mobility of GaAs is less than 400 $cm^2V^{-1}S^{-1}$ [47], which is undesirable for a CMOS logic circuit. At high temperature, the insulating property of the (SI) GaAs substrate will deteriorate, arising from its relatively narrow bandgap (1.42 ev) [22]. Junction isolation is required to address this problem [22]. Furthermore, the thermal conductivity of GaAs is only 0.55 $Wcm^{-1}K^{-1}$ at 300 K and falls

to about 0.15 $Wcm^{-1}K^{-1}$ at 573 K [47], which makes heat extraction more difficult than the Si in elevated temperature operation.

2.3.1.3 GaN

GaN is very similar to GaAs in some aspects, for example the fabrication steps and device layout (HEMTs). However, this semiconductor has a much wider bandgap and higher thermal conductivity, which are favourable to high temperature power applications. In addition, this material can be grown on (SI) SiC substrates for enhanced thermal performance [9], but a much higher cost will be incurred. Theoretical speaking, GaN is more advantageous than Si and SiC for HV power transistors, regardless of the implementation of RESURF concept (see Fig. 2.10 right) [44]. However, the research to approach the GaN limit is in progress and more investigations need to be done to ascertain the surface, bulk quality and defect density of this material [36]. Recently, functional GaN CMOS devices have been demonstrated, which lays a foundation for the GaN power ICs [12]. However, the electron mobility (300 $cm^2V^{-1}S^{-1}$) was found to be much lower than that of the discrete GaN transistors (1000 $cm^2V^{-1}S^{-1}$), and the hole mobility is only 20 $cm^2V^{-1}S^{-1}$ [12]. To sum up, more research needs to be done to achieve the full potential of GaN in power transistors.

2.3.1.4 SiC

SiC has three polytypes adequate for device fabrication, namely 3C, 6H and 4H. Currently, 4H-SiC is the most active in the power applications first due to its high breakdown field [47]. Secondly, the mobility of 4H-SiC is higher than that of 6H-SiC along the c-axis (0001), which is preferable to the vertical HV power MOSFETs [48] [49]. With the announcement of 200 mm 4H-SiC wafers and its high thermal conductivity [36], this material further consolidates its position in high-voltage (≥1200 V) power electronics market. 4H-SiC bidirectional IGBTs has been successfully fabricated for 27 kV applications, with good conductivity modulation observed in the on-state [50]. Super junction technology has also been experimentally implemented in 4H-SiC, and the resulting device is targeted for 1200 V operation and called the CoolSiC trench power MOSFETs [51]. High temperature gate reliability tests on such transistor showed that its extrinsic failure rate satisfied the industrial standards [51]. The RESURF layout used in 4H/6H-SiC LDMOSFETs improves their figure-of-merits and boosts the breakdown

voltage up to 3000 V [52] [42]. It can be seen that none of the state-of-art SiC devices aforementioned is designed for low-medium (≤ 600 V) power applications. This is because SiC MOS channel has a very poor mobility, which substantially raises the on-resistance if the rated voltage is not very high. As can be seen in Fig. 2.10 left, the theoretical SiC limit is only able to correctly describe the practical devices above 4000 V, with a substantial deviation below 1000 V. Furthermore, there are many traps at the SiO_2/SiC interface and its quality has not yet matched the SiO_2/Si in the Si MOS channel [36].

2.3.1.5 Ga_2O_3

β-Ga_2O_3 is found to be the most stable form of this compound material for device fabrication and has a bandgap wider than those of GaN and SiC [36]. The availability of melt-growth techniques for this semiconductor enables large volume and low cost production, which is similar to the Si case [36]. It has been experimentally shown that to block 230 V, the Ga_2O_3 MOSFETs require a gate-to-drain spacing of only 0.6 μm, meaning that the average and breakdown field are up to 3 and 5.8 MV/cm respectively [36]. Wong et al. reported a 750 V Ga_2O_3 MOSFET, built into a (UID) Ga_2O_3 buffer layer on a (SI) Ga_2O_3 substrate [53]. This layout provides a very good electrical isolation at high temperature and stable performance is observed up to 300 °C, without irreversible thermal damage [53]. Nonetheless, Ga_2O_3 is a very powerful thermal insulator (0.13-0.21 W/cmK) and the electrical isolation achieved by this material alone will worsen the self-heating effect. To address this problem, (SI) 4H-SiC can be used as a platform for cooling the Ga_2O_3 transistors, as proposed by Russell et al. [54]. Another issue facing Ga_2O_3 is the lack of p-type dopants. As a consequence, the reported Ga_2O_3 transistors are all depletion-mode N-channel devices and normally-on at zero gate-source voltage [36]. Furthermore, p-type conduction can be hindered by self-trapping of holes in the bulk Ga_2O_3, as predicted in [36] [55].

2.3.1.6 Diamond

Diamond is considered to be the most promising semiconductor for high temperature and power application, due to its ultra-high bandgap, very high breakdown field and superior thermal conductivity. The electrical conductivity of this material can be realised with doping like Si and SiC or Al_2O_3/C-H diamond HEMT structures, which is analogous

to GaAs and GaN [36]. Diamond devices in both technologies exhibit very high breakdown fields in the range of 2 to 10 MV/cm, and high blocking voltages up to 2000 V [36]. It is shown that at room temperature, the diamond HEMTs have a leakage current 2-3 orders of magnitude lower than those of AlGaN/GaN HEMTs [40]. With the improved deposition process for the Al_2O_3 cap layer, the sheet resistivity and hole density of 2DHG were found to be almost constant at temperatures between 27 to 500 ^{o}C, which is more desirable than boron-doped diamond FET for high temperature applications [56]. The formation of a partial C-O channel enables normally-off behaviour in the diamond HEMTs, a valuable feature for safe operation [40]. However, the absence of effective n-type dopants restricts the device types that can be made from this material [36].

2.3.1.7 AlN

AlN is a very good thermal conductor with a bandgap even wider than that of diamond. Therefore, this material can be used as a heat sink with a remarkable insulating property. Research on this nitride for HV electronics is still at early stage but the preliminary results by Fu et al. are encouraging [57]. Their lateral 1 kV Schottky diode has an n-type AlN layer as the active region, on an unintentional doped (UID) AlN for electrical isolation [57]. The breakdown mechanism is believed to be associated with the electric field crowding at the edge of Schottky contact, rather than the AlN layers [57]. A noticeable rectifying I-V relationship is demonstrated at room temperature, featuring a turn-on voltage of 1.2 V, an on/off current ratio of 10^5 and a reverse current below 1 nA [57]. All these indicate the potential of AlN to be used for high temperature and power IC applications.

2.3.2. Conclusions

In conclusion, wide/ultra-wide-bandgap semiconductors are challenging Si in high temperature and power applications. Once their processing is well-developed, wafer prices reduced and technological problems solved, the replacement of Si with those materials for high temperature power electronics is likely. However, Si is still very competitive on the market at the present time, especially for low-medium voltage ($\leq$ 600 V) power ICs working below 300 ^{0}C.

2.4. Others technologies for high-temperature devices

Having introduced different semiconductors and their technologies, presented here are another two solutions that can realise high-temperature power electronics, namely semi-insulator and vacuum technologies.

2.4.1. Semi-insulator technologies

Semi-insulating (SI) semiconductors are gaining interest for use in the harsh environment, specifically given recent interest in photoconductive semiconductor switches (PCSS). SI semiconductors no longer rely on foreign elements to increase its electrical conductivity. Instead, in order to raise the resistivity of the material, it will either remain unintentionally doped, or will be electrically neutralised by implanting deep-level dopants. This intrinsic behaviour can be disrupted by exposing the material to laser pulses, which deliver significant optical energy. This allows the SI semiconductor to be populated with carriers, resulting in current conduction. This phenomenon is similar to the effect of temperature and electric field on the electron-hole pairs aforementioned, however this laser excitement is deliberate and controllable. The more laser energy the semiconductor absorbs, the lower the on-state resistivity will be. Devices exploiting this optical mechanism are termed photoconductive semiconductor switches (PCSS). Such devices can demonstrate a very high on/off ratio and its electric field distribution can be quite even, thereby increasing the breakdown voltage. Furthermore, the semiconductor is not heavily engineered—only metal contacts are compulsory—which can avoid the damage introduced during the fabrication in semiconductor technologies.

Recently, (SI) 4H, 6H-SiC have been used for the PCSS due to their high resistivity and breakdown field [11, 58, 59]. The initial prototype was made from (SI) 6H-SiC and used a lateral layout to minimise the effect of micropipes [58]. The second and third generation displayed a reduced on-resistance due to the replacement of 6H-SiC with 4H-SiC, with the latter device showing a breakdown voltage of 50 kV [11, 59]. In [11], the power switching tests showed that the 4H-SiC PCSS could deliver a peak current of 940 A to a 30.8 Ω load, with a 30 kV DC supply. The peak power and current density were

measured to be 27 MW and 50 kA/cm^2, respectively [11]. Even though no results have been reported on their high temperature operation, it can be expected that devices of this kind resemble the SiC-based electronics in semiconductor technologies to some degree, in terms of the electrical characteristics in hot environment. More specifically, in the off-state where the optical source is turned off, the SiC PCSS can be regarded purely as a semiconductor device and the leakage will go up with increasing temperature like its traditional counterpart. In the on-state, the resistance is related to the device geometry and inversely proportional to the carrier mobility and density [11]. Therefore, the two device types share the same principle for current conduction, which can lead to a similar temperature dependency in the on-state if the optical carrier generation in the PCSS is not strongly sensitive to temperature. One can infer that carrier lifetime is one reason for the temperature sensitivity of the optical process but this is not formulated in the equations in [11], where the process is demonstrated to be temperature-independent.

2.4.2. Vacuum technologies

After being usurped by semiconductor devices and replaced in the majority of applications, vacuum electronics were not completely eliminated and are still used in a few areas. One example is the traveling-wave-tube amplifier used for satellite communication [60]. Over more than half a century, there has not been a semiconductor device that can challenge its position [60]. High temperature operation is another field where an intense competition between vacuum and semiconductor technologies can happen. Even though both device types suffer thermal degradation caused by chemical reaction, metal diffusion and packaging [22], the carrier transport in vacuum electronics is temperature-independent [22], which is different from the semiconductor counterparts. It has been demonstrated that miniature thermionic vacuum circuits can work with little or no loss of functionality in 13000 h test at 500 ^{0}C [22].

Unlike the other two technologies, the electrons are not supplied by the material along the current path, but a hot filament (thermionic) or a cold cathode. It has to be mentioned that the definition of vacuum in this technology can be space void of matter, or a dielectric material (e.g. diamond & glass) [61]. With the advance of micromachining, the cold cathode is desirable due to the increase of reliability. Arrays of cone-shaped protrusions are formed on the cathode surface, to facilitate electron field emission. The released

carriers will be attracted by the anode and travel through the vacuum environment (or the dielectric). Recently, Evince company have mentioned a field emission triode (FET) currently being developed, using diamond as a filling material to create a pseudo-vacuum environment [61].

Chapter 3 Theory

In this Chapter, the principle of LDMOSFET and its figure-of-merits are first stated to offer background information for this work. Prior to the discussion of RESURF technologies, different types of substrates are introduced and compared, with their pros and cons detailed. The last section briefly talks about the on-state resistance and saturation current of the LDMOS, in terms of low and high-side configuration as well as their temperature dependencies.

3.1. Introduction of LDMOSFET

By convention, LDMOSFET is a unipolar device whose on-state current conduction relies on only one type of charge carrier, namely electrons or holes. The LDMOSFETs that employ these two carriers are termed nLDMOS and pLDMOS, respectively. They have the same operation but differ in the polarity of the doped regions and bias conditions for the terminals. Unless stated otherwise, the LDMOSFET described in this section is n-channel, with electrons constituting the main current flow.

Similar to a MOSFET, the operating modes of a LDMOSFET are determined by the voltages applied to its four electrodes, namely source, drain, gate and substrate. Normally speaking, the substrate is connected to ground and its potential can be equal to or lower than that of the source. To turn on the device, the gate-to-source potential (V_{GS}) has to exceed the threshold voltage (V_{th}), with the drain more positively biased than the source. In this case, the transistor will be operated either in the linear region if the drain-to-source voltage (V_{DS}) is small, or in the saturation region if V_{DS} is large (see Fig. 3.1). The drain-to-source current (I_{DS}) is increased with higher V_{DS} and V_{GS} in the linear region, whereas in the saturation region it is only a function of V_{GS}. If self-heating effects are considered, the saturation current will be reduced and negative resistance occurs (see the dashed lines in Fig. 3.1). This is due to the increased power dissipation as V_{DS} goes up, raising the temperature and therefore lowering the carrier mobility.

With V_{GS} equal to zero, the device is in the off-state mode and only shows considerable current at the breakdown voltage (BV_{DSS}) where the avalanche mechanism commences.

Increasing V_{GS} leads to a reduction in BV_{DSS} because the number of mobile charges is increased, which causes high electric field at the drain side [62]. This is called the Kirk effect and the resulting avalanche process will generate holes which drift to the source [63, 64]. If this hole current is large enough, the parasitic npn transistor will be triggered and the LDMOSFET loses control [63, 64]. This forward breakdown voltage at each V_{GS} outlines the boundary of the electrical safe operation area (eSOA). Likewise, the thermal safe operation area (tSOA) defines the conditions under which the transistor starts to show thermal instability. The parasitic npn structure also plays an important role in this case but the device malfunction is initiated by junction temperature [64]. In practice, the safe zone of a device will be influenced by combined electro-thermal actions and changes with bias conditions and ambient environment. At high temperature, increasing the device area and choosing high thermally conductive materials can effectively enlarge the SOA, as the faulty operation is more easily activated by the thermal effects than the electrical.

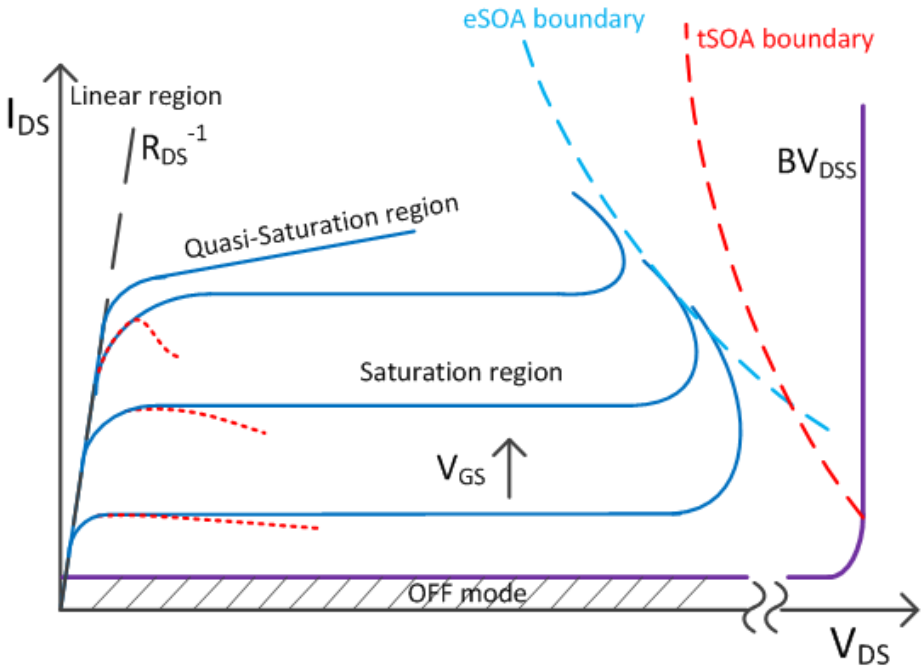

Figure 3.1. I-V characteristics of a n-type LDMOSFET

The high BV_{DSS} is one aspect that differentiates LDMOSFETs from its low-voltage counterparts. This is enabled by introducing a lightly-doped (drift) region between the gate (channel) and drain contact region. This voltage-sustaining region reduces the sensitivity of current to the gate bias at high V_{GS}, creating a quasi-saturation region (see Fig. 3.1). The reason behind this is the high field mobility degradation and electric field

screening [66]. The drift region also requires a larger chip area (A) and will increase the on resistance (R_{DS}). The product of R_{DS} and A is termed specific on resistance (R_{sp}), and widely used to benchmark the on-state performance of various LDMOSFETs. R_{sp} and BV_{DSS} are a pair of trade-off factors and have been studied for many years, which eventually led to the Reduced Surface Field (RESURF) principle, which will be discussed in depth later. Using this concept, a better compromise between BV_{DSS} and R_{sp} can be realised in a power transistor, which translates into a smaller chip area and lower cost. In practice, the device area can be larger than that determined by the RESURF principle so that a better ruggedness and energy capability can be achieved in the LDMOSFET [63]. Therefore, the final product is more likely to be conceived by seeking the balance among BV_{DSS}, R_{sp} and safe operation area (SOA) (see Fig. 3.2 [64])

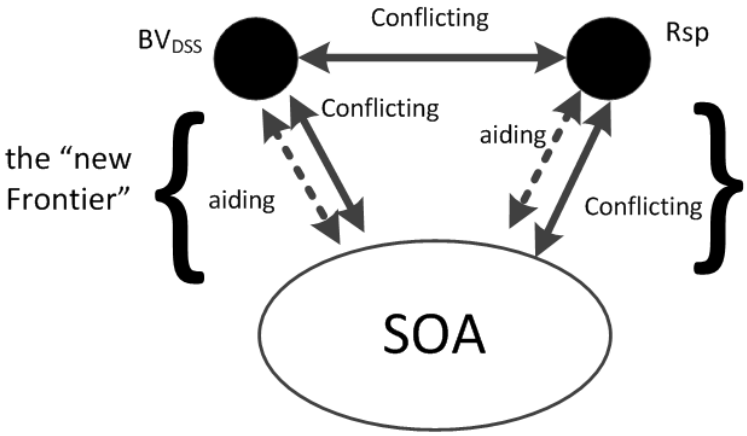

Figure 3.2. A triangle relationship among BV_{DSS}, R_{sp} and safe operation area (SOA) for LDMOS design, taken from [64]

3.2. The substrates of LDMOSFET/LIGBT

Unlike their vertical counterpart, the lateral power device has low and high-voltage terminals on the same side of the wafer, and is designed to perform electrical functions only on the very top region (up to 20 μm thick [67]). Ideally speaking, the rest of the wafer should be completely electrical inactive, and serves only as a heat sink and mechanical support during device fabrication and operation. In reality, the wafer will be engineered in a way that the substrate's electrical interference is minimised or can be manipulated under the specified working conditions. This can bring about a beneficial

change in one aspect but detrimental change in others. Over the last decade, many Si-based platforms have been developed for power ICs, such as Bulk Si, SOI, Partial SOI (PSOI), Si on thick insulator (SOTI), membrane SOI and Membrane bulk Si (see Fig. 3.3). Some of these structures are free from strong substrate effect, while some have to live with it owing to the presence of built-in PN junction or Silicon-SiO_2-Silicon (SOS) layout.

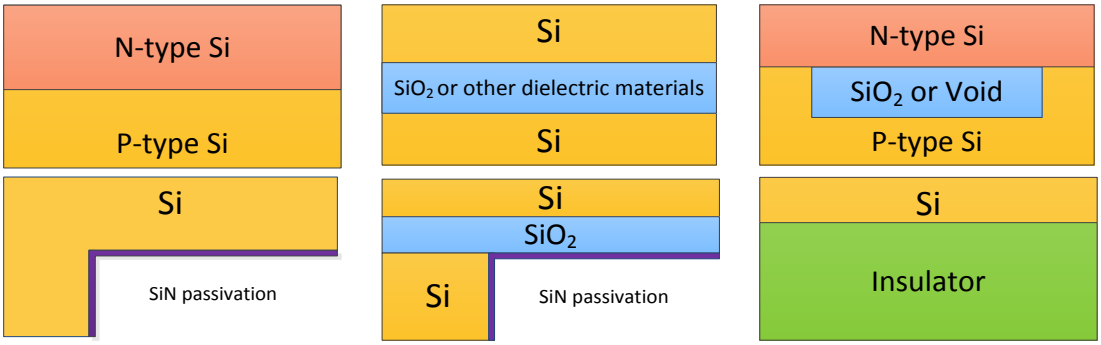

Figure 3.3. The Si-based substrates where lateral power devices are fabricated. From left to right, top to bottom, are Bulk Si, SOI, PSOI, Membrane Bulk Si, Membrane SOI and Si on thick insulator (SOTI).

3.2.1. Structures with substrate effects

Bulk Si, SOI and PSOI are equipped with either a horizontal PN junction or/and a SOS capacitor (see Fig. 3.3), both for electrical isolation. The PN junction allows heat to escape easily while the SOS capacitor does not, which makes Bulk Si the most thermally conductive among the three. However, the PN structure can react with a device's n or p type regions and activate parasitic BJTs, which causes bipolar action and injects carriers into the substrate, thereby increasing turn-off losses. Furthermore, the PN junction is not a strong electrical barrier at high temperature, due to a large thermally produced drain-to-substrate leakage current. By contrast, the dielectric isolation (DI) in SOI prevents the substrate's bipolar effects and offers remarkable device confinement at high temperature. This significantly reduce the power losses in SOI devices in general, which can partially counteract the poor heat transfer ability. Other methods for thermal improvement of SOI includes the flip-chip design [26], replacement of SiO_2 with other dielectric materials such as diamond, SiC or AlN [68, 69, 70], or the PSOI architecture [5]. PSOI permits a combination of the benefits of Bulk Si and SOI, achieving a better trade-off between electrical isolation and heat extraction. An opening is created in the buried layer within

the active area and can be placed under the drain or source side [71], which results in a substrate effect mainly controlled by a PN junction or SOS capacitor respectively. This partial isolation can suppress some undesirable behaviour but large leakage can still be produced at elevated temperature [72]. To tackle this problem, the opening can be placed out of the active area next to the drain, which increases the chip area but makes the device well-confined [73]. Alternatively, the leakage can be supressed by using p-type SiC as the substrate material instead of Si, which forms Silicon/oxide/Silicon carbide (SiOSiC) [72].

In LDMOSFETs/LIGBTs, the high voltage applied to the drain/collector has to be sustained laterally and vertically. This requires the built-in PN or SOS layout to withstand a drain-to-substrate potential up to the specified blocking voltage. The PN junction has an advantage in this case as the SOS structure supports the applied voltage with only the overlayer and buried oxide. The enhanced depletion in the top Si film can cause premature avalanche breakdown in LDMOSFETs, or punch-through breakdown in LIGBTs. The lack of substrate depletion enlarges the drain-substrate capacitance and lowers the switching speed [74]. Increasing the oxide thickness can raise the blocking voltage and alleviate the substrate effect, but worsen the heat transfer ability and induce wafer warpage [75, 76]. Silicon on double insulator (SODI) [77], PSOI structure and the trenched BOX layer [78] can address this dilemma but formation of such wafers is not as straightforward as that of SOI [79]. The same applies to another type of PSOI where the interrupted oxide is replaced with an air cavity (void), which forms a silicon on nothing (SON) structure and improves the breakdown voltage [80, 81]. However, if the SOI transistor has very a high blocking voltage and limited power rating, self-heating will not be a big issue. One example is the 2000 V SOI LDMOSFET having a 12.2 μm BOX layer, developed for HVIC applications [82]. The SOI structure was prepared by wafer bonding and no warpage problem being reported [82]. Although a thick buried oxide is present in this device, the large chip area required for 2000 V increases the thermal capacitance and cross section for vertical heat transfer. In summary, of the three substrates discussed, the SOI architecture suffers the least from the parasitic effects induced by the substrate at elevated temperatures, despite being weak at heat extraction.

3.2.2. Structures without strong substrate effects

Si on thick insulator (SOTI), membrane bulk Si and SOI are constructed to achieve the same goal—the complete removal of substrate effects. The implementation of deep reactive ion etch (DRIE) detaches the Si under the drift and drain/anode region in the two membrane architectures, leaving only a pillar behind under the source for mechanical support [83, 84]. Forming SOTI wafers often involves epitaxial Si growth or a wafer bonding process performed on a bulk insulator, such as sapphire [85] and semi-insulating SiC [14]. As a result, the semi-insulating substrate suppresses any substrate effects on the device and the vertical breakdown limit eased. This allows fast HV LIGBTs to be built on the membrane bulk Si and be free from the back gate MOS effect, preventing the punch-through breakdown [86]. However, the RESURF effect facilitated by the substrate is lost, which lowers the doping allowance in the drift region of traditional LDMOS designs. However, this can be solved by using 3D RESURF technique which depletes the Si layer in the direction of the device width [87].

Compared with the membrane structures, one drawback of the SOTI substrate is the quality of the Si layer. For example, atomic migration can happen during high temperature treatment (e.g. annealing and oxidation) in Si/Diamond and Si/Al_2O_3, leading to an amorphous SiC layer sandwiched in-between [88] and a Si film contaminated by Al acceptors from Al_2O_3, respectively [89]. It has been experimentally proven that Si/(SI) SiC substrates are compatible with the conventional Si fabrication process [14, 15]. Nonetheless, the Si/SiC wafers have higher cost and less wafer yield at the present time, putting them in disadvantage compared with the membrane structures.

3.3. LDMOS topology

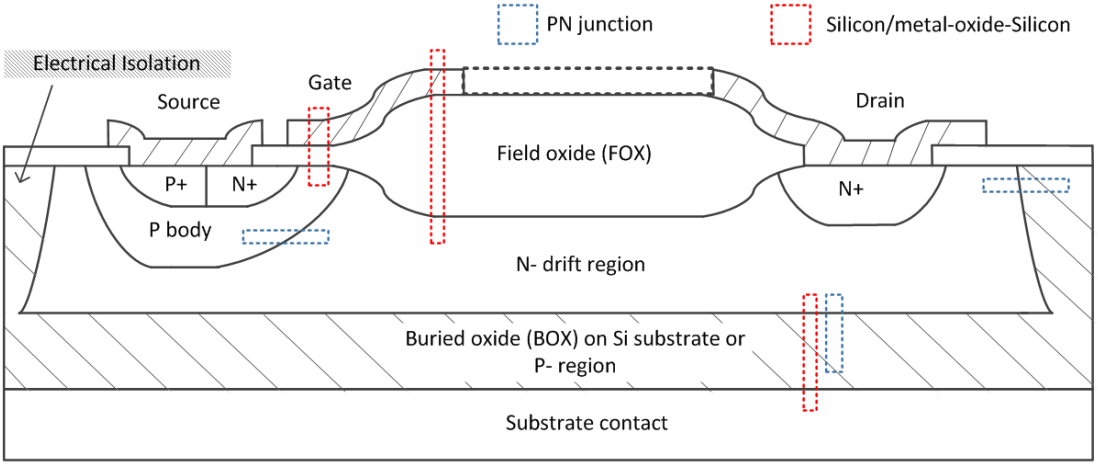

Figure 3.4. The locations of PN junctions and/or silicon/metal-oxide-semiconductor layouts in a LDMOSFET

Fig. 3.4 illustrates an n-type LDMOS layout employing a bulk-Si or SOI wafer. As such, the structure between the n-active layer and the substrate contact is either a thick P- region, or a buried oxide (BOX) layer on top of a Si substrate (n or p type) respectively. The n-type active layer comprises a body region, a channel region, a drift region and a drain region. The body region is defined by a p body doping profile and has a P+ and N+ zone shorted with the source metal. The channel region is laterally offset from the N+ region, embodying the P body width, a gate oxide and a polysilicon top layer. The channel and drain region (N+) is separated by the drift region, above which a field oxide (FOX) layer is formed. The polysilicon gate, acting as a field plate, is extended over the FOX layer without touching the drain metal, or connects to it via semi-insulating material [90] or a PiN diode [91].

Despite the complexity at first glance, this topology contains only two building blocks, namely PN junctions and Silicon/metal-oxide-Silicon (S/MOS) capacitors. Both layouts appear in the drift region and are used to create RESURF effects. PN junctions can be found in the body region and electrical isolation area. An S/MOS structure is placed as the field plate or in the channel region. The next section will describe the RESURF effects induced by the two structures mainly. For more information on their other electrical behaviours (e.g. channel inversion), please refer to this book [39].

3.4. RESURF technologies

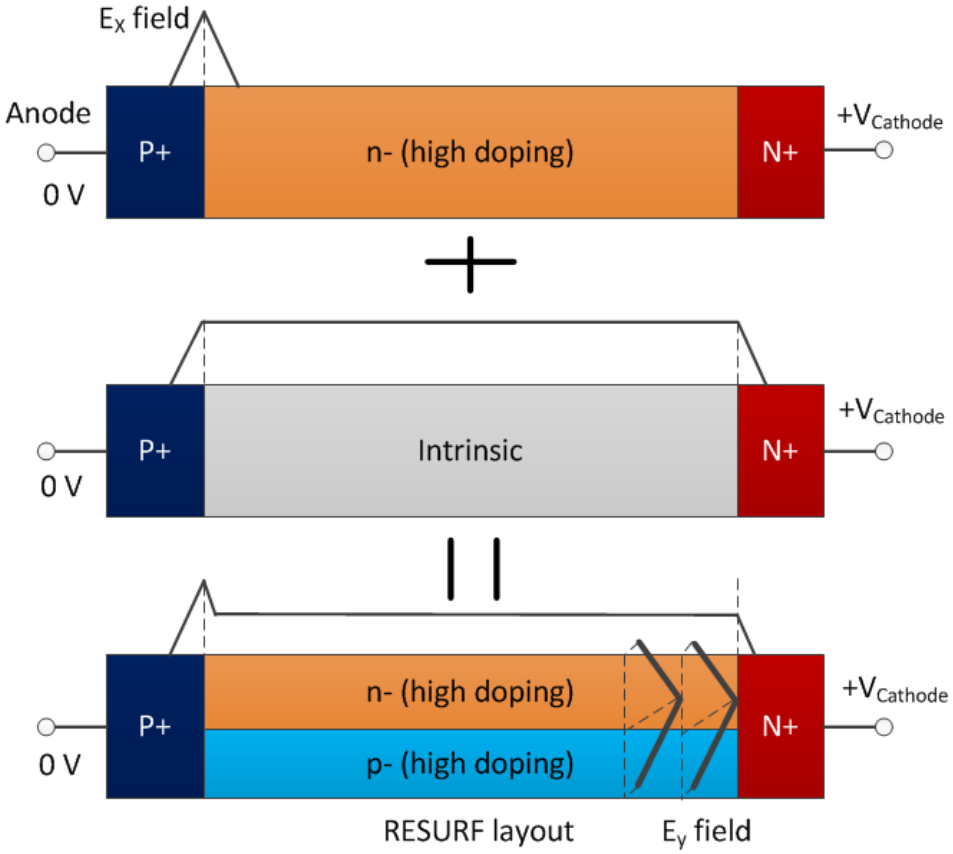

Figure 3.5. A simple demonstration of the RESURF concept by using three PiN diodes differing in the settings of the drift region

The concept behind RESURF technologies is to reduce the on-resistance by sacrificing the least blocking capability. This is realised by depleting the drift region fully in a 2D manner at low voltage using PN and/or M/SOS structures. A concise illustration of this RESURF effect is given in Fig. 3.5, using three PiN diodes consisting of a P+ anode, a drift region and a N+ cathode. They differ only in the setup of the drift region. Also drawn are their electric field distributions at the onset of the avalanche breakdown. With a highly-doped (extrinsic) n-type drift region, the top diode has a very low on-resistance but fails to deliver a high breakdown voltage. This is because the electric field peaks at the P+/n- and only a small portion of the drift region sustains the voltage. With an intrinsic drift region, the blocking voltage is maximised as a result of a uniform electric field distribution. However, this configuration increases the on-resistance substantially. As a

result, neither of the two diodes exhibits remarkable on and off characteristics at the same time. Using a p and n type pillar in parallel in the drift region, the bottom diode can combine the advantages of the first two structures, namely the low on-resistance and high blocking voltage. In the on-state, the conductivity of this diode is related to the doping and size of the n pillar. In the off-state, the two pillars are fully depleted in the x and y direction so that a pseudo-intrinsic behaviour is achieved.

The RESURF principle has more impact on high voltage LDMOSFETs than other device types. The first reason is that in these transistors, the drift region contributes a large proportion of the total on-resistance, for example 96.5 % at 600 V. [44]. Secondly, the specific on-resistance (R_{sp}) is strongly associated with the drift region dose (Q_d/q). This is different from the IGBTs where the drift region conducts current with minority carrier injection. However, some state-of-art LDMOS types can populate their drift regions with extra carriers in the on-state, which is enabled by bimodal [92], accumulation [93] or inversion mechanism [94]. In these cases, the relationship between Q_d and R_{sp} is weakened but the effect of Q_d on the BV_{DSS} still applies as usual, owing to the disappearance of excessive carriers in the off-state. Before jumping into the details of RESURF technologies, a 1-D PiN diode is provided to review the fundamental knowledge of depletion.

3.4.1. 1-D model

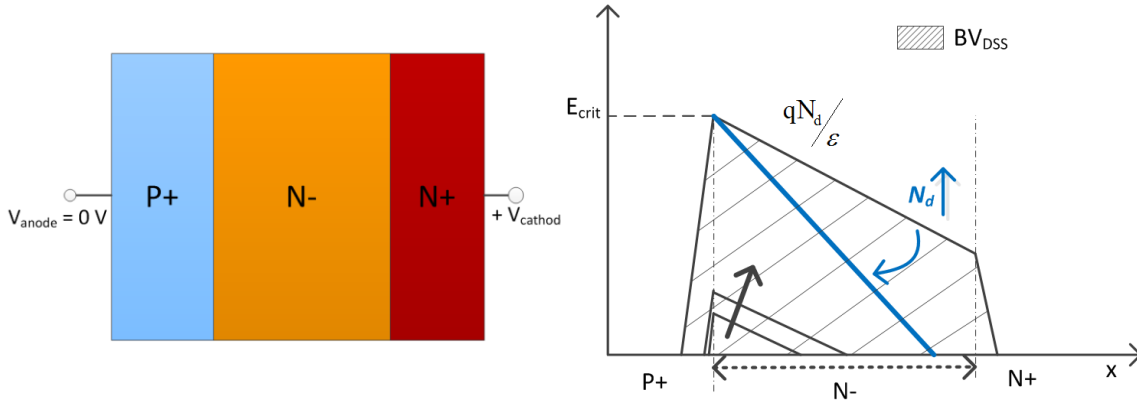

Figure 3.6. A reverse-biased PiN diode (left) and its corresponding electrical field distribution (right)

As can be seen in Fig. 3.6, the 1-D PiN diode is reverse biased and consists of a P+ anode, N+ cathode and N- drift region with a doping density of N_d. According to

Poisson's equation [39], the electric field peaks at the P+/N- junction and drops linearly in both regions at a rate of qN/ε [39]. The integration of electric field along the x direction approximates to the applied voltage. As this voltage increases, the area enclosed by the electric field enlarges and eventually, its vertex reaches the Si critical field level where the avalanche process begins (see Fig. 3.6). Assuming that the N- region is long enough to allow a large number of avalanche carriers to be generated, this critical field level marks the threshold beyond which the PiN diode breaks down, and the applied voltage at this moment is denoted as BV_{DSS}. If one wants to increase the conductivity, more donors will be added into the drift region and the slope of electric field be raised accordingly (see Fig. 3.6). If the critical field level is doping-independent, the BV_{DSS} will decrease and parts of the drift region will support insignificant amounts of voltage. This model has long been used for determining the Si limit for power MOSFETs, but fails to characterise the devices with 2-D depletion behaviour such as CoolMOS and MDMesh [44].

3.4.2. 2-D model

There have been numerous research papers dedicated to RESURF effects in power LDMOS devices. Popescu et al. evaluated some RESURF models for SOI and Bulk-Si cases, and proposed an analytical method able to be used for not only the two traditional technologies but also partial SOI and 3-D devices [95]. Ludikhuize et al. discussed the doping boundaries of RESURF for Bulk Si LDMOSFETs, with the consideration of both low and high-side operation [96]. Boksteen et al. investigated various FP-assisted RESURF layouts suitable for SOI substrates and put forward a mathematical model to optimise them [97]. Zhang et al. studied 3-D RESURF effects on LDMOS and formulated a solution to obtain minimal on-resistance for a specific BV_{DSS} [98]. It can be seen that RESURF analysis can start from different perspectives and be expanded in its own way. As such, the RESURF principle described here will not cover every single aspect, but only introduce the basic concept needed for understanding the structures simulated herein, such as Philips' SOI [46] and Disney's bulk Si LDMOS [99].

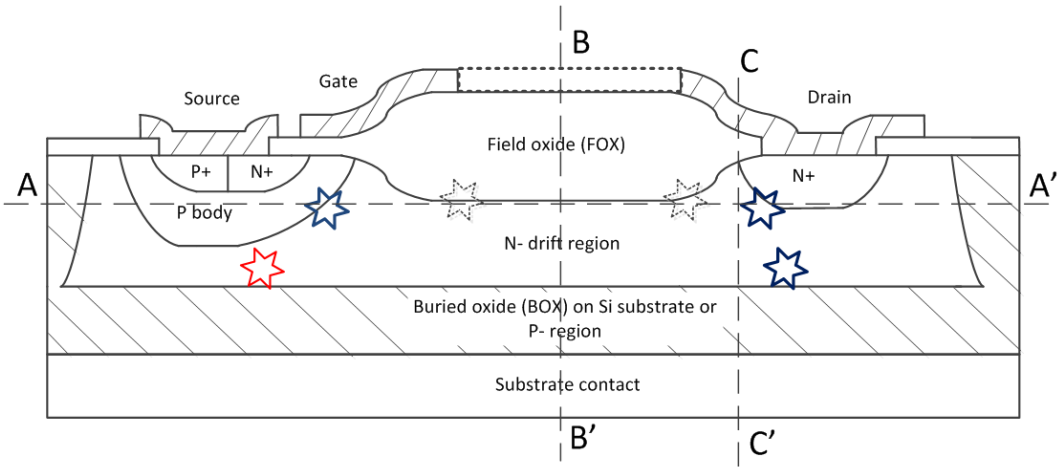

Figure 3.7. A HV LDMOSFET with stars indicating possible breakdown locations. AA', BB' and CC' are the cutlines for analysing the E field along the surface, at the midpoint of drift region and under the N+ drain in vertical direction, respectively

As can be seen in Fig. 3.7, the stars mark the possible breakdown locations of a HV LDMOSFET. From the left to right they are underneath the P body, at the P body/N- junction, below the two points where FPs are terminated, at the corner of N+ drain and the bottom of the active region under the drain. Channel punchthrough and gate oxide breakdown are not considered here as they are related to channel parameters such as P body doping and gate oxide thickness. In a well-designed LDMOS structure, the gate and drain FPs serve as a method to induce depletion from the top of the drift region, which reduces the electric field crowding at the P body/N- junction and drain N+ region. For a LDMOS requiring high-side capability (operating with high voltages compared to the substrate), the doping level in the drift region has to be high enough to hinder the depletion arising from the potential difference between source and substrate, otherwise the punch-through breakdown will happen [96]. For a LDMOS in RESURF technologies, the horizontal junction (PN or SOS) under the N+ drain is where the avalanche process commences. The horizontal field distribution between the remaining two points on cutline (AA') is what makes the RESURF model different from the conventional 1-D case. For a better understanding of this RESURF effect, the vertical field at the midpoint of the drift region (BB') and close to the N+ drain (CC') are highlighted.

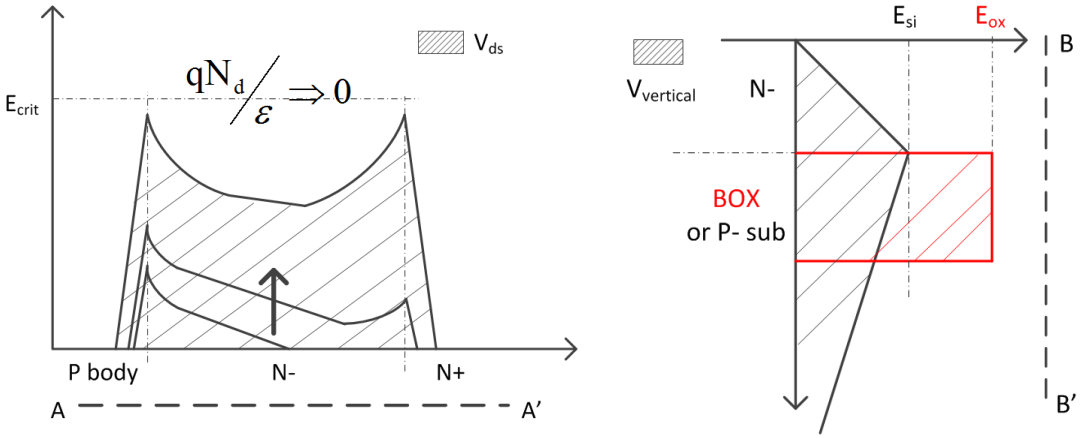

Figure 3.8. The electric field distribution along AA' (left) and BB' (right), for the 1st order RESURF LDMOSFET

If the LDMOSFET has an optimal RESURF condition and FPs effect is ignored, the surface field (AA') will feature two peaks located at P body/N- and N-/N+ junction (see Fig. 3.8). The full depletion of the drift region will occur at low voltage and the slope of E field far from the two peaks approaches to zero. This can be understood by viewing the onset of full depletion at the midpoint (BB') (see Fig. 3.8). Because the horizontal PN or SOS structure is under reverse-bias, a vertical depletion is present and raises the vertical electric field, leading to voltage drop in the *x* direction. This can happen in most parts of the drift region if the optimal dose for each location is satisfied. Despite the drift region having a certain amount of donors, this positive charge is balanced by negative charge in the substrate, resulting in an effective dose of almost zero. Therefore, the gradient of the E field in this case is not in a close relationship with the qN_d, but the difference of the space charges in the depletion zones of the drift region and that of the substrate $q(N_d-N_{sub})$.

The key to creating this effect is the arrangement of the impurity dose in the drift region. The dose value is the product of N_d and the thickness of drift region. It has been found that the optimal RESURF condition demands a drift region with an effective dose ascending from the source to the drain side [100, 101, 102, 103, 104]. Doing so also makes devices strong against the kirk effect as it is difficult for extra electrons to disturb the electric field distribution in the on-state [105]. In practice, a uniform-doped drift region is good enough to deliver a RESURF transistor using a bulk Si substrate. However, LDMOSFETs in traditional SOI technology usually require a drift region with a linearly

varying effective dose, for the formation of a rectangular E field distribution. The following is the RESURF analysis for the bulk Si (PN) and SOI case (M/SOS).

3.4.2.1 Bulk Si

In bulk Si, the RESURF effect is normally produced by PN Junctions (e.g. p- sub/n drift region) with a uniform doping profile. This doping value has to meet two requirements. First, the drift region should be fully depleted at low reverse bias prior to avalanche breakdown. Secondly, breakdown should occur at the bottom of the active region under the drain. Fig. 3.9 illustrates the ideal electric field along BB' (from Figure 3.7) and the one along AA' at the onset of avalanche mechanism, under three different doping conditions. The overdose (dark blue) and underdose (cyan) in the drift region violates the charge condition at the source side and drain side respectively, lowering the blocking voltage. By contrast, the drift region with optimal dose (blue) supports the greatest drain-source potential, due to the presence of an even electric field distribution. The maximum value of this doping is approximated as follows [99]. Along the cutline BB' the vertical field falls from 1.5×10^5 V/cm to zero at the surface, indicating the full depletion of the drift region. Any further increase in the applied voltage will make the maximum electric field under the drain exceed 3×10^5 V/cm, thereby causing avalanche breakdown. At this moment, the dose can be calculated:

$$\frac{dE_y}{dy} = \frac{qN_d}{\varepsilon_{si}} = \frac{E_{surface}}{t_{si}}$$

$$Q_d/q = N_d \times t_{si} \leq \frac{\varepsilon_{si} \times E_{surface}}{q} = 9.8 \times 10^{11}\ cm^{-2} \approx 1 \times 10^{12}\ cm^{-2} \qquad (3.1)$$

Where $E_{surface}$ is the electric field at the surface of the drift region. t_{si} and Q_d/q are the thickness of the drift region and the first order RESURF dose respectively. This dose can be provided by a thick or thin layer, with the corresponding doping density according to Equation 3.1.

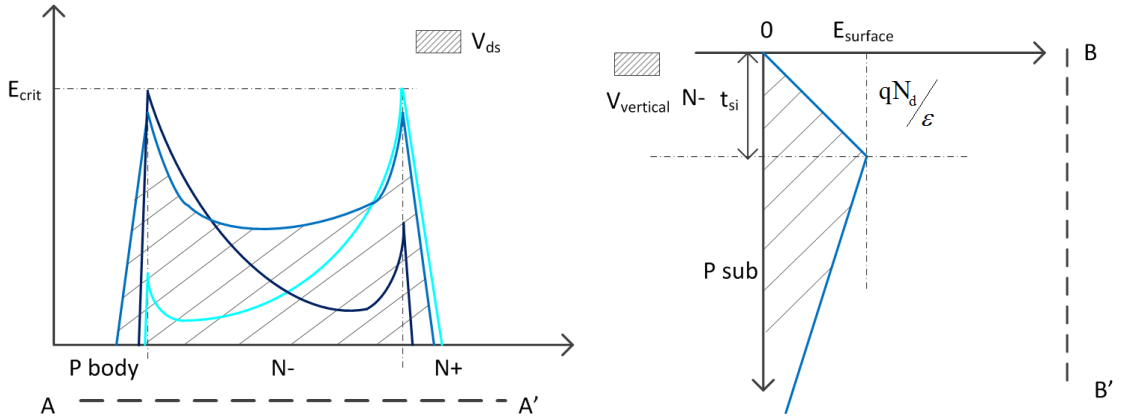

Figure 3.9. The electric field distribution along cutline AA' (left) and BB' (right), when the avalanche breakdown point is tend to be reached.

It is possible to increase Q_d, and thereby further reducing on-state losses, by introducing a p type layer in the drift region. If such a layer is placed on the surface, above the drift region, the drift region will be depleted from the top and bottom and the limit of RESURF dose be doubled (2×10^{12} cm^{-2}) [106] (see Fig. 3.10). It is worth noting that the parameters of the p top region also need to be configured based upon Equation 3.1. By burying the p type layer, the drift region is separated into two sections (see Fig. 3.11) [99]. The upper part is depleted from one side by the p buried layer whereas the depletion is induced from both sides in the lower part. In this case, if a uniform doping profile is assumed, the bottom region has to be two times wider than the top one [99]. As a result, the dose allowance in the drift region is tripled and equal to 3×10^{12} cm^{-2} [99]. This impurity level is compensated by the partially-depleted substrate, and the fully-depleted buried layer with a dose of 2×10^{12} cm^{-2}. Therefore, the drift region exhibits a pseudo intrinsic behaviour despite being highly-doped.

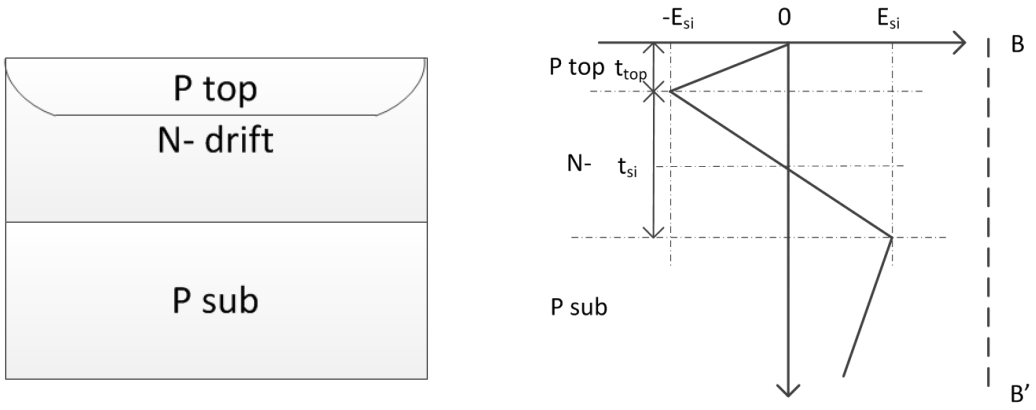

Figure 3.10. Double RESURF Layout (left) and the corresponding electric field along BB' when the drift region is fully depleted (right)

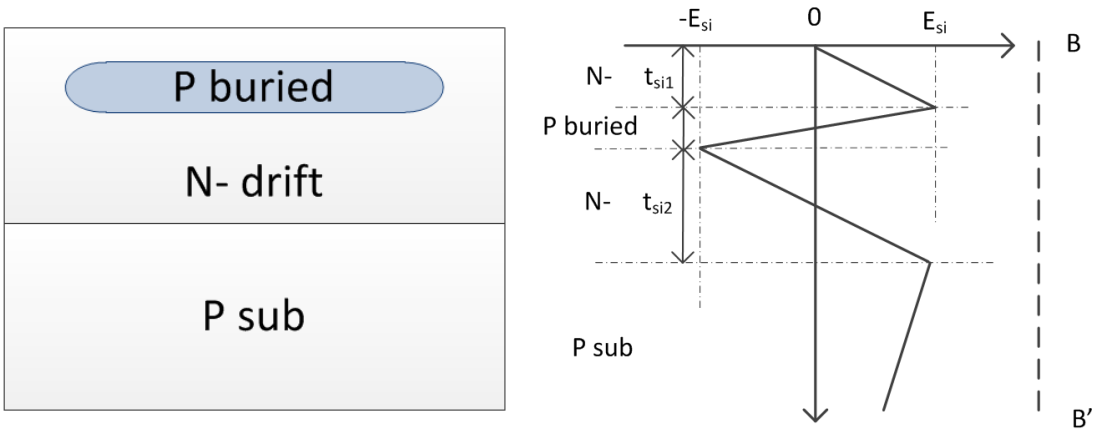

Figure 3.11. Triple RESURF layout (left) and the corresponding electric field along BB' when the drift region is fully depleted (right)

The added P-type region elevates the current by increasing the dose in the N-type drift region. However, this region itself does not allow electrons to pass in the on-state and hence the effective area for current conduction is smaller than the cross section of the drift region. To address this issue, a second gate can be introduced [107] to control the p pillar in their 3D RESURF design, forming a PLDMOSFET in parallel with the original NLDMOSFET. When both gates are fully turned on, an extra hole current will flow through the new transistor, accompanied by minority carrier injection in the n/p pillar

[107]. In this case, the LDMOSFET uses two carriers for conduction and this is referred to as bimodal mode [107]. Zhang et al. have implemented this concept experimentally in their 2D RESURF LDMOSFETs [108]. The structure is conceived based upon the triple RESURF design, with a p top layer being part of the slave PLDMOSFET [108]. In this case, the dose of the n-type top channel will be doubled and the same as that of the bottom channel [108]. This technology is termed Quadruple RESURF p-n bimodal conduction, which results in more than 30% increase in the saturation current compared to the case without the bimodal operation [108]. Despite this, some components need to be added to synchronise the two gates, such as a resistor, a current source, and a HV NMOS [108]. The price of these gate control units are the extra chip area and cost [108]. To operate this device more efficiently and safely, it was recommended that the turn-on action was performed for the N-gate first then P-gate, and that both gates were required to be turned off at the same time to the blocking voltage [108].

3.4.2.2 SOI

The RESURF conditions in traditional SOI are much stricter than that of bulk Si. This is because, in the off state, a large amount of negative charge gathers under the BOX layer at the drain side, descending towards the source [109]. This gives rise to a drastic difference in the RESURF dose requirement between the drain and source, which makes a uniform doping profile unfit for forming the optimal RESURF condition. One solution to this is to thicken the BOX layer so that the SOS capacitive effect is diminished [76]. Alternatively, the drift region can be engineered in such a way that the net doping increases linearly from the source to drain, for the purpose of charge balancing. As mentioned before, a PSOI structure could also be used, but this has mixed RESURF effects from the built-in PN and SOS structures. Here, only the LDMOSFET under the pure SOI (SOS) RESURF layout is described based upon [100] where an optimal linear doping profile is developed for a thin-film SOI architecture.

Starting with a 2-D Poisson's equation, one has:

$$\nabla E(x,y) = \frac{qN(x)}{\varepsilon_{si}}$$
$$\frac{\partial E_x(x,y)}{\partial x} + \frac{\partial E_y(x,y)}{\partial y} = \frac{qN(x)}{\varepsilon_{si}} \tag{3.2}$$

Where *N(x)* is the doping of the drift region as a function of lateral distance, ε_{si} is the Si permittivity with E_x and E_y being the horizontal and vertical component of electric field. This relation holds true within the depletion region. Since a lateral field under optimal RESURF conditions has a gradient of zero (see Fig. 3.12), Equation (3.2) becomes:

$$\frac{\partial E_y(x,y)}{\partial y} = \frac{qN(x)}{\varepsilon_{si}} \tag{3.3}$$

Assuming that the applied voltage and the resulting depletion length in *x* direction is V and W respectively (see Fig. 3.12), this also gives:

$$V = E_x \times W$$

$$\varphi(x,0) = \frac{Vx}{W} \tag{3.4}$$

Where $\varphi(x,0)$ is the surface potential within the deletion region ($0<x<W$).This variable can also be obtained in the vertical direction (Fig. 3.12 (right)):

$$\varphi(x,0) = \left(\frac{1}{2}t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \times t_{ox}\right) E_y(x,t_{si}) \tag{3.5}$$

Combining Equation 3.4 and 3.5, the *y* component of electric field at the bottom of the Si layer is:

$$E_y(x,t_{si}) = \frac{Vx}{W\left(\frac{1}{2}t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \times t_{ox}\right)} \tag{3.6}$$

Since this value drops linearly towards the surface of Si layer (Fig. 3.12 (right)), the vertical field at any location in the depletion region ($0<x<W$) can be formulated:

$$E_y(x,y) = \frac{Vxy}{W\left(\frac{1}{2}t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \times t_{ox}\right) t_{si}} \tag{3.7}$$

Substituting this to Equation 3.3, the optimal doping and its gradient at location *x* can be expressed:

$$N(x) = \frac{Vx\varepsilon_{si}}{qW\left(\frac{1}{2}t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \times t_{ox}\right) t_{si}} \tag{3.8}$$

$$\frac{dN(x)}{dx} = \frac{V\varepsilon_{si}}{qW\left(\frac{1}{2}t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \times t_{ox}\right) t_{si}} \tag{3.9}$$

Note that, this equation can also be satisfied by keeping $N(x)$ constant with other parameters being the variables as a function of x, such as $t_{si}(x)$ and $t_{ox}(x)$ [97]. In fact, the net effects of all these forms are the same—to create a linearly varying dose for charge balancing. Here, only the case described by Equation 3.8 is considered. For further information, please refer to [97].

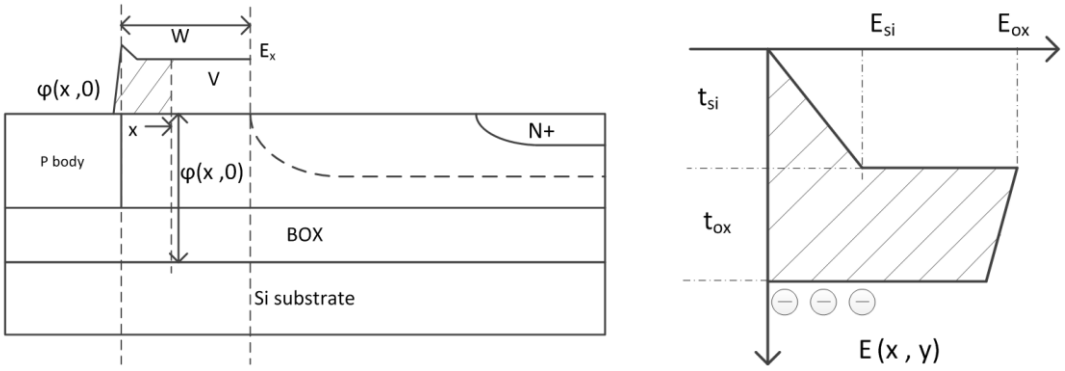

Figure 3.12. A 2-D SOI diode with the optimal RESURF condition under a reverse voltage of $\boldsymbol{V}$, having an electric field $\boldsymbol{E_x}$ in $\boldsymbol{x}$ direction throughout a lateral depletion distance of about $\boldsymbol{W}$ (left), and a electric field distribution at location $\boldsymbol{x}$ highlighted in the device (right)

If the drift region is sufficiently long, the avalanche breakdown will take place in the Si layer under the drain. Assuming that a relatively thick layer (>10 μm) is present, the multiplication effect in SOI is similar to that in bulk Si and hence the critical field value will be equal to about 3×10^5 V/cm. Nonetheless, this boundary condition will underestimate the blocking capability of SOI structures with a sub-micron (<1 μm) film. The reason is that the avalanche effect becomes insignificant in such thin vertical distances [110]. In this circumstance, the breakdown field is adjusted to about five times higher than the customary value, for initiating the avalanche process [110]. This unique feature in SOI gives rise to a parabolic dependency of blocking voltage on the thickness of the Si layer, as can be seen in Fig. 3.13 from [100]. If the Si layer is below 1μm and above 10 μm, the breakdown limit rises for a SOI structure with a 2 μm BOX. The increase on the left is more drastic than the one on the opposite side, regarding the Si layer thickness in logarithmic scale. For high temperature operation, it is desirable to use a SOI wafer with a sub-micron Si film due to the reduction of the leakage and ease of electrical isolation. However, dielectric breakdown can occur [100] and interfacial effects can be significant in a thin film, which limits the minimum Si layer thickness.

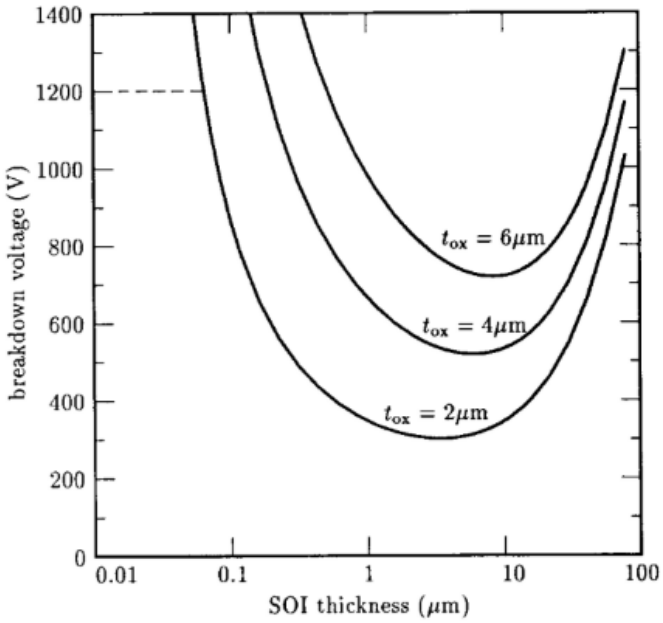

Figure 3.13. The relationship between the breakdown voltage and thicknesses of the Si and BOX layer in SOI devices, taken from [100]

3.5. On-resistance & Saturation current

The total on-state resistance of a LDMOSFET comes mainly from the channel and the drift regions. If high gate-source bias V_{GS} is applied to a high voltage ($BV_{DSS} \geq 200$ V) Si LDMOSFET, the drift region contributes the most in the on-state resistance. The conditions to measure this resistance depend on how the transistor is used. Fig. 3.14 shows one example where different standards can apply to the low and high-side LDMOSFETs for extraction of on-resistance. In both cases, the substrate is grounded and the V_{GS} biased to a certain level (e.g. +10 V in [111]) for minimising the channel resistance. However, they differ in the substrate-to-source voltage, which is zero in the low-side and a negative value in the high-side (e.g. -400 V in [111]), respectively. The V_{DS} bias for the on-resistance in the high-side configuration can be a small value similar to the low-side case (e.g. 1 V in [112]), or up to 15 V where the LDMOSFET enters saturation mode [111] [113]. In this case, the device performance is judged manly by the saturation current whose magnitude is strongly related to the built-in JFET [114]. This parasitic structure reduces the effective area for current conduction, which can be counteracted by using a high-resistive substrate [96], increasing the thickness of the Si layer [114] or/and the RESURF dose [115].

The on-resistance of a HV LDMOSFET usually exhibits a positive temperature coefficient, but the opposite can happen if the dose in the drift region is low and temperature sufficiently high [116]. In this work, a positive temperature coefficient is seen in the simulated structures due to the relatively high RESURF dose in the drift region. The main reason for the temperature dependency is that the Si atoms release more phonons at high temperature, which interacts with charged carriers and lowers their mobility [117]. One way to mitigate this effect is to add more dopants into the lattice. It is true that this method will decrease the mobility [117] and can also reduce the breakdown voltage.

However, the conductivity in this scenario is influenced more from the quantity of carriers instead of the quality (mobility). If the doping is high enough, the thermally-generated carriers will be insignificant and therefore the on-resistance is less sensitive to temperature. By implementing RESURF technologies as mentioned earlier, the degradation of the breakdown voltage will be minimised and a HV LDMOSFET that is robust against temperature is achieved.

Depending on the V_{GS} bias, temperature can affect the saturation current differently. At low V_{GS} value (<4 V [116]), the saturation current goes up with higher temperature but an opposite relationship can occur at high V_{GS} (>4 V), resulting in a zero-temperature-coefficient (ZTC) point [116]. In this thesis, the high V_{GS} bias (≥ 10 V) is used to reduce the channel resistance and highlight the effect of RESURF dose on device performance.

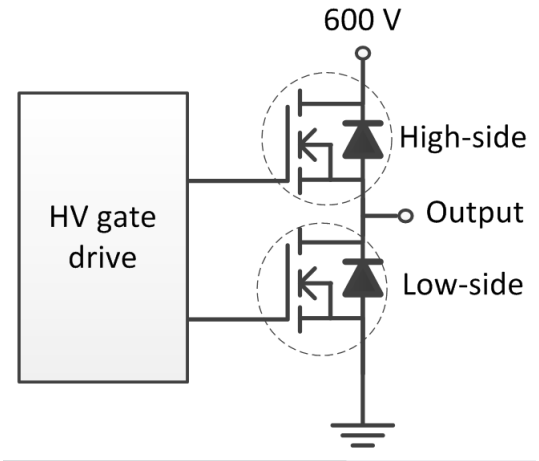

Figure 3.14. A half bridge circuit consisting of a HV gate drive block, a low-side and high-side N channel LDMOSFET

Chapter 4 TCAD models verification and discussion

4.1. Introduction

The aim of this chapter is to apply the theory mentioned in Chapter 3 to Technology computer-aided design (TCAD) models, and validate them by using the experimental results of the Philips SOI LDMOSFETs. The first section introduces the SILVACO TCAD package, covering its software functions and methodology. Secondly, the references used for model benchmarking are evaluated, with the validation carried out by two SOI LDMOSFETs in Philips technology. In Appendix C, the transferability of the models to the Si/SiC architecture is analysed with the literature and our wafer bonded results. The thermal model for self-heating are discussed and arranged in Appendix A.

4.2. TCAD software

TCAD simulation is a powerful method to develop and optimise semiconductor devices for specific applications. SILVACO software package is one of those able to deliver such methodology. This simulator contains a variety of Si-based models that are verified by experiments, and can characterise the electrical, optical and thermal behaviour of different materials. Also included are the DC, AC and transient modelling, which can examine and compare different designs. Process simulation in this software provides a reliable and convenient way for users to set up a draft for device fabrication. The built-in SPICE models can further examine the devices' behaviour in a circuit under different conditions. The implementation of such multifunctional TCAD forms the initial step of device development and lays a theoretical foundation for the subsequent stages.

Generally speaking, the input of the TCAD software is a structural file where the device parameters are stored, such as the 2D geometry and doping profile. To obtain the

solution, the structure will be discretised into a mesh and divided into a finite number of elements. Each element has a set of equations to mathematically describe the physical mechanisms within. If the boundary conditions and initial guess is given, those equations will be solved by direct or iterative methods until the convergence criteria are met. Finally, the results of all equations are assembled to represent the behaviour of the entire system. The procedures mentioned above are referred to as finite element method (FEM).

FEM approximates real device behaviour and undoubtedly produces errors arising from mesh definition, model configuration, numerical methods and convergence criteria. Through use of the guide, and the many examples available in SILVACO, the user can acquire basic knowledge of how to design a mesh layout and configure the numerical solver correctly, for increasing the simulation accuracy and efficiency. The model selection and implementation, however, not only demands computing skills, but also a deep understanding of semiconductor physics. In order to deliver convincing results, the parameters of the models must be compared to those in related references and adjusted according to the available evidence. This sets up a benchmarked standard in the simulation, allowing the users to establish a structure with optimised settings and the minimum mesh/nodes so that the program can be run in a timely but accurate fashion, delivering usable data. If necessary, new models will be developed from such benchmarking, to achieve a better fit between the simulation and experimental outcomes. The next section will detail this procedure for the simulated SOI and Si/SiC structures.

4.3. Model benchmarking

SILVACO considers various physical mechanisms, and many of them can be described with different models. The selection of these models for one specific physical mechanism is subject to conditions, which can produce subtle but appreciable differences in the simulation. The designer first needs to have an appreciation of the expected physical behaviour of the targeted structure. This information can be obtained through the literature review and/or experimental prototypes. Secondly, the models for the same physical effect will be examined and compared via references, from which the most suitable one is chosen. Once this is done for all the physical effects, the simulation will have a higher chance to produce reliable outcomes, and be finished with fine-tuning against the references. In some circumstances, the selected models are not compatible

with each other and the program will end with numerical errors. The response to this is to search for the problematic models, redefining the mesh, and model settings. If the issue still exists, a less adequate model will be selected and the simulation program re-executed. This is an iterative process that is only complete once the simulation data suitably replicates that from references.

It can be seen that reference data are of paramount importance in device modelling. Prior to a TCAD study on Si/SiC LDMOSFETs, it is necessary to engage in an exercise of reverse-engineering, to establish structures in SILVACO, carefully analyse the models and evaluate simulation results against the experimental data in the selected references. Among many articles on Si-based power LDMOSFETs, those by Philips Research group [46] [100] [110] [118] were utilised for benchmarking the simulated Si/SiC transistors. The first reason is that to the best of our knowledge, only those papers contain the information on the experimental behaviour of 600-700 V LDMOSFETs in DI and JI technology, over the temperature range of 27-300 °C. These are what most of the related papers cannot offer as they mainly focused on power transistors working at room temperature. Therefore, the models in SILVACO can be verified and deliver cogent outcomes over a wide temperature range. Secondly, the Philips SOI LDMOSFETs feature a low on-resistance and a leakage current of only 1.5 nA/μm at 300 °C [46], which are remarkable in terms of high temperature operation. Using this device as a comparison revealed several pros and cons of the Si/SiC architecture. Thirdly, the physical models for their devices are well-documented in the references [46] [110] and, more importantly, are available in SILVACO simulators, which significantly reduces the time spent on model selection. In addition, nearly all these models are developed by one developer, Klaassen [119], thereby reducing the risk of incompatibility during simulation. Fourthly, there is a unique feature in the Philips SOI transistor, which is the appearance of tunnelling leakage at about 450 V [110]. This can be one indicator of how close the simulated device and the one by Philips are. Fifth and finally, the Philips LDMOSFETs can be transformed into LIGBTs [111] [113] or lateral thyristors [120] with only small changes. These reasons make the Philips framework the ideal starting point for defining a robust model for the Si/SiC LDMOS, while they are also the ideal device to benchmark the Si/SiC technology against.

4.3.1. The first benchmark structures (600 V)

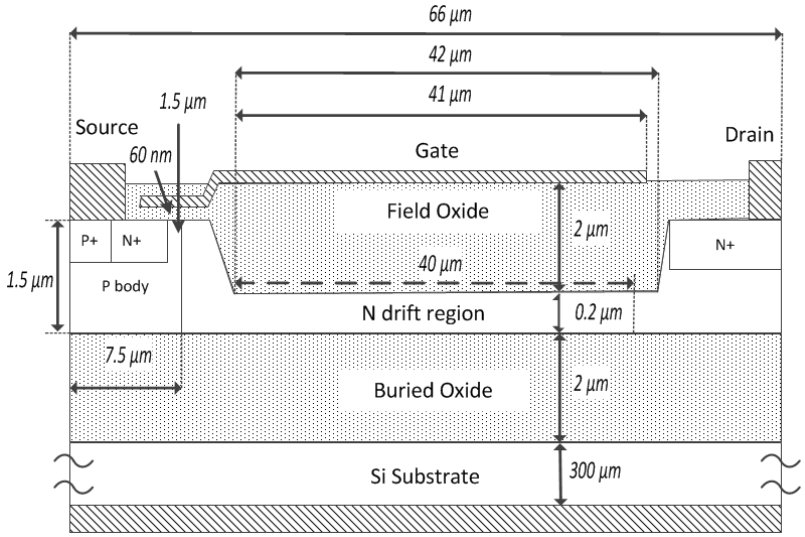

Figure 4.1. One of the Philips SOI transistors [46] used in SILVACO for benchmarking, where the key parameters are indicated

The 2-D schematic of the Philips 600 V LDMOSFET is shown in Fig. 4.1 and established in SILVACO based upon [46]. In practice, this embodiment is formed by Philips 'EZ-HV' fabrication process [121], which combines these high voltage devices with the control CMOS on the same chip. The LDMOS layout employs a SOI wafer consisting of a 1.5-µm Si layer, a 2-µm buried oxide (BOX) and a 300-µm Si substrate with n-type doping of 1×10^{15} cm^{-3}. The active area has 66 µm in length and an N drift region 0.2 µm thick and 42 µm long. This thinned-down region is created by local oxidation of Silicon (LOCOS) process [121], which also yields a 2 µm field oxide layer (FOX). On top of this dielectric layer is a gate contact terminated 1 µm away from the end of the thinned-down region. The gate electrode also covers a 60-nm gate oxide over a channel region, which has a p-type doping of 6.5×10^{16} cm^{-3} and 7.5 µm in length. A N+ region is placed 1.5 µm away from the right border of the p body, whereby the channel length is defined. The drain and source metal are deposited on highly-doped regions for ohmic contacts.

A linear doping profile starts from the onset of the thinned-down region, extending 40 µm towards the drain side (see Fig. 4.1 the dashed line). As mentioned in Chapter 3, this doping distribution can be obtained by using Equation 3.9 as long as all its variables are

known. However, it has to be pointed out that the Si layer thickness (t_{si}^{*}) used in Equation 3.9 will be half of the physical value (t_{si}) in the simulated structure. This is because the depletion from the BOX or FOX side just needs to occupy a 0.1-μm-thick Si layer. This effectively doubles the impurity dose in the Si layer. As indicated in Fig. 3.13, a 600 V SOI device with t_{ox} = 2 μm requires a Si layer thinner than 0.25 μm, which is met by the geometry of the simulated structure. As a result, the gradient of the linear doping profile is attained (see Fig. 4.2) with the following values:

$$V = 600\,V, W = 40\ \mu m, t_{si}^{*} = 0.1\ \mu m, t_{ox} = 2\ \mu m, q = 1.6 \times 10^{-19}\,C,$$

$$\varepsilon_{ox} = 3.45 \times 10^{-13}\,Fcm^{-1}, \varepsilon_{si} = 1.04 \times 10^{-12}\,Fcm^{-1}$$

$$\frac{dN(x)}{dx} = \frac{V\varepsilon_{si}}{qW\left(\frac{1}{2}t_{si}^{*}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}\times t_{ox}\right)t_{si}^{*}} = 1.6 \times 10^{20}\ cm^{-4} \qquad (4.1)$$

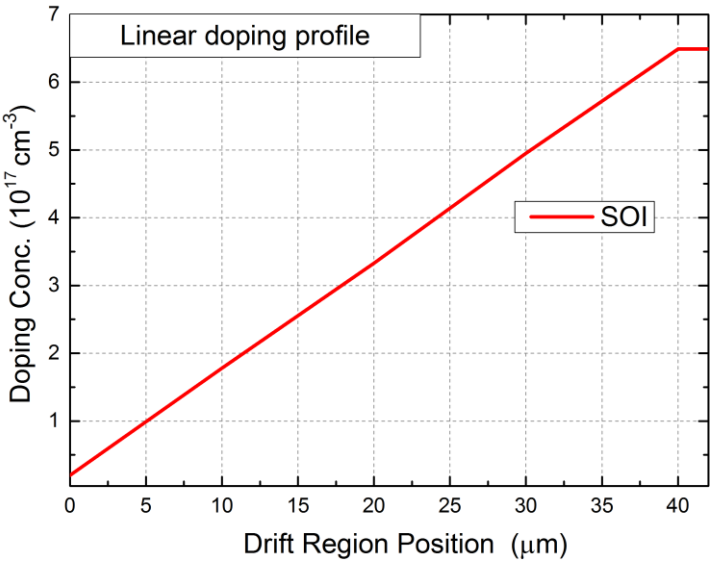

Figure 4.2. The linear doping profile of the simulated SOI LDMOSFET

Apart from this linear profile, there exists a base doping value (N_b) in the drift region. As long as N_b is small relative to $N(x)$, the total doping value ($N(x) + N_b$) still results in a blocking voltage of at least 600 V. The reason is that the spacing between the p body and

drain is longer than the thinned-down region, which provides some extra room for the blocking capability. In this structure, the base doping is set to $2x10^{16}$ cm^{-3} and the effective dose in the drift region is:

$$Q_{eff} = N_b t_{si} + \frac{1}{2}\frac{dN(x)}{dx} \times W \times t_{si} = 6.8 \times 10^{12}\ cm^{-2} \quad (4.2)$$

In [46], Klaassen physical models are used to analyse the high temperature performance of the bulk Si and Philips SOI LDMOSFET. According to this, the models are applied in the simulation and comprise of Darwish CVT, KLASRH, KLAAUGER, BBT.KL and BGN2 [122]. The Darwish CVT integrates the Klaassen mobility models with a new expression for surface roughness [122]. The lattice scattering factors, THETAN. KLA and THETAP. KLA, are configured to 2.8 to match the temperature-dependent mobility values in [46]. The generation and recombination mechanism is taken into account by the KLASRH and KLAAUGER models, with carrier lifetimes adjusted to 1.5 μs [46] [123]. The BBT.KL is activated to consider the band-to-band tunnelling in the Philips SOI devices [110]. The band gap narrowing effect is enabled by BGN2 with Klaassen default parameters. Supplementary to this Klaassen setup is FLDMOB for velocity saturation, FERMI for Fermi-Dirac statistics and SELB for avalanche breakdown [122]. For the full mathematical forms of the used models, please refer to [122].

Sandwiched by FOX and BOX, the 0.2 μm layer in the Philips SOI suggests an increase in leakage current due to the Si/SiO_2 interfacial states. Nevertheless, the experimental measurement by Philips shows that the effect of Si/SiO_2 interface charge on the device is insignificant, due to its value being just $+4\times10^{10}$ cm^{-2} [124]. This value is so low that the RESURF dose is hardly disturbed. In this simulation, the interface charges of Si/BOX and Si/FOX are set to $+4\times10^{10}$ cm^{-3} as in [124]. It is worth noting that some configurations may be different from those of the Philips device because not all parameters are mentioned in [46]. However, similar outcomes are found in the simulations, as shown below.

4.3.1.1 Off-state characteristics

Fig. 4.3 shows the potential distribution of the benchmark structure at the onset of avalanche breakdown (670 V). Although the linear doping profile of the Philips SOI [121] stops at a different location compared with the simulated transistor (See Fig. 4.3), their

potential contours have a very similar pattern. Fig. 4.4 demonstrates that the potential at the middle of the drift region increases linearly, and that the electric field is saturated at 1.5×10^5 V/cm in most of the thinned-down region. These two indicate that a very good RESURF effect is created for the structure. It is worth noting that in this design, potential lines crowd in the field oxide at the end of the field plate. This will enhance hot carrier injection and therefore reduce the reliability.

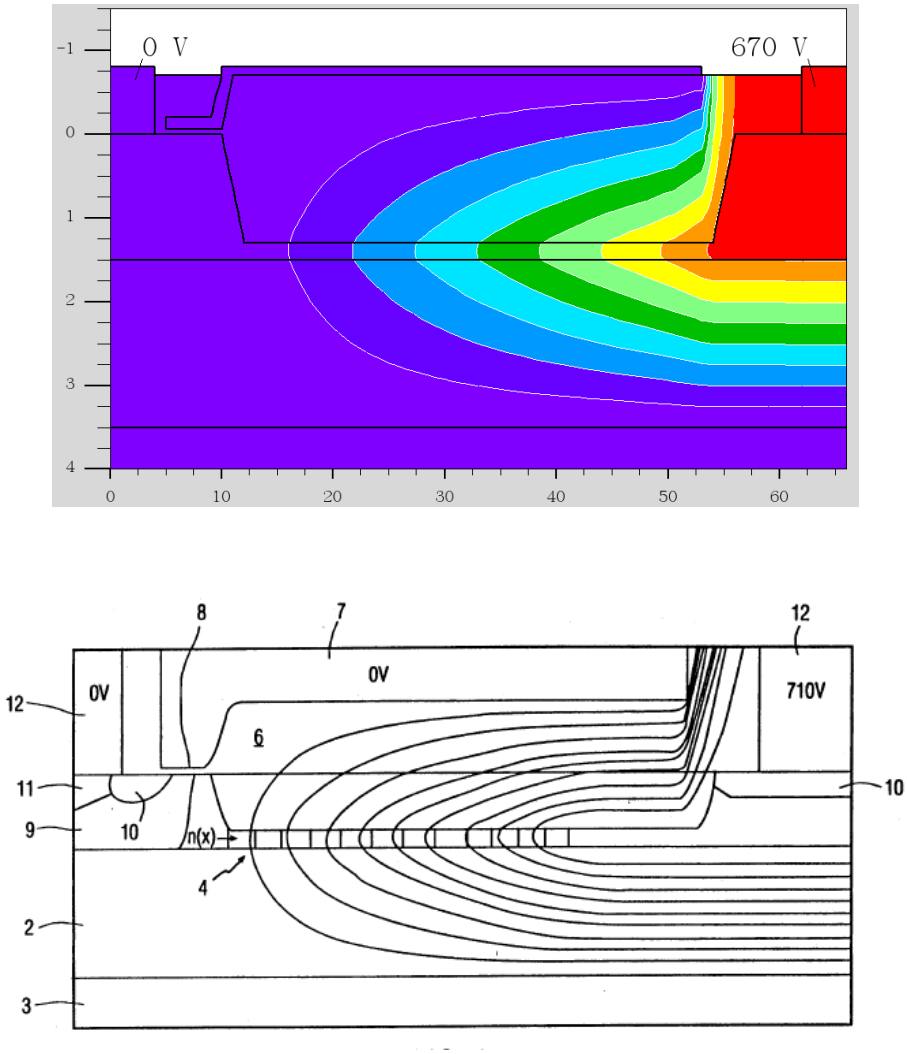

Figure 4.3. The potential contours of the benchmark LDMOS (top), and the Philips SOI (bottom) [121], on the verge of avalanche breakdown. (axes units: μm)

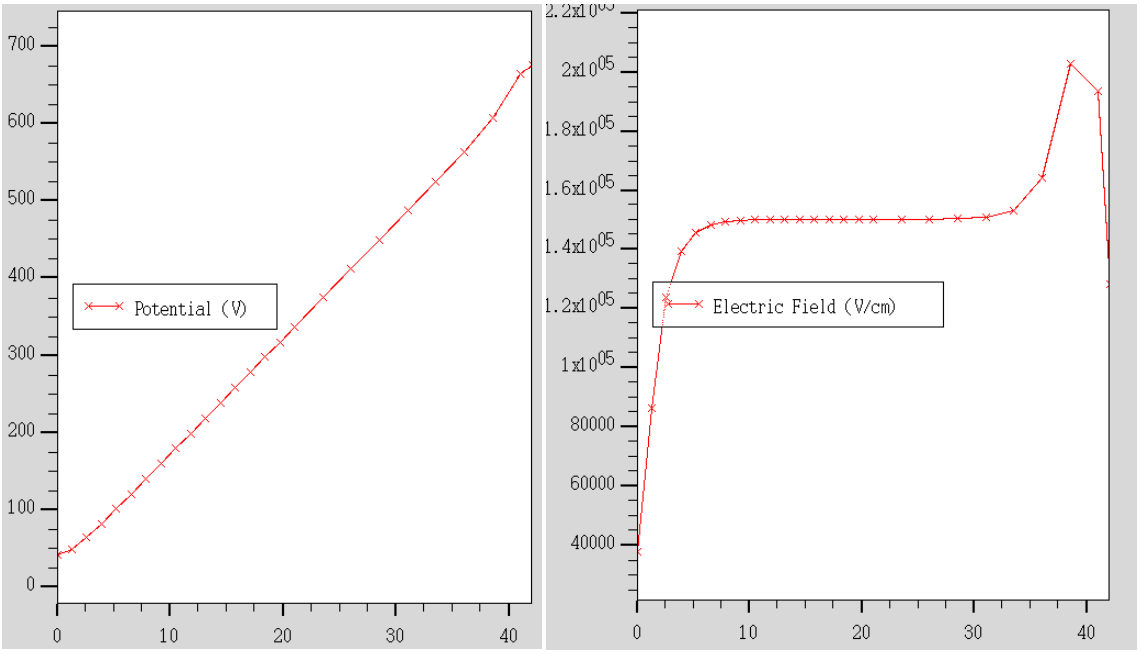

Figure 4.4. The potential and electric field at the middle of the N drift region, at the onset of avalanche breakdown

As can be seen in Fig. 4.5, the simulation closely replicates the off-state behaviour of the practical Philips SOI at room temperature and 200 ^{0}C. One can find that the curves produced by the simulation are more similar to those in [110] (See Fig. 4.5 bottom), where the tunnelling effect is thoroughly studied by Philips. Owing to band-to-band tunnelling [110], the leakage at 27 ^{0}C goes up more rapidly after 450 V, and eventually avalanche breakdown happens at 670 V. However, this cannot be observed in the curve at 200 ^{0}C, due to the tunnelling being overshadowed by the generation mechanism [46].

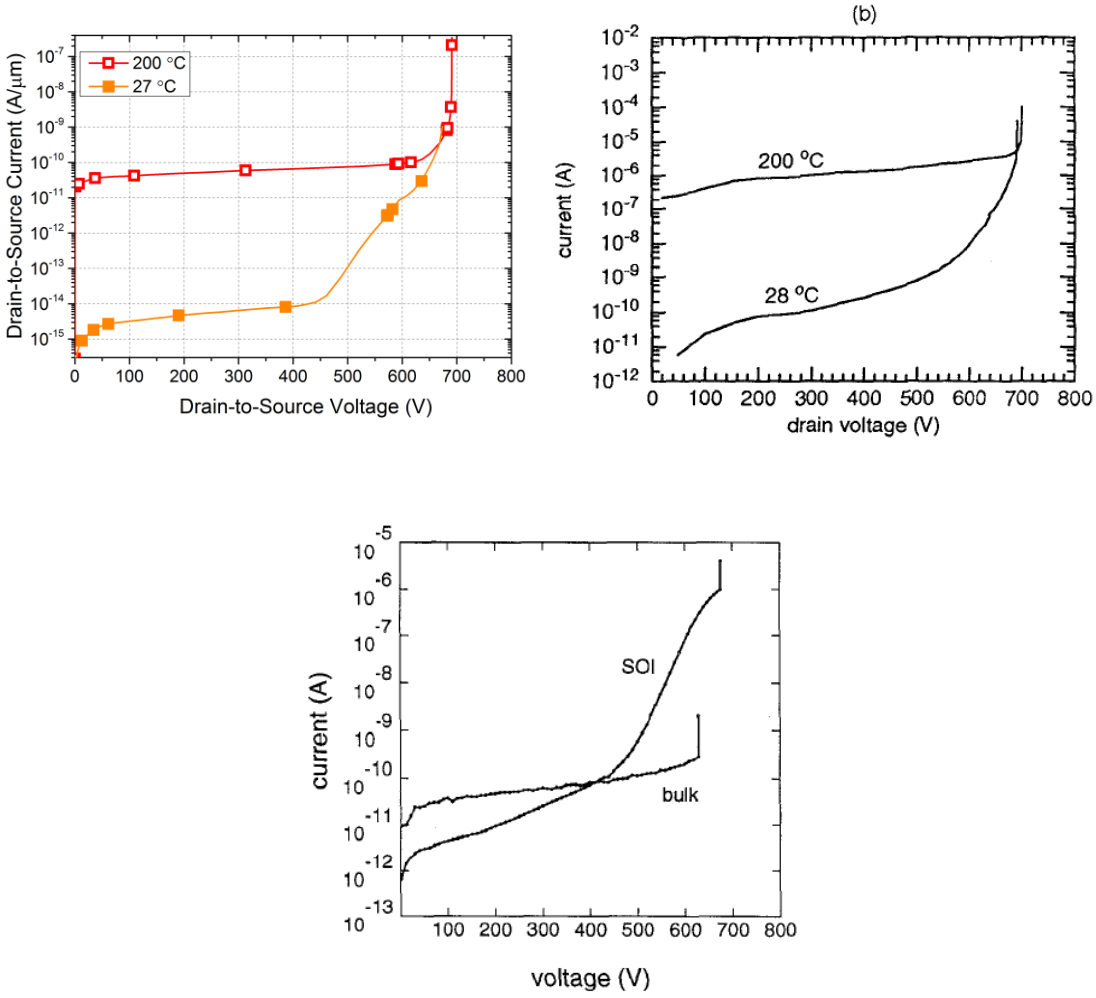

Figure 4.5. Off-state characteristics of the simulation SOI (Left) and the Philips SOI (right) [46], at room temperature and 200 ^{0}C. The bottom graph from [110] is more similar to the simulation result

In [46], the relationship between the leakage current and temperature is analysed by using Equation 4.3:

$$I_{dark} = \frac{q\boldsymbol{n_i}V_{dep}}{\tau} + \frac{qA\boldsymbol{n_i^2}}{N_A}\left(\frac{\mu kT}{q\tau}\right)^{\frac{1}{2}} \tag{4.3}$$

Where τ is the effective lifetime, V_{dep} the depleted volume, A the lateral area of the neutral region bordering the space-charge region, $N_A$the doping, μ the electron mobility in the neutral region, k the Boltzmann constant and n_i the intrinsic carrier density as a function of temperature T [125]:

$$n_i = 3.1 \times 10^{16}\, T^{3/2} \exp\left(-\frac{0.603q}{kT}\right) \tag{4.4}$$

In the simulation, Equation 4.4 is approximated by implementing the following two formulas:

$$n_i = \sqrt{N_C N_V} \exp\left(\frac{-E_g(T)}{2kT}\right) \quad [122] \tag{4.5}$$

$$E_g(T) = 1.206 - 2.73 \times 10^{-4}\, T \tag{4.6}$$

Where N_C and N_V are referred to as effective density of states for electrons and holes [122].

Equation 4.3 only takes into account the generation (first term) and diffusion leakage (second term), excluding the expression for band-to-band tunnelling [46]. Nonetheless, this is a very good approximation of the leakage as in practice, a 600 V device will be operated at $V_{DS} = 300\ V$, a bias condition where the tunnelling component is negligible. This bias also induces full depletion in the LDMOSFETs using SOI and bulk-Si substrate [46], which means that the generation components for both cases start to saturate. This allows a fair comparison between the Philips SOI and bulk Si technology, regarding their total leakage over a wide temperature range. Therefore, Arnold et al. measured the leakage current under this condition for their transistors, at temperature up to 300 °C (see Fig. 4.6 right) [46]. They also analysed the bulk Si transistor and extracted its diffusion and generation component, highlighted by a dotted or dashed line in Fig. 4.6 right. Through comparison, it can be found that the rise of SOI leakage has little to do with the diffusion mechanism.

In our simulation, the $\propto n_i^2$ and $\propto n_i$ line are used to represent the diffusion and generation mechanism, respectively (see Fig. 4.6 left). The correlation between n_i, n_i^2 and the leakage components can be observed in Equation 4.3, highlighted in boldface. The SOI leakage is raised following the $\propto n_i$ line up to 200 °C, above which the curve is bent upwards and its increased rate approaches that of the $\propto n_i^2$ line. This signifies strong carrier diffusion at high temperature, which is different from the experimental results in [46].

This phenomenon is not uncommon in LDMOSFETs, as demonstrated in [126] [116] where the transition from generation to diffusion mechanism starts at about 150 °C. There are two possible explanations for the divergence between the simulation and experimental results by Philips [46]. First, the Klaassen models were only calibrated up to 500 K [122], which creates uncertainty for the simulation results above that temperature. However, the implementation of these models up to 573 K is evident in [46]. Secondly, Arnold et al. mentioned that according to [127], the leakage current decreases faster-than-linearly with thickness, for the very thin SOI layer [124]. Based upon Equation 4.3, the finding implies that the layer thinning results in a drop in the intrinsic carrier density n_i, as this act decreases V_{dep} linearly and does not have a strong influence on the generation lifetime τ [123] (the recombination lifetime will be affected though). In [128], Nakagawa et al. reported that the experimental leakage current of their SOI devices was more than one order of magnitude smaller than the calculated value, and that SOI leakage shrunk effectively with the thickness of Si layer. It can be suggested that the bandgap and density of states become less sensitive to temperature in the thin SOI layer, which translates into a diffusion process less noticeable at high temperature. Unfortunately, there is no model available in SILVACO to describe this effect and hence the leakage current above 200 °C can be overestimated. However, the model setting provides a good data fitting in general for the off-state characteristics, and this is less problematic than underrating the leakage as doing so can predict a maximum operating temperature unreachable by the practical devices.

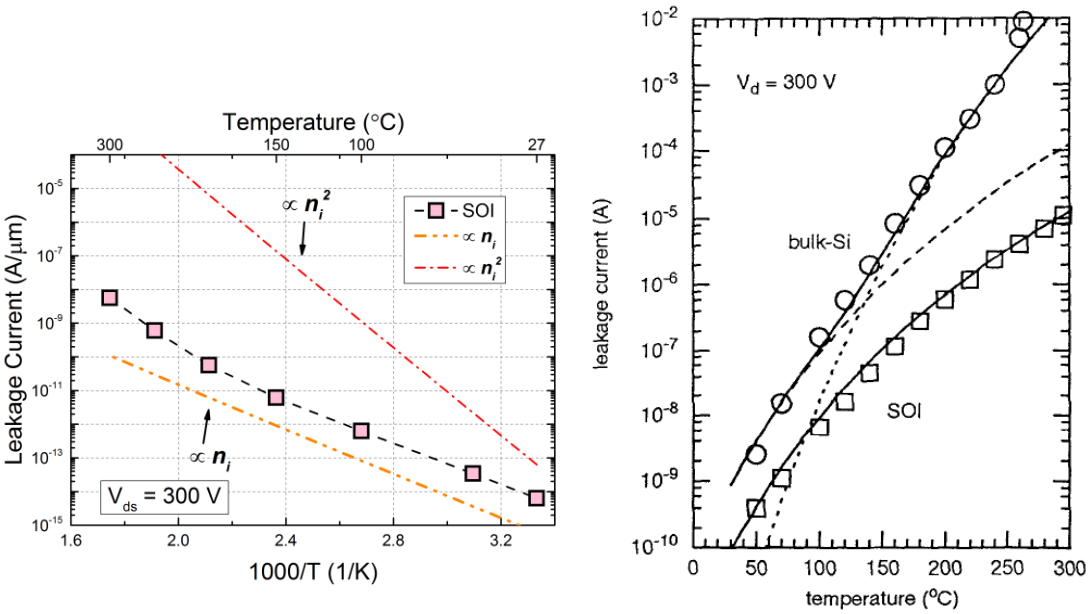

Figure 4.6. The temperature dependency of leakage current at V_{DS} = 300 V for the simulated structure (left), and the Philips SOI [46] (right). In the right figure, the dotted and dashed line indicate the diffusion and generation component, respectively

4.3.1.2 On-state characteristics

Fig. 4.7 and 4.8 show the influence of temperature on the threshold voltage and on-resistance, for the benchmark device and the Philips SOI. It can be seen that there is little difference between them in both graphs. The specific resistance is modelled under the conditions of $V_{gs} = 15\,V, V_{DS} = 1\,V$ and $V_{sub} = V_S = 0\,V$, a setting for low-side operation. Then this value is converted to on-resistance by the equation below, over the temperature range of 27 – 300 °C:

$$R_{on} = \frac{R_{sp}}{W \times L} \tag{4.7}$$

Where W and L are the width and length of the simulated device, respectively. As indicated in Fig. 4.1, the length is 66 µm and the width 8 mm as in [46]. It is worth noting that the drain and source contact area will affect the value of on-resistance. In conclusion, the Klaassen models used in SILVACO reproduce most experimental data from [46], which is essential to the comparative study on the SOI, bulk Si and Si/SiC.

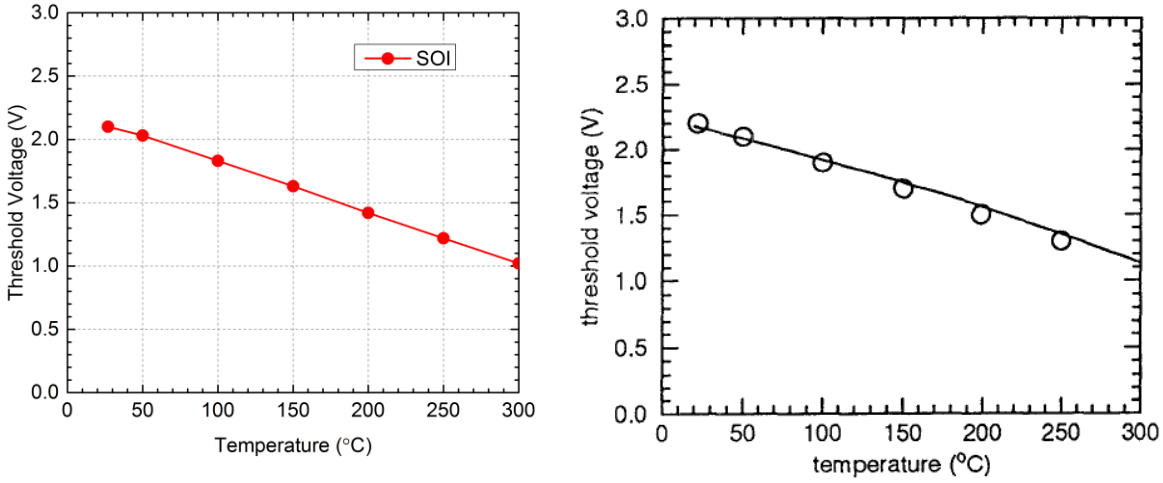

Figure 4.7. The threshold voltage vs temperature for the simulated structure (left) and the Philips SOI (right) [46]

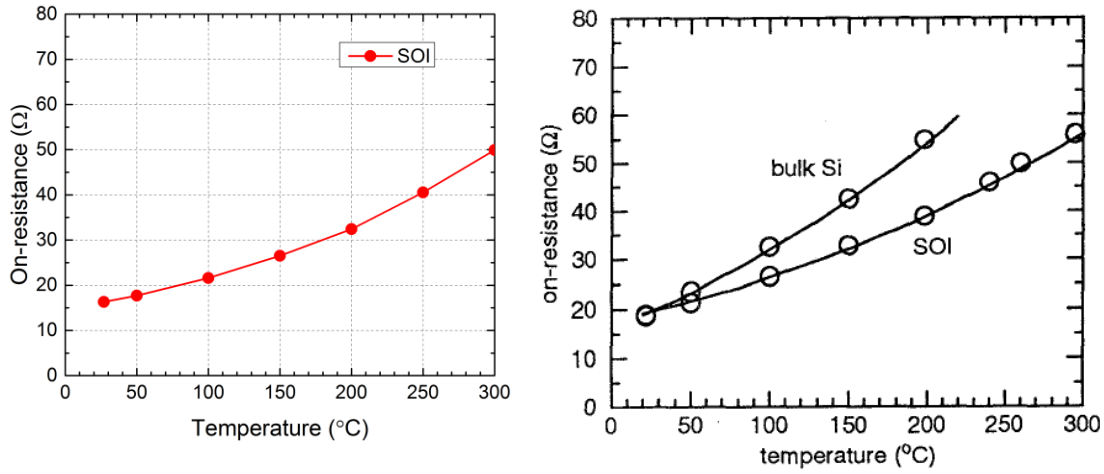

Figure 4.8. The low-side resistance vs temperature for the simulated structure (left) and the Philips SOI (right) [46]

4.3.2. The second benchmark structure (~200 V)

This section studies another Philips LDMOS design with a blocking voltage of 190 V [129], a value that corresponds to the lower limit of the Si/SiC devices to be developed (~200 V). According to [129], the structure is created in SILVACO and is a more compact version of the aforementioned 600 V transistor (see Fig. 4.9). For achieving 190 V breakdown voltage (see Fig. 3.13) with a double RESURF effect [129], the 1.1 µm Si

layer is thinned down to 0.6 μm in the drift region. Both FOX and BOX are 1 μm thick. In additions, the lengths of the linear doping profile, gate extension and the spacing between the P body and N+ drain are set to 6.5, 9.8 and 12 μm, respectively. The doping of the drift region is arranged in a manner similar to the 600 V case by using Equation 3.9. The gate oxide is 30 nm thick and the channel length is 1.5 μm. The p body region is 8 μm wide and has a doping density of 8×10^{16} cm^{-3}. The chip area is 22.5 μm in total, with other settings (e.g. carrier lifetime) the same as previous. Again, some parameters are deduced from [129] and maybe different from those used by Philips.

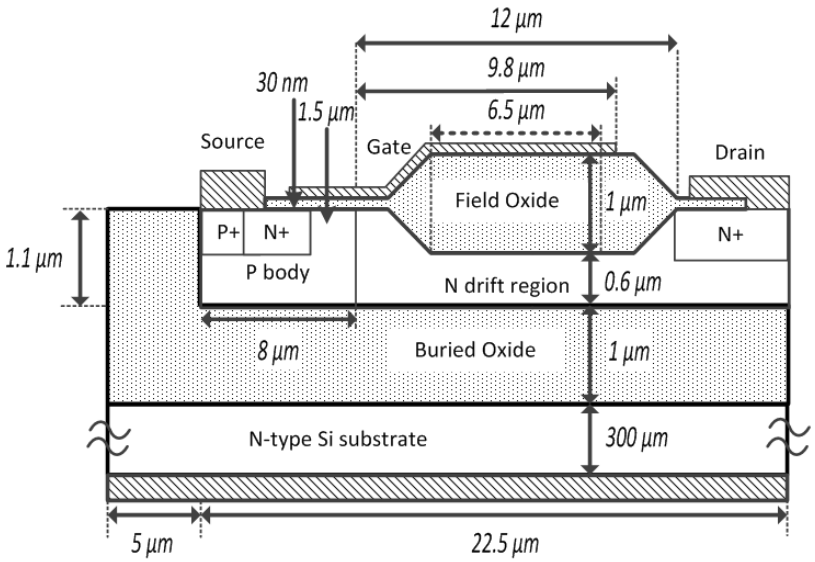

Figure 4.9. The second benchmark structure based upon [129], with a blocking voltage of 190 V

Under these settings, the potential is evenly distributed in the drift region of the simulated device at 190 V (See Fig. 4.10). The gradient of leakage current is constant from 50 V to the onset of avalanche breakdown, with no tunnelling observed. This is because the electric field in the 0.6 μm layer is not high enough to trigger band-to-band tunnelling. Similar to the Philips device in [129], the threshold voltage is about 1.2 V at $V_{DS} = 0.1\ V$ and the saturation current approximates to $250\ mA/mm$ at $V_{gs} = 12\ V$ (see Fig. 4.11). However, the extracted on-resistance ranges from 567 to 620 mΩmm^2 at V_{DS} biases up to 1 V, higher than that (510 mΩmm^2) in [129]. This indicates that there still exist some differences between the simulated and Philips LDMOS layout. One cause of the disparity can be the sizes of the channel and drain region, which affect the calculation

of on resistance. Nevertheless, their other properties are near identical so this benchmark structure is deemed a good duplicate of the Philips 190 V design.

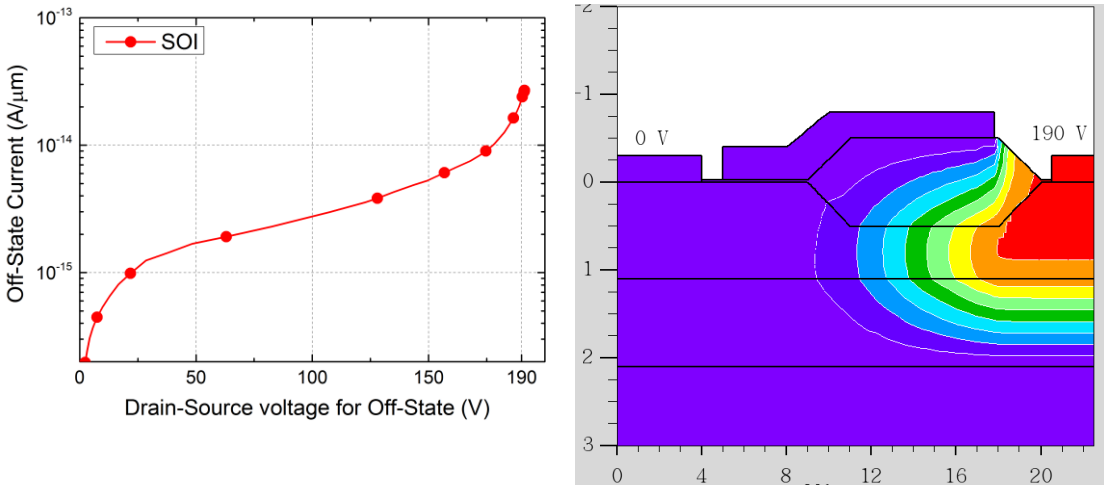

Figure 4.10. The off-state I-V curve (left) and potential distribution (right) at the onset of avalanche breakdown and 300 K, for the simulated structure (axes unit: μm)

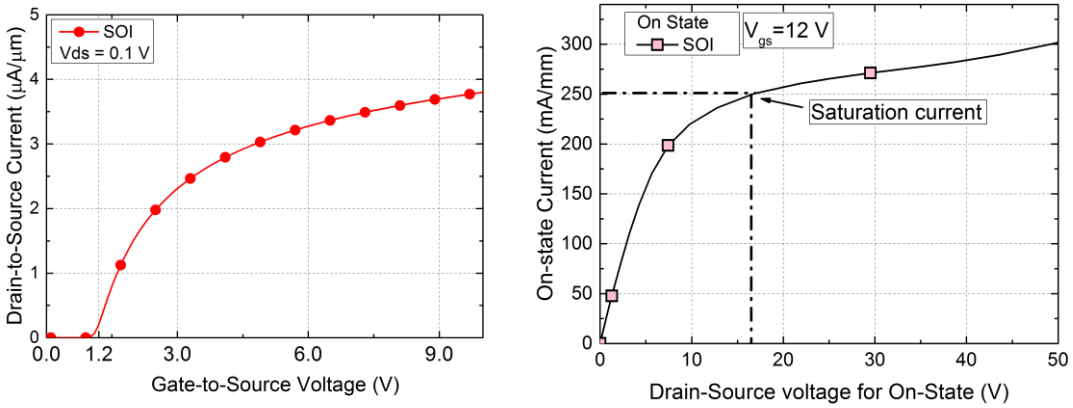

Figure 4.11. The $V_{GS} - I_{DS}$ curve at $V_{DS} = 0.1\ V$ (left) and the on-state characteristics at $V_{gs} = 12\ V$ (right), for the simulated structure

4.3.3. Conclusion

To sum up, the FEM model that will be used in Chapter 5 have been benchmarked with two SOI LDMOSFETs in Philips technology. The changes of the parameters in this model for the Si/SiC case can be found in Appendix A&C. By applying this

configurations, a like-for-like comparison can be performed between the Si/SiC and SOI transistor in Chapter 6 & 7.

Chapter 5 RESURF Si/SiC LDMOS designs and simulation setups

5.1. Introduction

This chapter is aimed to introduce the RESURF Si/SiC LDMOSFETs and modelling setups that will be used in the Chapter 6&7 where the simulation results are presented. Preceding the description of the RESURF Si/SiC transistors, a preliminary TCAD study is given on non-RESURF PiN diodes to build up the basic knowledge of the Si/SiC structure. The content of this study has been published in [132]. Having understood the fundamentals, the simulated Si/SiC LDMOS topologies are then presented, which are optimised based upon the RESURF theory mentioned in Chapter 3. Their bulk Si, PSOI and SOI equivalents will also be described. The first to be demonstrated is a 600 V Si/SiC LDMOSFET with a SOI RESURF layout. The second Si/SiC LDMOS structure is also rated at 600 V, but designed with a PN RESURF layout. The third is conceived with the same technology as the first, albeit the blocking voltage is reduced to 190 V. The last section of this chapter is dedicated to the simulation setups for the LDMOSFETs. The application of the physical models discussed in Chapter 4 and Appendix C will first be described and followed by the introduction of the switching circuits used for transient simulation.

5.2. Si/SiC non-RESURF PiN diodes

The goal of this section is to investigate the Si/SiC architecture at a fundamental level, without considering the RESURF effect. This is achieved by simulating several PiN diodes which are simple, free from strong RESURF effects and only differ in the substrate. There are two parts in this study. The first simplifies the PiN diode down to a heat source

on multiple substrates of interest, namely Si/SiC, SOI, Si/SiO_2/SiC, bulk Si and SiC. DC thermal simulation is performed on these substrates, by solving the lattice heat flow equation (details in Appendix A) and neglecting the effects of thermal radiation and hot carriers. The second simulation considers the detail layout of the PiN diodes in SOI and Si/SiC architectures, with the comparison of their results regarding forward and reverse I-V behaviour as well as the effect of device geometry on the breakdown voltage.

5.2.1. Thermal simulation of the substrates

In this simulation, the PiN diode is represented by a 100×100×1 μm^3 cuboid with a power dissipation of 0.1 W [78]. This heat source is centred on a 500×500×100 μm^3 substrate with an Al back contact at a fixed temperature of 300 K. As such, no electrical action will be performed by the diode and only the self-heating model is activated. Fig. 5.1 illustrates such thermal models for a SOI and Si/SiC substrate, where the different layers and their thicknesses are presented. From top to bottom, the SOI is structured with a 1 µm Si layer, a 1 µm BOX, a 98 µm bulk Si and 1 µm Al region. The same applies to the Si/SiC, except for the BOX and bulk Si being replaced with a 99 µm 6H-SiC. The thermal conductivity of each region is specified as in Appendix A. It can be seen that the temperature in the SOI structure reaches a maximum of 309 K, whereas the Si/SiC reaches just 301 K. This difference is explained by the presence of the BOX layer that acts as a thermal barrier impeding heat transfer. This causes self-heating in the Si as insufficient heat is passed vertically, increasing the temperature of the Si film. This effect is exacerbated by the temperature dependence of thermal conductivity, which drops as the temperature rises, worsening the situation. The bulk Si beneath the oxide has little influence on thermal performance.

In the Si/SiC simulation, the 6H-SiC functions as a heat sink and extracts most of the heat down to the Al layer. It reduces not only the device temperature but also the lateral spread of heat that will affect neighbouring components (see Fig. 5.1). Therefore, this Si/SiC can offer a ‘thermal integration’ to power ICs and hence reduce their reliance on external cooling equipment.

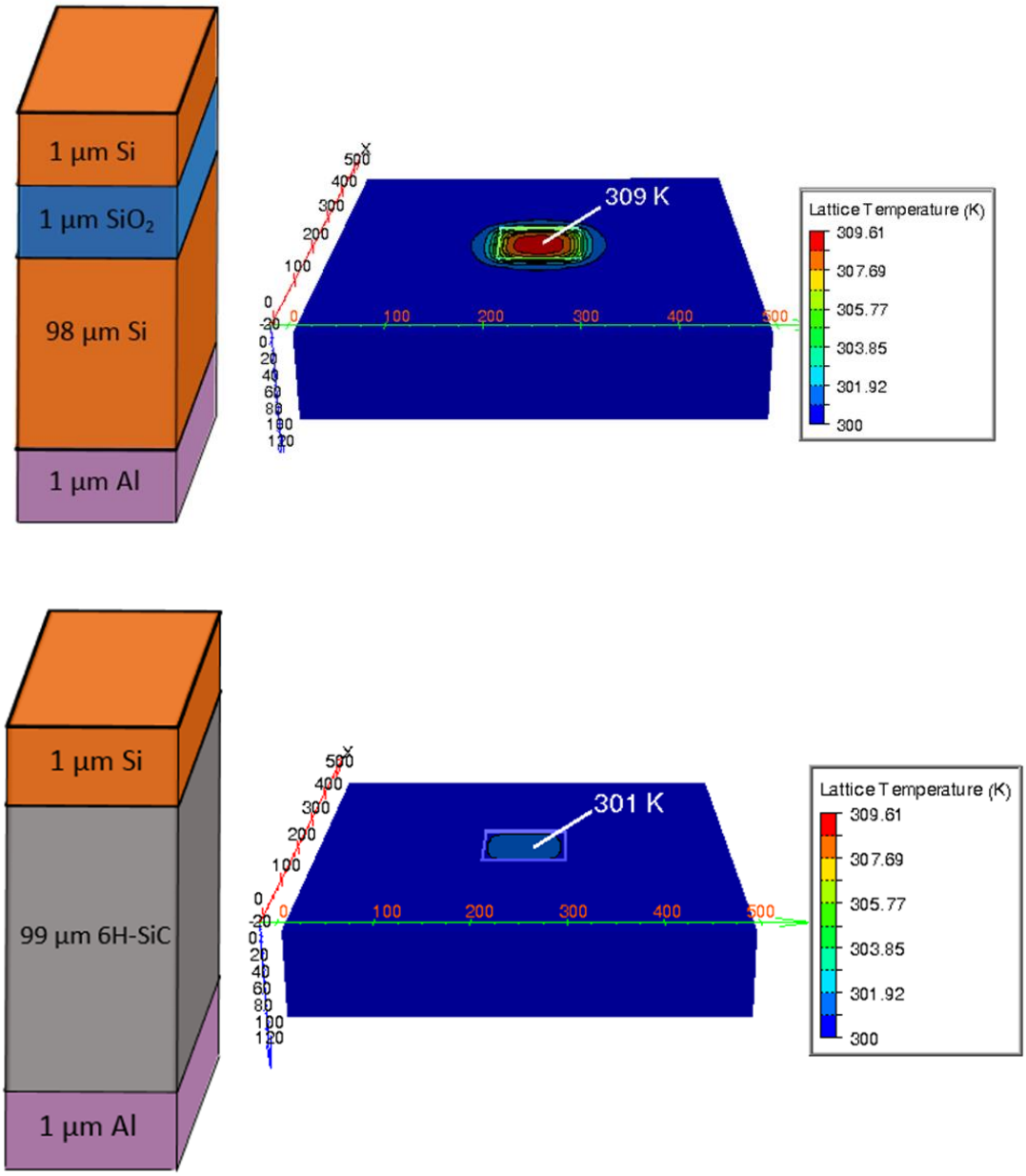

Figure 5.1. The SOI (top) and Si/SiC (bottom) simulation models showing temperature distributions with a range of 300-309.61 K. Their maximum temperatures are 309 K (top) and 301 K (bottom) respectively.

Fig. 5.2 displays the relationship between the power density and the maximum temperature for all the different substrates considered. Bulk SiC is shown to be the best solution for dissipating the heat and the Si/SiC can exhibit a similar thermal behaviour if the Si layer is very thin (1 µm). Increasing the Si layer to 10 µm reduces power capability, the curve tending to the bulk Si case with increasing Si thickness, a result indicative of a

weaker cooling effect. There are three SOI variants in Fig. 5.2 and common to them is the thickness of top Si film (1 µm). With a 1 µm BOX and Si substrate, the SOI has the poorest power capability at 300 °C. By reducing the BOX layer from 1 to 0.5 µm only, the power capability is improved and again approaches that of bulk Si. By just replacing the Si substrate with SiC, the $Si/SiO_2/SiC$ structure is formed and the improvement observed, but not as effective as the previous solution. It is worth noting that in this structure, there is no window opened in the SiO_2 layer to bring the Si and SiC region in contact, unlike the Si/oxide/SiC (SiOSiC) substrate proposed by Udrea et al. [72].It can be seen that the thin BOX layer has a dominant effect on the heat transfer ability of SOI substrate. This is due to the low thermal conductivity of SiO_2 (0.014 W/Kcm).

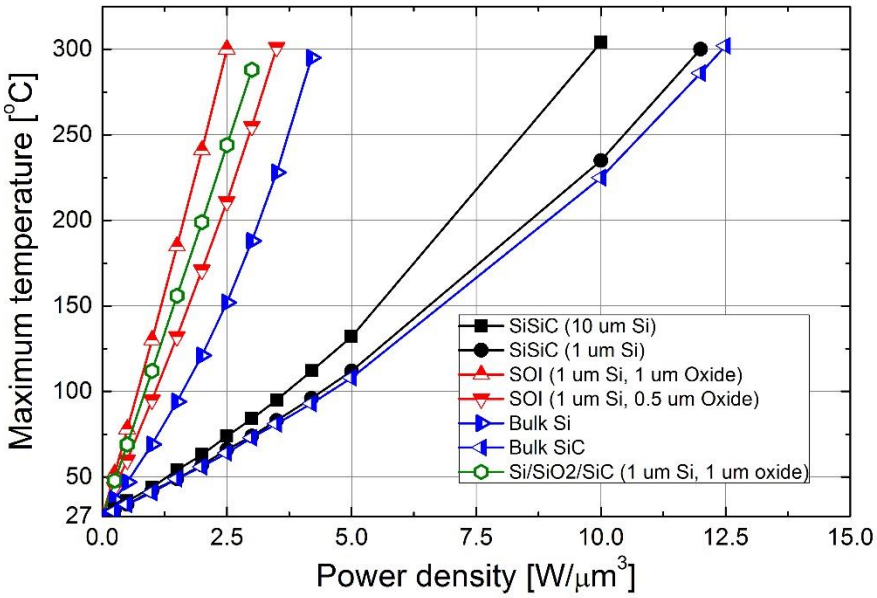

Figure 5.2. Simulated max temperatures (27-300°C) vs. power density for different structures

5.2.2. Electro-thermal modelling of PiN diodes

5.2.2.1 Simulated structures

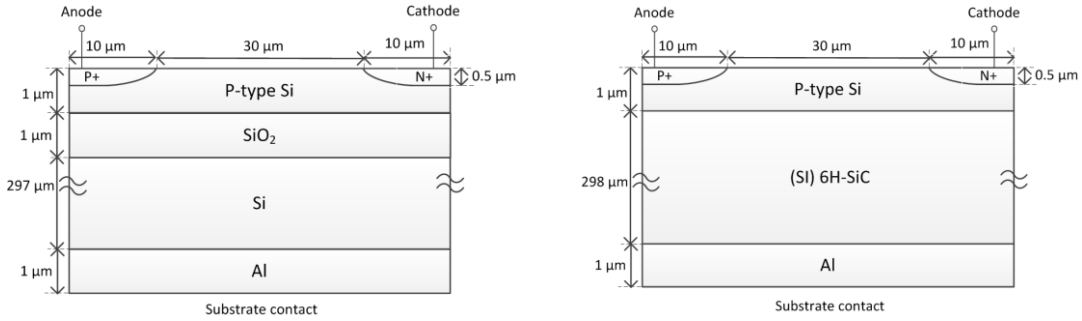

Figure 5.3. The simulated SOI (left) and Si/SiC PiN diodes (right)

As can be seen in Fig. 5.3, a SOI substrate is simulated with a Si device layer, a BOX layer, an n-type Si substrate and an Al back electrode. The thicknesses of these regions are 1, 1, 297 and 1 µm, respectively. A PiN diode is created in the top Si layer with a uniformly p-type doping density of 3×10^{15} cm^{-3}. The anode and cathode of the diode have ohmic behaviour, which is achieved by defining an N+ and P+ region under the contacts. The doping profile of each region is characterised by a vertical and lateral spreading according to a Gaussian function and a peak doping value of 1.5×10^{19} cm^{-3} at the surface. As a result, the junction area is about 10×0.5 μm^2 with a rounded corner. Between the two highly doped zones is a drift region having 30 µm in length. For fair comparison, a PiN diode is established with the same configuration into a Si/SiC substrate. This architecture comprises a Si layer, a (SI) 6H-SiC region and an Al back electrode, which are 1, 298 and 1µm in height respectively.

In the two diodes, the doping of the drift region is decided without using the RESURF principle. Therefore, the simulation is not based upon optimised devices and does not reveal the maximum potential of the SOI and Si/SiC structures. However, a comparison is made between the same diodes only differing in the substrate, which can highlight the electrical and thermal effects of identical structures on the different substrates. Simulations on devices optimised for each substrate will be presented in Chapter 6 & 7.

5.2.2.2 Simulation setup

To simplify the simulation, no parameter (e.g. fixed charges and traps) is configured along the Si/SiC and Si/Oxide interface. Furthermore, the simulation is run with carrier lifetimes of 100 ns and the band-to-band tunneling model being deactivated. The substrate contact and cathode are grounded unless stated otherwise. To see the dimensional effect on the breakdown, the length and thickness of drift region will be altered.

For electro-thermal modelling, the anode, cathode and Al electrode are defined as thermal contacts to consider horizontal and vertical heat dissipation. Both isothermal and non-isothermal simulations are performed. The isothermal model considers the device at a fixed temperature (300 K) and is used herein for validation of the comparative electrical characteristics. Within the non-isothermal simulation self-heating is reintroduced, as temperature is iteratively updated due to the power dissipated, affecting the properties of the semiconductor including thermal conductivity.

5.2.2.3 Simulation results

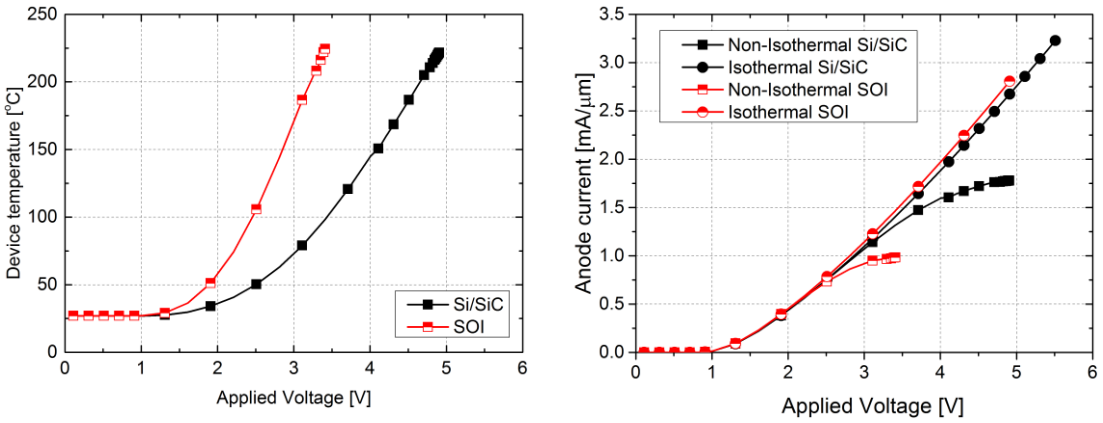

Figure 5.4. Applied Voltage vs. Device temperature (left) and Anode current (right) for the Si/SiC and the SOI

To operate the diodes in the on-state, positive voltages are applied to the anode. Fig. 5.4 shows the on-state I-V curves of these two diodes and their device temperatures. The isothermal model shows that if temperature effects are ignored, both devices have a turn-on voltage of 0.7 V and very similar resistance. However, this relationship only holds true within a small region of the non-isothermal simulations. Self-heating effects are observed in both diodes, but the Si/SiC one suffers less performance penalty. Its linear region is

longer and the heat transfer ability is much better. At 3 V, the higher current in the Si/SiC device means more power is being dissipated than in the SOI device. However, its temperature is approximately 75 °C, about two times lower than its counterpart (see Fig. 5.4). It is worth noting that in practice, the temperature rise associated with conduction losses is less considerable than that in the simulation as the diodes are controlled by pulse signals instead of DC.

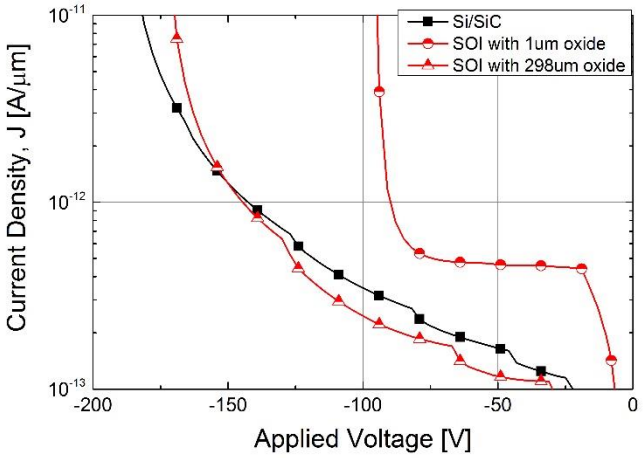

Figure 5.5. Reverse I-V curves for Si/SiC and SOI structures

By applying a negative bias to the anode, the diodes are operated in the off-state. Fig. 5.5 demonstrates the I-V curves of the PiN diodes under reverse bias in the Si/SiC and SOI structures. Because the reverse current is very small, the diodes do not induce any temperature rise. The SOI diode breaks down at -87 V whereas its Si/SiC counterpart can support reverse voltages up to -175 V. Furthermore, the SOI leakage is much higher even with a better insulating layer. By increasing the BOX thickness to 298 μm, the difference in the I-V curves between the two diodes is less apparent.

This indicates that the poorer off-state behaviour in the SOI is caused by the built-in Silicon-oxide-Silicon (SOS) capacitor. If the BOX is very thin (1 μm) and the diode is reverse-biased, a large number of holes will gather under the BOX at the anode side and decline towards the cathode. In response to this, the Si layer has to be depleted more at the anode side to balance such charge distribution. Therefore, vertical breakdown will occur at the P-/oxide junction under the anode in the SOI. With a very thick BOX layer or (SI) SiC, the SOS capacitive effect becomes so weak that the Si layer is depleted mainly by the P-/N+ junction at the cathode. This increases the blocking voltage by relaxing the electric field at the anode and lowers the generation leakage by shrinking the depletion volume.

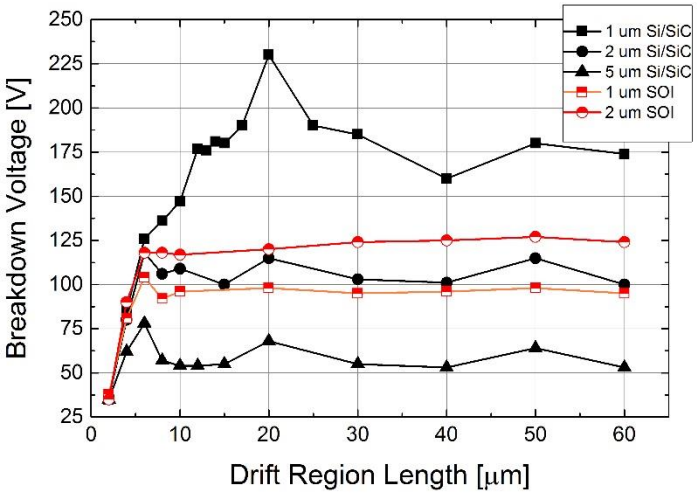

Figure 5.6. Drift region length vs. Breakdown voltage

Figure 5.6 displays the relationship between the drift region length and the breakdown voltage for both structures with different thickness of the top Si layer. Each curve has a value for drift region length below which the breakdown voltage scales up with the length, and above which the breakdown voltage is determined mainly by the thickness of silicon. By increasing the Si thickness from 1 to 2 μm, the SOI blocking voltage is raised from 100 to 125 V with a long drift region. This proves that the avalanche breakdown takes place at the P-/BOX junction under the P+ anode, as the extra thickness allows a wider depletion region to support vertical potential. However, the opposite is true in the Si/SiC, with the 1 μm Si layer achieving the highest blocking capability. This behaviour reveals that the breakdown point of Si/SiC is not at the anode but the P-/N+ junction.

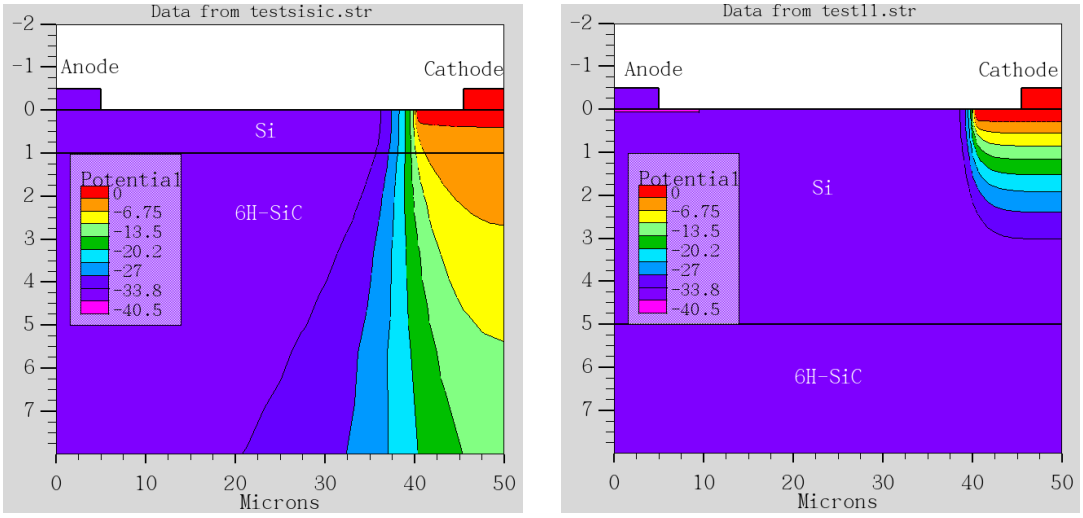

Figure 5.7. The potential distributions of the Si/SiC with a 1 μm (left) and 5 μm thick Si layer (right), at an anode voltage of -40 V

Fig. 5.7 shows the potential distribution at an anode voltage of -40 V, for two Si/SiC structures with 1 μm and 5 μm Si layer. This thin-film Si/SiC diode has a higher breakdown voltage than its thick-film counterparts. It can be seen that the thick layer densifies the potential lines at the corner of P-/N+ junction, creating a strong electric field crowding effect. By contrast, the depletion regions of the P-/N+ junction are wider laterally in the thin Si layer because of a much sparser potential contour in the vertical direction. Therefore, the thin-film PiN diode can be simply described by the 1-D breakdown model whereas the thick-film case requires a 2-D analysis to consider the edge effects [39]. This explains the reduction of blocking voltage in the Si/SiC structures with a thick Si layer. Nonetheless, the breakdown will always take place at the P-/N+ junction in the Si/SiC and if one wants to improve the on-resistance by increasing the layer thickness and doping, the blocking voltage will correspondingly be reduced. To tackle this problem, the RESURF designs are indispensable.

Such distinct features of the two substrates can also be analysed by the RESURF principle. As mentioned in Chapter 3, the optimal RESURF condition can be satisfied by having an effective dose profile higher at the drain side and descending towards the source. In the case of the PiN diodes, the anode and cathode can be viewed as the drain and source respectively. In the SOI where the breakdown point is at the p-/oxide, a thicker layer accommodates more impurities, thereby creating a better RESURF effect at the anode side; In the Si/SiC where the breakdown is at p-/N+ junction, a thinner layer provides lower doses, thereby improving the RESURF effect at the cathode.

5.3. Si/SiC RESURF LDMOS designs

As mentioned in the last section, the Si/SiC PiN diodes support reverse voltage by the unbalanced depletion in the drift region, with an electric field peak at the p-/N+ junction. This reduces the scalability of the drift region length to the blocking voltage and indirectly lowers the electrical conductivity. Such behaviour can also be seen in an n-type non-RESURF LDMOSFET using the Si/SiC substrate, as the applied voltage is sustained by a built-in PiN diode consisting of a P body, N- drift region and N+ drain. If the P body is deep enough to meet the Si/SiC interface, the depletion is one-dimensional and only significant at the P body/N- junction in the transistor. To deplete the drift region evenly in the off-state, RESURF layouts have to be introduced.

As mentioned in Chapter 3, there are two fundamental RESURF structural types, namely SOI and PN junctions. They can be seen in power ICs in dielectric isolation (DI) and junction isolation (JI) technology, respectively. Their function is to develop a space charge region vertically so that a uniform electric field distribution is produced in the drift region. One example for the SOI RESURF is the Philips transistor [46] used in Chapter 4 for the model verification. The instances for the PN RESURF are detailed in Chapter 3, namely the single, double, triple and quadruple case. Generally speaking, the RESURF effects in a transistor can be created with the SOI, PN structure or both of them (e.g. [82]), structured in either 2D or 3D domain. Furthermore, these two can be merged into a new RESURF type that features a thin dielectric layer between an N and P type region [91]. To simplify the TCAD study, 600/190 V Si/SiC LDMOSFETs are conceived in a 2-D plane with either the SOI or PN structures, based upon the Philips' [46] and D. Disney's designs [99]. This section first introduces a 600 V Si/SiC LDMOSFET with a SOI RESURF layout, followed by a 600 V Si/SiC in the PN RESURF technology and completed with a 190 V Si/SiC LDMOSFET designed with the SOI RESURF concept. In each part, their SOI, PSOI or bulk Si counterparts are also described, with emphasis on the similarities and differences between them.

5.3.1. 600 V Si/SiC LDMOS with SOI RESURF

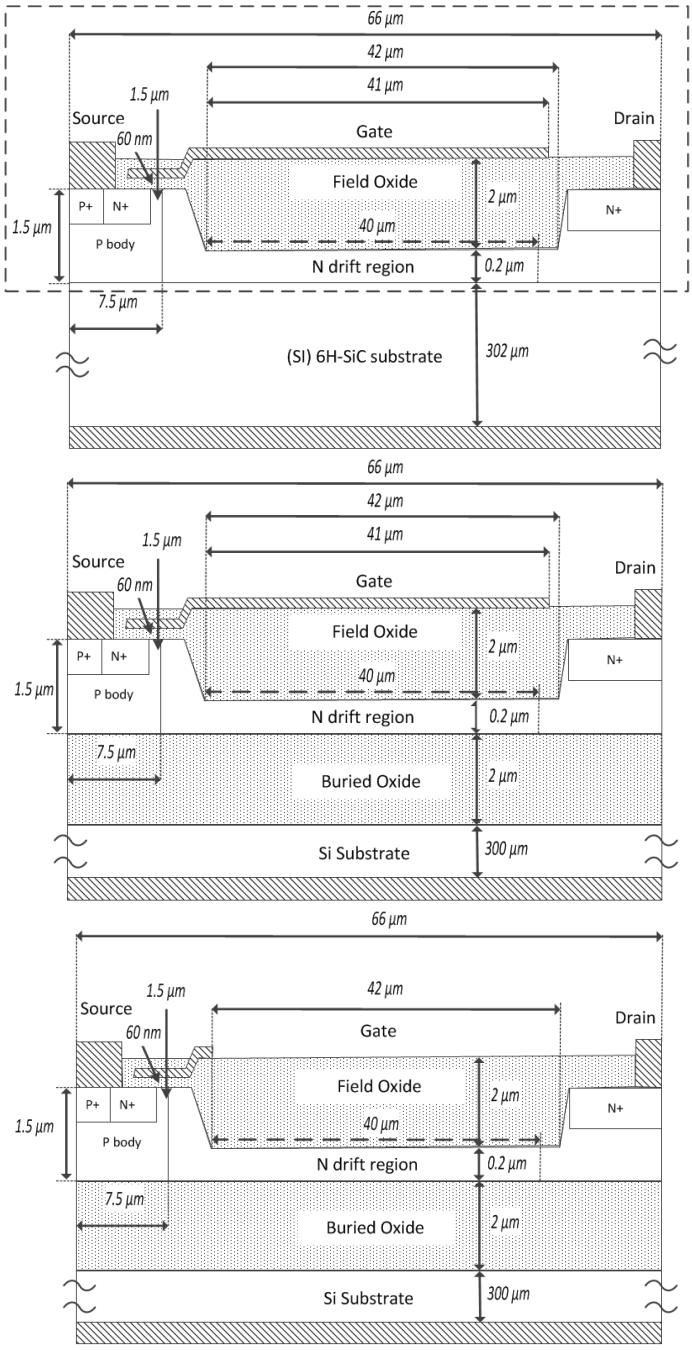

Figure 5.8. The 600 V Si/SiC LDMOS design with a SOI RESURF layout (top) and its SOI counterparts in the Philips technology (middle) [46] and by Paul et al. (bottom) [133]

Fig. 5.8 shows three 600 V LDMOSFETs using SOI RESURF, with their key parameters labelled. From top to bottom, they are the Si/SiC transistor, the Philips SOI design [46] described in detail in Chapter 3, and a second SOI LDMOS structure based upon [133]. This second SOI design is employed to study the RESURF and accumulation effect induced by the extension of the gate field plate. On the whole, they are very similar regarding the LDMOS structures in the Si layer. In Chapter 6, this Si/SiC design and the Philips SOI will be compared to understand the effect of the BOX layer on the electrical and thermal properties of the LDMOSFETs. In addition, the accumulation effect will be studied by the comparison between the Si/SiC transistor and the SOI without the field plate.

Identical to the Philips SOI, the Si/SiC embodiment is 66 μm in length and has a 1.5 μm thick Si layer where a 42×0.2 μm^2 drift region is formed, separating a p body and drain region. A linear doping profile starts from the onset of the drift region and is 40 μm long. On top of the thinned-down region is a 2 μm thick field oxide, covered by a gate contact extended up to 41 μm with respect to the origin of the drift region. The p body region is 7.5 μm in width and has a doping density of 6.5×10^{16} cm^{-3}. In this region, the gate oxide is 60 nm in height and the effective channel length is 1.5 μm, being defined by the lateral spacing between an N+ zone and the edge of p body. The drain and source metal are deposited on highly doped regions for ohmic contacts.

Different from the Philips SOI, the Si/SiC design includes a 302-μm-thick (SI) 6H-SiC substrate under the aforementioned LDMOS topology. This means that the drift region is only able to be depleted from an inverse SOI structure (IOS). This layout is made of the gate electrode, field oxide and Si layer, and enclosed by a dashed box (see Fig. 5.8). In this arrangement, the gate contact behaves like the substrate electrode in the SOI case as it almost entirely overlaps the field oxide and is zero-biased in the reverse blocking state [4]. Therefore, as long as the field oxide is thick enough to support the required potential, this IOS layout is equivalent to ordinary SOI. This idea originates in [134], where a step field oxide is used for a uniform-doped silicon-on-sapphire device. This design was then refined using linear doping to increase the breakdown voltage to 600 V, with reduced resistance [6]. In this case, the Si layer thickness used in Equation 3.9 is 0.2 μm and the gradient of the linear doping is calculated:

$$V = 600\ V, W = 40\ \mu m, t_{si} = 0.2\ \mu m, t_{ox} = 2\ \mu m,$$

$$q = 1.6 \times 10^{-19}\ C,$$

$$\varepsilon_{ox} = 3.45 \times 10^{-13}\ Fcm^{-1}, \varepsilon_{si} = 1.04 \times 10^{-12}\ Fcm^{-1}$$

$$\frac{dN(x)}{dx} = \frac{V\varepsilon_{si}}{qW\left(\frac{1}{2}t_{si} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \times t_{ox}\right)t_{si}} \tag{5.1}$$

$$= 7.95 \times 10^{19}\ cm^{-4}$$

The base doping of the drift region N_b is set to be 8×10^{15} cm^{-3} for a breakdown voltage of approximately 640 V. Based upon this, the doping profile in the drift region is obtained and shown in Fig. 5.9. Also plotted is the graded profile for the Philips SOI LDMOSFET. The profile for the SOI is much steeper and the maximum doping is two times higher. The reason for this is that a dual-plate structure is present in the SOI that generates a symmetric charge modulation in the Si layer [135].

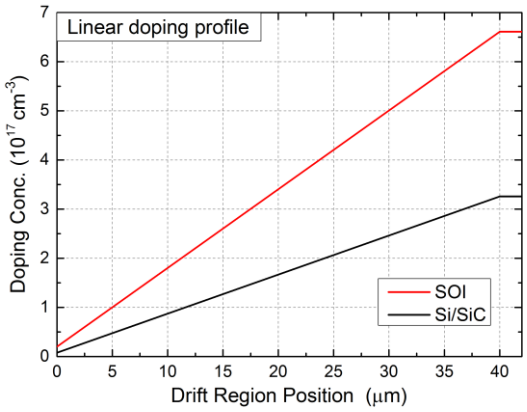

Figure 5.9. The linear doping profiles in the drift regions of the Si/SiC and Philips SOI

Integrating the doping profile over the drift region thickness, one attains the effective dose:

$$Q_{eff} = N_b t_{si} + \frac{1}{2}\frac{dN(x)}{dx} \times W \times t_{si} = 3.34\ \times 10^{12}\ cm^{-2}$$

At a low gate bias, this value indicates how many free electrons are available per unit area for on-state current conduction. As the gate bias is increased, the accumulation effect arising from the IOS layout becomes more significant and supplies extra carriers to lower the resistance [135]. To view this phenomenon, the SOI structure without the gate

extension [133] is used and compared with the Si/SiC. In this SOI, the gate contact covers a very small portion of the field oxide and is terminated at the origin of the drift region. Doing so minimises the accumulation effect and reduces the electric field peak at the body region. In addition, the depletion from the field oxide is eliminated so that the RESURF effect mirrors that of the Si/SiC. As such, the gradient of the doping profile for this SOI is the same as that for the Si/SiC. However, the base doping has to be reduced to 4×10^{15} cm^{-2} for a breakdown voltage of above 600 V because such gate field plate creates an electric field peak at the onset of the drift region. When comparing with this SOI for the accumulation effect, the Si/SiC design will be configured to have a base doping of 4×10^{15} cm^{-2} instead of 8×10^{15} cm^{-2}. Apart from the gate extension and linear doping profile, this SOI design is exactly the same as the Philips SOI.

The effect of this RESURF dose on the potential distribution for the three structures can be viewed in Fig. 5.10. All three devices are at the onset of avalanche breakdown. It can be seen that a nearly linear voltage drop is present along the x-direction of the drift region of the Si/SiC device, which results from the vertical depletion induced by the IOS layout. The SOI without the gate extension has a similar depletion effect, though the contours are inverted. The Philips SOI features a mirroring pattern for its potential outlines, indicating a double SOI RESURF effect. In the Si/SiC transistor, the electric field is kept at a constant value of about 1.5×10^{5} V/cm in the drift region, with a peak at 7.5 µm due to the presence of the P body/N- junction (see Fig. 5.11).

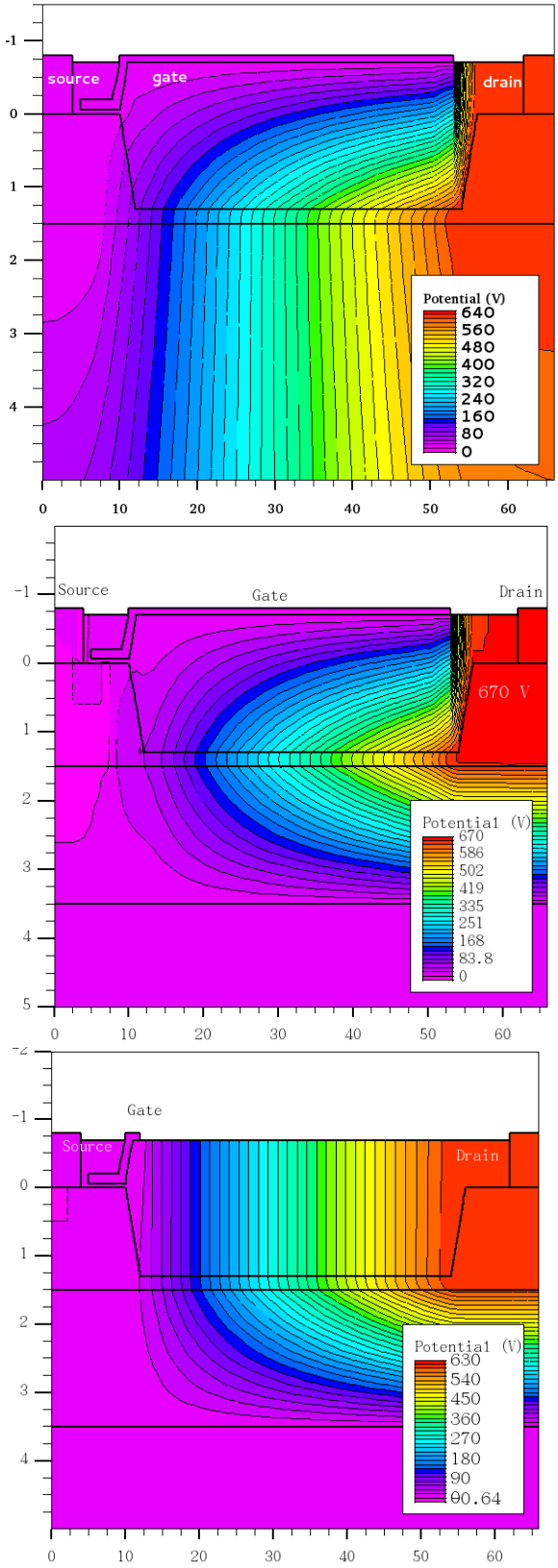

Figure 5.10. The potential contours at 300 K and onset of breakdown, for (top) the Si/SiC and (middle) the Philips SOI and (bottom) the SOI without the field plate extension (axes units: μm)

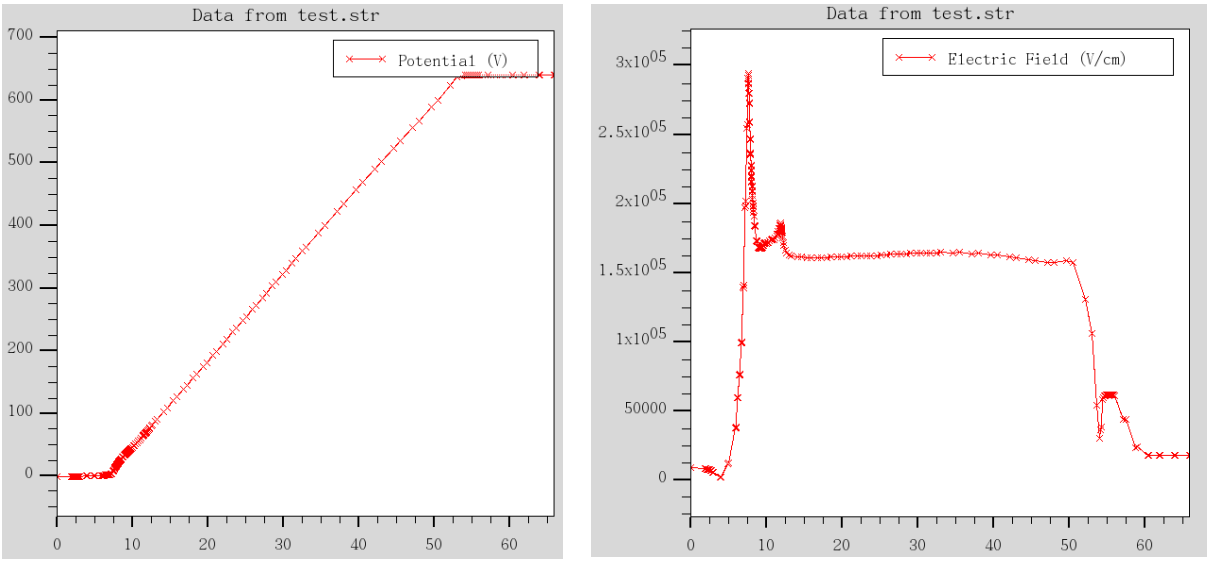

Figure 5.11. The potential distribution (left) and electric field (right) at the bottom of the Si layer in the Si/SiC transistor, at the onset of avalanche breakdown and 300 K (axes units: μm)

5.3.2. 600 V Si/SiC LDMOS with PN RESURF

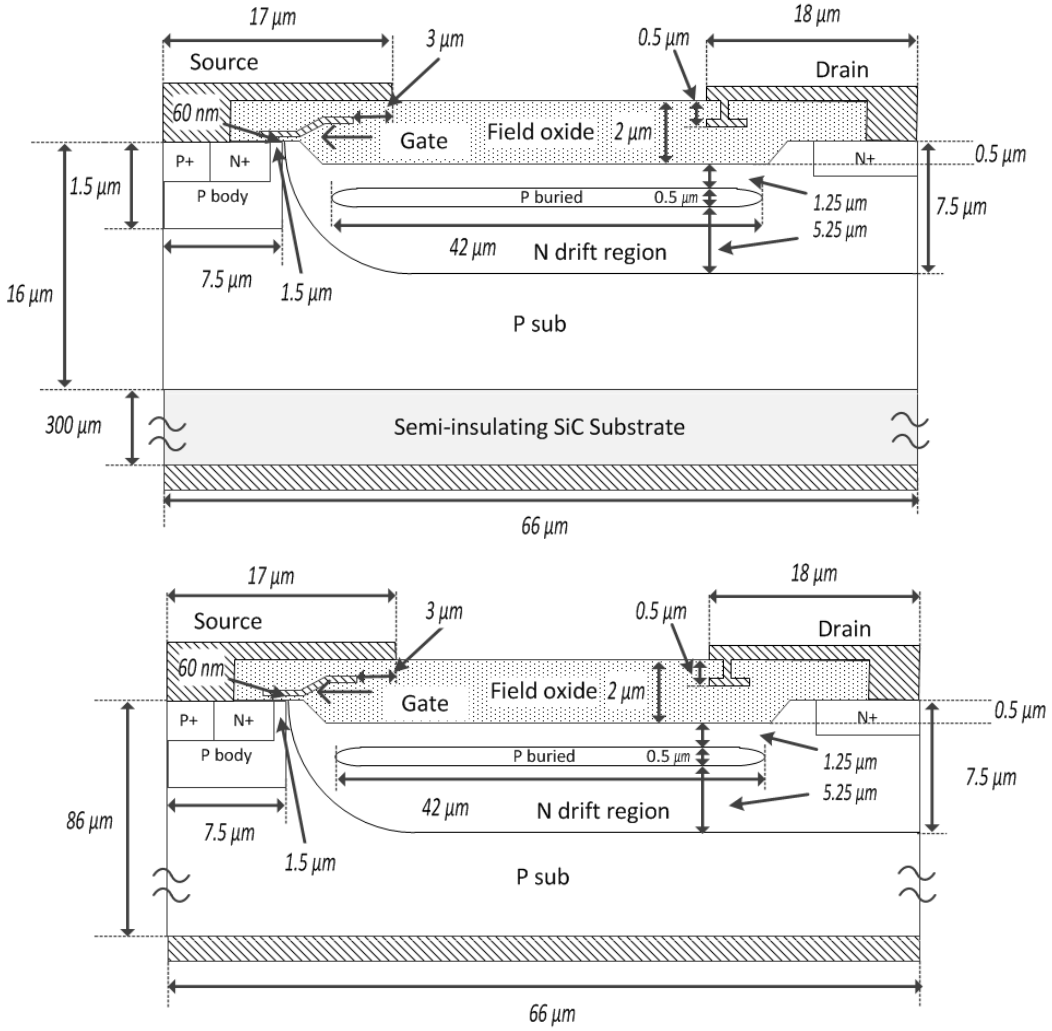

Figure 5.12. Two 600 V LDMOSFETs with a triple RESURF layout, using the Si/SiC (top) and the bulk-Si substrate (bottom)

Fig.5.12 shows a 600 V Si/SiC LDMOSFET with a PN RESURF layout and its bulk-Si counterpart. In Chapter 6, these devices will be compared in order to understand the effects of the (SI) SiC substrate on the leakage current and breakdown voltage at high temperature.The design of both transistors uses the LDMOS framework proposed by Disney et al. [99]. Therefore, they are similar to each other and characterised by a buried P layer in an N drift region. This setup creates a triple RESURF effect and results in a drift region dose of 3×10^{12} cm^{-2}, a value similar to that of the 600 V Si/SiC device in SOI RESURF technology. Unlike the Philips structure, the LDMOS framework used here is specific to the bulk-Si substrate and not tailored for high temperature application.

However, the implementation of the Si/SiC substrate for this design can minimise the drain-to-substrate current and offer a better electrical isolation, which increases the upper limit of operating temperature. To house this design in the Si/SiC substrate, the Si layer has to be P- type and very thick (16 µm). Such Si/SiC wafers have been fabricated by direct wafer bonding and exhibit very good electrical behaviour [131]. Similar to the thick SOI case, this Si/SiC device can be insulated completely by using deep trench isolation technique [67] as the Si layer thickness is less than 20 µm. Therefore, this thick-film Si/SiC LDMOSFET can be another candidate for elevated temperature operation, just like its thin-film counterpart in the Philips technology.

In the bulk-Si case, the LDMOS design is built into a p type substrate 86 µm thick with a doping density of 1×10^{14} cm^{-3}, which enables a vertical blocking capability up to 640 V at 300 K. This configuration can be compared to [136], where the LDMOSFETs were fabricated into high resistive p type substrates 150 µm thick (ρ=1.2 x 10^{14} cm^{-3}), for a breakdown voltage of 1200 V. For having the same triple RESURF effect, the Si/SiC LDMOSFET uses a 16 µm thick p type layer with a doping density of $1x10^{15}$ cm^{-3}, on a 300 µm thick (SI) 6H-SiC substrate. For fair comparison between their cooling performances (Chapter 6), the thickness of bulk Si substrate will be increased to 300 µm.

It can be found that the bottom channel is more than four times thicker than the top channel, which deviates from the triple RESURF setting stated in Chapter 3. This is because the theory is explained by assuming a uniform doping profile in PN pillars, which is rarely` the case in reality [8] [17]. In the drift regions of the two thick-film devices, a more realistic impurity distribution is used and obtained from SILVACO process simulator, SSUPREM4 [18]. For the bulk Si case, the simulation began with a phosphorous implantation at energy of 380 eV, with a dose of 3.57×10^{12} cm^{-2}. This was followed by an 1180 °C anneal for 500 mins to enable donors' diffusion and form the N well. After this, boron ions were implanted at 1150 eV, with a dose of 2.25×10^{12} cm^{-2} and a subsequent rapid thermal anneal was carried out at 700 °C for 0.5 mins to shape the p buried region. The same applies to the Si/SiC case, but with some small adjustments on the settings for implantation and annealing owing to different doping values of P sub in the two cases. Fig. 5.13 shows the resulting vertical doping profiles at the middle of the drift region, for the two thick-film transistors. Also illustrated is an impurity distribution in the ideal triple RESURF layout. The donor concentration drops with increasing Si layer

thickness. The acceptor density peaks at the middle of the buried layer and falls drastically in the vertical directions. As such, the p buried layer has to be positioned closer to the surface, to fully deplete the top channel which has a higher doping than the ideal case. A similar setup can be found in [8], where the bottom conduction path is 6 times wider than the top one. In the Si/SiC transistor using the Philips technology, the effect of dopant diffusion in the vertical direction is ignored due to the presence of a thin layer [19].

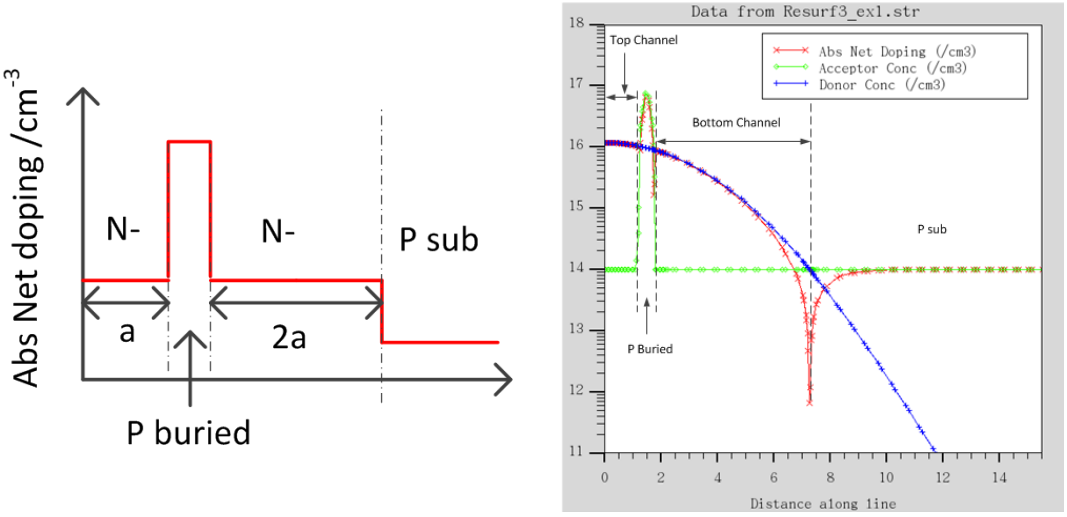

Figure 5.13. The doping profiles in the ideal triple RESURF case (left) and in the TCAD simulation (right), for the two thick-film transistors

With this doping profile, the potential is distributed similarly in the thick-film Si/SiC and its bulk Si counterpart at the onset of avalanche breakdown (see Fig. 5.14). The P substrate and buried layer deplete the top and bottom channel vertically, allowing the majority parts of drift region to share equal amount of voltage. The field plate design makes the contours crowd in the field oxide at the end of the source and drain metal, reducing the electric field peaks at the p body/N- and N-/N+ junction.

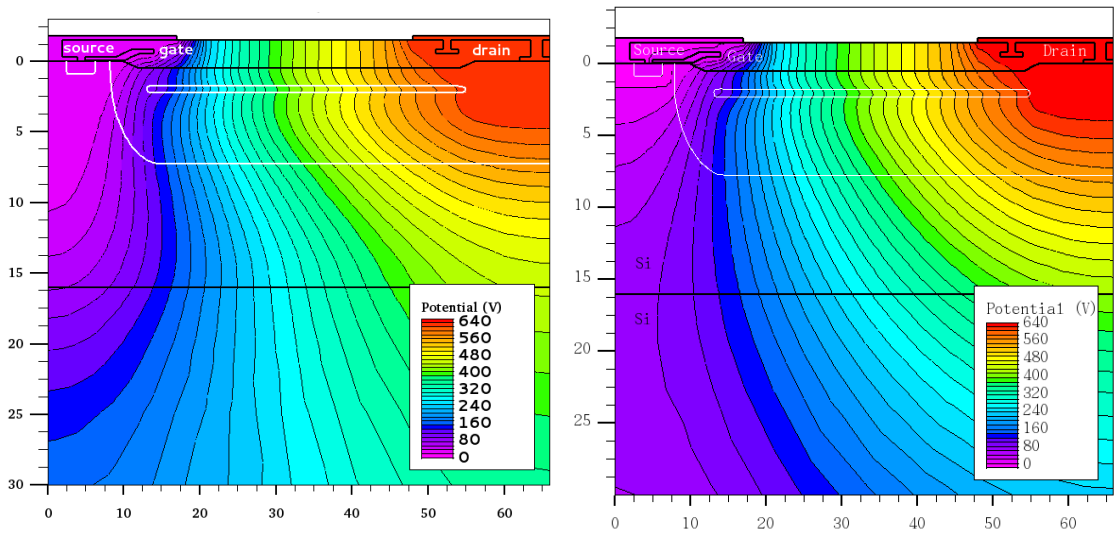

Figure 5.14. The potential distributions at 300 K and onset of breakdown, for the thick-film Si/SiC (left) and its bulk Si counterpart (right) (axes units: µm)

5.3.3. 190 V Si/SiC LDMOS with SOI RESURF

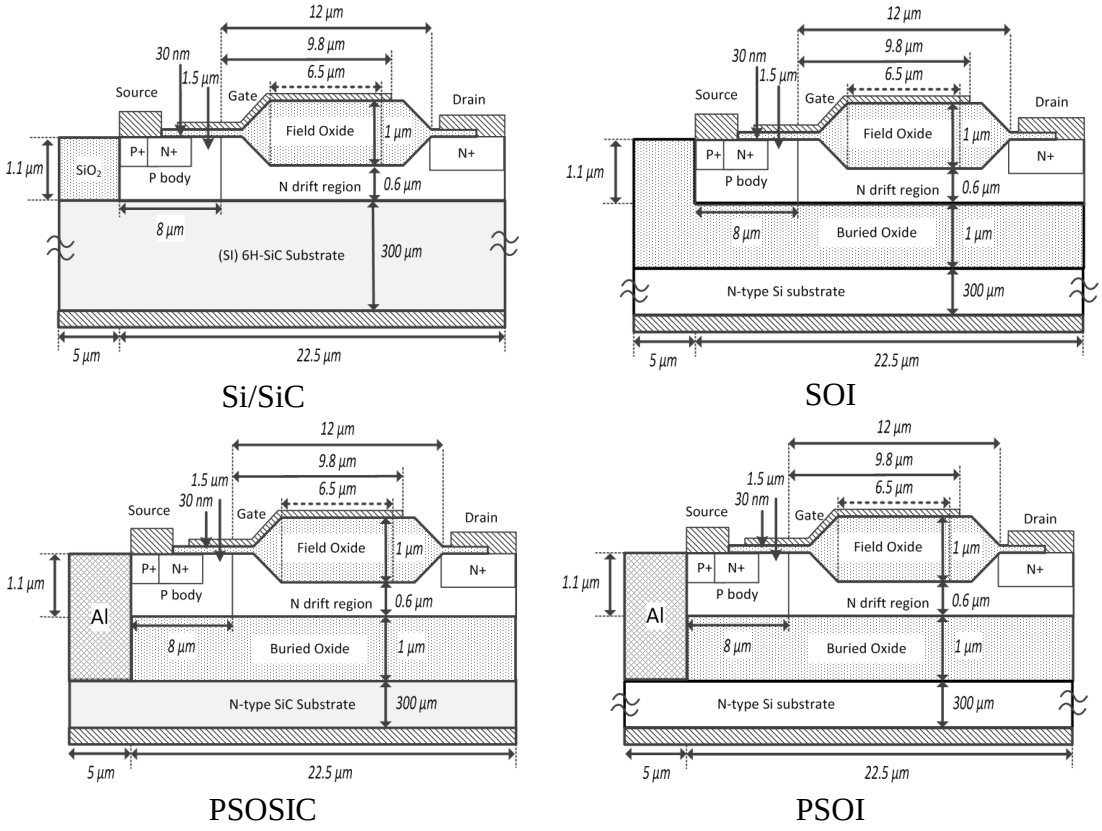

Figure 5.15. 190 V LDMOSFETs using different substrates, namely Si/SiC, SOI, PSOSIC and PSOI

Fig. 5.15 illustrates four 190 V LDMOSFETs which have the same geometry in the active region. The LDMOS topology is transferred from the 190 V Philips LDMOSFET described in Chapter 4. All the architectures accommodate the LDMOS design as well as a region 5 µm wide on the left hand side. In the Si/SiC and SOI, this region is filled with SiO_2 and offers electrical isolation. In the other two architectures, the SiO_2 is replaced with Al and the region borders an N-type substrate, interrupting the buried oxide. This is a Partial SOI (PSOI) layout as mentioned in Chapter 3. To distinguish them, 'PSOI' is used for the device featuring an N-type Si substrate, while PSOSIC is the Partial $Si/SiO_2/SiC$ featuring an N-type SiC substrate. It is worth noting that the potential of the Partial $Si/SiO_2/SiC$ to be applied in power applications has been studied by Udrea et al. [72], though the SiC substrate is P-type and will react with an N-type Si layer to form a PN RESURF effect. It is expected that this partial removal of the BOX layer in the PSOI and PSOSIC can suffer less heating compared with the SOI, but not as thermally efficient as the Si/SiC solution which features the complete removal of the BOX. In Chapter 7, these devices will be compared in order to understand the effectiveness of different thermal-aware designs in improving energy capability.

In each structure, the LDMOSFET is 22.5 µm wide and has a Si layer 1.1 µm thick. In lateral sequence from left to right, presented in the Si layer are a body region, a drift region and a drain region. The body region is 8 µm in width and has a p-type doping density of $8x10^{16}$ cm^{-3}. An N+ and P+ zone are added to form an ohmic contact with a source metal. The N+ is offset from the edge of p body by a lateral distance of 1.5 µm which is defined as the channel length. The channel and a gate metal are separated by a 30 nm oxide layer. The drift region is 12 µm long, with a thinned-down region 0.6 µm thick. One top of this region is a 1 µm thick field oxide, covered by a gate extension. The gate is extended 9.8 µm and 6.5 µm, with respect to the border of p body and origin of drift region, respectively.

In the Si/SiC layout, the device sits directly on a 300 µm thick (SI) 6H-SiC substrate whereas the other cases have a 1 µm BOX between the Si layer and a 300 µm thick conductive substrate. In this case, the three SOI devices and the Si/SiC have double and single RESURF effect respectively. To achieve the optimal electric field distribution, Equation 3.8 is utilised to calculate their linear doping profiles. Such procedures can be referred to the case of the 600 V Si/SiC LDMOSFET. Their potential distributions are not

shown here as they are very similar to those of the 600 V devices in the SOI RESURF technology.

5.4. Simulation setups

This section outlines the setups that will be used in Chapter 6 & 7 for device modeling. First introduced is the settings of the physical-based models that are verified and discussed in Chapter 4 and Appendix C. Secondly is the description of four different switching circuits that will be simulated for the aforementioned LDMOSFETs.

5.4.1. Application of the physical-based models

As mentioned in Chapter 4 and Appendix C, the SOI, bulk Si and Si/SiC devices share the same models, apart from the settings for the interfaces and the thermal properties of the substrates. More specifically, the SOI device is simulated with a positive charge of 4×10^{10} cm^{-2} for both Si/SiO_2 interfaces [124], while the Si/SiC uses the same value for its top interface but a negative charge of 2×10^{10} cm^{-2} for the bottom one [131]. According to [46], this charge value is also applicable to the bulk Si case where the Si/SiO_2 interface value is specified to $+4\times10^{10}$ cm^{-2} as well. The thermal models for the simulated structures can be referred to Appendix A. Carrier lifetimes are set to 1.5 and 70 μs at room temperature for the thin and thick-film structures, to achieve generation lifetimes, which are similar to those in [46]. Unless stated otherwise, the substrate electrode of each device is grounded and defined as a thermal contact at a fixed temperature of 300 K. This setup will be used throughout the DC and transient simulation.

5.4.2. Simulated switching circuits

In SILVACO, the circuit-based modeling is performed by Mixed-Mode simulators [122] where electrical components can be described at multilevel of abstractions. For instance, the semiconductor device under investigation can be represented by a physical-based model and other non-critical component by compact models. This methodology can achieve a better trade-off between simulation time and accuracy, but increases the complexity and difficulty of the modeling setup. Other than the semiconductor physics, the users need to familiarise themselves with the SPICE programming language [122] for

defining the circuit network. Numerical problems can arise due to the incompatibility between the physical and compact models and therefore lengthy debugging can be involved in the process. To increase the computing efficiency, the practical circuit is usually simplified in the simulation to some degree, but with its main functions retained. This means that some components will be ignored or replaced with a much simpler form. The operation will be limited to a few cycles as well and the heating effect restricted to the semiconductor devices only.

In this section, four circuits are introduced that will be used in the transient simulation of the power MOSFETs mentioned earlier. Firstly, a diode-clamped inductive load switching circuit will be demonstrated, for the 600 V Philips SOI LDMOSFET and its Si/SiC equivalent. Secondly, presented is a Rectangular Power Pulse (RPP) circuit that is used to assess the thermal performance among the 600 V Si/SiC, SOI and bulk-Si devices. The results of these two circuits will be analysed in Chapter 6. The last two switching circuits feature a capacitive load and an inductive load with a Zener diode respectively, for the four 190 V LDMOSFETs using SOI, PSOI, Si/SiC and PSOSIC substrate. Their dynamic characteristics will be compared in Chapter 7.

5.4.2.1 Clamped inductive switching (600 V)

5.4.2.1.1 Introduction

Before looking at the simulated circuit, some background information is given on the applications of the 600 V class power MOSFET. The 600 V MOSFET is the core component in an AC/DC flyback and a half bridge topology, as shown in Fig. 5.16 [5] [6] [7]. These circuit are widely used in applications where power conversion needs to be performed, such as TVs, phone chargers, motor drives and electric vehicle traction systems [5]. In the circuits, the role of the HV MOSFET is to deliver power to an inductive load through switching actions. Such operation is carried out at high frequencies (e.g. 200 kHz), which reduces the size and weight of the inductive components [5]. By using a lateral layout for the MOSFET, the system can be made more compact and with less parasitic effects, as the LDMOSFET can be integrated with the control logic. It is even possible for the inductor to be integrated into the semiconductor process [8], enabling further integration. Fig. 5.17 illustrates some key integrated components in the JI technology optimised for HV AC/DC conversion [5]. It can be seen that a bulk Si

substrate accommodates not only CMOS devices but also a 700 V LDMOSFET with a double PN RESURF layout.

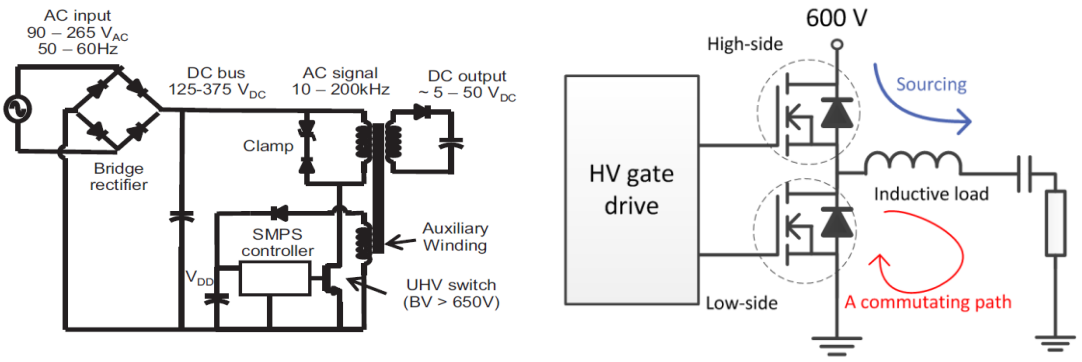

Figure 5.16. A flyback topology for AC/DC conversion [137] (left) and a half bridge circuit with an inductive load (right)

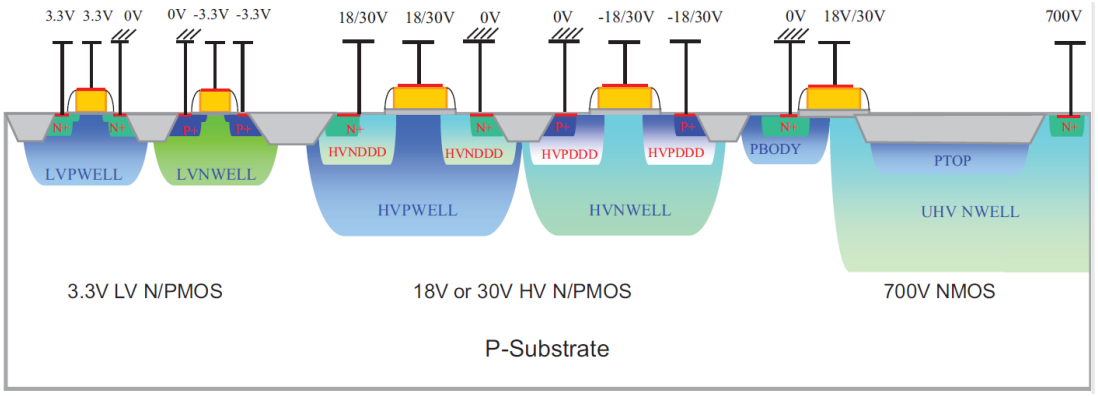

Figure 5.17. The lateral MOSFETs in the JI technology optimised for fully integrated AC/DC Power ICs [137]

In Fig. 5.16, the flyback circuit contains a UHV transistor and an inductor, connected in series across a 375 V DC supply. Two inverse-series diodes are in parallel with the inductor and used for voltage clamping. When the transistor is on, the current will charge the inductor and create a voltage across it, with the two diodes inactive. When the transistor is off, the inductor will be discharged and the polarity of its voltage reversed. During the off-state, the diodes offer a low resistive path for the current and determine the voltage across the inductor. As such, the V_{DS} is clamped to a rated value, which protects the transistor. Without the diodes, there is no way to dissipate the inductive energy in the off-state except for shorting the power MOSFET. The V_{DS} will be fixed at

the device's breakdown voltage until the energy is fully consumed. In this case, the transistor has a higher chance to be destroyed due to the presence of high current and voltage. In the half bridge circuit, the built-in PiN diode of the low-side transistor can be used for circulating the inductive current. When the high and low-side MOSFET is on and off, respectively, the DC bus is feeding the inductor. If the upper switch is turned off, the current flow will be maintained safely by the body diode of the lower switch.

To activate the protection correctly, the added diodes must create an open and short circuit when the MOSFET is on and off. This requires the diode to be able to withstand the voltage used for driving the inductor. To reduce the reverse recovery losses, the diode should be able to remove the stored charges very quickly. It is found that the diode inherent in the Philips SOI LDMOSFET has a reverse recovery time comparable to an ultra-fast PiN diode at room temperature but smaller by a factor of two at 150 °C [46]. This demonstrates the advantage of the SOI technology in high temperature power IC applications. To deplete the inductive energy more rapidly, a resistor or a Zener diode will be placed in series with the diode. This setup raises the voltage across the inductor and makes the current fall more quickly, resulting in a shorter turn-off transition for the power MOSFET. However, doing so will stress the transistor to a greater degree by creating a higher voltage at the drain and therefore the value of the resistor should be carefully selected.

5.4.2.1.2 Circuit topology

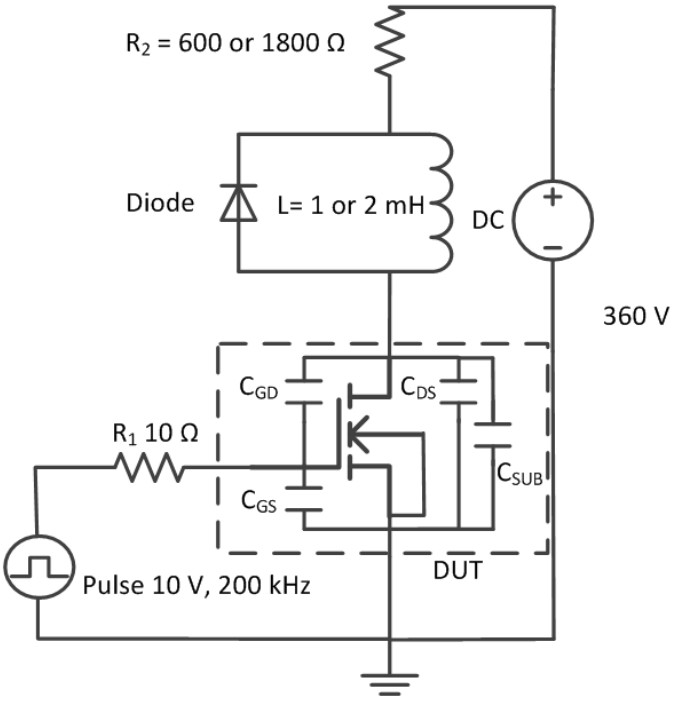

Figure 5.18. A diode-clamped inductive switching circuit in the Mixed-Mode simulation

Fig. 5.18 shows the clamped inductive circuit used in the Mixed-Mode simulation. Enclosed in the dashed box is a device under test (DUT) containing four electrical capacitors, namely C_{GS}, C_{GD}, C_{DS} and C_{SUB} [138]. Using this circuit in the simulation can show the effects of the parasitic capacitors on the device transient characteristics and the temperature rise under multiple cycles. The simulated DUT is either the Philips SOI LDMOSFET or its Si/SiC equivalent. Their device widths are 1 and 1.65 cm respectively to achieve the same electrical resistance and current, at the initial ambient temperature of 150 °C. The gate is switched at 200 kHz via a pulse signal, through a 10 Ω gate resistor, with a 50% duty cycle. The peak voltage is 10 V and the time for rising and falling is equal to 1 ns. The drain contact is linked to a parallel network composed of a diode and an inductor. Attached to this network is a current-limiting resistor connected to a 360 V voltage source. The SOI or Si/SiC transistor is modelled in this circuit for two cases, one of which has a 2-mH inductor and 1800 Ω current-limiting resistor. The other uses 1 mH and 600 Ω for them, respectively. These setups are designed to mimic the inductive switching of low-side LDMOSFETs in a flyback topology under low and high-current conditions and to observe their temperature responses due to self-heating. To speed up

the numerical calculation, other electrical elements are represented by temperature independent compact models. The model for the diode is ideal and has a turn-on voltage of 0.65 V, with no series resistance considered. This means that there are no reverse recovery losses in the diode and that the inductor is hardly de-energised during the off-state of the MOSFET. Nonetheless, such setup allows the current to reach its steady-state value in a few switching cycles. The series resistor (600 or 1800 Ω) is introduced to define the steady-state current and does not stand for any component in a practical circuit. Without this element, the transistor will be quickly biased in the saturation region and suffer thermal runaway. To sum up, this simplified circuit is used to study the dynamic behaviour of the DUT only during inductive switching and is not configured to deliver AC/DC conversion as in Fig. 5.16. The results of this circuit simulation will be demonstrated in Chapter 6.

5.4.2.2 Rectangular Power Pulse (600 V)

5.4.2.2.1 Introduction

The Rectangular Power Pulse (RPP) circuit is one way to evaluate the energy capability and heating effects under the transient overload condition for power LDMOSFETs [118] [139] [140]. The DUT in this setup is stressed with a rectangular power pulse, which is different from the inductive switching circuit where the pulse is triangular in shape [140]. However, it has been proven that the RPP method is equivalent to the clamped inductive switching in terms of judging the device energy capability [140]. Furthermore, this RPP setup is much simpler and the outcomes are unique to the device and do not depend on the circuit elements (e.g. load inductance and capacitance) [17]. One example of using the RPP circuit in practice is shown in [118], where the 600 V Philips SOI LDMOSFET is compared with its bulk Si counterpart. The simulation work of this circuit is demonstrated in [5] which analyses the cooling effect of the 600 V PSOI device in contrast with a SOI in the Philips technology.

5.4.2.2.2 Circuit topology

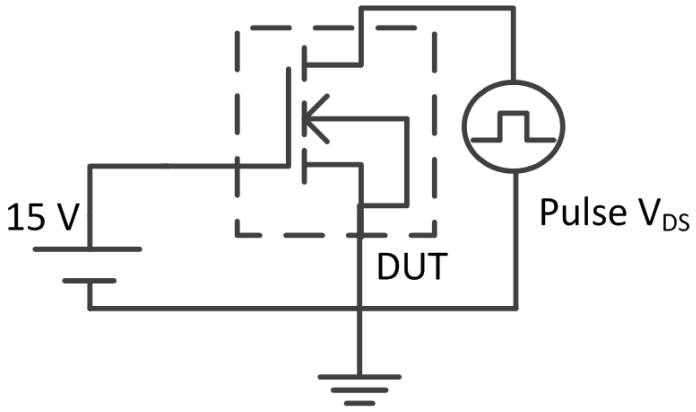

Figure 5.19. The rectangle power pulse circuit used in the Mixed-mode simulation for the 600 V LDMOSFETs

Fig. 5.19 illustrates a simulated rectangle power pulse circuit consisting of the DUT, a 15 V DC source for the gate and a pulse voltage source across the DUT. Involved in this Mixed-mode simulation are the 600 V LDMOSFETs, namely the Philips SOI, the bulk Si transistor and their Si/SiC counterparts. To perform this modelling, all the transistors are simulated as being 1-mm-wide and have a 300-μm thick substrate, under which a thermal contact is defined and fixed at 300 K. Self-heating models are applied to the transistors. The voltage pulse lasts 10 μs, with its value tailored for each device to achieve the same power pulse of 90 W/mm^2. These parameters are intended to energise the DUT and does not represent normal power dissipations [118]. This circuit configuration is aimed to compare the 600 V devices in terms of the transient heating, under the same condition of power density. The results can be found in Chapter 6.

5.4.2.3 Capacitive load switching and Zener-diode-clamped inductive switching (190 V)

5.4.2.3.1 Introduction

The 190 V class LDMOSFETs can be used in battery, In-Vehicle networking, plasma display and electro-luminescent display drivers [129]. In these applications, the transistors are exposed to brief short-circuit durations which are not only determined by their parasitic capacitors but also the external reactive loads. This requires the power

switches to be able to handle this energy smartly such that the resulting temperature rise is minimised. In order to do so, the LDMOS design has to offer a low thermal resistance in such a way that less power is converted to temperature. As shown in section 5.3.3, the PSOI and PSOSIC transistors have a heat conduction path outside the device region. This configuration is expected to deliver a better thermal performance than the SOI, despite the chip are is increased by 22 %. The Si/SiC features a complete removal of the BOX layer so that the heat transfer occurs within the device area. No extra space is needed for the thermal conduction path but the device has to be made 75 % wider, to compensate for the higher resistance compared with the other SOI solutions. In conclusion, the LDMOSFETs built in the Si/SiC, PSOI and PSOSiC substrate have thermal advantage over the SOI, but at the expense of a larger chip area. The effects of these trade-offs for these technologies are evaluated based upon the two switching events that can cause significant heating.

The first case is the turn-on of the device when being connected with a capacitor in parallel. Upon the switching, the voltage across the transistor will drop gradually with the presence of a capacitive discharge current. The second is the turn-off of the device when being connected with an inductor in series. During this transient state, the transistor will still be on while supports a high drain-to-source voltage. These stress conditions can raise the temperature substantially and reduce the device reliability. The circuits to create such switching actions are described as follows.

5.4.2.3.2 Circuit topology

Capacitive load switching

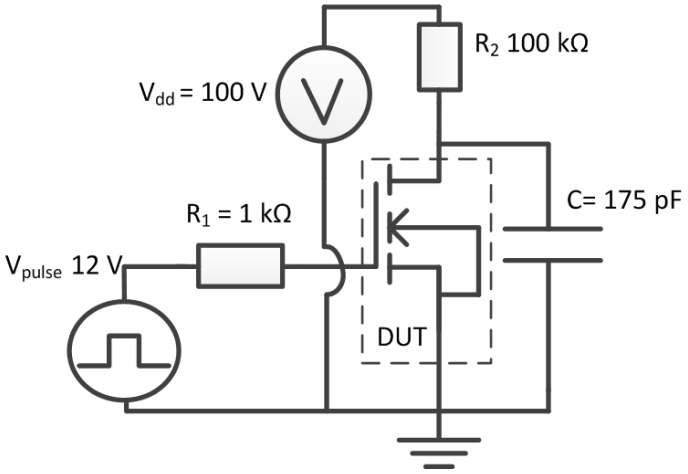

Figure 5.20. The simulated capacitive discharge circuit based upon [62], for the 190 V LDMOSFETs in Si/SiC, SOI, PSOI and PSOSiC technology

Fig. 5.20 illustrates the capacitive switching circuit used in the simulation for the four 190 V LDMOSFETs. This simulated circuit is based upon [62], consisting of a 1 kΩ gate resistor, a 12 V pulse signal, a 175 pF capacitor and a 100 kΩ resistor in series with the transistor and a 100 V voltage source. No protection component is added so all the capacitive energy will be dumped into the transistor. The purpose of this setup is to see how the DUT reacts to the discharge current from the load during the turn-on state. The LDMOSFETs will be simulated at an initial temperature of 27 ^{0}C, with the widths of the Si/SiC and other SOI transistors set to 1.75 mm and 1 mm respectively to achieve the same resistance. Self-heating models are activated.

Zener-diode-clamped inductive switching

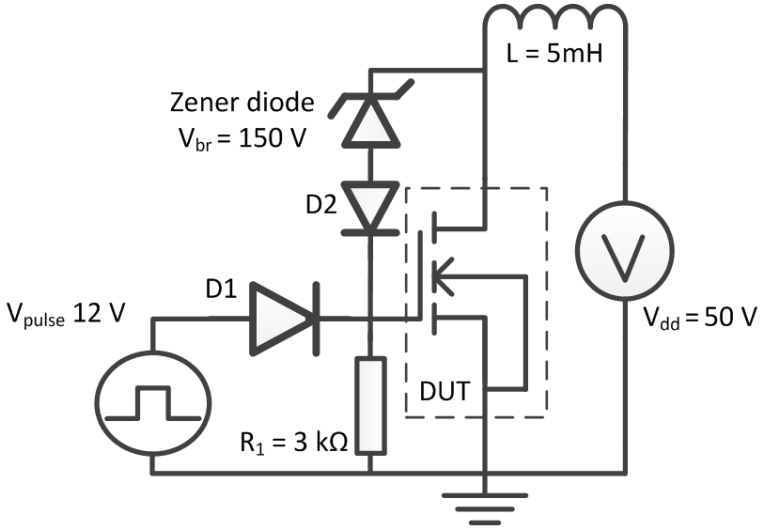

Figure 5.21. The clamped inductive switching setup with a Zener diode, for the 190 V LDMOSFETs

Fig. 5.21 shows the clamped inductive switching circuit based upon [141], used for the 190 V LDMOSFETs in the simulation. The DUT is controlled by a pulse signal of 12 V and protected by two inverse-series diodes. The Zener diode has a breakdown voltage of 150 V whereas the other one is represented by an ideal diode model with a turn-on voltage of 0.65 V. A 5 mH inductor is connected between the transistor and a voltage source of 50 V. This inductor is charged for 10 µs and LDMOS turned off, which triggers the Zener diode conducing current to the ground via a 3 kΩ resistor (R1). Therefore, a voltage is dropped across this resistor, partially switching on the device throughout the inductor discharge period. During this transient period, the drain voltage will be clamped at about 150 V. This setup is designed to see the effectiveness of different device structures in handling the inductive energy during the turn-off period. The initial temperature of the simulation is 27 ^{0}C and the self-heating model is activated.

Chapter 6 TCAD study on the 600 V Si/SiC LDMOSFETs

6.1. Introduction

This chapter provides a TCAD study on the static and dynamic behaviour of the two 600 V Si/SiC LDMOSFETs. The analysis of the DC behaviour is split into three parts. In the first and second part, the Si/SiC devices are compared with their own SOI and bulk-Si counterparts regarding the I-V characteristics. The last part compares the two Si/SiC transistors and their equivalents all together, in terms of the temperature dependence of the leakage current, low and high-side resistance. The study on the transient characteristics are separated into two sections. The first section focuses on the dynamic behaviour of the Philips SOI and its Si/SiC equivalent in the inductive switching circuit mentioned in Chapter 5. Next, comparison is made among the Philips SOI, bulk Si and the two Si/SiC LDMOSFETs, of the heating effects in the RPP circuit introduced in Chapter 5. Much of this chapter has been published in [142] [143] [144] [145].

6.2. DC characteristics

6.2.1. Si/SiC LDMOS in SOI RESURF technology VS SOI

In this section, the first comparative study is made mainly between the Philips SOI and its Si/SiC counterpart to see the effects of the BOX layer and the (SI) SiC substrate on the electrical and thermal properties of the LDMOSFETs. The SOI without the gate field plate is involved in the comparison to observe the effects of the FOX and BOX layer on the leakage current. This structure is also used for analysing the accumulation effect induced by the FOX.

6.2.1.1 Off-state behaviour

As shown in Equation 4.3, the total leakage current can be characterised as the sum of the diffusion component in the neutral region and the generation current in the depletion region [39]. Fig. 6.1 shows the off-state behavior for the Philips SOI and the Si/SiC, respectively. The diffusion current is insignificant in these two structures as the linear doping profile permits full depletion of the thin film. At room temperature, both devices can support more than 600 V and their leakage currents increase up to about 10^{-14} A/µm at 450 V. Beyond this voltage, the tunneling component becomes dominant, raising the total leakage current in both cases. This reveals that both structures have a depletion zone in the drift region, with field strength high enough to allow band-to-band tunneling. This occurs due to the highly doped Si film and inherent SOI layout that induces vertical depletion, causing a strong electric field in the space charge region.

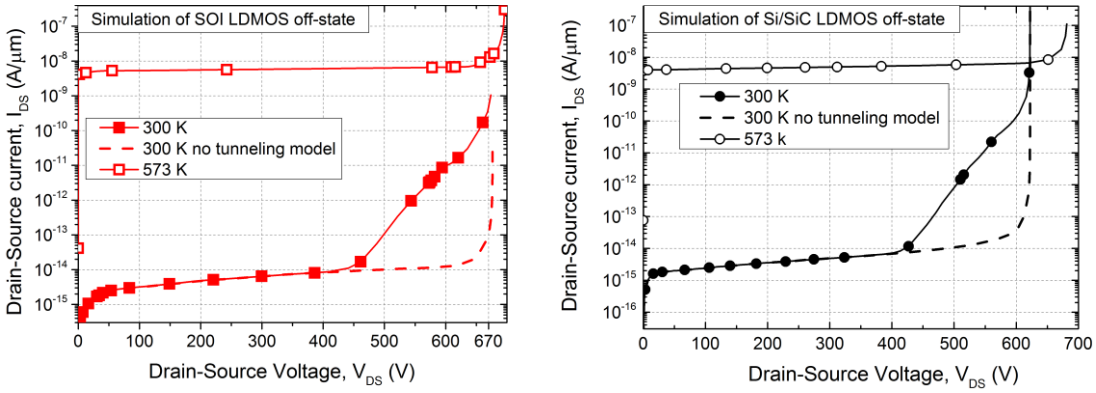

Figure 6.1. OFF-state I–V characteristics of the Philips SOI (left) and Si/SiC LDMOS (right)

At 300 °C, the breakdown voltage increases in both structures to 680 V, a result indicative of an avalanche breakdown mechanism rather than tunneling [39]. However, this relation is not as strong as that of a 1-D junction shown in [39], meaning that the uniform electric field in the drift region compensates for some of the energy of travelling carriers lost at high temperature, thereby reducing the increment of the breakdown voltage. At 300 °C, the leakage current is also increased to around 3×10^{-9} A/µm. The contribution at high voltage from the tunneling component vanishes because of its weak relationship to temperature [46]. Besides, the current generated in the depletion region is a function of intrinsic carrier density and hence is exponentially related to temperature. As a result, the current is dominated by the generation component at high temperatures regardless of

bias condition and the contribution of the tunneling component can be disregarded [46]. This behaviour can also be found in the SOI LMDOSFET without the field plate extension (see Fig. 6.2). It can be concluded that the depletions from the BOX and FOX have equivalent effects on the leakage current at 300 and 573 K.

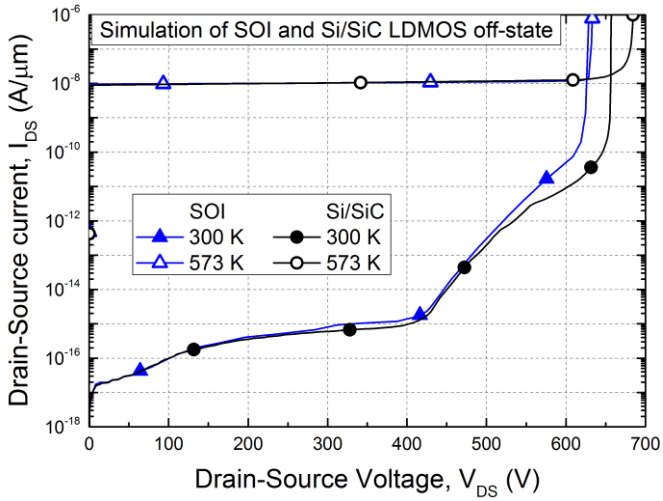

Figure 6.2. Off-state characteristics of the Si/SiC (black) and the SOI without the field plate extension (blue)

6.2.1.2 On-state behaviour

6.2.1.2.1 Isothermal simulation

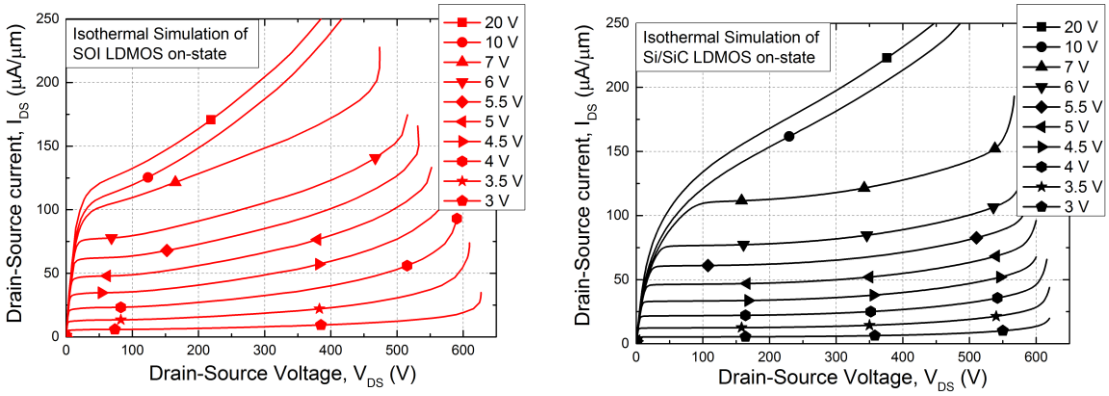

Figure 6.3. On-state characteristics of the Philips SOI (left) and Si/SiC LDMOSFETs (right), under isothermal conditions at 300 K

Fig. 6.3 demonstrates the ON-state behavior of the Philips SOI and the Si/SiC at 27 °C using an isothermal model, which ignores the effects of self-heating. Common to both transistors are threshold voltages of 2 V (shown in Fig. 4.7, Chapter 4) due to the identical

configuration of the channel regions. The gate-to-source voltage ranges from 3 to 20 V. It can be seen that neither device suffers a significant reduction in breakdown voltage at high gate bias because both designs have a high impurity dose at the drain-end of the drift region, thus reducing the Kirk effect [146] and enlarging the electrical safe operating area.

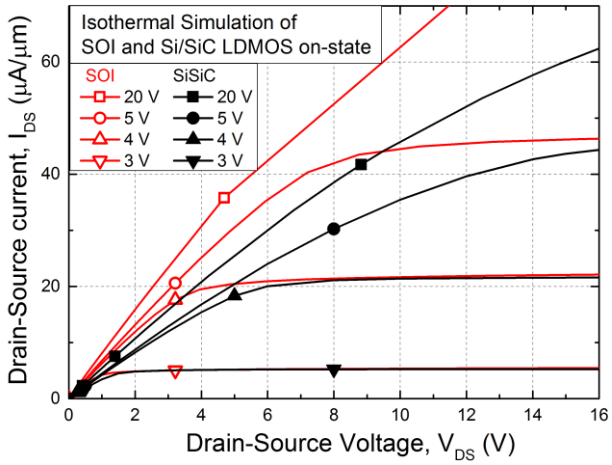

Figure 6.4. the ohmic regions of the I-V curves for the Philips SOI and Si/SiC at 300 K

In the ohmic region, the SOI device conducts more current due to its doping being two times higher than the Si/SiC equivalent (see Fig. 6.4). However, this configuration does not double the SOI current in the saturation region. Instead, both cases have a similar current level at large drain biases up to 100 V (see Fig. 6.3), meaning that a counter effect exists in the SOI and is enhanced with increasing drain voltage. Given that the same channel and geometry of the drift region are designed in the two devices, this phenomenon is likely caused by the BOX layer. At relatively high drain bias, the SOI drift region is depleted from above by the gate field plate and below by the charge-rich region under the BOX. These effectively squeeze the drift region from both sides, limiting carrier transport to the middle undepleted region. In the Si/SiC case, the removal of the BOX removes the bottom field plate effect, leaving the bottom of the drift region undepleted. Therefore, the SOI resistance increases faster against drain voltage and eventually reaches a value comparable to that of the Si/SiC.

6.2.1.2.2 Non-isothermal simulation

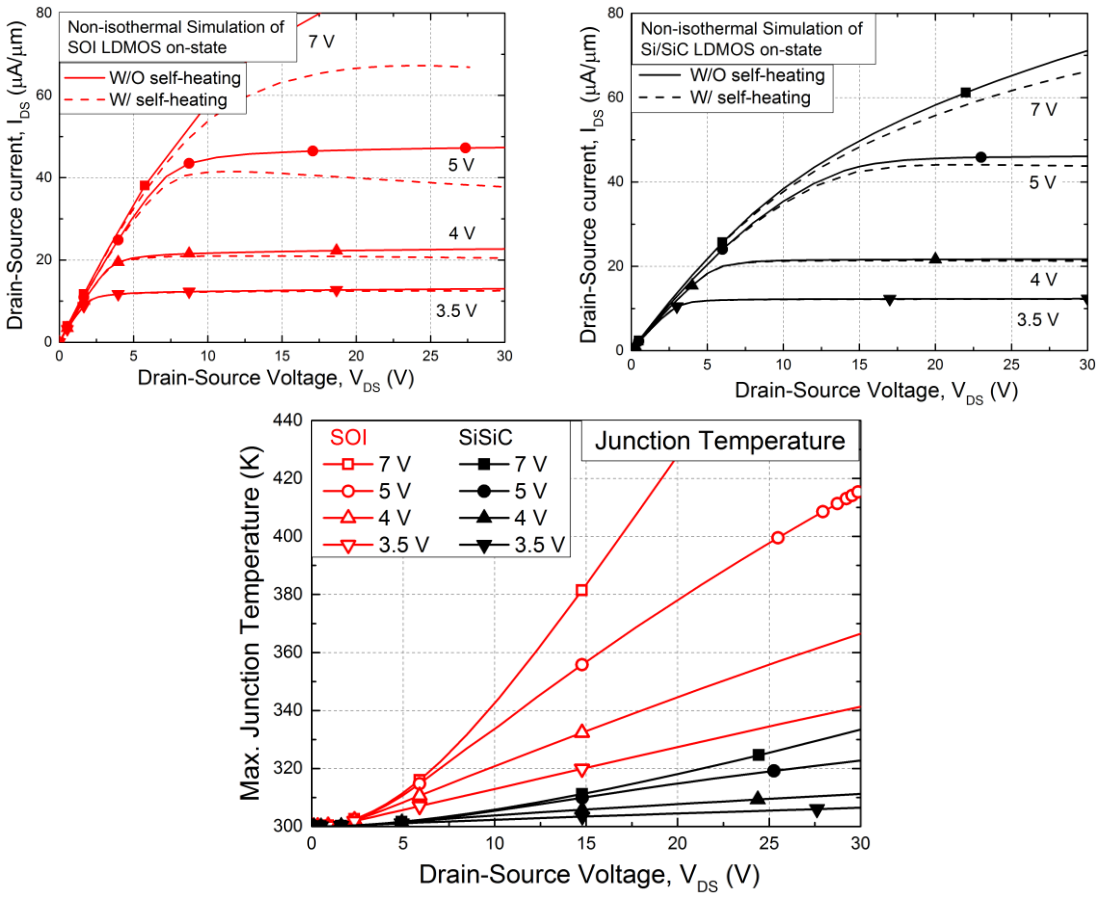

Figure 6.5. The steady-state effect of self-heating on forward characteristics of SOI (left) and Si/SiC LDMOS (right), as well as their junction temperature (bottom)

The steady-state effects of self-heating in both the Philips SOI and Si/SiC LDMOS transistors are seen in Fig. 6.5 (left) and (right), respectively. The isothermal sets for both devices are included for comparison and represented by solid lines. The dashed lines indicate the I–V characteristics produced from nonisothermal modeling. The isothermal and nonisothermal data are in good agreement in the linear region irrespective of gate voltages, as well as in the saturation regime at low gate bias (e.g., 3.5 V). However, they diverge as resistance and current increase. This gives rise to substantial power losses that increase the local temperature, thereby reducing carrier mobility. This situation is worsened at increasing gate and drain voltages and eventually significant deviation occurs, with the effect of negative resistance becoming evident in the nonisothermal cases. In the Si/SiC device, this is not obvious until the gate voltage is raised to 5 V as opposed to around 4 V in the SOI. Fig. 6.5 (bottom) is from the same simulation and shows the

corresponding temperature rise for each nonisothermal I–V simulation. Internal temperate rises sharply against drain voltage in the SOI, with the temperature at any given point over four times greater in this substrate than in the Si/SiC. Furthermore, temperature sensitivity to gate voltage is lower in the Si/SiC, which reduces the risk of thermal-induced failures at high gate biases.

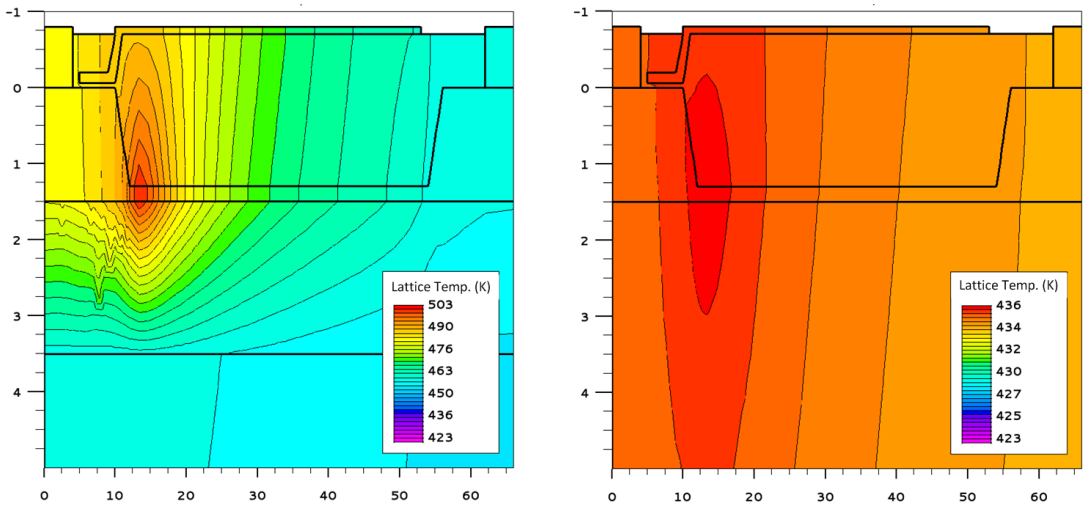

Figure 6.6. Temperature contours of (left) SOI and (right) Si/SiC under V_{DS} = 15 V, V_{GS} = 10 V conditions (axes units: μm)

It is reported in [5] [147] that the linear doping profile will cause a non-uniform heating in the SOI transistor and this phenomenon is demonstrated in Fig. 6.6 for the Philip SOI and Si/SiC transistors. In the two devices, the gate and drain contact are supplied by 10 and 15 V DC voltage source, respectively. With the ambient at 423 K, the maximum temperature in the Si/SiC is 436 K, compared to 502 K in the SOI. Both devices have a hot spot located at the source side of the drift region, from which heat spreads toward other areas, forming a nonuniform temperature profile. However, thermal diffusion is hampered in the SOI due to the BOX, which elevates the temperature in the left part of the device and threatens the gate and source contact. In the Si/SiC transistor, the SiC substrate removes most of the heat from the Si, which reduces the temperature gradient in the drift region. As a result, the Si/SiC transistor can be operated with a higher power for a given junction temperature, at the same power for a much reduced junction temperature, or at a similar power level at an elevated ambient temperature.

6.2.1.2.3 Accumulation effect

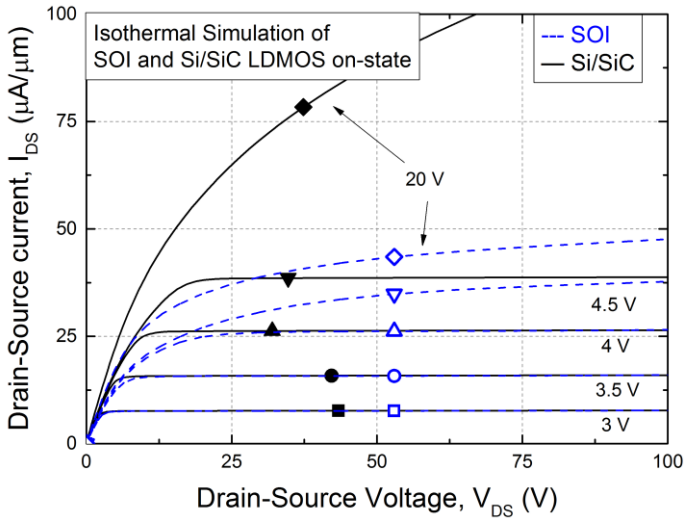

Figure 6.7. On-state characteristics of the Si/SiC (black) and SOI without the field plate extension (blue), under isothermal conditions.

To observe the accumulation effect in the SOI, comparison is made between the on-state I-V curves of the Si/SiC and SOI LDMOSFET without field plate extension. Removing the field plate removes the top-side RESURF effect from the SOI, so inducing a one-sided RESURF, similar to the Si/SiC. In order to do so, the base doping density in the Si/SiC has to be reduced from 8×10^{15} to 4×10^{15} cm^{-3}, a value used in the SOI to achieve a breakdown voltage above 600 V. As such, the Si/SiC is more resistive than before but has a linear doping profile the same as the SOI without the field plate extension. Fig. 6.7 presents the isothermal simulation of the SOI and Si/SiC LDMOSFET with the gate biased from 3 V to 20 V at 300 K. It can be observed that the difference becomes larger between the on-state resistances of the two structures with higher gate voltage. Given that the same doping profile is employed in each case, this effect occurs mainly owing to the design of the gate contact. In the SOI, the gate setup affects the channel region mainly, leaving the drift region unmodulated. Conversely, an accumulation channel is formed in the top of the drift region by means of the gate extension in the Si/SiC. With larger applied voltage, more electrons are attracted in this layer, which greatly reduces the drift resistance. However, the high applied voltage will enhance hot carrier injection and therefore reduce the device's reliability.

6.2.2. Si/SiC LDMOS in PN RESURF technology VS Bulk Si

6.2.2.1.1 Off-state behaviour

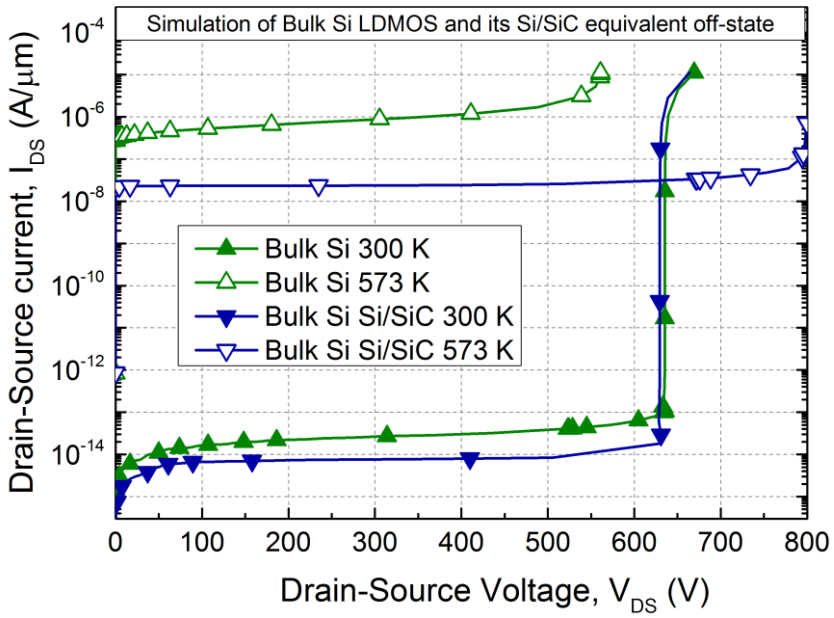

Figure 6.8. Off-state characteristics of the Si/SiC (dark blue) and the Bulk Si counterpart (green), at 300 and 573 K

As can be seen in Fig. 6.8, the Si/SiC device has a slightly reduced breakdown voltage and a lower leakage current compared with the bulk Si at 300 K. At 573 K, the effects of the Si/SiC architecture are more noticeable, resulting in a blocking voltage 250 V higher and a leakage current two orders of magnitude lower than the Bulk-Si. This indicates that the Si/SiC structure breaks down with the avalanche mechanism [39] and has a much better electrical insulating property. Given than the LDMOS topology is common to the two devices, the degradation of the bulk Si is solely ascribed to the p-type Si substrate. This region acts as a conductor at high temperature and has a substrate contact 66 μm wide, which creates a very strong parasitic bipolar effect. It is believed that this effect causes the reduction of the breakdown voltage and increase of leakage current in the bulk-Si.

6.2.2.1.2 On-state behaviour

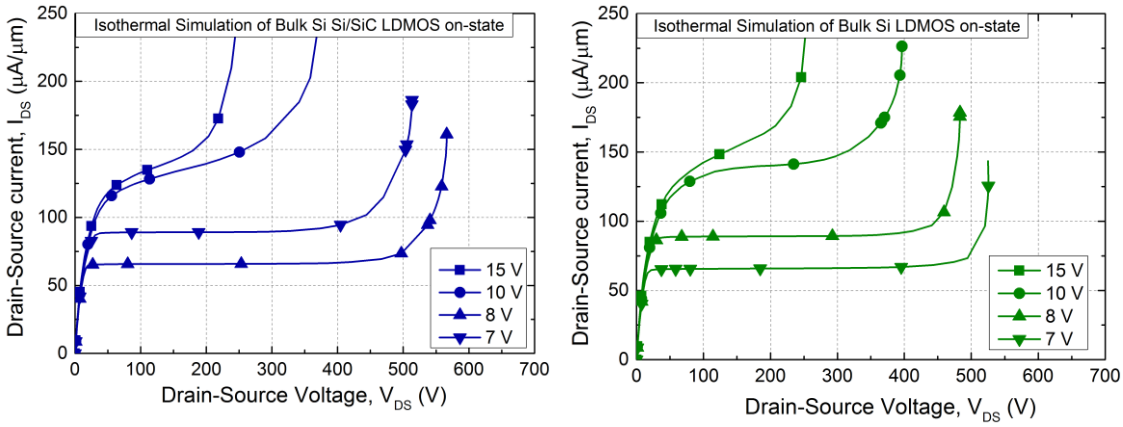

Figure 6.9. On-state characteristics of the thick-film Si/SiC (left) and bulk Si LDMOSFETs (right), under isothermal conditions (300 K)

In the on-state, the two devices have a nearly identical behaviour under isothermal conditions (Fig. 6.9). Their specific on-resistances are calculated to be 90.6 Ωmm^2 at V_{DS} = 1 V and V_{GS} = 15 V, which is similar to that in [99]. However, both transistors have a poorer forward breakdown capability compared to the 600 V devices in the Philips technology, meaning that they are more susceptible to the Kirk effect [62]. This is because their RESURF doses are uniformly arranged in the drift regions. With the presence of mobile charge in the on-state, the amount of net positive charge will be reduced and the RESURF condition disturbed at the drain side. By applying a higher V_{DS} and V_{GS} value, the charge unbalancing is more severe and therefore a lower breakdown voltage is induced. If there are more donors at the drain side, a higher current density and drain-source voltage are needed to activate the Kirk effect. The linear doping profile in the Philips SOI is an embodiment of this very idea which minimises the electrical field at the p body/N- junction.

6.2.3. Temperature effects on the Si/SiC, SOI and Bulk Si LDMOS

In this section, the comparative study on the 600 V LDMOSFETs will be supported by their leakage current, low and high-side specific on-resistances. These parameters are extracted from the I-V curves produced by the DC simulation, over the temperature range of 27-300 ^{0}C. The extraction conditions have been mentioned in Chapter 3 and will be

briefly stated in the paragraphs below for each parameter. For convenience purposes, the thin-film SOI device and its equivalent Si/SiC device are referred to as 'SOI' and 'SOI Si/SiC' respectively. Similarly, the acronyms for the bulk-Si and its Si/SiC equivalent are 'Bulk-Si' and 'Bulk-Si Si/SiC'. The goal of this section is to see the pros and cons of the Si/SiC architecture in contrast with other solutions for high temperature application.

6.2.3.1.1 Leakage current

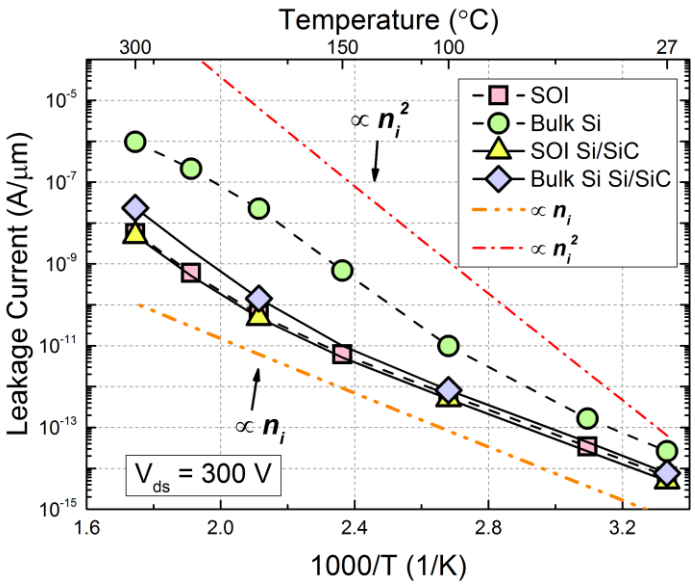

Figure 6.10. Temperature dependence of leakage current for the SOI, Bulk-Si, SOI Si/SiC and Bulk-Si Si/SiC LDMOS at a drain voltage of 300 V, along with two lines ($\propto n_i$ & $\propto n_i^2$) representing generation and diffusion component, respectively

Fig. 6.10 presents the variation of reverse current with temperature for the two Si/SiC LDMOSFETs and their corresponding designs in SOI and Bulk-Si technology [46] [99]. Also shown are two dashed lines that indicate a (n_i), or n_i^2 relationship between temperature and intrinsic carrier concentration, which, respectively, indicates generation and diffusion leakage mechanisms. These two outweigh other leakage components arising from the interface, tunnelling and avalanche effects, because the devices are simulated here with low interface charge and a drain-source voltage of 300 V [46] [117]. Over the temperature range of 27-300 ^{0}C, the SOI and its Si/SiC equivalent has very similar reverse current, slightly lower than that of the Bulk-Si Si/SiC which has a much thicker Si layer, thereby increasing the generation component despite higher carrier lifetime [46]. The gradients of their leakages against temperature are similar and can be

mostly described by the $\propto n_i$ line (see Fig. 6.10). However, the Bulk-Si LDMOS distinguishes itself from the others by having a much larger leakage current, whose increased rate approaches the $\propto n_i^2$ line. The reason for this is that the generation leakage is raised when the depletion region expands into the P type substrate of the Bulk-Si transistor, and that a vertical diffusion current appears owing to the absence of electrical isolation.

6.2.3.1.2 Low-side specific on-resistance

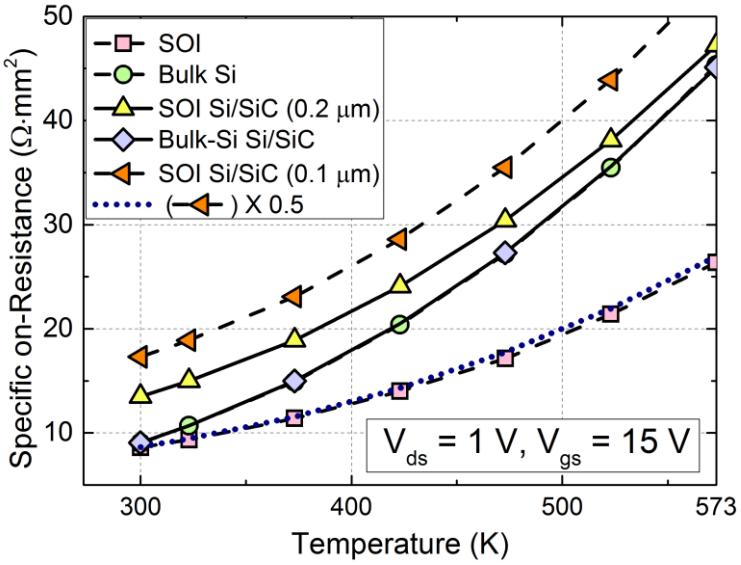

Figure 6.11. Temperature dependence of low-side specific on-resistance for the SOI, Bulk-Si, Bulk-Si Si/SiC and two SOI Si/SiC transistors that have differing Si layer thickness, namely 0.2 and 0.1 μm. The dotted line is derived from halving the curve for the SOI Si/SiC LDMOS with a 0.1-μm-thick Si film

The effect of temperature on the low-side specific on-resistance of different devices can be seen in Fig. 6.11. The bias conditions of V_{ds} = 1 V and V_{gs} = 15 V are applied in the simulation to minimise the influence of channel resistance and "pinch-off", thus the total resistance mainly depends on the quantity of donors in the drift region. All the transistors are designed with an effective dose [93] of around 3×10^{12} cm^{-2} [99] [144] in their drift regions for 600 V, except for the Philips' LDMOS having about 6.8×10^{12} cm^{-2} on account of the double RESURF effect [135]. It is worth noting that in the SOI and SOI-like Si/SiC device, a charge-rich region will be formed underneath the FOX because of the gate extension and applied gate bias [28]. However, the effect of such induced electrons on the resistance is limited and not as substantial as that shown in [93], where

one third of the drift region is flooded with accumulation carriers, accounting for 68% of the total current conduction [93].

Under this setting, very high charge density (cm^{-3}) is present in the SOI group and their carrier transports are dominated by impurity scattering [46] [117]. By contrast, the thick-film (16 μm) transistors accommodate far less impurity atoms per unit volume and hence lattice scattering prevails [46] [117]. This brings about the on-resistance of the SOI-like Si/SiC transistors less dependent on temperature compared with the thick-film Si/SiC counterpart, but in return a higher resistivity is observed, with the 0.1-μm-thick device having the least conductance due to the highest impurity density (see Fig. 6.11). No difference in the resistance is observed between the Bulk-Si and its equivalent Si/SiC device, because the p-substrate region in this Si/SiC plays the same role as the one in the Bulk-Si structure, facilitating a back RESURF for the drift region. However, the thin-film SOI exhibits a resistance slightly lower than those of the two thick-film LDMOSFETs at room temperature. Its degradation rate with temperature is also smaller than those of any other structures. This is because the transistor features a double SOI RESURF effect, and can be regarded as two SOI devices with a 0.1-μm Si layer working back-to-back [135], as can be demonstrated with the dotted line in Fig. 6.11, which is obtained from halving the results of the 0.1-μm Si/SiC, which operates with just a single SOI RESURF technique.

Compared to the SOI, the thin and thick film Si/SiC transistors have 56% and 5% more low-side resistance at 300 K respectively, increasing to 79% and 71% at 573 K. Therefore, it is advantageous in high temperature operations that high doping density and high order RESURF are employed in the unipolar transistors. In the case of the Si/SiC architecture, a 3D super-junction layout [148] could be the answer to improving the on-resistance, as the SAD effect is weak in the Si-on-(SI) SiC structure such that the depletion of the of 3D RESURF structure is mainly induced from the sides, in the direction of device width, leading to a double RESURF effect with relatively high doping. The Si/SiC LDMOSFET with this 3D RESURF layout can be found in Appendix B.

6.2.3.1.3 High-side specific on-resistance

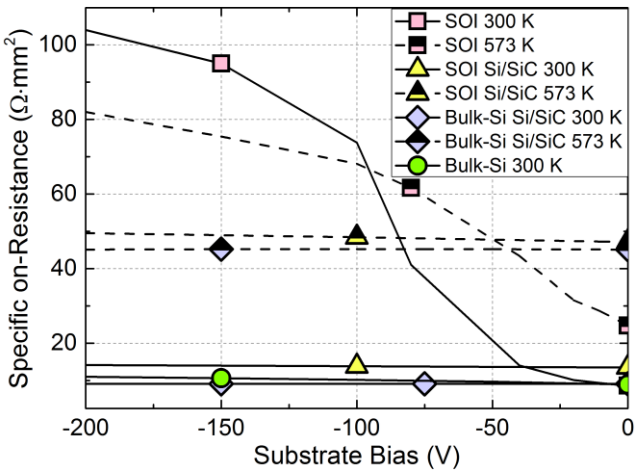

Figure 6.12. Relationships between specific on-resistance and substrate bias for the simulated LDMOSFETs at 300 K and 573 K, excluding the one for the Bulk-Si at 573 K

Fig. 6.12 demonstrates the high-side specific on-resistance as a function of substrate voltage for the simulated transistors at ambient temperatures of 300 and 573 K. The gate and drain terminals are biased at 15 V and 1 V, with the substrate voltage varying from 0 to -200 V. This simulation setup is equivalent to that of a practical high-side operation. For example, to drive a high-side LDMOSFET in the linear region, the bias settings are 199 V, 214 V, 200 V and 0 V for the source, gate, drain and substrate contact. These are the same as applying 0 V, 15 V and 1 V for the source, gate and drain, with the substrate biased at -199 V. Doing so can reduce the time it takes in the simulation to ramp up the voltages. In order to reduce the effect of substrate bias on the backgate (P body), the N-well in the Bulk-Si structure is extended laterally to enclose the channel region [149]. Furthermore, this LDMOS is excluded from the simulation at 573 K, owing to the activation of the parasitic BJTs that distorts the device's characteristics.

It can be found in Fig. 6.12 that the Si/SiC devices have on-resistances insensitive to the substrate bias regardless of ambient temperature, so does the Bulk-Si at 300 K. The common reason is that they all have a high resistive substrate which sustains most of the applied voltage, thereby minimising the depletion in the Si active region [149]. In the Bulk-Si and its equivalent Si/SiC device, the thick Si layer (16 μm) and application of charge compensation (triple RESURF) [150] also alleviate the effect of substrate bias, by increasing the depletion limit and decreasing the depletion width respectively. However,

in the SOI device, potential is confined by the BOX so that the depletion in the top Si film is enhanced. This significantly lessens the effective area for current conduction in the already-thin Si layer, resulting in a rapid rise of on-resistance up to -100 V at 300 K (see Fig. 6.12). Beyond this value, the expansion of the depletion region with the substrate bias is hindered by the formation of an inversion layer [150], leading to a less drastic increase in on-resistance. Similar features are observed in the curve for the SOI at 573 K, but the impact of substrate bias seems to be weakened, yielding an even less abrupt change and eventually the resistance is lower than that at 300 K. This is because, with the presence of a large amount of thermally generated carriers, the depletion region does not function as strong a potential barrier as at 300 K.

Despite reducing low-side resistance as shown in the previous section, the SAD effect in this case is disrupted by the substrate bias, thereby increasing the resistance. Compared with the SOI, the equivalent Si/SiC achieves 86% and 40% reduction in the high-side resistance at 300 K and 573 K respectively, under a substrate potential of -200 V. Likewise, the Bulk-Si Si/SiC has 91% and 36% lower high-side resistance at 300 K and 573 K. By introducing a step Si film on a thicker BOX layer [151], this downside in the SOI can be partially resolved but the dependency on substrate bias still exists, which gives rise to a difference between low and high-side resistance.

6.3. Dynamic characteristics

6.3.1. Philips SOI vs Si/SiC on inductive switching

This section demonstrates the simulation results of the diode-clamped inductive switching circuit, for the Philips SOI and its Si/SiC equivalent (see section 5.3.1, Chapter 5). Firstly, device behaviour under multiple switching actions are presented and discussed. Secondly, the analysis will focus on their transient currents and power in one cycle, to study the origin of the high turn-on losses and the resulting transient heating.

6.3.1.1 Overview of switching characteristics

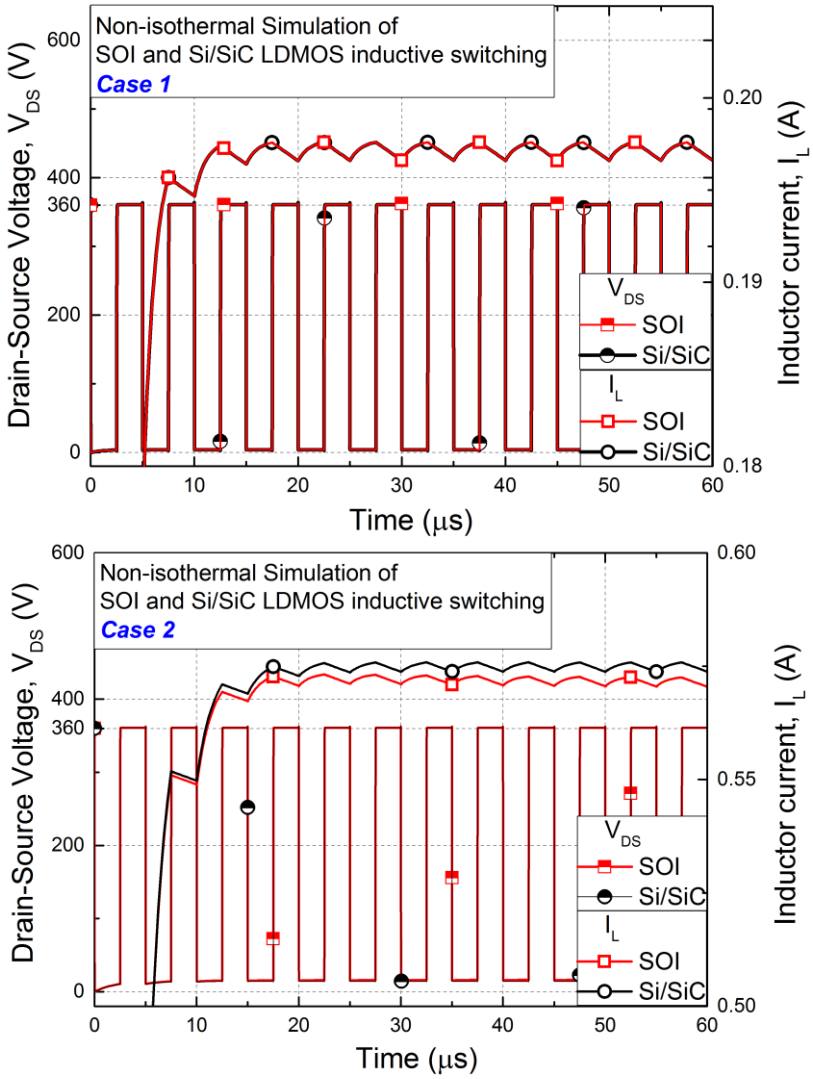

Figure 6.13. Drain–source voltage and inductor current for the two transistors during V_{GS} = 10 V, 200 kHz switching nonisothermal simulations. The inductor and current-limiting resistor are 2 mH and 1800 Ω in Case 1 (Top) and 1 mH and 600 Ω in Case 2 (Bottom)

Fig. 6.13 shows the drain–source voltage and inductor current for the 600 V SOI and Si/SiC LDMOSFETs under inductive switching conditions. The simulation starts at an ambient temperature of 150 °C and lasts 60 μs. Two cases are considered in which the transistors are simulated under high and low-current conditions, both within the linear region. It can be seen that the two LDMOSFETs have the same performance under low current conditions (Case 1). Under high-current conditions (Case 2), a small current mismatch exists due to increased self-heating effects.

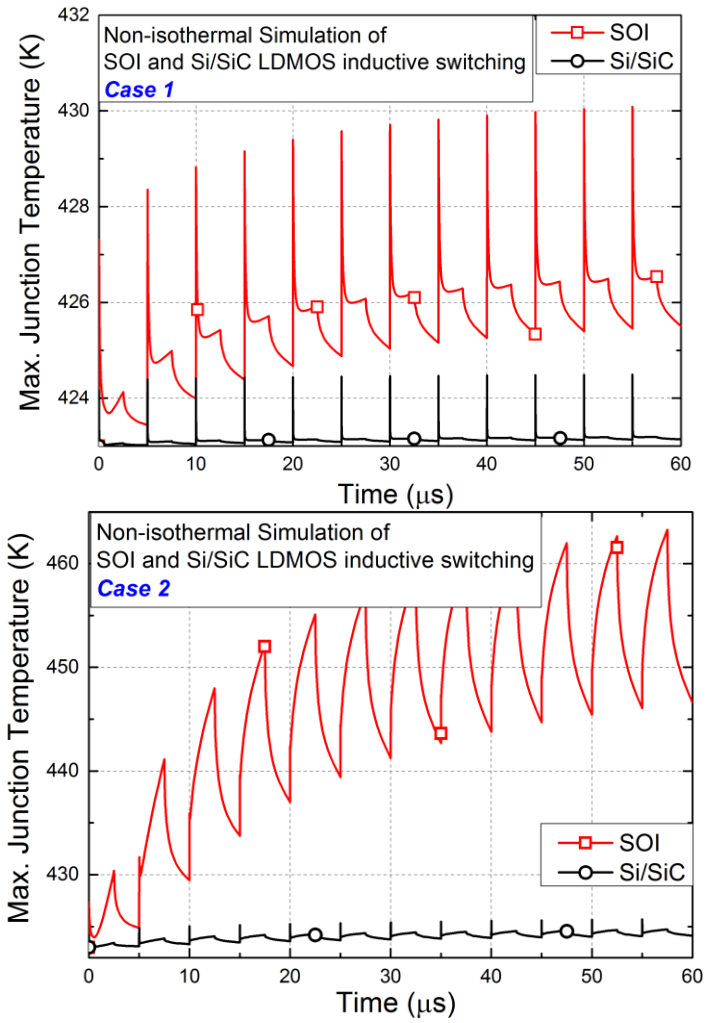

Figure 6.14. Dynamic temperature response of the two transistors in the nonisothermal switching for Case 1 (top) and Case 2 (bottom)

Fig 6.14 shows the differing self-heating effects, presenting the corresponding junction temperature of the transistors for both conditions. In both cases, the SOI heats up faster and reaches a higher steady-state temperature. The pulsed operation allows a period when the devices can be cooled down but introduces transient losses that can be substantial at high frequency. In Case 1, temperature spikes appear as the SOI or Si/SiC device is turned on, meaning that high power is dissipated in this dynamic state. However, these peaks are only very short in duration and the temperature drops briefly, before on-state losses dominate. After this, the conduction current raises the temperature for as long as the transistor is on.

In Case 2, the device delivers a current about three times that of Case 1, which accounts for the rapid temperature response in the SOI (see Fig. 6.14). The temperature spikes due to turn-on losses are hardly seen in this waveform and the majority of heating is due to the conduction losses. If this pulse action continues, the temperature will rise and eventually fluctuate around a steady-state value. The increase in temperature leads to a degradation in the device's electrical and thermal properties, causing an increase in losses compared to those at the initial temperature.

As can be seen in Fig. 6.13, there is a negligible difference between the electrical behaviours of the two technologies, a result indicative of very similar on-state power losses in the two MOSFETs. However, the thermal resistance and capacitance of the SiC substrate are much improved, allowing it to work like an embedded heat sink regulating device temperature close to that of the ambient environment (423 K). In Case 2, the peak temperature in the Si/SiC is 425 K, lower than 463 K in the SOI, thereby increasing reliability. The drawback is that this layout requires 65% more chip area than the SOI at 423 K but smaller external heat sinks can be employed due to this thermally aware design, which can lower the total volume of the power module.

6.3.1.2 Analysis of transient currents and power

To reduce the inductor size further, the power transistor can be operated at megahertz frequencies [152]. In this case, the device will undergo more switching cycles per second and shorter time for cooling, thereby increasing the junction temperature at a faster rate. As can be seen in Fig. 6.14, the turn-on events contribute a great deal to the transient heating in the SOI and Si/SiC under the low current conditions. In the high current case, the conduction heating is minimised in the Si/SiC but the temperature spikes during the turn-on are still significant. When the switching speed of the power device is elevated, the temperature rise will be related more to the turn-on losses.

Therefore, a study on the origin of this dynamic behaviour is crucial to achieving reliable operation at very high frequencies. To analyse the transient losses, the currents and power dissipations of case 1 are given in Fig. 6.15, 6.16 & 6.17.

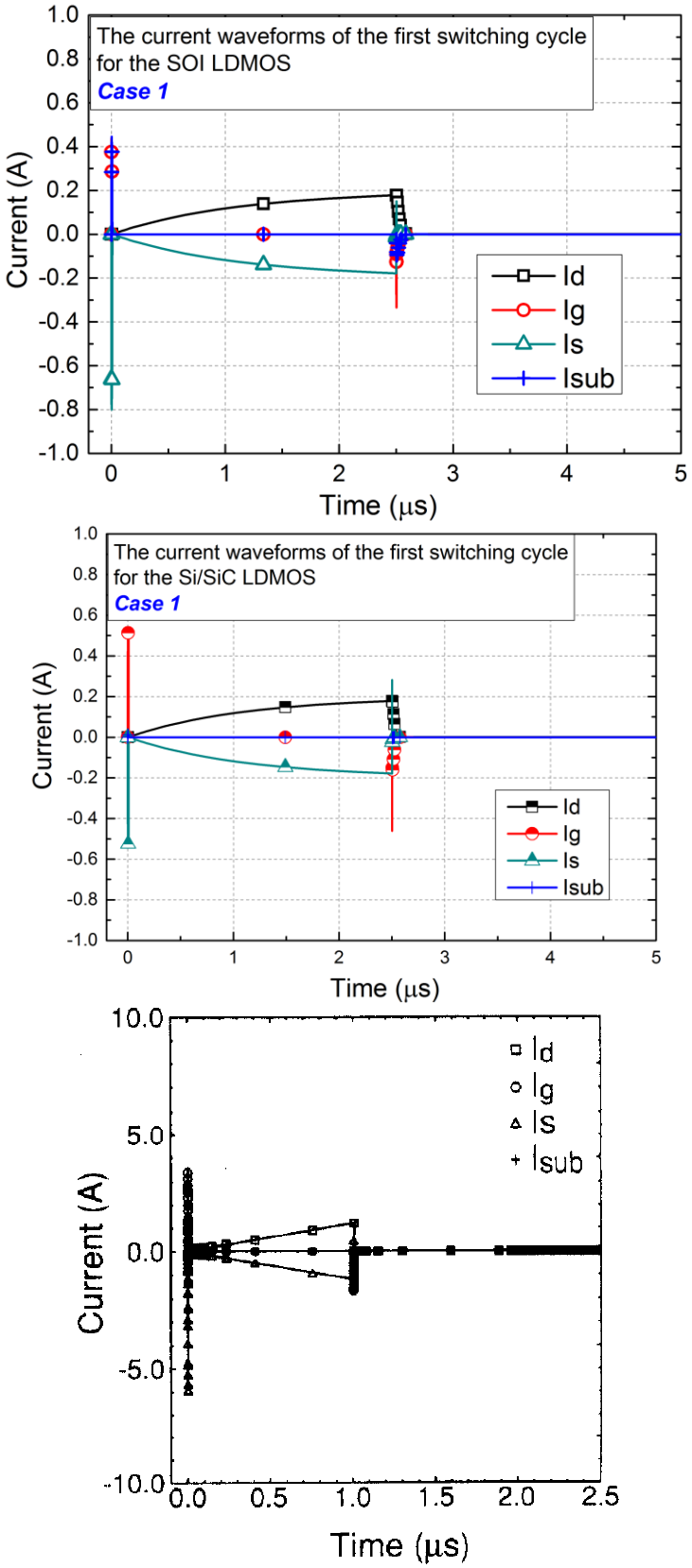

Figure 6.15. The current waveforms of the first switching cycle for the 600 V Philips SOI (top), 600 V Si/SiC (middle) and the 200 V SOI LDMOSFET in [152] (bottom)

Fig. 6.15 demonstrates the currents of four LDMOS terminals during the first switching cycle of Case 1, for the Philips SOI and Si/SiC structure. They are the drain, gate, source and substrate current. Also shown are the current waveforms taken from [152], where a 200 V SOI LDMOSFET was simulated and tested in a clamped inductive circuit at 1 MHz. These results are used to aid the analysis of the switching behaviour of the two transistors and are not involved in the detailed comparison of transient current and instant power. The current is positive if it is flowing into the electrode, otherwise it is negative. Compared with the results in [152], the drain and source current of the Philips SOI are less linear in the on-state, owing to the presence of a series resistor (see Fig. 5.18). Other than that, they are very similar to each other and have surge currents at the gate, source and substrate during the turn-on (For better views for these of the 200 V SOI, please refer to [152]). These inrush currents are caused by the parasitic capacitors and are many times larger than their steady-state values. After this transient period, the device is in the on-state where the source and drain current are the same except for their directions, with no current flowing through the gate and substrate. This situation continues until the device is turned off, resulting in a drop in the drain current. At this moment, instantaneous currents appear again at the gate, source and substrate, with their directions being reversed as opposed to the turn-on cases. Once all the currents are gone, the device is completely off and the drain potential is clamped to a value which is the sum of the DC supply and the voltage across the inductor. The on-state currents of the Si/SiC are exactly the same as those of the Philips SOI. However, the Si/SiC produces slightly higher transient currents at the gate and source, probably due to it being wider than the SOI for achieving the same rated current. Despite this, the substrate current of the Si/SiC is negligible throughout the whole cycle owing to the absence of the capacitive effect arising from the buried oxide.

The details of the transient currents for the SOI and Si/SiC during turn-on and off of the fifth cycle can be seen in Fig. 6.16. In both devices, the turn-on event starts at 20 μs and lasts for 10 ns. This delay results from the charging of the C_{GS} and discharging of C_{GD}, C_{DS} and C_{SUB}. The substrate capacitive current is insignificant in the Si/SiC whereas this is as significant as other dynamic currents in the SOI. There are more transient current flowing out of the source than into the drain because of the extraction of energy in the C_{GD} and C_{DS} [153]. Once the devices are switched off, the source

current is suddenly reversed and then falls to zero briefly whereas the drain current continues to flow for about 70 ns. This means that the charged carriers from the drain are used for energising the C_{GD} and C_{DS} rather than travelling to the source [153]. The negative substrate current in the SOI means that electrons are attracted to the positive drain bias and migrate to the bottom of the BOX layer. Throughout the switching cycle, the gate current of each transistor is related to other current components following the Kirchhoff's current law.

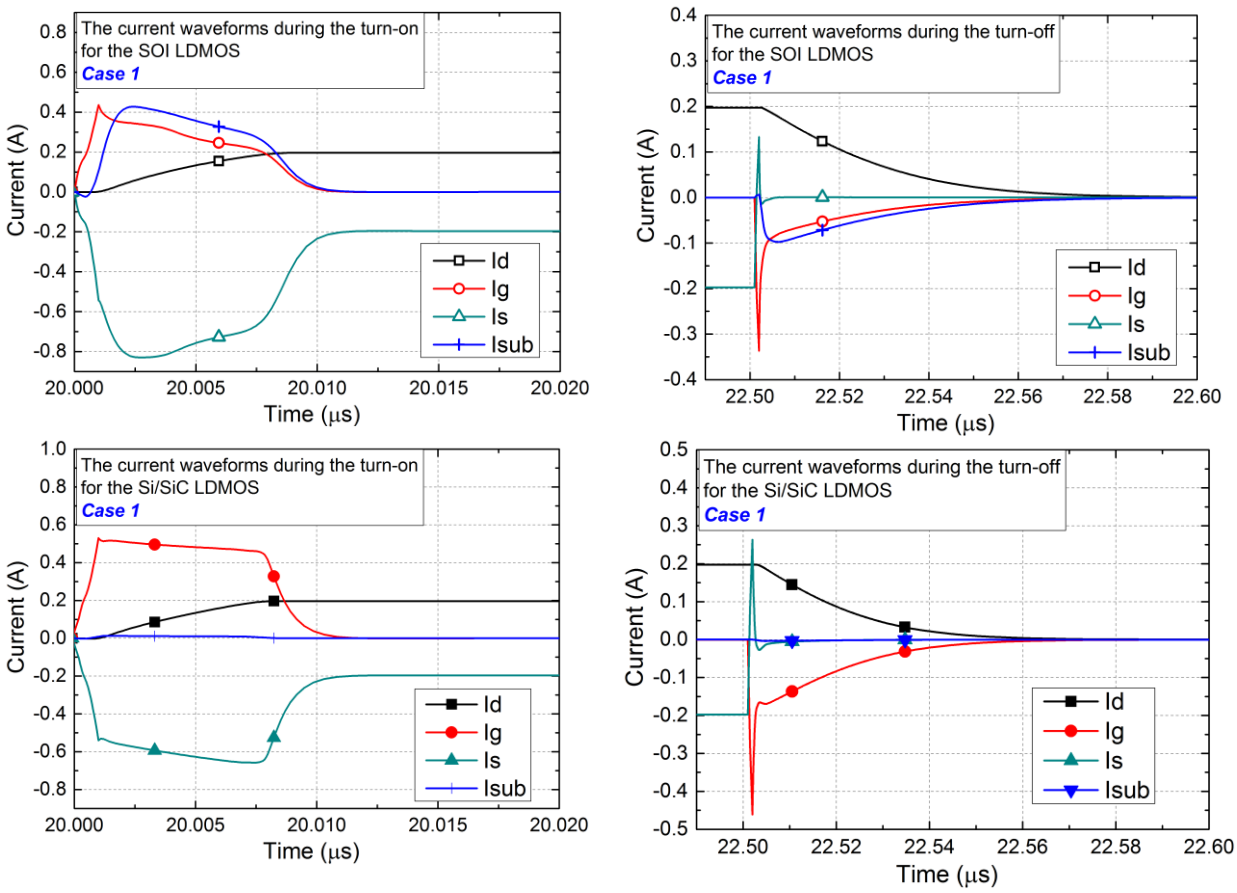

Figure 6.16. The SOI and Si/SiC transient currents during the turn-on and off, in Case 1

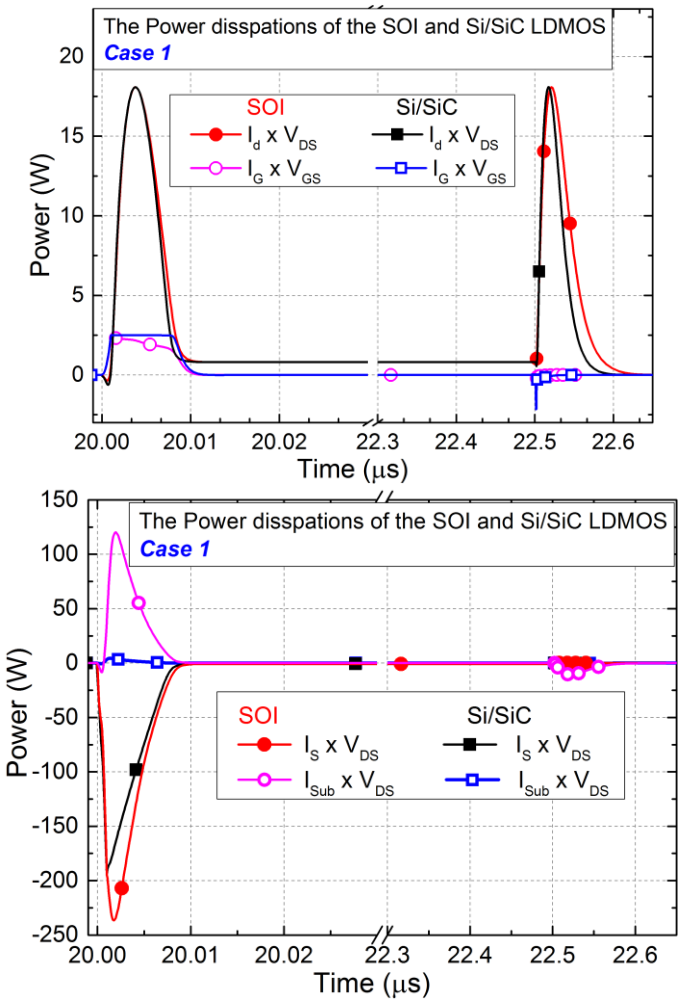

Figure 6.17. Power disspations calculated by $I_D \times V_{DS}$ and $I_G \times V_{GS}$ (top), and by $I_S \times V_{DS}$ and $I_{SUB} \times V_{DS}$ (bottom) for the Philip SOI and Si/SiC in one cycle

According to [152], the instantaneous power is calculated from the product of voltage and current for both drain and gate (see Fig. 6.17 top). Despite differences in the substrate and device width, the two LDMOSFETs generate a similar amount of power losses in one cycle. The Si/SiC dissipates less drain-to-source switching losses during the turn-off event but has higher gate charge losses. In each device, the power is constant throughout the steady state and has bell-shaped distributions during the transient. The turn-on power pulse is about 10 times shorter than the turn-off but they have the same peak value of 18 W. The gate-drive losses are much lower than the switching losses. These results indicate that the devices are more likely to be heated up quickly during the turn-off than other states, but the temperature responses in Fig. 6.14 show otherwise.

In [153], Shen et al. analysed the suitability of using the product of drain voltage and current for the calculation of the switching losses. It was found that this method

underestimated the turn-on losses by ignoring the additional current arising from the capacitive discharge, and overestimated the turn-off losses by disregarding the capacitor charging with the assumption that all the drain current flowing through the channel to cause the joule heating [153]. To consider those effects, the channel current was introduced to replace the drain current for the calculation of the power losses [153]. Based upon this, the instantaneous power is obtained by multiplying the drain voltage and the source current as this current behaves similarly to the channel current in [153]. The results are demonstrated in Fig. 6.17 bottom, along with the power calculated from the product of the drain voltage and substrate current. It can be seen in both transistors that the turn-on results in the power losses are considerably larger than the turn-off, which can explain the temperature spikes in Fig. 6.14. In the SOI, this heating can depend more on the current at the source since the substrate current generates losses in the bulk region below the BOX layer rather than in the top Si [154]. Compared with the SOI, the Si/SiC has less turn-on losses and transient heating with insignificant substrate capacitive effect. These are very attractive features to power ICs operating at very high frequency (> 1 MHz).

6.3.2. Si/SiC, Philips SOI vs Bulk Si LDMOS on RPP circuit

This section shows the temperature responses of different 600 V LDMOSFETs in the RPP circuit introduced in Chapter 5. The simulated power transistors are the Philips SOI, bulk Si and their Si/SiC equivalents. The aim of this simulation is to analyse the cooling effect of the Si/SiC devices under transient overload condition.

6.3.2.1 Simulation results

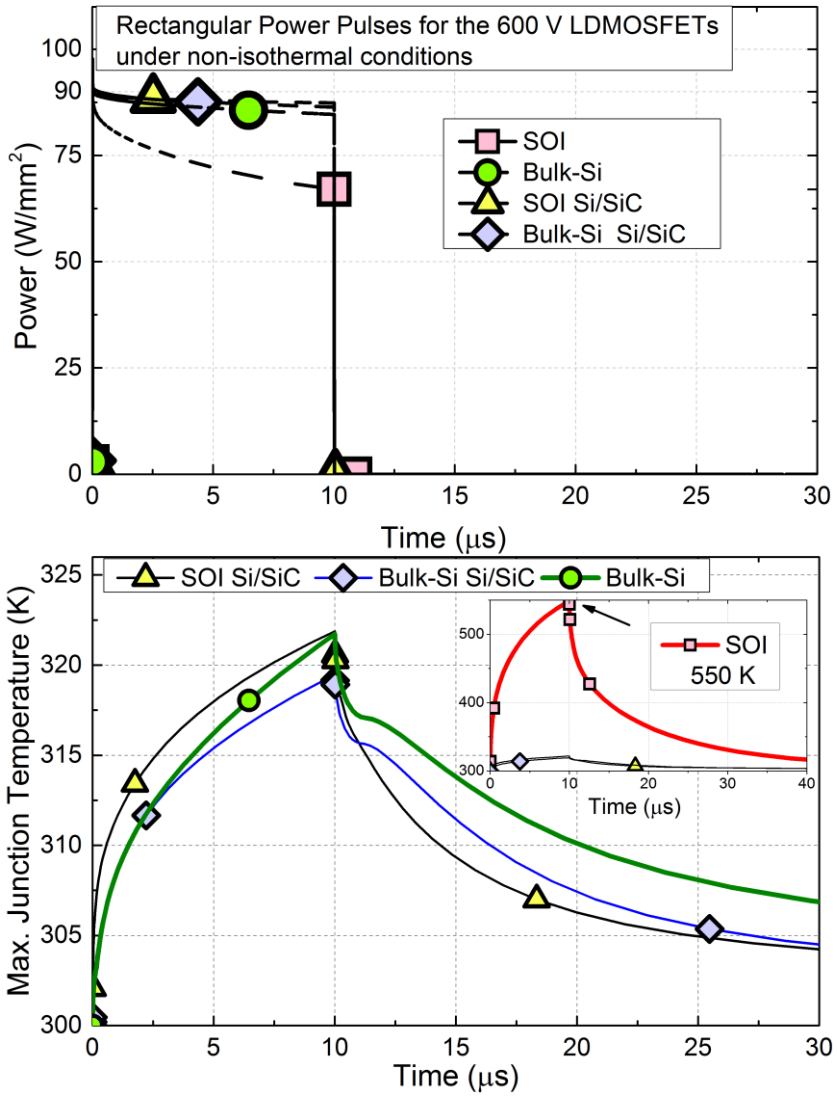

Figure 6.18. The power pulses (top) and temperature responses (bottom) for the simulated 600 V structures

Due to strong self-heating, the power applied in the SOI drops from the initial value to about 67 W/mm^2 at 10 μs, and the maximum temperature rises up to 550 K (see Fig. 6.18).

On the contrary, other devices have far less temperature increases and their power pulses are nearly the same. The disparity of junction temperature between the bulk-Si and its equivalent Si/SiC starts to appear at 2.5 μs, indicating the cooling effect of the SiC substrate. The thin-film Si/SiC also receives such thermal benefit, but a slightly rapider temperature rise is found when compared with the bulk-Si devices, mainly due to nonuniform heating [147] caused by the linear doping in the drift region. Nevertheless, the maximum junction temperature of this device is the same as that of the bulk-Si (green) at 10 μs, and thereafter decays faster than that of the thick-film Si/SiC counterpart. One can expect that more thermal improvement can be offered by the Si/SiC solutions under conditions where longer and larger power pulses are present.

Chapter 7 TCAD study on the 190 V Si/SiC LDMOSFETs

7.1. Introduction

In this chapter, a TCAD study is made on the energy capability of 190 V LDMOSFETs in Si/SiC, SOI, PSOI and PSOSiC technology, using the capacitive and inductive switching circuit (Chapter 5, section 5.4.2.3). The purpose of this study is to find out how effective is the Si/SiC substrate in handling the energy surge during switching, compared with other solutions. The first section of this chapter demonstrates the on/off I-V curves of the four transistors under isothermal condition at 300 K. Secondly, comparison is made between the four transistors on their switching performances during the capacitive turn-on and inductive turn-off event. This chapter has been published in [145].

7.2. DC characteristics

7.2.1. Off and on-state behaviour

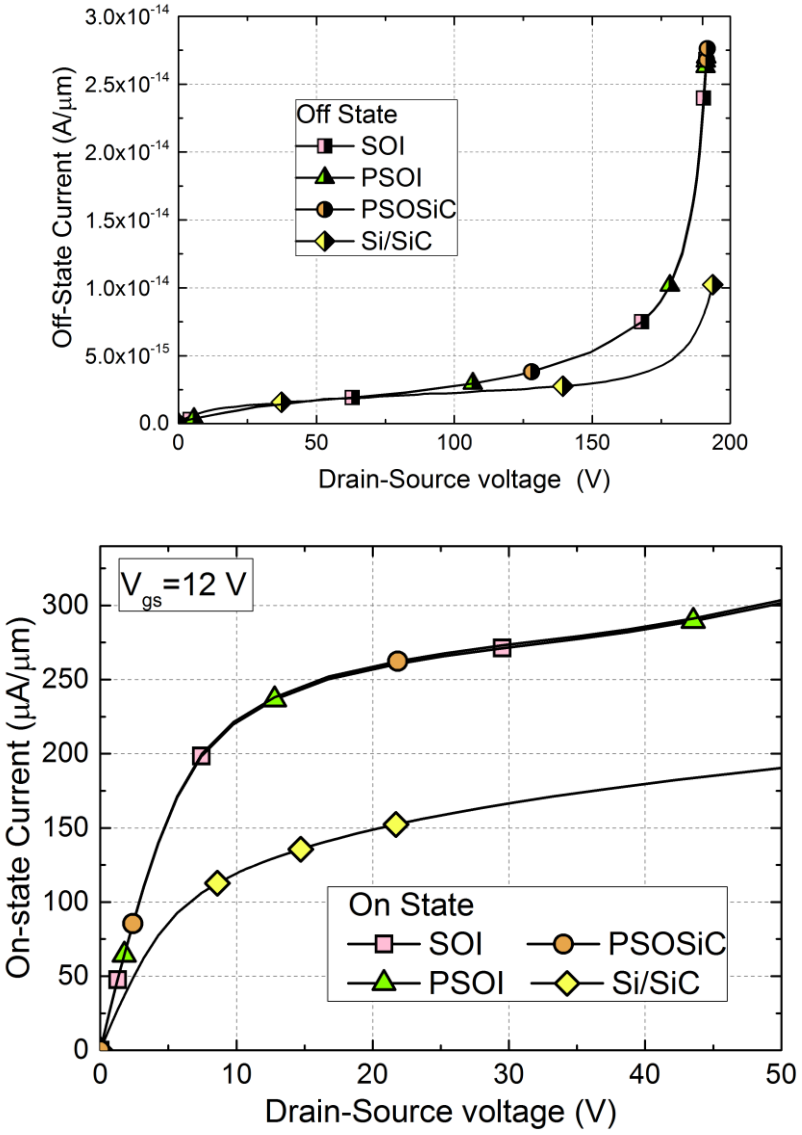

Figure 7.1. On (top) and off-state I-V curves (bottom) for the simulated 190 V devices under isothermal conditions at 300 K

Fig. 7.1 shows the electrical behaviour of the four 190 V transistors in the on- and off-state at 300 K. Self-heating models are deactivated in these simulations and the gate contacts are biased at 12 V for the on-state. The application of SOI RESURF enables

them to support a breakdown voltage of 190 V [129], but a higher on-resistance is found in the Si/SiC compared with the SOI group, owing to the absence of the BOX (single RESURF). Negligible difference in the I-V curves is observed among the SOI group members, indicating that the heat conduction path does not affect a device's electrical functioning under isothermal conditions. Based upon these I-V relations, the device widths of the Si/SiC and other SOI transistors are 1.75 mm and 1 mm, respectively, in order to achieve the same resistance.

7.3. Dynamic characteristics

7.3.1. Capacitive load switching

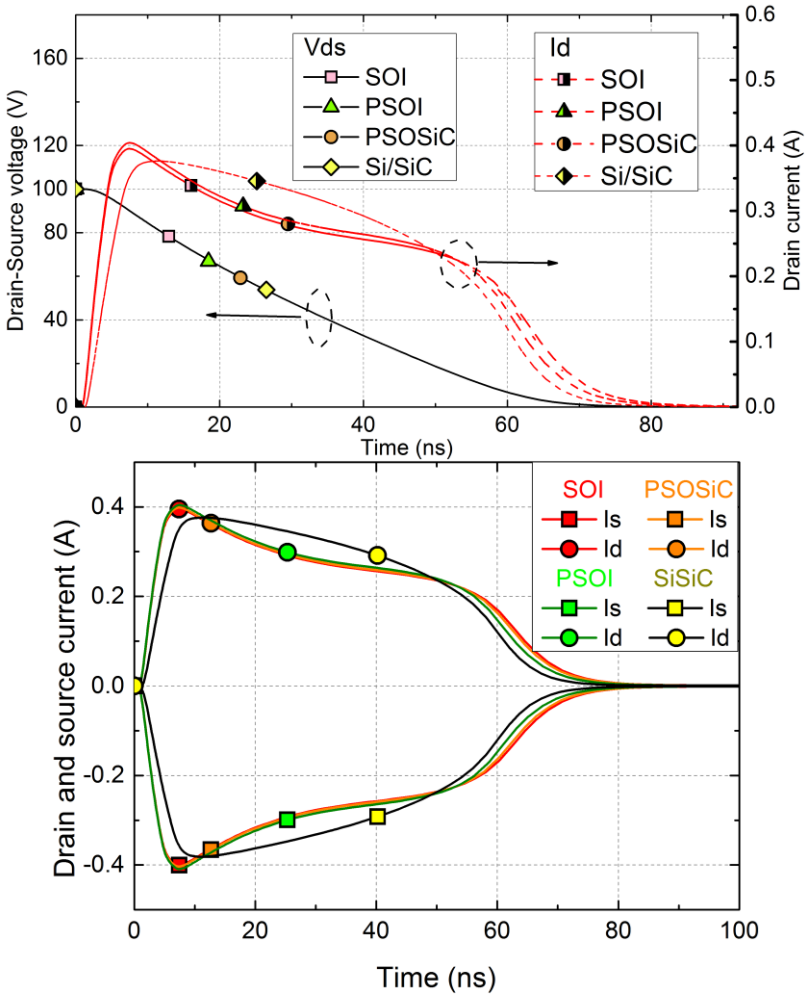

Figure 7.2. The I-V switching behaviour during the turn-on for the four LDMOSFETs (top) and their drain and source currents (bottom)

Fig. 7.2 demonstrates the transient I-V characteristics for the simulated 190 V transistor in the capacitive switching circuit described in Chapter 5. When the device is switched on, a large current (red) is visible initially as a result of capacitor discharge, and lasts for about 70 ns before the circuit reaches the steady state, with its current being limited to a very low value due to the 100 kΩ series resistor. This can be seen in all the transistors and a small disparity between the Si/SiC and other counterparts is perceptible, likely due to the differences in their device width and electrical capacitance. Unlike the inductive switching for the 600 V devices, the drain and source current are symmetric about the x axis (see Fig. 7.2 bottom), meaning that the instantaneous power values obtained from the two currents are the same. Fig. 7.3 presents the power and temperature curves during the transient state, for the simulated LDMOSFETs. It can be seen that the power pulses are similar in shape and the dissipated energy (0.87 µJ), as the I-V behaviours of the four devices are comparable. However, the thermal advantage is only found in the Si/SiC while the other solutions are identical regarding temperature rise. This indicates that the heat conduction paths in the PSOI and PSOSiC are much less sensitive to the transient heating than the Si/SiC case.

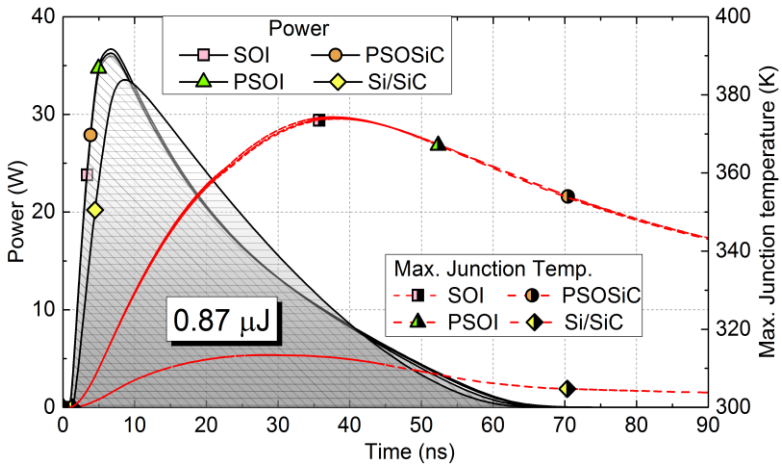

Figure 7.3. The instantaneous power and temperature responses during the capacitive discharge for the simulated LDMOSFETs

7.3.2. Zener-diode-clamped inductive switching

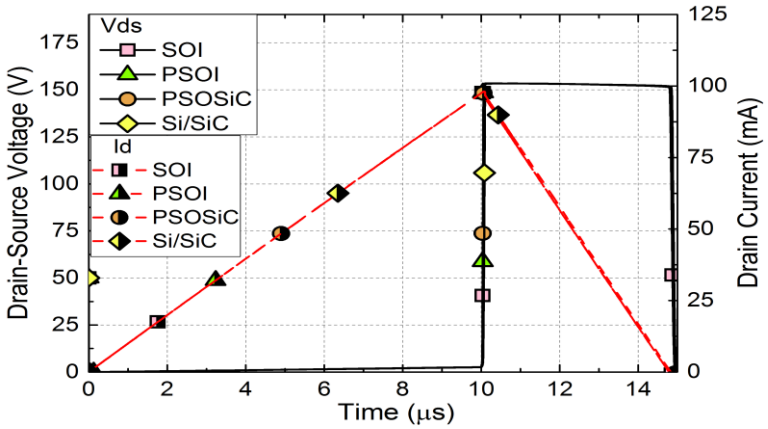

Figure 7.4. The V_{ds} and I_d curves under the conditions of V_{pulse} = 12 V, V_{dd} = 50 V, L = 5 mH, BV_{Zener} = 150 V, R1 = 3 kΩ and a ramp-up time of 10 µs, for the four simulated structures

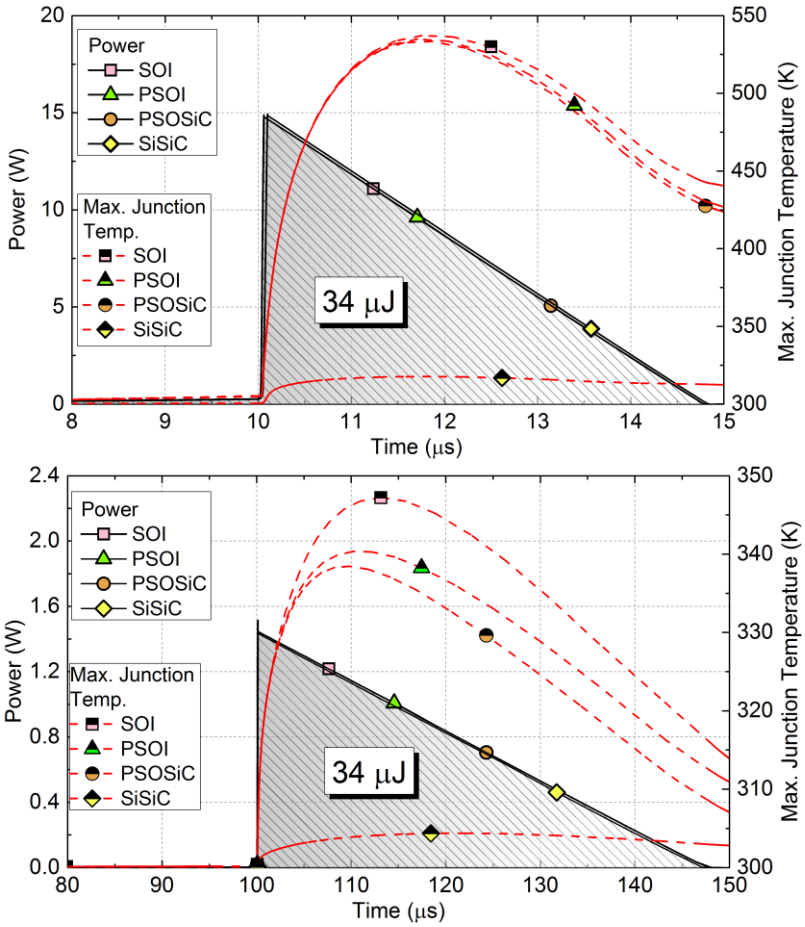

Figure 7.5. The power and temperature curves of inductive switching, under (top) the conditions mentioned in Fig. 7.13, and (bottom) with the inductor value and ramp-up time changed to 500 mH and 100 µs

The inductive switching setup for this section can be found in Fig. 5.21. As can be seen in Fig. 7.4, there is no difference among the electrical behaviour of the devices. When the DUT is switched on, all the supply voltage is dropped across the inductor and the drain current rises linearly. At 10 µs, the device is switched off and the drain potential increased to the rated clamped value of 150 V. Following this is a 4.8-µs-long transition period when the drain voltage is fixed at 150 V and the current falls linearly to zero. This transient behaviour results in a power pulse 4.8-µs-long with 34 µJ energy for each transistor, as can be seen in Fig. 7.5 (top). Similar to the capacitive switching, the Si/SiC has the best thermal performance and the SOI group experiences a rapid temperature increase, but slight deviations among their curves are noticeable and indicative of the effects of the PSOI layout and SiC substrate. This thermal improvement becomes more obvious when the 34 µJ power pulses are reshaped to about 48 µs, by increasing the inductor value and charge time to 500 mH and 100 µs (see Fig. 7.5 bottom). The difference at the peak of the maximum junction temperature between the SOI and PSOSiC is about 9 K in this case, greater than 4 K in the previous with the shorter power pulse.

7.3.3. Conclusion

It has been found that in spite of having a chip area 75% larger than the SOI structure, the Si/SiC solution undergoes negligible heating in any of the switching conditions simulated, exhibiting a very high energy capability. By contrast, the 22% area increase in the PSOSiC does not considerably change the way the energy is handled. This is in part because the thin Si layer offers a weak lateral thermal path which is part of the thermal shunt network. Therefore, the initial thermal process is mainly heat storage rather than heat transfer, and the thin film again exacerbates the situation by its small heat capacity that induces rapid temperature rise. After a couple of microseconds, this thermal charging of the Si layer is almost complete and the following energy tends to be directed to other regions. The contribution of the added thermal path and the SiC substrate becomes apparent at longer pulse lengths, as can be seen in Fig. 7.5. This is similar to the results by L. Yan et al. [155], showing that the thermal impedance of their PSOI devices is the same as that of the SOI at high frequency (10^5~10^6 Hz), but with 30% reduction at low frequency (~10^2 Hz). In the Si/SiC LDMOS, the absence of a BOX minimises the thermal storage within the Si, while the presence of the thin Si film reduces the involvement of Si in thermal conduction. The influence of the SiC substrate is therefore maximised,

significantly enhancing heat transfer, while less energy is absorbed in the Si layer. As a result, a fast cooling is achieved even with very short power pulses, which is beneficial to high frequency and power operations.

Chapter 8 Conclusions and further work

In this final chapter, the conclusions of the Si/SiC research conducted in this thesis are provided. After this, areas of future work on the Si/SiC architecture are outlined, namely experimental results, Physical-based TCAD models, RESURF design, switching circuits and LIGBTs.

8.1. Conclusions

The objective of the research presented in this thesis was to explore the potential of Si/SiC LDMOSFETs to be used for high-temperature power applications. This goal was fulfilled in three stages. First, the TCAD models were validated against the references over the temperature range of 27-300 ^{0}C, to ensure the credibility of the simulation results. Secondly, the Si/SiC LDMOS designs were optimised by using SOI and PN RESURF technologies, to deliver electrical behaviour similar to their bulk Si and SOI equivalents. Thirdly, several comparative studies were made on the LDMOSFETs using the Si/SiC, bulk Si and SOI substrate based upon DC and transient simulation, to highlight the effects of the Si/SiC architecture on the electrical and thermal performance of the devices. From this study, it is expected that the availability of the Si/SiC LDMOSFETs will enable power ICs to work at very high frequency (> 1 MHz) and high temperature up to 300 ^{0}C with increased reliability. However, it is also expected that for a given value of breakdown voltage (BV_{DSS}), the SOI-like Si/SiC design will have a higher low-side specific R_{on} than its SOI counterpart. The bulk-Si-like Si/SiC can improve this R_{on} vs BV_{DSS} relationship but suffer more degradation in R_{on} at high temperature. In order to achieve a competitive figure of merit for Si/SiC LDMOSFETs, implementation of 3D RESURF layouts in the Si/SiC substrate is one solution.

In high-voltage power applications, the key parameters of the semiconductor switch are the on-resistance and breakdown voltage. They are a pair of trade-off factors and widely used to assess different power LDMOSFETs. To achieve a better compromise

between them, RESURF techniques are used in the LDMOS design. The fundamentals of these technologies were stated in Chapter 3, covering two basic RESURF layouts: the SOI and PN structure. Also included in this Chapter were the introduction of LDMOSFETs and their substrates. Using this knowledge, a 600 and a 190 V SOI LDMOSFET were constructed in the simulator to validate the TCAD models against the references [46] over the temperature range of 27-300 ^{0}C. This was demonstrated in Chapter 4 and it was concluded that, in the main, the models correctly represented the physical behaviour of the Philips designs. In Appendix C, the transferability of these models to the Si/SiC architecture was discussed with the literature [14] [130] [131] and existing Si/SiC wafer bonding results [156]. It was concluded that it was possible to fabricate the Si/SiC substrate with a device-quality Si layer, high voltage capability and minimal interface effect, and that the fabricated Si/SiC MOSFET could behave like its SOI and bulk-Si counterparts. This meant that the Si/SiC and bulk Si and SOI could share the same model setups, with the interface charge values specified for each case according to the literature [124] [131]. To consider the heating effects, the thermal models are established and detailed in Appendix A.

With the models being analysed and established, a preliminary Si/SiC study was first given in Chapter 5 on lateral PiN diodes as a simple device to compare outputs. These diodes were simple, free from strong RESURF effects, and only differing in the substrate materials. The modelling of these diodes consisted of two parts. The first simplified a PiN diode down to a 100×100×1 μm^3 heat source on a 500×500×100 μm^3 domain representing the substrates of interest, namely SOI, Si/SiO$_2$/SiC, bulk Si, SiC and Si/SiC. Thermal simulation was performed on them and showed that the Si/SiC architecture, with its thin Si film intimately formed on SiC, displayed significant thermal advantages over any other Si solution, and was comparable to bulk SiC. The second simulation considered the detailed layout of a lateral PiN diode in SOI and Si/SiC architectures. This modelling revealed that compared with the SOI PiN diode, the Si/SiC had a higher breakdown voltage and were more robust against self-heating effect. However, the blocking capability of the Si/SiC was limited by an unbalanced depletion with an electric field peak at the p-/N+ junction. By using a thin Si layer on the SiC substrate, this effect was diminished but at the expense of a higher on-resistance.

To address this problem, the PN and SOI RESURF layouts were transferred from the bulk Si and SOI LDMOSFETs mentioned in Chapter 3, to thick and thin-film Si/SiC architectures respectively. These Si/SiC, SOI and bulk-Si LDMOS designs were categorised into three groups with detailed descriptions on their parameters. In each group, the Si/SiC transistor was constructed to be very similar to its SOI or bulk Si counterparts for the comparative studies later on. Firstly a thin-film 600 V Si/SiC transistor in the SOI RESURF technology was introduced, along with two SOI counterparts for benchmarking. Second was the description of two thick-film 600 V LDMOSFETs designed with the PN RESURF principle, employing a Si/SiC and bulk-Si structure. Third, the four thin-film 190 V LDMOSFETs in the same SOI RESURF technology were presented, using a Si/SiC, SOI, PSOI and PSOSIC substrate. The potential contours at the onset of avalanche breakdown for the 600 V class devices were illustrated and showed that the SOI and PN RESURF structures created a uniform electric field distribution in the drift region. This formed the second part of Chapter 5.

In the last section of Chapter 5, the simulation setups for the aforementioned LDMOSFETs were detailed and split into two parts. First, the application of the physical models discussed in Chapter 4 was described. Second was the introduction of four different switching circuits used for the transient simulation. The first two circuits were designed for the 600 V class transistors, namely the diode-clamped inductive switching circuit for the Philips SOI and its Si/SiC counterparts and the rectangular power pulse circuit for the Philips SOI, bulk Si and their Si/SiC equivalents. The last two were the capacitive and the inductive switching circuit with a Zener diode, for the four 190 V power transistors.

In Chapter 6, a TCAD study was conducted on the static and dynamic behaviour of the two 600 V Si/SiC LDMOSFETs. The analysis of the DC behaviour was split into three parts. The first part compared the Si/SiC transistor in the SOI RESURF technology with its two SOI counterparts, namely the Philips SOI and the SOI without the gate extension. It was shown that the 600 V Philips LDMOSFET and its Si/SiC equivalent had near identical off-state behaviour at 27 and 300 ^{0}C, with a significant tunnelling leakage component emerging above 450 V at room temperature. This was also observed in the SOI LDMOSFET without the field plate extension. It was concluded that depletion from the BOX and FOX had equivalent effects on the leakage current at 300 and 573 K. In the

on-state, the Si/SiC device had higher electrical resistance but much lower thermal resistance, leading to less self-heating and higher reliability. The comparison between the Si/SiC and the SOI without the gate field plate showed that the accumulation effect on the drift region was stronger at high V_{DS} and led to a lower on-resistance and higher saturation current.

In the second part of the DC behaviour in Chapter 6, the bulk Si LDMOSFET in the PN RESURF technology was compared with its Si/SiC equivalent. It was concluded that the Si/SiC and bulk Si were very similar in the I-V characteristics at room temperature, namely the on-resistance and Kirk effects. Nonetheless, the Si/SiC delivered a leakage current two orders of magnitude lower and a breakdown voltage 250 V higher at 300 ^{0}C, due to a much better electrical insulating property.

The last part of the DC behaviour in Chapter 6 provided a comparative study among the two Si/SiC transistors and their equivalents, in terms of the leakage current, low and high-side resistance over the temperature range of 27-300 ^{0}C. It was concluded that the two Si/SiC devices exhibited an off-state leakage current as low as the SOI device at a drain-source bias of 300 V, due to a small charge density of -2×10^{10} cm^{-2} [21] defined along the Si/SiC interface. In terms of the on-state, it was concluded that although the SOI delivered a low-side resistance smaller and less sensitive to temperature than those of the Si/SiC devices, the resistance of the SOI became larger when high substrate biases are applied, which represented a typical high-side operation. These relations held true over the temperature range of 27 to 300 ^{0}C, and their differences in the resistance were as follows. In the on-state, the Si/SiC using SOI RESURF had a low-side resistance 56% and 79% higher than the SOI at 300 K and 573 K respectively, owing to a lack of SAD effect. The Si/SiC using PN triple RESURF had a low-side -resistance 5% and 71% higher than the SOI at 300 K and 573 K respectively, which was caused by lower doping density in the drift region. Under high-side conditions, the resistance of the SOI increased with the substrate potential, and eventually reached a value 86% and 91% greater than those of the SOI Si/SiC and Bulk-Si Si/SiC respectively at -200 V and 300 K. At 573 K, these differences were reduced to 40% and 36% correspondingly.

After the analysis of the DC characteristics, a study on their transient behaviour was presented and separated into two sections. First, a diode-clamped inductive switching circuit was simulated for the 600 V Philips SOI LDMOSFET and its Si/SiC equivalent

under low and high current condition (Case 1 & 2). It was shown that even though the SOI had a smaller chip area and suffered from strong substrate effects during the transient state, the two devices had similar currents and power dissipations at the gate, drain and source. The turn-on losses was found to be higher than that of the turn-off due to the presence of the parasitic capacitors. However, this similarities did not lead to similar thermal responses in both devices and the SOI was heated up at a much faster rate. By contrast, the SiC substrate in the Si/SiC functioned like an embedded heat sink regulating device temperature close to that of the ambient environment (423 K). In Case 2, the peak temperature in the Si/SiC is 425 K, lower than 463 K in the SOI, thereby increasing reliability.

In the second section, a comparison is made among the Philips SOI, bulk Si and the two Si/SiC LDMOSFETs, of the heating effects in the RPP circuit introduced in Chapter 5. Simulation of this circuit was performed for the Philips SOI and bulk-Si LDMOSFET and their Si/SiC counterparts. Through comparison, it was evident that the Si/SiC structures had thermal performance comparable to the bulk-Si and much better than the SOI, with a 10 μs pulse of 90 W/mm2. It was concluded that more thermal improvement could be offered by the Si/SiC solutions under conditions where longer and larger power pulses were present.

The final results Chapter presented a TCAD study on the energy capability of 190 V LDMOSFETs in Si/SiC, SOI, PSOI and PSOSiC technology, using the capacitive and inductive switching circuit. The comparison among their static I-V curves under isothermal conditions found that the application of SOI RESURF enabled the four devices to support a breakdown voltage of 190 V, and that the SOI group had the same on-state behaviour at 300 K, which was lower than that of the Si/SiC. The results of the capacitive and inductive switching circuits showed that in spite of having a chip area 75% larger than the SOI structure, the Si/SiC solution underwent negligible heating in any of the switching conditions simulated, exhibiting a very high energy capability. However, the 22% area increase in the PSOSiC did not considerably change the way how energy was handled. This indicated that the Si/SiC was much more effective than PSOI and PSOSIC in dealing with the transient heating.

8.2. Future work

The work presented in this thesis was an exploratory study on RESURF Si/SiC LDMOSFETs for high temperature operations and will lay a foundation for the succeeding Si/SiC research. The following are some areas that the future work can cover to provide a more in-depth understanding of the Si/SiC architecture.

8.2.1. Experimental results

In this project, the experimental results are limited to the TEM observations on the Si/SiC interface (see Fig. C.4 in Appendix C). Although the amorphous layer at the interface is very thin (up to 8 nm), its effects on carrier mobility and lifetime are still not clear. To further examine the quality of the Si film on the SiC substrate, experiments such as Hall effects measurements, X-ray diffraction (XRD) [85] and MOSFET fabrication should be performed. These are very important not only to the validation of the FEM models but also the advancement of the Si/SiC study from a conceptual level to a practical solution available for mass production. The works associated with this are currently conducted in the SaSha project, funded by the EU's Horizon 2020 programme.

8.2.2. Physical-based TCAD models

In this thesis, all the LDMOS designs were simulated with the same physical-based TCAD models, with differences in the values of the interface charge and carrier lifetime. These settings were used based upon the literature that demonstrated that the fabricated Si/SiC devices had electrical behaviour very similar to the bulk Si and SOI counterparts, and that no adverse effects of the Si/SiC interface had been found on the LDMOS characteristics, for example the reduction of the blocking capability. From a standpoint of analysing the potential of the Si/SiC architecture, this model configuration is reasonable and sufficient enough to deliver credible results for the comparative study. However, it is likely that the wafer bonding and annealing process will degrade the quality of the Si layer and result in a large number of interface charges in the Si/SiC structure. To consider these effects and increase the accuracy, the models are required to be adjusted against the experimental outcomes before being used for device development.

8.2.3. RESURF design

In this thesis, the Si/SiC LDMOSFETs were optimised based upon two classic templates—the first using SOI RESURF as in Arnold et al. [46], and the second using PN RESURF as in Disney et al. [99]. These two LDMOS topologies are widely-reported and well-understood, which is helpful to the study and verification of the physical TCAD models. Using these two structures also allows a like-for-like comparison to be made, whereby the effects of the Si/SiC architecture are highlighted. Furthermore, the fabrication techniques of the two LDMOSFETs are mature and can be readily implemented in the Si/SiC for the prototype development. Nevertheless, the Philips and Disney designs were developed and tailored for SOI and bulk wafers respectively, with the consideration of the substrate effects. This means that the electrical characteristics of the Si/SiC devices can be inferior to their SOI and bulk Si references. For instance, the 600 V Si/SiC LDMOSFETs in the SOI technology exhibits a low-side resistance higher than that of the Philips SOI (Chapter 6). As such, it is necessary to apply a RESURF structure more suitable to the Si/SiC architecture for better performance. A 3D RESURF technique can be one option as in this concept, the ideal model features depletion only between alternate n and p-type stripes arranged in the direction of device width [148] [157]. The substrate should not be involved in the development of the space charge regions in the PN pillars. In the traditional SOI and bulk Si structures, substrate assisted depletion is unavoidable and has to be suppressed by some special layouts [101] [157] to achieve charge balancing. This can increase the complexity and cost of the LDMOSFETs. By contrast, the Si/SiC transistor in the 3D RESURF technology does not require those layouts as the (SI) SiC substrate is neutral. A simple example of such Si/SiC design is demonstrated in Appendix B. However, it is worth noting that the Si/SiC interface charge can deplete the n drift region and upset the optimal 3-D field distribution. By using narrower PN stripes, this effect can be reduced due to a higher doping allowance which limits the depletion from the interface. In addition, the presence of a thin oxide layer at the Si/SiC interface can adversely affect the blocking capability. To execute this idea, an experimental work on the Si/SiC interface prior to the simulation is suggested.

8.2.4. Switching circuits

In this thesis, the transient simulation was carried out with four different circuits to examine the heating and energy capability of the LDMOSFETs. A common feature of the simulated circuit is that the source of the device is grounded, a typical low-side condition. To deliver high power level, power conversion systems usually employ a half bridge topology where the source of the high-side device is floating [2]. Therefore, to gain a complete picture of the device performance, the high-side switching circuit needs to be simulated. In this case, the transistor can operate in the saturation region where an extreme stress condition is presented [151]. The fast cooling offered by the Si/SiC substrate can protect the device from overheating, thereby increasing the performance and reliability. Additionally, it was found in this work that the Si/SiC LDMOSFETs suffered no degradation in the on-resistance under the high-side configuration, which led to a smaller chip area in a power system.

In a fully-integrated half bridge circuit, the body diode of the LDMOSFET is very important as it prevents the power switch from being energised from the inductive load. This diode will produce losses during the reverse recovery, where significant heating can occur. This effect can be worsened in a hot environment because the reverse recovery time has a positive temperature coefficient [46]. It is expected that the Si/SiC architecture can ensure the safe operation of the diode with the remarkable heat transfer ability. To better understand the diode reverse recovery in Si/SiC devices, TCAD simulation on this should be included in the future work.

It was concluded in Chapter 6 that the Si/SiC architecture could make the LDMOSFETs work more reliably at high frequencies (>1 MHz) due to better heat transfer ability. This was based upon the simulation results of the 600 V Si/SiC and SOI transistor at 200 kHz, in the clamped inductive switching circuit. For a more conclusive study on this topic, it is necessary to simulate the Si/SiC devices at 1 MHz and beyond, under non-isothermal condition

8.2.5. LIGBTs

To achieve a higher current in a flyback and half bridge circuit, the low or high-side LDMOSFETs can be replaced with LIGBTs [111] [158]. The LIGBTs in the traditional bulk-Si and SOI technology face problems like slow turn-off [83] and premature punch-through breakdown [158]. The current solutions to this are the membrane bulk-Si and SOI substrate where the substrate effects are eliminated, thereby increasing the speed and blocking capability [83] [158]. In theory, the Si/SiC architecture is well-suited for such bipolar devices as the substrate assisted depletion (SAD) effect is absent in this structure. The lack of this depletion will reduce the doping allowance in the Si/SiC LDMOSFETs, which increases the on-resistance. However, it is expected that less degradation is seen in the Si/SiC LIGBT in the on-state, due to the fact that the resistivity of such device type is determined by minority carrier injection. Furthermore, the (SI) SiC substrate can minimise the heating effect and provide mechanical support during device operation, which is beneficial to harsh environment applications. It is suggested that the research on the Si/SiC LIGBTs should be carried out once the Si/SiC LDMOSFETs are successfully fabricated and tested.

Appendix

A Thermal models

A.1 Methodology

In order to study the heating effect, self-heating model (LAT. TEMP) [122] is activated in the simulation. The lattice heat flow equation is given below [122]:

$$C\frac{\partial T_L}{\partial t} = \nabla(\kappa \nabla T_L) + H \tag{A.1}$$

Where C is the heat capacitance per unit volume, κ the thermal conductivity, T_L the local lattice temperature and H the heat generation. C is as the product of specific heat at constant pressure (C_P) and density of the material (ρ). This equation relates the thermal storage ($C\frac{\partial T_L}{\partial t}$) to the thermal transfer ($\nabla(\kappa \nabla T_L)$) and thermal generation (H). A simplified expression for the thermal generation has the form [159]:

$$H = \vec{J}\vec{E} + UE_g \tag{A.2}$$

Where $\vec{J}$ is the current density, $\vec{E}$ the electric field, U the recombination rate and E_g the bandgap of the semiconductor. The first and second term represent Joule and recombination heating respectively. In unipolar devices, the heating mechanism is Joule heating due to the absence of conductivity modulation.

In the steady-state simulation, $\frac{\partial T_L}{\partial t}$ on the left hand side of Equation A.1 is reduced to zero so the lattice temperature is only associated with heat transfer and generation. In the transient simulation, the thermal storage will be significant if the heat capacitance (C) of a material is very large.

To solve the lattice heat flow equation, thermal boundary conditions need to be set in the simulation. In a transistor, all the metal contacts can exchange heat with the ambient

environment (e.g. package). The substrate contact, however, has the largest area and is connected with the external cooling equipment. This means that the heat escapes mainly via the substrate and hence defining the substrate electrode as the only thermal contact does not dramatically reduce the reliability of the simulation results. For the sake of simplicity, the temperature of the thermal contact is fixed at 300 K or even higher and no external heat sink is specified.

Due to the self-heating effect, the simulated SOI transistors can experience a considerable increase or decrease in temperature. In this case, the temperature effect on the heat capacitance and thermal conductivity are considered to increase the accuracy of the models. This setup was applied by Lim et al. in [5], where the HV LDMOSFETs in PSOI and Philips technology were studied by SILVACO and the authors' analytic model. A very good agreement was found between the results obtained from the two methods and the thermal advantage of the PSOI device was clearly shown. The following are the settings of the thermal properties for the materials that appear in the LDMOS structure.

A.2 Thermal conductivity and heat capacitance

Depending on materials, the lattice temperature can affect the thermal conductivity (κ) and heat capacitance (c_s) in different ways. It is reported that SiO_2 is insensitive to temperature and hence κ and c_s are fixed at 0.014 *W/cmK* and 3.066 *J/cm^{3}K*, respectively [5]. The thermal conductivities of Si and SiC, however, degrade with increasing temperature. In the case of Si, this relationship can be formulated by:

$$\kappa(T) = 1/(t_{CA} + t_{CB}T_L + t_{CC}T_L^2) \tag{A.3}$$

The values of t_{CA}, t_{CB} and t_{CC} for Si are obtained from [5] and shown in Table A.1. The unit of thermal conductivity is W/cmK.

According to [160], the thermal conductivity of 6H-SiC is as a reciprocal function of the lattice temperature:

$$\kappa(T) = 611/(T_L - 115) \tag{A.4}$$

In the simulation, this is done by using a power function and its parameters are listed in Table A.1:

$$\kappa(T) = t_{cconst}(T_L/300)^{t_{cpower}} \tag{A.5}$$

Fig. A-1 plots the lattice temperature effect on the thermal conductivity of 6H-SiC, by using Equation A.4 [160] and A.5. The two curves are very similar from 300 to 600 K. The thermal conductivity of 6H-SiC described here is for the direction parallel to the c axis ($\kappa_{||}$) [161]. To consider the anisotropic property of 6H-SiC, the κ normal to the c axis ($\kappa_{\perp}$) can be specified as $\kappa_{||}/0.7$ in SILVACO [162]. Due to being a wide bandgap semiconductor, the (SI) SiC has a κ value higher than that of its conductive form and the related parameters can be adjusted according to [163]. In our simulation, the κ of 6H-SiC is simplified as an isotropic parameter described by the power function (Equation A.5), as in [161].

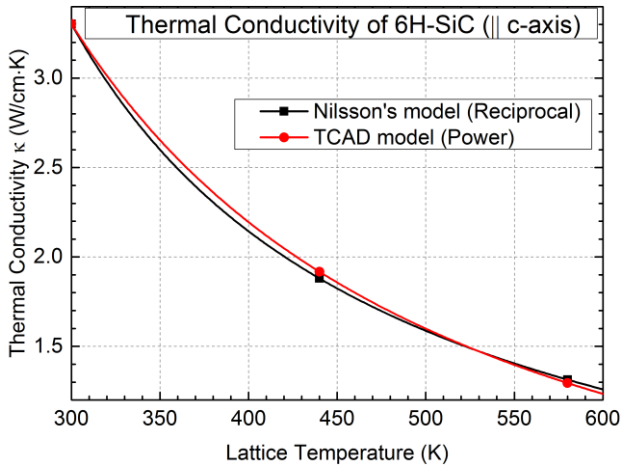

Figure A-1 Thermal conductivity of 6H-SiC as a reciprocal (black) and power function (red) of lattice temperature. The Nilsson's model is detailed in [160]

The heat capacitance of Si and 6H-SiC is related to lattice temperature by the equation below:

$$c_s(T) = hc.a + hc.b\,T_L + hc.c\,T_L^2 + hc.d/T_L^2 \qquad \text{(A.6)}$$

Where the values of $hc.a$, $hc.b$, $hc.c$ and $hc.d$ for the two materials are obtained from [5] [164] and listed in Table A.1. The unit of heat capacitance is J/cm^3K. 4H-SiC can be set up in a similar way for the thermal simulation, as the properties of the two polytypes (4H&6H) are alike [160].

Thermal conductivity κ				
	t_{CA}	t_{CB}	t_{CC}	
Si	0.03	1.56×10^{-3}	1.65×10^{-6}	
	t_{cconst}	t_{cpower}		
6H-SiC	3.3027	1.42		
Heat capacitance c_s				
	$hc.a$	$hc.b$	$hc.c$	$hc.d$
Si	1.97	3.6×10^{-4}	0	-3.7×10^{4}
6H-SiC	3.293	0.645×10^{-3}	0	-11.75×10^{4}

Table A.1 The thermal parameters for Si and 6H-SiC used in TCAD simulation

Appendix

B 3D RESURF for Si/SiC

Fig. B-1 demonstrates a Si/SiC LDMOSFET in 3D RESURF technology and its mesh layout. In the drift region, the n and p-type pillar are in orange and sky blue colour respectively. The green area represents a charge neutral region and its size depends on the mesh density. This setup can deplete the n-type region from both sides in the off-state, creating a double RESURF effect. Even though this layout is 3D, the development of the space charge region is a 2D action as the (SI) SiC substrate (grey) is not able to deplete the drift region.

Fig. B-2 shows the potential and electric field distribution at the onset of avalanche breakdown (200 V). It can be seen that the equal potential lines spread deeply into the SiC substrate and the voltage across the drift region is dropped linearly from the drain to source. The electric field peaks at the corners of the n/p pillars where the avalanche mechanism commences. However, it is worth noting that the Si/SiC interface charge can disrupt the charge balancing effect and induce premature breakdown.

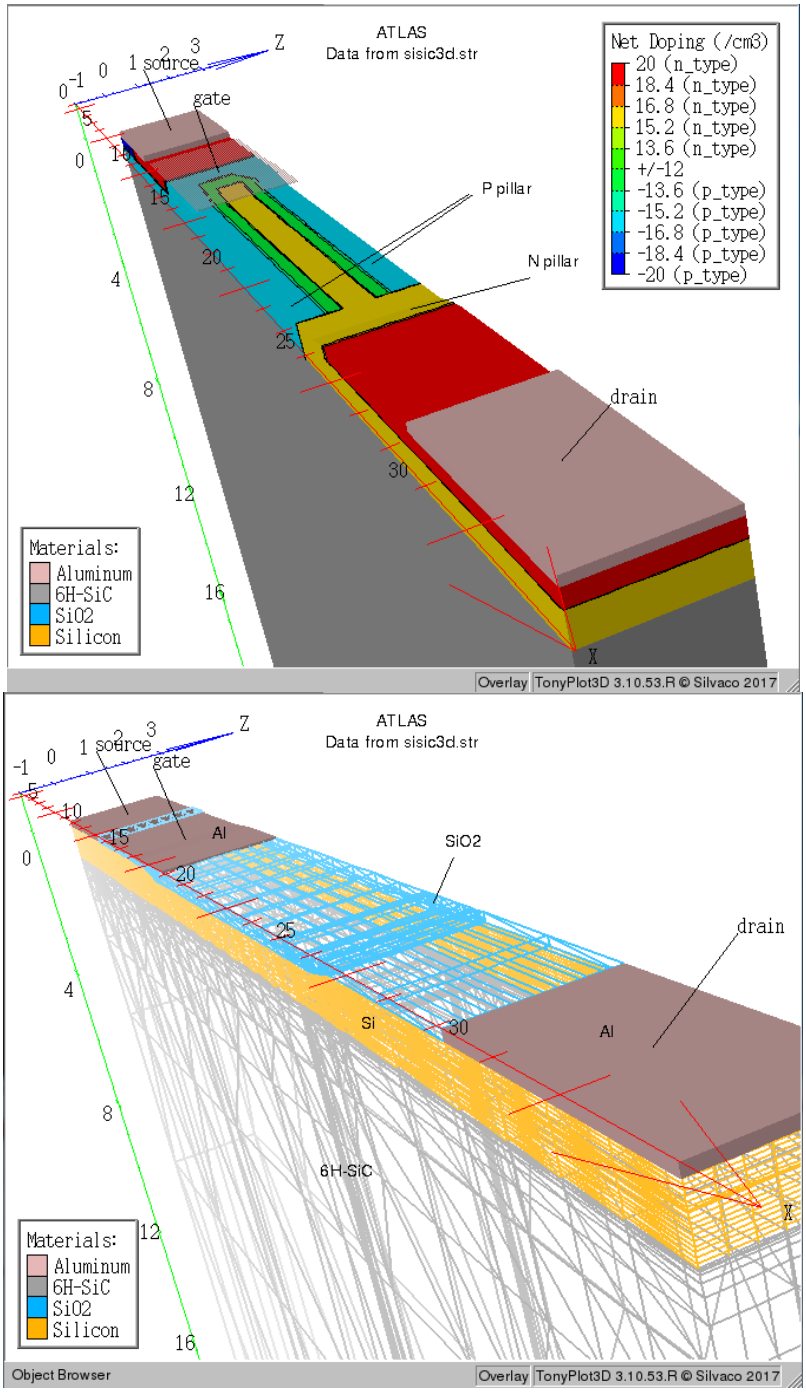

Figure B-1 A 3D view of the Si/SiC LDMOSFET in 3D RESURF technology

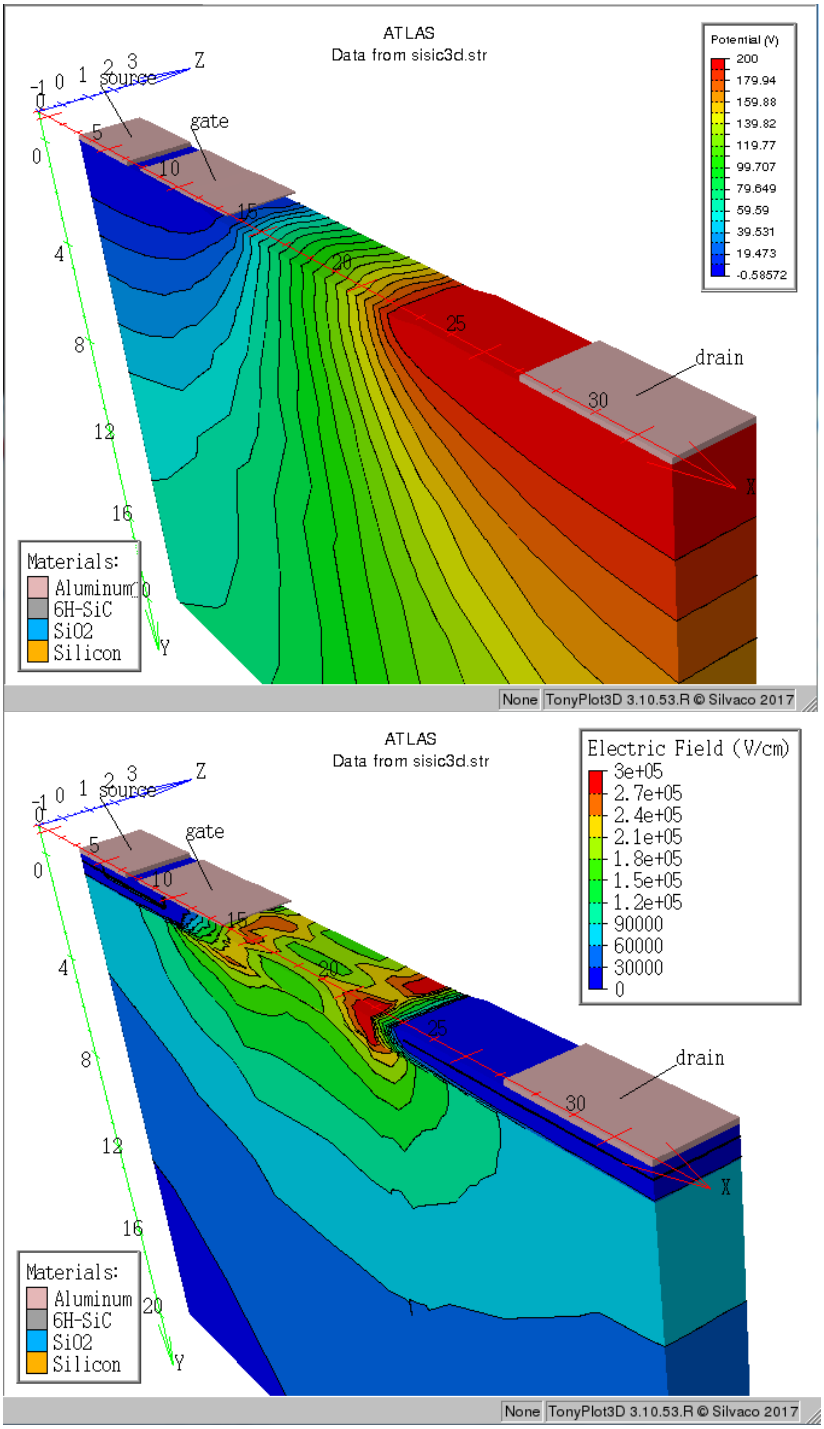

Figure B-2 3-D potential (top) and electric field distribution (bottom) of the Si/SiC LDMOSFET at the onset of avalanche breakdown (200 V)

Appendix

C Experimental Si/SiC issues affecting TCAD simulation

There are three points which can affect the TCAD models for the Si/SiC architecture, namely the quality of the top Si film, the properties of (SI) SiC and the Si/SiC interface states. This discussion will be supported by experimental wafer bonding results and related references. The purpose of this section is to ascertain the quality of the Si layer within the Si/SiC structure, to compare the insulating properties of the SiC wafer to the SOI wafer and to understand the effects of the SiC substrate on the Si device layer. This will inform the setup of the models in response to the traits of the Si/SiC substrate.

C.1 The quality of Si on SiC

It has been experimentally proven that forming a uniform Si layer on SiC via epitaxial techniques is difficult, due to the lattice mismatch between Si and SiC [38]. One molecular beam epitaxy experiment shows that the growth starts with many separated Si islands in different shapes and sizes, enlarging in three dimensions and merging into several bumpy continents (see Fig. C.1), if the epitaxy process is long enough [38]. This is ascribed to the weak affinity of Si with the SiC surface, and the atomic binding tends to occur between Si atoms mainly [38]. These Si-Si bonds only constitute a crystal lattice on a small scale and lack the homogeneity required for device fabrication.

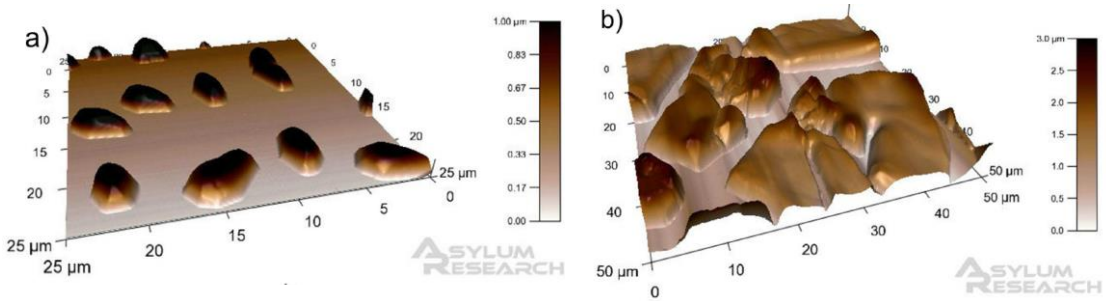

Figure C.1. Atomic force microscopy for the Si/SiC heterojunction layer by molecular beam epitaxy (MBE), designed to be 100 nm thick (left) and 1 µm thick (right) [38]

Wafer bonding, however, can transfer a monocrystalline Si layer onto a SiC substrate and the atomic interaction takes place exclusively between the two surfaces. Fig. C.2 demonstrates the pre and post-anneal directly-bonded Si/SiC samples, produced after a 3 inch on-axis semi-insulating (SI) 4H-SiC handle wafer and a 4 inch bulk-Si seed wafer having undergone the Smart Cut^{TM} process [13]. This process creates a hydrogen-rich region in the seed wafer by implantation, which defines the thickness of the transferred Si film (1 µm, here). This layer is then split away from the bulk Si during annealing as the hydrogen expands. The first anneal lasted 1.5 hours in an Argon environment at 450 ^{o}C in order to fracture the Si-Si bonds in the implanted region. This was followed by a 1000 ^{o}C rapid thermal annealing (RTA) in Argon to enhance the Si/SiC interfacial bonds. The Si is a dark grey whereas the (SI) SiC is colourless and transparent in nature. It can be seen in Fig. C.2 that the wafer cleavage is only partially successful, with voids present in most of the surface areas.

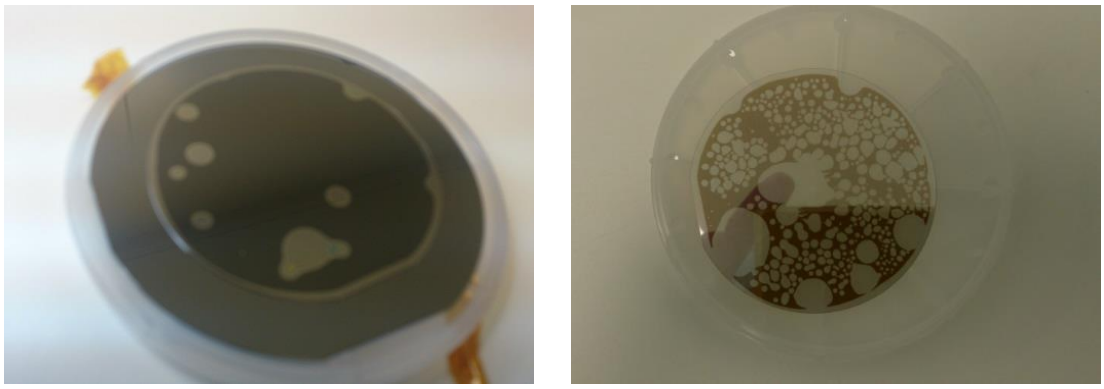

Figure C.2. The 3 inch Si/SiC bonded samples before and after annealing (left & right). The Si seed wafer is treated with Smart Cut^{TM} process.

Fig. C.3 are the images for the post-anneal Si/SiC wafers captured by scanning electron microscopy (SEM) in different perspectives. Viewed in high angle, the edge of the bonded

and unbonded region is visible and the Si area looks very rough. This is confirmed by the top view of the Si region and the surface morphology features flaking, which can be the trail of the H_2 expansion. Though the layer transfer is functional only in some areas, the cross-sectional shot clearly shows that the bonded Si is 1 µm thick uniformly. This indicates that the H^+-induced micro crack can exfoliate the layer, and that the adhering effect is achievable in the Si/SiC heterojunction. In [13], the yield of the Si/SiC bonded wafer by Smart Cut^{TM} is more than 80%, with the surface roughness of only 5.8 nm. Therefore, the poor Si coverage on SiC in our samples can be due to the presence of alien particles that disrupt the binding. From a device fabrication point of view, this approach is deemed to be inadequate due to the low-yield bonded areas.

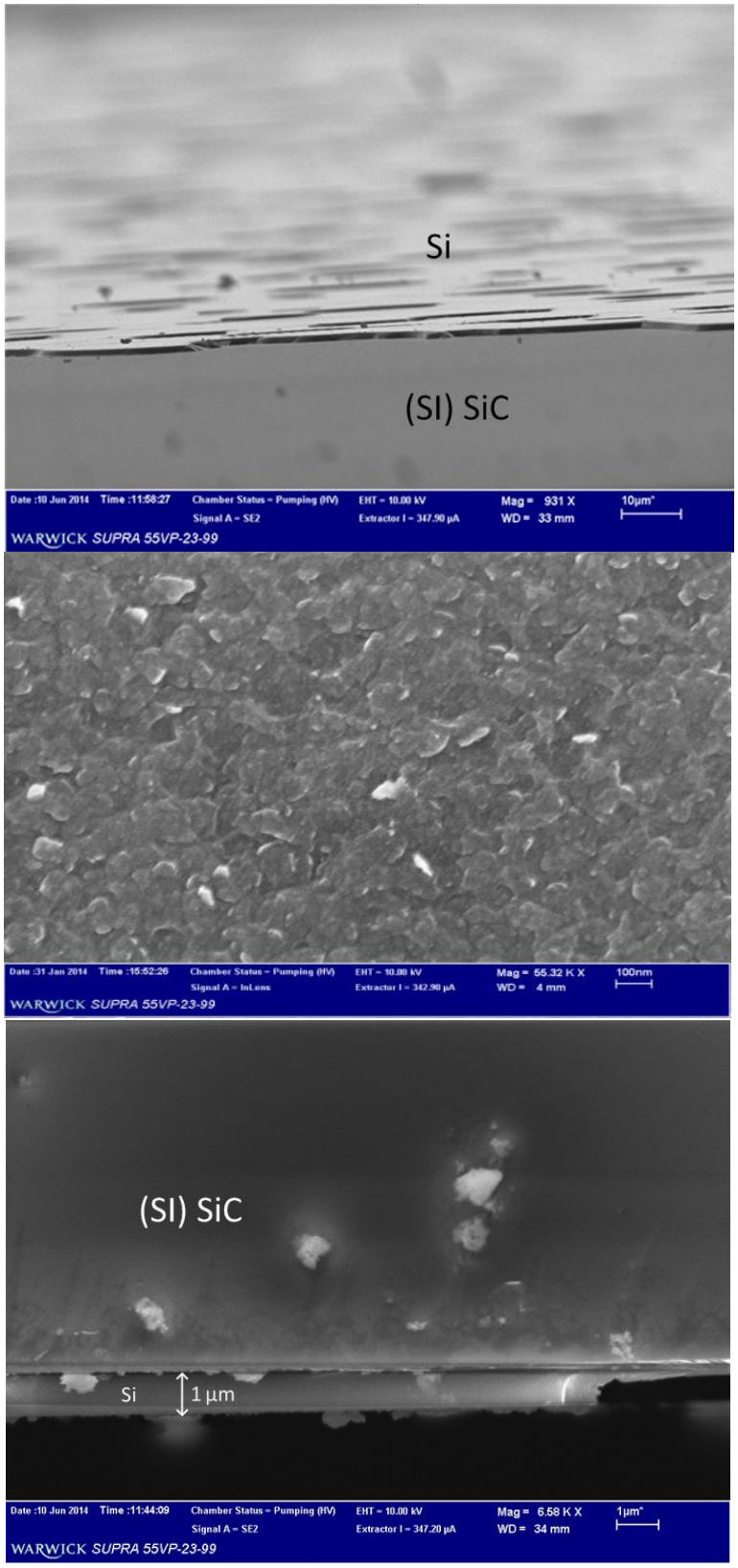

Figure C.3. SEM images of the Si/SiC samples in high angle (top), of top view (middle) and side view (bottom)

Apart from the Smart Cut^{TM} process, the thin Si film can be defined by transferring the device layer of a SOI substrate [130]. After bonding the top surfaces of a SOI wafer and a SiC substrate, the Si handle wafer and the BOX can be removed by grinding and etching so that only the device layer remains on the SiC wafer. Si/SiC wafers were developed for this project using this method by IceMOS Technology Ltd, Northern Ireland. These are shown in Fig. C.4, where the yield is satisfactory regardless of the Si layer thickness (1, 2 and 5 µm) [156]. The annealing temperature for these wafers is 1200 ºC. The trenches are introduced prior to the wafer mating, as a solution to outgassing [156]. TEM images reveal that the Si/SiC heterojunction can be a sharp interface with and without an amorphous layer, or takes the form of an island-like defect. The dislocation region seems to exist mostly at the Si side and extends up to 8 nm. These results are in agreement with those by other research groups [14] [165]. Results qualifying these Si layers were not available at the beginning of this project and for the simulation, data was taken from other references with similar processing.

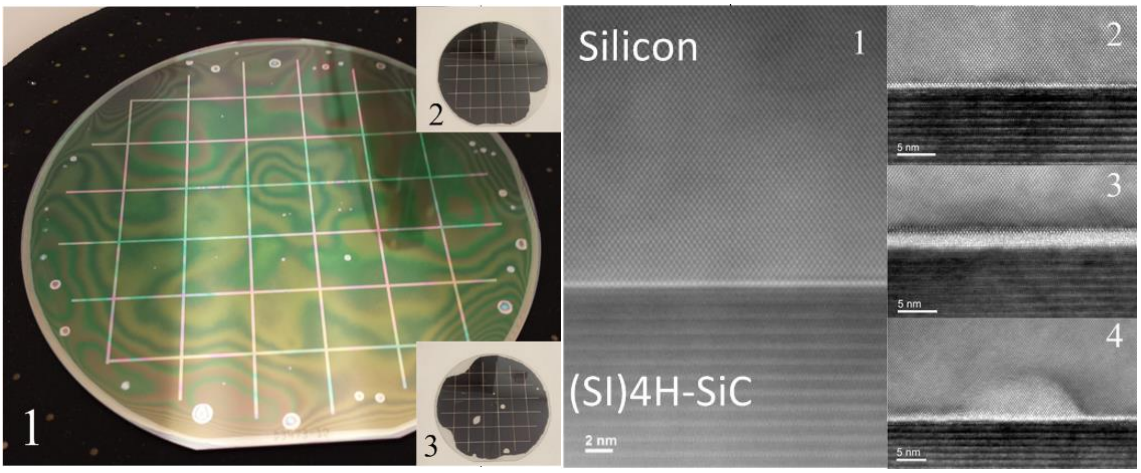

Figure C.4. (a) 100mm Si/SiC bonded wafers with a (1) 1-µm, (2) 2-µm or (3) 5-µm-thick Si film, as well as TEM views of the Si/SiC interfaces, showing (1) no interfacial layer, (2)&(3) presence of an amorphous layer and (4) an island-like defect, respectively [156]

As such, it is expected that the dislocation of Si atoms close to the interface can degrade the device performance if a thin Si layer is used. However, Shinohara et al. proved that in their Si/SiC bonded wafers, with a 1 µm thick Si layer, the channel mobility of the fabricated MOSFETs is 575 $cm^2V^{-1}S^{-1}$ at room temperature, higher than that of the bulk-Si counterpart (489 $cm^2V^{-1}S^{-1}$)[14]. This is probably due to the presence of tensile strain in the Si film, which increases the electron mobility [85].In addition, other device

characteristics are very similar between the Si/SiC and bulk-Si, meaning that the transferred Si retains the quality of the seed wafer and the physical damage after bonding is negligible. Lotfi et al. also found similarities in most of their results extracted from Si/poly-Si/poly-SiC and SOI LDMOSFETs with two main differences, namely the leakage current and breakdown voltage [130]. Specifically, the slightly higher leakage in the Si/SiC is likely to be caused by the use of the poly-Si interlayer and poly-SiC substrate. The lower breakdown voltage is attributed to the lack of RESURF effect in the Si/SiC architecture [130]. In summary, the Si layer in the Si/SiC wafer can be as good as those of the bulk-Si and SOI. This means that there is no need to change the parameters and physical behaviour of Si material in the TCAD models (e.g. carrier mobility), for modelling the Si/SiC devices.

C.2 The (SI) SiC substrate

The electrical conductivity of a semiconductor can be characterised by the position of Fermi level with respect to the conduction and valance band. If the Fermi level is not close to either band, the material has a minimal number of electrons and holes available for current conduction. When a large bandgap is present in the semiconductor (e.g. SiC), the fermi level can be so far away from the two band edges that the quantity of carriers is extremely low, leading to semi-insulating behaviour. In practice, one way to form (SI) SiC is to introduce deep-level dopants such as vanadium, which pins the fermi level near the middle of SiC bandgap [166]. 4H-SiC [166], 6H-SiC [58] and even poly SiC [130] can be engineered to become a semi-insulator. In spite of being less thermal conductive [167] and lower resistivity, (SI) poly SiC is more advantageous over other polytypes in terms of wafer size and price. It should be noted that the resistivity of (SI) 4H/6H-SiC will drop from 10^{10} Ωcm (room temperature) to 10^{5}~10^{7} Ωcm at 300 °C [168] [169]. Nevertheless, these values are still at least two order magnitude higher than that (10^{3} Ωcm [39]) of the Si with n-type doping of 10^{13} cm^{-3} at room temperature. This indicates that the (SI) SiC substrate acts like an insulator in the Si/SiC device up to 300 °C. Therefore, the TCAD models do not need to expand to consider the SiC physics in terms of current conduction (e.g. anisotropy carrier mobility).

The intrinsic property of (SI) SiC significantly boosts the voltage capability of a lateral MOSFET, but at the expense of a weaker RESURF effect. Huang et al. have fabricated

and analysed different HV lateral SiC devices built on the (SI) SiC platform [170] [171] [42] (see Fig. C.5). The use of (SI) SiC as a substrate material instead of p type SiC eases the vertical breakdown limit, allowing high voltages beyond 2 kV to be achieved in lateral SiC transistors [42]. Nonetheless, all their devices have a buried p-type layer for charge balancing (see Fig. C.5), otherwise the n-type dose has to be lowered to maintain the same blocking voltage [170] [171] [42]. This indicates that the (SI) SiC is neutral and does not offer any significant substrate assisted depletion (SAD) effect [42]. Furthermore, it has been shown that the carrier lifetime of (SI) SiC is about 100 ps, meaning that conductivity modulation in bipolar devices will not be aided by such substrate [171]. To represent these intrinsic properties, no doping is specified for the (SI) SiC material in the simulation (default settings). Furthermore, the inclusion of SiC breakdown mechanism is unnecessary in the TCAD models as the maximum blocking voltage in the simulation is only 700 V, far lower than the 2 kV mentioned above.

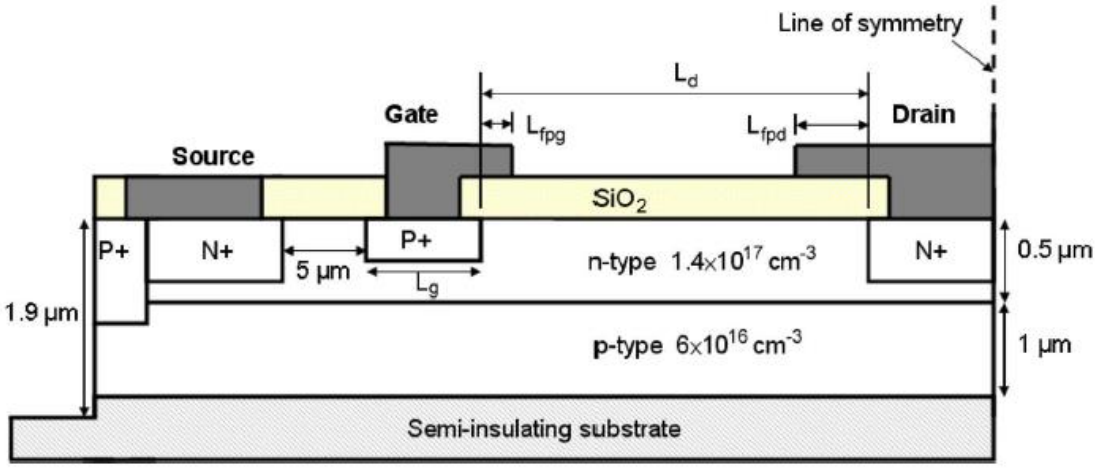

Figure C.5. A cross-sectional view of a 4H-SiC lateral JFET on a (SI) SiC substrate, able to block voltage up to 3500 V [170]

The superior heat transfer ability of (SI) SiC has been proven experimental in [14], where the Si/6H-SiC MOSFET was exposed to hot air at 300 °C and mounted on a cooling device at 15 °C. The same setup applied to the equivalent bulk Si MOSFET [14]. Compared with the case at room temperature, the channel mobility of both transistors decreased but the Si/SiC only suffered a 10% drop whereas this is 82% in the bulk-Si, a result indicative of remarkable thermal properties. However, it has to be mentioned that this heat transfer ability will be weakened if the temperature difference between the front (MOSFETs) and back side (cooling equipment) is small. To simulate this cooling effect,

it is necessary to configure the thermal properties of different materials. This can be found in Appendix A and was used along with the TCAD models in the electro-thermal simulation.

C.3 The Si/SiC interface

In [131], the interface charges of Si/ (SI) 6H-SiC was obtained from a PN diode manufactured on a nearly intrinsic Si layer with different doping types ($N_d/N_a = 10^{13}\ cm^{-3}$). Comparison between this diode on the Si/SiC and bulk-Si wafer found that a significant leakage current was only produced in the n-type Si on SiC, with the p-type samples having a leakage one order magnitude lower than the bulk-SiC reference [131]. This indicates that their bonded wafers had a device-quality Si layer with good electrical insulation properties, and that the leakage is likely to be induced by the depletion or inversion of the very low-doped N-type region [131]. The Si/SiC interface charge density was extracted to be less than -2×10^{10} cm^{-2} [131], a value comparable to that of Si/SiO_2 ($+4\times10^{10}$ cm^{-2} [124]) and far lower than the first order RESURF dose (1×10^{12} cm^{-2}). In their Si/SiC wafer, with a 16 μm thick Si layer, the impurity dose is calculated to be 1.6×10^{10} cm^{-2}, a value not high enough to counteract the interface charge and hence a back surface conductive channel can be induced. This is very similar to the Silicon on Sapphire (SOS) case [172], albeit their interface charge was positive charge, not negative. In [172], McGreivy reported that the leakage in n-type SOS MOSFETs was consistently lower than that in their p-type counterparts from wafer to wafer, due to the presence of donor-like defects at the Si/Al_2O_3 interface. This leakage difference was significantly reduced after the deep boron implantation was used for the p-type sample, as the extra acceptors obstructed the formation of space charge and an inversion region was induced by the positive interface charge [172]. Likewise, it is expected that the Si/SiC interfacial effect can be addressed by using a Si layer with a high dose, with the maximum value determined by the RESURF principle.

Another problem related to the Si/SiC interface is its effect on the thermal conductivity and breakdown voltage. During the hydrophilic wafer bonding process, a very thin SiO_2 (e.g. ~3 nm) can be produced between the Si and SiC. Such dielectric layer can degrade the heat transfer ability and also create a capacitive effect that could lead to premature

breakdown, which is similar to the SOI case. However, it is questionable if this parasitic structure functions like a capacitor, as the SiC is semi-insulating and carriers can tunnel through the very thin SiO_2. Loti et al. reported that their Si/SiC LDMOSFETs had a lower breakdown voltage than the SOI reference [130]. However, it was concluded that the poorer breakdown capability was caused by the lack of back depletion [130].

It is found that the SiO_2 interlayer in the Si/SiC structure can be thinned down or completely removed by high temperature long time annealing (>1150 °C, >2.5 h) [173]. These conditions permit the oxygen atoms at the interface to diffuse out of the bonded sample while recrystallising the interfacial Si lattice to some degree [173]. However, pyramidal defects can appear at the interface if the annealing temperature is above 1000 °C [165]. This Si dislocation is similar to the island-like defect present in our Si/SiC wafers annealed at 1200 ^{0} C, as shown in Fig. C.4. To summarise, caution should be taken on how to conduct this oxide-free process as it can cause crystal defects at the Si/SiC interface. It is possible that the impact of the thin SiO_2 on device performance is so small that this process is not necessary. Based upon these results, it is concluded that the TCAD models can represent the physics of the Si/SiC interface by simply setting the Si/SiC interface charge value to be -2×10^{10} cm^{-2}.

References

[1] D. Disney and Z. J. Shen, "Review of Silicon Power Semiconductor Technologies for Power Supply on Chip and Power Supply in Package Applications," *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 28, no. 9, pp. 4168-4181, 2013.

[2] D. Disney, T. Letavic, T. Trajkovic, T. Terashima and A. Nakagawa, "High-Voltage Integrated Circuits: History, State of the Art, and Future Prospects," *IEEE Transactions on Electron Devices,* vol. 64, no. 3, pp. 659 - 673, 2017.

[3] M. Rub, M. Bar, G. Deml, H. Kapels, M. Schmitt, S. Sedlmaier, C.Tolksdorf and A. Willmeroth, "A 600V 8.7Ohmmm2 Lateral Superjunction Transistor," *in Proc. Int. Symp. Power Semiconductor Devices and ICs (ISPSD),* p. 305–308, 2006.

[4] H. Boezen, "SOI in Automotive IC Design," *NXP Semiconductors,* pp. available online: https://www.wesrch.com/electronics/paper-details/pdf-EL1SE1000SMNO-soi-in-automotive-ic-design#page1, 2015.

[5] H. T Lim, F. Udrea, D. M. Garner, W. I. Milne, "Modelling of self-heating effect in thin SOI and Partial SOI LDMOS power devices," *Solid-State Electronics,* Vols. 43, iss. 7, pp. 1267-1280, 1999.

[6] J. Roig, D. Flores, I. Cortes, S. Hidalgo and J. Millan, "Thin film SOI and SOS LDMOS structures with Linear Doping Profile and enlarged field plate," *Microelectronics, 2004. 24th International Conference on,* vol. 1, pp. 141-144, 2004.

[7] S. D. Hu, X. R. Luo, B. Zhang, and Z. J. Li, "Design of compound buried layer SOI high voltage device with double windows," *Electron. Lett.,* Vols. 46, iss. 1, pp. 82-84, 2010.

[8] P. Baine et al., "Improved Thermal Performance of SOI Using a Compound Buried Layer," *Electron Devices, IEEE transactions on,* vol. 61, pp. 1999-2006, 2014.

[9] S. Arulkumaran, T. Egawa, H. Ishikawa and T. Jimbo, "High-temperature effects of AlGaN/GaN high electron-mobility transistors on sapphire and semi-insulating SiC substrates," *Applied Physics Letters,* vol. 80, pp. 2186-2188, 2002.

[10] C. F. Huang, C. L. Kan, T. L. Wu, M. C. Lee, Y. Z. Liu, K. Y. Lee and F. Zhao, "3510-V 390-mΩ cm2 4H-SiC Lateral JFET on a Semi-Insulating Substrate," *IEEE Electron Device Letters,* Vols. 30, iss. 9, pp. 957-959, 2009.

[11] C. Hettler, W. W. Sullivan, J. Dickens and A. Neuber, "Performance and Optimization of a 50 kV Silicon Carbide Photoconductive Semiconductor Switch for Pulsed Power Applications," *IEEE International Power Modulator and High Voltage Conference (IPMHVC), San Diego, CA, USA,* pp. 70-72, 2012.

[12] R. Chu, Y. Cao, M. Chen, R. Li, and D. Zehnder, "An Experimental Demonstration of GaN CMOS Technology," *IEEE Electron Device Letters,* vol. 37, no. 3, pp. 269-271, 2016.

[13] M. R. Jennings, A. Perez-Tomas, O. J. Guy, R. Hammond, S. E. Burrows, P. M. Gammon, M. Lodzinski, J. A. Covington, and P. A. Mawby, "Si/SiC Heterojunctions Fabricated by Direct Wafer Bonding," *Electrochem. Solid-State Lett.,* vol. 11, pp. H306-H308, 2008.

[14] H. Shinohara, H. Kinoshita, and M. Yoshimoto, "Si metal-oxide-semiconductor field-effect transistor on Si-on-SiC directly bonded wafers with high thermal conductance," *Applied Physics Letters 93, 122110,* 2008.

[15] S. Lotfi, L.-G. Li, Ö. Vallin, L. Vestling, H. Norström and J. Olsson, "LDMOS-transistors on semi-insulating silicon-on-polycrystalline-silicon carbide substrates for improved RF and thermal properties," *Solid-State Electronics,* vol. 70, pp. 14-19, 2012.

[16] A. Perez-Tomas, M. Lodzinski, O. J. Guy, M. R. Jennings, M. Placidi, J. Llobet, P. M. Gammon, M. C. Davis, J. A. Covington, S. E. Burrows, and P. A. Mawby, "Si/SiC bonded wafer: A route to carbon free SiO2 on SiC," *Appl. Phys. Lett. 94,* Vols. 94, 103510, 2009.

[17] S. Lotfi, "Design and Characterization of RFLDMOS Transistors and Si-on-SiC Hybrid Substrates," *Ph.D. dissertation, Uppsala University, 2014.*

[18] P. A. Mawby, "Basic Device Physics," *CPE Tutorial, The University of Warwick,* 5th June, 2015.

[19] J. M. O'Connor, J. C. Tsang and J. B. McKitterick ", "225 C high temperature silicon-on-insulator (SOI) ASICs for harsh environments," *IWIPP Proceedings. IEEE International Workshop on Integrated Power Packaging (Cat. No.98EX203), Chicago, IL,* pp. 2-5, 1998.

[20] W. Wondrak, "Physical Limits and Lifetime Limitations of Semiconductor Devices at High Temperatures," *Microelectronics Reliability,* vol. 39, pp. 1113-1120, 1999.

[21] http://www.mouser.co.uk/applications/harsh-environment-technology/, Date accessed: 2017.

[22] P. L. Dreike, D. M. Fleetwood, D. B. King, D. C. Sprauer and T. E. Zipperian, "An overview of high-temperature electronic device technologies and potential applications," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A,* vol. 17, no. 4, pp. 594-609, 1994.

[23] D. J. Hoffman, et al., "Concept design of high power solar electric propulsion vehicles for human exploration," 2011.

[24] L. R. Piñero and G. E. Bowers, "Multi-kilowatt power module for high-power Hall thrusters," *40th AIAA Joint Propulsion Conference, AIAA–2004–3973, Fort Lauderdale, FL,* 2004.

[25] R. Singh and B. Baliga, "Analysis and optimization of power MOSFETs for cryogenic operation," *Solid-state electronics,* vol. 36, pp. 1203-1211, 1993.

[26] Y. Liu, "Power Electronic Packaging: Design, Assembly Process, Reliability," *Springer-Verlag New York,* 2012.

[27] C. N. Liao, C. Chen, and K. N. Tu, "Thermoelectric characterization of Si thin films in silicon-on-insulator wafers," *Journal of Applied Physics,* vol. 86, pp. 3204-3208, 1999.

[28] Motorola Analog Products Division, "Power Integrated Circuit Switch Training," *http://cache.freescale.com/files/analog/doc/train_ref_material/ANALOGPOWERICTR.pdf?WT_TYPE=Traini_1,* Date accessed: 2017.

[29] STMicroelectronics, "N-channel 600V FDmesh™ Power MOSFET (with fast diode),"

http://www.st.com/content/ccc/resource/technical/document/datasheet/f3/75/e5/d4/f9/68/46/97/CD00003368.pdf/files/CD00003368.pdf/jcr:content/translations/en.CD00003368.pdf, 2006.

[30] Vishay Siliconix, "IRF540, SiHF540 Power MOSFET," *https://www.vishay.com/docs/91021/91021.pdf,* 2017.

[31] ON Semiconductor, "Reliability Stress Test Descriptions," *https://www.fairchildsemi.com/Assets/-Policies/Quality-Reliability/Reliability-Stress-Test-Descriptions.pdf,* Date accessed: 19/01/2018.

[32] Texas instruments, "Reliability testing," *http://www.ti.com/support-quality/reliability/reliability-testing.html,* Date accessed: 19/01/2018.

[33] S. Poli, S. Reggiani, G. Baccarani, E. Gnani, A. Gnudi, M. Denison, S. Pendharkar, R. Wise and S. Seetharaman, "Investigation on the temperature dependence of the HCI effects in the rugged STI-based LDMOS transistor," *Proceedings of The 22nd International Symposium on Power Semiconductor Devices & ICs, Hiroshima,* pp. 311-314, 2010.

[34] O. Triebl, "Reliability Issues in High-Voltage Semiconductor Devices," *PhD thesis, Technischen Universität Wien,* 2012.

[35] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose, and R. Ida, "A Double RESURF LDMOS With Drain Profile Engineering for Improved ESD Robustness," *IEEE Electron Device Letters,* vol. 23, no. 4, pp. 212-214, 2002.

[36] T. Paul Chow, Ichiro Omura, Masataka Higashiwaki, Hiroshi Kawarada and Vipindas Pala, "Smart Power Devices and ICs Using GaAs and Wide and Extreme Bandgap Semiconductors," *IEEE TRANSACTIONS ON ELECTRON DEVICES (Invited paper),* vol. 64, no. 3, pp. 856-873, 2017.

[37] S. Hamady, "New concepts for normally-off power Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT)," *PhD thesis, Micro and nanotechnologies/Microelectronics. Universite,* 2014.

[38] P. M. Gammon, "Development of SiC Heterojunction Power Devices," *PhD thesis, the University of Warwick,* May 2011.

[39] S. M. Sze, "Physics of Semiconductor Devices," *Hoboken, New Jersey, USA: John Wiley and Sons,* 1981.

[40] Y. Kitabayashi, T. Kudo, H. Tsuboi, T. Yamada, D. Xu, M. Shibata, D. Matsumura, Y. Hayashi, M. Syamsul, M. Inaba, A. Hiraiwa, and H. Kawarada, "Normally-Off C–H Diamond MOSFETs With Partial C–O Channel Achieving 2-kV Breakdown Voltage," *IEEE Electron Device Letters,* vol. 38, no. 3, pp. 363-366, 2017.

[41] R. T. Kemerley, H. B. Wallace and M. N. Yoder, "Impact of wide bandgap microwave devices on DoD systems," *in Proceedings of the IEEE,* vol. 90, no. 6, pp. 1059-1064, 2002.

[42] W. S. Lee et al., "Design and Fabrication of 4H–SiC Lateral High-Voltage Devices on a Semi-Insulating Substrate," *IEEE Transactions on Electron Devices,* Vols. 59, iss. 3, pp. 754-760, 2012.

[43] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," *Applied Physics Reviews,* vol. 2, p. 021307, 2015.

[44] F. Udrea, G. Deboy and T. Fujihira, "Superjunction Power Devices, History, Development, and Future Prospects," *IEEE Transactions on Electron Devices,* vol. 64, no. 3, pp. 720-734, 2017.

[45] M. M. H. Iqbal, F. Udrea and E. Napoli, "On the static performance of the RESURF LDMOSFETS for power ICs," *2009 21st International Symposium on Power Semiconductor Devices & IC's, Barcelona,* pp. 247-250, 2009.

[46] E. Arnold, T. Letavic, S. Merchant, and H. Bhimnathwala, "High-Temperature Performance of SOI and Bulk-Silicon RESURF LDMOS Transistors," *in Proc. ISPSD,* pp. 93-96, 1996.

[47] Ioffe Physico-technical institute , "Electronic archive New Semiconductor Materials. Characteristics and Properties," *http://www.ioffe.ru/SVA/NSM/Semicond/GaAs/electric.html, Date accessed: Aug 2017,* 2017.

[48] C.A. Fisher, "Development of 4H-SiC PiN Diodes for High Voltage Applications," *PhD thesis,* Feb 2014.

[49] W. J. Schaffer, G.H. Negley, K.G. Irvine and J.W. Palmour, "Conductivity Anisotropy in Epitaxial 6H and 4H SiC," *MRS Proceedings,* vol. 339, pp. 595-600, 1994.

[50] S. Chowdhury, C. Hitchcock, Z. Stum, R. P. Dahal, I. B. Bhat and T. P. Chow, "Experimental Demonstration of High-Voltage 4H-SiC Bi-Directional IGBTs," *IEEE Electron Device Letters,* vol. 37, no. 8, pp. 1033-1036, 2016.

[51] D. Peters et al., "The New CoolSiC™ Trench MOSFET Technology for Low Gate Oxide Stress and High Performance," *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany,* pp. pp. 1-7., 2017.

[52] T. Kimoto,H. Kosugi, J. Suda, Y. Kanzaki, and H. Matsunami, "Design and Fabrication of RESURF MOSFETs on 4H-SiC(0001), (1120), and 6H-SiC(0001)," *IEEE Transactions on Electron Devices,* vol. 52, no. 1, pp. 112-117, 2005.

[53] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi and M. Higashiwaki, "Field-Plated Ga2O3 MOSFETs With a Breakdown Voltage of Over 750 V," *in IEEE Electron Device Letters,* vol. 37, no. 2, pp. 212-215, 2016.

[54] S. A. O. Russell et al., "Heteroepitaxial Beta-Ga2O3 on 4H-SiC for an FET With Reduced Self Heating," *in IEEE Journal of the Electron Devices Society ,* vol. 5, no. 4, pp. 256-261, 2017.

[55] J. B. Varley, A. Janotti, C. Franchini, and C. G. Van de Walle, "Role of self-trapping in luminescence and p-type conductivity of wide-band-gap oxides," *Phys. Rev. B, Condens. Matter,* vol. 85, p. 081109R, 2012.

[56] A. Daicho, T. Saito, S. Kurihara, A. Hiraiwa and H. Kawarada, "High-reliability passivation of hydrogen-terminated diamond surface by atomic layer deposition of Al2O3," *Journal of Applied Physics,* vol. 115, pp. 223711-1 - 223711-4, 2014.

[57] H. Fu, I. Baranowski, X. Huang, H. Chen, Z. Lu, J. Montes, X. Zhang, and Y. Zhao, "Demonstration of AlN Schottky barrier diodes with blocking voltage over 1kV," *IEEE Electron Device Letters,* vol. 38, no. 9, pp. 1286-1289, 2017.

[58] C. James, C. Hettler and J. Dickens, "High voltage photoconductive switches using semi-insulating, vanadium doped 6H-SiC," *2009 IEEE Pulsed Power Conference, Washington, DC,* pp. 283-286, 2009.

[59] C. James, C. Hettler, and J. Dickens, "High-Purity Semi-Insulating 4H-SiC as a High-Voltage Switch Material," *IEEE International Power Modulator and High Voltage Conference, Atlanta, GA,* pp. 282-284, 2010.

[60] C. M. Armstrong, "The quest for the ultimate vacuum tube," *in IEEE Spectrum*, vol. 52, no. 12, pp. 28-51, 2015.

[61] Evince Technology, "Making A Practical Diamond Device," *http://www.evincetechnology.com/techoverview.html,* p. Date accessed: May 2017, 2017.

[62] A. W. Ludikhuize , "Kirk effect limitations in high voltage IC's," *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics, Davos,* pp. 249-252, 1994.

[63] P. L. Hower et al., "Avalanche-induced thermal instability in Ldmos transistors," *in Proc. 13th Int. Symp. Power Semiconductor Device ICs,* pp. 153-156, 2001.

[64] P. L. Hower, "Safe Operating Area -- a New Frontier in Ldmos Design," *Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics,* pp. 1-8, 2002.

[65] B. Sampath Kumar and M. Shrivastava, "Part I: On the Unification of Physics of Quasi-Saturation in LDMOS Devices," *IEEE Transaction on Electron Devices,,* vol. 65, no. 1, pp. 191-198, 2018.

[66] M. Yamaji, K. Abe, T. Maiguma, H. Takahashi and H. Sumida, "A novel 600V-LDMOS with HV-interconnection for HVIC on thick SOI," *in Proc. ISPSD, Hiroshima,* pp. 101-104, 2010.

[67] M. Rabarot et al., "Silicon-On-Diamond layer integration by wafer bonding technology," *Proceedings of Diamond 2009, The 20th European Conference on Diamond,* Vols. 19, iss. 7-9, p. 796–805, 2010.

[68] J. Roig, D. Flores, S. Hidalgo, M. Vellvehi, J. Rebollo and J. Millan, "Study of novel techniques for reducing self-heating effects in SOI power LDMOS," *Solid-State Electronics,* vol. 46, pp. 2123-2133, 2002.

[69] B. A. Biegel, M. A. Osman and Z. Yu, "Analysis of aluminium-nitride SOI for high temperature electronics," *HiTEC 2000,* 2000, available on line: http://people.nas.nasa.gov/~biegel/pubs/hitec_paper.pdf.

[70] J.M. Park, T. Grasser, H. Kosina and S. Selberherr, "A numerical study of partial-SOI LDMOSFETs," *Solid-State Electronics,* vol. 47, pp. 275-281, 2003.

[71] F. Udrea A. Mihaila and R. Azar, "Silicon/Oxide/Silicon Carbide (SiOSiC)-A new approach for high voltage, high frequencies integrated circuits," *Materials Science Forum,* Vols. 389-393, pp. 1255-1258, 2002.

[72] E.K.C Tee, M. Antoniou, F. Udrea, A. Holke, D. K. Pal, L. Y. Ng and W.A.B.W.Z. Abidin, "Analysis on the off-state design and characterization of LIGBTs in partial SOI technology," *Solid State Electronics,* vol. 96, pp. 38-43, 2014.

[73] H. T. Lim, F. Udrea, D. M. Garner, K. Sheng and W. I. Milne, , "Partial SOI LDMOSFETs for high-side switching," *Semiconductor Conference, 1999. CAS '99 Proceedings. 1999 International, Sinaia,,* vol. 1, pp. 149-152, 1999.

[74] Y. Baba, S. Yanagiya, Y. Koshino and Y. Udo, "High voltage trench drain LDMOS-FET using SOI wafer," *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics, Davos,* pp. 183-186, 1994.

[75] K. Watabe, H. Akiyama, T. Terashima, S. Nobuto, M. Yamawaki and T. Hirao, ,, "A 0.8 μm high voltage IC using newly designed 600 V lateral IGBT on thick buried-oxide SOI," *in Proc. of ISPSD,* pp. pp. 151-154, 1996.

[76] H. Akiyama, N. Yasuda, J. Moritani, K. Takanashi and G. Majumdar, "A high breakdown voltage IC with lateral power device based on SODI structure," *2004*

Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs, Kitakyushu, Japan, pp. 375-378, 2004.

[77] X. Luo, B. Zhang, and Z. Li, "New High-Voltage (> 1200 V) MOSFET With the Charge Trenches on Partial SOI," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 55, no. 7, pp. 1756-1761, 2008.

[78] J. M. Dilhac, D. Zerrouk, C. Ganibal, P. Rossel and M. Bafleur, "Fabrication of SOI structures by uniform zone melting recrystallization for high voltage ICs," *in Proc. ISPSD* , pp. 215-218, 1996.

[79] Zhuo Wang, Muting Lu, Xin Zhou, Jun Wang, Wen Yang and Bo Zhang, "A novel SON LDMOS with Triple-RESURF technology," *Superlattices and Microstructures* , vol. 75, p. 151–158, 2014.

[80] B. C. Jeon, D. Y. Kim, Y. S. Lee, J. K. Oh, M. K. Han and Y. I. Choi, "Buried air gap structure for improving the breakdown voltage of SOI power MOSFET's," *Proceedings IPEMC 2000,* vol. 3, pp. 1061-1063, 2000.

[81] T. Okawa, H. Eguchi, M. Taki and K. Hamada, "2000 V SOI LDMOS with new drift structure for HVICs," *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague,* pp. 435-438, 2016.

[82] T. Trajkovic, N. Udugampola, V. Pathirana, A. Mihaila, F. Udrea, G. A. J. Amaratunga, Bill Koutny, K. Ramkumar and S Geha, "High frequency 700V PowerBrane LIGBTs in 0.35µm Bulk CMOS Technology," *in Proc. Int. Symp. Power Semiconductor Devices ICs,* p. 307–310, 2009.

[83] T. Trajkovic, F. Udrea, C. Lee, N. Udugampola, V. Pathirana, A. Mihaila and G. A. J. Amaratunga, "Thick silicon membrane technology for reliable and high performance operation of high voltage LIGBTs in Power ICs," *in Proc. Int. Symp. Power Semiconductor Devices ICs,* pp. 327-330, 2008.

[84] G. P. Imthurn, A. M. Miscione, K. Landry, A. Vaufredaz, T. Barge, and C. Lagahe-Blanchard, "Strain reduction in silicon-on-sapphire by wafer bonding," *in Proc. IEEE Int. SOI Conf. (SOI),* pp. 1-2, 2011.

[85] Florin Udrea, "SEMICONDUCTOR DEVICE IN WHICH AN INJECTOR REGION IS ISOLATED FROM A SUBSTRATE," *United States Patent, US 7465964 B2,* 2008.

[86] F. Udrea, A. Popescu and W. I. Milne , "A new class of lateral power devices for HVIC's based on the 3D RESURF concept," *Bipolar/BiCMOS Circuits and Technology Meeting, Minneapolis, MN,* pp. 187 - 190, 1998.

[87] S. Duangchan, Y. Uchikawa, Y. Koishikawa, B. Akiyoshi, K. Nakagawa, S. Matsumoto and M. Hasegawa, "The silicon on diamond structure by low-temperature bonding technique," *Electronic Components and Technology Conference (ECTC),* pp. 187-192, 2015.

[88] R. E. Reedy, T. W. Sigmon, and L. A. Christel, "Suppressing AI outdiffusion in implantation amorphized and recrystallized silicon on sapphire films," *Applied Physics Letters,* vol. 42, pp. 707-709, 1983.

[89] B. Duan, Z. Cao, S. Yuan and Y. Yang, "Complete 3D-Reduced Surface Field Superjunction Lateral Double-Diffused MOSFET Breaking Silicon Limit," *in IEEE Electron Device Letters,* vol. 36, no. 12, pp. 1348-1350, 2015.

[90] L. Vestling, B. Edholm, J. Olsson, S. Tiensuu and A. Soderbarg, "A novel high-frequency high-voltage LDMOS transistor using an extended gate RESURF technology," *Power Semiconductor Devices and IC's, 1997. ISPSD '97,* pp. 45-48, 1997.

[91] Y. Zhang, S. Pendharkar, P. L. Hower, S. Giombanco, A. Amoroso, F. Marino, "A RESURF P-N Bimodal LDMOS Suitable for High Voltage Power Switching

Applications," *Proceedings of the 27th International Symposium on Power Semiconductor Devices & IC's*, pp. 61-64, 2015.

[92] J. Wei, X. Luo, Y. Zhang, P. Li, K. Zhou, B. Zhang and Z. Li, "High-Voltage Thin-SOI LDMOS With Ultralow ON-Resistance and Even Temperature Characteristic," *IEEE Transactions on Electron Devices*, vol. 63, no. 4, pp. 1637-1643, 2016.

[93] X. Chen, "Lateral low-side and high-side high-voltage devices," *U.S. Patent 6 998 681 B2*, Feb. 14, 2006..

[94] A. Popescu, F. Udrea, R. Ng and W. I. Milne, "Analytical modelling for the RESURF effect in JI and SOI power devices," *IEE Proceedings - Circuits, Devices and Systems*, vol. 149, no. 56, pp. 273-284, 2002.

[95] A. W. Ludikhuize, "A versatile 700-1200-V IC process for analog and switching applications," *IEEE Transactions on Electron Devices*, vol. 38, no. 7, pp. 1582-1589, 1991.

[96] B. K. Boksteen, A. Ferrara, A. Heringa, P. G. Steeneken, G. E. J. Koops and R. J. E. Hueting, "Design optimization of field-plate assisted RESURF devices," *Proceedings of The 25th International Symposium on Power Semiconductor Devices & ICs, Kanazawa*, pp. 237-240, 2013.

[97] W. Zhang, B. Zhang, M. Qiao, Z. Li, X. Luo and Z. Li, "Optimization of Lateral Superjunction Based on the Minimum Specific ON-Resistance," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 1984-1990, 2016.

[98] D. R. Disney, A. K. Paul, M. Darwish, R. Basecki and V. Rumennik, "A new 800V lateral MOSFET with dual conduction paths," *in Proc. ISPSD*, pp. 399-402, 2001.

[99] S. Merchant, E. Arnold, H. Baumgart, S. Mukherjee, H. Pein and R. Pinker, "Realization of high breakdown voltage (>700 V) in thin SOI devices," *in Proc. ISPSD*, pp. 31-35, 1991.

[100] R. Ng, F. Udrea, K. Sheng, K. Ueno, G.A.J. Amaratunga and M. Nishiura, "Lateral Unbalanced Super Junction (USJ)/3D-RESURF for High breakdown voltage on SOI," *in Proc. of ISPSD*, pp. 395-398, 2001.

[101] S. Hardikar, M.M. De Souza, Y.Z. Xu, T.J. Pease, E.M. Sankara Narayanan, "A novel double RESURF LDMOS for HVIC's," *Microelectronics Journal*, vol. 35, p. 305–310, 2004.

[102] S. Hardikar, R. Tadikonda, D. W. Green, K. V. Vershinin and E. M. S. Narayanan, "Realizing High-Voltage Junction Isolated LDMOS Transistors With Variation in Lateral Doping," *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 51, no. 12, pp. 2223-2228, 2004.

[103] M. F. Kong and X. B. Chen, "High voltage low side and high side power devices based on VLD technique," *IEEE 11th International Conference on Solid-State and Integrated Circuit Technology*, pp. 1-3, 2012.

[104] Wen-Yi Chen and Ming-Dou Ker, "Characterization of SOA in Time Domain and the Improvement Techniques for Using in High-Voltage Integrated Circuits," *IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY*, vol. 12, no. 2, pp. 382-390, 2012.

[105] Z. Hossain, M. Imam, J. Fulton and M. Tanaka, "Double-RESURF 700 V n-channel LDMOS with best-in-class on-resistance," *in Proc. of ISPSD*, pp. 137-140, 2002.

[106] F. Udrea, A. Popescu and W. I. Milne, "3D RESURF double-gate MOSFET: a revolutionary power device concept," *Electronics Letters*, vol. 34, no. 8, pp. 808-809, 1998.

[107] Y. Zhang, S. Pendharkar, P. Hower, S. Giombanco, A. Amoroso and F. Marino, "A RESURF P-N bimodal LDMOS suitable for high voltage power switching applications," *IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong Kong,* pp. 61-64, 2015.

[108] F. Udrea, "SOI-based devices and technologies for High Voltage ICs," *2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Boston,* pp. 74-81, 2007.

[109] S. Merchant, E. Arnold and M. Simpson, "Tunneling in Thin SOI High Voltage Devices," *in Proc. ISPSD,* pp. 130-135, 1995.

[110] J. Petruzzello, T. Letavic, H. van Zwol, M. Simpson and S. Mukherjee, "A thin-layer high-voltage silicon-on-insulator hybrid LDMOS/LIGBT device," *Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics,* pp. 117-120., 2002.

[111] T. Erlbacher, "Modern MOS-Based Power Device Technologies in Integrated Circuits," *in Lateral Power Transistors in Integrated Circuits. Switzerland: Springer,* pp. 105-131, 2014.

[112] T. Letavic, J. Petruzzello, J. Claes, P. Eggenkamp, E. Janssen and A. van der Wal, "650V SOI LIGBT for Switch-Mode Power Supply Application," *2006 IEEE International Symposium on Power Semiconductor Devices and IC's, Naples,* pp. 1-4, 2006.

[113] T. Letavic, M. Simpson, E. Arnold, E. Peters, R. Aquino, J. Curcio, S. Herko and S. Mukherjee, "600 V power conversion system-on-a-chip based on thin layer silicon-on-insulator," *in Proc. ISPSD,* pp. 325-328, 1999.

[114] E. Arnold, S. Merchant, M. Amato, S. Mukherjee and H. Pein, "Comparison of junction-isolated and soi high-voltage devices operating in the source-follower mode," *in Proc. ISPSD,* p. 242–243, 1992.

[115] G. M. Dolny, G. E. Nostrand and K. E. Hill, "The effect of temperature on lateral DMOS transistors in a power IC technology," *in IEEE Transactions on Electron Devices,* vol. 39, no. 4, pp. 990-995, 1992.

[116] D. B. M. Klaassen, "A unified mobility model for device simulation - I. Model equations and concentration dependence, II. Temperature dependence of carrier mobility and lifetime," *Solid-state Electronics,* vol. 35, pp. 953-959, and 961-967, 1992.

[117] E. Arnold, H. Pein and S. P. Herko, "Comparison of self-heating effects in bulk-silicon and SOI high-voltage devices," in *Electron Devices Meeting, IEDM '94. Technical Digest., International,* San Francisco, CA, USA, pp. 813-816, 1994.

[118] D. B. M. Klaassen, "A unified mobility model for device simulation - I. Model equations and concentration dependence, II. Temperature dependence of carrier mobility and lifetime," *Solid-state Electronics,* vol. 35, pp. 953-959, and 961-967, 1992.

[119] I. M. Emmerik-Weijland, R. van Dalen, A. B. van der Wal and M. J. Swanenberg, "Development of high-side capable thyristors in thin SOI technology," *2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Kanazawa,* pp. 353-356, 2013.

[120] S. Merchant, "Method for making an improved high voltage thin-film transistor having a linear doping profile," *US patent, US005246870A,* Sep. 21, 1993.

[121] SILVACO, "Atlas User's Manual, DEVICE SIMULATION SOFTWARE," *Silvaco, Inc.,* August 26, 2016.

[122] T. Matsudai, Y. Yamaguchi, N. Yasuhara, A. Nakagawa and H. Mochizuki, "Thin SOI IGBT leakage current and a new device structure for high

temperature operation," *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics, Davos,* pp. 399-403, 1994.

[123] E. Arnold, T. Letavic and H. Bhimnathwala, "High-temperature off-state characteristics of thin-SOI power devices," *in IEEE Electron Device Letters,* vol. 17, no. 12, pp. 557-559, 1996.

[124] MA. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon," *J. Appl. Phys.,* vol. 67, pp. 2946-2954, 1990.

[125] R. Sunkavalli, B. J. Baliga and Y. S. Huang, "High temperature performance of dielectrically isolated LDMOSFET: characterization, simulation and analysis," *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics, Davos,* pp. 359-364, 1994.

[126] J. B. McKitterick, "Very thin silicon-on-insulator devices for CMOS at 500 C," *in Trans. 1st Int. High Temperature Electron. Con.,* pp. 37-41, 1991.

[127] A. Nakagawa, Y. Yamaguchi, T. Matsudai and N. Yasuhara, "200 C high-temperature and high-speed operation of 440 V lateral IGBTs on 1.5 um thick SOI," *Proceedings of IEEE International Electron Devices Meeting, Washington, DC, USA,* pp. 687-690, 1993.

[128] A. W. Ludikhuize et al., "Extended (180 V) voltage in 0.6 μm thin-layer-SOI A-BCD3 technology on 1 μm BOX for display, automotive and consumer applications," *Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics,* pp. 77-80, 2002.

[129] C.W. Chan, P. M. Gammon, V. A. Shah, H. Chen, M.R. Jennings, C.A. Fisher, A. Pérez-Tomás, M. Myronov and P.A. Mawby, "Simulations of a Lateral PiN Diode on Si/SiC Substrate for High Temperature Applications," *Materials Science Forum,* Vols. 821-823, pp. 624-627, 2015.

[130] K. Paul et al., "High voltage LDMOS transistors in sub-micron SOI films," *Power Semiconductor Devices and ICs, 1996. ISPSD '96 Proceedings., 8th International Symposium on, Maui, HI,* pp. 89-92, 1996.

[131] J. Roig, D. Flores, J. Rebollo, S. Hidalgo, and J. Millan, "A 200 V silicon-on-sapphire LDMOS structure with a step oxide extended field plate," *Solid-State Electron.,* vol. 48, no. 2, p. 245–252, 2004.

[132] T. Letavic, E. Arnold, M. Simpson, R. Aquino, H. Bhimnathwala, R. Egloff, A. Emmerik, S. Wong and S. Mukherjee, "High performance 600 V smart power technology based on thin layer silicon-on-insulator," *in Proc. ISPSD,* pp. 49-52, 1997.

[133] Y. Sasada, T. Kurumi, H. Shimizu, H. Kinoshita and M. Yoshimoto, "Junction formation via direct bonding of Si and 6H-SiC," *Materials Science Forum,* Vols. 778-780, pp. 714-717, 2014.

[134] J. S. Ajit, D. Kinzer and N. Ranjan, "1200 V high-side lateral MOSFET in junction-isolated power IC technology using two field-reduction layers," *Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs, Monterey CA,* pp. 230-235, 1993.

[135] D. Disney, I. L. Y. Park, W. C. Lin and J. Kim, , "High-voltage IC technologies for AC/DC power conversion," *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore,* pp. 142-145, 2015.

[136] Y. Suzuki, Y. K. Leung and S. S. Wong, "Influence of Parasitic Capacitances on Switching Characteristics of SOI-LDMOSs," *Proceedings of Intemational Symposium on Power Semiconductor Devices & ICs, Yokohama,* pp. 303-308, 1995.

[137] H . Neu brand, R. Constape and R. Boot, "Thermal Behaviour of Lateral Power Devices on SO1 Substrates," *Proc. of the 6th Internat. Symposium on Power Semiconductor Devices & IC's,* pp. 123-127, 1994.

[138] G. Van den bosch, P. Moens, P. Gassot, D. Wojciechowski and G. Groeseneken, "Analysis and application of energy capability characterization methods in power MOSFETs," *Solid-State Device Research conference, 2004 (ESSDERC),* pp. 453-456, 2004.

[139] D. Farenc, G. Charitat, P. Dupuy, T. Sicard, I. Pages and P. Rossel, "Clamped inductive switching of LDMOST for smart power IC's," *Power Semiconductor Devices and ICs,* pp. 359-362, 1998.

[140] C.W. Chan, Y. Bonyadi, P. A. Mawby and P. M. Gammon, "Si/SiC Substrates for the Implementation of Linear-Doped Power LDMOS Studied with Device Simulation," *Materials Science Forum,* vol. 858, pp. 844-847, 2016.

[141] C. W. Chan, F. Li, A. Sanchez, P. A. Mawby, P. M. Gammon, "Comparative Study of RESURF Si/SiC LDMOSFETs for High-Temperature Applications Using TCAD Modeling," *Electron Devices IEEE Transactions on,* vol. 64, pp. 3713-3718, 2017.

[142] C. Chan, P. A. Mawby and P. M. Gammon, "Analysis of Linear-Doped Si/SiC Power LDMOSFETs Based on Device Simulation," *in IEEE Transactions on Electron Devices,* vol. 63, no. 6, pp. 2442-2448, 2016.

[143] C. W. Chan, F. Li, P.A. Mawby and P.M. Gammon, "Numerical study of energy capability of Si/SiC LDMOSFETs," *Material Science Forum,* vol. 897, pp. 751-754, 2017.

[144] A. Nakagawa, "Power IC technologies," *in The VLSI Handbook, 2nd ed. Boca Raton, FL, USA: CRC Press,* 2007.

[145] Y. K. Leung et al., "Spatial Temperature Profiles Due to Nonuniform Self-Heating in LDMOS's in Thin SOI," *IEEE ELECTRON DEVICE LETTERS,* Vols. 18, iss. 1, pp. 13-15, 1997.

[146] F. Udrea, A. Popescu and W. I. Milne , "A new class of lateral power devices for HVIC's based on the 3D RESURF concept," *Bipolar/BiCMOS Circuits and Technology Meeting, Minneapolis, MN ,* pp. 187 - 190, 1998.

[147] A. W. Ludikhuize, "A versatile 700-1200-V IC process for analog and switching applications," *in IEEE Transactions on Electron Devices,* Vols. 38, iss. 7, pp. 1582-1589, 1991.

[148] E. Arnold, S. Merchant, M. Amato, S. Mukherjee, H. Pein, and M. A. Ludikhuize, "Comparison of junction-isolated and SOI high voltage devices operating in the source-follower mode," *in Proc. ISPSD,* p. 242–243, 1992.

[149] T. Letavic, M. Simpson, E. Arnold, E. Peters, R. Aquino, J. Curcio, S. Herko and S. Mukherjee, "600 V power conversion system-on-a-chip based on thin layer silicon-on-insulator," *in Proc. ISPSD,* pp. 325-328, 1999.

[150] T. Sakai, S. Matsumoto, I. J. Kim, T. Fukumitsu and T. Yachi, "Potential of SOI power MOSFETs as a switching device for megahertz DC/DC converters," *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE, Taipei,* vol. 1, pp. 450-456, 1994.

[151] Z. J. Shen, Y. Xiong, X. Cheng, Y. Fu and P. Kumar, "Power MOSFET Switching Loss Analysis: A New Insight," *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting, Tampa, FL,* pp. 1438-1442., 2006.

[152] F. Li, D. Giannopoulos and I. Wacyk, "A low loss high-frequency half-bridge driver with integrated power devices using EZ-HV SOI technology," *APEC.*

Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335), Dallas, TX, vol. 2, pp. 1127-1132, 2002.

[153] L. Yan, G. Koops, P. Steeneken, A. Heringa, R. Surdeanu, L. V. Dijk, "Integrated heat sinks for SOI power devices," *Proceedings of The 25th International Symposium on Power Semiconductor Devices & ICs, Kanazawa*, pp. 285-288, 2013.

[154] S. Lotfi, L.-G. Li, Ö. Vallin, L. Vestling, H. Norström, J. Olsson, "LDMOS-transistors on semi-insulating silicon-on-polycrystalline-silicon carbide substrates for improved RF and thermal properties," *Solid-State Electronics, vol. 70, pp. 14-19,* 2012.

[155] P. M. Gammon et al., "The effect of interfacial charge on the development of wafer bonded silicon-on-silicon-carbide power devices," *Mater. Sci. Forum.*, vol. 897, p. 747–750, 2017.

[156] W. Zhang, B. Zhang, M. Qiao, Z. Li, X. Luo and Z. Li, "Optimization and New Structure of Superjunction With Isolator Layer," *in IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 217-223, 2017.

[157] F. Udrea et al., "Ultra-fast LIGBTs and superjunction devices in membrane technology," *Proceedings. ISPSD '05. The 17th International Symposium on Power Semiconductor Devices and ICs, 2005., Santa Barbara, CA*, pp. 267-270, 2005.

[158] Y. K. Leung, A. K. Paul, K. E. Goodson, J. D. Plummer and S. S. Wong, "Heating Mechanisms of LDMOS and LIGBT in Ultrathin SOI," *in IEEE Electron Device Letters*, vol. 18, no. 9, pp. 414-416, 1997.

[159] O. Nilsson, H. Mehling, R. Horn, J. Fricke, R. Hofmann, S.G. Muller, R Eckstein and D. Hofmann, "Determination of the thermal diffusivity and conductivity of monocrystalline silicon carbide (300-2300 K)," *High Temperatures-High Pressures*, vol. 29, pp. 73-79, 1997.

[160] T. Ayalew, "SiC Semiconductor Devices, Technology, Modeling, and Simulation," *PhD thesis, Technische Universität Wien*, 2004.

[161] E. A. Burgemeister, W. von Muench, and E. Pettenpaul, "Thermal conductivity and electrical properties of 6H silicon carbide," *Journal of Applied Physics*, vol. 50, pp. 5790-5794, 1979.

[162] R. Wei, , S. Song, , K. Yang, , Y. Cui, , Y. Peng, , X. Chen, , X. Hu, and X. Xu, "Thermal conductivity of 4H-SiC single crystals," *Journal of Applied Physics 113,*, vol. 113, pp. 053503 1-053503 4, 2013.

[163] Poco Graphite, Inc edited by A. H. Rashed, "Properties and Characteristics of Silicon Carbide," *Poco Graphite, Inc. 300 Old Greenwood Rd. Decatur, TX 76234,* 2002, http://www.poco.com/Portals/0/Properties.and.Characteristics.of.Silicon.Carbide.pdf.

[164] Takamasa Kurumi et al., "TEM observation of directly bonded interface between Si and SiC," *2012 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK) ,* 2012.

[165] J. R. Jenny et al., "High-purity semi-insulating 4H-SiC grown by the seeded-sublimation method," *Journal of Electronic Materials*, vol. 31, no. 5, p. 366–369, 2002.

[166] L.-G. LI et al., "Thermal Characterization of Polycrystalline SiC," *Journal of ELECTRONIC MATERIALS*, vol. 43, no. 4, pp. 1150-1153, 2014.

[167] P. G. Muzykov et al., "High Resistivity Measurement of SiC Wafers Using Different Techniques," *Journal of ELECTRONIC MATERIALS,* vol. 32, no. 6, pp. 505-510, 2003.

[168] Wolfgang Jantz, Stefan Muller, Rudolf Stibal, "Investigation of Semi-Insulating SiC Wafers Using Contactless Topographic and Temperature-Dependent Resistivity Analysis," *The International Conference on Compound Semiconductor Manufacturing Technology, 4.4, avaliable on line: http://csmantech.org/OldSite/Digests/2005/2005papers/4.4.pdf ,* 2005.

[169] Chih-Fang Huang et al., "3510-V 390-mΩ · cm2 4H-SiC Lateral JFET on a semiinsulating substrate," *IEEE ELECTRON DEVICE LETTERS,* vol. 30, no. 9, pp. 957-959, 2009.

[170] C. F. Huang, J. R. Kuo and C. C. Tsai, "High Voltage (3130 V) 4H-SiC Lateral p-n Diodes on a Semiinsulating Substrate," *IEEE ELECTRON DEVICE LETTERS,* vol. 29, no. 1, pp. 83-85, 2008.

[171] D. J. McGreivy, "On the Origin of Leakage Curnents in Silicon-On-Sapphire MOS transistors," *in IEEE Transactions on Electron Devices,* vol. 24, no. 6, pp. 730-738, 1977.

[172] L.-G. Li, Ö. Vallin, J. Lu, U. Smith, H. Norström, and J. Olsson, "Oxygen out-diffusion from buried layers in SOI and SiC-SOI," *Solid-State Electronics,* vol. 54, no. 2, pp. 153-157, 2010.

[173] M. N. Darwish, "Study of the quasi-saturation effect in VDMOS transistors," *in IEEE Transactions on Electron Devices,* vol. 33, no. 11, pp. 1710-1716, 1986.