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Original citation:
Li, Fan, Vavasour, O., Walker, Marc, Martin, David, Sharma, Yogesh K., Russell, Stephen, Jennings, M. R., Pérez-Tomás, Amador and Mawby, P. A. (Philip A.). (2017) Physical characterisation of 3C-SiC(001)/SiO2 interface using XPS. Materials Science Forum, 897 . pp. 151-154.

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Publisher's statement:
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Published version: https://doi.org/10.4028/www.scientific.net/MSF.897.151

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Physical characterisation of 3C-SiC(001)/SiO_2 interface using XPS

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Keywords: 3C-SiC on Si, MOS, gate threshold, channel mobility, XPS

Abstract. Normally-off MOSFETs were fabricated on 3C-SiC epilayers (Si face) using high temperature (1300 °C) wet oxidation. XPS analysis found little carbon at the MOS interface yet the channel mobility (60 cm^2/V.s) is considerably low. Si suboxides (SiO_x, x<2) exist at the wet oxidised 3C-SiC/SiO_2 interface, which may act as interface traps and degrade the conduction performance.

Introduction

3C-SiC(001) is the only cubic SiC polytype that can be hetero-epitaxially grown on large area Si substrate. Attributed to the smaller band gap (2.3eV), most of interface traps deteriorating the 4H-SiC/SiO_2 interface are in the conduction band of 3C-SiC. Nitridation (NO, N_2O [1, 2]) and hydrogenation (wet O_2, forming gas [1, 3, 4]) processes were previously studied for the 3C-SiC/SiO_2 interface. 3C-SiC on Si lateral MOSFETs were fabricated in our lab using high temperature (1300°C) nitridaiton processes [5], and both direct oxidation and post oxidation annealing in N_2O atmosphere resulted in an improved peak channel field-effect mobility (μ_{FE}) value comparing to O_2 dry oxidised devices. However, a considerable negative threshold voltage was also observed, most likely caused by nitrogen counter doping in the channel region [6]. In this study, we aim to shift the device threshold voltage to positive values by introducing a high temperature (1300°C) wet oxidation process, which was known to not only cause positive threshold voltage shift in the 4H-SiC case [7], but also reduce the interface traps in past low temperature (<1000°C) experiments [1, 3].

Experimental details

Materials used in this study were 4 μm thick n-type epilayers grown on Si(001) substrate via CVD. Lateral MOSFETs with channel dimensions of 150 μm long and 290 μm wide were fabricated to study the effects of various oxidation conditions. Double implantations (Al ~$1x10^{18}cm^{-3}$ for P-body and N ~$5x10^{20}cm^{-3}$ for source & drain) were employed to form the junctions. A high temperature (600°C) and doping level was used for P-body implantation to compensate for the low Al activation rate, since the annealing temperature is limited by the Si melting point 1412°C [8]. Post implantation annealing was conducted at 1375°C for 1 hour in Ar atmosphere without any surface protection caps. After that, all samples went through a solvent clean (acetone, propanol, acetone and methanol), followed by further piranha (H_2SO_4:H_2O_2=3:1) and RCA procedures. Four gate oxidation conditions were studied: O_2 dry oxidation, N_2O direct oxidation, O_2+H_2O wet oxidation, and N_2O direct oxidation followed by a wet post oxidation anneal (POA), all performed at 1300°C. Wet oxygen was prepared by feeding dry oxygen through a bubbler containing DI water heated at 95°C. More detailed parameters are summaried in Table 1. A Ti/Ni (30 nm/100 nm) bilayer was evaporated at low pressure ($2x10^{-7}$ Torr) as source/drain contacts, which were annelaed in RTA furnace at 1000°C for 1min to obtain ohmic behaviours. Finally, 500nm Al was evaporated as the gate contact.

Table 1. Oxidation and post-oxidation annealing process parameters for the MOSFET samples

Sample	Oxidation process	Post-oxidation annealing	Oxide thickness (nm)	Threshold field (MV/cm)	Peak field-effect mobility (cm^2/V.s)
1	5 slm diluted dry O_2 (O_2:Ar=1:4) at 1300°C for 30 mins	None	≈32	≈-0.25	≈70
2	5 slm diluted N_2O (N_2O:Ar=1:4) at 1300°C for 120 mins	None	≈98	≈-3.75	≈88
3	5 slm diluted wet O_2 (O_2:Ar=1:4) at 1300°C for 20 mins	None	≈92	≈1	≈60
4	5 slm diluted N_2O (N_2O:Ar=1:4) at 1300°C for 90 mins	5 slm diluted wet O_2 (O_2:Ar=1:4) at 1300°C for 10 mins	≈75	≈-2	≈58

Results and Discussions

Typical turn-on behaviours of fabricated MOSFETs are shown in Fig .1. Due to the different oxide thickness, the drain current is plotted against the gate field for direct comparisons. Considerable leakage currents were observed for all devices in previous experiments [5] and reproduced here, as a result of the high density of stacking faults in the channel region [9]. It can be seen in Fig. 1 that the dry oxidized device (square) readily behaves as normally-on device with a gate threshold close to zero (≈-0.25 MV/cm). This agrees with the "Carbon Cluster Model" [10] which describes that only donor-like states are present at the 3C-SiC/SiO_2 interfac. Since they are positively charged when empty, these donor-like states should be responsible for the inherent negative threshold. Ther nitrided sample (circle) has an even more negative threshold (≈-3.75 MV/cm) due to the channel counter doping effect [6], while the wet oxidized sample (upper triangle) has the most positive gate threshold (≈1 MV/cm). A combination of N_2O nidridation and wet POA led to an intermediate threshold around -2 MV/cm. It is obvious that the high temperature (1300°C) wet oxygen processing successfully shifted the gate threshold to a more positive value, either by reducing the positive fixed charges in the bulk oxide or by bringing in extra negative charges. Nevertheless, fixed charges should not have big influences on the device on-state conduction. However, by plotting the field-effect mobility curves against the gate field in Fig. 2, it can be seen that both wet oxidized and wet POA processed samples have a peak μ_{FE} value around 60 cm^2/V.s, which is lower than the dry oxidized sample by 10 cm^2/V.s and the N_2O nitrided sample by 30 cm^2/V.s.

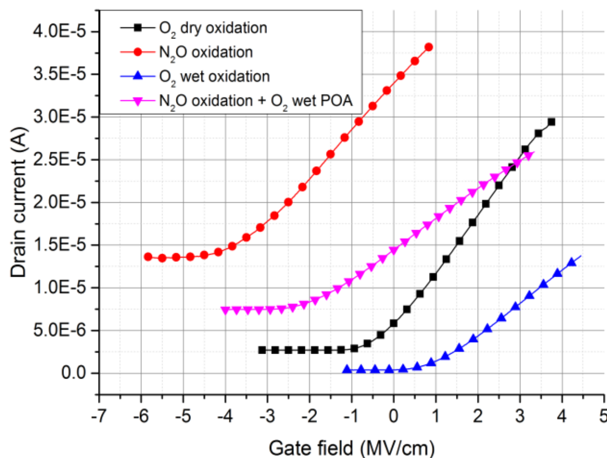

Fig. 1. Transfer curves for 1300°C oxidized devices with various conditions (V_{ds}=0.1 V).

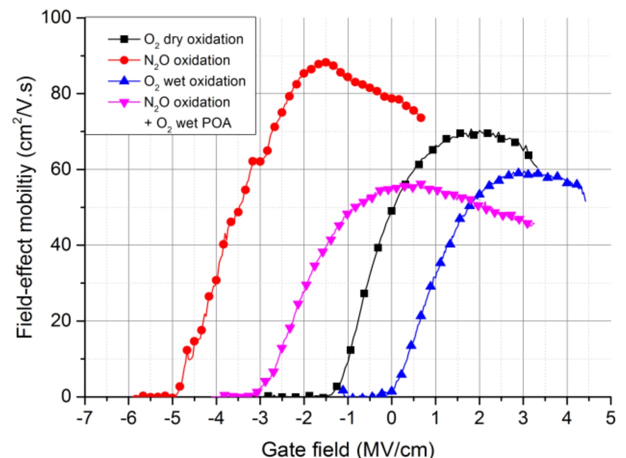

Fig. 2. Peak field-effect mobility of 1300°C oxidized devices with various conditions.

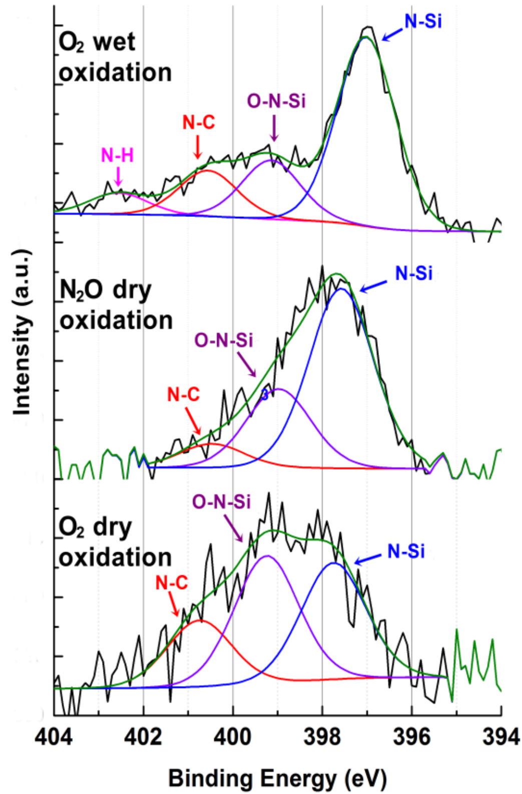

Fig. 3. N 1s XPS spectrum with possible bonds assignments for various oxidation conditions.

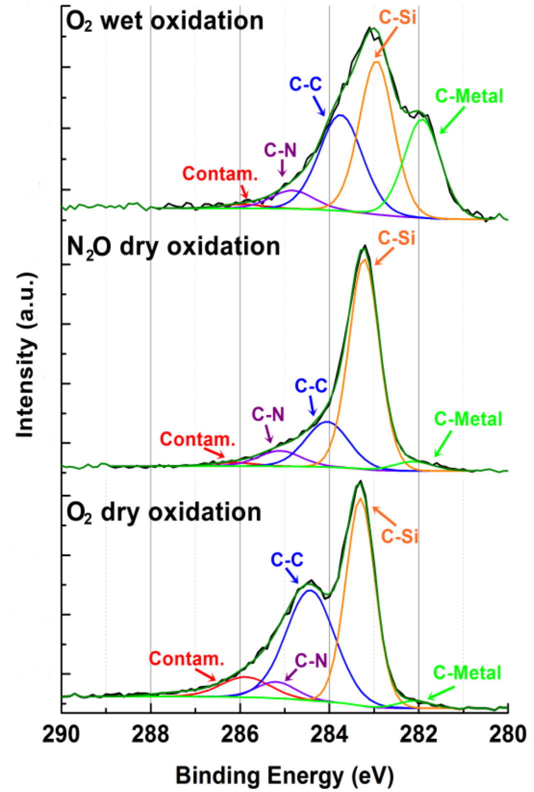

Fig. 4. C 1s XPS spectrum with possible bonds assignments for various oxidation conditions.

X-ray photoelectron spectroscopy (XPS) was applied to the 3C-SiC/SiO_2 interfaces for a more in-depth study of chemical bonds. Al gates were completely removed by phosphoric acid, and the gate oxide was thinned to below 10 nm by Ar sputtering in the XPS chamber. The measurements were then performed in the channel regions. The noticeable shift of N-Si and C-C peaks in Fig. 3 and Fig. 4 can be explained by the charging of the remaining SiO_2 on the sample surface [11]. The N 1s spectrum (Fig. 3) suggests N bonds exist at the 3C-SiC/SiO_2 interface of all samples, 0.58% (dry), 1.01% (N_2O), and 1.78% (wet). N in the non-intentionally nitrided samples most likely comes from the residual air (N_2) left in the furnace before the oxidation process started. The reason why the wet oxidised sample has the highest N bonds concentration may be due to the fact that it has the highest oxide growth rate, thus much more free Si bonds being exposed at a time, and in this situation oxygen alone may not be sufficient to passivate all the free Si bonds, resulting in nitrogen and hydrogen being incorporated. Fig. 3 unveils an extra high energy (~402.5 eV) N bond (magenta peak) at the wet oxidised interface. Excluding the possibility of nitrogen bonded to organics, this peak most likely refers to an N-H bond. By calculating the area under the C-C peak in the C 1s spectrum (Fig. 4) and divided by the whole XPS survey area (not shown here), C-C bond concentrations at the MOS interface were estimated to be 15.81% (dry), 5.44% (N_2O), and 2.51% (wet). A reduction of C-C bonds should mean fewer interface traps and higher channel mobility, as is the case for the dry and N_2O oxidised samples. Conversely, the wet oxidised sample does not follow the rule, instead the MOS interface presents the fewest C-C bonds while lowest mobility value. From the ideal ratio: Si/C=1 (SiC) and Si/O=0.5 (SiO_2), theoretical Si 2p bonds required for the experimental XPS C 1s and O 1s data are calculated and shown in Table 2. Comparing the experimental Si 2p data and the calculated data, it can be seen that, for dry oxidised sample, the actual Si 2p bonds are fewer than required, indicating that there are extra C-C bonds as mentioned. The nitrided sample has an almost stoichiometric interface (42.06%≈41.64. The wet oxidised interface, however, is Si rich, which agrees with previous assumption that high oxidation rate leads to the formation of Si suboxide or extra Si dangling bonds. Si suboxides are known to contribute to interface traps within the band gap close to

the conduction band of 4H-SiC [12, 13] and it seems to have a great impact on 3C-SiC as well, even with a smaller band gap.

Table 2. Chemical bonds concentration at the studied 3C-SiC/SiO_2 interfaces

Sample	C 1s	O 1s	N 1s	Si 2p	Theoretical Si 2p needed
O_2 dry oxidised	39.95%	21.12%	0.58%	38.36%	50.51% (C rich)
N_2O dry oxidised	26.64%	29.99%	1.01%	42.06%	41.64% (stoichiometric)
O_2 wet oxidised	8.45%	36.57%	1.78%	53.2%	26.74% (Si rich)

Summary

In this work we investigated the electrical and chemical properties of 3C-SiC/SiO_2 interfaces oxidised by dry O_2, N_2O and wet O_2, all at a high temperature of 1300 °C. The wet oxidation or wet post oxidation annealing successfully shifted the inherent negative threshold of 3C-SiC MOS devices to more positive values, however, accompanied with a degradation of the peak channel mobility: 14.3% lower than the dry oxidised sample and 33.3% comparing to the nitrided sample. It was revealed by the XPS analysis that, the high temperature wet oxidation led to the formation of Si suboxide, which may have acted as extra interface traps, even though the more conventional traps caused by C-C bonds are greatly reduced.

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